

EE599_Assignment1

Zixi Gu

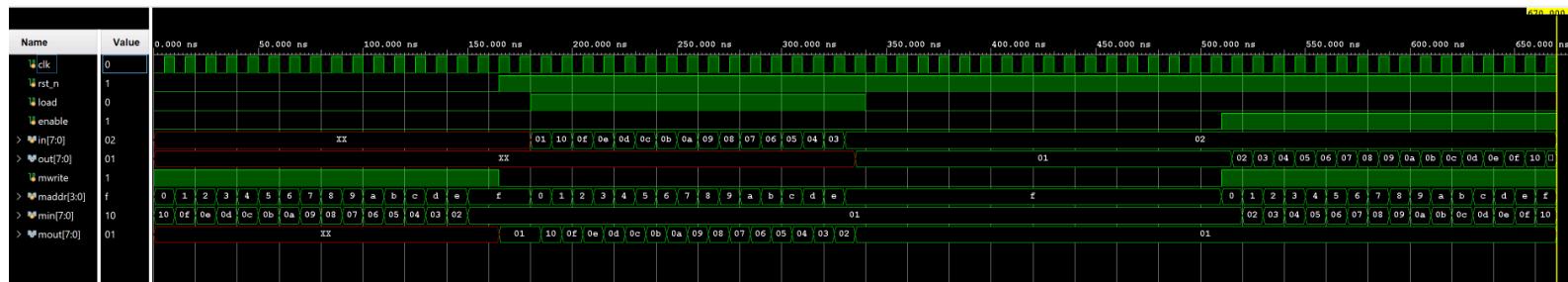
Q1:odd_even

Q2:Matrix-Matrix Multiplication

Git: https://github.com/Go0zx/EE599_ZixiGu_6974574312.git

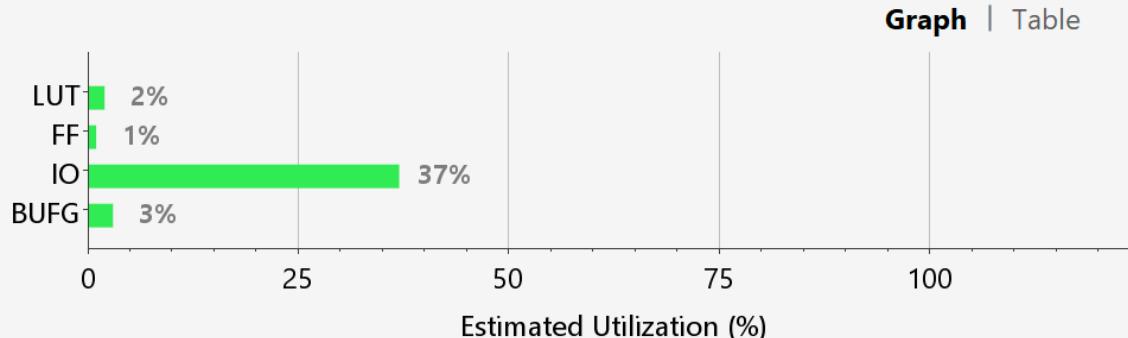
odd_even

16 (clk period = 5ns)



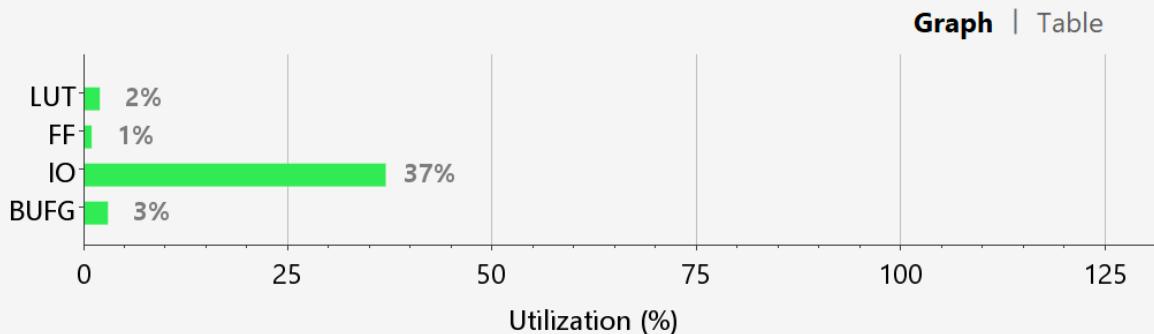
Utilization

Post-Synthesis | Post-Implementation



Utilization

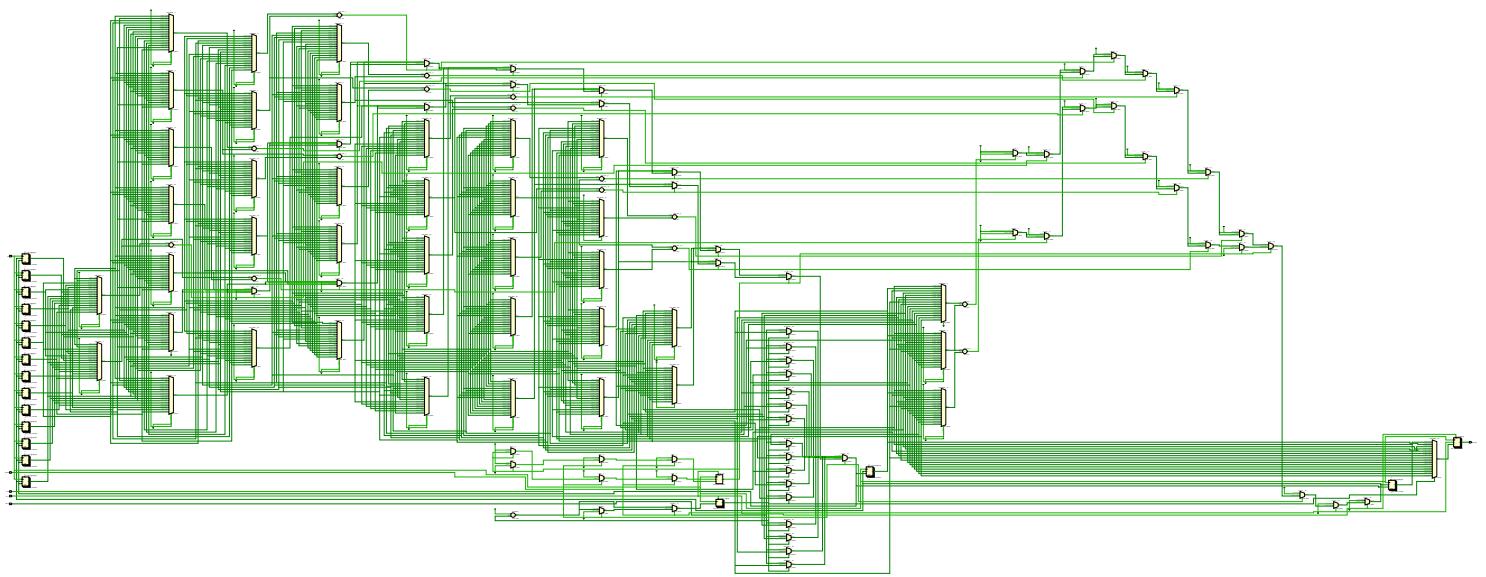
Post-Synthesis | Post-Implementation

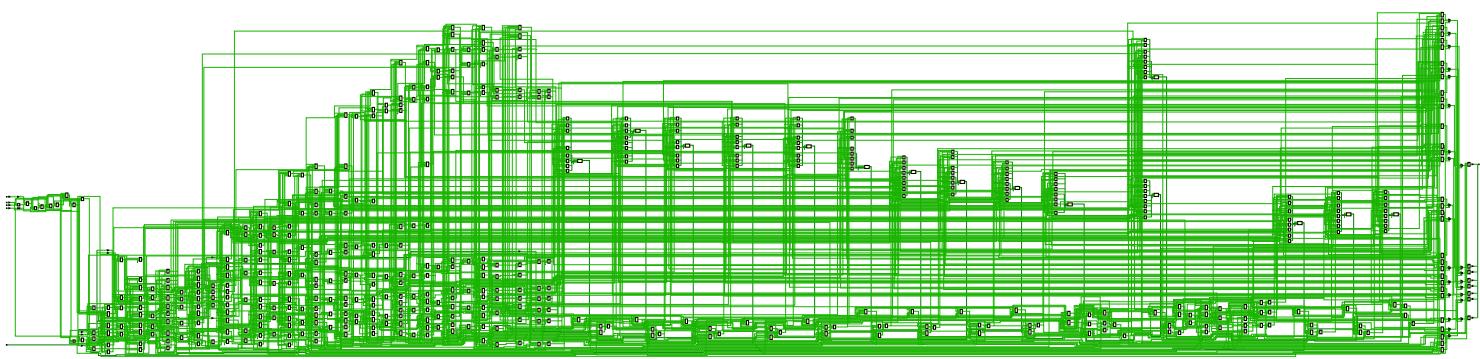


Design Timing Summary

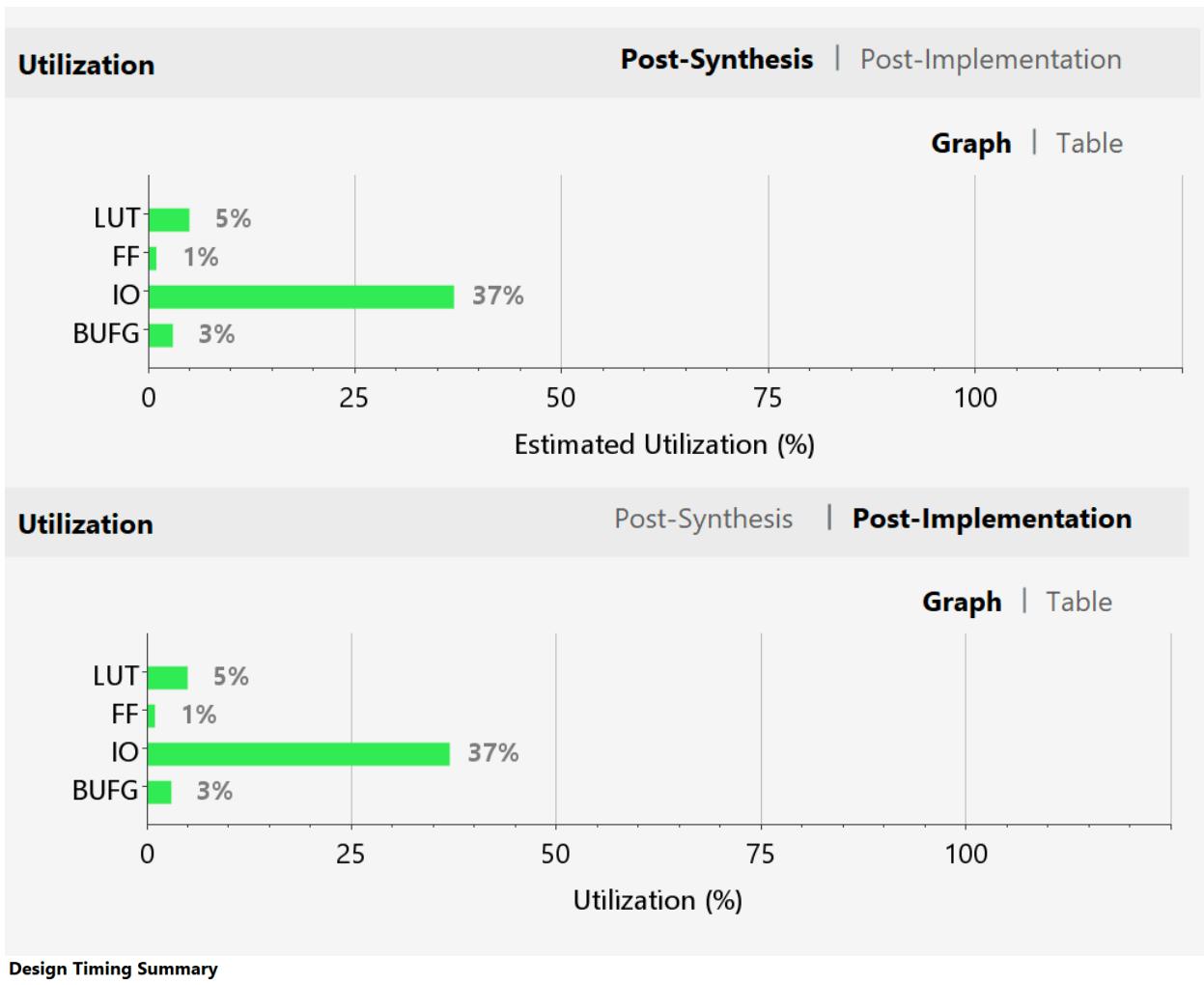
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 1.094 ns	Worst Hold Slack (WHS): 0.163 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 269	Total Number of Endpoints: 269	Total Number of Endpoints: 142

All user specified timing constraints are met.



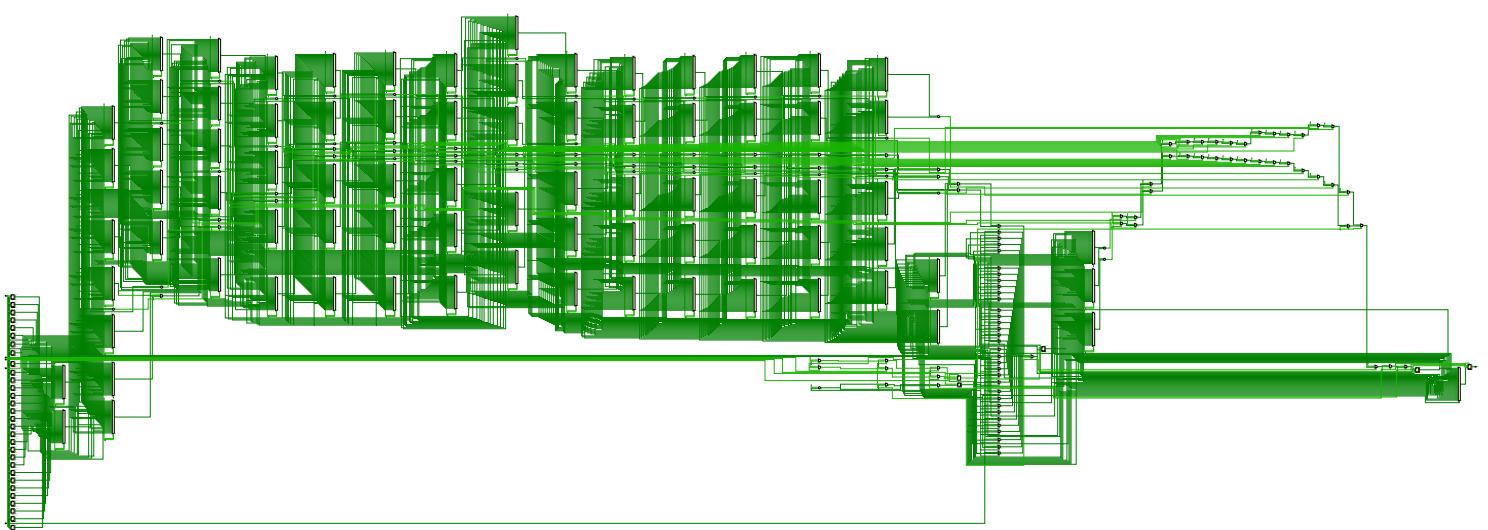


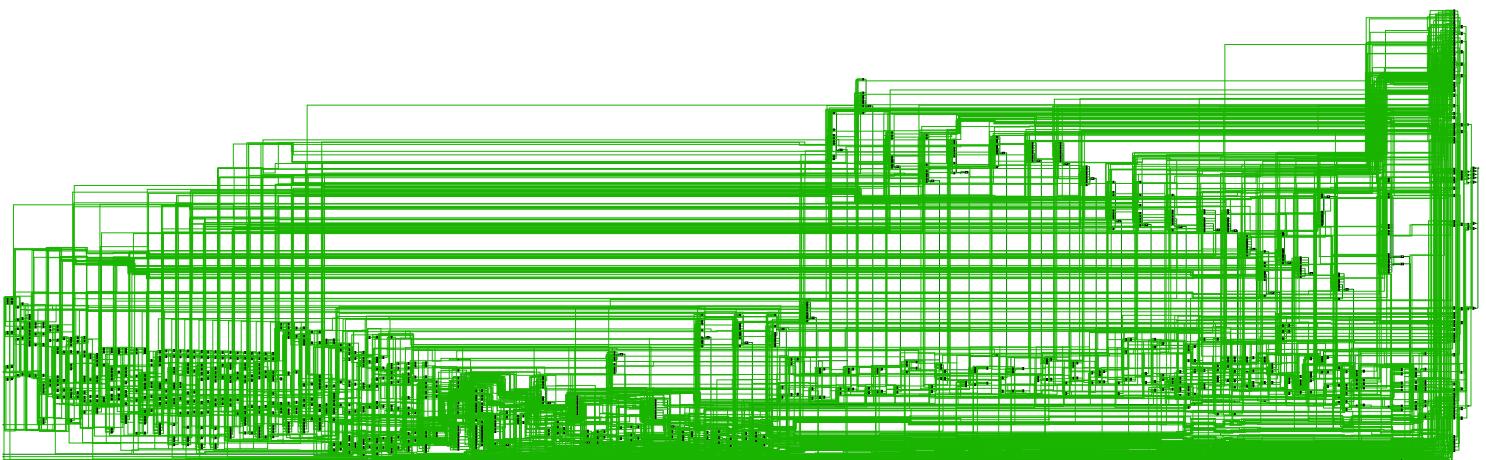
32 (clk period = 5ns)



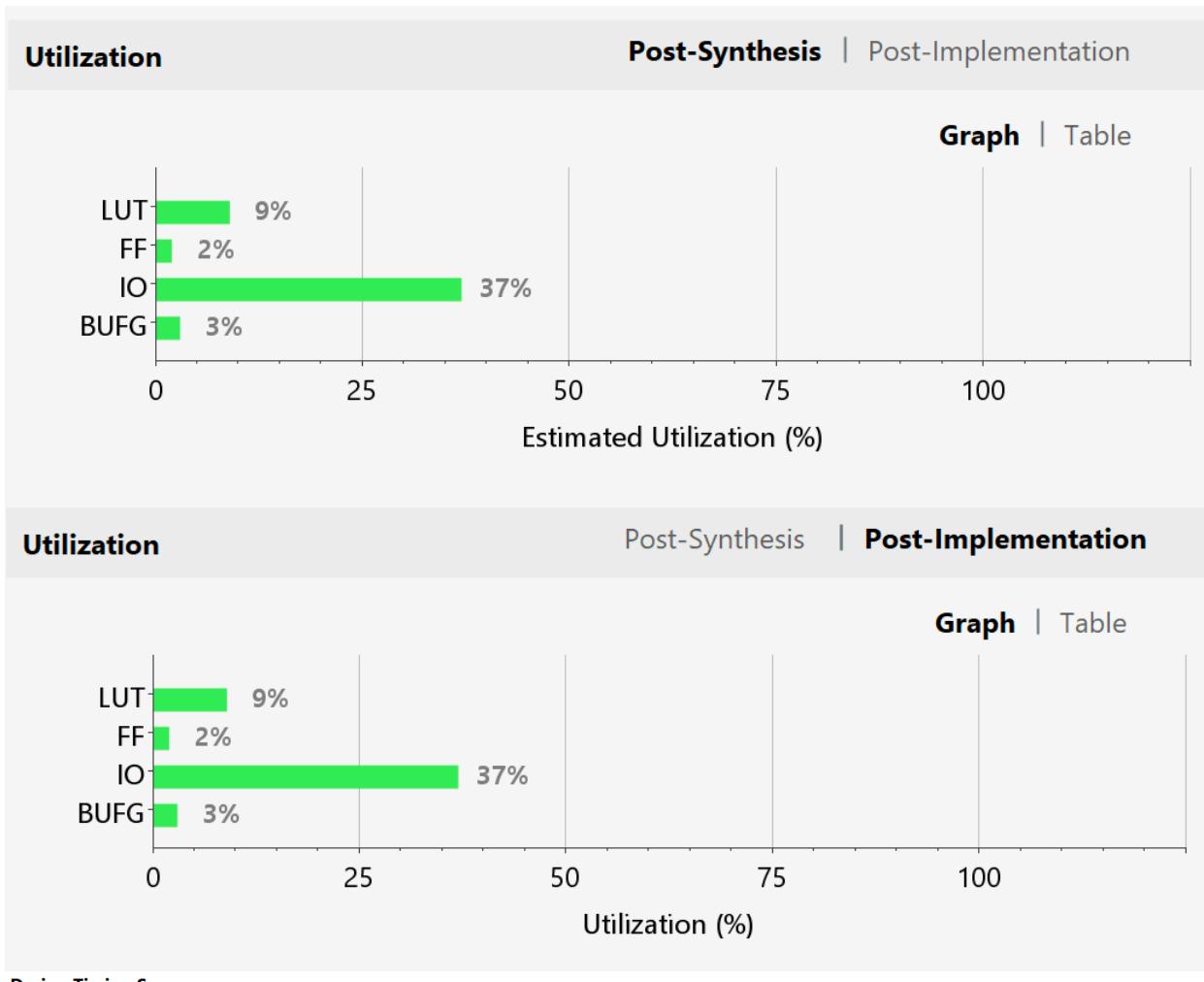
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 1.027 ns	Worst Hold Slack (WHS): 0.166 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 534	Total Number of Endpoints: 534	Total Number of Endpoints: 279

All user specified timing constraints are met.





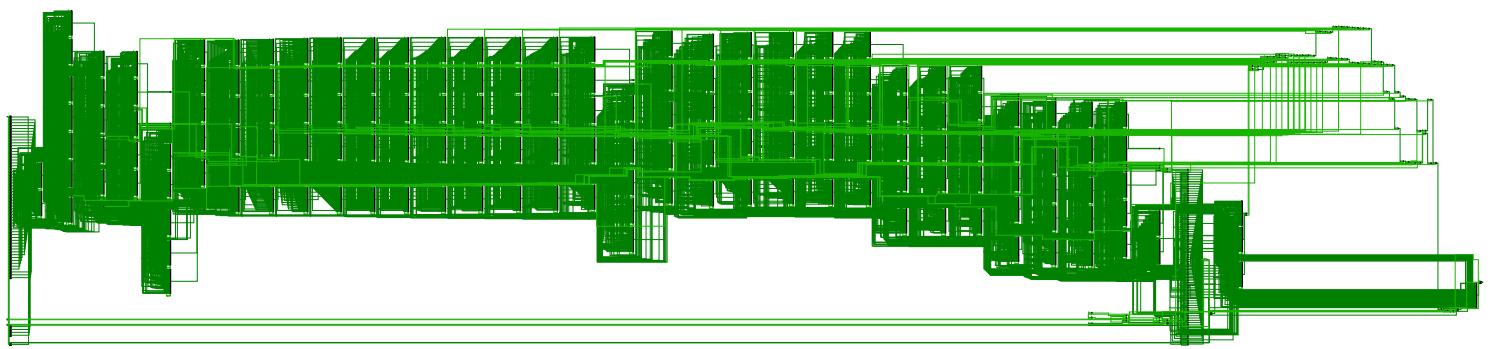
64 (clk period = 5ns)

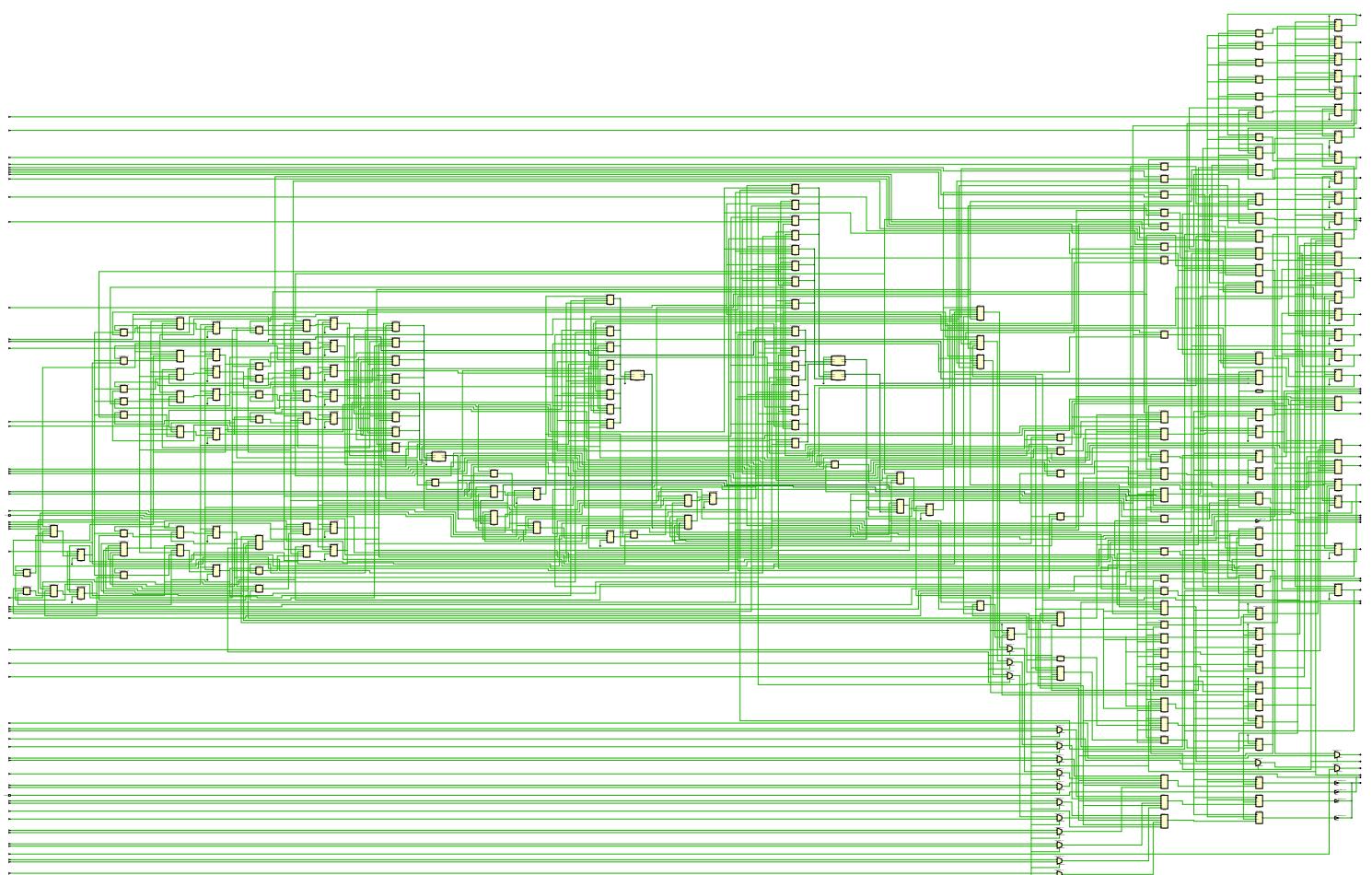


Design Timing Summary

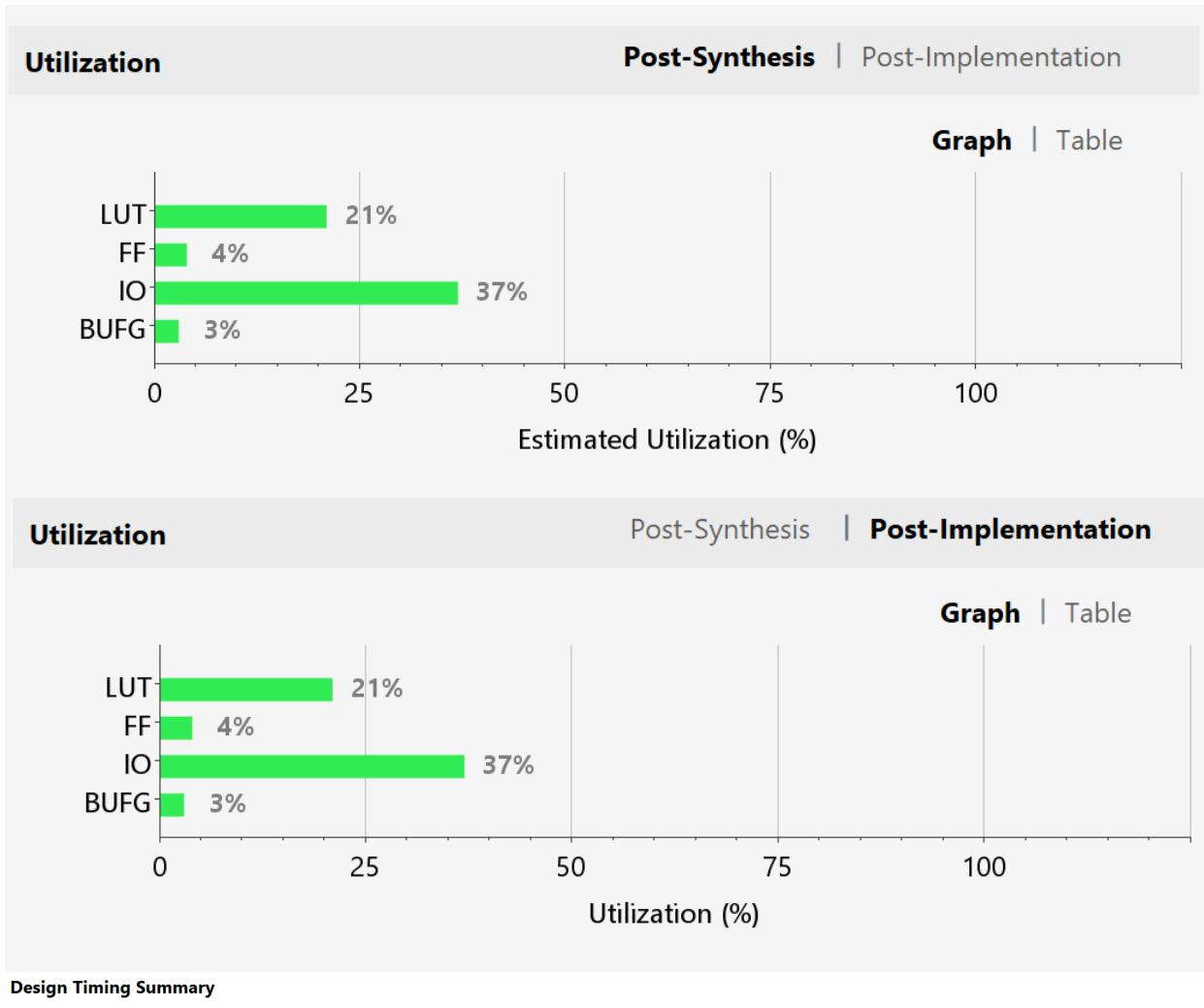
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 1.053 ns	Worst Hold Slack (WHS): 0.212 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 1047	Total Number of Endpoints: 1047	Total Number of Endpoints: 536

All user specified timing constraints are met.





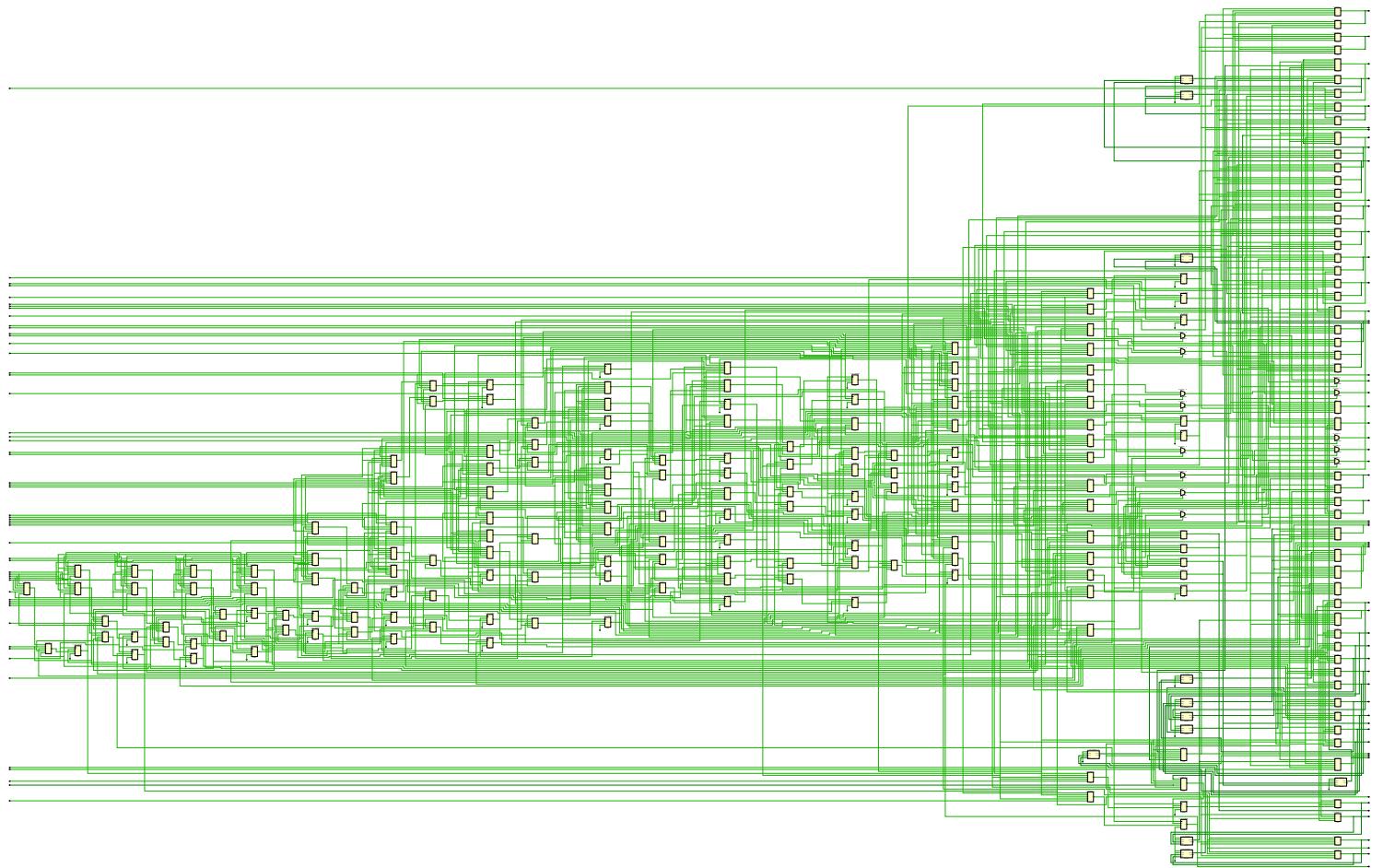
128 (clk period = 5ns)



Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.333 ns	Worst Hold Slack (WHS): 0.128 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 2101	Total Number of Endpoints: 2101	Total Number of Endpoints: 1078

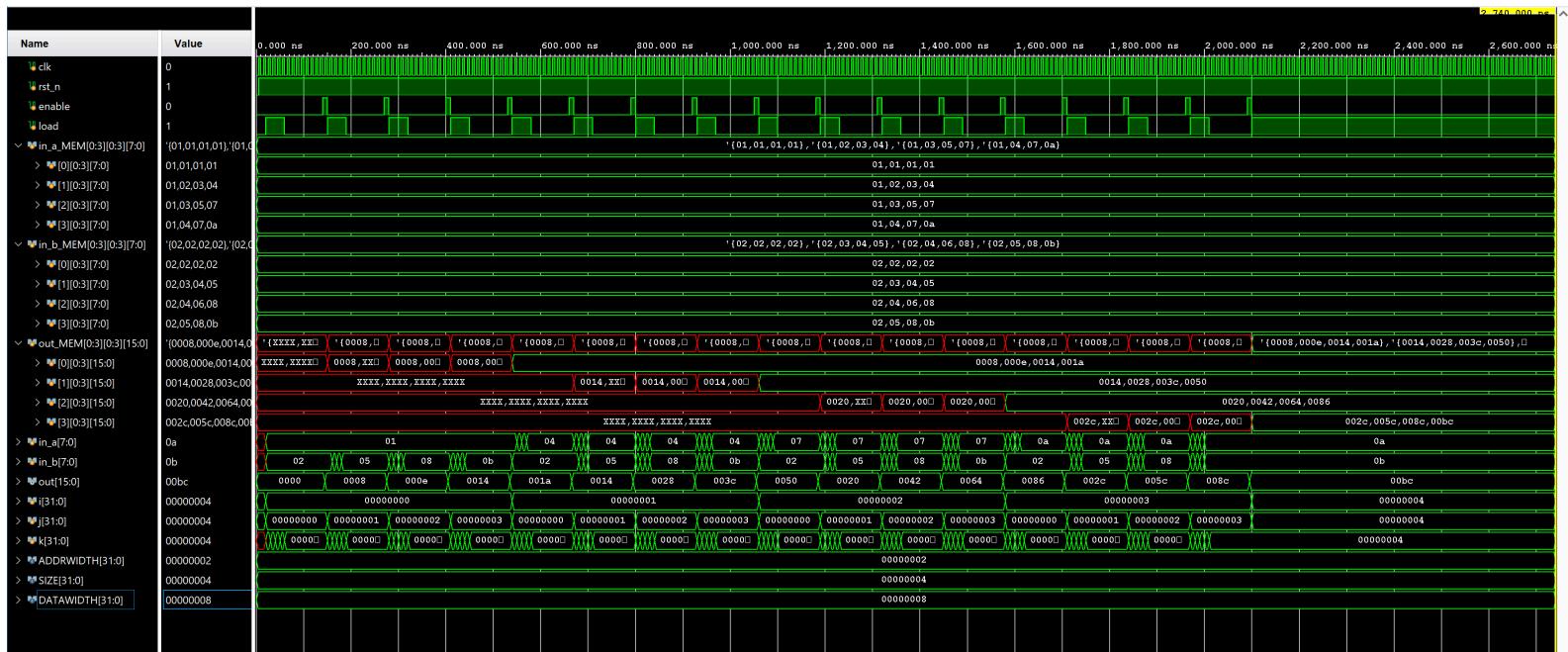
All user specified timing constraints are met.





Matrix-Matrix Multiplication

4*4 (clk period = 5ns)

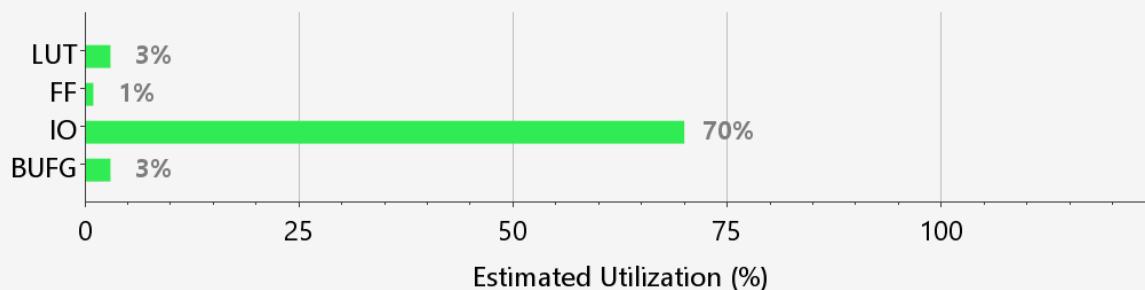


in_a_MEMORY[0:3][0:3][7:0]	{1,1,1,1},{1,2,3,4},{1,3,5,7},{1,4,7,10}	Array
> [0][0:3][7:0]	1,1,1,1	Array
> [1][0:3][7:0]	1,2,3,4	Array
> [2][0:3][7:0]	1,3,5,7	Array
> [3][0:3][7:0]	1,4,7,10	Array
in_b_MEMORY[0:3][0:3][7:0]	{2,2,2,2},{2,3,4,5},{2,4,6,8},{2,5,8,11}	Array
> [0][0:3][7:0]	2,2,2,2	Array
> [1][0:3][7:0]	2,3,4,5	Array
> [2][0:3][7:0]	2,4,6,8	Array
> [3][0:3][7:0]	2,5,8,11	Array
out_MEMORY[0:3][0:3][15:0]	{8,14,20,26},{20,40,60,80},{32,66,100,134},{44,92,140,188}	Array
> [0][0:3][15:0]	8,14,20,26	Array
> [1][0:3][15:0]	20,40,60,80	Array
> [2][0:3][15:0]	32,66,100,134	Array
> [3][0:3][15:0]	44,92,140,188	Array

Utilization

Post-Synthesis | Post-Implementation

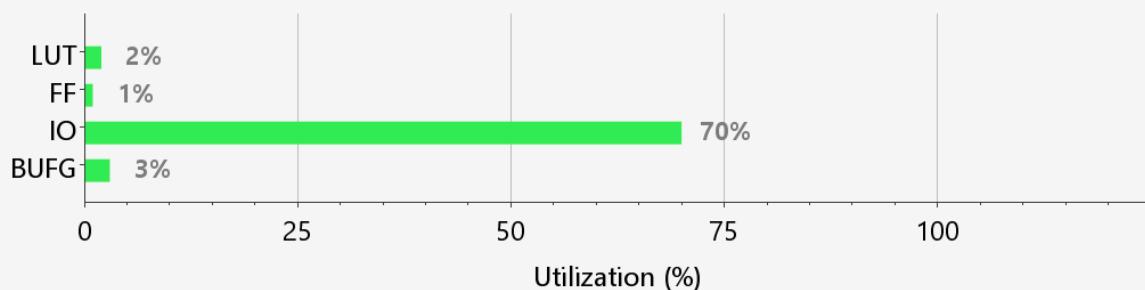
[Graph](#) | [Table](#)



Utilization

Post-Synthesis | Post-Implementation

[Graph](#) | [Table](#)



Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.078 ns	Worst Hold Slack (WHS): 0.160 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 199	Total Number of Endpoints: 199	Total Number of Endpoints: 200

All user specified timing constraints are met.

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:

0.125 W

Design Power Budget:

Not Specified

Power Budget Margin:

N/A

Junction Temperature:

26.4°C

Thermal Margin:

58.6°C (5.0 W)

Effective θJA:

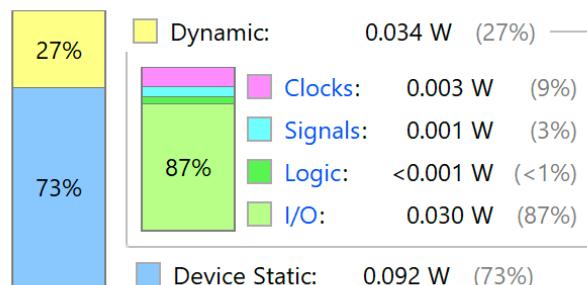
11.5°C/W

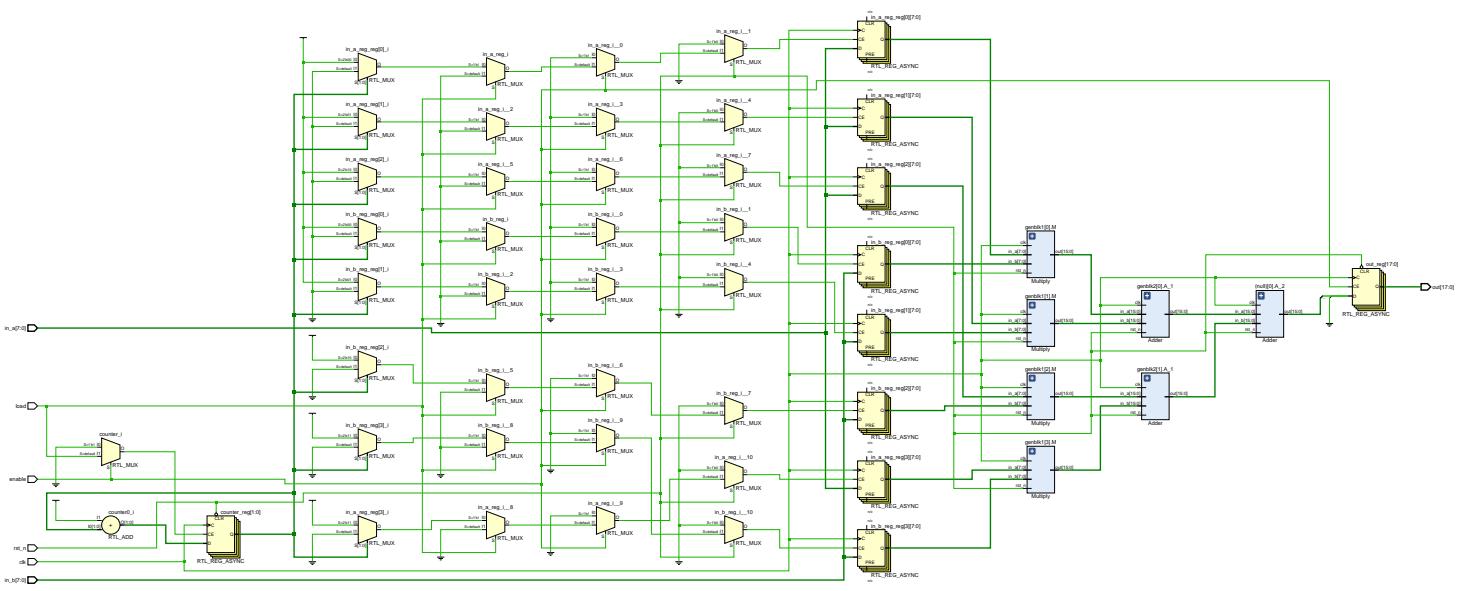
Power supplied to off-chip devices: 0 W

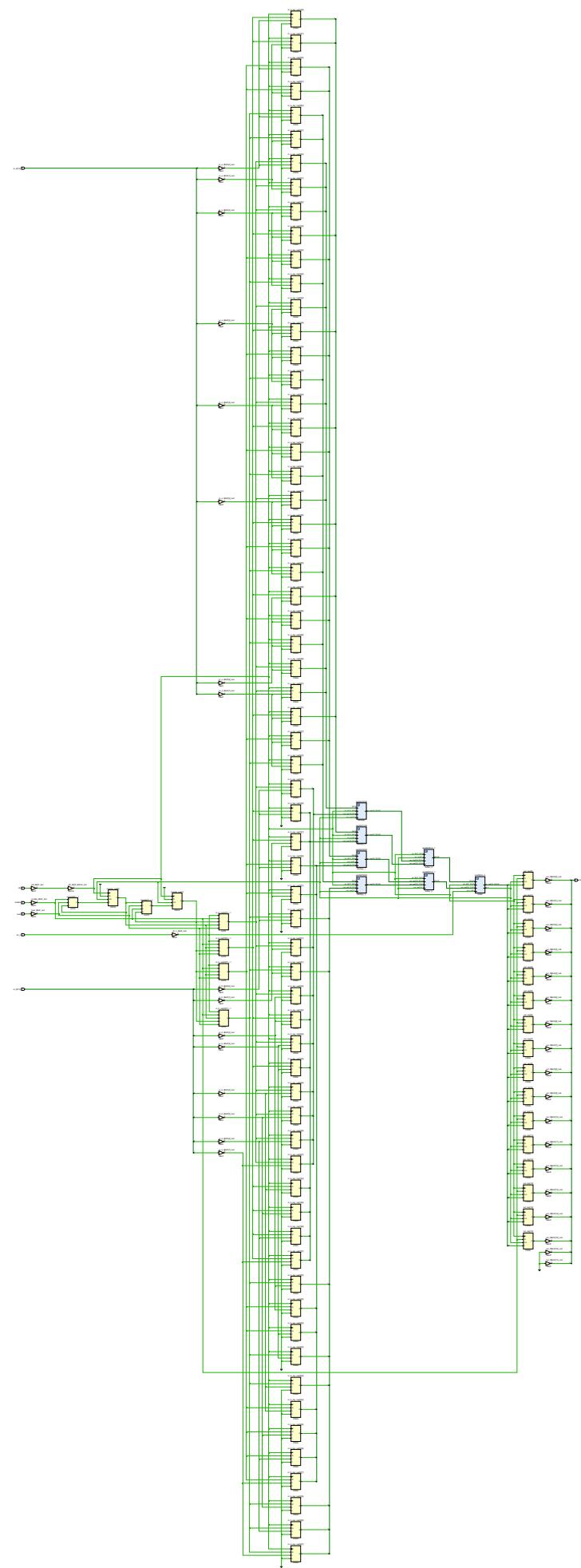
Confidence level: **Low**

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

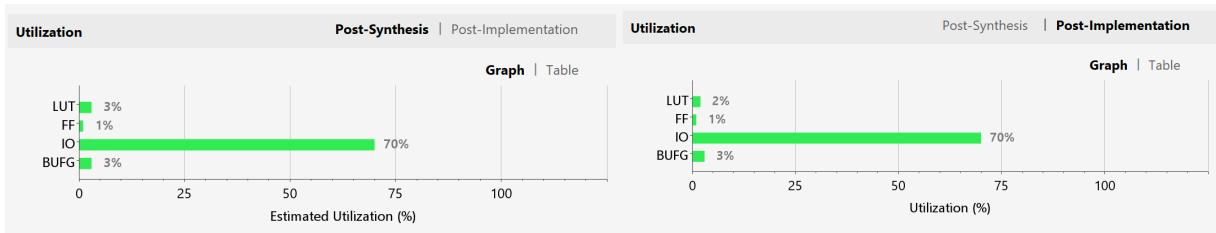
On-Chip Power





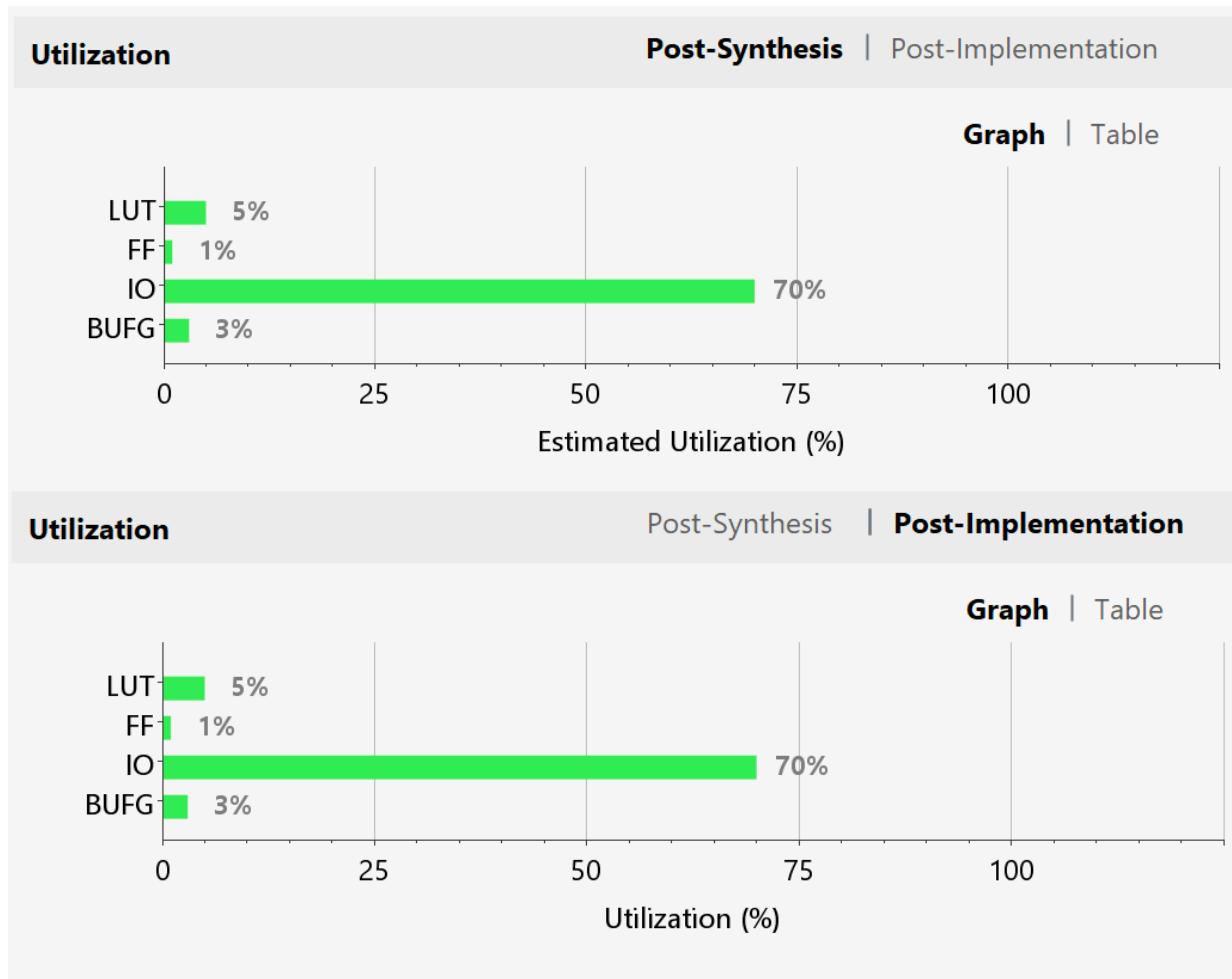


How many of parallel MulandAddTrees can be implemented in this FPGA
(Provide resource utilization reports with parallel MulandAddTrees)?



For 4*4 Matrix, the maximum number of parallel MulandAddTrees is between 33 and 50.

8*8 (clk period = 5ns)



Design Timing Summary

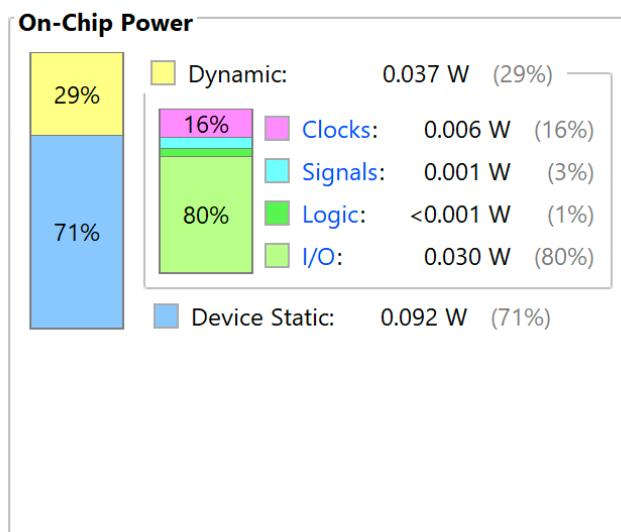
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.000 ns	Worst Hold Slack (WHS): 0.155 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns

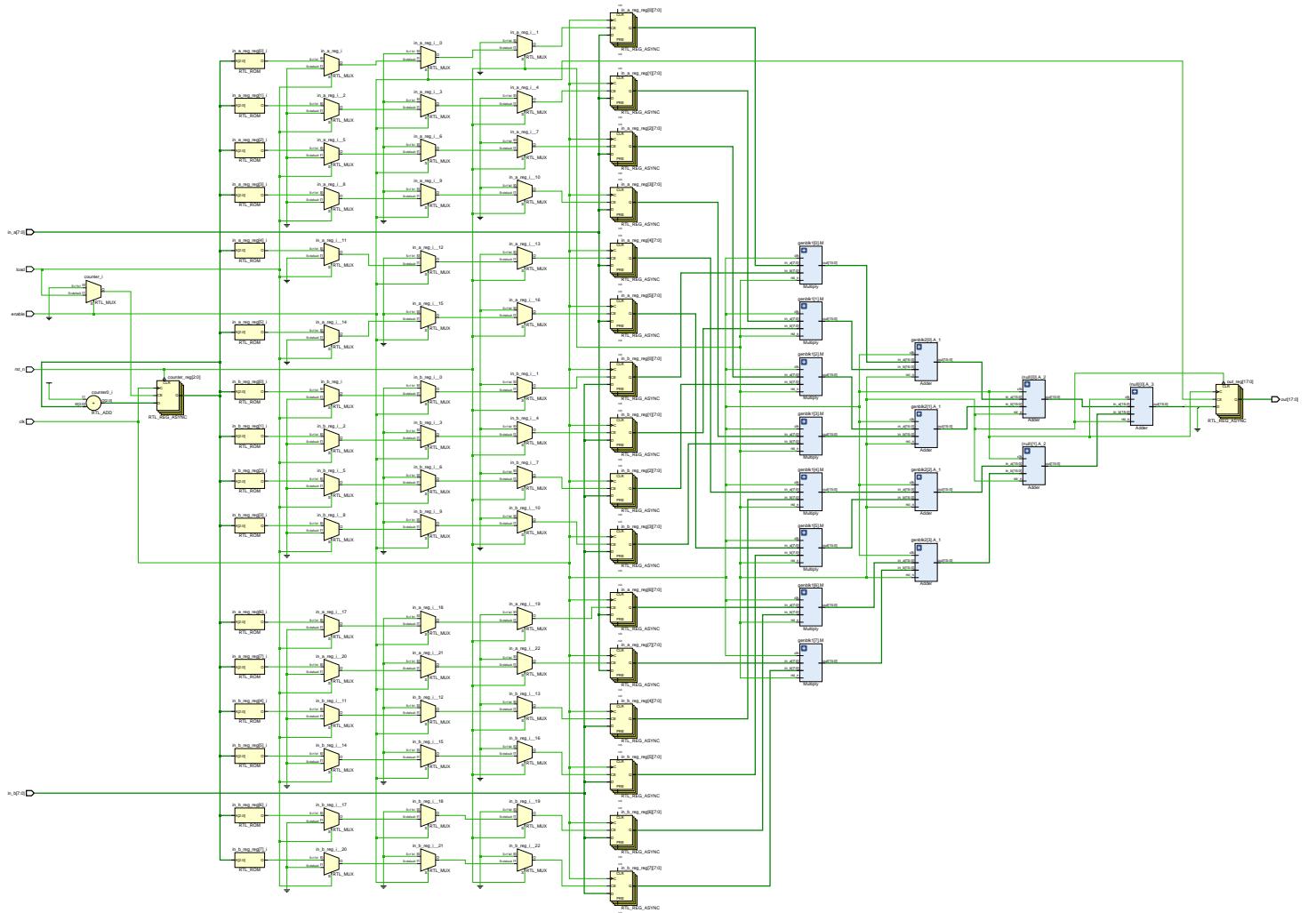
Summary

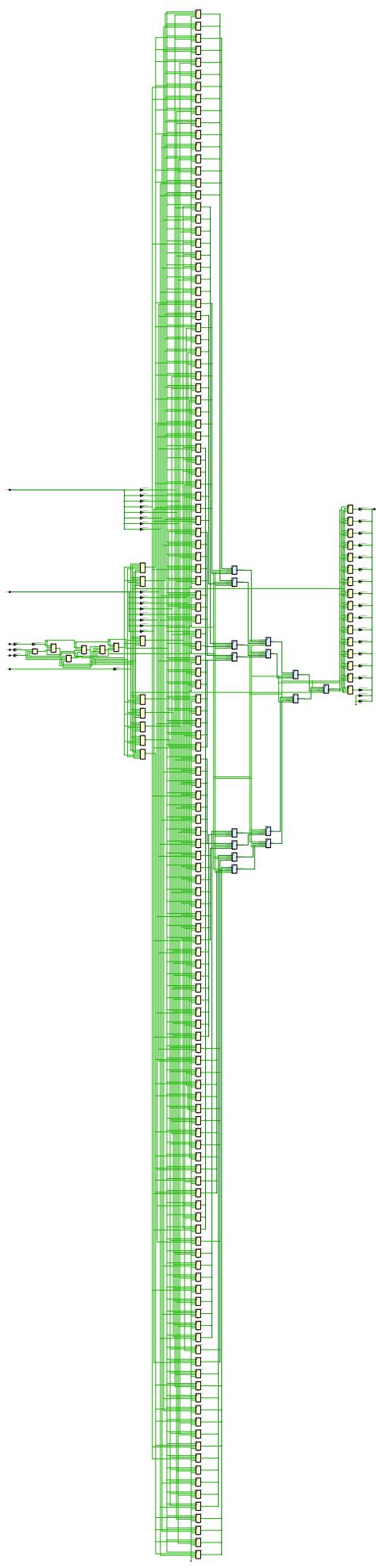
Power analysis from implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	0.129 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	26.5°C
Thermal Margin:	58.5°C (5.0 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

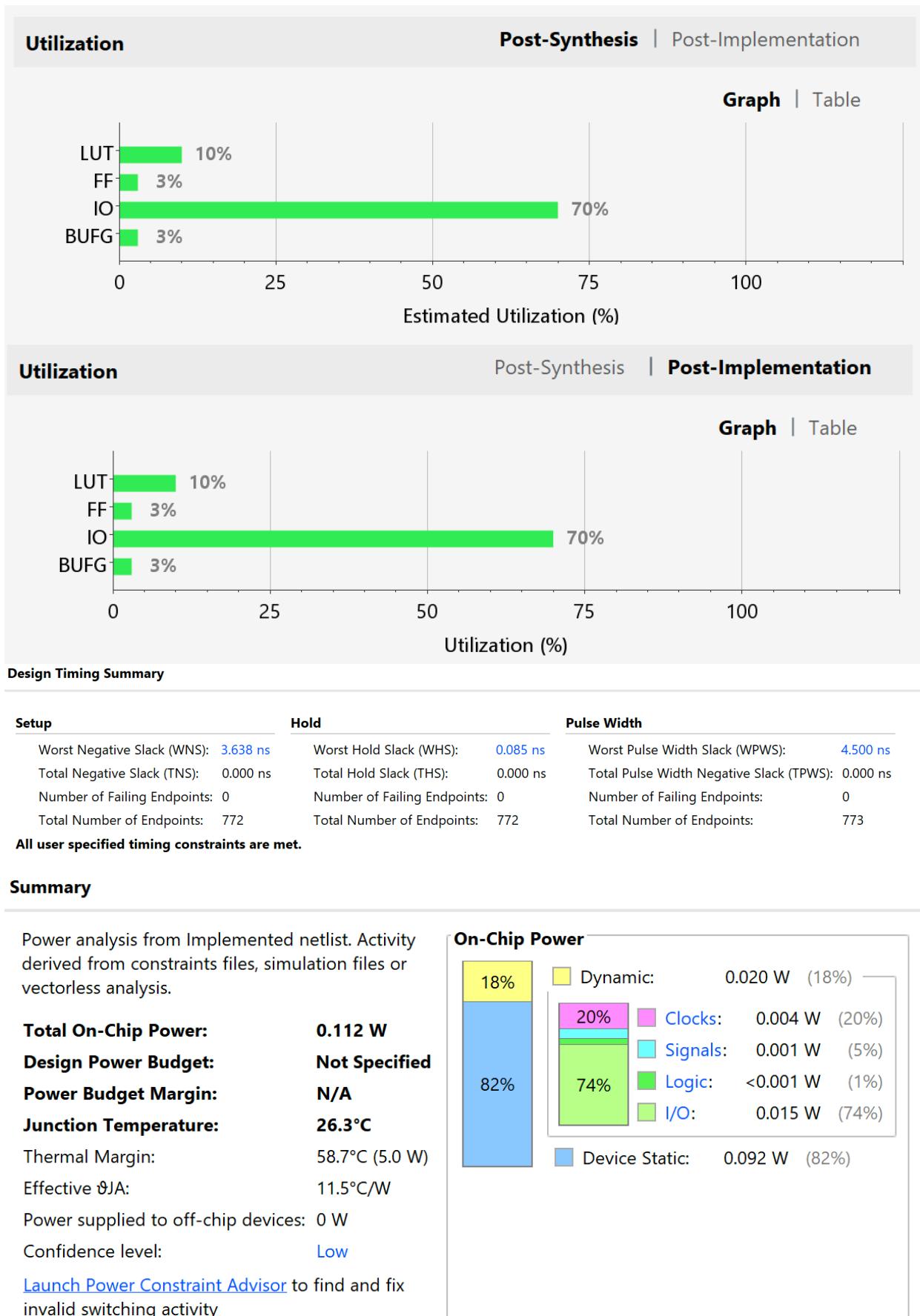
[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

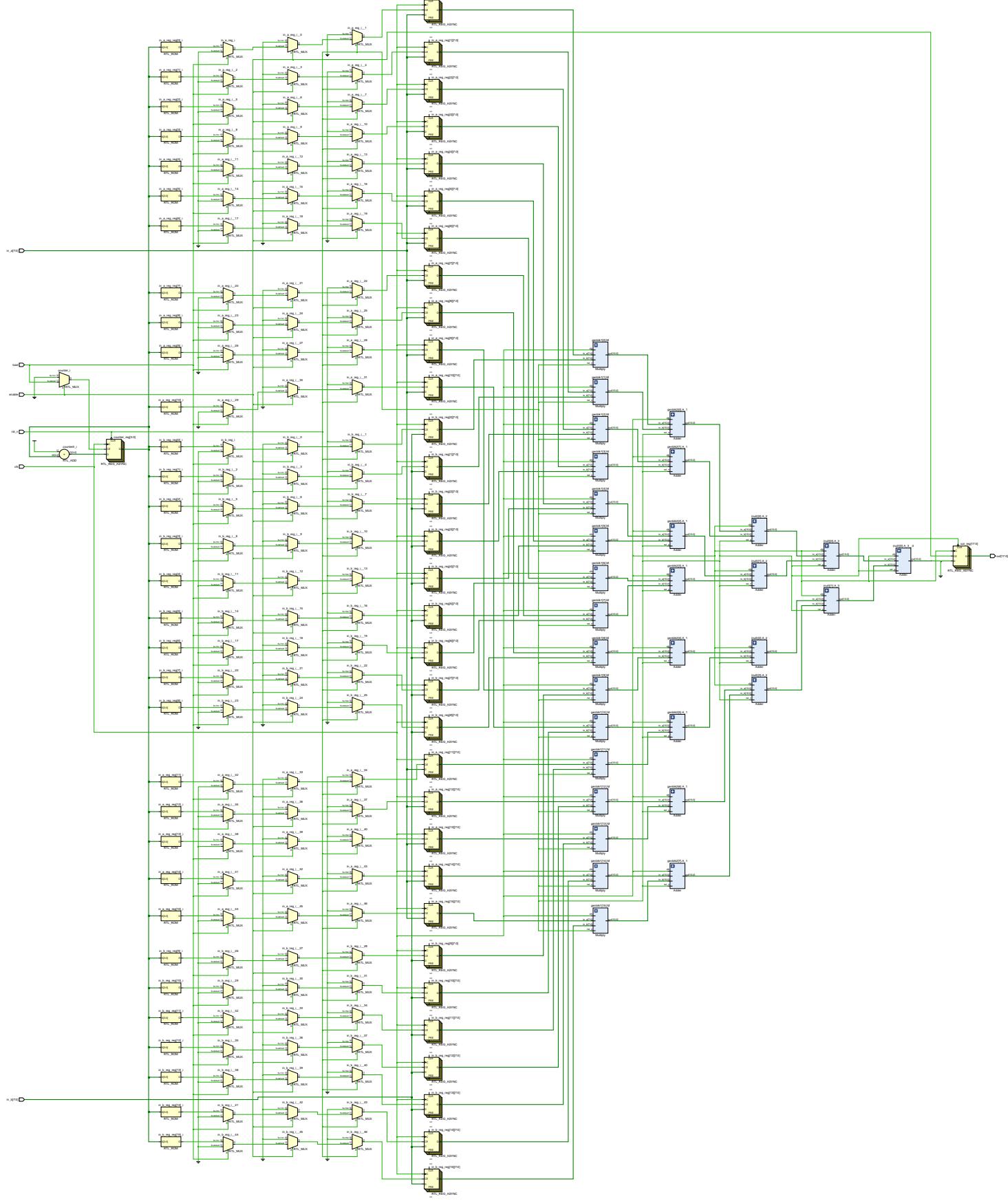


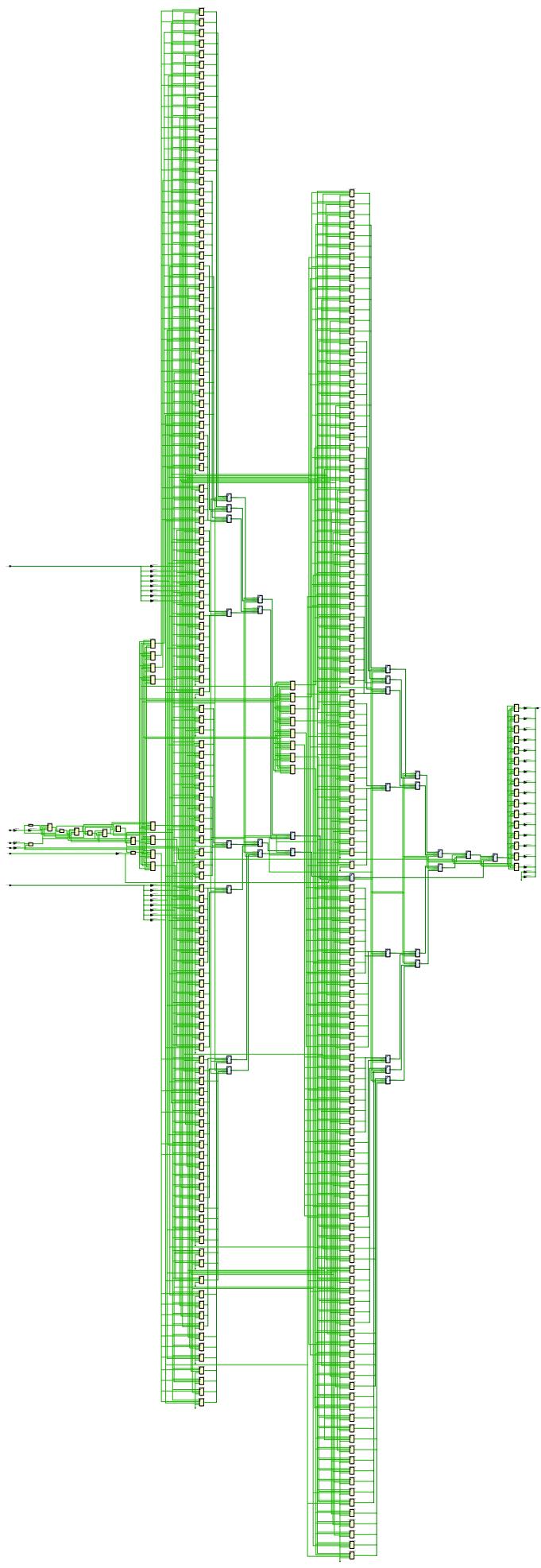




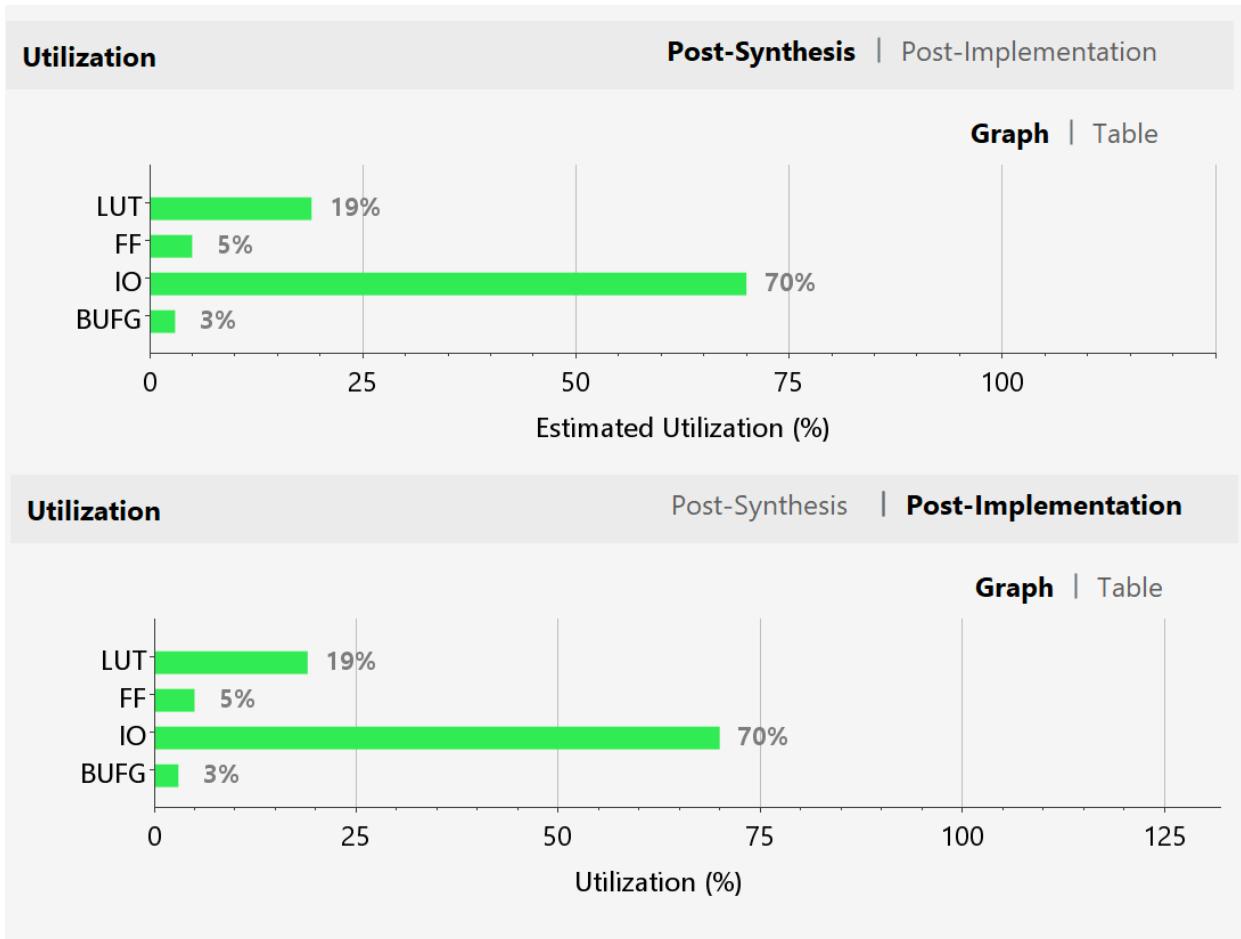
16*16 (clk period = 10ns)







32*32 (clk period = 10ns)



Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.582 ns	Worst Hold Slack (WHS): 0.080 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 1541	Total Number of Endpoints: 1541	Total Number of Endpoints: 1542

All user specified timing constraints are met.

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	0.117 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	26.3°C
Thermal Margin:	58.7°C (5.0 W)
Effective θ _{JA} :	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low
Launch Power Constraint Advisor to find and fix invalid switching activity	

