

# COMSM1302

## Overview of Computer Architecture

### Lecture 9

### ModuleSim

# In the previous lecture

1. Computer systems layers.
2. 4-bit CPU from 4-bit counter.
3. ModuleSim simulation software

# In this lecture



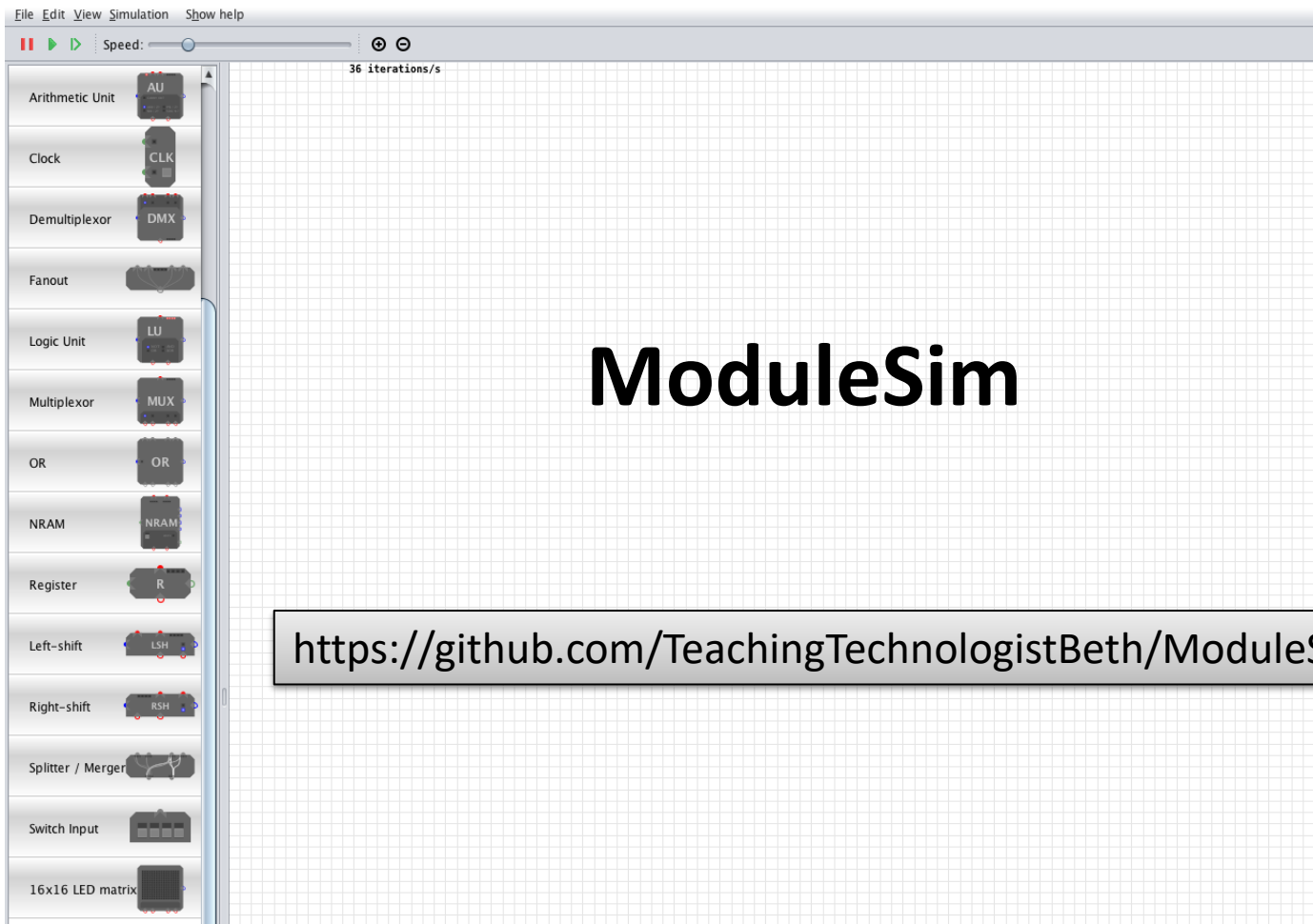
## 1. Modulesim

1. Bus in Modulesim
2. Different components in ModuleSim
3. Solve some design problems

## 2. At the end of this lecture:

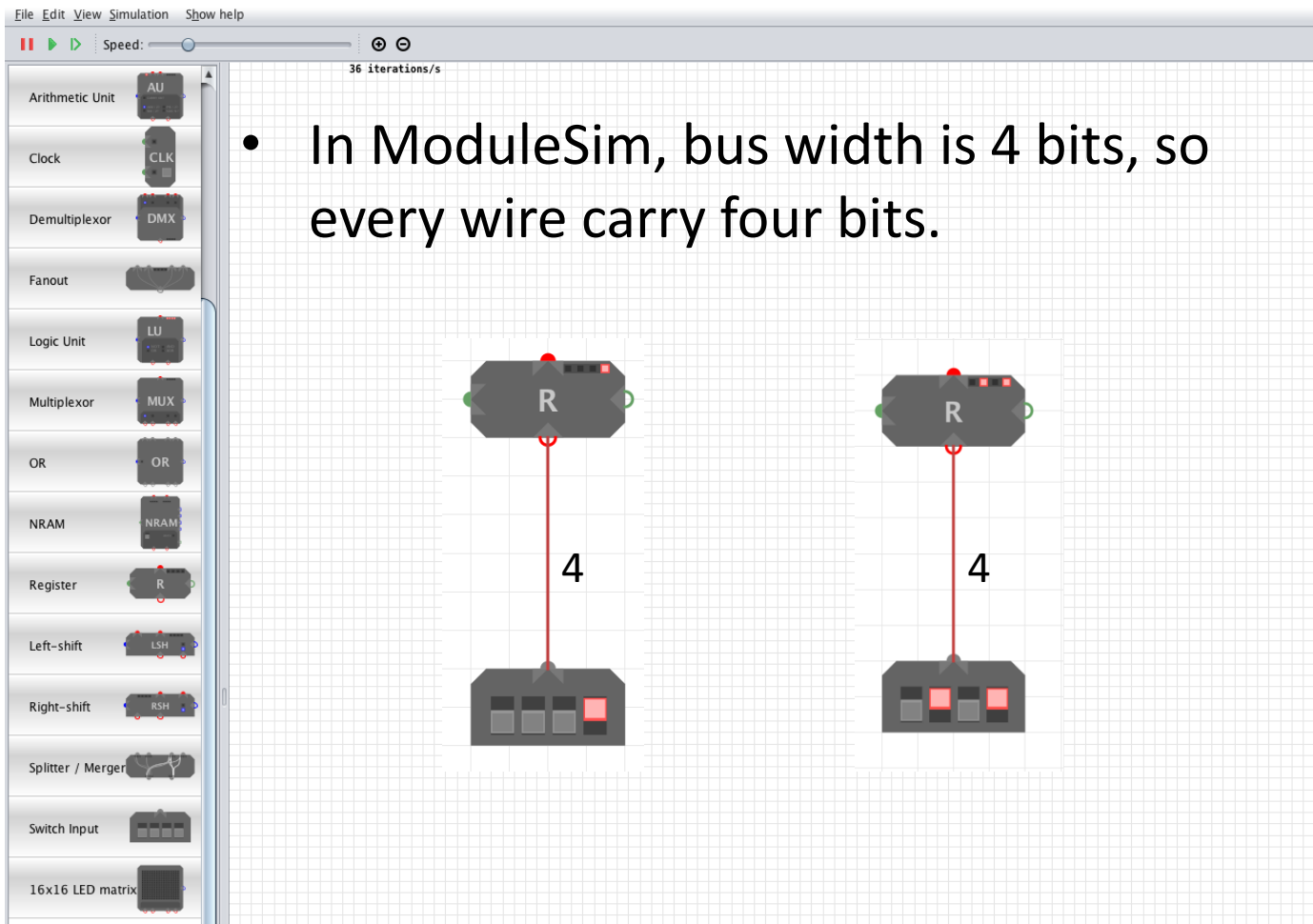
1. To use ModuleSim to implement and test your designs.

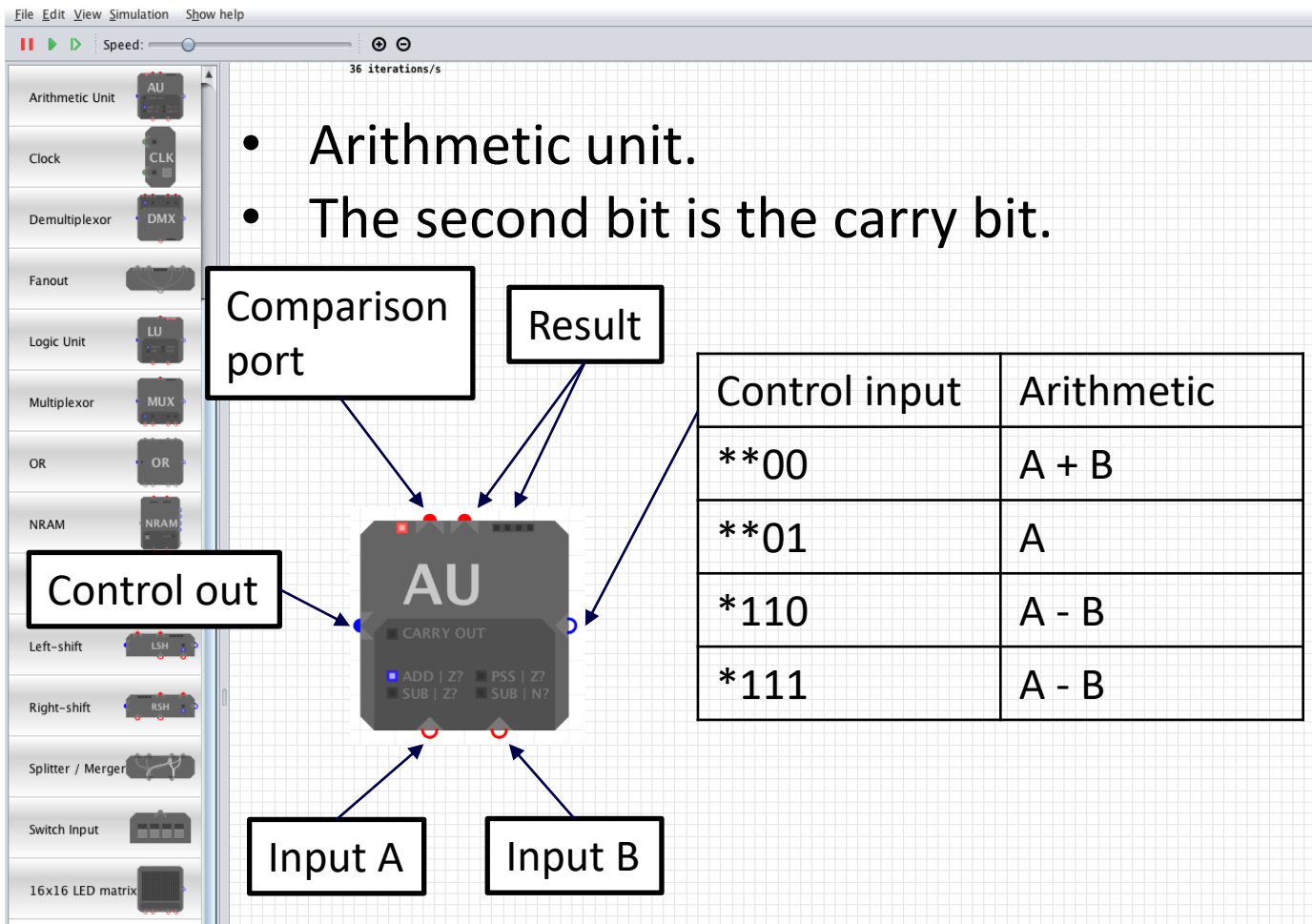
# Simulation



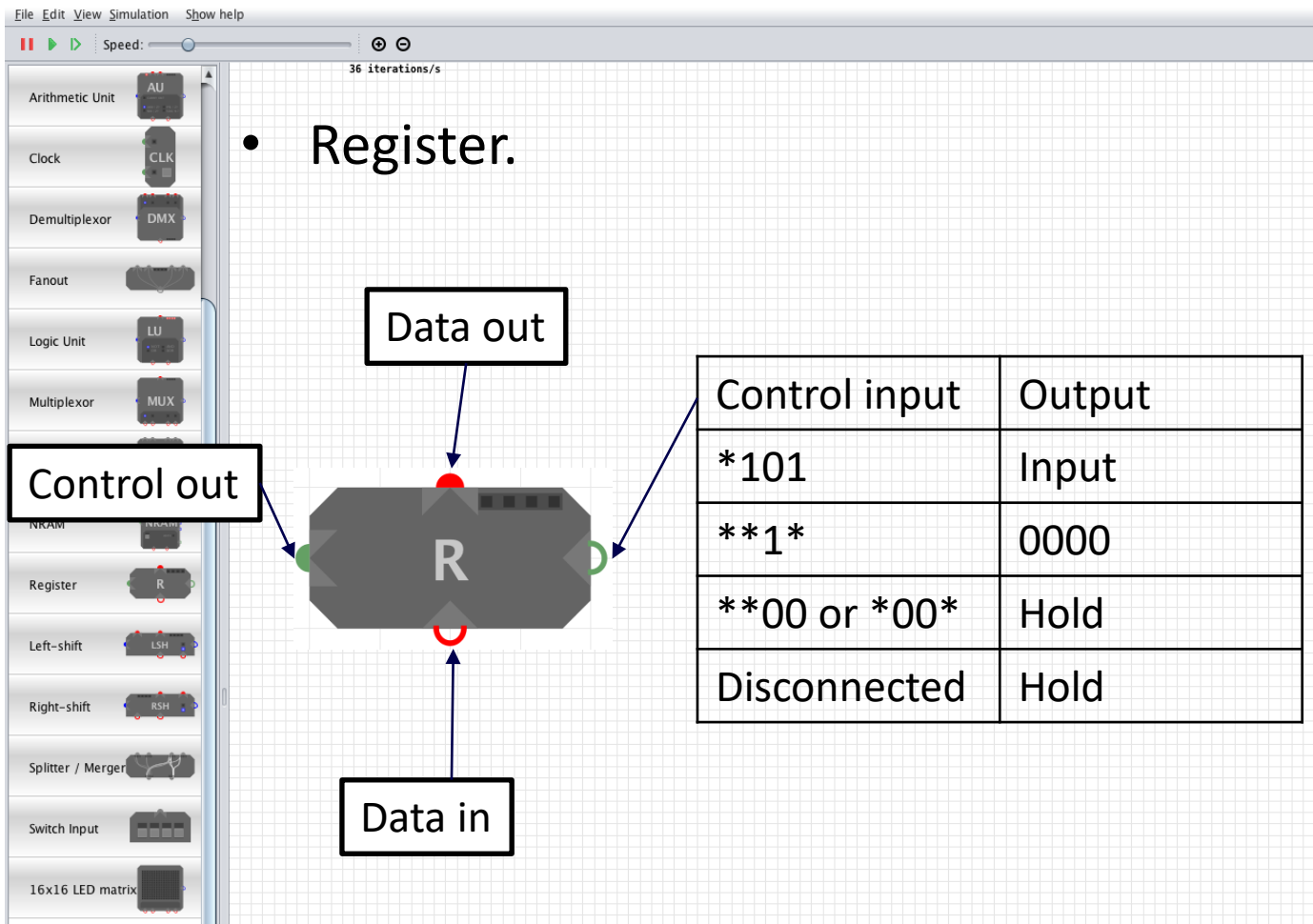
<https://github.com/TeachingTechnologistBeth/ModuleSim/releases>

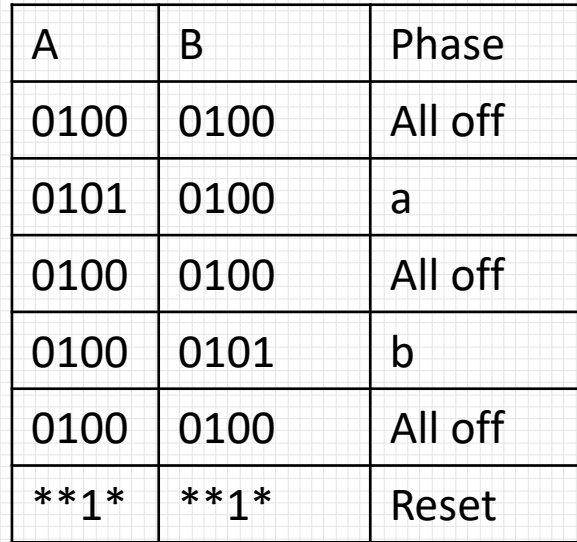
# Bus





# Register







# Clock use



File Edit View Simulation Show help

Speed:

36 iterations/s

Arithmetic Unit

Clock

Demultiplexor

Fanout

Logic Unit

Multiplexor

OR

NRAM

Register

Left-shift

Right-shift

Splitter / Merger

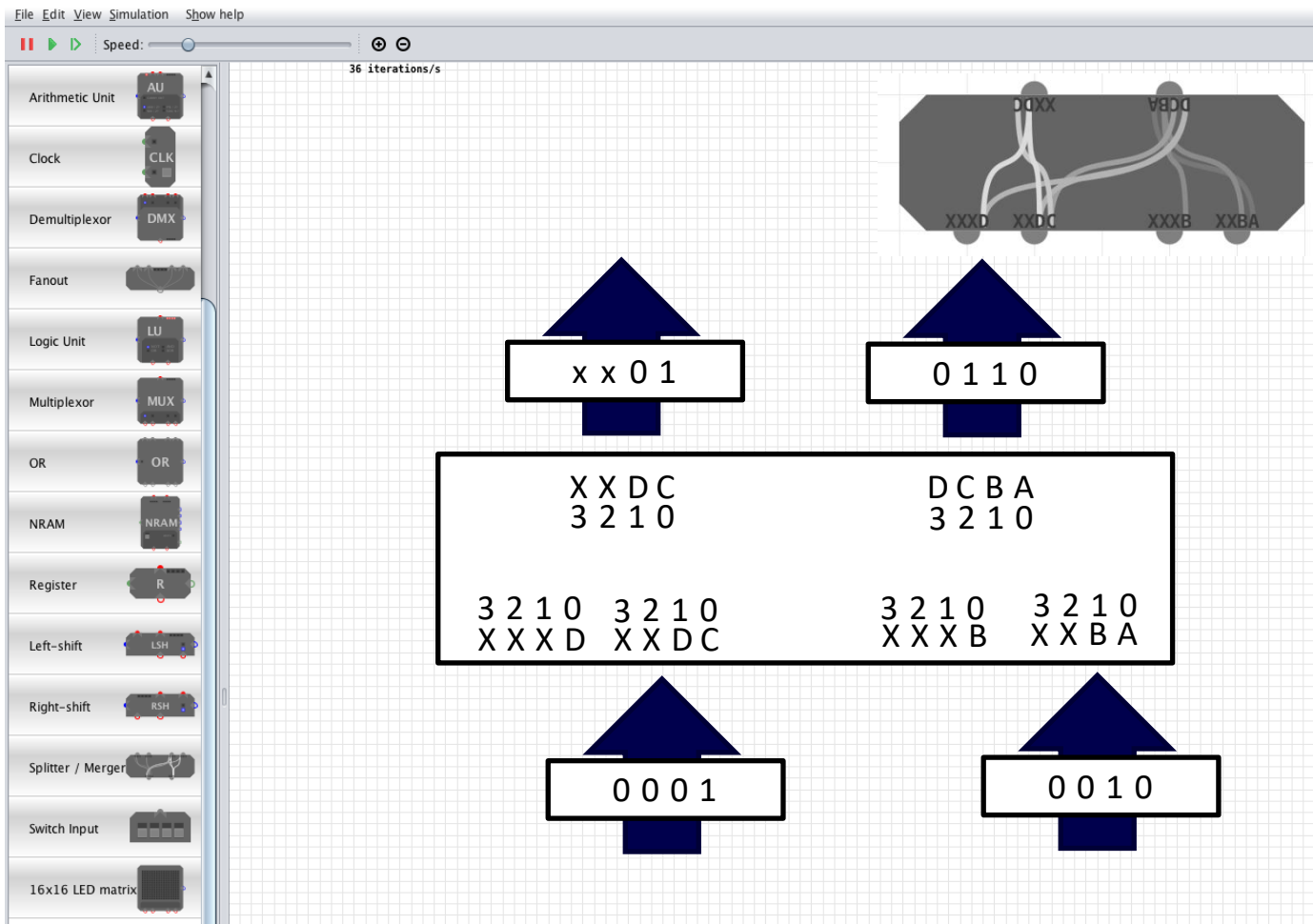
Switch Input

16x16 LED matrix

A	B	Phase
0100	0100	All off
0101	0100	a
0100	0100	All off
0100	0101	b
0100	0100	All off
**1*	**1*	Reset

Registers control input	Output
*101	Input
**1*	0000
**00 or *00*	Hold

# Split/Merge



# Split/Merge – use 2-1



File Edit View Simulation Show help

Speed: 36 iterations/s

Arithmetic Unit AU

Clock CLK

Demultiplexor DMX

Fanout

Logic Unit LU

Multiplexor MUX

OR

NRAM

Register R

Left-shift LSH

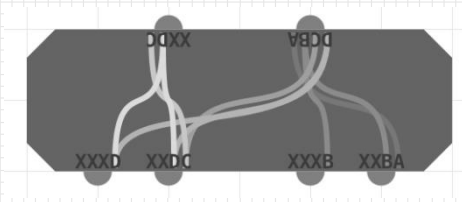
Right-shift RSH

Splitter / Merger

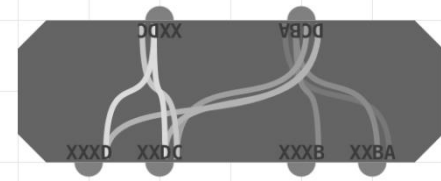
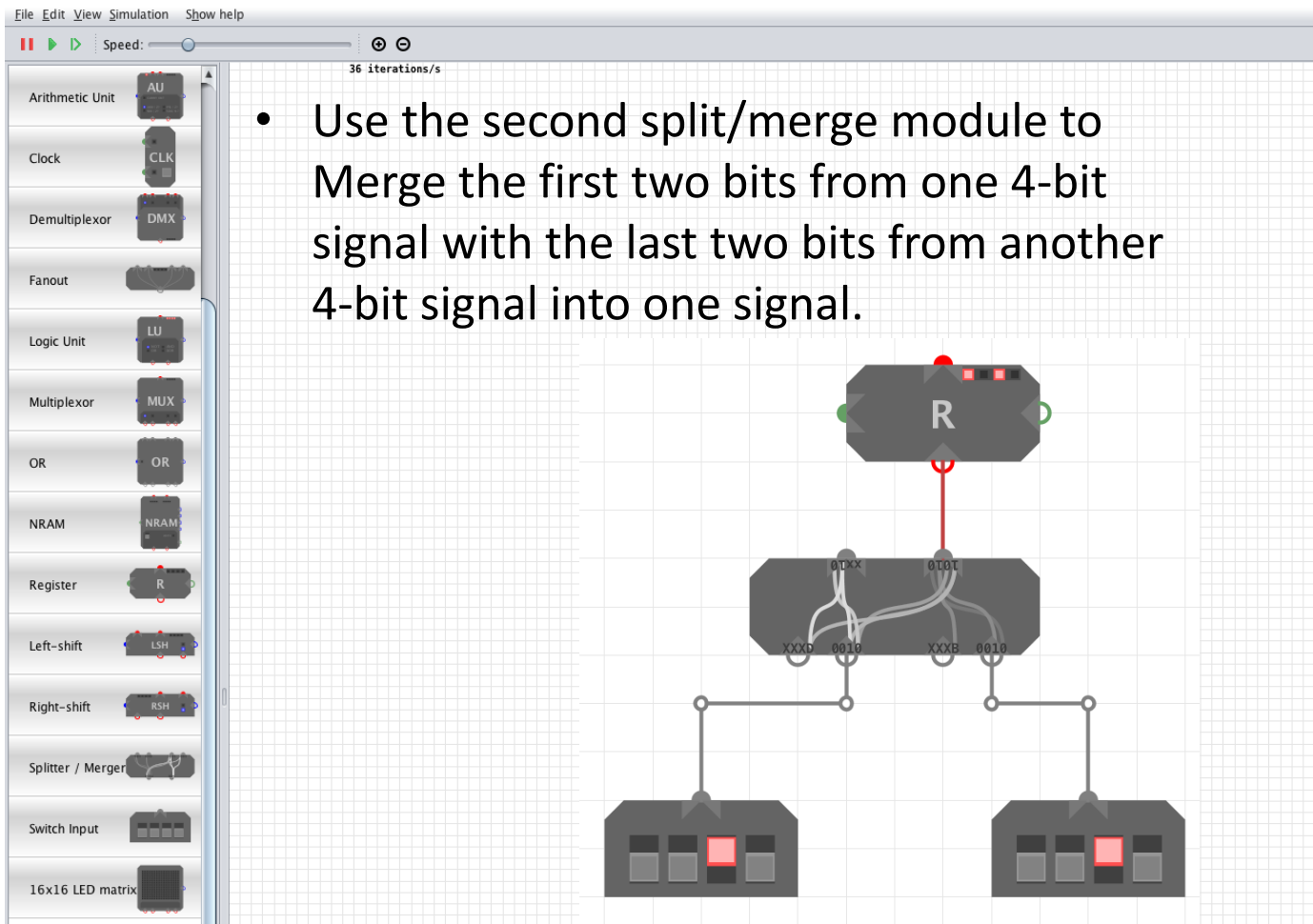
Switch Input

16x16 LED matrix

2. Use this split/merge module to merge the first two bits from one 4-bit signal  $1_3 1_2 1_1 1_0$  with the first two bits from another 4-bit signal  $2_3 2_2 2_1 2_0$  into one signal  $2_1 2_0 1_1 1_0$ .



# Split/Merge – use 2-2



# Split/Merge – use 1-1

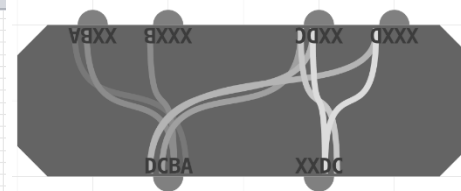


File Edit View Simulation Show help

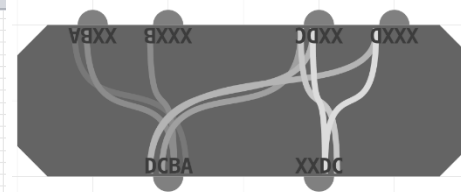
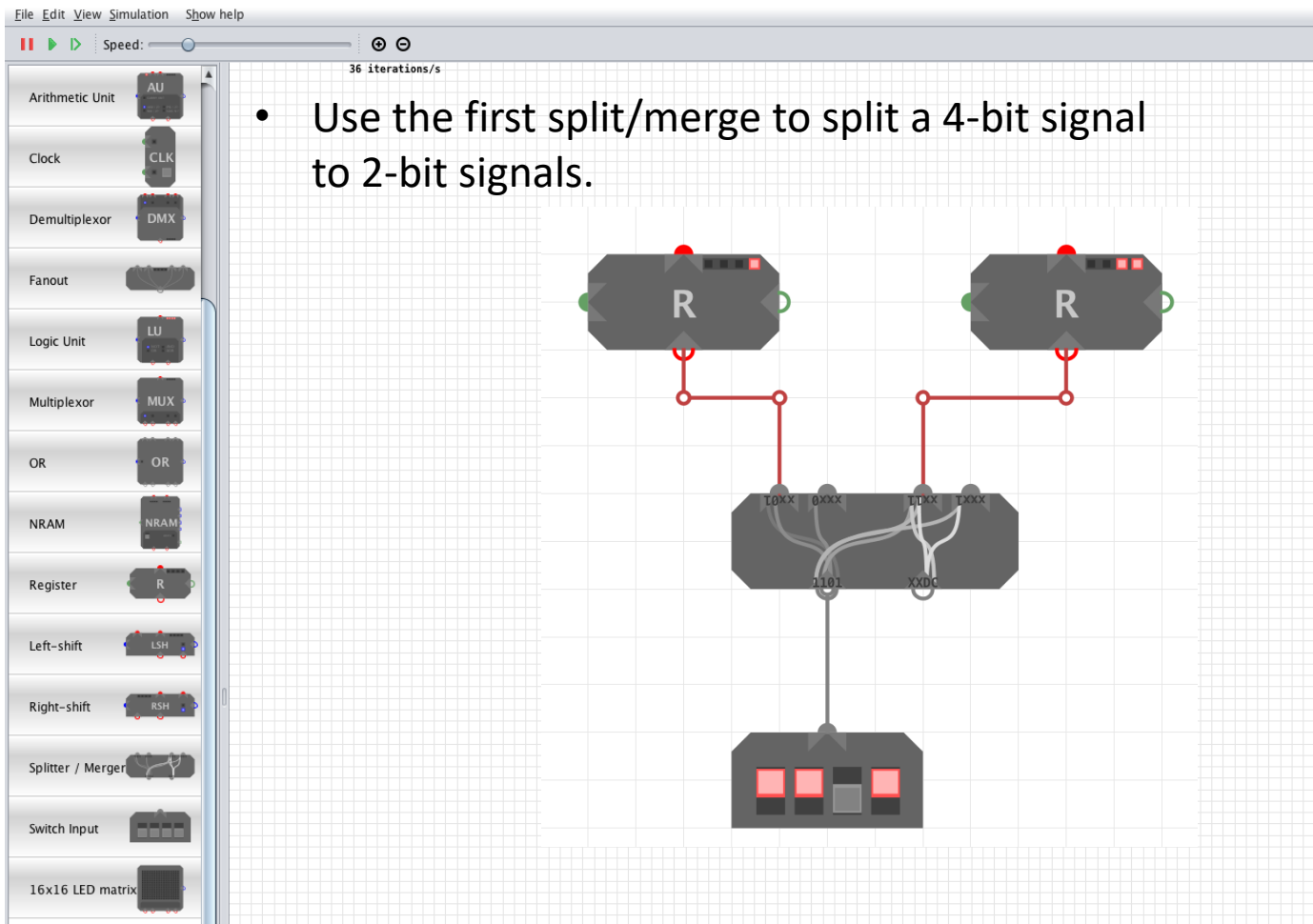
Speed: 36 iterations/s

Arithmetic Unit (AU)  
Clock (CLK)  
Demultiplexor (DMX)  
Fanout  
Logic Unit (LU)  
Multiplexor (MUX)  
OR  
NRAM  
Register (R)  
Left-shift (LSH)  
Right-shift (RSH)  
Splitter / Merger  
Switch Input  
16x16 LED matrix

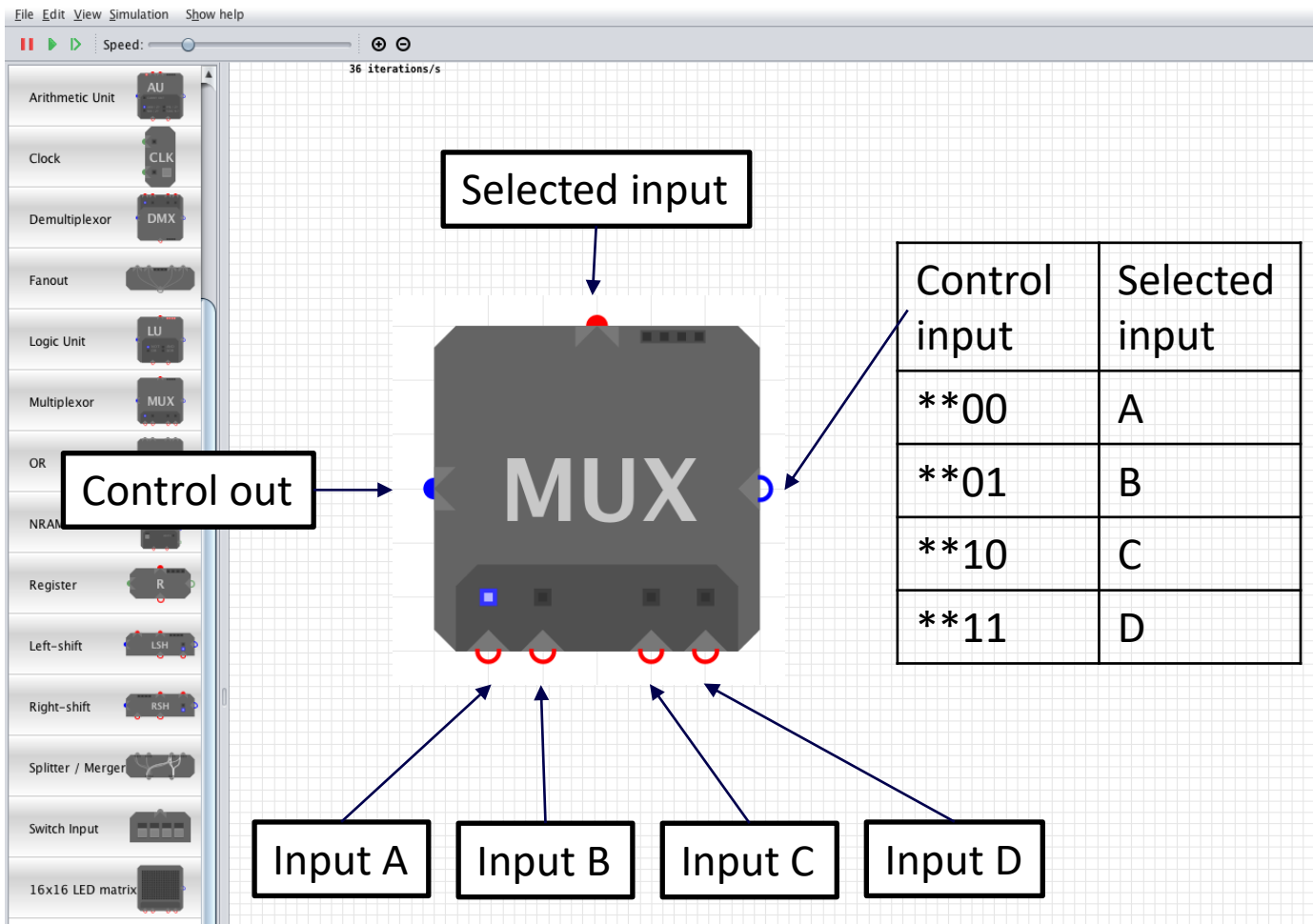
1. Use the first split/merge to split a 4-bit signal  $1_3 1_2 1_1 1_0$  to 2-bit signals. Such that the first two bits (LSB's) of the signal are the first two bits of one signal  $xx1_1 1_0$  and the two high bits of the original signal are first two bits of another signal  $xx1_3 1_2$ .



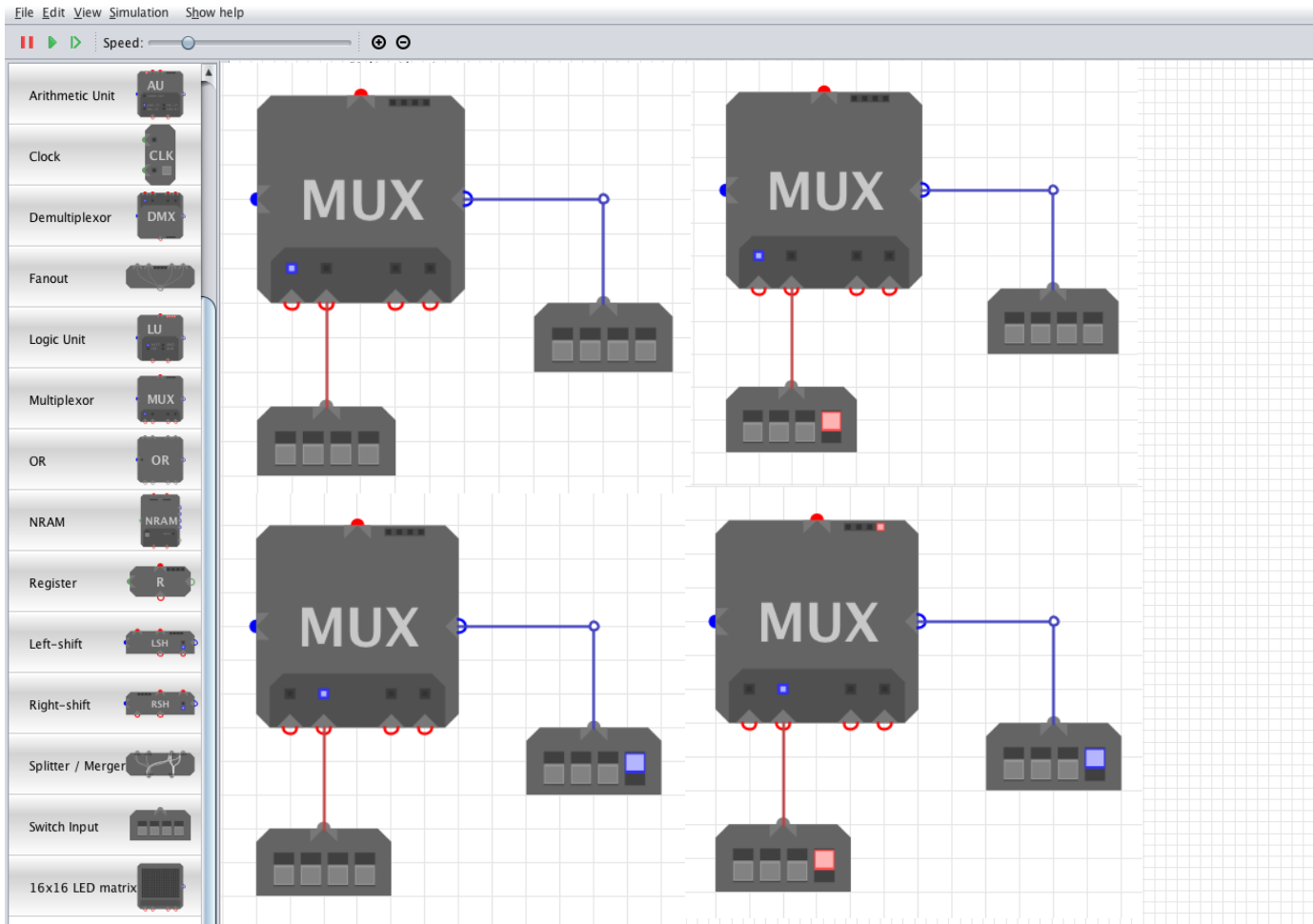
# Split/Merge – use 1-2



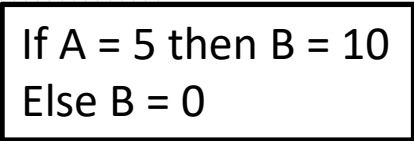
# MUX

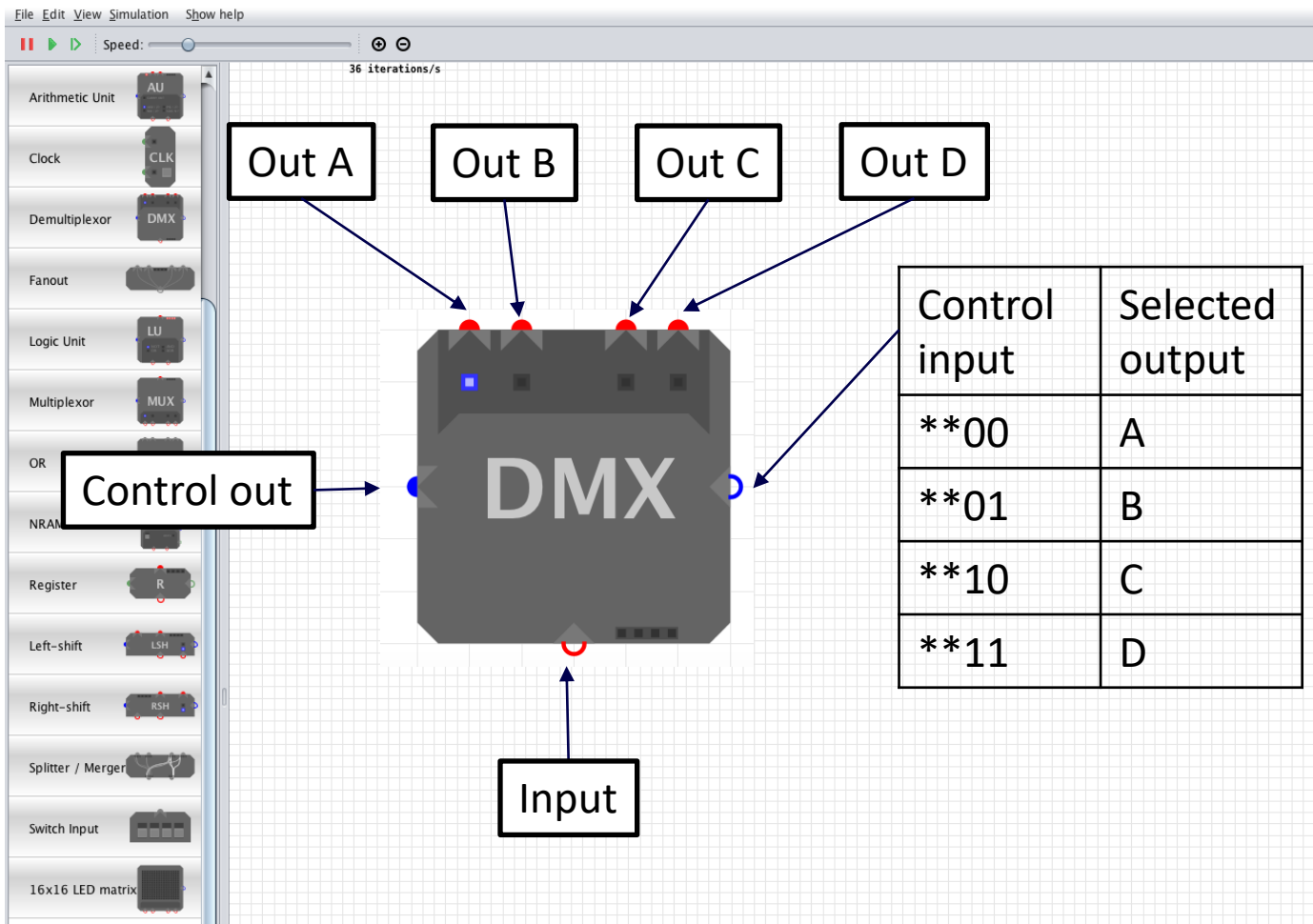


# AND from MUX









# DMX with counter

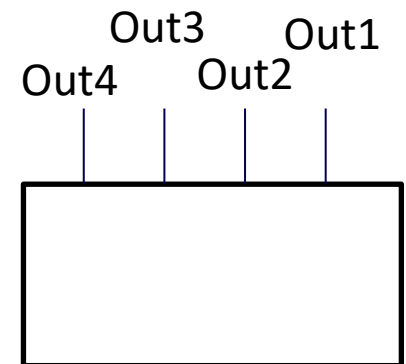


File Edit View Simulation Show help  
Speed: 36 iterations/s

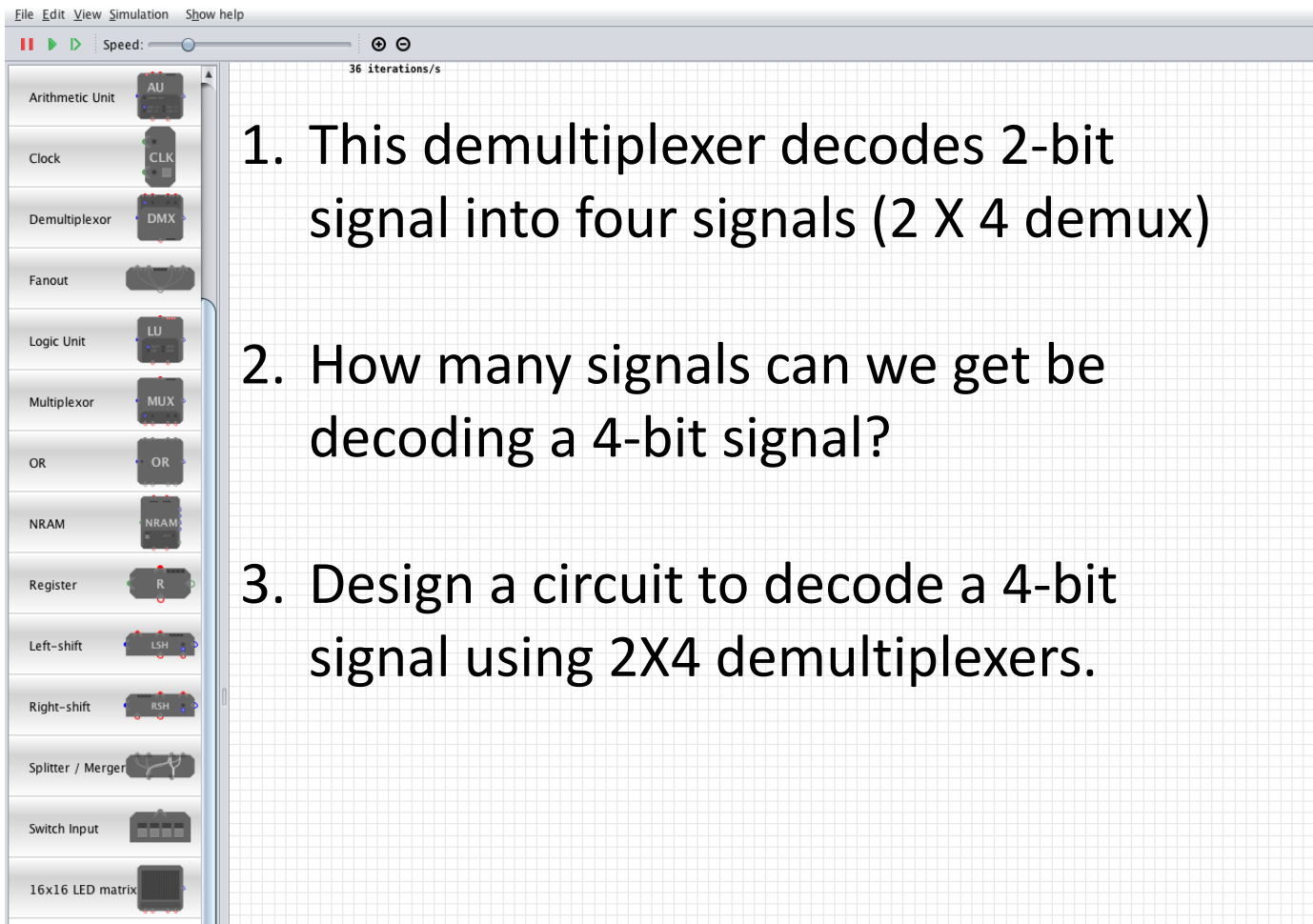
- Use a counter and a 2X4 demultiplexer to produce four signals such that one of them is high at a time.

Out1	Out2	Out3	Out4
0001	0000	0000	0000
0000	0001	0000	0000
0000	0000	0001	0000
0000	0000	0000	0001

- Hint – use the output of the counter to control the demultiplexer.



# 4 X 16 DMX



File Edit View Simulation Show help

Speed: 36 iterations/s

1. This demultiplexer decodes 2-bit signal into four signals (2 X 4 demux)
2. How many signals can we get be decoding a 4-bit signal?
3. Design a circuit to decode a 4-bit signal using 2X4 demultiplexers.

Control input	Selected output
**00	A
**01	B
**10	C
**11	D

# OR



File Edit View Simulation Show help

Speed: [Slider]

36 iterations/s

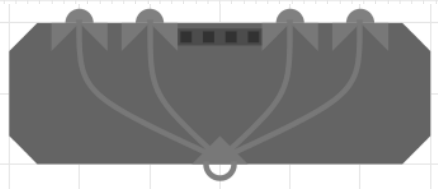
- Chained OR out =  $in1_1 + in2_1 + in3_1 + in4_1 + \text{Chained OR in}$

# Fanout



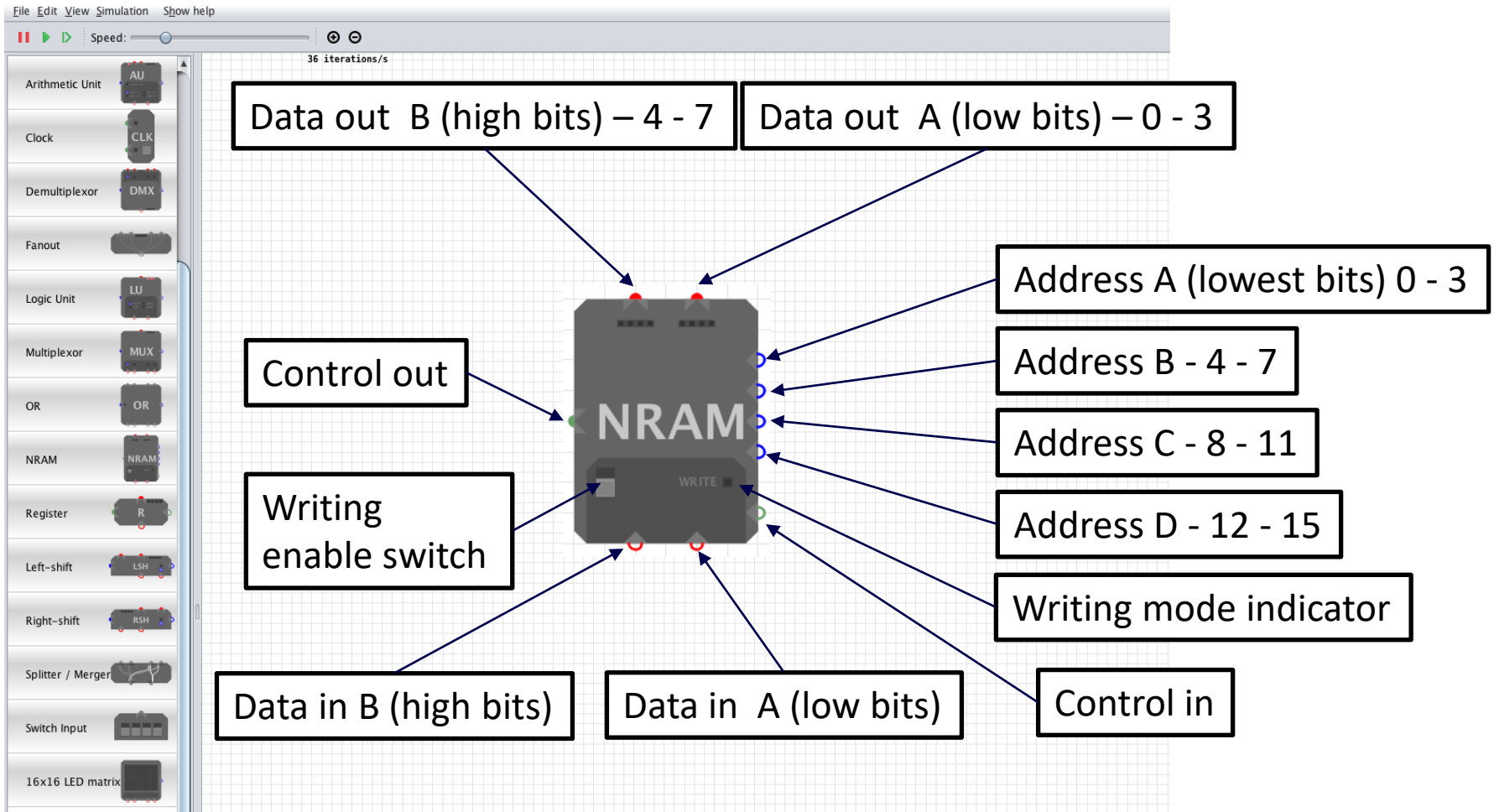
File Edit View Simulation Show help

Speed: 36 iterations/s



- $\text{Input} = \text{out}_1 = \text{out}_2 = \text{out}_3 = \text{out}_4$
- It's just a junction or a repeater.

# Memory



# Memory - size



File Edit View Simulation Show help

Speed: 36 iterations/s

Arithmetic Unit AU

Clock CLK

Demultiplexor DMX

Fanout

Logic Unit LU

Multiplexor MUX

OR

NRAM

Register R

Left-shift LSH

Right-shift RSH

Splitter / Merger

Switch Input

16x16 LED matrix

1. What is the size of the data elements in this memory?
2. How many data elements can we store in this memory?
3. What is the layout of this memory?
4. What is the size of this memory?

data (4 – 7)

data (0 – 3)



Add (0 – 3)

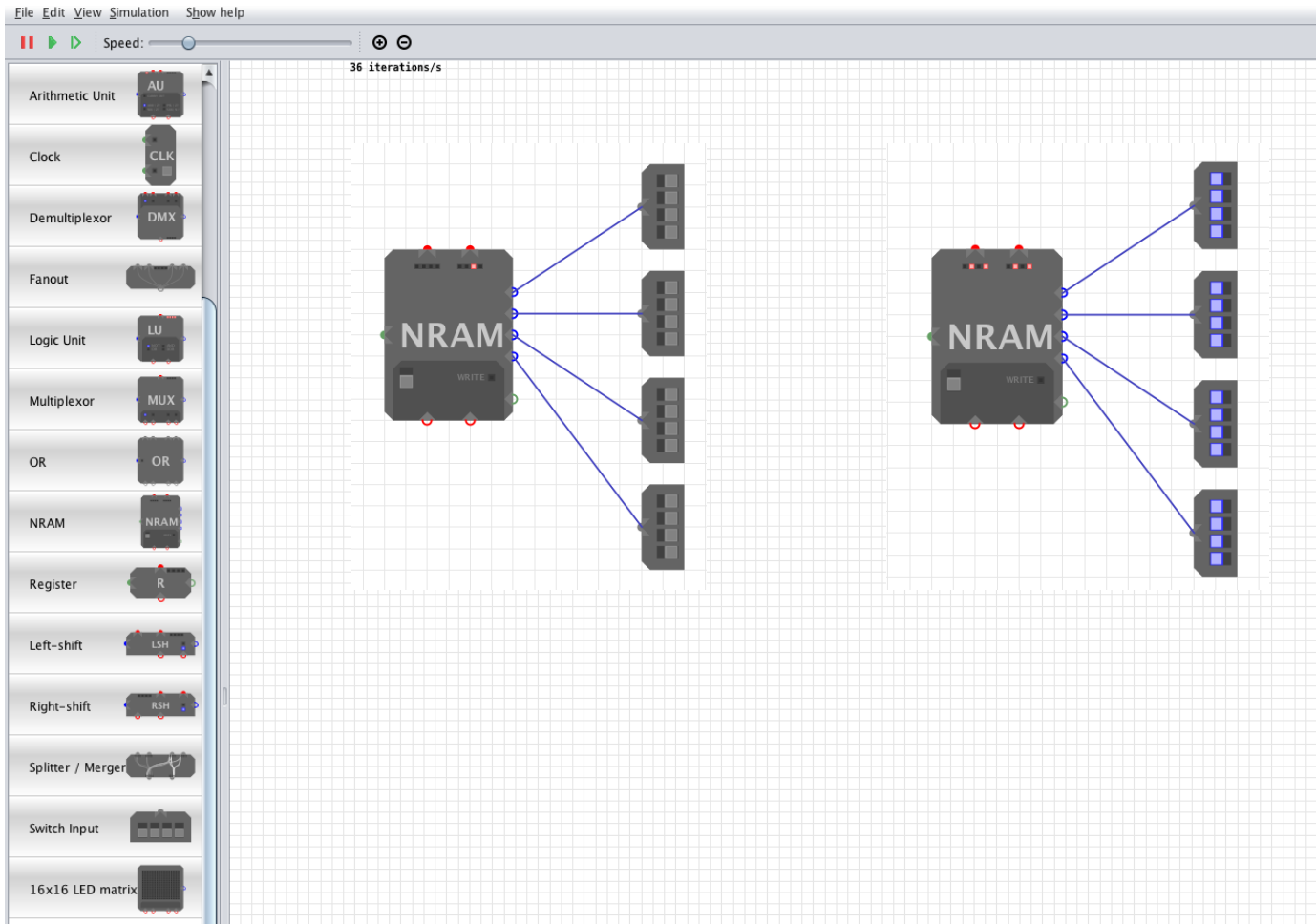
Add (4 – 7)

Add (8 – 11)

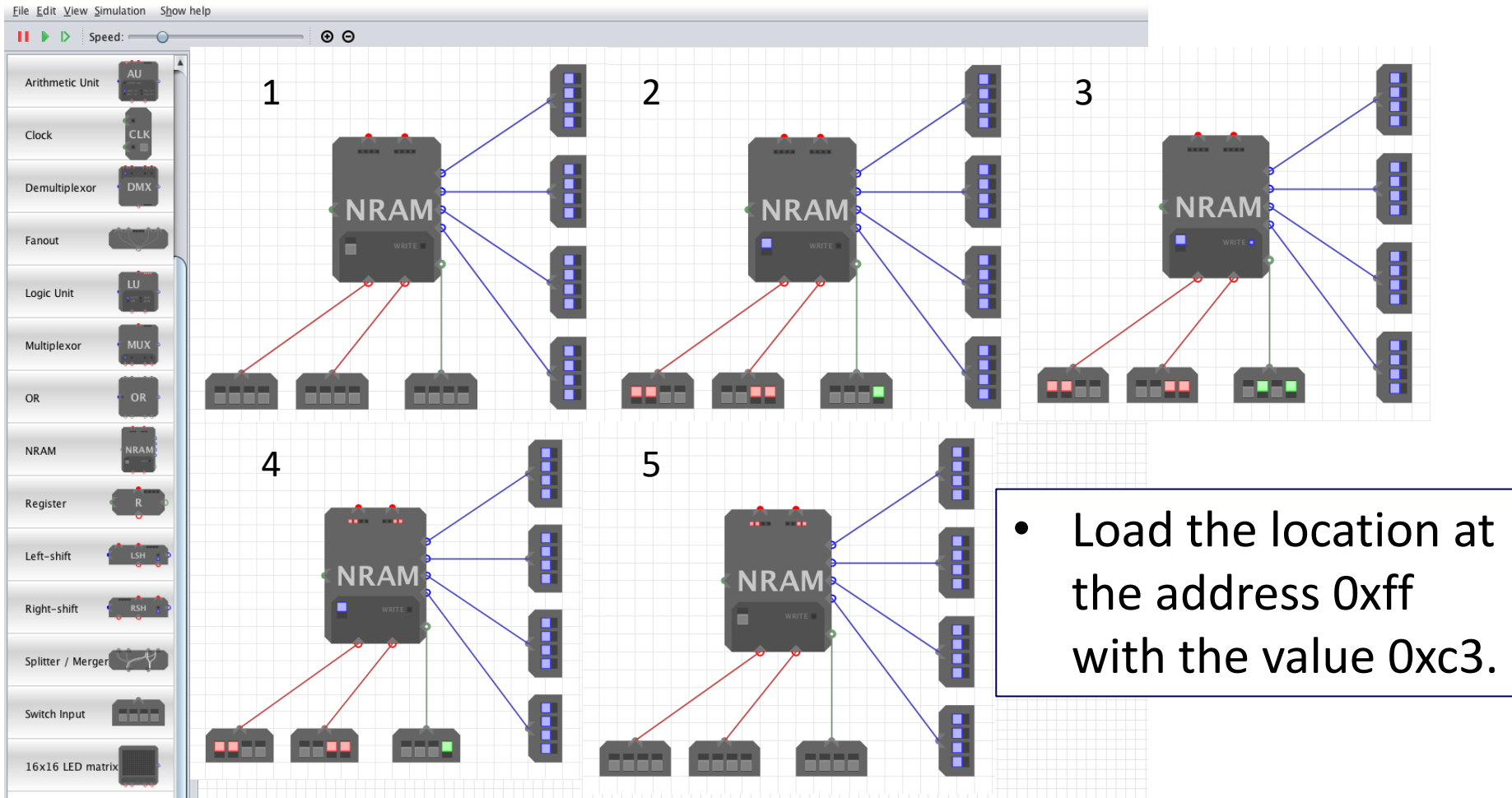
Add (12 – 15)



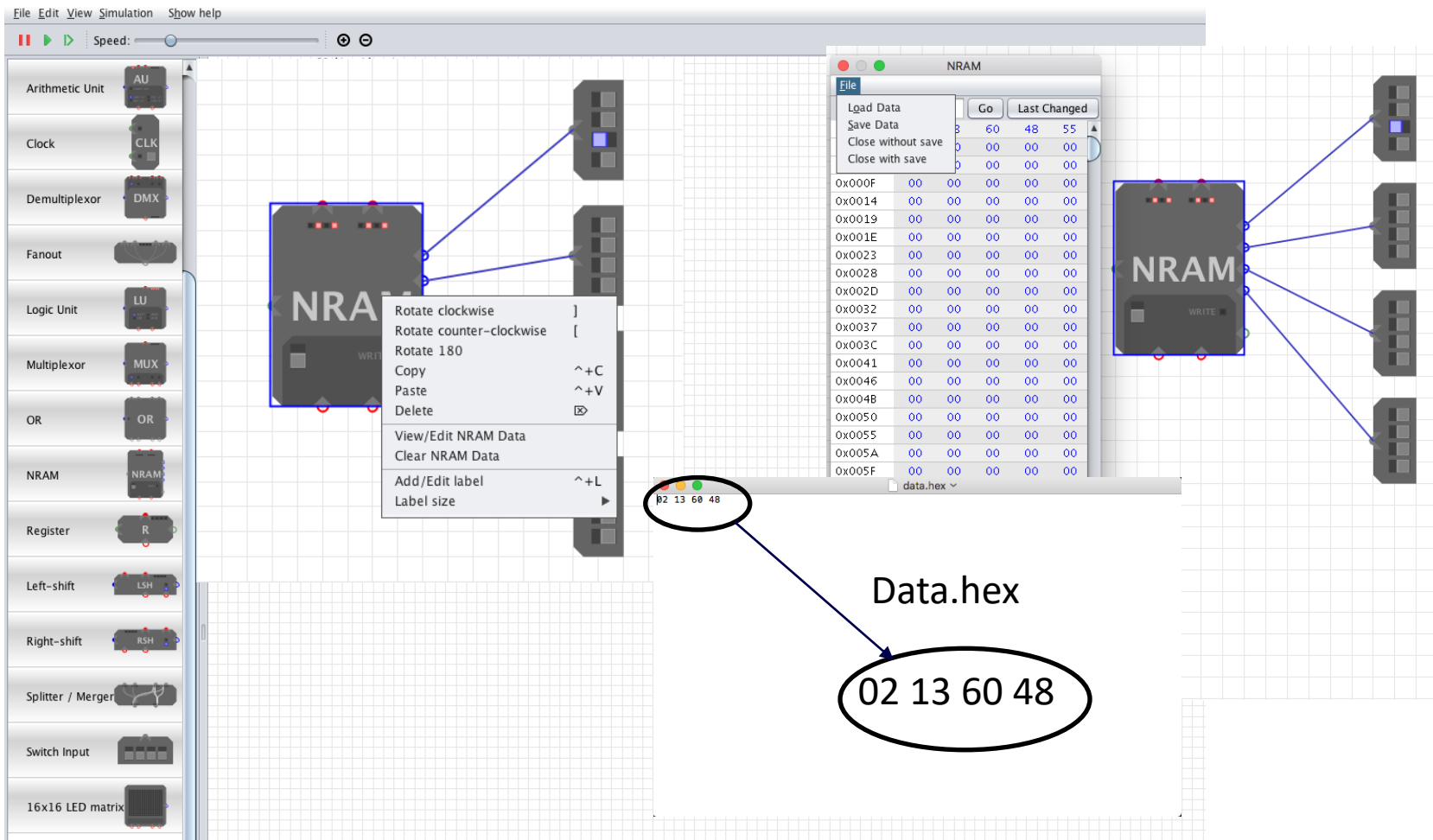
# Memory - read



# Memory – write



# Memory – load data




# Memory - design problem -1



File Edit View Simulation Show help  
Speed: 36 iterations/s

- You have two memory components. Design a circuit to copy the content of the first 16 bytes from the first memory to the first 16 bytes of the second memory.

data	address
0x02	0x0
0x13	0x1
0x60	0x2



data	address
0x02	0x0
0x13	0x1
0x60	0x2

# Memory - design problem -2

File Edit View Simulation Show help  
Speed: 36 iterations/s

Arithmetic Unit (AU)  
Clock (CLK)  
Demultiplexor (DMX)  
Fanout  
Logic Unit (LU)  
Multiplexor (MUX)  
OR  
NRAM  
Register (R)  
Left-shift (LSH)  
Right-shift (RSH)  
Splitter / Merger  
Switch Input  
16x16 LED matrix

Extra challenge. Design a circuit to move the data from the first memory to the second memory. The data should be unchanged if the value of each 4bits is greater than zero and to store 0xf for each 4 bits if their value is zero.

data	address
0x02	0x0
0x13	0x1
0x60	0x2

→

data	address
0xf2	0x0
0x13	0x1
0x6f	0x2



# Summary

1. ModuleSim and some of its components.
  1. How clock control registers
  2. How to use Split/Merge
  3. Some applications of multiplexers and demultiplexers.
2. Memory component and two design problem.