Transistor H_{FE} Tester

Submitted By Group - 32

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Problem statement - User requirements

Design a microprocessor based transistor hFE tester. The system has to display the H_{FE} value of NPN transistors.The transistor under test (TUT) is to be inserted in the socket, and its base is energized with a current from a device DI.The current I produced by the device DI, can be controlled by supplying it with a DC voltage V. The relationship is as follows:

$$\mathbf{I = V * 10^{-6}\ A}$$

The emitter of the transistor is grounded, and the collector is connected to a 1K resistor, whose other end is connected to the +5V supply. The Voltage drop across a 1K resistor is measured and this is related to the H_{fe} by the following relation:

$$\mathbf{H_{FE} * I * 1000 = Voltage\ Drop}$$

The H_{fe} value should be displayed on a seven segment display. If the hFE value is less than 20, an alarm should be sounded. For the transistor being tested current varying from 1-10μA is given as input in steps with a resolution of 1μA.

A switch is provided for the user -which has to be closed after the transistor has been placed in TUT Slot.

Assumptions and Justifications:

- We are using an ADC : AD 7819. This uses a busy signal which remains high during the conversion process. So polling is used to check when conversion is complete (4.5microseconds to complete)
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- HFE Value is within 3 digits as we have used 3 seven segment displays.
- The transistor under test (TUT) is operating in active mode.
- To provide an increment of 1 μA, we need an increment of 1V through the DAC to the voltage controlled current source. The DAC used is an 8 Bit DAC so Vref to be applied is 2.56 so that resolution is 0.01. This means that the transconductance of the voltage controlled current source will have to be changed to $I = V * 10^{-4}$ A.

Components used with justification:

- 8086 Microprocessor
- 8284 Clock generator - for clock and reset of 8086 and 8255
- 8255 - for I/O interfacing
- AD 7819 - ADC for converting analog voltage drop to digital
- AD 7224 - DAC for providing voltage input to voltage controlled current source
- Voltage Controlled Current Source - device DI as in problem statement
- 7447 - BCD to seven segment decoder (common anode)
- 2716 - this is the smallest ROM chip available
- 6116 - this is the smallest RAM chip available
- 74LS138 - decoder for memory interfacing and 8255 chip select
- 74LS373 - latch
- 74LS245 - buffer
- Common anode seven segment display
- 1K Ohm resistor - connected to collector of Transistor Under Test
- 2N3906 - PNP Transistor required for the displays
- Switch
- Hybrid relay
- NPN BC337- NPN transistor
- Buzzer
- Resistances for the display connections

Memory mapping :

Memory	Addresses	# of chips used
RAM	00000H-00FFFH	2 RAM chips of size 2k each
ROM	FF000H-FFFFFH	2 ROM chips of size 2k each

I/O Mapping :

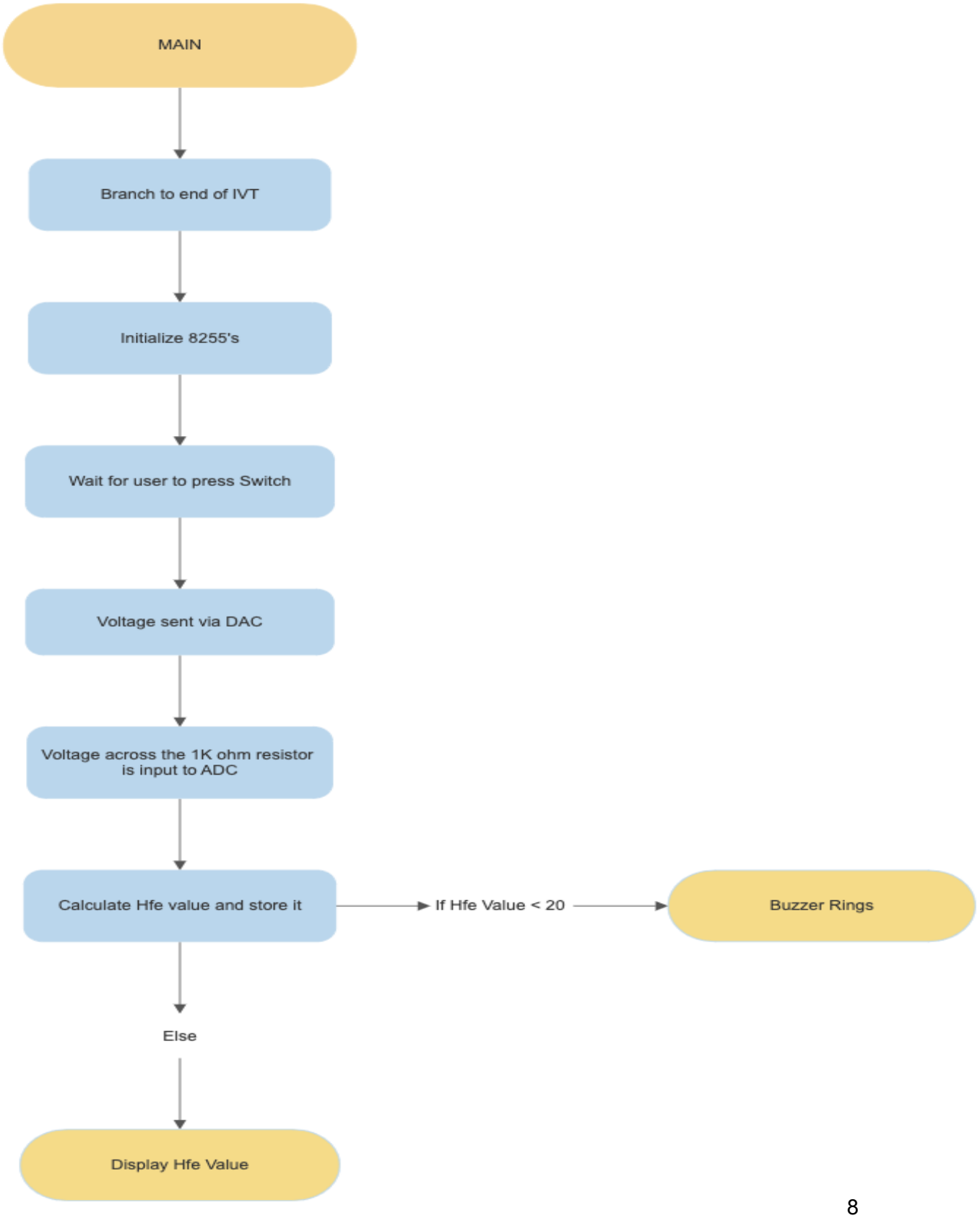
8255 (#1)

Port	Port Address	Input/Output
A	00H	Output - to DAC
B	02H	Input - from ADC
C (Lower)	04H	Output - to ADC control
C (Upper)	04H	Input - from ADC control and switch
Control Register	06H	

8255 (#2)

Port	Port Address	Input/Output
A	08H	
B	0AH	Output - to - 7447
C (Lower)	0CH	Output - to display
C (Upper)	0CH	Output - to buzzer
Control Register	0DH	

Flow Chart :


MAIN
Branch to end of IVT
Initialize 8255's
Wait for user to press Switch
Voltage sent via DAC
Voltage across the 1K ohm resistor is input to ADC
Calculate Hfe value and store it
If Hfe Value < 20
Buzzer Rings
Else
Display Hfe Value