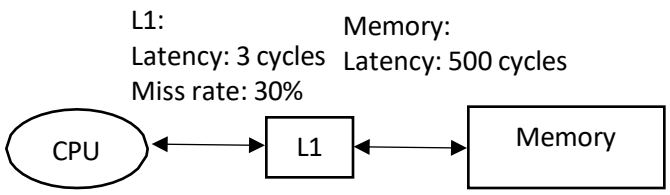
CSE 140 Lab/HW#6 – 4/26 11:59PM

Caches (15pts + 15pts)

1. Suppose the following cache hierarchies.



   a. What is the average memory access time?

Average memory access time = (L1 latency + miss rate*memory latency)
= (3 +0.3*500) = 153 cycles

   b. You want to improve the average memory access time so you added a L2 cache between L1 and Memory. L2 takes 20 cycles and miss rate is 10%. What is the average memory access time? And what is the speedup over the initial design (the above hierarchy)?

Average memory access time = (L1 latency + miss rate*(L2 latency + L2 miss rate *memory latency))
= (3 +0.3(20 +0.1*500)) = 24 cycles
Speedup = 153/24 = 6.375

Virtual memory (30pts)

2. Consider the following assumptions:
   - Size of virtual address: 64 bits
   - Size of physical address: 29 bits
   - Page size: 8 KB
   - Size of meta data per page table entry: 8 bits

   What is the size of the page table for this system?

   Max size of virtual address = 2^64 bytes

   Size of physical address: 29 bits = 2^29 bytes

   Page size: 8KB = 2^3 * 2^10 = 2^13 bytes

   Size of meta data per page table entry: 8 = 2^3 bytes

   Total pages = Max size of virtual address/page size = 2^64/2^13 =2^51

   Size of page table = Total pages * size of meta data per page table(2^3 bits =2^1 bytes)

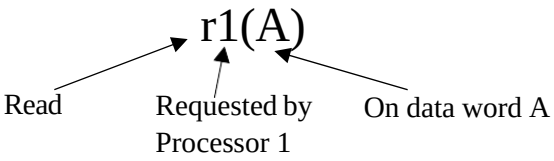
   = 2^51 *2^0 = 2^51 bytes = 2^1 *2^50 = 2 PB(petabyte)

Cache Coherence (40 pts)

3. Consider the following reference stream:

r1(A), r3(B), w3(B), r1(A), r2(A), w1(B), r2(B), w1(B), w3(A), r1(A)

All of the references in the stream are to the same cache block but for different data words, A and B within the same cache block. r and w indicate read and write, respectively, and the digit refers to the processor issuing the reference.



We run MESI protocol. Assume that all caches are initially empty and the accessed cache block is not evicted while executing the reference stream. Use the following cost model:

- Read / write cache hit with no bus access: 1 cycle
- Invalidation broadcasting without requesting the cache block (BusUpgr): 10 cycles
- Request remote processor to send updated a cache block (BusRd / BusRdX): 50 cycles
- Request the memory (or next level cache) to send a cache block (BusRd): 150 cycles

Fill the following table with the coherence state of the three processors, coherence message, and cache hit/miss for each memory references. Each column should show the status of the corresponding data word (either A or B). Show the total number of cycles used for running the reference stream.

	r1(A)	r3(B)	w3(B)	r1(A)	r2(A)	w1(B)	r2(B)	w1(B)	w3(A)	r1(A)
hit/miss	M	M	H	M	H	M	M	H	M	M
bus	BusRd	BusRd	-	BusRd	BusRd	BusUpgr	BusRd	-	BusUpgr	BusRd
State1	E	I	I	S	S	M	S	M	I	S
State2	I	I	I	I	S	I	S	I	I	I
State3	I	E	M	S	S	I	I	I	M	S
cycles	150	150	1	50	150	10	50	1	10	50

The total number of cycles : 622 cycles

Submission Guideline

- Submit your solution in an MS Word or a pdf format to the CatCourse.
- Deadline: **4/26 11:59PM** (All sections have the same deadline for this HW)