Indian Institute of Information Technology, Vadodara

International Campus Diu

Practical Work Book

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Branch: Computer Science Engineering

Batch: 2023

Subject: COA

Experiment no. 7

Aim:- Design and implementation of a pipeline architecture in verilog.

Prerequisites:- A fair understanding of pipeline concept and verilog language.

Theory:- Pipelining is a technique used in modern processors to improve performance by executing multiple instructions simultaneously. It breaks down the execution of instructions into several stages, where each stage completes a part of the instruction. These stages can overlap, allowing the processor to work on different instructions at various stages of completion, similar to an assembly line in manufacturing.

CODE:

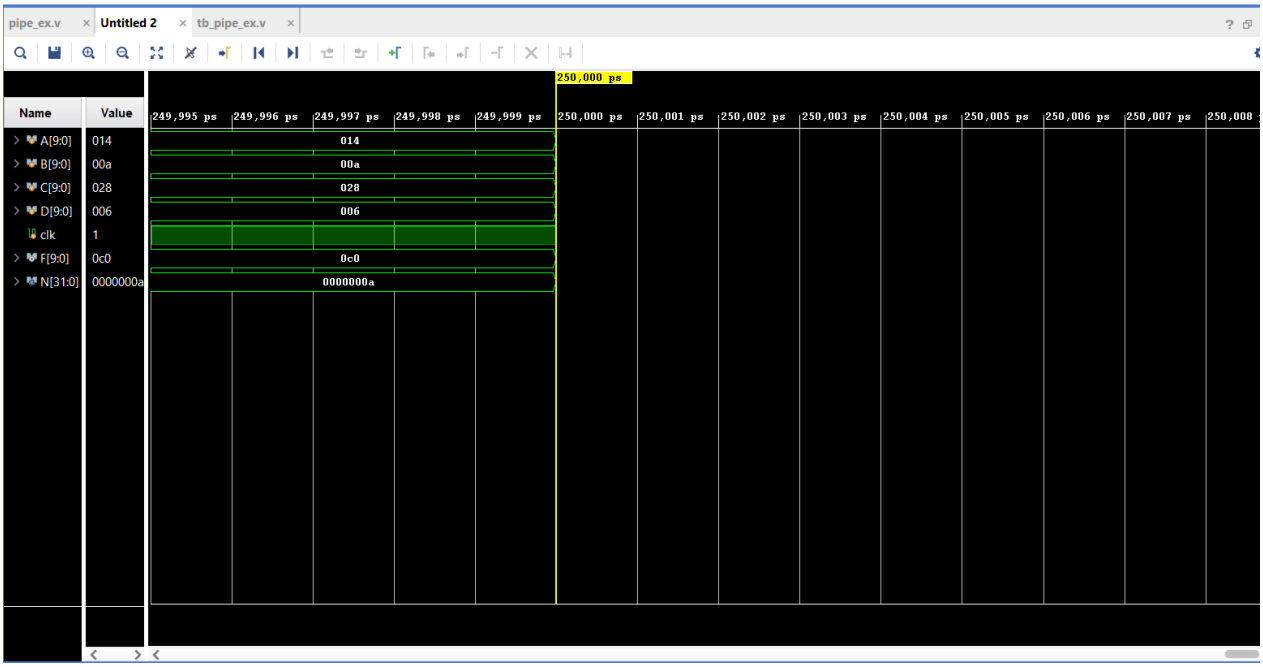
C:/Users/KSHITIZ GANGWAR/project_1/project_1.srcs/sources_1/new/pipe_ex.v

```
1  module pipe_ex (F, A, B, C, D, clk);
2      parameter N = 10;
3
4      input [N-1:0] A, B, C, D;
5      input clk;
6      output [N-1:0] F;
7
8      reg [N-1:0] L12_x1, L12_x2, L12_D;
9      reg [N-1:0] L23_x3, L23_D;
10     reg [N-1:0] L34_F;
11     reg [N-1:0] L45_F;
12
13     assign F = L45_F;
14
15     always @(posedge clk)
16     begin
17         L12_x1 <= #4 A + B;
18         L12_x2 <= #4 C - D;
19         L12_D <= D;
20         L23_x3 <= #4 L12_x1 + L12_x2;
21         L23_D <= L12_D;
22         L34_F <= #6 L23_x3 * L23_D;
23         L45_F <= #3 L34_F >> 1;
24     end
25 endmodule
26
```

C:/Users/KSHITIZ GANGWAR/project_1/project_1.srcs/sources_1/new/tb_pipe_ex.v

```
1   `timescale 1ns/1ps
2   module tb_pipe_ex();
3       parameter N = 10;
4
5       reg [N-1:0] A, B, C, D;
6       reg clk;
7       wire [N-1:0] F;
8       pipe_ex uut (F, A, B, C, D, clk);
9       initial begin
10          clk = 0;
11          forever #5 clk = ~clk;
12      end
13      initial begin
14          $dumpfile("pipeline.vcd");
15          $dumpvars(0, tb_pipe_ex);
16          A = 10; B = 5; C = 20; D = 2; #50;
17          A = 12; B = 7; C = 25; D = 3; #50;
18          A = 15; B = 8; C = 30; D = 4; #50;
19          A = 18; B = 9; C = 35; D = 5; #50;
20          A = 20; B = 10; C = 40; D = 6; #50;
21          $finish;
22      end
23  endmodule
24
```

OUTPUT:


pipe_ex.v
Untitled 2
tb_pipe_ex.v
Name
Value
A[9:0]
014
B[9:0]
00a
C[9:0]
028
D[9:0]
006
clk
1
F[9:0]
0c0
N[31:0]
0000000a
249,995 ps
249,996 ps
249,997 ps
249,998 ps
249,999 ps
250,000 ps
250,001 ps
250,002 ps
250,003 ps
250,004 ps
250,005 ps
250,006 ps
250,007 ps
250,000 ps
014
00a
028
006
0c0
0000000a