Report on Homework 5

1. Problem 1: Model the following logic expressions using `Combinatorial Logic` module in Simulink

1. $X = \overline{(AB)} + \overline{(BC)} + \overline{(AC)}$
2. $Y = (\overline{A} + B)(\overline{B} + C)(\overline{C} + A)$
3. $Z_1 = X + Y$
4. $Z_2 = XY$

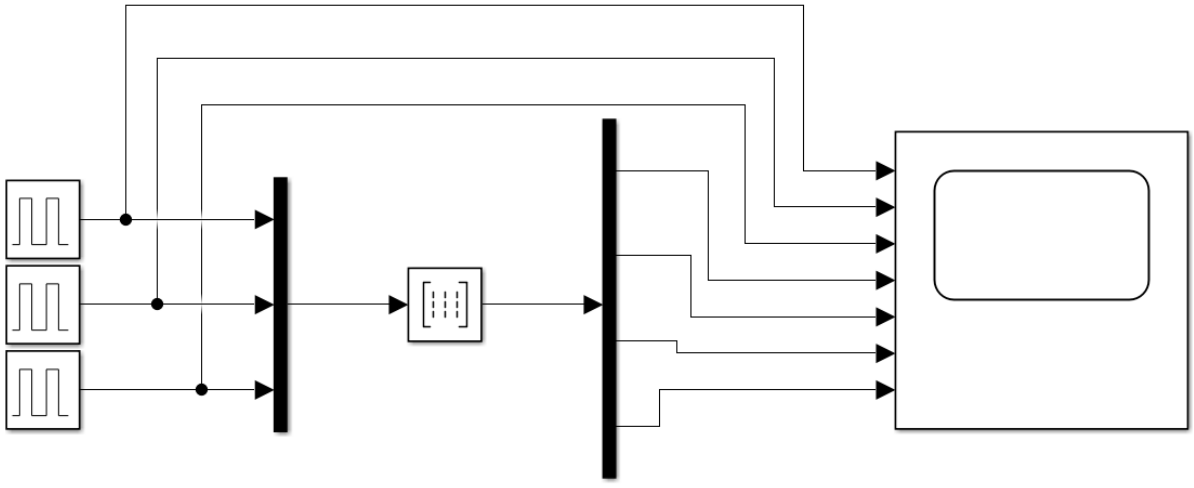
1.1. Simplification

1. $X = (\overline{A} + \overline{B}) + (\overline{B} + \overline{C}) + (\overline{C} + \overline{A}) = \overline{A} + \overline{B} + \overline{C} = \overline{ABC}$
2. $Y = \overline{A}\,\overline{B}\,\overline{C} + ABC$

1.2. Truth Table

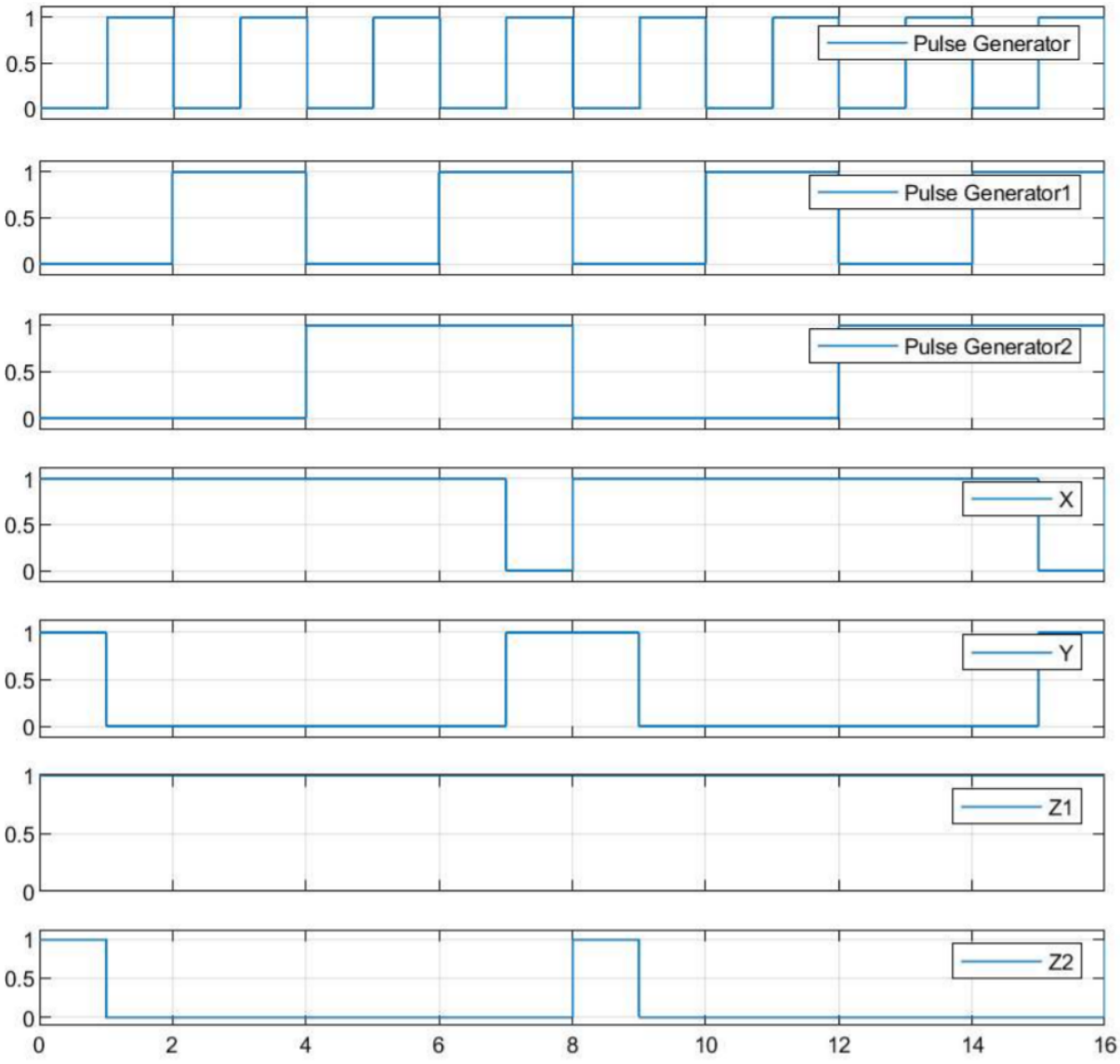
C	B	A	X	Y	Z1	Z2
0	0	0	1	1	1	1
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	1	0	1	0
1	0	0	1	0	1	0
1	0	1	1	0	1	0
1	1	0	1	0	1	0
1	1	1	0	1	1	0

1.3. Block Diagram



	Period/sec	Pulse Width/sec	Phase Delay/sec
Pulse Generator 0	2	1	1
Pulse Generator 1	4	2	2
Pulse Generator 2	8	4	4

1.4. Result



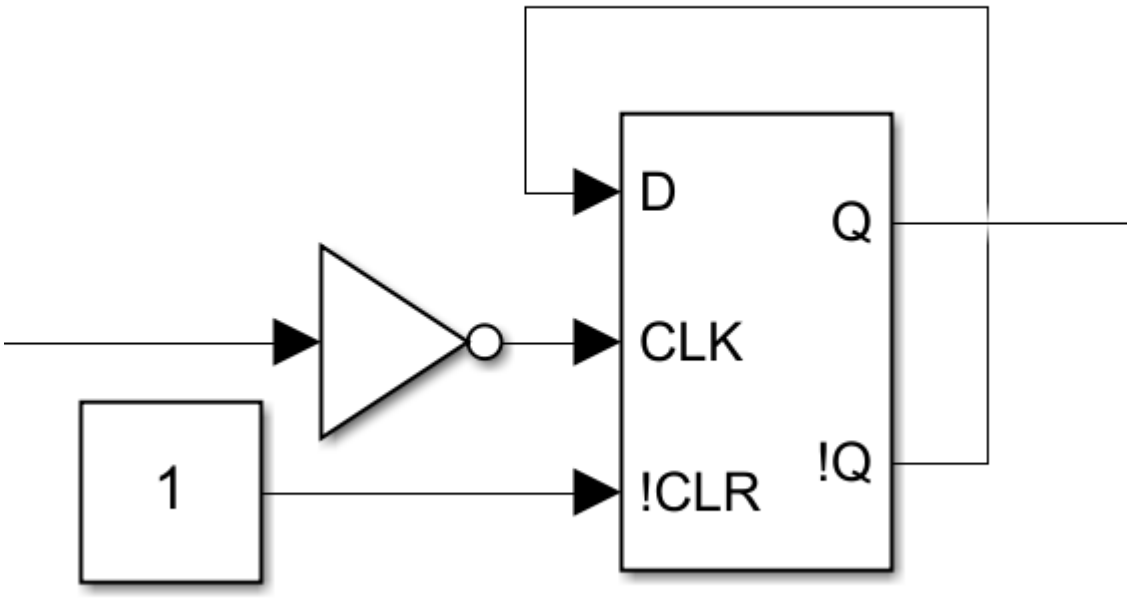
2. Problem 2: Construct a f/10 frequency divider using Flip-Flops (D or J-K) in Simulink

2.1. Solution

Consider a mod-5 counter and a 2-divider. Connecting the carry of the mod-5 counter to the clk of 2-divider yields a 10-divider.

2.1.1. 2-divider

We can use D Flip-Flop as 2-divider:



2.1.2. Mod-5 counter

To design a mod-5 counter, first draw its truth table:

Q2	Q1	Q0	C	Q2*	Q1*	Q0*	C*
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0
0	1	0	0	0	1	1	0
0	1	1	0	1	0	0	0
1	0	0	0	0	0	0	1

Second, draw the Karnaugh map of Q2* Q1* Q0* according to its truth table:

Q2\Q1Q0	00	01	11	10
0	001	010	100	011
1	000	xxx	xxx	xxx

For Q0:

Q2\Q1Q0	00	01	11	10
0	1	0	0	1
1	0	x	x	x

For Q1:

Q2\Q1Q0	00	01	11	10
0	0	1	0	1
1	0	x	x	x

For Q2:

Q2\Q1Q0	00	01	11	10
0	0	0	1	0
1	0	x	x	x

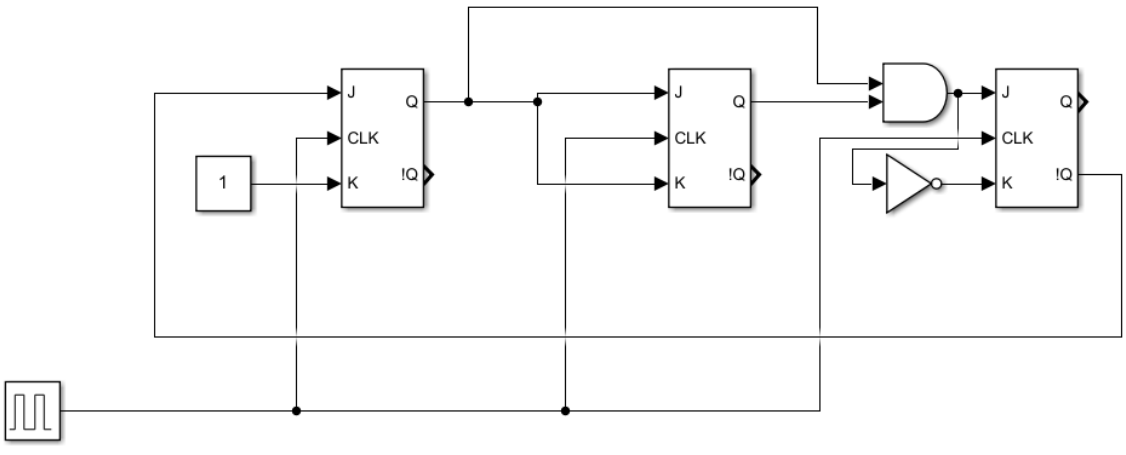
Third, write down the equation of state transition using the Karnaugh map:

- $Q_0^* = \overline{Q_2}Q_0$
- $Q_1^* = \overline{Q1}Q_0 + Q_1\overline{Q_0}$
- $Q_2^* = Q_1Q_0$
- $C^* = Q_2$

Fourth, convert the above equation into the characteristic equation of J-K Flip-Flops:

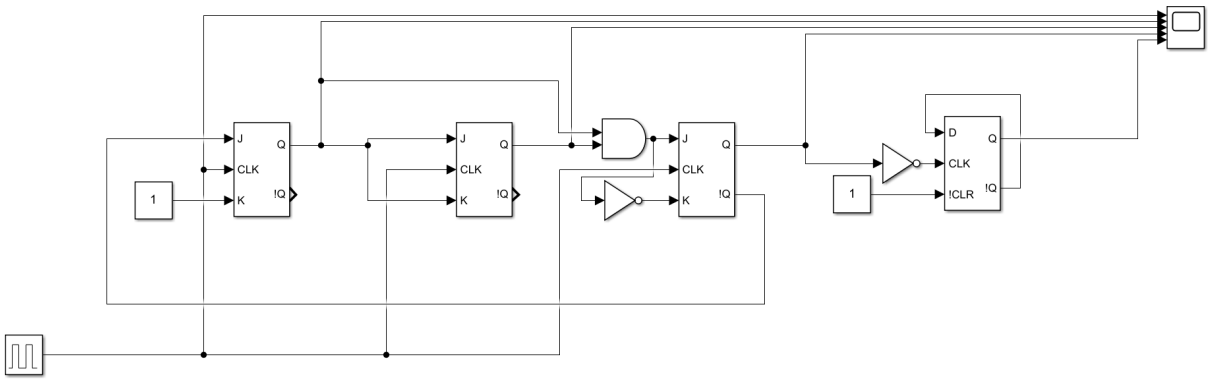
- $Q_0^* = J\overline{Q_0} + KQ_0$, where $J = \overline{Q_2}, K = 1$
- $Q_1^* = J\overline{Q_1} + KQ_1$, where $J = Q_0, K = Q_0$
- $Q_2^* = J\overline{Q_2} + KQ_2$, where $J = Q_1Q_0, K = \overline{(Q_1Q_0)}$

Finally, draw the circuit diagram using the above equations:



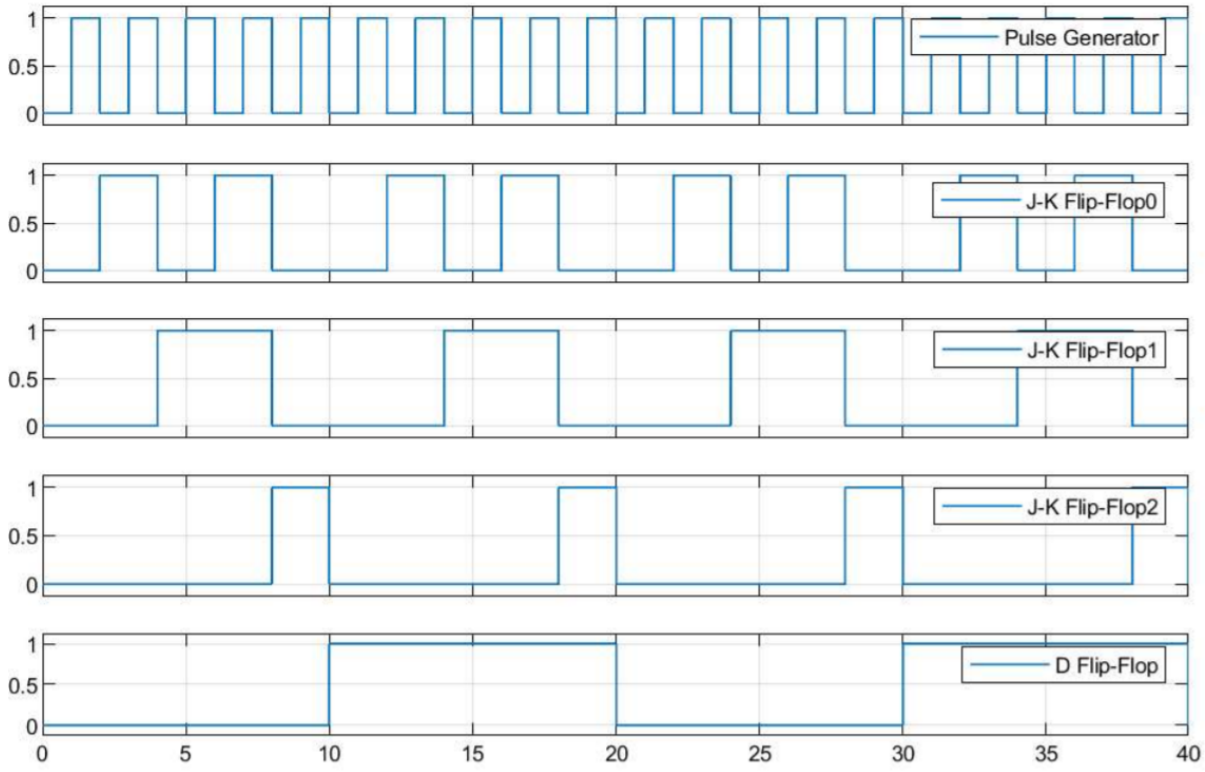
2.2. Block Diagram

Combining the 2-divider and the mod-5 counter:



Parameters of the pulse generator: period = 2s, pulse width = 1s, phase delay = 1s.

2.3. Result



As shown in the picture, the output of D F-F has 1/10 the frequency of the input pulses.