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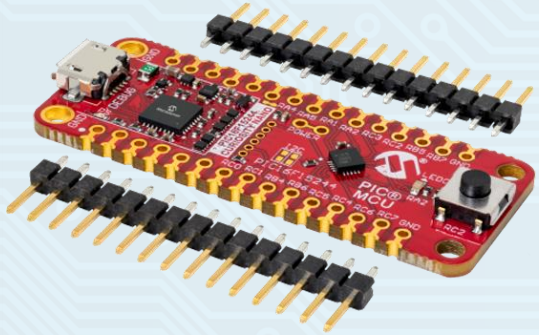

```
PSECT Input_Digital,class=CODE,reloc=2
Input_Digital:
        goto        main

PSECT code
main:
        ;Configuracion del Oscilador
        movlw       0x62
        movlb       57
        movwf       BANKMASK(OSCCON1),b
        movlw       2
        movwf       BANKMASK(OSCFRQ),b
        movlb       58
        clrf        BANKMASK(ANSELA),b

        clrf        max,c
bucle:
        movff       PORTA,tmp
```

El nuevo Assembler de Microchip (PIC-ASS).

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MPLAB X IDE

MPLAB XC COMPILER

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El nuevo Assembler de Microchip (PIC-ASS).

Lenguaje Máquina, Mnemónicos, programa ensamblador

Sanchez H. Godo

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Sesión 1

- *Introducción a las nuevas Familias de Microchip*
- *Arquitectura de los PIC18*
- *Lenguaje Ensamblador, XC8 pic-ass*
- *Set de Instrucciones en Ensamblador*
- *Implementación*

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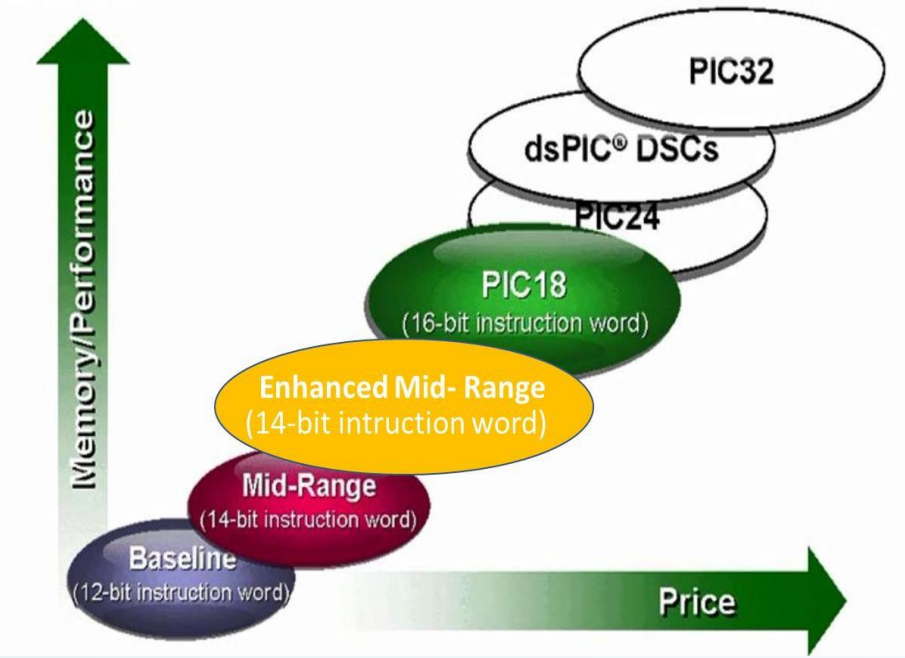
Introducción a las nuevas Familias de Microchip



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Introducción a las nuevas Familias de Microchip

CURIOSITY NANO

PIC18F57Q43

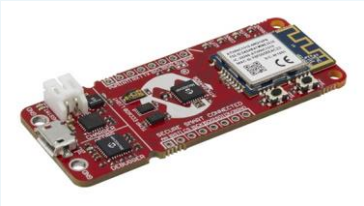
Clasicos

- 18f4550
- 328p
- 16f85

MEJORADA

- 18f45k50
- 328pb
- 16f1855

AVR IOT



XPLEINED MINI QTOUCH

ATMEGA 328PB

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Introducción a las nuevas Familias de Microchip

Periféricos Core independientes (CIP)

CORE INDEPENDENT PERIPHERALS

- Módulos de Hardware autónomos (Funcionan independientes al núcleo del Microcontrolador).
- Realizan tareas que normalmente requerían ejecución por software
- Fácilmente configurables con el MCC

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Introducción a las nuevas Familias de Microchip

CORE INDEPENDENT PERIPHERALS

- **Reduce carga de procesamiento en CPU**
  - Libera a la CPU de enfocarse en la aplicación
- **Reduce consumo de energía**
  - CPU puede correr a velocidades más lentas
  - CPU puede estar en modo SLEEP
- **Reduce complejidad en Hardware**
  - Reduce componentes externos

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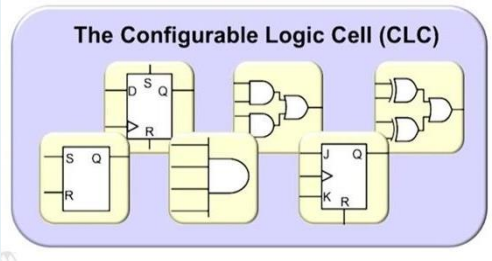
Introducción a las nuevas Familias de Microchip

CLC - Celda Lógica Configurable



Circuito lógico combinacional y secuencial configurable

Puertas lógicas combinacionales disponibles:

- AND / NAND
- OR / XOR / NOR /XNOR
- NOT

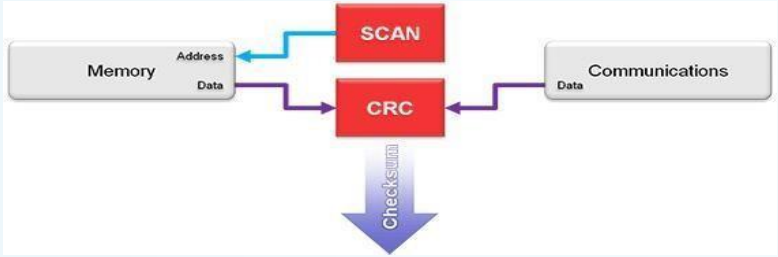
Circuitos secuenciales disponibles:

- D y JK Flips Flops
- D y SR Latches

CRC - Verificación de redundancia cíclica

Características:

- Detecta fallas en la integridad de datos
- CRC de hasta 16 bits
- SCAN en memoria automático



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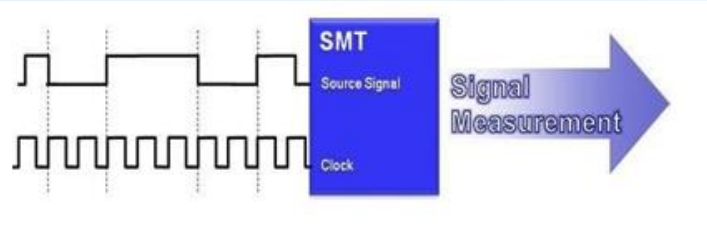
Introducción a las nuevas Familias de Microchip

SMT -Temporizador de Medición de Señal

Características:

- Timer de 24 bits
- Medición flexible de parámetros de señales digitales:
  - Periodo, Ancho de Pulso, Duración, Ciclo de trabajo (Duty Cycle), Ventana.

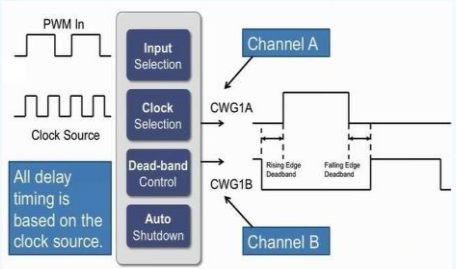


CWG - Generador de Forma de Onda Complementaria

Características:

Produce 2 formas de onda complementarias a partir de una entrada.

- Señal de entrada seleccionable
- Polaridad de salida configurable
- Dead Band Control



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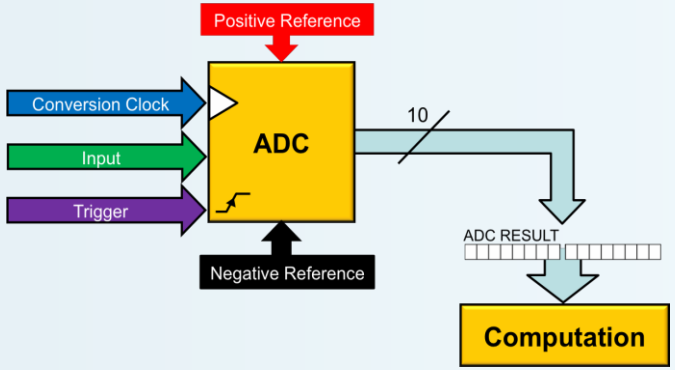
Introducción a las nuevas Familias de Microchip

ADCC

Características:

- Funciones matemáticas automatizadas en señales de entrada, como promedios, cálculos de filtros, sobre muestreo y comparación de umbrales.
- Automatiza el muestreo táctil



ZCD - Zero-Cross Detect

Características:

- Detecta cuando la señal de CA en el pin cruza por cero.

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Introducción a las nuevas Familias de Microchip

Intelligent Analog
Sensor Interfacing & Signal Conditioning

Waveform Control
PWM Drive & Waveform Generation

Timing & Measurements
Signal Measurement with Timing & Counter Control

Logic & Math
Customizable Logic & Math Functions

Safety & Monitoring
Hardware Monitoring & Fault Detection

Communications
Wired, Wireless & Encryption

User Interface
Capacitive Touch Sensing & LCD Control

Low Power & System Flexibility
XLP Low Power Technology, Peripheral & Interconnects

8-bit PIC® and AVR ® Microcontrollers

CPU		Memory		
8-/10-/12-bit ADC	(Enhanced) Capture/ Compare/ PWM	Input Capture	Direct Memory Access Controller	Configurable Custom Logic
ADC with Gain Stage	Complementary Output Generator	Angular Timer	High Endurance Flash (Data)	Configurable Logic Cell
ADC with Computation*	Complementary Waveform Generator	Charge Time Measurement	Event System	Crypto Engine AES/DES
Comparators	Data Signal Modulator	RTC/C	IDLE & DOZE	CAN
DAC	Numerically Ctld Oscillator	Signal Measurement Timer	Peripheral Module Disable	(E)USART
High Speed Comparators*	Programmable Switch Mode Cntlr	8-/12-/16-/20-/24-bit Timers	Peripheral Pin Select	ETHERNET MAC
Operational Amplifiers*	10b/12b/16b PWM	Quadrature Decoder	eXtreme Low Power XLP Technology	I²C/TWI
Ramp Generator*	Waveform Extension	Output Compare	picoPower	LIN
Slope Compensation*	Clock Failure Detection	mTouch® solution	EEPROM	SPI™
Voltage Reference	Cyclical Redundancy Check	Qtouch Solution	External Bus Interface	Keeloq® Sub-GHz RF
Zero Cross Detect*	Hardware Limit Timer	Peripheral Touch Controller	Hardware Multiply	Crystal Free USB
High Current I/O*	Windowed WDT	LCD	Math Accelerator	Full-Speed USB Device w/w/o OTG
TEMP Indicator/Sensor	Brown-Out Detection			IRCOM

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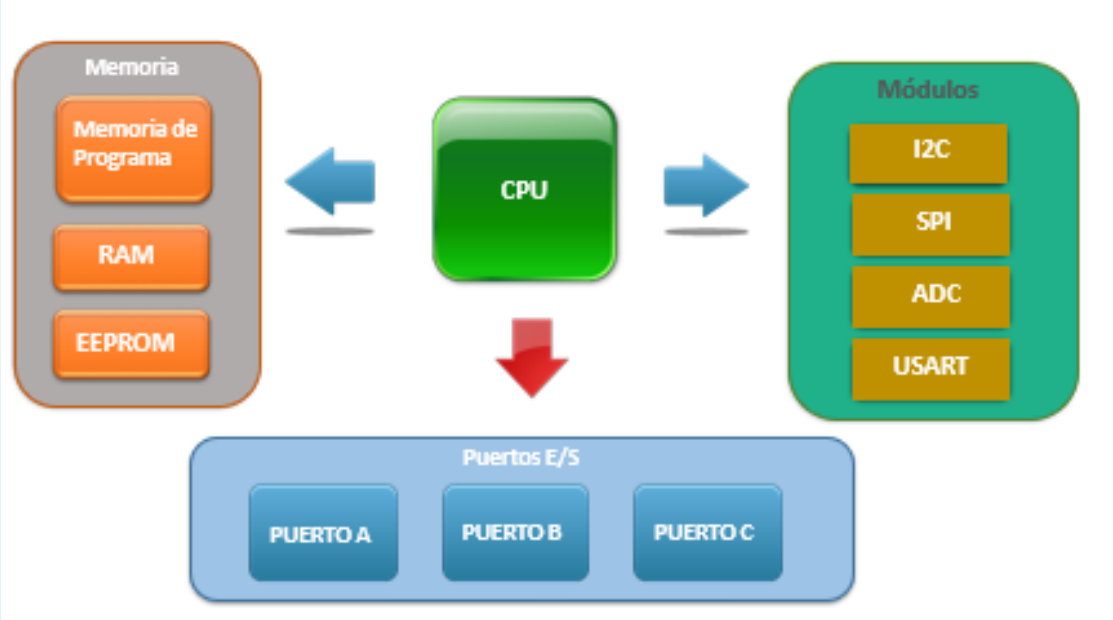
Arquitectura de los PIC18



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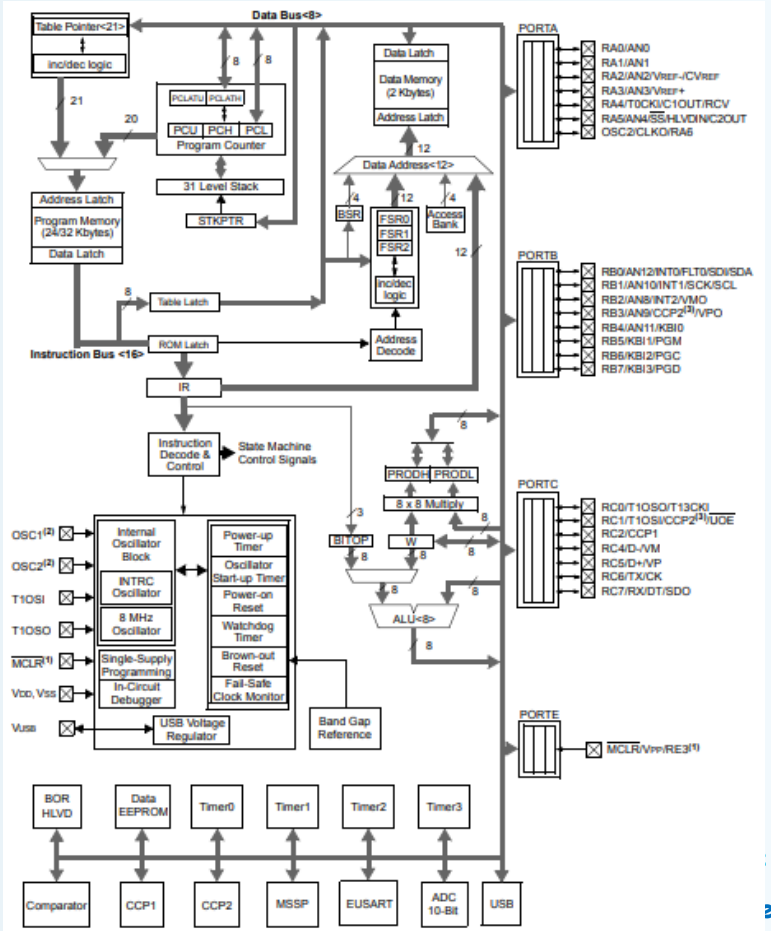
Arquitectura de los PIC18



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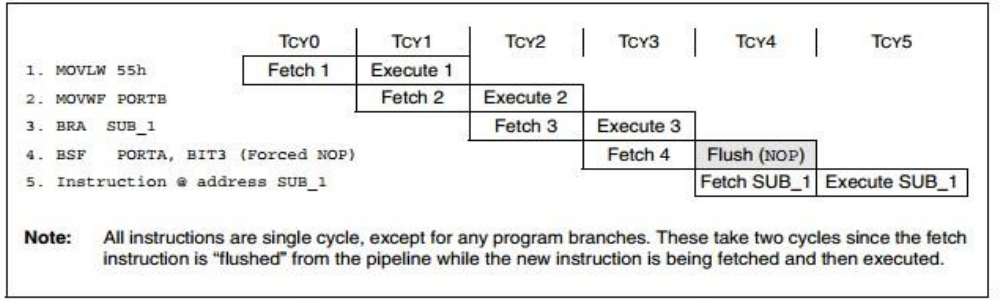
Arquitectura de los PIC18



4 ciclos de reloj (4 ***Tosc***)

hacen 1 ciclo máquina (***TCY***).

¿Qué valor tiene 1 ***TOSC***? y 1 ***TCY***?

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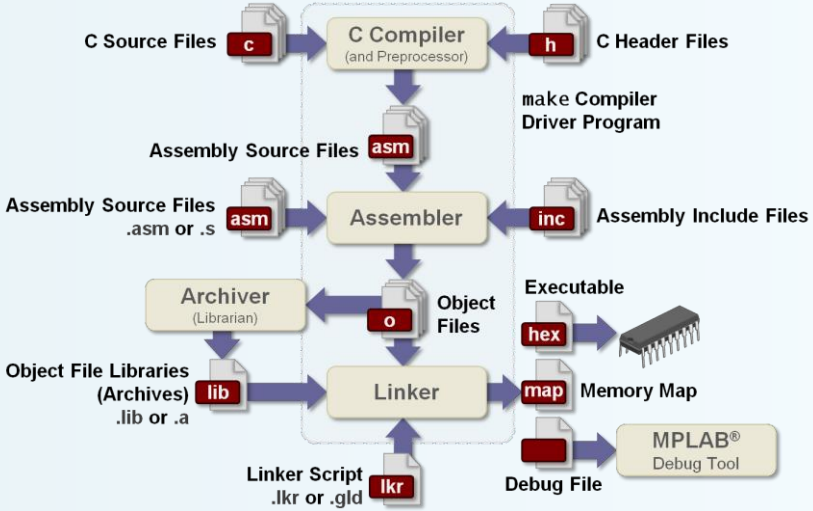
Arquitectura de los PIC18

¿Cuál es la función de un compilador?

Traducir el lenguaje de alto nivel (Lenguaje C, Basic,etc.) a lenguaje Ensamblador.



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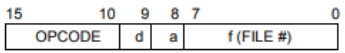
Lenguaje Ensamblador, XC8 pic-ass

Byte-oriented file register operations

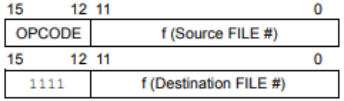


d = 0 for result destination to be WREG register
d = 1 for result destination to be file register (f)
a = 0 to force Access Bank
a = 1 for BSR to select bank
f = 8-bit file register address

Example Instruction

```
ADDWF MYREG, W, B
```

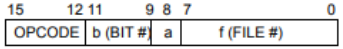
Byte to Byte move operations (2-word)



f = 12-bit file register address

```
MOVFF MYREG1, MYREG2
```

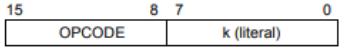
Bit-oriented file register operations



b = 3-bit position of bit in file register (f)
a = 0 to force Access Bank
a = 1 for BSR to select bank
f = 8-bit file register address

```
BSF MYREG, bit, B
```

Literal operations

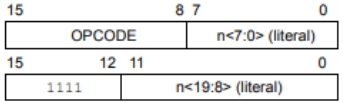


k = 8-bit immediate value

```
MOVLW 7Fh
```

Control operations

CALL, GOTO and Branch operations




```
GOTO Label
```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Lenguaje Ensamblador, XC8 pic-ass

Destino y Accesos de Operacion

Style	Wreg destination	File register destination
XC8	,w	,f
MPASM	,0	,1

Acceso y operaciones con la RAM

Style	Banked access	Unbanked access
XC8	,b	,c or ,a
MPASM	,1	,0

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Lenguaje Ensamblador, XC8 pic-ass

Selección de banco y página

```
movlw 20
BANKSEL(_foobar)    ;select bank for next file instruct
movwf BANKMASK(_foobar)  ;write data and mask address
```

Constantes numéricas

Radix	Format
Binary	Digits 0 and 1 followed by `B`
Octal	Digits 0 to 7 followed by `O`, `Q`, `o` or `q`
Decimal	Digits 0 to 9 followed by `D`, `d` or nothing
Hexadecimal	Digits 0 to 9, A to F preceded by `0x` or followed by `H` or `h`

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Lenguaje Ensamblador, XC8 pic-ass

Operadores en Assembler

Operator	Purpose	Example
*	multiplication	movlw 4*33,w
+	addition	bra $+1
-	subtraction	DB 5-2
/	division	movlw 100/4
= or eq	equality	IF inp eq 66
> or gt	signed greater than	IF inp > 40
>= or ge	signed greater than or equal to	IF inp ge 66
< or lt	signed less than	IF inp < 40
<= or le	signed less than or equal to	IF inp le 66
<> or ne	signed not equal to	IF inp <> 40
low	low byte of operand	movlw low(inp)
high	high byte of operand	movlw high(1008h)
highword	high 16 bits of operand	DW highword(inp)
mod	modulus	movlw 77mod4
& or and	bitwise AND	clrf inp&0ffh
^	bitwise XOR (exclusive or)	movf inp^80,w
|	bitwise OR	movf inp|1,w
not	bitwise complement	movlw not 055h,w
<< or shl	shift left	DB inp>>8
>> or shr	shift right	movlw inp shr 2,w
rol	rotate left	DB inp rol 1
ror	rotate right	DB inp ror 1
float24	24-bit version of real operand	DW float24(3.3)
nul	tests if macro argument is null	

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Lenguaje Ensamblador, XC8 pic-ass

Directivas en Assembler

Directive	Purpose
ALIGN	Aligns output to the specified boundary.
ASMOPT	Controls whether subsequent code is optimized by the assembler.
BANKSEL	Generates code to select bank of operand.
CALLSTACK	Indicates the call stack depth remaining.
[NO]COND	Controls inclusion of conditional code in the listing file.
CONFIG	Specifies configuration bits.
DB	Defines constant byte(s).
DW	Defines constant word(s).
DS	Reserves storage.
DABS	Defines absolute storage.
DLABS	Define linear-memory absolute storage.
DDW	Defines double-width constant word(s).
ELSE	Alternates conditional assembly.
ELSIF	Alternates conditional assembly.
ENDIF	Ends conditional assembly.
END	Ends assembly.
ENDM	Ends macro definition.
EQU	Defines symbol value.
ERROR	Generates a user-defined error.
[NO]EXPAND	Controls expansion of assembler macros in the listing file.
EXTRN	Links with global symbols defined in other modules.
FNADDR	Indicates a routine's address has been taken.

Directive	Purpose
FNARG	Indicates calls in a routine's arguments.
FNBREAK	Breaks links in the call graph.
FNCALL	Indicates call hierarchy.
FNCONF	Indicates call stack settings.
FNINDIR	Indicates indirect calls made by routines.
FNSIZE	Indicates the size of a routines auto and parameter objects.
FNROOT	Indicates the root of a call tree.
GLOBAL	Makes symbols accessible to other modules or allow reference to other global symbols defined in other modules.
IF	Conditional assembly.
INCLUDE	Textually includes the content of the specified file.
IRP	Repeats a block of code with a list.
IRPC	Repeats a block of code with a character list.
[NO]LIST	Defines options for listing file.
LOCAL	Defines local tabs.
MACRO	Macro definition.
MESSG	Generates a user-defined advisory message.
ORG	Sets location counter within current psect.
PAGELEN	Specifies the length of the listing file page.
PAGESEL	Generates set/clear instruction to set PCLATH bits for this page.
PAGEWIDTH	Specifies the width of the listing file page.
PROCESSOR	Defines the particular chip for which this file is to be assembled.
PSECT	Declares or resumes program section.
RADIX	Specifies radix for numerical constants.
REPT	Repeats a block of code n times.
SET	Defines or re-defines symbol value.
SIGNAT	Defines function signature.
SUBTITLE	Specifies the subtitle of the program for the listing file.
TITLE	Specifies the title of the program for the listing file.

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MUCHAS GRACIAS

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