

CENG513 Compiler Design and Construction Instruction Selection

Note by Işıl ÖZ:

Our slides are adapted from Cooper and Torczon's slides that are prepared for COMP 412 at Rice.

Copyright 2010, Keith D. Cooper & Linda Torczon, all rights reserved.

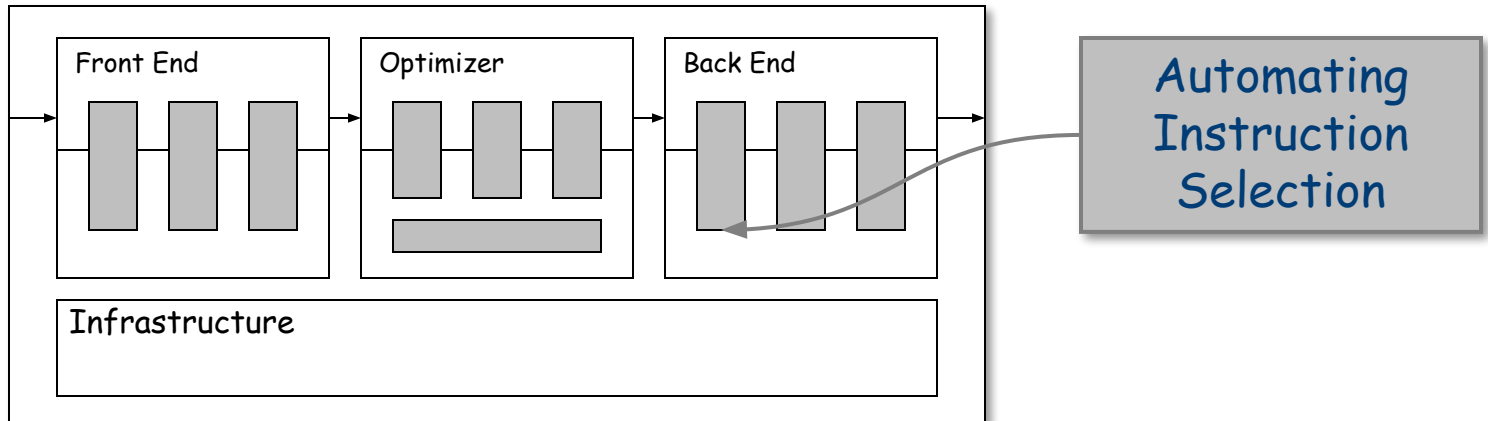
Students enrolled in Comp 412 at Rice University have explicit permission to make copies of these materials for their personal use.

Faculty from other educational institutions may use these materials for nonprofit educational purposes, provided this copyright notice is preserved.

The Problem

Writing a compiler is a lot of work

- Would like to reuse components whenever possible
- Would like to automate construction of components



- Front end construction is largely automated
- Middle is largely hand crafted
- (Parts of) back end can be automated

Definitions

Instruction selection

- Mapping IR into assembly code
- Assumes a fixed storage mapping & code shape
- Combining operations, using address modes

Instruction scheduling

- Reordering operations to hide latencies
- Assumes a fixed program (*set of operations*)
- Changes demand for registers

Register allocation

- Deciding which values will reside in registers
- Changes the storage mapping, may add false sharing
- Concerns about placement of data & memory operations

ILOC - Instruction Set Review

Linear assembly code for a simple abstract RISC machine

Typical ILOC instructions (EaC Appendix A)

load	r_1	$\Rightarrow r_2$	$r_2 = \text{Mem}[r_1]$
loadI	c_1	$\Rightarrow r_1$	$r_1 = c_1$
loadAI	r_1, c_1	$\Rightarrow r_2$	$r_2 = \text{Mem}[r_1 + c_1]$
loadA0	r_1, r_2	$\Rightarrow r_3$	$r_3 = \text{Mem}[r_1 + r_2]$
store	r_1	$\Rightarrow r_2$	$\text{Mem}[r_2] = r_1$
storeAI	r_1	$\Rightarrow r_2, c_1$	$\text{Mem}[r_2 + c_1] = r_1$
storeA0	r_1	$\Rightarrow r_2, r_3$	$\text{Mem}[r_2 + r_3] = r_1$
i2i	r_1	$\Rightarrow r_2$	$r_2 = r_1$
add	r_1, r_2	$\Rightarrow r_3$	$r_3 = r_1 + r_2$
addI	r_1, c_1	$\Rightarrow r_2$	$r_2 = r_1 + c_1$
Similar for arithmetic, logical, and shifts			
jump	r_1		$\text{PC} = r_1$
jumpI	l_1		$\text{PC} = l_1$
cbr	r_1	$\Rightarrow l_1, l_2$	$\text{PC} = r_1 ? l_1 : l_2$

The Problem

Modern computers (still) have many ways to do anything

Consider register-to-register copy in ILOC

- Obvious operation is $r_i \Rightarrow r_j$
- Many others exist

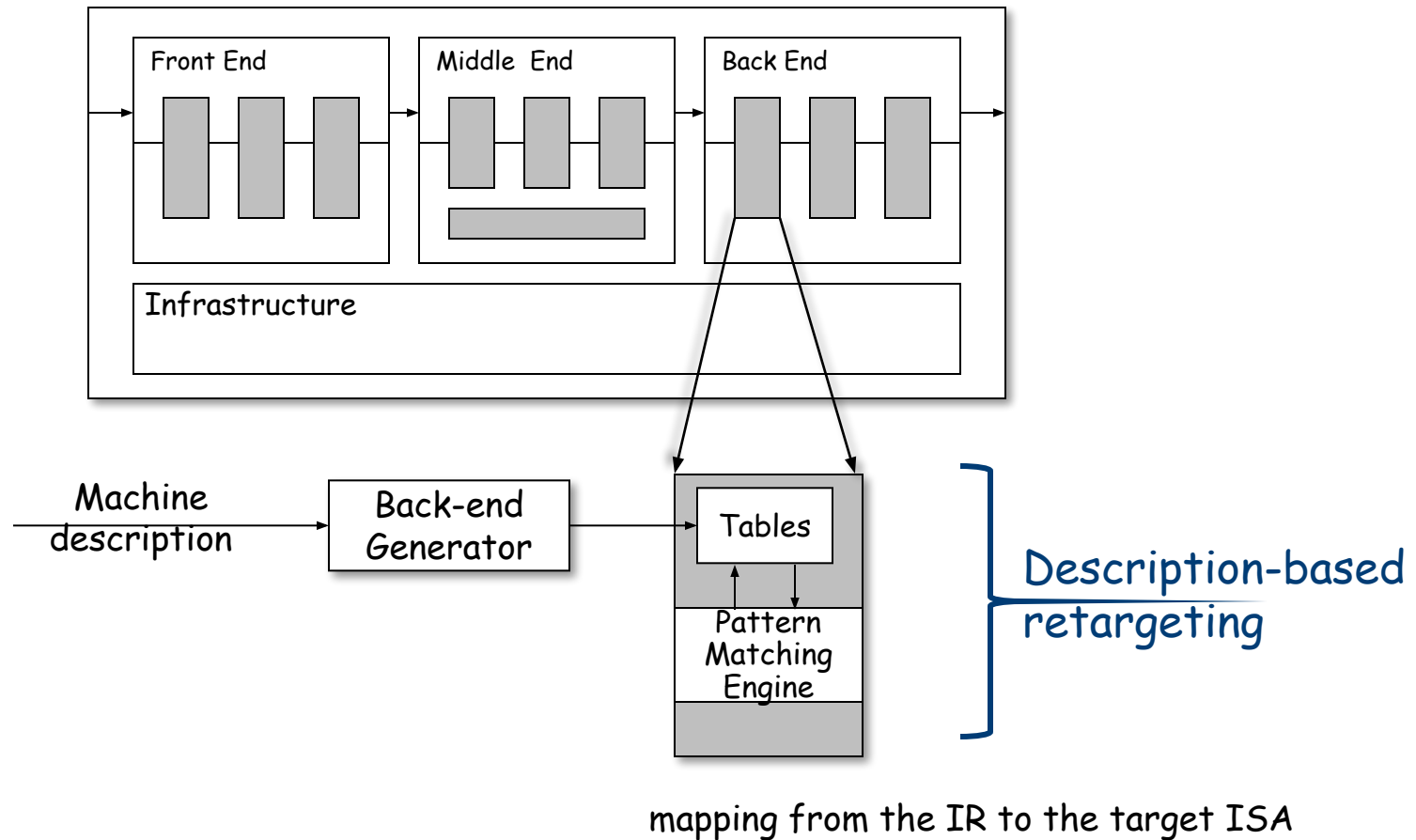
addl $r_i, 0 \Rightarrow r_j$	subl $r_i, 0 \Rightarrow r_j$	lshifl $r_i, 0 \Rightarrow r_j$
multl $r_i, 1 \Rightarrow r_j$	divl $r_i, 1 \Rightarrow r_j$	rshifl $r_i, 0 \Rightarrow r_j$
orl $r_i, 0 \Rightarrow r_j$	xorl $r_i, 0 \Rightarrow r_j$... and others ...

- Human would ignore all of these
- Algorithm must look at all of them & find low-cost encoding
 - Take context into account *(busy functional unit?)*

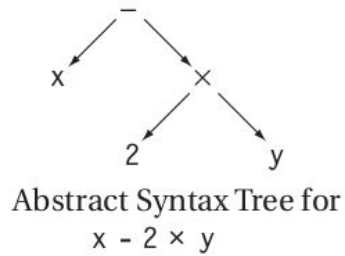
And ILOC is an overly-simplified case

The Goal

Want to automate generation of instruction selectors



Simple Tree-Walk for Expressions



```
loadI  @x      ⇒ r1
loadA0  rarp, r1 ⇒ r2
loadI   2       ⇒ r3
loadI  @y      ⇒ r4
loadA0  rarp, r4 ⇒ r5
mult    r3, r5 ⇒ r6
sub     r2, r6 ⇒ r7
```

Tree-Walk Code Generator

```
expr(node) {
    int result, t1, t2;
    switch(type(node)) {
        case X, ÷, +, -:
            t1 ← expr(LeftChild(node));
            t2 ← expr(RightChild(node));
            result ← NextRegister();
            emit(op(node), t1, t2, result);
            break;

        case IDENT:
            t1 ← base(node);
            t2 ← offset(node);
            result ← NextRegister();
            emit(loadA0, t1, t2, result);
            break;

        case NUM:
            result ← NextRegister();
            emit(loadI, val(node), none,
                result);
            break;
    }
    return result;
}
```


Simple Tree-Walk Routine for Variables and Numbers

case IDENT:

```
t1  $\leftarrow$  base(node);  
t2  $\leftarrow$  offset(node);  
result  $\leftarrow$  NextRegister();  
emit (loadA0, t1, t2, result);  
break;
```

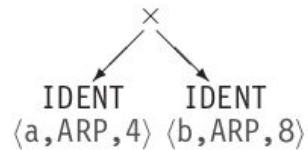
case NUM:

```
result  $\leftarrow$  NextRegister();  
emit (loadI, val(node),  
      none, result);  
break;
```

***emit* (*Op*, *src1*, *src2*, *dest*)**

Naive Selection - Tree Walk

a × b



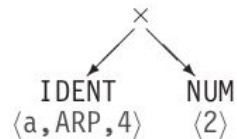
```

loadI  4      ⇒ r5
loadAO r_arp, r5 ⇒ r6
loadI  8      ⇒ r7
loadAO r_arp, r7 ⇒ r8
mult   r6, r8  ⇒ r9
  
```

```

loadAI r_arp, 4 ⇒ r5
loadAI r_arp, 8 ⇒ r6
mult   r5, r6  ⇒ r7
  
```

a × 2



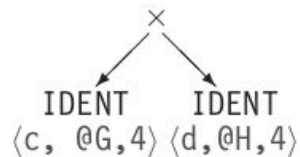
```

loadI  4      ⇒ r5
loadAO r_arp, r5 ⇒ r6
loadI  2      ⇒ r7
mult   r6, r7  ⇒ r8
  
```

```

loadAI r_arp, 4 ⇒ r5
multI  r5, 2    ⇒ r6
  
```

c × d



```

loadI @G      ⇒ r5
loadI  4      ⇒ r6
loadAO r5, r6  ⇒ r7
loadI @H      ⇒ r8
loadI  4      ⇒ r9
loadAO r8, r9  ⇒ r10
mult   r7, r10 ⇒ r11
  
```

```

loadI  4      ⇒ r5
loadAI r5, @G  ⇒ r6
loadAI r5, @H  ⇒ r7
mult   r6, r7  ⇒ r8
  
```

Pattern Matching

Need pattern matching techniques to transform IR sequences to assembly sequences

- Must produce good code *(some metric for good)*
- Must run quickly

When the code generator considers multiple possible matches for a given sub-tree, it needs a way to choose among them

If the compiler writer can associate a cost with each pattern, then the matching scheme can select patterns in a way that minimizes the costs

Need to describe the target machine's ISA in a formal notation

- Tree pattern matching
- Peephole optimization

How do we perform this kind of matching ?

Tree-oriented IR suggests pattern matching on trees

- Process takes tree-patterns as input, matcher as output
- Each pattern maps to a target-machine instruction sequence
- Use dynamic programming or bottom-up rewrite systems

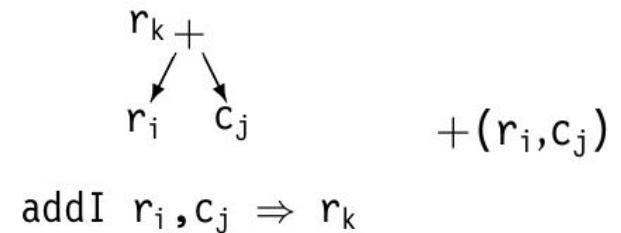
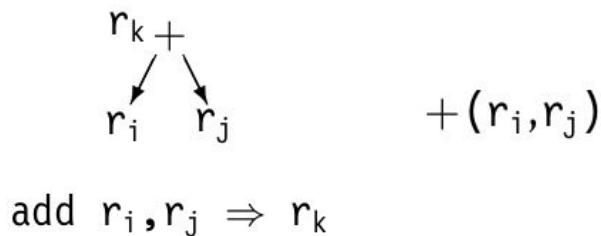
Linear IR suggests using some sort of string matching

- Process takes strings as input, matcher as output
- Each string maps to a target-machine instruction sequence
- Use text matching (Aho-Corasick) or peephole matching

In practice, both work well; matchers are quite different

Tree Pattern Matching - Low-Level AST

Both the IR form of the program and the target machine's instruction set must be expressed as trees

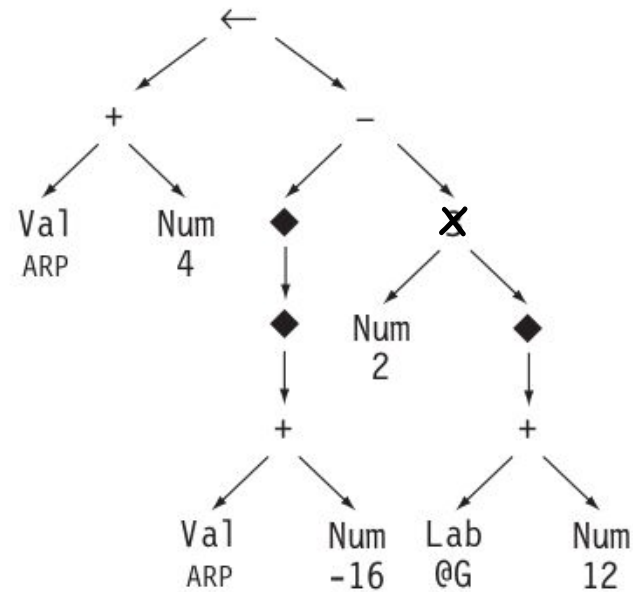


IR is in low level AST form exposing storage type of operands

Tile AST with operation trees

Recursively tile tree and bottom-up select the cheapest tiling

Low-Level AST for $w \leftarrow x - 2 \times y$



$\leftarrow (+(\text{Val}_1, \text{Num}_1), -(\diamond(\diamond(+(\text{Val}_2, \text{Num}_2))), \times(\text{Num}_3, \diamond(+(\text{Lab}_1, \text{Num}_4)))))$

Tree Pattern Matching - Rewrite Rules

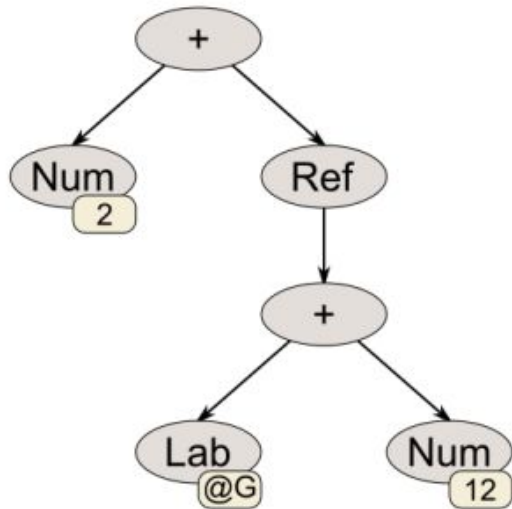
Operations are connected to AST subtrees by a set of ambiguous rewrite rules

Rules have costs - ambiguity allows cost based choice

Subset of rules

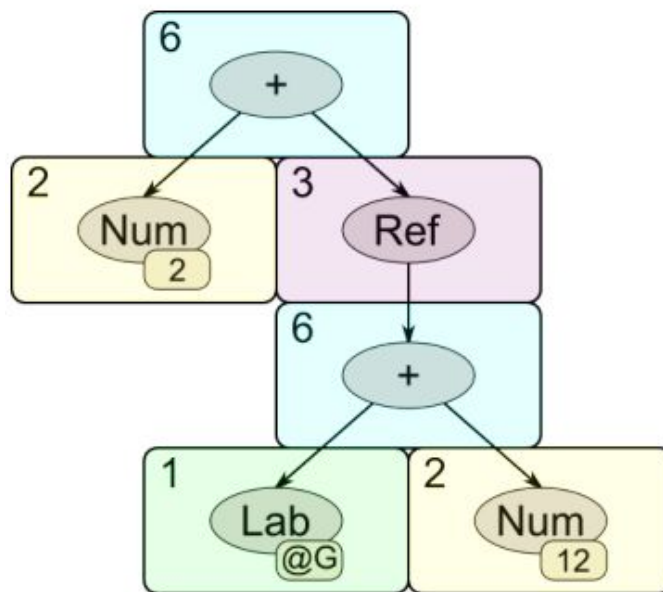
Id	Production	Code Template
1:	$Reg \rightarrow Lab$	loadI $ b \Rightarrow r_{new}$
2:	$Reg \rightarrow Num$	loadI $n_1 \Rightarrow r_{new}$
3:	$Reg \rightarrow Ref(Reg)$	load $r_1 \Rightarrow r_{new}$
4:	$Reg \rightarrow Ref(+ (Reg_1, Reg_2))$	loadA0 $r_1, r_2 \Rightarrow r_{new}$
5:	$Reg \rightarrow Ref(+ (Reg, Num))$	loadAI $r_1, n_1 \Rightarrow r_{new}$
6:	$Reg \rightarrow + (Reg_1, Reg_2)$	add $r_1, r_2 \Rightarrow r_{new}$
7:	$Reg \rightarrow + (Reg, Num)$	addI $r_1, n_1 \Rightarrow r_{new}$
8:	$Reg \rightarrow + (Num, Reg)$	addI $r_1, n_1 \Rightarrow r_{new}$

Tree Pattern Matching - Tiling



Begin tiling AST bottom up

Tree Pattern Matching - Tiling



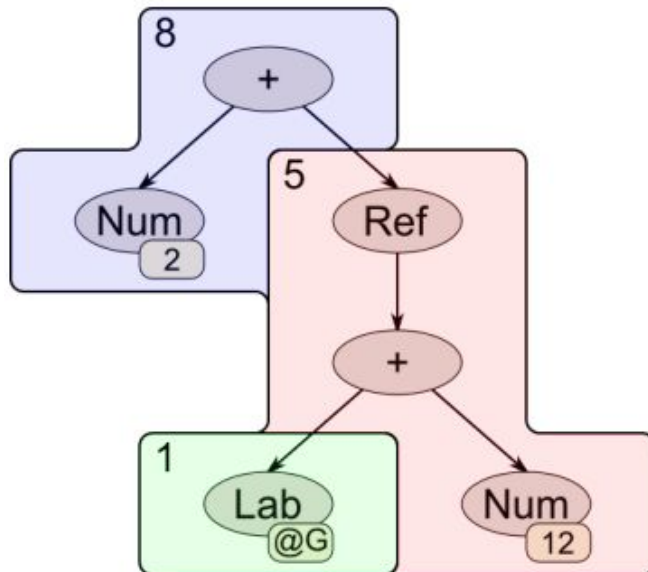
Code produced

```
loadI  @G    ⇒ r1
loadI  12    ⇒ r2
      add  r1, r2 ⇒ r3
      load  r3    ⇒ r4
loadI  2      ⇒ r5
      add  r4, r5 ⇒ r6
```

Bad tiling: productions used

1: $Reg \rightarrow Lab$	$loadI\ lbl \Rightarrow r_{new}$
2: $Reg \rightarrow Num$	$loadI\ n_1 \Rightarrow r_{new}$
3: $Reg \rightarrow Ref(Reg)$	$load\ r_1 \Rightarrow r_{new}$
6: $Reg \rightarrow +(Reg_1, Reg_2)$	$add\ r_1, r_2 \Rightarrow r_{new}$

Tree Pattern Matching - Tiling



- Many different sequences available
- Selecting lowest cost bottom-up gives

Code produced

```
loadI  @G    ⇒ r1
loadAI  r1, 12 ⇒ r2
addI    r2, 2  ⇒ r3
```

Good tiling: productions used

1: $Reg \rightarrow Lab$	$loadI \text{ } b \Rightarrow r_{new}$
5: $Reg \rightarrow Ref(+ (Reg, Num))$	$loadAI \text{ } r_1, n_1 \Rightarrow r_{new}$
8: $Reg \rightarrow + (Num, Reg)$	$addI \text{ } r_1, n_1 \Rightarrow r_{new}$

Tree Pattern Matching - Cost-Based Selection

- If, at each match, the code generator retains the lowest-cost matches, it will produce a locally optimal tiling
- This bottom-up accumulation of costs implements a dynamic-programming solution to find the minimal-cost tiling
- The cost function depends, inherently, on the target processor; it cannot be derived automatically from the grammar
- It must encode properties of the target machine and reflect the interactions that occur between operations in an assembly program—particularly the flow of values from one operation to another
- Examples assume all operations are equal cost, certain ops may be more expensive - divs

Peephole Matching

Basic idea

- Compiler can discover local improvements locally
 - Look at a small set of adjacent operations
 - Move a “peephole”-sliding window- over code
 - Search for improvement
- Classic example was store followed by load

Original code

storeAI $r_1 \Rightarrow r_0, 8$
loadAI $r_0, 8 \Rightarrow r_{15}$

Improved code

storeAI $r_1 \Rightarrow r_0, 8$
i2i $r_1 \Rightarrow r_{15}$

Peephole Matching

Basic idea

- Compiler can discover local improvements locally
 - Look at a small set of adjacent operations
 - Move a “peephole”-sliding window- over code
 - Search for improvement
- Simple algebraic identities

Original code

addI $r_2, 0 \Rightarrow r_7$
mult $r_4, r_7 \Rightarrow r_{10}$

multI $r_5, 2 \Rightarrow r_7$

Improved code

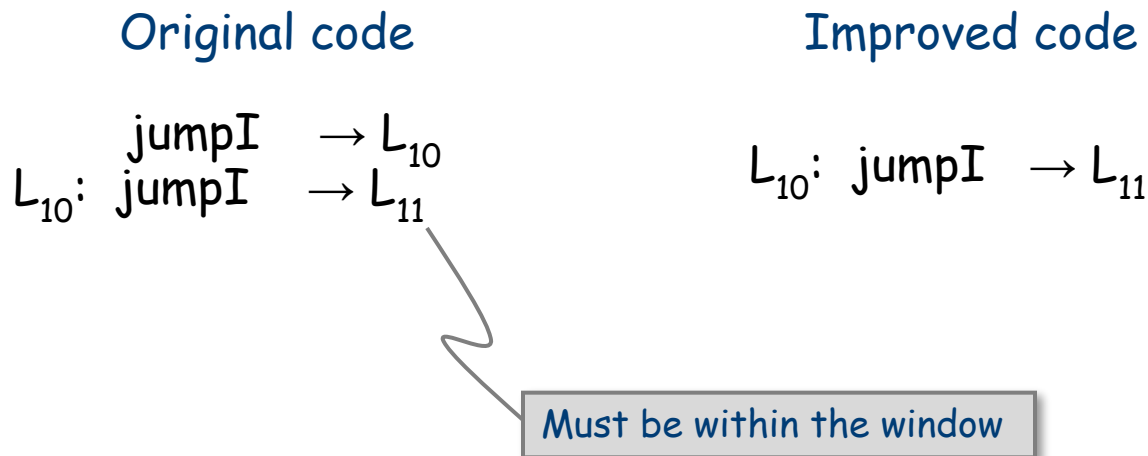
mult $r_4, r_2 \Rightarrow r_{10}$

add $r_2, r_2 \Rightarrow r_7$

Peephole Matching

Basic idea

- Compiler can discover local improvements locally
 - Look at a small set of adjacent operations
 - Move a “peephole”-sliding window- over code
 - Search for improvement
- Jump to a jump



Peephole Matching

Implementing it

- Early systems used limited set of hand-coded patterns
- Window size ensured quick processing

Modern peephole instruction selectors

- Break problem into three tasks



- Apply symbolic interpretation & simplification systematically

Peephole Matching

Expander

- Turns IR code into a low-level IR (LLIR) such as RTL
- Operation-by-operation, template-driven rewriting
- LLIR form includes all direct effects of the operations
- Significant, albeit constant, expansion of size



Peephole Matching

Simplifier

- Looks at LLIR through window and rewrites it
- Uses forward substitution, algebraic simplification, local constant propagation, and dead-effect elimination
- Performs local optimization within window



- This is the heart of the peephole system
 - Benefit of peephole optimization shows up in this step

Peephole Matching

Matcher

- Compares simplified LLIR against a library of patterns
- Picks low-cost pattern that captures effects
- Must preserve LLIR effects, may add new ones
- Generates the assembly code output



Example

$w = x - 2 * y$ becomes

Original IR Code

OP	Arg ₁	Arg ₂	Result
mult	2	y	t ₁
sub	x	t ₁	w

Symbolic names for memory-bound variables

Example

$w = x - 2 * y$ becomes

Original IR Code

OP	Arg ₁	Arg ₂	Result
mult	2	y	t ₁
sub	x	t ₁	w

Symbolic names for memory-bound variables

Expand



LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

Example

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

Simplify



LLIR Code

```
r13 ← MEM(r0 + @y)
r14 ← 2 × r13
r17 ← MEM(r0 + @x)
r18 ← r17 - r14
MEM(r0 + @w) ← r18
```

Example

LLIR Code

```
r13 ← MEM(r0 + @y)
r14 ← 2 × r13
r17 ← MEM(r0 + @x)
r18 ← r17 - r14
MEM(r0 + @w) ← r18
```

Match



ILoc Code

```
loadAI r0,@y ⇒ r13
multI 2 × r13 ⇒ r14
loadAI r0,@x ⇒ r17
sub r17 - r14 ⇒ r18
storeAI r18 ⇒ r0,@w
```

- Introduced all memory operations & temporary names
- Turned out pretty good code

Steps of the Simplifier

(3-operation window)

LLIR Code

$r_{10} \leftarrow 2$

$r_{11} \leftarrow @y$

$r_{12} \leftarrow r_0 + r_{11}$

$r_{13} \leftarrow \text{MEM}(r_{12})$

$r_{14} \leftarrow r_{10} \times r_{13}$

$r_{15} \leftarrow @x$

$r_{16} \leftarrow r_0 + r_{15}$

$r_{17} \leftarrow \text{MEM}(r_{16})$

$r_{18} \leftarrow r_{17} - r_{14}$

$r_{19} \leftarrow @w$

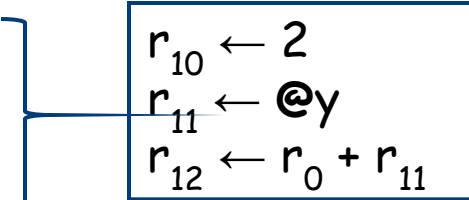
$r_{20} \leftarrow r_0 + r_{19}$

$\text{MEM}(r_{20}) \leftarrow r_{18}$

Steps of the Simplifier (3-operation window)

LLIR Code

```
r10 ← 2  
r11 ← @y  
r12 ← r0 + r11  
r13 ← MEM(r12)  
r14 ← r10 × r13  
r15 ← @x  
r16 ← r0 + r15  
r17 ← MEM(r16)  
r18 ← r17 - r14  
r19 ← @w  
r20 ← r0 + r19  
MEM(r20) ← r18
```



Steps of the Simplifier (3-operation window)

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
```



```
r10 ← 2
r12 ← r0 + @y
r13 ← MEM(r12)
```

Steps of the Simplifier (3-operation window)

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

```
r10 ← 2
r12 ← r0 + @y
r13 ← MEM(r12)
```



```
r10 ← 2
r13 ← MEM(r0 + @y)
r14 ← r10 × r13
```

Steps of the Simplifier (3-operation window)

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

```
r10 ← 2
r13 ← MEM(r0 + @y)
r14 ← r10 × r13
```



```
r13 ← MEM(r0 + @y)
r14 ← 2 × r13
r15 ← @x
```

Folding 2 into computation of r₁₄ made the 1st op dead.

Steps of the Simplifier (3-operation window)

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

$r_{13} \leftarrow \text{MEM}(r_0 + @y)$
 $r_{14} \leftarrow 2 \times r_{13}$
 $r_{15} \leftarrow @x$



$r_{14} \leftarrow 2 \times r_{13}$
 $r_{15} \leftarrow @x$
 $r_{16} \leftarrow r_0 + r_{15}$

Simplifier **emits** ops that are *live* when they roll out of the window.

Steps of the Simplifier (3-operation window)

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

$r_{14} \leftarrow 2 \times r_{13}$
 $r_{15} \leftarrow @x$
 $r_{16} \leftarrow r_0 + r_{15}$



$r_{14} \leftarrow 2 \times r_{13}$
 $r_{16} \leftarrow r_0 + @x$
 $r_{17} \leftarrow \text{MEM}(r_{16})$

Steps of the Simplifier (3-operation window)

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

$r_{14} \leftarrow 2 \times r_{13}$
 $r_{16} \leftarrow r_0 + @x$
 $r_{17} \leftarrow \text{MEM}(r_{16})$



$r_{14} \leftarrow 2 \times r_{13}$
 $r_{17} \leftarrow \text{MEM}(r_0 + @x)$
 $r_{18} \leftarrow r_{17} - r_{14}$

Steps of the Simplifier (3-operation window)

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

$r_{14} \leftarrow 2 \times r_{13}$
 $r_{17} \leftarrow \text{MEM}(r_0 + @x)$
 $r_{18} \leftarrow r_{17} - r_{14}$

$r_{17} \leftarrow \text{MEM}(r_0 + @x)$
 $r_{18} \leftarrow r_{17} - r_{14}$
 $r_{19} \leftarrow @w$

Steps of the Simplifier (3-operation window)

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

$r_{17} \leftarrow \text{MEM}(r_0 + @x)$
 $r_{18} \leftarrow r_{17} - r_{14}$
 $r_{19} \leftarrow @w$



$r_{18} \leftarrow r_{17} - r_{14}$
 $r_{19} \leftarrow @w$
 $r_{20} \leftarrow r_0 + r_{19}$

Steps of the Simplifier (3-operation window)

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

```
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
```



```
r18 ← r17 - r14
r20 ← r0 + @w
MEM(r20) ← r18
```

Steps of the Simplifier (3-operation window)

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

```
r18 ← r17 - r14
r20 ← r0 + @w
MEM(r20) ← r18
```

```
r18 ← r17 - r14
MEM(r0 + @w) ← r18
```

Example

LLIR Code

```
r10 ← 2
r11 ← @y
r12 ← r0 + r11
r13 ← MEM(r12)
r14 ← r10 × r13
r15 ← @x
r16 ← r0 + r15
r17 ← MEM(r16)
r18 ← r17 - r14
r19 ← @w
r20 ← r0 + r19
MEM(r20) ← r18
```

Simplify



LLIR Code

```
r13 ← MEM(r0 + @y)
r14 ← 2 × r13
r17 ← MEM(r0 + @x)
r18 ← r17 - r14
MEM(r0 + @w) ← r18
```

References

Chapter sections from the book:

- 11.1-11.4, Appendix A

Selected videos from compiler course from California State University:

- https://www.youtube.com/watch?v=jKN_kjtb128&list=PL6KMWPQP_DM97HhOPYNgJord-sANFTI3i&index=25