-VIDEO ASSIGNMENT 3-

In the part one of the video Prof. Frank K. Gürkaynak talked about RISC-V instruction set architecture which is an open source ISA which means that anyone can use that ISA freely. Speciality of RISC-V architecture comes from being open source, so that different companies can come up with different implementations of RISC-V core, which allows community of computer architecture to observe certain advantages and disadvantages of particular implementation and improve the architecture further by collaboration. Relatively bad part of RISC-V is that it is still under refinement and adjustment. Also Software tools and development environments should be adapted according to latest chages in RISC-V architecture. RISC-V Compressed instruction extension ‘C’ provides compressed instructions and the least significant bit of instruction format determines the length of the instruction. This property of RISC-V extension ‘C’ increases fetch-bandwith, for example if we have fetched two 16 bit length instructions to 32-bit registers in a single-cycle processor subsequent cycle will not require instruction fetch anymore which increases performance. Another good property of RISC-V architecture is that it is a reduced instruction set computer architecture which means it has small and concise ISA compared to other computer architectures like X86 and ARM7. This property keeps the implementation of microarchitecture simple.

REFERENCES

- https://riscv.org/wp-content/uploads/2015/05/riscv-compressed-spec-v1.7.pdf