

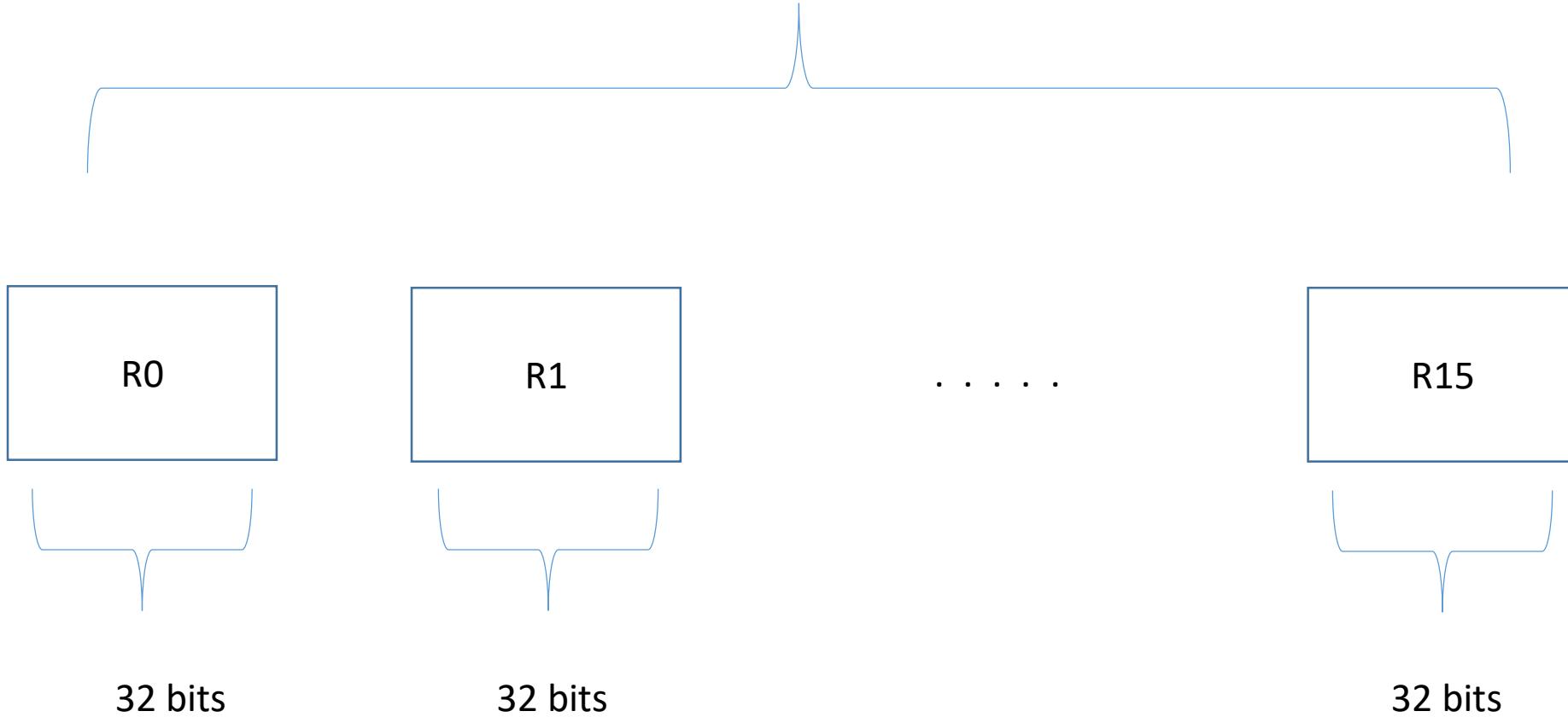
Lecture 10-RTL

FNA

EX 1. A digital system has 16 registers, each with 32 bits. It is necessary to provide parallel data transfer from each register to each other register.

- (a) How many lines are needed for direct parallel transfer?
- (b) How many lines are needed for transfer along a common bus?
- (c) Let the registers in memory be designated by R0 to R15. List the sequence of micro-operations for a transfer of the content of R6 to R13. (Assuming registers form a scratch-pad memory)

16 registers



(a) How many lines are needed for direct parallel transfer?

Let n= num. registers and m= num. bits in each register

$$\text{Total lines} = n*(n-1)*m = 16 * 15 * 32 = 7680$$

(a) How many lines are needed for transfer along a common bus?

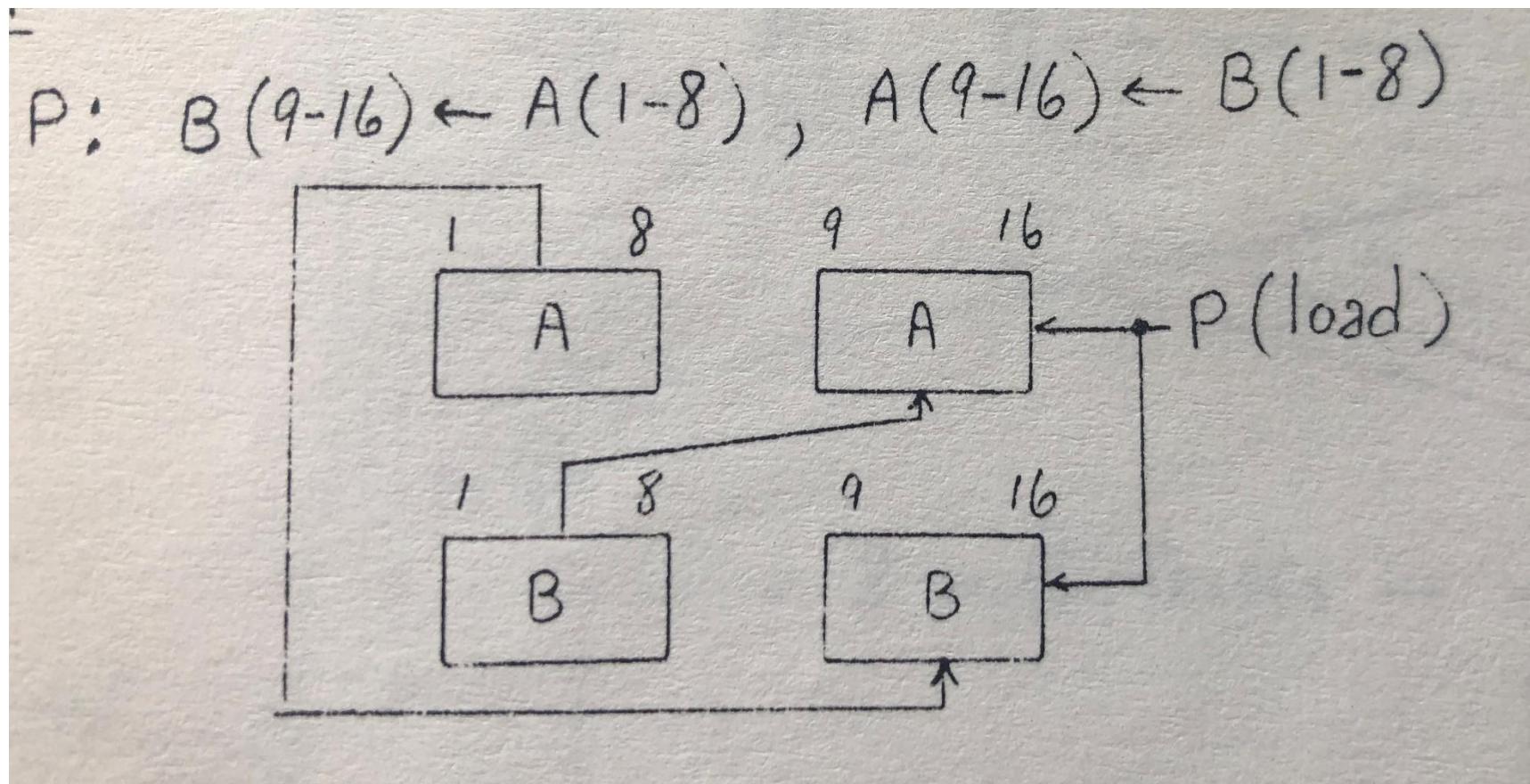
32 lines for the bus + 512 wires ($16 * 32$) from bus to each register

(a) Let the registers in memory be designated by R0 to R15. List the sequence of micro-operations for a transfer of the content of R6 to R13.

0	R0
1	
2	
3	
4	
5	
6	
.	
.	
15	R15

MAR \leftarrow 0110 Address of R6 into MAR
MBR \leftarrow M Read contents of R6 into MBR
MAR \leftarrow 1101 Adress of R13
M \leftarrow MBR Store in R13

Ex 2. List the micro-operations that transfer bits 1-8 of register A to bits 9-16 of register B and bits 1-8 of register B to bits 9-16 of register A. Draw a block diagram of the hardware.



A(1-8)

A(9-16)

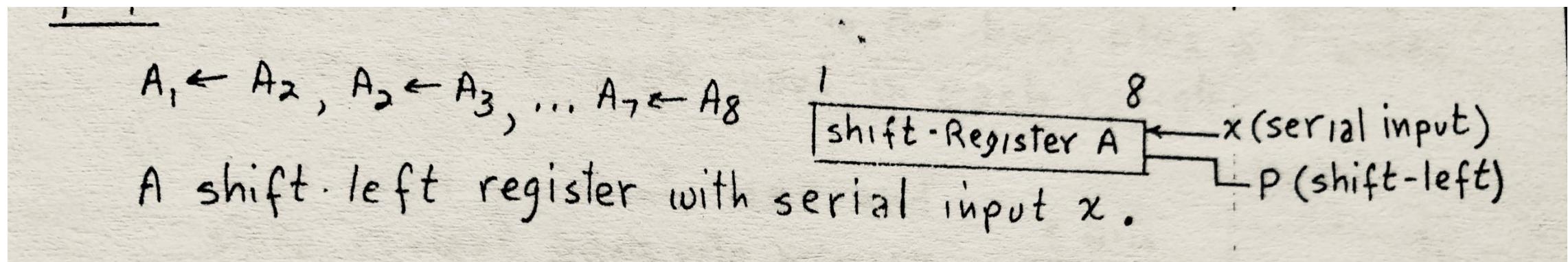
B(1-8)

B(9-16)

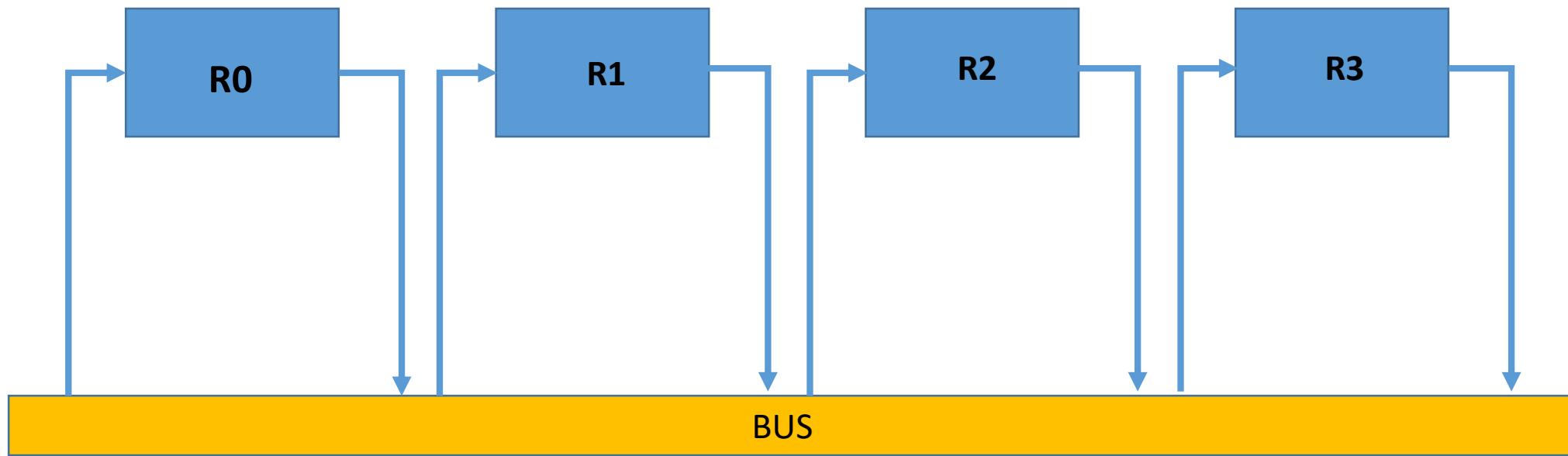
Ex 3. An 8-bit register A has one binary input x. The register operation can be described symbolically as follows:

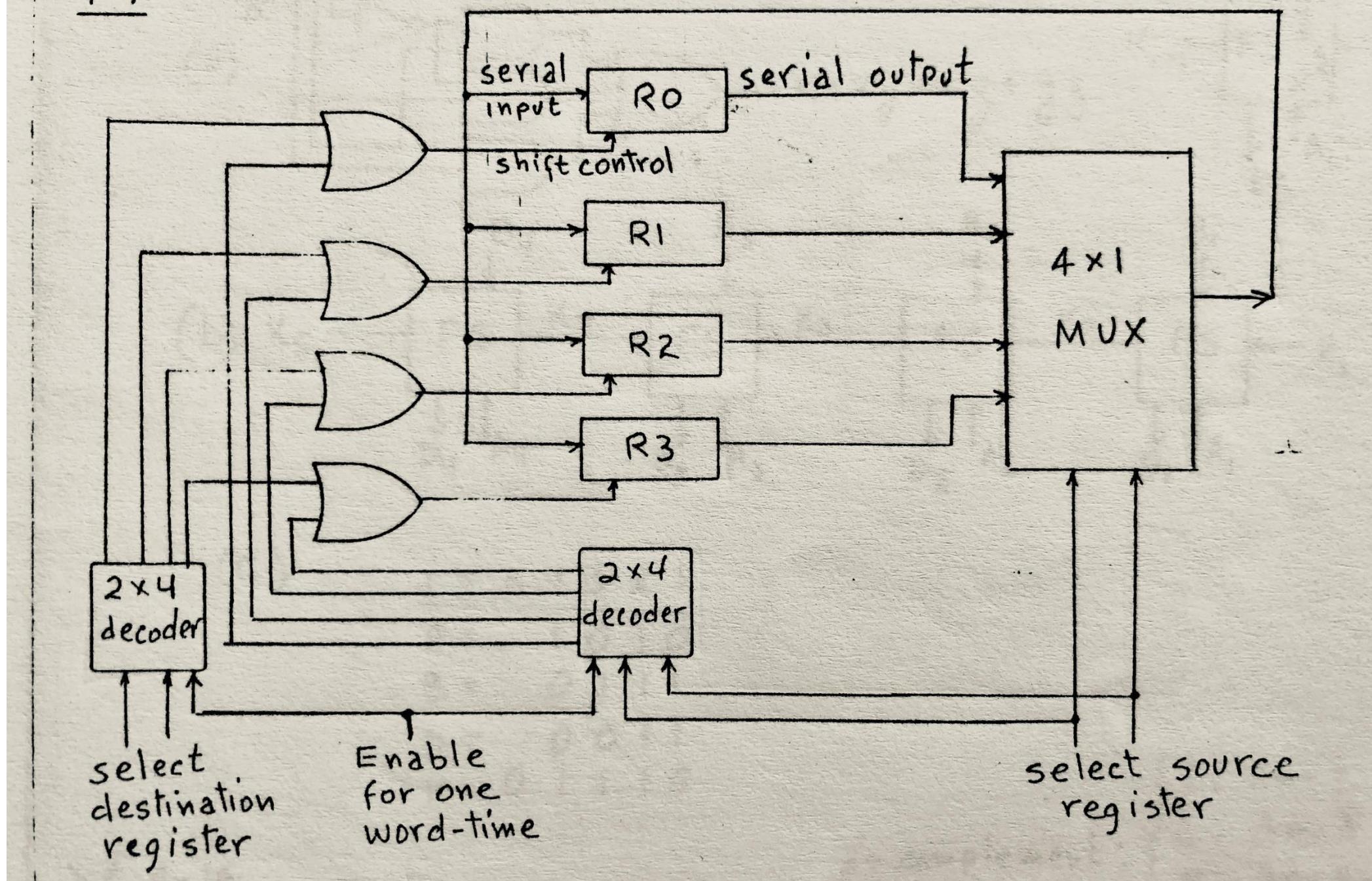
$$P: A_8 \leftarrow x, A_i \leftarrow A_{i+1}, i = 1, 2, 3, \dots, 7$$

What is the function of the register? The cells are numbered from left to right.

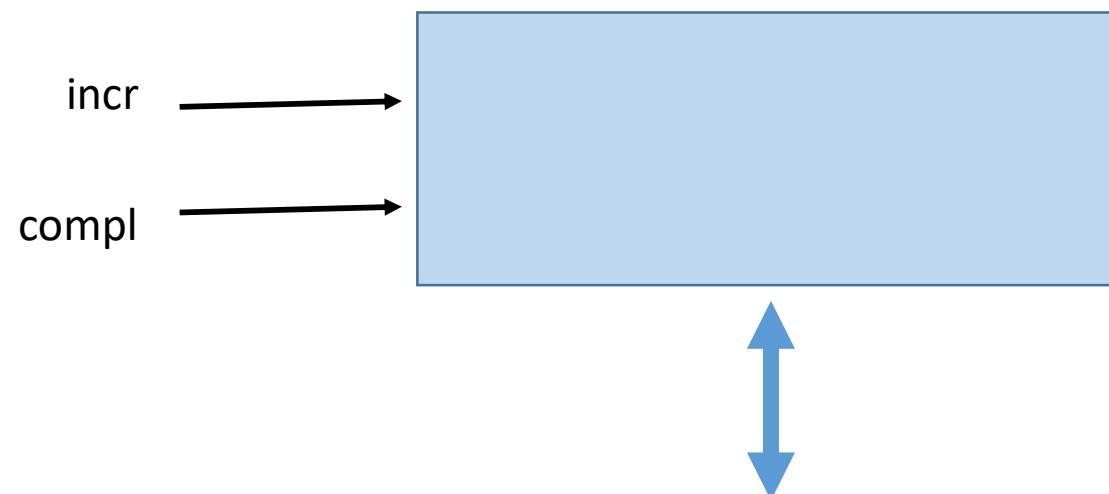


Ex 4. Draw a block diagram of a bus system connected to four registers with information transferred *serially* from any register to any other register. Use a decoder and a multiplexer to select the source register and a decoder to select the destination register.

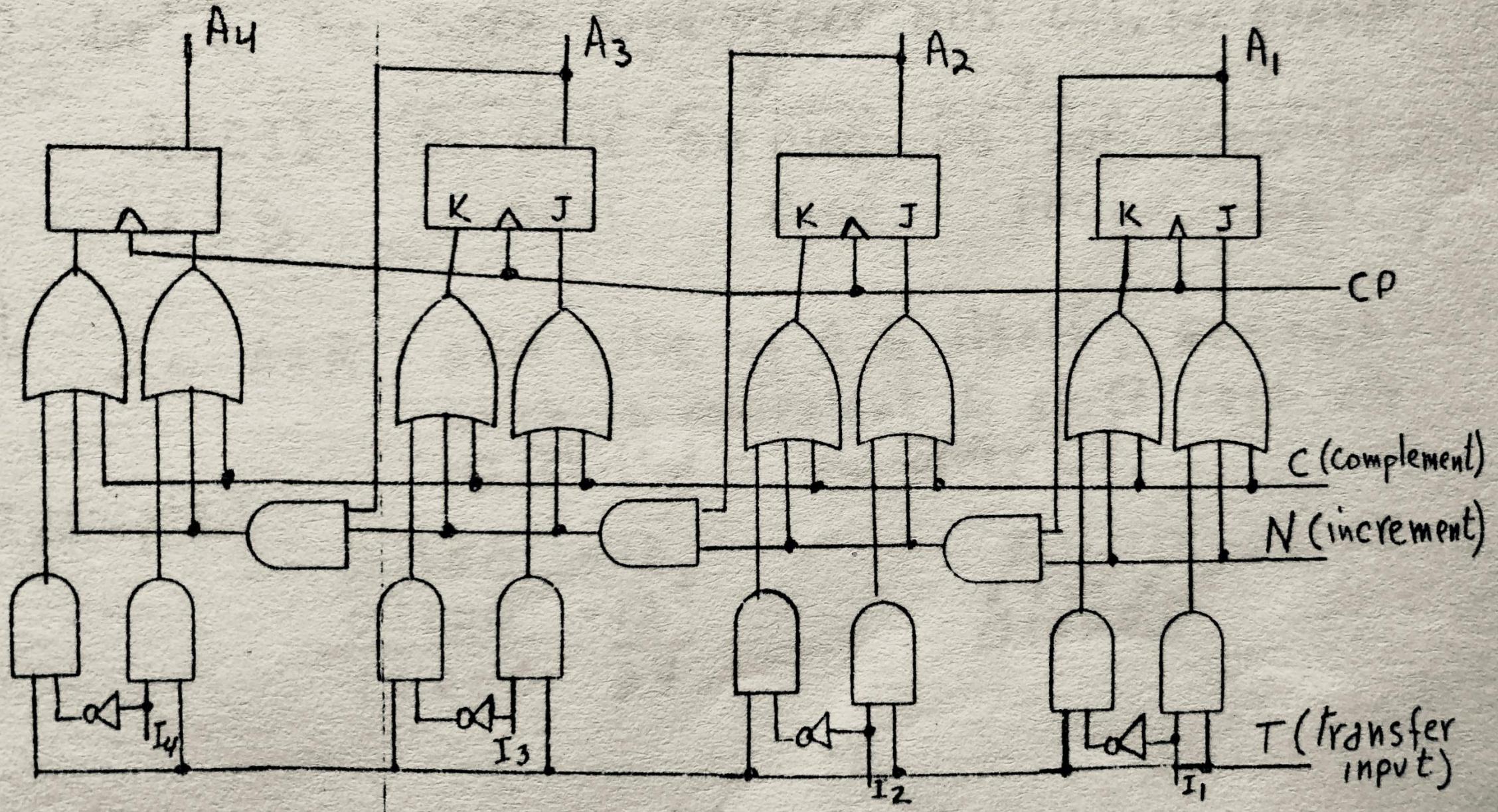




Ex 5. Draw the logic diagram of a 4-bit register with clocked JK-FFs having control inputs for the *increment*, *complement*, and *parallel transfer* micro-operations. Show how the 2's complement can be implemented in this register.



JK Flip-Flop		$Q(t + 1)$
J	K	
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$



Ex 6. The content of register A is 1101 and that of B is 0110. Show that either one of the micro-operation sequences listed below produce the difference 0111.

$$(a) T_1: B \leftarrow B'$$

$$T_2: B \leftarrow B + 1$$

$$T_3: A \leftarrow A + B$$

$$(b) T_1: B \leftarrow B'$$

$$T_2: EA \leftarrow A + B$$

$$ET_3: A \leftarrow A + 1$$

$$A = 1101$$

$$B = 0110$$

$$(a) T_1: B \leftarrow \overline{B} \quad 1001 = B$$

$$T_2: B \leftarrow B + 1 \quad 1010 = B$$
$$\underline{1101} = A$$

$$T_3: A \leftarrow A + B \quad 0111 = A$$

$$(b) T_1: B \leftarrow \overline{B} \quad 1001 = B$$

$$T_2: EA \leftarrow A + B \quad \begin{array}{r} 1101 \\ 0110 \\ \hline 0110 \end{array} = A$$

$$ET_3: A \leftarrow A + 1 \quad 0111 = A$$

1 1 0 1

E

A

0 1 1 0

B

Ex 7. Design a typical stage (similar to the figure below) that implements the following logic operations.

$$P_6 : A \leftarrow A \vee B'$$

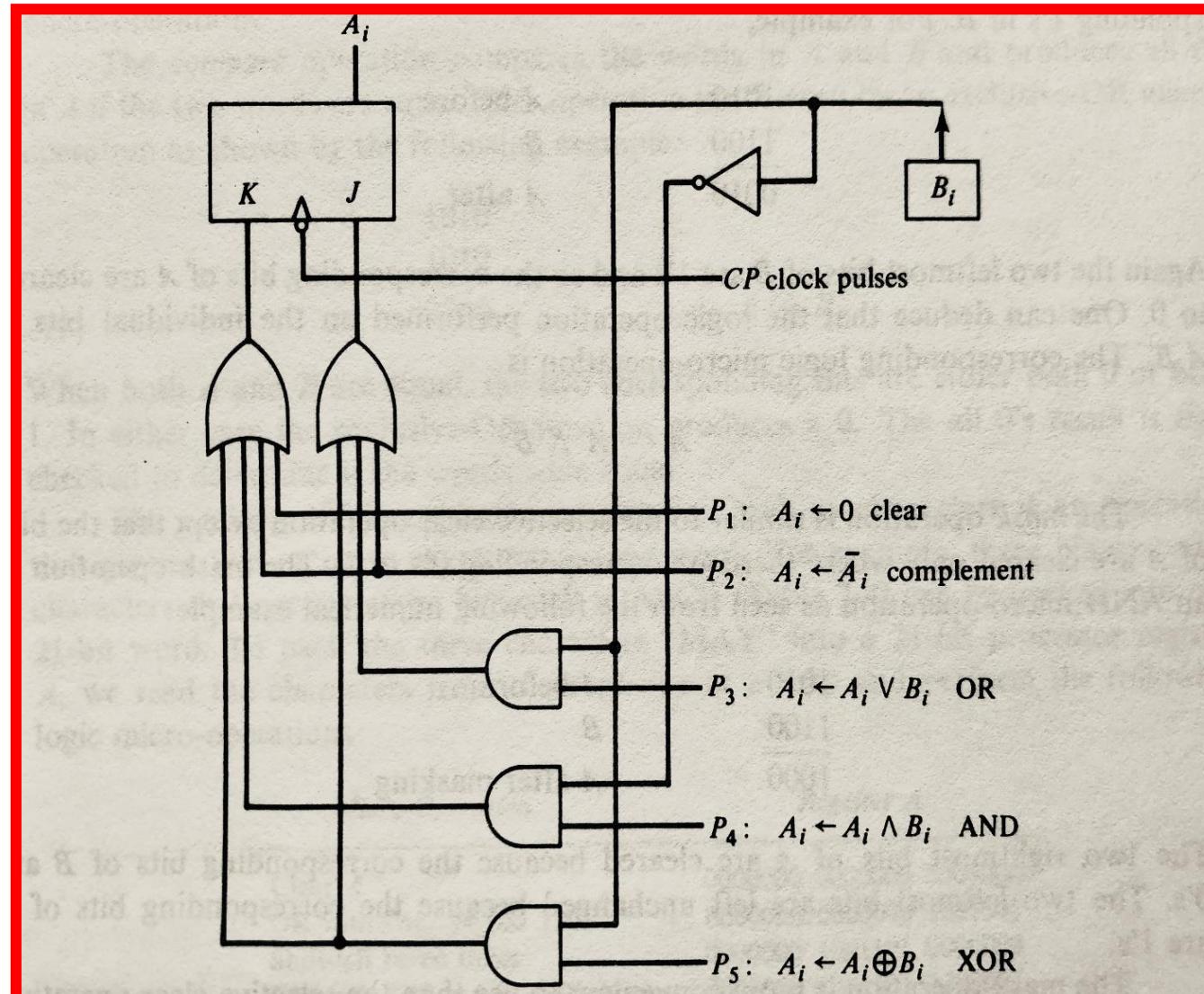
$$P_7 : A \leftarrow A' \wedge B$$

$$P_8 : A \leftarrow (A \vee B)'$$

$$P_9 : A \leftarrow (A \wedge B)'$$

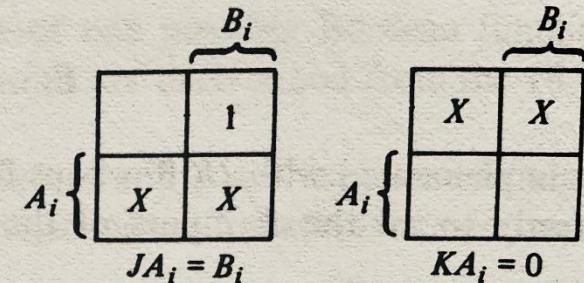
JK Flip-Flop

J	K	$Q(t + 1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$



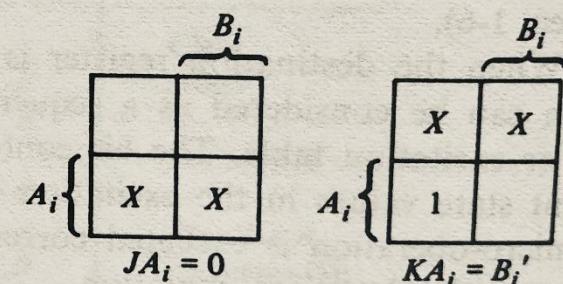
jth stage of
Logic Unit

<i>Present State</i>	<i>Input</i>	<i>Next State</i>	<i>Flip-flop Inputs</i>	
<i>A_i</i>	<i>B_i</i>	<i>A_i</i>	<i>JA_i</i>	<i>KA_i</i>
0	0	0	0	X
0	1	1	1	X
1	0	1	X	0
1	1	1	X	0



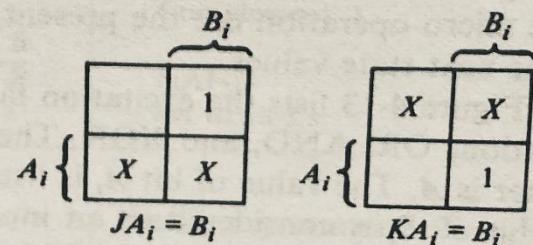
(a) Logic OR

<i>Present State</i>	<i>Input</i>	<i>Next State</i>	<i>Flip-flop Inputs</i>	
<i>A_i</i>	<i>B_i</i>	<i>A_i</i>	<i>JA_i</i>	<i>KA_i</i>
0	0	0	0	X
0	1	0	0	X
1	0	0	X	1
1	1	1	X	0



(b) Logic AND

<i>Present State</i>	<i>Input</i>	<i>Next State</i>	<i>Flip-flop Inputs</i>	
<i>A_i</i>	<i>B_i</i>	<i>A_i</i>	<i>JA_i</i>	<i>KA_i</i>
0	0	0	0	X
0	1	1	1	X
1	0	1	X	0
1	1	0	X	1



(c) Logic exclusive-OR (XOR)

$P_6 : A \vee \bar{B}$

P.S. IMP.		NS	FF inputs	
A_i	B_i	A_i	J_{A_i}	K_{A_i}
0	0	1	1	X
0	1	0	0	X
1	0	1	X	0
1	1	1	X	0

$$A_i \begin{pmatrix} 1 & & \\ & X & X \end{pmatrix} \quad J_{A_i} = B'_L$$

$$\begin{array}{|c|c|} \hline X & X \\ \hline & \\ \hline \end{array} \quad K_{A_i} = 0$$

$P_7 : A \leftarrow \bar{A} \wedge B$

P.S. IMP.		N.S.	FF inputs	
A_i	B_i	A_i	J_{A_i}	K_{A_i}
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	0	X	1

$$J_{A_i} = B_i$$

$$K_{A_i} = 1$$

$P_8 : A \leftarrow \bar{A} \vee B$

P.S. IMP.		N.S.	FF inputs	
A_i	B_i	A_i	J_{A_i}	K_{A_i}
0	0	1	1	X
0	1	0	0	X
1	0	0	X	1
1	1	0	X	1

$$J_{A_i} = B'_L$$

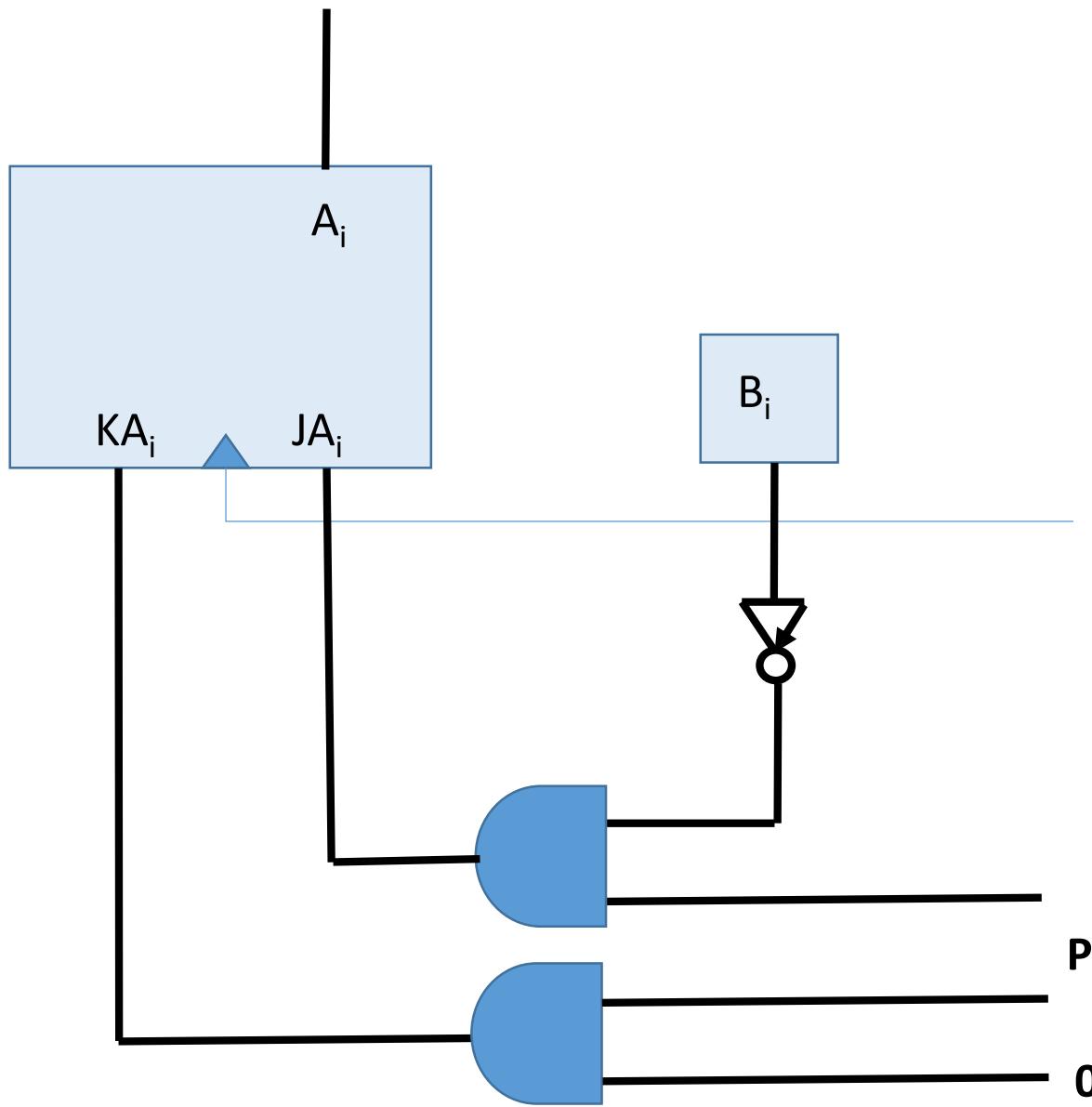
$$K_{A_i} = 1$$

$P_9 : A \leftarrow \bar{A} \wedge \bar{B}$

P.S. IMP.		N.S.	FF inputs	
A_i	B_i	A_i	J_{A_i}	K_{A_i}
0	0	1	1	X
0	1	1	1	X
1	0	1	X	0
1	1	0	X	0

$$J_{A_i} = 1$$

$$K_{A_i} = B_i$$



CP

$P_6 : A \vee B'$

0

Ex 7. List the sequence of logic micro-operations required for packing the six alphanumeric characters HI-LO into 48-bit registers. Use 8 bits per character, obtained from the 7 ASCII (see table below) bits and an even parity bit in the most significant position.

<i>Character</i>	<i>Binary Code</i>	<i>Character</i>	<i>Binary Code</i>
A	100 0001	0	011 0000
B	100 0010	1	011 0001
C	100 0011	2	011 0010
D	100 0100	3	011 0011
E	100 0101	4	011 0100
F	100 0110	5	011 0101
G	100 0111	6	011 0110
H	100 1000	7	011 0111
I	100 1001	8	011 1000
J	100 1010	9	011 1001
K	100 1011		
L	100 1100		
M	100 1101	blank	010 0000
N	100 1110	.	010 1110
O	100 1111	(010 1000
P	101 0000	+	010 1011
Q	101 0001	\$	010 0100
R	101 0010	*	010 1010
S	101 0011)	010 1001
T	101 0100	—	010 1101
U	101 0101	/	010 1111
V	101 0110	,	010 1100
W	101 0111	=	011 1101
X	101 1000		
Y	101 1001		
Z	101 1010		

clear A

OR H = 0100 1000

shift left eight times

OR I = 1100 1001

shift left eight times

OR - = 0010 1101

shift left eight times

OR L = 1100 1100

shift left eight times

OR O = 1100 1111

shift left eight times

OR P = 0010 1110

Ex 8. Show that the statement

$$A \leftarrow A + A$$

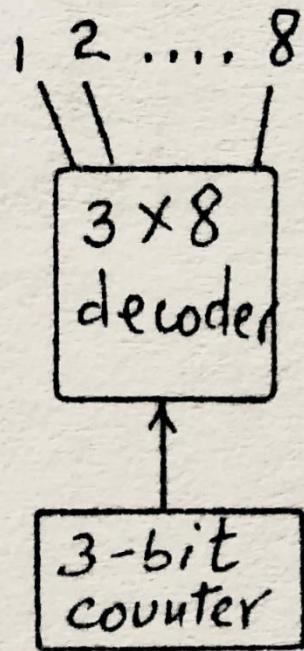
symbolizes a *shift-left* micro-operation.

$A \leftarrow A + A$ adds value of A to itself which is equal to $2A$
which is equivalent to *shift-left* with 0 shifted in lower-order bit.

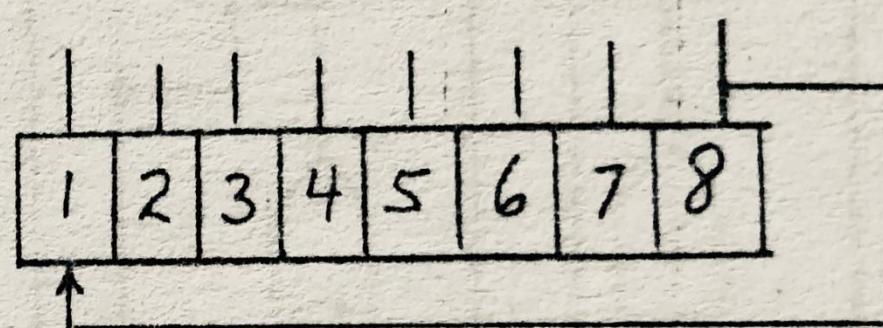
Example:

$A = 01011101 = (93)_{10}$
after shl $A = 10111010 = (186)_{10}$

Ex 9. Show that an n -bit binary counter connected to an n -to- 2^n decoder is equivalent to a ring counter with 2^n flip-flops. Show the block diagram of both circuits for $n=3$. How many timing signals are generated?



decoder outputs	
1	0 0 0 0 0 0 0
0	1 0 0 0 0 0 0
0	0 1 0 0 0 0 0
0	0 0 1 0 0 0 0
	⋮
0	0 0 0 0 0 0 1



ring - counter outputs :
 1 0 0 0 0 0 0 0
 0 1 0 0 0 0 0 0 etc.
 same as decoder outputs

Ex 10. A digital system has three registers: AR, PR, and BR. Three flip-flops provide the control functions for the system: S is a flip-flop which is enabled by an external signal to start the system's operations; F and R are used for sequencing the micro-operations. A fourth flip-flop, D, is set by the digital system when the operation is completed. The function of the system is described by the following register-transfer operations:

$$S: \quad PR \leftarrow 0, S \leftarrow 0, D \leftarrow 0, F \leftarrow 1$$

$$F: \quad F \leftarrow 0, \text{ if } (AR = 0) \text{ then } (D \leftarrow 1), \text{ if } (AR \neq 0) \text{ then } (R \leftarrow 1)$$

$$R: \quad PR \leftarrow PR + BR, AR \leftarrow AR - 1, R \leftarrow 0, F \leftarrow 1$$

- (a) Show that the digital system multiplies the contents of AR and BR and places the product in BR.
- (b) Draw a block diagram of the hardware implementation. Include a *start* input to flip-flop S and a *done* output from flip-flop D.

S: $PR \leftarrow 0, S \leftarrow 0, D \leftarrow 0, F \leftarrow 1$

F: $F \leftarrow 0, \text{ if } (AR = 0) \text{ then } (D \leftarrow 1), \text{ if } (AR \neq 0) \text{ then } (R \leftarrow 1)$

R: $PR \leftarrow PR + BR, AR \leftarrow AR - 1, R \leftarrow 0, B \leftarrow 1$

Initially : $PR = 0$

After $S=1$: $PR = \underbrace{BR + BR + BR + BR + \dots + BR}_{\text{A number of times equal to the value in AR.}}$

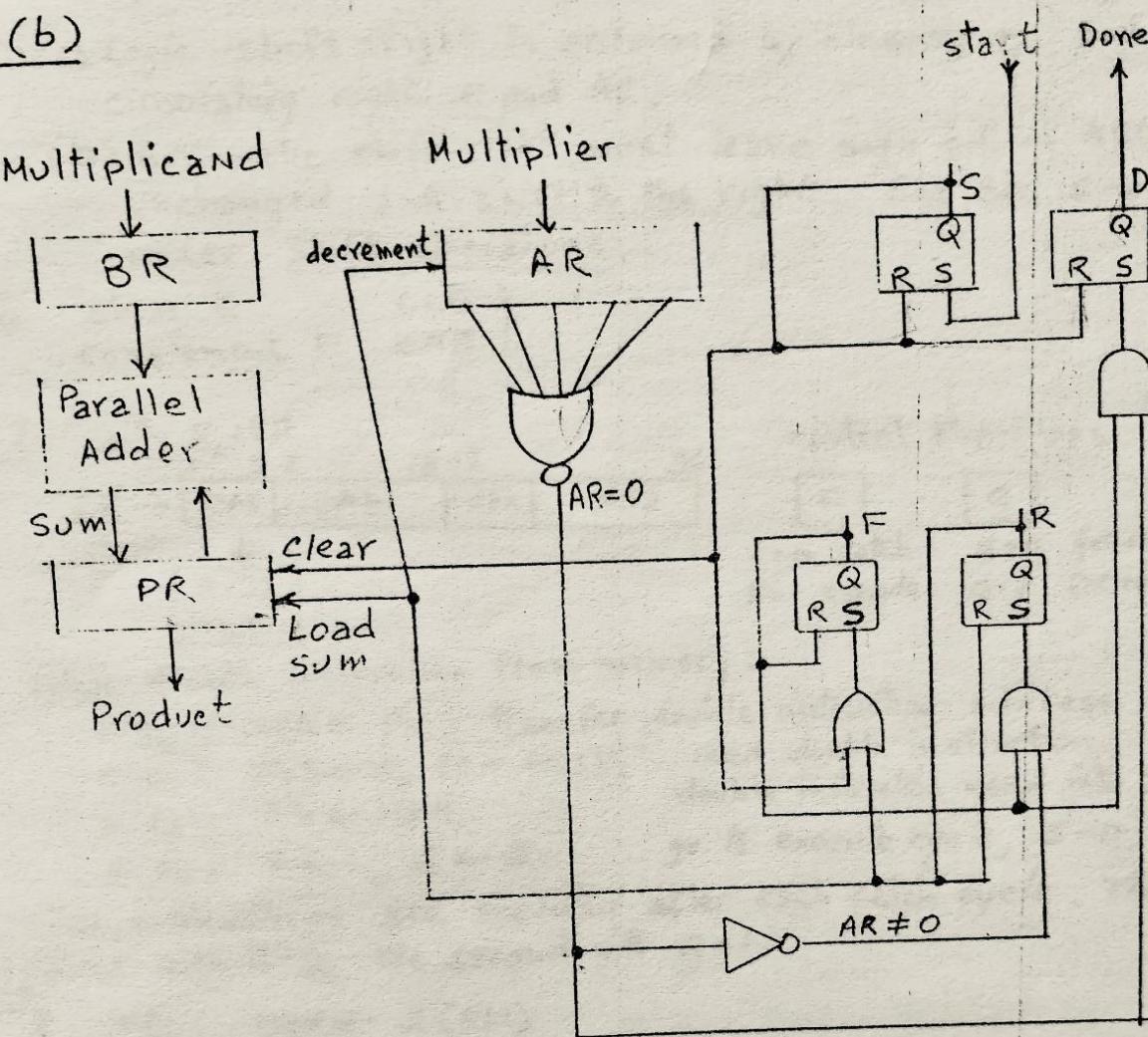
Therefore : $PR = BR * AR$ (multiplication)

S: $PR \leftarrow 0, S \leftarrow 0, D \leftarrow 0, F \leftarrow 1$

F: $F \leftarrow 0$, if $(AR = 0)$ then $(D \leftarrow 1)$, if $(AR \neq 0)$ then $(R \leftarrow 1)$

R: $PR \leftarrow PR + BR, AR \leftarrow AR - 1, R \leftarrow 0, B \leftarrow 1$

S	R	Q	State
0	0	Previous State	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Forbidden



S: $PR \leftarrow 0, S \leftarrow 0, D \leftarrow 0, F \leftarrow 1$

F: $F \leftarrow 0$, if $(AR = 0)$ then $(D \leftarrow 1)$, if $(AR \neq 0)$ then $(R \leftarrow 1)$

R: $PR \leftarrow PR + BR, AR \leftarrow AR - 1, R \leftarrow 0, F \leftarrow 1$