BASIC ELECTRONICS

Laboratory Manual/Practical File

Semester: 3rd
Subject Code: ARI 253

University School of Robotics & Automation

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Delhi Campus
Surajmal Vihar, Delhi

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6		To study half wave, full wave and bridge rectifier with filters.		
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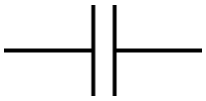
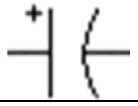
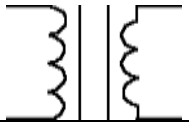
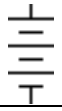
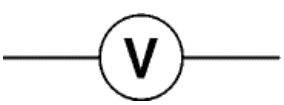
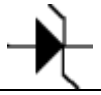
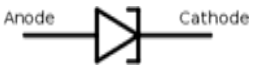
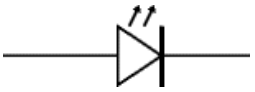
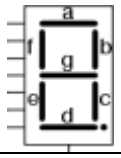
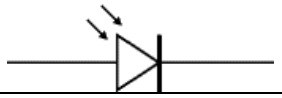
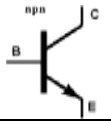
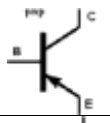
8		Realize Master-Slave J K Flip-Flop using NAND/NOR gates		
9		Realize a Serial and parallel Adder		
10		To study the input and output characteristics of a transistor, JFET and MOSFET in its various configurations.		
11		To study diode based clipping and clamping circuits		

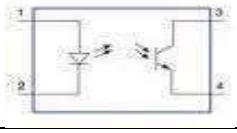
EXPERIMENT NO.: 1 **Date:**

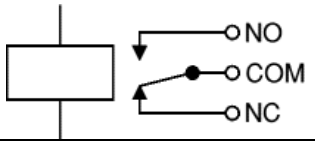
AIM: To Understand & Draw the symbols of various electronic devices.

Write theory (on right hand side) about the devices in 1 or 2 lines and draw symbols (on the left hand side) on blank page.

Sr. No.	Device Name	Symbol
1.	Resistor	
2.	Variable resistor	
3.	Capacitor	
4.	Electrolyte (polarized) Capacitor	
5.	Variable capacitor	
6.	Inductor	
7.	Transformer	
8.	DC power supply	
9.	Ground	
10.	AC supply	
11.	voltmeter	

12.	Current meter	
13.	CRO	
14.	ohm meter	
15.	PN junction diode	
16.	Zener diode	
17.	Tunnel diode	
18.	Light Emitting diode(LED)	
19.	Seven segment display	
20.	Photo diode	
21.	npn transistor	
22.	pnp transistor	
23.	Photo transistor	

24.	Optocoupler	
25.	Thermistor	
26.	LDR(Light Dependent Resistor)	
27.	UJT(Uni Junction Transistor) n-type	
28.	UJT(Uni Junction Transistor) p-type	
29.	SCR(Silicon Controlled Rectifier)	
30.	DIAC	
31.	TRIAC	
32.	n-channel JFET	
33.	p-channel JFET	
34.	n-channel depletion MOSFET	
	p-channel depletion MOSFET	

35.		
36.	n-channel enhance MOSFET	
37.	p-channel enhance MOSFET	
38.	Relay	
39.	DC Supply	
40.	AC Supply	

EXPERIMENT NO.: 2 **Date:**

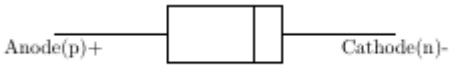
AIM: To study and plot the characteristics of a junction diode**.**

http://vlabs.iitkgp.ernet.in/be/exp5/index.html#

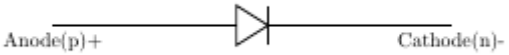
Write theory (on right hand side) and draw symbols, tables and charts (on the left hand side) on blank page.

Theory: Structure of P-N junction diode

The diode is a device formed from a junction of n-type and p-type semiconductor material. The lead connected to the p-type material is called the anode and the lead connected to the n-type material is the cathode. In general, the cathode of a diode is marked by a solid line on the diode.



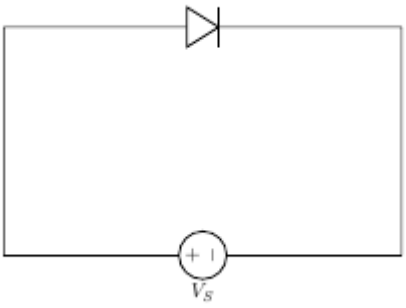
Figurer:1



Figurer:2

Function of a P-N junction diode in Forward Bias

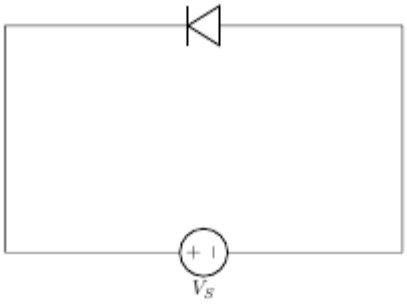
The positive terminal of battery is connected to the P side(anode) and the negative terminal of battery is connected to the N side(cathode) of a diode, the holes in the p-type region and the electrons in the n-type region are pushed toward the junction and start to neutralize the depletion zone, reducing its width. The positive potential applied to the p-type material repels the holes, while the negative potential applied to the n-type material repels the electrons. The change in potential between the p side and the n side decreases or switches sign. With increasing forward-bias voltage, the depletion zone eventually becomes thin enough that the zone's electric field cannot counteract charge carrier motion across the p–n junction, which as a consequence reduces electrical resistance. The electrons that cross the p–n junction into the p-type material (or holes that cross into the n-type material) will diffuse into the nearby neutral region. The amount of minority diffusion in the near-neutral zones determines the amount of current that may flow through the diode.



Figurer:3

Function of a P-N junction diode in Reverse Bias

The positive terminal of battery is connected to the N side(cathode) and the negative terminal of battery is connected to the P side(anode) of a diode. Therefore, very little current will flow until the diode breaks down.

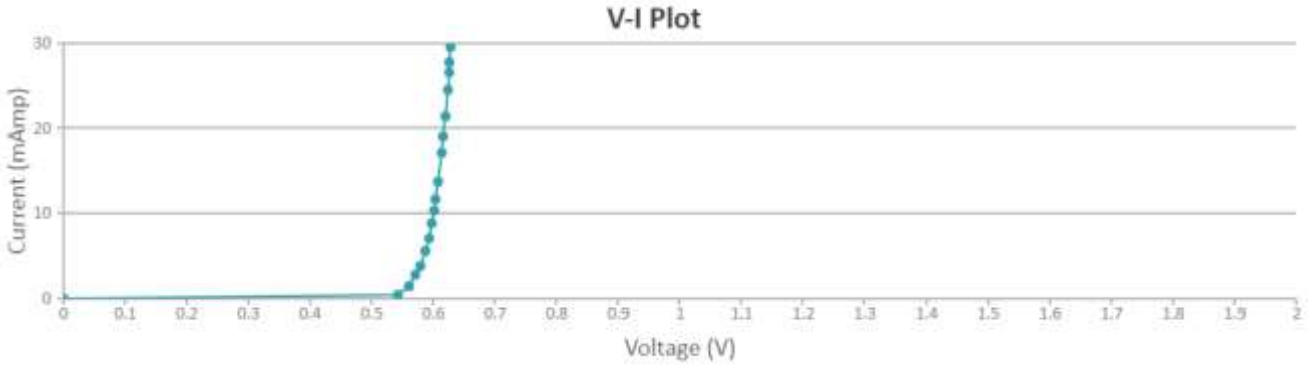


Figurer:4

The positive terminal of battery is connected to the N side(cathode) and the negative terminal of battery is connected to the P side(anode) of a diode, the 'holes' in the p-type material are pulled away from the junction, leaving behind charged ions and causing the width of the depletion region to increase. Likewise, because the n-type region is connected to the positive terminal, the electrons will also be pulled away from the junction, with similar effect. This increases the voltage barrier causing a high resistance to the flow of charge carriers, thus allowing minimal electric current to cross the p–n junction. The increase in resistance of the p–n junction results in the junction behaving as an insulator. The strength of the depletion zone electric field increases as the reverse-bias voltage increases. Once the electric field intensity increases beyond a critical level, the p–n junction depletion zone breaks down and current begins to flow, usually by either the Zener or the avalanche breakdown processes. Both of these breakdown processes are non-destructive and are reversible, as long as the amount of current flowing does not reach levels that cause the semiconductor material to overheat and cause thermal damage.

Forward and reverse biased characteristics of a Silicon diode

In forward biasing, the positive terminal of battery is connected to the P side and the negative terminal of battery is connected to the N side of the diode. Diode will conduct in forward biasing because the forward biasing will decrease the depletion region width and overcome the barrier potential. In order to conduct, the forward biasing voltage should be greater than the barrier potential. During forward biasing the diode acts like a closed switch with a potential drop of nearly 0.6 V across it for a silicon diode. The forward and reverse bias characteristics of a silicon diode. From the graph, it can be noticed that the diode starts conducting when the forward bias voltage exceeds around 0.6 volts (for Si diode). This voltage is called cut-in voltage.

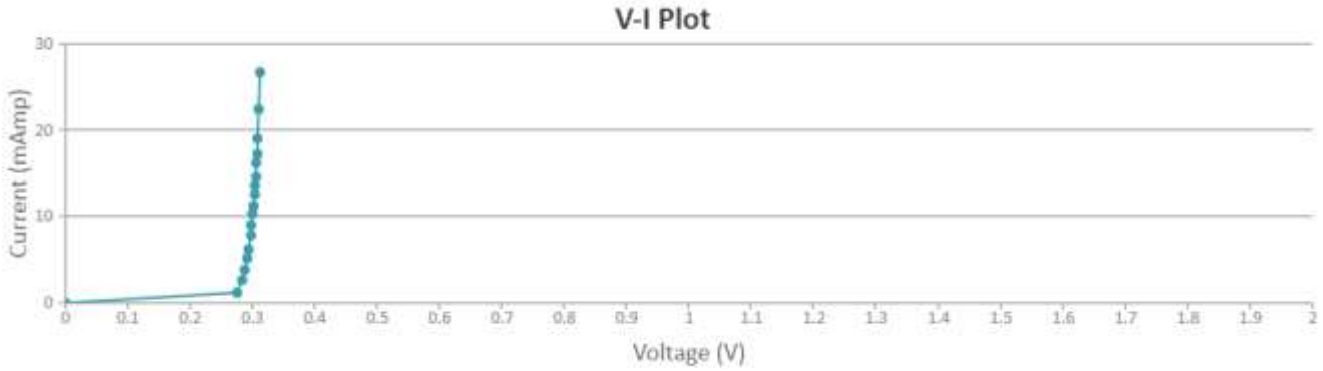


Figurer:5

In reverse biasing, the positive terminal of battery is connected to the N side and the negative terminal of battery is connected to the P side of a diode. In reverse biasing, the diode does not conduct electricity, since reverse biasing leads to an increase in the depletion region width; hence current carrier charges find it more difficult to overcome the barrier potential. The diode will act like an open switch and there is no current flow.

Forward and reverse biased characteristics of a Germanium diode

In forward biasing, the positive terminal of battery is connected to the P side and the negative terminal of battery is connected to the N side of the diode. Diode will conduct in forward biasing because the forward biasing will decrease the depletion region width and overcome the barrier potential. In order to conduct, the forward biasing voltage should be greater than the barrier potential. During forward biasing the diode acts like a closed switch with a potential drop of nearly 0.3 V across it for a germanium diode. The forward and reverse bias characteristics of a germanium diode. From the graph, it can be noticed that the diode starts conducting when the forward bias voltage exceeds around 0.3 volts (for Ge diode). This voltage is called cut-in voltage.



Figurer:6

In reverse biasing, the positive terminal of battery is connected to the N side and the negative terminal of battery is connected to the P side of a diode. In reverse biasing, the diode does not conduct electricity, since reverse biasing leads to an increase in the depletion region width; hence current carrier charges find it more difficult to overcome the barrier potential. The diode will act like an open switch and there is no current flow.

Diode Equation

In the forward-biased and reversed-biased regions, the current (I_f), and the voltage (V_f), of a semiconductor diode are related by the diode equation:

$$I_f = I_s \times (e^{\frac{V_f}{n*V_T}} - 1)$$

where,

I_s is reverse saturation current or leakage current,

I_f is current through the diode (forward current),

V_f is potential difference across the diode terminals (forward voltage)

V_T is thermal voltage, given by

$$V_T = \frac{k*T}{q}$$

and
k is Boltzmann's constant = 1.38×10^{-23} J /°Kelvin,
q is the electronic charge = 1.6×10^{-19} joules/volt(Coulombs),
T is the absolute temperature in °Kelvin (°K = 273 + temperature in °C),
At room temperature (25 °C), the thermal voltage is about 25.7 mV,
n is an empirical constant between 0.5 and 2

The empirical constant, n, is a number that can vary according to the voltage and current levels. It depends on electron drift, diffusion, and carrier recombination in the depletion region. Among the quantities affecting the value of n are the diode manufacture, levels of doping and purity of materials.

If n=1, the value of $\frac{k*T}{q}$ is 26 mV at 25°C.
When n=2, the value of $\frac{k*T}{q}$ becomes 52 mV.
For germanium diodes, n is usually considered to be close to 1.
For silicon diodes, n is in the range of 1.3 to 1.6.

Results
Draw observation table, plot graphs

Conclusion

EXPERIMENT NO.: 3 **Date:**

AIM: Verification and interpretation of truth table for AND, OR, NOT, NAND, NOR, Ex-OR, Ex-NOR gates and Realization of all gates using NAND & NOR gates

https://de-iitr.vlabs.ac.in/exp/truth-table-gates/

https://de-iitr.vlabs.ac.in/exp/realization-of-logic-functions/

Write theory (on right hand side) and draw symbols, tables and charts (on the left hand side) on blank page.

Logic gates are the basic building blocks of any digital system. Logic gates are electronic circuits having one or more than one input and only one output. The relationship between the input and the output is based on certain logic. Based on this, logic gates are named as

1. AND gate
2. OR gate
3. NOT gate
4. NAND gate
5. NOR gate
6. Ex-OR gate
7. Ex-NOR gate

1) AND gate

The AND gate is an electronic circuit that gives a high output (1) only if all its inputs are high. A dot (.) is used to show the AND operation i.e. A.B or can be written as AB.

Y= A.B

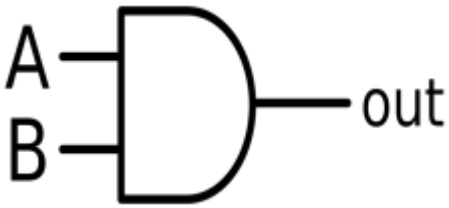


Figure-1:Logic Symbol of AND Gate

Input		Output
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

Figure-2:Truth Table of AND Gate

2) OR gate

The OR gate is an electronic circuit that gives a high output (1) if one or more of its inputs are high. A plus (+) is used to show the OR operation.

Y= A+B

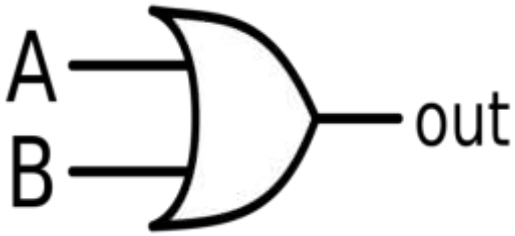


Figure-3:Logic Symbol of OR gate

Input		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

Figure-4:Truth Table of OR Gate

3) NOT gate

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an inverter. If the input variable is A, the inverted output is known as NOT A. This is also shown as A' or A with a bar over the top, as shown at the outputs.

Y= A'

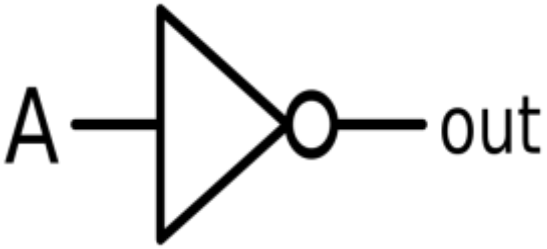


Figure-5:Logic Symbol of NOT Gate of NOT Gate

Input	Output
A	Y
0	1
1	0

Figure-6:Truth Table

4) NAND gate

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if any of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

Y= (AB)'

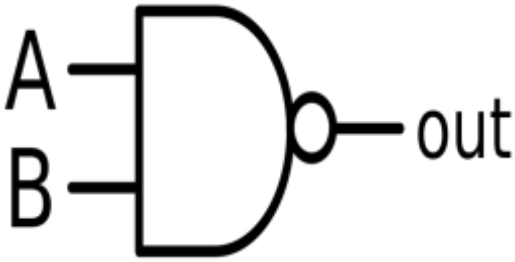


Figure-7:Logic Symbol of NAND Gate

Input	Input	Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Figure-8:Truth Table of NAND Gate

5) NOR gate

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if any of the inputs are high. The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

Y= (A+B)'

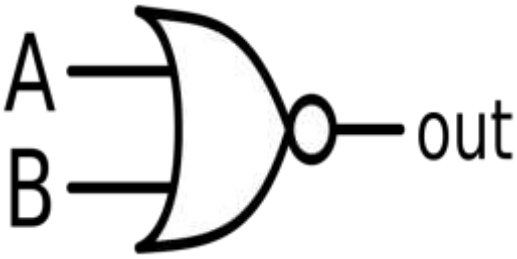


Figure-9:Logic Symbol of NOR Gate

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Figure-10:Truth Table of NOR gate

6) Ex-OR gate

The 'Exclusive-OR' gate is a circuit which will give a high output if either, but not both of its two inputs are high. An encircled plus sign (⊕) is used to show the Ex-OR operation. Ex-OR gate is created from AND, NAND and OR gates. The output is high only when both the inputs are different.

Y= A⊕B = (A'B + AB')

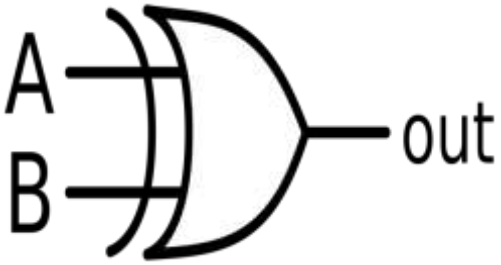


Figure-11:Logic Symbol of Ex-OR gate

A	B	A **XOR** B
0	0	0
0	1	1
1	0	1
1	1	0

Figure-12:Truth Table of Ex-OR gate

7) Ex-NOR gate

The 'Exclusive-NOR' gate circuit does the opposite to the EX-OR gate. It will give a low output if either, but not both of its two inputs are high. The symbol is an EX-OR gate with a small circle on the output. The small circle represents inversion. Ex-NOR gate is created from AND, NOT and OR gates.The output is high only when both the inputs are same

Y= A⊕B = AB+A'B'

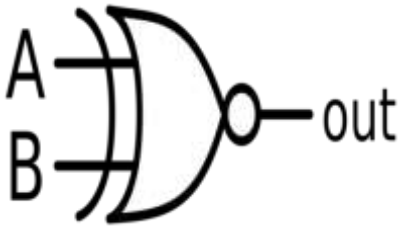


Figure-13:Logic Symbol of Ex-NOR gate

XNOR Truth Table		
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

Figure-14:Truth Table of Ex-NOR gate

Logic gates are electronic circuits which perform logical functions on one or more inputs to produce one output. There are seven logic gates. When all the input combinations of a logic gate are written in a series and their corresponding outputs written along them, then this input/ output combination is called Truth Table.

1)Nand gate as Universal gate

NAND gate is actually a combination of two logic gates i.e. AND gate followed by NOT gate. So its output is complement of the output of an AND gate.This gate can have minimum two inputs. By using only NAND gates, we can realize all logic functions: AND, OR, NOT, Ex-OR, Ex-NOR, NOR. So this gate is also called as universal gate.

1.1)NAND gates as OR gate

From DeMorgan's theorems:

$$(A.B)' = A' + B'$$

$$(A'.B')' = A'' + B'' = A + B$$

So, give the inverted inputs to a NAND gate, obtain OR operation at output.

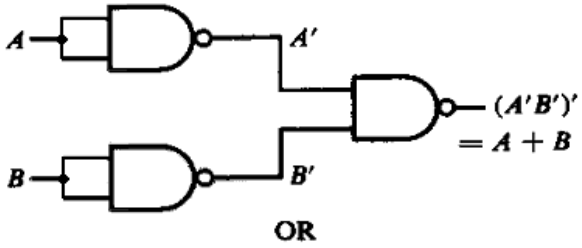


Figure-15:NAND gates as OR gate

1.2)NAND gates as AND gate

A NAND produces complement of AND gate. So, if the output of a NAND gate is inverted, overall output will be that of an AND gate.

Y = ((A.B)')'

Y = (A.B)

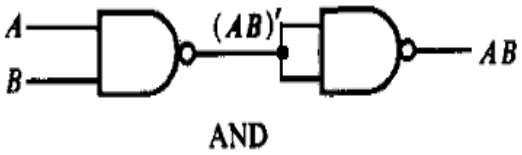


Figure-16:NAND gates as AND gate

1.3)NAND gates as Ex-OR gate

The output of a two input Ex-OR gate is shown by: Y = A'B + AB'. This can be achieved with the logic diagram shown in the left side.

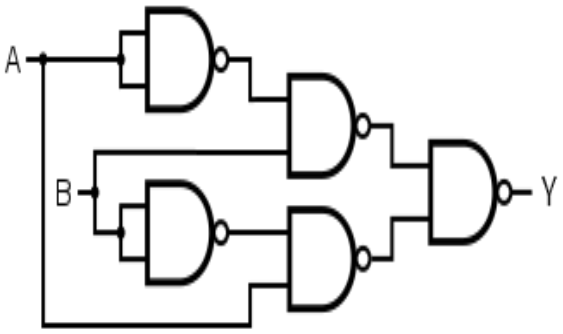


Figure-17:NAND gate as Ex-OR gate

1.4)NAND gates as Ex-NOR gate

Ex-NOR gate is actually Ex-OR gate followed by NOT gate. So give the output of Ex-OR gate to a NOT gate, overall output is that of an Ex-NOR gate.

Y = AB+ A'B'

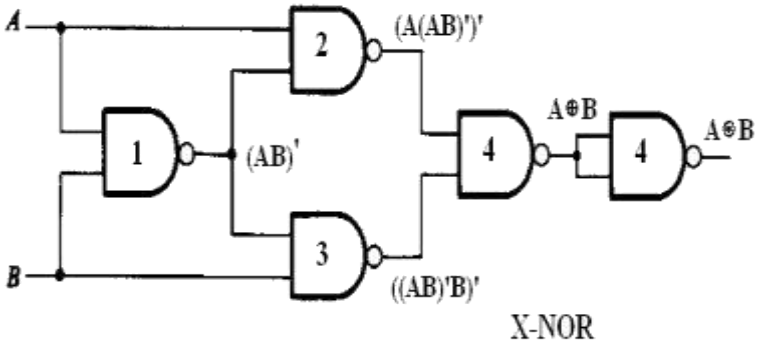


Figure-18:NAND gates as Ex-NOR gate

2)Nor gate as Universal Gate

NOR gate is actually a combination of two logic gates: OR gate followed by NOT gate. So its output is complement of the output of an OR gate.This gate can have minimum two inputs, output is always one. By using only NOR gates, we can realize all logic functions: AND, OR, NOT, Ex-OR, Ex-NOR, NAND. So this gate is also called universal gate.

2.1)NOR gates as OR gate

A NOR produces complement of OR gate. So, if the output of a NOR gate is inverted, overall output will be that of an OR gate.

Y = ((A+B)')'

Y = (A+B)

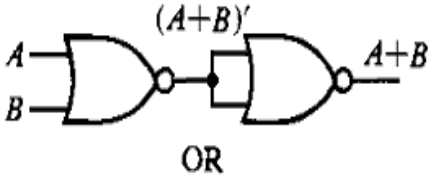


Figure-19:NOR gates as OR gate

2.2)NOR gates as AND gate

From DeMorgan's theorems:
(A+B)' = A'B'
(A'+B')' = A''B'' = AB

So, give the inverted inputs to a NOR gate, obtain AND operation at output.

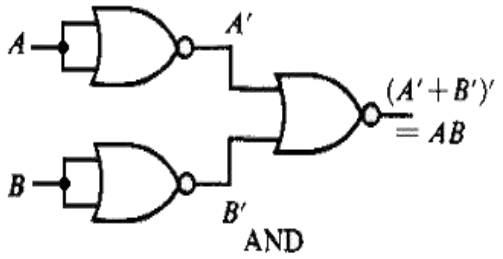


Figure-20:NOR gates as AND gate

2.3)NOR gates as Ex-OR gate

Ex-OR gate is actually Ex-NOR gate followed by NOT gate. So give the output of Ex-NOR gate to a NOT gate, overall output is that of an Ex-OR gate.

Y = A'B+ AB'

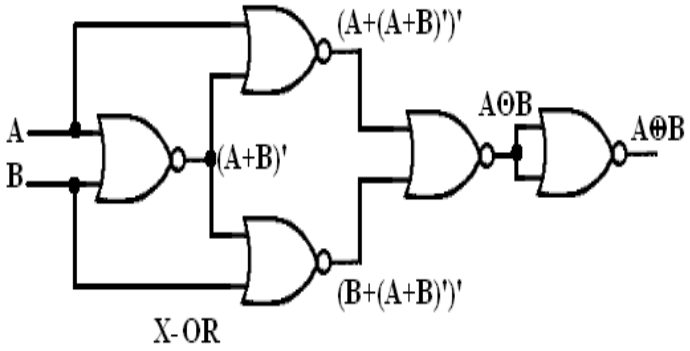


Figure-14:NOR gates as Ex-OR gate

2.4)NOR gates as Ex-NOR gate

The output of a two input Ex-NOR gate is shown by: Y = AB + A'B'. This can be achieved with the logic diagram shown in the left side.

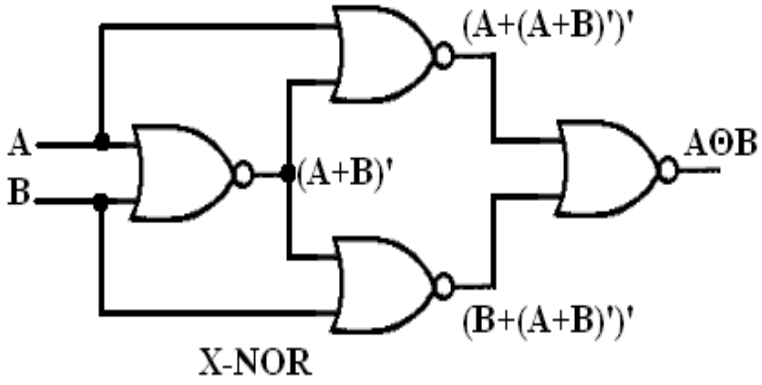


Figure-16:NOR gates as Ex-NOR gate

Results

Draw observation table, plot graphs

EXPERIMENT NO.: 4 **Date:**

AIM: Realize Half Adder, Full Adder, Half Subtractor and Full Subtractor

https://de-iitr.vlabs.ac.in/exp/half-full-adder/

https://de-iitr.vlabs.ac.in/exp/half-full-adder/simulation.html

Write theory (on right hand side) and draw symbols, tables and charts (on the left hand side) on blank page.

Introduction of Adders

Adders are digital circuits that carry out addition of numbers. Adders are a key component of arithmetic logic unit. Adders can be constructed for most of the numerical representations like Binary Coded Decimal (BCD), Excess – 3, Gray code, Binary etc. out of these, binary addition is the most frequently performed task by most common adders. Apart from addition, adders are also used in certain digital applications like table index calculation, address decoding etc.

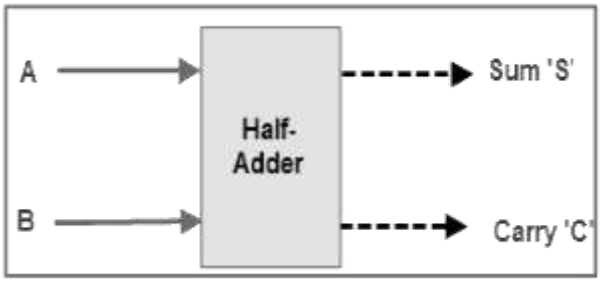
Binary addition is similar to that of decimal addition. Some basic binary additions are shown below.

0	0	1	1
+0	+1	+0	+1
0	1	1	(carry) 1 0

Figure 1. Schematic representation of half adder

1)Half Adder

Half adder is a combinational circuit that performs simple addition of two binary numbers. If we assume A and B as the two bits whose addition is to be performed,the block diagram and a truth table for half adder with A, B as inputs and Sum, Carry as outputs can be tabulated as follows.

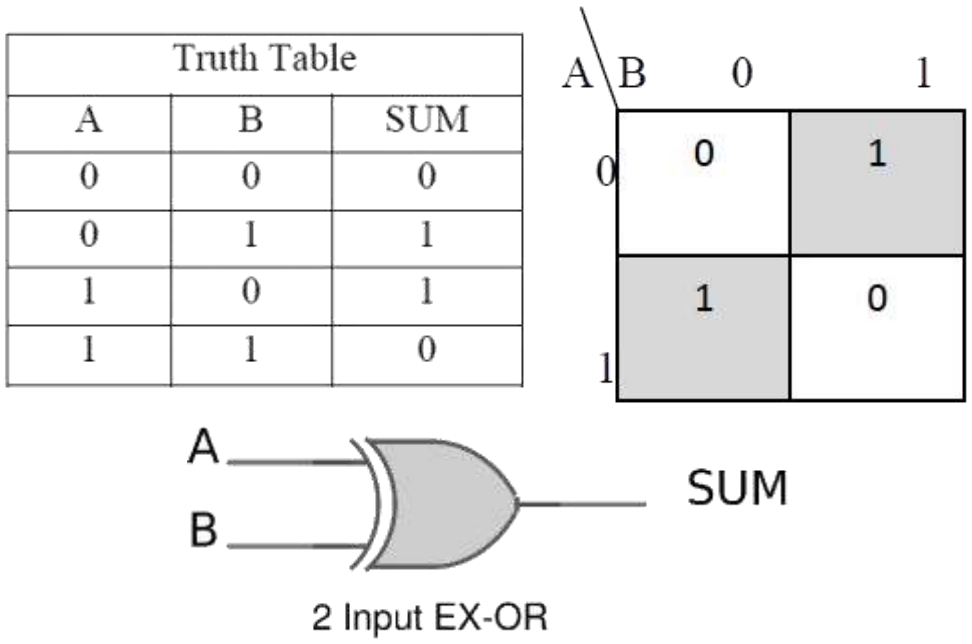


Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 2. Block diagram and truth table of half adder

The sum output of the binary addition carried out above is similar to that of an Ex-OR operation while the carry output is similar to that of an AND operation. The same can be verified with help of Karnaugh Map.

The truth table and K Map simplification and logic diagram for sum output is shown below.

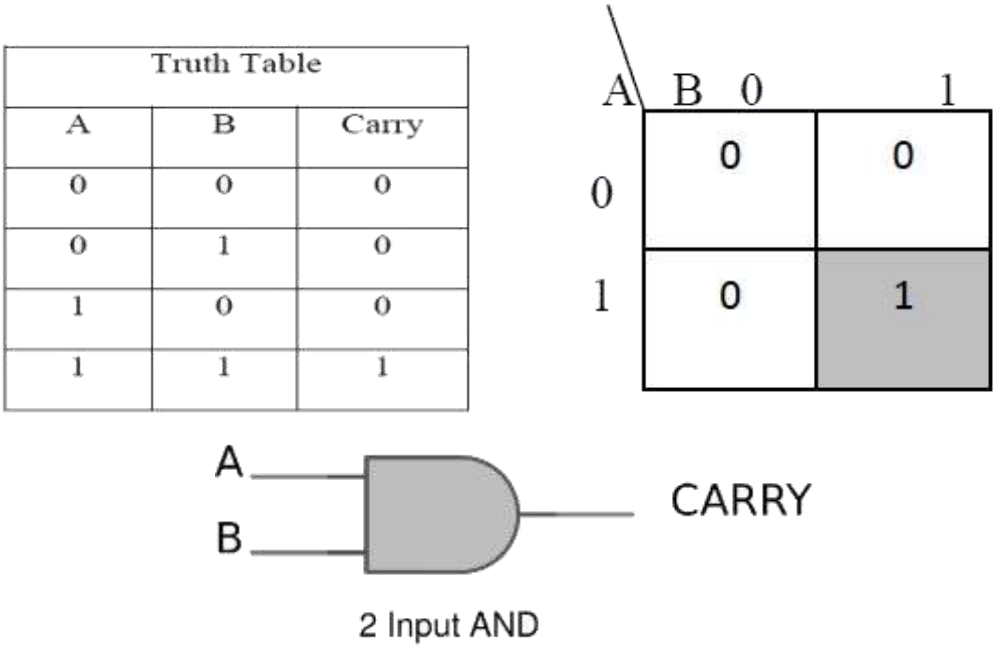


Truth Table		
A	B	SUM
0	0	0
0	1	1
1	0	1
1	1	0

Figure 3. Truth table, K Map simplification and Logic diagram for sum output of half adder

Sum = A B' + A' B

The truth table and K Map simplification and logic diagram for carry is shown below.



Truth Table		
A	B	Carry
0	0	0
0	1	0
1	0	0
1	1	1

Figure 4. Truth table, K Map simplification and Logic diagram for sum output of half adder

Carry = AB

If A and B are binary inputs to half adder, then the logic function to calculate sum S is Ex – OR of A and B and logic function to calculate carry C is AND of A and B. Combining these two, the logical circuit to implement the combinational circuit of half adder is shown below.

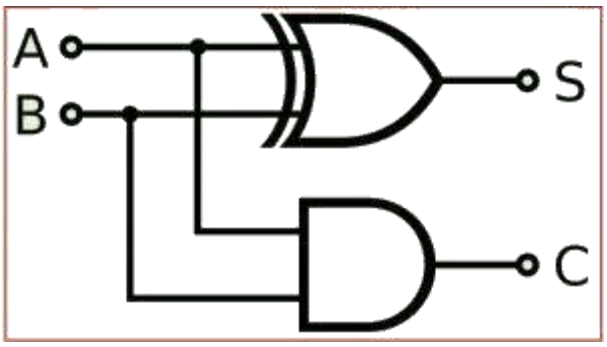


Figure 5. Half Adder Logic Diagram

K-Map for SUM:

A \ B	00	01
00		1
01	1	

SUM = A'B + AB'

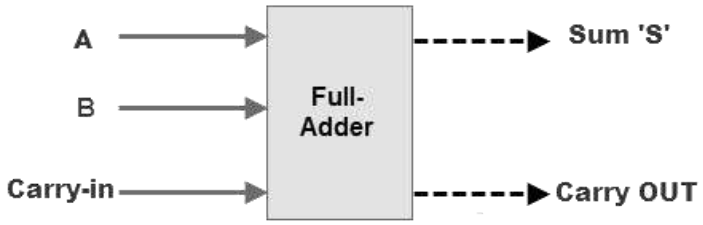
K-Map for CARRY:

A \ B	00	01
00		
01		1

CARRY = AB

2)Full Adder

Full adder is a digital circuit used to calculate the sum of three binary bits. Full adders are complex and difficult to implement when compared to half adders. Two of the three bits are same as before which are A, the augend bit and B, the addend bit. The additional third bit is carry bit from the previous stage and is called 'Carry' – in generally represented by CIN. It calculates the sum of three bits along with the carry. The output carry is called Carry – out and is represented by Carry OUT. The block diagram of a full adder with A, B and CIN as inputs and S, Carry OUT as outputs is shown below.



Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 8. Full Adder Truth Table

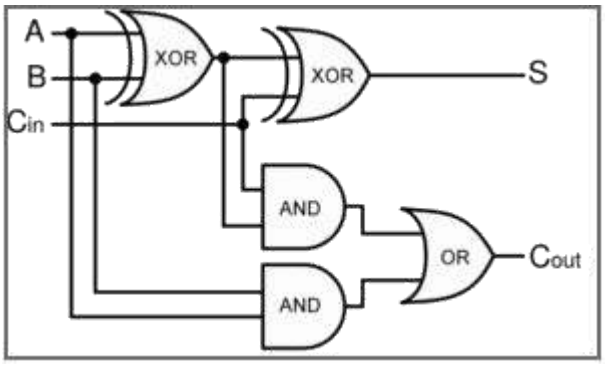


Figure 9. Full Adder Logic Diagram

Based on the truth table, the Boolean functions for Sum (S) and Carry – out (COUT) can be derived using K – Map.

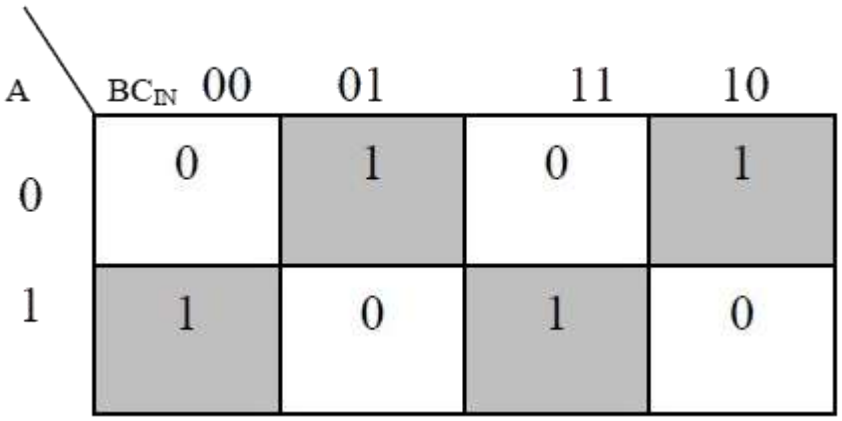


Figure 10. The K-Map simplified equation for sum is S = A'B'Cin + A'BCin' + ABCin

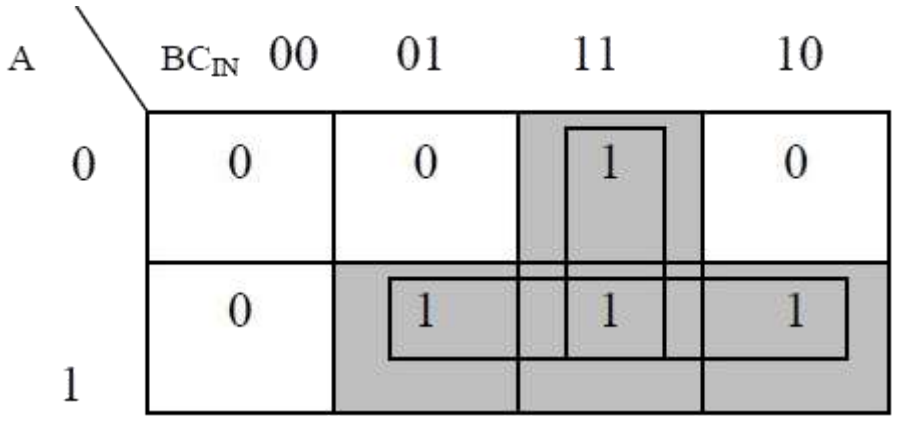


Figure 11. The K-Map simplified equation for COUT is COUT = AB + ACIN + BCIN

In order to implement a combinational circuit for full adder, it is clear from the equations derived above, that we need four 3-input AND gates and one 4-input OR gates for Sum and three 2-input AND gates and one 3-input OR gate for Carry – out.

Introduction to Subtractors

Subtractor circuits take two binary numbers as input and subtract one binary number input from the other binary number input. Similar to adders, it gives out two outputs, difference and borrow (carry-in the case of Adder). There are two types of subtractors.

1. Half Subtractor
2. Full Subtractor

1) Half Subtractor

The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, A (minuend) and B (subtrahend) and two outputs Difference and Borrow. The logic symbol and truth table are shown below.

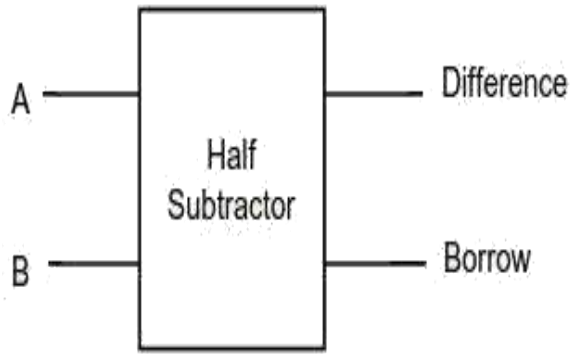


Figure-1: Logic Symbol of Half subtractor

Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Figure-2:Truth Table of Half subtractor

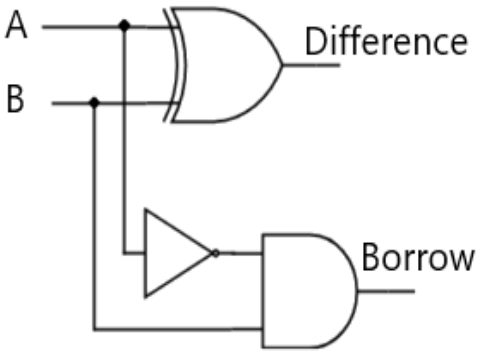


Figure-3:Circuit Diagram of Half subtractor

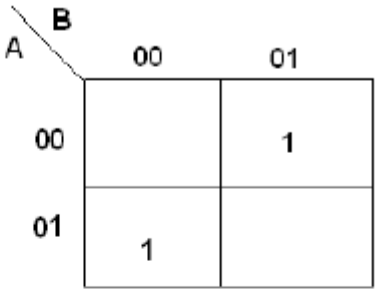
From the above truth table we can find the boolean expression.

Difference = A ⊕ B

Borrow = A' B

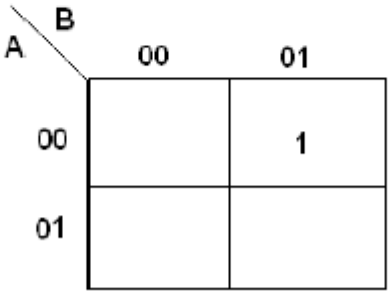
From the equation we can draw the half-subtractor circuit as shown in the figure 3.

K-Map for DIFFERENCE:



DIFFERENCE = A'B + AB'

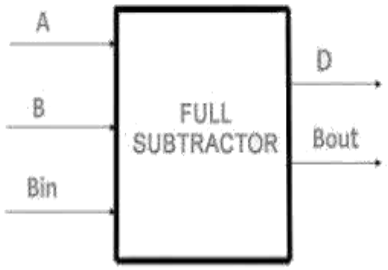
K-Map for BORROW:



BORROW = A'B

2) Full Subtractor

A full subtractor is a combinational circuit that performs subtraction involving three bits, namely A (minuend), B (subtrahend), and Bin (borrow-in) . It accepts three inputs: A (minuend), B (subtrahend) and a Bin (borrow bit) and it produces two outputs: D (difference) and Bout (borrow out). The logic symbol and truth table are shown below.

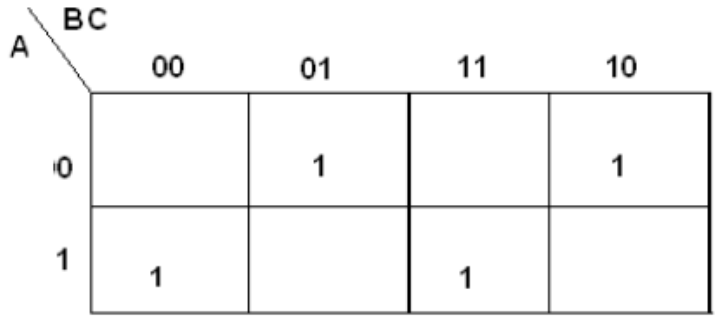


A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Figure-4:Logic Symbol of Full Subtractor **Figure-5:Truth Table of Full subtractor**

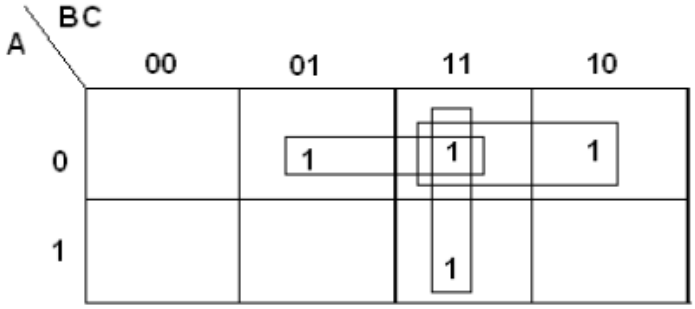
From the above truth table we can find the boolean expression.

K-Map for Difference:



Difference = A'B'C + A'BC' + AB'C' + ABC

K-Map for Borrow:



Borrow = A'B + BC + A'C

D = A ⊕ B ⊕ Bin

Bout = A' Bin + A' B + B Bin

From the equation we can draw the Full-subtractor circuit as shown in the figure 6.

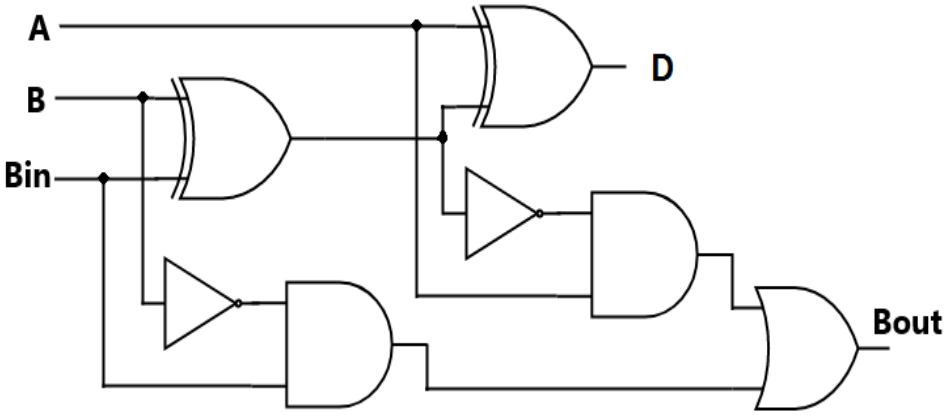


Figure-6:Circuit Diagram of Full subtractor

Results