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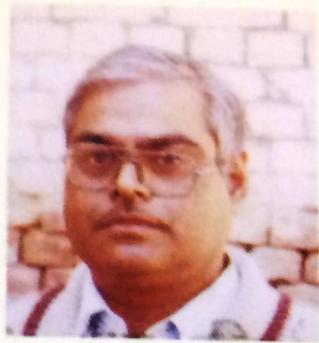
# **ANALOG ELECTRONICS**

**(CIRCUITS and DEVICES)**



**Dr. D.K. Kaushik**

**DHANPAT RAI PUBLISHING COMPANY**



Dr. D.K. Kaushik presently working as the Head department of Electronics and Computer Science, Dayanand Post-Graduate college, Hisar, Haryana. He obtained his masters degree from Meerut University and Ph.D. in 1981 from Kurukshetra University, Kurukshetra. He has 22 years teaching experience in the subject of Electronics and published more 20 research papers

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# **ANALOG ELECTRONICS**

## **(CIRCUITS AND DEVICES)**

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## PREFACE

The book *Analog Electronics (Circuits and Devices)* contains eleven chapters with comprehensive material, discussed in a very systematic, elaborative and lucid manner. The author of this book has made sincere efforts in bringing the book very up to date. It has thoroughly been edited by Prof. P. J. George, Senior Most Professor and chairman Electronic Science Department, Kurukshetra University, Kurukshetra.

It will prove to be good text book for polytechnic and B.E./B.Tech. students of all the engineering colleges in India. It will also cater to the needs of the students of B.Sc. (Electronics), U.G.C. sponsored restructured course. The book also covers the syllabi of B.Sc. (IT), M.Sc.(Physics specialization in Electronics), M.Tech (electronics).

The objective of this book is to enable students to understand basic circuits and devices. The discussion on the subject in adequate and after going through the book the students will not only have the fundamental knowledge but will have the overall knowledge.

First three chapters of this book contain the circuit theory and deal the network analysis with d.c. and time varying sources and two port network. Different network theorems, different parameters of Two Port Network and their interconnections, different types of passive filters with their frequency and phase response curves have thoroughly and lucidly been discussed with typical solved problems.

Next two chapters i.e. chapters 4 & 5 deal the physics of semiconductor, different types of semiconductor diodes including Zener diodes, photo diodes and light emitting diodes. The application of diodes such as different types of rectifiers, filters, voltage multipliers, and clipping, clamping and log antilog circuits have also been discussed. Complete theoretical aspects have been considered in these chapters.

Chapters 6 – 8 contain the theory of transistors. These chapters cover physical behaviour of junction transistors their characteristics, base width modulation, models of the transistors along with transistor biasing and thermal stabilization with exhaustive analytical explanation.

Ninth chapter deals the basic theory of Junction Field Effect Transistors and MOS Field Effect Transistors with its model and biasing circuits. Latest theory and analytical treatment have been discussed.

Chapter 10 deals the multistage amplifiers; different types of amplifiers including push pull and power amplifiers.

Theory, construction and working of electronic instruments such as cathode ray oscilloscope, multimeters, digital voltmeters, digital frequency meters etc, have been discussed in the last chapter of the book.

The book has been systematically organized and present form help the students to understand and to have the overall knowledge in the field without having prior background of electronics.

### **SALIENT FEATURES:**

The following are the salient features of the proposed text book:

- The material contained in the book is as per class room lectures. The material is neither too large nor too short.
- Written in the simple language but strong pedagogical approach.
- A large number of simple as well complicated numerical solved problems have been introduced. Some unsolved problems with their answers have also been introduced at the end of each chapter.
- The contents are symmetrically arranged.
- The emphasis has been made on the concept using the proper mathematical derivations wherever necessary.
- It will prove to be good text book for all those who study Electronics. It will help the students preparing for NET/SET competitive examination for Physics and Electronics.

Hisar

D.K.Kaushik

## Acknowledgements

The first edition of the book “Analog Electronics (Circuits and Devices)” is the result of the efforts of many of my colleagues, who helped in many ways in bringing the book in the present form. In particular, thanks are due to Lecturers in Electronics Sh. Rajesh Kad, Dayanand College, Hisar., Sh. O. P. Garg, R. K. S. D. College, Kaithal, Sh. Parveen Mathur and Dr. R. S. Rana, S. D. College, Ambala cantt., Sh. Rakesh Jain and Sh. S. K. Gupta, S. A. Jain College, Ambala City, Sh. Gulshan Sethi and Dr. Anil Pundir, M. L. N. College, Yamuna Nagar, Dr. Dushyant Gupta and Sh. Hitender Tyagi, University College, Kurukshetra, Dr. Ashok Thakur, D. A. V. College, Ambala City, Dr. S. P. Garg and Sh. Attar Singh, C. R. M. Jat College, Hisar, Sh. Dalip Singh and Sh. Bhushan Monga, Govt. College, Sirsa, Sh. Rakesh Singla , S. D. College, Panipat.

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Any constructive comments, suggestions and criticism from the readers will be highly appreciated.

HISAR

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# 1

## Network Analysis with d. c. Sources

The components used in electronic circuits may be classified into two categories namely active and passive components. Active components are those which can perform signal processing functions such as signal generation, rectification and amplification. These components basically are semiconductor diodes, transistors and SCR's etc. Batteries and generators which supply energy, also fall in the category of active components. The passive components are those which can not by themselves perform the above mentioned functions. The basic passive components are resistors, inductors and capacitors. In this chapter the analysis of electric circuits or networks, consisting of d.c. sources as the source of energy and other elements like resistors will be discussed using different methods. In addition different theorems will also be discussed to analyze complicated networks.

Before discussing the methods of analysis of network, it is necessary to give the model of the battery or the generator which supply energy to the network.

**1.1 Model for a Battery:** To discuss the model for the battery, consider a

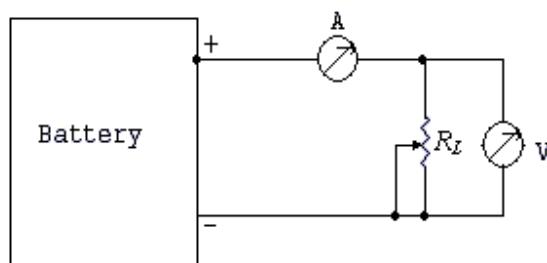


Fig. 1.1

variable load resistance  $R_L$  connected to the output terminals of the battery as shown in figure 1.1. Voltage across the load resistance is measured with the help of a voltmeter  $V$ . The current flowing through the load resistance  $R_L$  is measured with the help of an ammeter connected in series with it. By varying the load resistance, the current  $I$  flowing through and the voltage across the load resistance  $R_L$  is measured. A graph is plotted

between the current  $I$  and voltage  $V$  as shown in figure (1.2). This is a straight line which cuts at  $V_0$  to the  $Y$ -axis and at  $I_0$  to the  $X$ -axis.

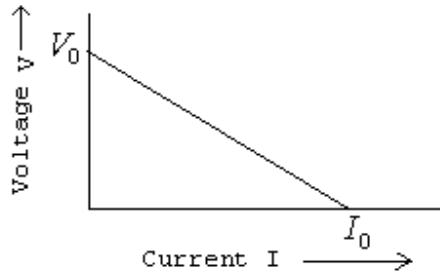


Fig. 1.2

The equation for the straight line is of the form  $y = mx + C$ ,

where  $m = -\frac{V_0}{I_0}$ , is the slope of the curve

and  $C = V_0$ , is the intersect to the  $Y$ -axis.

Thus  $V = -\frac{V_0}{I_0}I + V_0$ ;  $\frac{V_0}{I_0}$  has the dimension of resistance represented by  $R_0$ .

This equation will be  $V = V_0 - R_0 I$  ----- (1.1)

The equivalent circuit of the equation (1.1) is given in figure (1.3).

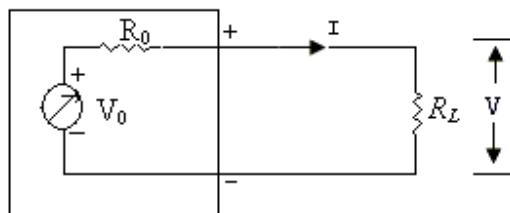


Fig. 1.3

From this circuit, it is clear that the practical battery may be represented by a voltage source  $V_0$  and a resistance  $R_0$  in series with it. The resistance  $R_0$  is known as internal resistance, output resistance or source resistance of the battery.

Now put  $I = 0$ , i.e., the load resistance is removed from the circuit, then  $V = V_0$  and  $V_0$  is called as the open circuit voltage of the source. It is in fact the terminal voltage when no current is drawn from the source. The open circuit voltage when measured with a voltmeter will draw certain amount of current from the source. Thus open circuit voltage should be measured with an ideal voltmeter. Similarly, one more conceptual quantity called the short circuit current may be defined as the current flowing from the battery, when the external terminals of the battery are short circuited. The short circuit

current  $I_0$  will be equal to  $\frac{V_0}{R_0}$ , since  $V = 0$ . This current can only be measured with an ideal current meter. The ratio of open circuit voltage  $V_0$  to the short circuit current  $I_0$  is known as internal resistance of the battery.

From the model of the battery the following inferences can be drawn:

- (i) If a load resistance  $R_L$  is connected to a battery (fig. 1.4), then

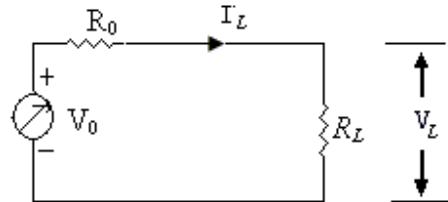


Fig 1.4

the load current  $I_L$  is given by:

$$I_L = \frac{V_0}{(R_0 + R_L)} \quad \text{----- (1.2)}$$

The output voltage  $V_L$  is given by:

$$V_L = I_L R_L = \frac{V_0 R_L}{(R_0 + R_L)} = \frac{V_0}{\left(1 + \frac{R_0}{R_L}\right)} \quad \text{----- (1.3)}$$

From this equation it clear that if  $\frac{R_0}{R_L} \rightarrow 0$  or  $R_0 \ll R_L$ , then  $V_L = V_0$ ; the source will behave like an ideal voltage source. That is the source will said to be a good source if the internal resistance of the source is small enough than the load resistance. The ideal voltage source may be defined as follows:

**Ideal voltage source:** An ideal voltage source is that source which provides a constant potential difference between its terminals, irrespective of the current drawn from it. An ideal voltage source is represented in figure 1.5(a) and it's V – I relationship in figure 1.5(b).

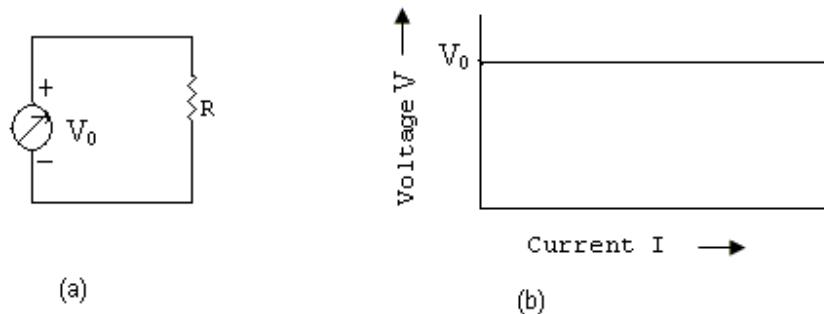


Fig. 1.5

(ii) Rewriting the equation (1.2), we get:

$$I_L = \frac{V_0 / R_0}{(1 + \frac{R_L}{R_0})} = \frac{I_0}{(1 + \frac{R_L}{R_0})} \quad \text{----- (1.4)}$$

It can be understood from this equation that the load current  $I_L$  will be equal to the short circuit current, if the  $\frac{R_L}{R_0} \rightarrow 0$  or  $R_L \ll R_0$ ; the source will behave like an ideal current source. That is the voltage source will act as a good current source if the source resistance is large enough than the load resistance. The current source is represented as short circuit current  $I_0$  and a source resistance  $R_0$  in parallel with it (fig.1.6). The ideal current source may be defined as follows:

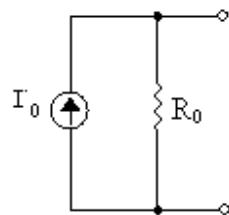


Fig. 1.6

**Ideal Current Source:** An ideal current source is one which delivers a constant current in the circuit irrespective of the load connected to it. The  $V-I$  relationship of the ideal current source and its symbolic representation are shown in figure 1.7.

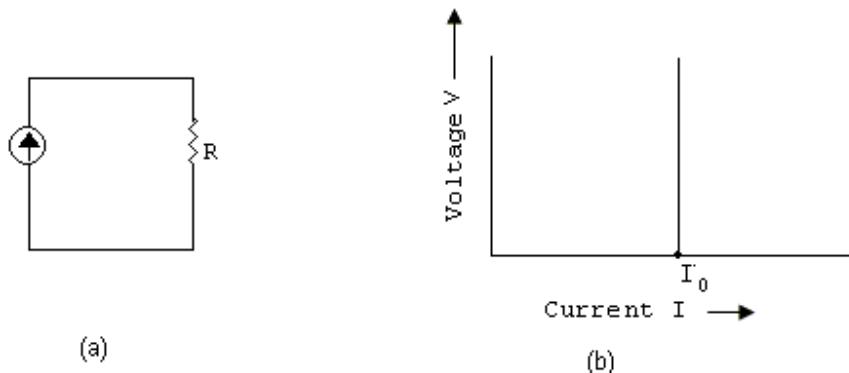


Fig. 1.7

(iii) Sometimes it becomes useful to transform or convert a voltage source into its equivalent current source or vice-versa. We equate the current flowing through the load resistance connected to both the circuits shown in fig. 1.8.

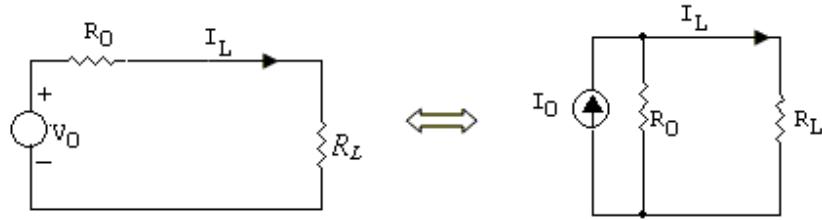


Fig. 1.8

From voltage equivalent circuit  $I_L = \frac{V_0}{(R_0 + R_L)}$  and

From Current equivalent circuit  $I_L = \frac{I_0 R_0 R_L}{(R_0 + R_L)}$

Equating these equations we have  $V_0 = R_0 I_0$  or  $I_0 = \frac{V_0}{R_0}$

It is, therefore, concluded that the voltage source  $V_0$  with a series resistance  $R_0$  may be transformed to its equivalent current source  $I_0$  and the resistance  $R_0$  in parallel with it. The value of current source  $I_0$  is given by  $I_0 = \frac{V_0}{R_0}$ . Similarly, a current source  $I_0$  with a resistance in parallel with it may be transformed to voltage source  $V_0$  and a resistance  $R_0$  in series with it.

The value of voltage source is given by  $V_0 = R_0 I_0$ .

**Example 1.1** A variable load resistance is connected to the terminals of a battery. When the current flowing in the load is 2A, the voltage across the load resistance is 5.8 volts; also when the load current is 5A, the voltage across the load resistance is 5.5 volts. All the measurements are made using ideal meters.

- Find: (a) Open circuit voltage and source resistance of the battery.  
 (b) Equivalent current source model of the battery.

Solution: (a) Let  $V_0$  and  $R_0$  are the open circuit voltage and source resistance of the battery respectively. As per statement of the problem:

(i) In the first case 5.8 volts = 2A  $R_L$  or  $R_L = 2.9 \Omega$ ;

$$\text{and } \frac{V_0 R_L}{(R_0 + R_L)} = 5.8 \quad \text{or} \quad \frac{V_0 \cdot (2.9)}{(R_0 + 2.9)} = 5.8 \quad \text{or} \quad V_0 = 2R_0 + 5.8$$

In the second case 5.5 volts = 5A  $R_L$  or  $R_L = 1.1 \Omega$ ;

$$\text{and } \frac{V_0 R_L'}{(R_0 + R_L')} = 5.5 \quad \text{or} \quad \frac{V_0 \cdot (1.1)}{(R_0 + 1.1)} = 5.5 \quad \text{or} \quad V_0 = 5R_0 + 5.5$$

From these two cases:  $V_0 = 6 \text{ volts}$  &  $R_0 = 0.1 \Omega$ .

(ii) The current source equivalent of the values calculated above is given in figure (1.9). The value of current source  $I_0 = 6 \times .1 = 60 \text{ mA}$

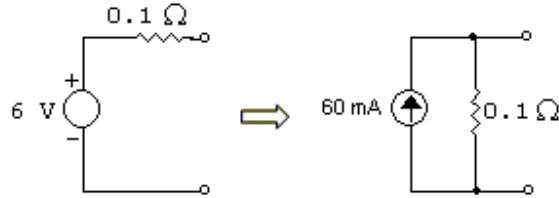


Fig. 1.9

**1.2 Network analysis:** The analysis of the electric circuits or networks which are formed by interconnecting the sources of electrical energy with other elements like resistances will now be discussed. Here consider the source of electrical energy as d.c. source which does not change with time. Simple circuits may be analyzed using well known Ohm's law. Kirchoff's laws may, however, be used to analyze more complicated circuits. Kirchoff presented two laws namely (i) Kirchoff's Current law (KCL) & (ii) Kirchoff's voltage law (KVL). These laws are the generalization of Ohm's law.

**1.2.1 Kirchoff's Current Law (KCL):** This law is applicable to any node or junction of electric circuit. The node or junction in an electric circuit is defined as the point where more than two elements meet. This law states that the algebraic sum of currents entering to any node of an electric circuit is zero. The total current entering to a node must be equal to that leaving it. The sign convention for this law is generally assumed that the current entering the node is positive while the current leaving the junction is negative. Mathematically, the law is  $\sum I = 0$ .

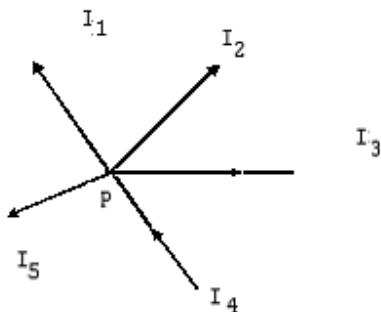


Fig. 1.10

This law may further be illustrated by considering the junction  $P$  shown in figure 1.10.  $I_1$ ,  $I_2$  &  $I_5$  are the currents entering the junction which are assumed to be positive while  $I_3$ , &  $I_4$  are negative, as these are leaving the junction.

$$\text{So } I_1 + I_2 - I_3 - I_4 + I_5 = 0$$

$$\text{or } I_1 + I_2 + I_5 = I_3 + I_4$$

Current leaving = Current entering

**1.2.2 Kirchoff's Voltage Law (KVL):** This law is applicable to a mesh or loop of an electric circuit. A mesh or loop is defined as a closed circuit. The Kirchoff's Voltage law states that the algebraic sum of all the voltage drops in any loop is zero.

The sign convention for applying the KVL to the closed loop is that an arbitrary reference direction of current in the clockwise direction is assumed. The associated reference direction across the resistances is marked positive at the tail of the arrow and negative to head of the arrow. If there is a voltage drop in the circuit, it is assumed to be positive while it is assumed to be negative for the voltage rise in the circuit.

For applying the KVL, we consider a closed circuit given the figure 1.11

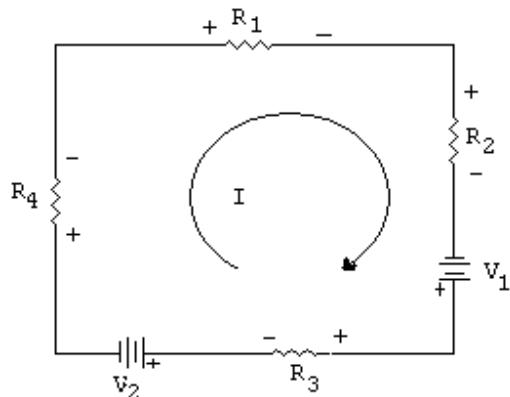


Fig 1.11

$$\text{From this figure: } R_1 I + R_2 I - V_1 + R_3 I + V_2 + R_4 I = 0$$

$$\text{or} \quad (R_1 + R_2 + R_3 + R_4)I = V_1 - V_2$$

From this equation it is clear that any unknown quantity may be calculated if rest of the quantities is known.

**Example 1.2** A voltmeter having the sensitivity of  $20\text{K}\Omega/\text{V}$  is used to measure the voltage across  $50\text{K}\Omega$  resistance in the circuit shown in the figure (1.12). The voltmeter is used in 50volts range.

Calculate (a) the reading of the voltmeter,  
(b) percentage error in the reading with respect to true value.

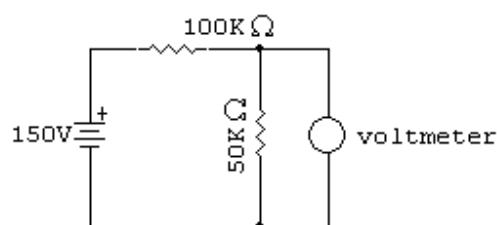


Fig. 1.12

Solution: The true voltage =  $\frac{150 \times 50K}{(100 + 50)K} = 50 \text{ volts}$

Resistance of the voltmeter in 50volt scale is

$$R_g = 50 \times 20K = 1M\Omega$$

When the voltage across  $50K\Omega$  resistance is measured, the voltmeter resistance  $R_g$  will also come in parallel with  $50K\Omega$  resistance. So the voltage will be measured across the parallel combination and not across  $50 K\Omega$  resistance. Due to which there will be an error.

Reading of the voltmeter  $V_m$  will be equal to the voltage across the parallel combination. Resistance of the parallel combination is given by:

$$R_{eq} = \frac{50K \times 1M}{(1M + 50K)} = 47.6K\Omega$$

$$\text{Voltmeter reading } V_m = \frac{150 \times 47.6}{(100 + 47.6)} = 48.36 \text{ volts}$$

$$\% \text{ error in the reading} = \frac{50 - 48.36}{50} = 3.28\%$$

**1.3 Mesh and Node Methods:** The practical or general approach of the KVL and KCL is mesh and node methods. These methods will now be discussed in detail.

**1.3.1 Node Method:** This method is used to determine the node voltages in the given network. The different nodes are identified in the network and one node is assumed as reference node. All other node voltages are then calculated with respect to the reference node. We find a set of nodal equations, representing one equation for each node. This method may be illustrated by considering a network shown in figure 1.13.

In this network, there are four independent nodes and one reference node. Let  $V_1$ ,  $V_2$ ,  $V_3$  &  $V_4$  are the node voltages at four nodes 1, 2, 3 & 4 respectively, with respect to reference node. The reference node is grounded (or is at zero potential).

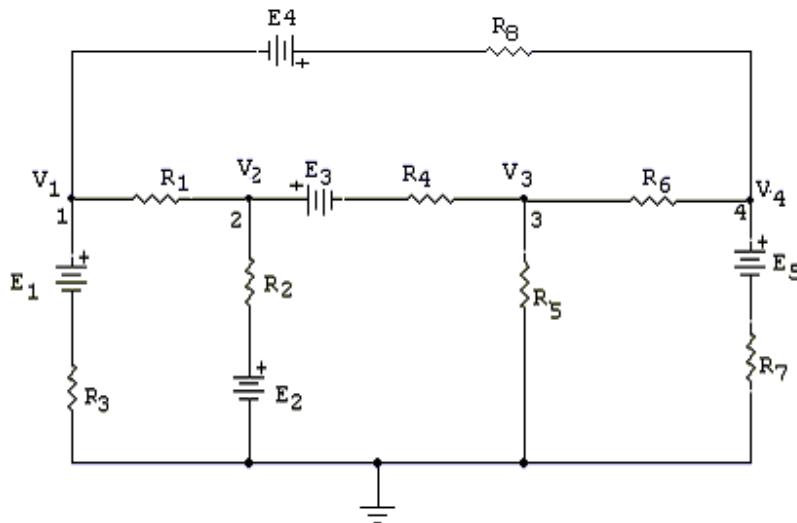


Fig. 1.13

For getting nodal equations, we first of all transform all the voltage sources into current sources as given in figure 1.14. The source  $E$  with a resistance  $R$  in series with it is replaced by a current source ( $I = \frac{E}{R}$ ) and the resistance  $R$  in parallel with the source.

The direction of arrow in the current source will depend upon the sign of voltage source. As it is well known that the conventional current flows from negative to positive inside the voltage source, the direction of arrow in the current source will also represent the inside view of the conventional current in the source.

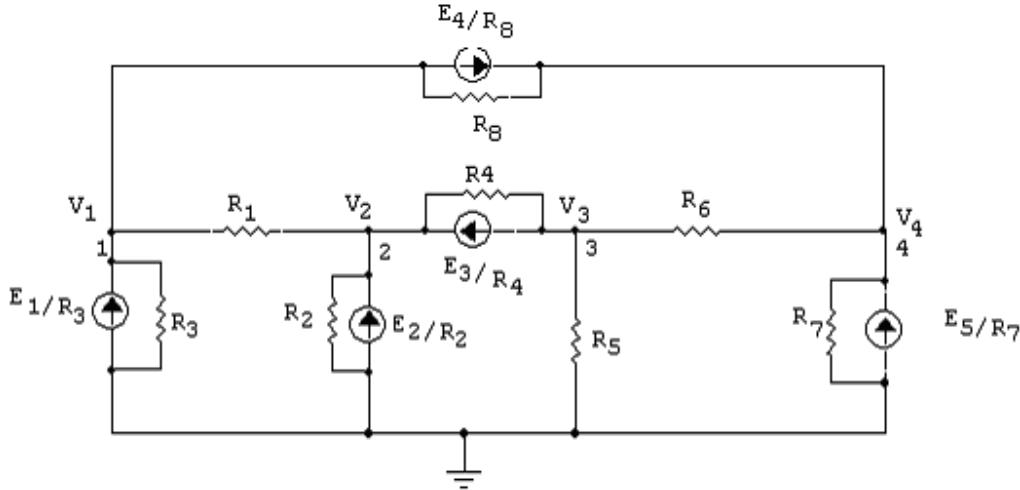


Fig. 1.14

By applying the Kirchoff's current law to each node (fig. 1.14), we may obtain the nodal equations as :

$$\text{I - Node : } \frac{V_1}{R_3} + \frac{V_1 - V_2}{R_1} + \frac{V_1 - V_4}{R_8} = \frac{E_1}{R_3} - \frac{E_4}{R_8}$$

Current leaving the node = current entering the node

$$\text{or } \left( \frac{1}{R_1} + \frac{1}{R_3} + \frac{1}{R_8} \right) V_1 - \frac{1}{R_1} V_2 - \frac{1}{R_8} V_4 = \frac{E_1}{R_3} - \frac{E_4}{R_8} = I_1 \quad (\text{say})$$

----- (1.5)

$$\text{II - Node: } \frac{V_2}{R_2} + \frac{V_2 - V_1}{R_1} + \frac{V_2 - V_3}{R_4} = \frac{E_2}{R_2} + \frac{E_3}{R_4}$$

$$\text{or } -\frac{1}{R_1} V_1 + \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_4} \right) V_2 - \frac{1}{R_4} V_3 = \frac{E_2}{R_2} + \frac{E_3}{R_4} = I_2 \quad (\text{say})$$

----- (1.6)

$$\text{III - Node: } \frac{V_3}{R_5} + \frac{V_3 - V_2}{R_4} + \frac{V_3 - V_4}{R_6} = -\frac{E_3}{R_4}$$

$$\text{or} \quad -\frac{1}{R_4}V_2 + \left( \frac{1}{R_4} + \frac{1}{R_5} + \frac{1}{R_6} \right)V_3 - \frac{1}{R_6}V_4 = -\frac{E_3}{R_4} = I_3 \quad (\text{say})$$

----- (1.7)

IV – node:

$$\frac{V_4}{R_7} + \frac{V_4 - V_3}{R_6} + \frac{V_4 - V_1}{R_8} = \frac{E_5}{R_7} + \frac{E_4}{R_8}$$

$$\text{or} \quad -\frac{1}{R_8}V_1 - \frac{1}{R_6}V_3 + \left( \frac{1}{R_6} + \frac{1}{R_7} + \frac{1}{R_8} \right)V_4 = \frac{E_5}{R_7} + \frac{E_4}{R_8} = I_4 \quad (\text{say})$$

----- (1.8)

If we concentrate on these equations, we may find some more easy method of writing these nodal equations. For this we rewrite the equation (1.5) as:

$$(G_1 + G_3 + G_5)V_1 - G_1V_2 - G_8V_4 = I_1 \quad \text{----- (1.9)}$$

where G are the conductances of their resistance values. This equation (1.9) may further be written in the general form as:

$$G_{11}V_1 - G_{12}V_2 - G_{13}V_3 - G_{14}V_4 = I_1$$

G's are the conductances of the corresponding resistances.

$G_{11}$  is the sum of conductances connected to the node 1, which is equal to  $\frac{1}{R_1} + \frac{1}{R_3} + \frac{1}{R_8}$  or  $(G_1 + G_3 + G_8)$ .

$G_{12}$  is the conductance connected between nodes 1 & 2, which is equal to  $\frac{1}{R_1}$  or  $G_1$ .

$G_{13}$  is the conductance connected between nodes 1 & 3, which is equal to 0.

$G_{14}$  is the conductance connected between nodes 1 & 4, which is equal to  $\frac{1}{R_8}$  or  $G_8$ .

The value of current  $I_1$  is the net current entering the node 1 which is equal to  $\frac{E_1}{R_3} - \frac{E_3}{R_8}$  as  $\frac{E_1}{R_3}$  current is entering the node 1 and  $\frac{E_3}{R_8}$  current is leaving the node 1 (hence the – ve sign).

The equations (1.6) to (1.8) may be rewritten in the similar fashion as:

$$\begin{aligned} -G_{21}V_1 + G_{22}V_2 - G_{23}V_3 - G_{24}V_4 &= I_2 \\ -G_{31}V_1 - G_{32}V_2 + G_{33}V_3 - G_{34}V_4 &= I_3 \\ -G_{41}V_1 - G_{42}V_2 - G_{43}V_3 + G_{44}V_4 &= I_4 \end{aligned}$$

In the matrix form these equations may be written as:

$$\begin{bmatrix} G_{11} & -G_{12} & -G_{13} & -G_{14} \\ -G_{21} & G_{22} & -G_{23} & -G_{24} \\ -G_{31} & -G_{32} & G_{33} & -G_{34} \\ -G_{41} & -G_{42} & -G_{43} & G_{44} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \quad \text{----- (1.10)}$$

In general G elements of the matrix are defined as:

$G_{ij}$  ( $i \neq j$ ) is the conductance connected between  $i^{\text{th}}$  and  $j^{\text{th}}$  node.

$G_{ii}$  ( $i = j$ ) is the sum of conductances connected to the  $i^{\text{th}}$  or  $j^{\text{th}}$  node.

$I_j$  is the net amount of current entering the  $j^{\text{th}}$  node.

$$[G][V] = [I] \quad \text{----- (1.11)}$$

The elements of  $G$  or  $I$  matrices are directly obtained from the given problem. It is worthwhile to mention here that the diagonal elements of  $[G]$  matrix are positive and off diagonal elements are always negative. This matrix is of  $4 \times 4$  orders as there are only 4 nodes. Thus we conclude that a matrix of  $n \times n$  orders will be obtained if there are  $n$  nodes in the given network. The matrix  $[G]$  may be solved for the node voltages by using the Cramer's rule.

**Example 1.3** Find the node voltages in the circuit given below.

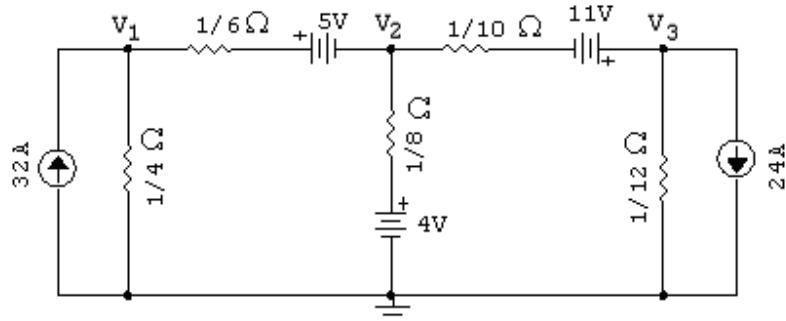


Fig. 1.15

**Solution:** Transform the voltage sources of the given network in to their equivalent current sources as shown in figure (1.16).

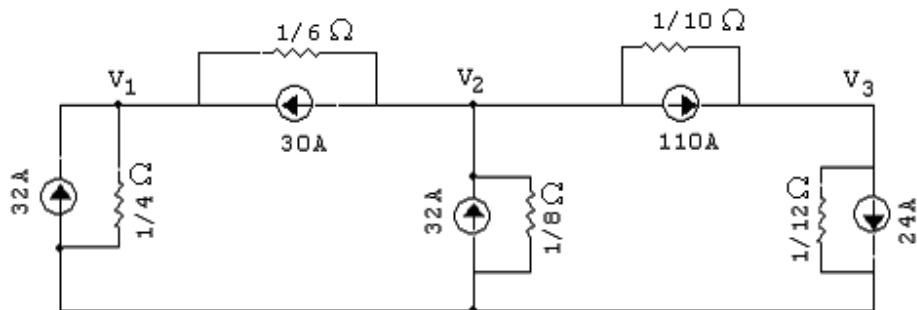


Fig. 1.16

We find the matrix equation of the form:  $[G][V] = [I]$

The  $G$  and  $I$  elements of the two matrices are obtained:

$$\begin{array}{lll} G_{11} = 4 + 6 = 10 \text{ mhos} & G_{12} = 6 \text{ mhos} & G_{13} = 0 \\ G_{21} = 6 \text{ mhos} & G_{22} = 6 + 8 + 10 = 24 \text{ mhos} & G_{23} = 10 \text{ mhos} \\ G_{31} = 0 & G_{32} = 10 \text{ mhos} & G_{33} = 10 + 12 = 22 \text{ mhos} \\ I_1 = 32 + 30 = 62A & I_2 = -30 + 32 - 110 = -108A & I_3 = -24 + 110 = 86A \end{array}$$

So we get the matrix as:

$$\begin{bmatrix} 10 & -6 & 0 \\ -6 & 24 & -10 \\ 0 & -10 & 22 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} 62 \\ -108 \\ 86 \end{bmatrix}$$

It can be solved for node voltages using Cramer's rule.

$$\Delta = \begin{vmatrix} 10 & -6 & 0 \\ -6 & 24 & -10 \\ 0 & -10 & 22 \end{vmatrix} = 10[22 \times 24 - 100] + 6[-6 \times 22] = 4280 - 860 = 3490$$

$$V_1 = \frac{\begin{vmatrix} 62 & -6 & 0 \\ -108 & 24 & -10 \\ 86 & -10 & 22 \end{vmatrix}}{\Delta} = \frac{62[22 \times 24 - 100] + 6[-(-108) \times 22 + 86 \times 10]}{3490} = \frac{17440}{3490} = 4.99 \text{ volts}$$

$$V_2 = \frac{\begin{vmatrix} 10 & 62 & 0 \\ -6 & -108 & -10 \\ 0 & 86 & 22 \end{vmatrix}}{\Delta} = \frac{10[(-108) \times 22 + 860] - 62[(-6) \times 22]}{3490} = \frac{-6976}{3490} = -1.99 \text{ volts}$$

$$V_3 = \frac{\begin{vmatrix} 10 & -6 & 62 \\ -6 & 24 & -108 \\ 0 & -10 & 86 \end{vmatrix}}{\Delta} = \frac{10[24 \times 86 - 108 \times 10] + 6[(-6) \times 86] + 62[60]}{3490} = \frac{10464}{3490} = 2.99 \text{ volt}$$

**1.3.2 Mesh or Loop Method:** Loop or Mesh method is used to find the loop currents in the given network. In the network different loops are first of all identified. The loop currents are assumed to be flowing in the different loops in the clock wise direction (reference direction). KVL is then applied to each loop, to get a set of different equations, the number of which will be equal to the loops present in the network. To discuss this method, consider a circuit shown in the figure (1.17).

In this figure there are four loops 1, 2, 3 & 4 in which  $I_1, I_2, I_3$  &  $I_4$  are assumed to be the loop currents flowing in the clock wise direction as shown figure. Four loop equations are obtained by applying KVL to each loop.

$$\begin{aligned} \text{Loop 1: } & R_1(I_1 - I_3) + R_2(I_1 - I_2) + E_2 + R_3I_1 - E_1 = 0 \\ \text{or } & (R_1 + R_2 + R_3)I_1 - R_2I_2 - R_3I_3 = E_1 - E_2 = V_1 \quad (\text{say}) \quad \text{----- (1.12)} \\ \text{Loop 2: } & R_2(I_2 - I_1) + E_3 + R_4(I_2 - I_3) + R_5(I_2 - I_4) - E_2 = 0 \end{aligned}$$

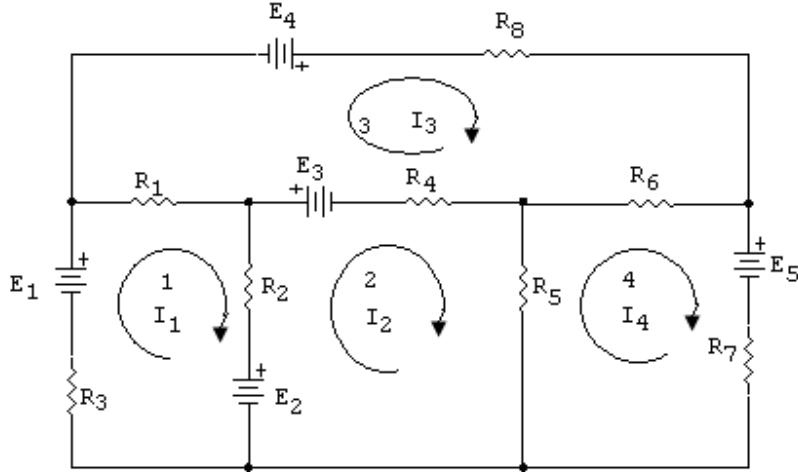


Fig.1.17

$$\text{or } -R_2I_1 + (R_2 + R_4 + R_5)I_2 - R_4I_3 - R_5I_4 = E_2 - E_3 = V_2 \quad (\text{say}) \quad \text{----- (1.13)}$$

$$\text{Loop 3 } -E_4 + R_8I_3 + R_6(I_3 - I_4) + R_4(I_3 - I_2) - E_3 + R_1(I_3 - I_1) = 0$$

$$\text{or } -R_1I_1 - R_4I_2 + (R_1 + R_4 + R_6 + R_8)I_3 - R_6I_4 = E_3 + E_4 = V_3 \quad (\text{say}) \quad \text{----- (1.14)}$$

$$\text{loop 4 } R_6(I_4 - I_3) + E_5 + R_7I_4 + R_5(I_4 - I_2) = 0$$

$$\text{or } -R_5I_2 - R_6I_3 + (R_5 + R_6 + R_7)I_4 = -E_5 = V_4 \quad (\text{say}) \quad \text{----- (1.15)}$$

These equations in the matrix form may be written as:

$$\begin{bmatrix} (R_1 + R_2 + R_3) & -R_2 & -R_1 & 0 \\ -R_2 & (R_2 + R_4 + R_5) & -R_4 & -R_5 \\ -R_1 & -R_4 & (R_1 + R_4 + R_6 + R_8) & -R_6 \\ 0 & -R_5 & -R_6 & (R_5 + R_6 + R_7) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \quad \text{----- (1.16)}$$

General form of the matrix may be written as:

$$\begin{bmatrix} R_{11} & -R_{12} & -R_{13} & -R_{14} \\ -R_{21} & R_{22} & -R_{23} & -R_{24} \\ -R_{31} & -R_{32} & R_{33} & -R_{34} \\ -R_{41} & -R_{42} & -R_{43} & R_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \quad \text{----- (1.17)}$$

We define the elements of the matrix in the general form as:

$R_{ij}$  ( $i \neq j$ ) is the resistance common between  $i^{\text{th}}$  and  $j^{\text{th}}$  loop.

$R_{ii}$  ( $I = j$ ) is the sum of resistances connected to the  $i^{\text{th}}$  or  $j^{\text{th}}$  loop.

$V_j$  is the net voltage rise in  $j^{\text{th}}$  loop.

$$[R][I] = [V] \quad \text{----- (1.18)}$$

The elements of R or V matrices are directly obtained from the given problem. The diagonal elements of the [R] matrix are positive and off diagonal elements are negative. The [R] matrix may be solved for the loop currents by using the Cramer's rule.

**Example 1.4** Solve for the loop currents in the circuit given below. Values of the resistances in the circuit are given in ohms.

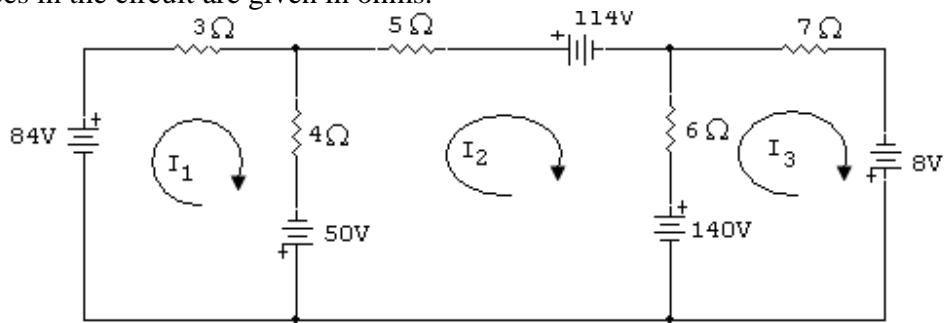


Fig. 1.18

Solution: To find the loop currents we apply the Loop Method and get the matrix of the form  $[R][I]=[V]$

The R's elements of the network are obtained as:

$$\begin{aligned} R_{11} &= 3 + 4 = 7\Omega & R_{12} &= 4\Omega & R_{13} &= 0 \\ R_{21} &= 4\Omega & R_{22} &= 4 + 5 + 6 = 15\Omega & R_{23} &= 6\Omega \\ R_{31} &= 0 & R_{32} &= 6\Omega & R_{33} &= 6 + 7 = 13\Omega \\ V_1 &= 50 + 84 = 134V & V_2 &= -114 - 140 - 50 = -304V & V_3 &= 8 + 140 = 148V \end{aligned}$$

We get the matrix as:

$$\begin{bmatrix} 7 & -4 & 0 \\ -4 & 15 & -6 \\ 0 & -6 & 13 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 134 \\ -304 \\ 148 \end{bmatrix} \quad \text{----- (1.19)}$$

It can be solved for loop currents using Cramer's rule:

$$\Delta = \begin{vmatrix} 7 & -4 & 0 \\ -4 & 15 & -6 \\ 0 & -6 & 13 \end{vmatrix} = 7[15 \times 13 - (-6) \times (-6)] + 4[(-4) \times 13] = 1113 - 208 = 905$$

$$I_1 = \frac{\begin{vmatrix} 134 & -4 & 0 \\ -304 & 15 & -6 \\ 148 & -6 & 13 \end{vmatrix}}{\Delta} = \frac{134[15 \times 13 - (-6) \times (-6)] + 4[(-304) \times 13 - (-6) \times 148]}{905} = \frac{21306 - 12256}{905} = 10A$$

$$I_2 = \frac{\begin{vmatrix} 7 & 134 & 0 \\ -4 & -304 & -6 \\ 0 & 148 & 13 \end{vmatrix}}{\Delta} = \frac{7[(-304) \times 13 - (-6) \times 148] - 134[(-4) \times 13]}{905} = \frac{-21448 + 6968}{905} = -16A$$

$$I_3 = \frac{\begin{vmatrix} 7 & -4 & 134 \\ -4 & 15 & -304 \\ 0 & -6 & 148 \end{vmatrix}}{\Delta} = \frac{7[15 \times 148 - (-304)(-6)] + 4[(-4) \times 148] + 134[(-4) \times (-6)]}{905} = \frac{2772 - 2368 + 3216}{905} = 4A$$

**1.4 Network Theorems:** General methods of network analysis discussed earlier provide lengthy calculations in complicated networks. It is required to develop some easy methods in solving the network problems. The network theorems, which are applicable for both A.C. and D.C. networks, are helpful in solving the complicated network problems. Some of the important theorems Viz. Superposition Theorem, Thevenin's Theorem, Norton's theorem, Reciprocity Theorem, Millman's Theorem, and Maximum Power Transfer Theorem will be discussed below.

**Superposition Theorem:** This theorem states that in a network containing impedances and sources (voltage sources and/or current sources), the current flowing at any point is the algebraic sum of the currents that would flow at that point if each source was considered separately, and all other sources were replaced with their internal impedances.

**Proof:** To prove this theorem, consider a network shown in the figure (1.19). In this circuit we assume that  $I_1$  and  $I_2$  are the two loop currents of the network flowing in the clockwise direction. It is further assumed that  $I'_1$  and  $I'_2$  are the two currents flowing in these loops when only  $V_1$  voltage source is considered and  $V_2$  is short circuited (Fig. 1.20 a).

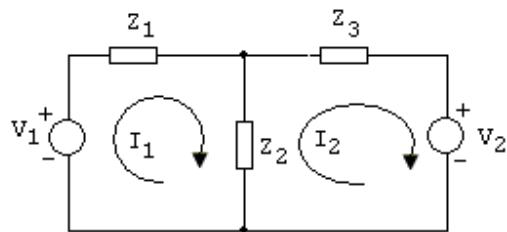


Fig. 1.19

Similarly,  $I_1'$  and  $I_2'$  are two currents in these two loops when only  $V_2$  voltage source is considered and  $V_1$  is short circuited (Fig. 1.20 b).

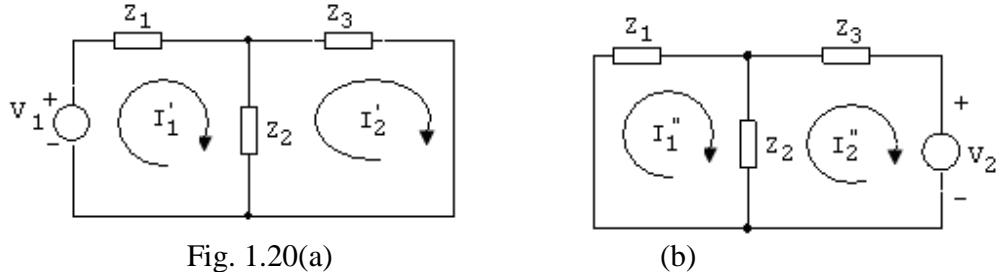


Fig. 1.20(a)

(b)

According to this theorem, we should get:

$$I_1 = I_1' + I_1'' \text{ and } I_2 = I_2' + I_2''$$

By applying Loop method in the two meshes (ref. Fig. 1.19), we get:

$$\begin{bmatrix} (Z_1 + Z_2) & -Z_2 \\ -Z_2 & (Z_2 + Z_3) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_1 \\ -V_2 \end{bmatrix} \quad \text{----- (1.21)}$$

By considering only  $V_1$  source and  $V_2$  is short circuited (putting  $V_2 = 0$ ) in Fig. 1.20(a), we get

$$\begin{bmatrix} (Z_1 + Z_2) & -Z_2 \\ -Z_2 & (Z_2 + Z_3) \end{bmatrix} \begin{bmatrix} I_1' \\ I_2' \end{bmatrix} = \begin{bmatrix} V_1 \\ 0 \end{bmatrix} \quad \text{----- (1.22)}$$

Now by considering only  $V_2$  source and  $V_1$  is short circuited (putting  $V_1 = 0$ ) Fig. 1.20(b), we get

$$\begin{bmatrix} (Z_1 + Z_2) & -Z_2 \\ -Z_2 & (Z_2 + Z_3) \end{bmatrix} \begin{bmatrix} I_1'' \\ I_2'' \end{bmatrix} = \begin{bmatrix} 0 \\ -V_2 \end{bmatrix} \quad \text{----- (1.23)}$$

Since [Z] matrix of both the equations (1.22) & (1.23) are same so we may combine these equations, as:

$$\begin{bmatrix} (Z_1 + Z_2) & -Z_2 \\ -Z_2 & (Z_2 + Z_3) \end{bmatrix} \begin{bmatrix} I_1' + I_1'' \\ I_2' + I_2'' \end{bmatrix} = \begin{bmatrix} V_1 \\ -V_2 \end{bmatrix} \quad \text{----- (1.24)}$$

Comparing equations (1.21) & (1.24) we get the required result.

$$I_1 = I_1' + I_1'' \text{ and } I_2 = I_2' + I_2''$$

Hence the theorem is proved.

**Example 1.5** Using Superposition theorems, find the current flowing through each resistances in the following circuit. The values of all resistances in the circuit are given in ohms.

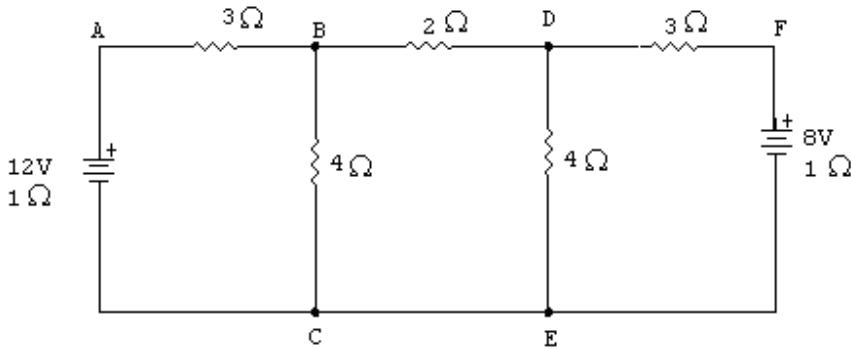


Fig. 1.21

**Solution:** In this circuit first only  $12V$  source is considered and other  $8V$  source is replaced by its internal resistance as shown in the figure 1.22. In this way we find the current flowing through all the resistances.

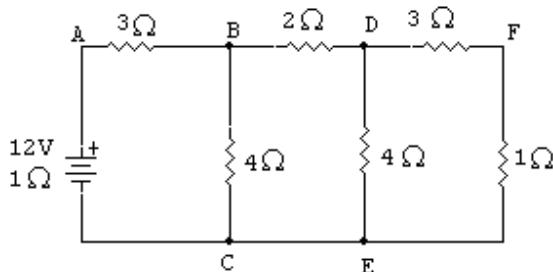


Fig. 1.22

The resistance between B & C points is  $2\Omega$  (parallel combination of two  $4\Omega$  resistances).

$$\text{Current flowing through AB branch is } I_{AB} = \frac{12}{3+1+2} = 2A \text{ from A to B}$$

$$\text{Current flowing through BC branch is } I_{BC} = \frac{I_{AB}}{2} = 1A \text{ from B to C}$$

$$\text{Current flowing through BD branch is } I_{BD} = I_{BC} = 1A \text{ from B to D}$$

$$\text{Current flowing through DE branch is } I_{DE} = \frac{I_{BD}}{2} = 0.5A \text{ from D to E}$$

$$\text{Current flowing through DF branch is } I_{DF} = I_{DE} = 0.5A \text{ from D to F}$$

Now other source of  $8$  volts is considered and  $12$  volt source is replaced by its internal resistance as shown in the circuit (fig. 1.23). The resistance between D & E points is  $2\Omega$  (parallel combination of two  $4\Omega$  resistances).

$$\text{Current flowing through DF branch is } I_{DF} = \frac{8}{3+1+2} = 1.33A \text{ from F to D}$$

$$\text{Current flowing through DE branch is } I_{DE} = \frac{I_{DF}}{2} = 0.67A \text{ from D to E}$$

$$\text{Current flowing through BD branch is } I_{BD} = I_{DE} = 0.67A \text{ from D to B}$$

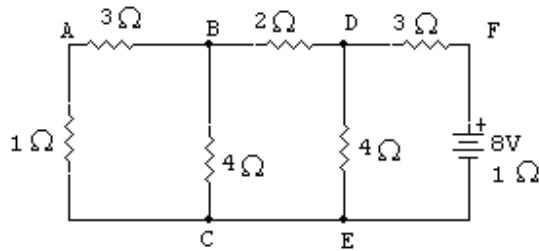


Fig. 1.23

Current flowing through BC branch is  $I_{BC}'' = \frac{I_{BD}}{2} = 0.33A$  from B to C

Current flowing through AB branch is  $I_{AB}'' = I_{BC}'' = 0.33A$  from B to A

The required current in AB branch  $I_{AB} = I_{AB}' - I_{AB}'' = 2 - 0.33 = 1.67A$  (A to B)

The required current in BC branch  $I_{BC} = I_{BC}' + I_{BC}'' = 1 + 0.33 = 1.33A$  (B to C)

The required current in BD branch  $I_{BD} = I_{BD}' - I_{BD}'' = 1 - 0.67 = 0.33A$  (B to D)

The required current in DE branch  $I_{DE} = I_{DE}' + I_{DE}'' = 0.5 + 0.67 = 1.17A$  (D to E)

The required current in DF branch  $I_{DF} = I_{DF}' - I_{DF}'' = 1.33 - 0.5 = 0.83A$  (F to D)

**1.4.2 Thevenin's Theorem:** Any network containing impedances and sources (voltage sources and/or current sources) can be replaced with a voltage source  $V_0$  and an impedance  $Z_0$  in series with it. The value of voltage source  $V_0$  is the open circuit voltage at the output terminals of the network,  $Z_0$  is the impedance at the output terminals of the network replacing all the sources with their internal impedances. According to this theorem, any network containing sources and impedances shown in figure 1.24(a) can be replaced by the circuit shown in figure 1.24(b)

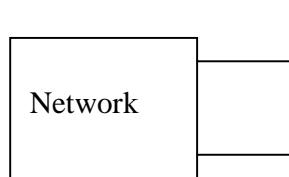


Fig. 1.24(a)

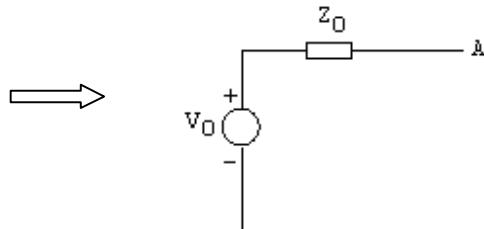


Fig. 1.24(b)

Proof: To establish Thevenin's theorem, a network containing voltage source and impedances is considered, which is shown in figure (1.25a).

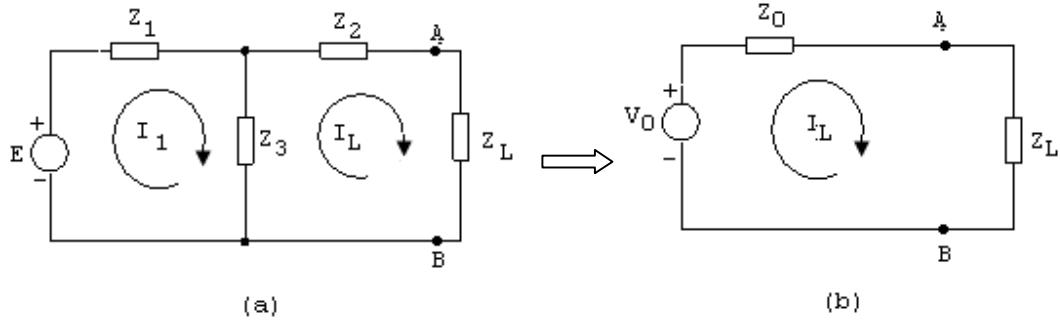


Fig. 1.25

According to this theorem, this network should be equal to a voltage source ( $V_0$ ) and impedance in series with it, as shown in fig. (1.25b). The load current will be calculated from both the circuits and will be proved that the two currents are equal.

Applying the loop method to the circuit of figure (1.25 a), we get:

$$\begin{bmatrix} (Z_1 + Z_3) & -Z_3 \\ -Z_3 & (Z_2 + Z_3 + Z_L) \end{bmatrix} \begin{bmatrix} I_1 \\ I_L \end{bmatrix} = \begin{bmatrix} E \\ 0 \end{bmatrix} \quad \text{----- (1.25)}$$

The value of  $I_L$  can be calculated from this equation, using Cramer's rule:

$$I_L = \frac{\begin{vmatrix} (Z_1 + Z_3) & E \\ -Z_3 & 0 \end{vmatrix}}{\begin{vmatrix} (Z_1 + Z_3) & -Z_3 \\ -Z_3 & (Z_2 + Z_3 + Z_L) \end{vmatrix}} = \frac{EZ_3}{(Z_1 + Z_3)(Z_2 + Z_3 + Z_L) - Z_3^2}$$

$$\text{or } I_L = \frac{E.Z_3}{Z_1Z_2 + Z_1Z_3 + Z_1Z_L + Z_2Z_3 + Z_3Z_L} \quad \text{----- (1.26)}$$

We now calculate the value of open circuit voltage  $V_0$  across AB terminals and Thevenin's impedance  $Z_0$  from the figure (1.25a), after removing the load impedance  $Z_L$

$$\text{as: } V_0 = \frac{E}{(Z_1 + Z_3)} Z_3$$

and  $Z_0 = Z_2 + Z_1 \parallel Z_3$  (Short circuiting the voltage source)

$$= Z_2 + \frac{Z_1 Z_3}{Z_1 + Z_3} = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_1 Z_3}{Z_1 + Z_3}$$

The load current  $I_L$  may be obtained from the fig. (1.25b) as:

$$I_L = \frac{V_0}{Z_0 + Z_L} = \frac{E \cdot Z_3 / (Z_1 + Z_3)}{(Z_1 Z_2 + Z_2 Z_3 + Z_1 Z_3 + Z_1 Z_L + Z_3 Z_L) / (Z_1 + Z_3)}$$

$$= \frac{E \cdot Z_3}{Z_1 Z_2 + Z_1 Z_3 + Z_1 Z_L + Z_2 Z_3 + Z_3 Z_L} \quad \text{----- (1.27)}$$

From the equations (1.26) & (1.27), we see that the value of  $I_L$  is the same, as calculated from both the circuits (Fig. 1.25a & 1.25 b).  
Hence the theorem is proved.

**Example 1.6** Find the Thevenin's equivalent of the network inside the Box

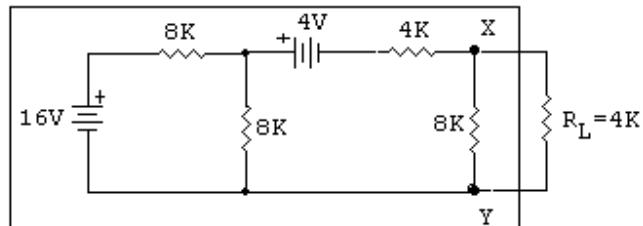


Fig. 1.26

of figure (1.26) and then calculate the current flowing through the load resistance  $R_L$  connected between XY terminals.

**Solution:** We are to find the open circuit voltage across XY terminals and the resistance across these two terminals when the sources have been replaced with their internal resistances. To find the voltage across XY terminals we may use loop method, and get the current flowing through these terminals removing the load resistance. Let  $I_1$  and  $I_2$  are the two current in the two loops as shown in fig. (1.27).

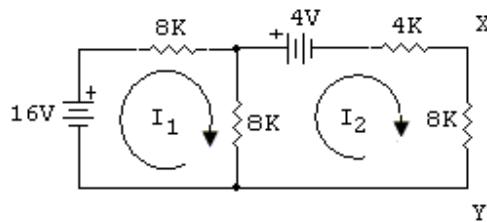


Fig. 1.27

The loop equation is given by:  $[R][I] = [V]$

$$\text{or } \begin{bmatrix} 16 & -8 \\ -8 & 20 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 16 \\ -4 \end{bmatrix} \quad \dots \dots (1.28)$$

$$\text{and } I_2 = \frac{\begin{vmatrix} 16 & 16 \\ -8 & -4 \end{vmatrix}}{\begin{vmatrix} 16 & -8 \\ -8 & 20 \end{vmatrix}} = \frac{[-64 + 16 \times 8]}{[16 \times 20 - 64]} = \frac{64}{256} = 0.25 \text{ mA}$$

(Resistance values are in Kilo-ohms hence current is in mA)

$$V_{XY} = 0.25 \text{ mA} \times 8 \text{ K}\Omega = 2 \text{ Volts}$$

Thevenin's resistance  $R_{XY} = [(8K \parallel 8K) + 4k] \parallel 8K = 8K \parallel 8K = 4K\Omega$  (All the sources are shorted).

The Thevenin's equivalent is shown in figure (1.28):

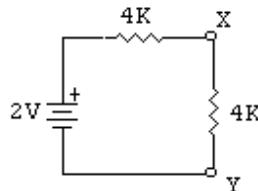


Fig. 1.28

$$\text{The load current is given by: } I_L = \frac{2\text{Volts}}{(4K + 4K)} = 0.25mA.$$

**1.4.3 Norton's Theorem:** Any network containing impedances and sources (voltage and / or current sources) can be replaced with a current

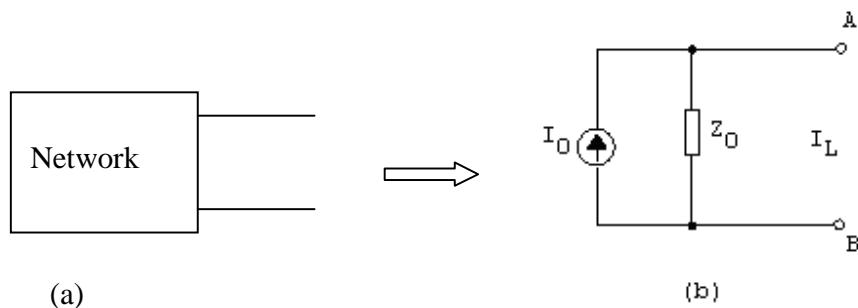


Fig. 1.29

source  $I_0$  and an impedance  $Z_0$  in Parallel with it. The value of current source  $I_0$  is the short circuit current obtained at the output terminals of the network,  $Z_0$  is the impedance at its output terminals replacing all the sources with their internal impedances. According to this theorem, any network containing sources and impedances (ref. figure 1.29a) can be replaced by a circuit shown in fig.(1.29 b).

Proof: To illustrate Norton's theorem, a network containing voltage source and impedances is considered, which is shown in figure (1.30a). As

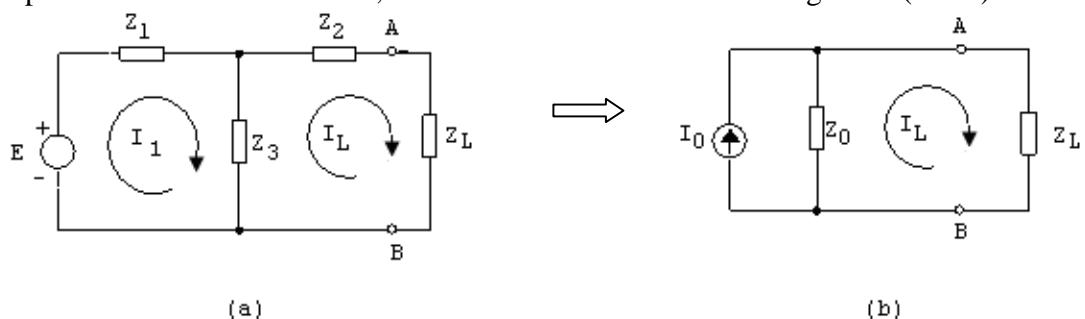


Fig. 1.30

discussed earlier, this network should be equal to a current source ( $I_0$ ) and impedance ( $Z_0$ ) in parallel with it (ref. fig. 1.30 b). Norton's theorem will be proved if the load current calculated from both the circuits is equal.

Applying the loop method to the circuit of figure (1.30 a), it is obtained as:

$$\begin{bmatrix} (Z_1 + Z_3) & -Z_3 \\ -Z_3 & (Z_2 + Z_3 + Z_L) \end{bmatrix} \begin{bmatrix} I_1 \\ I_L \end{bmatrix} = \begin{bmatrix} E \\ 0 \end{bmatrix} \quad \text{----- (1.29)}$$

Using Cramer's rule, the value of  $I_L$  can be calculated as:

$$I_L = \frac{\begin{vmatrix} (Z_1 + Z_3) & E \\ -Z_3 & 0 \end{vmatrix}}{\begin{vmatrix} (Z_1 + Z_3) & -Z_3 \\ -Z_3 & (Z_2 + Z_3 + Z_L) \end{vmatrix}} = \frac{EZ_3}{(Z_1 + Z_3)(Z_2 + Z_3 + Z_L) - Z_3^2}$$

$$\text{or} \quad I_L = \frac{EZ_3}{Z_1Z_2 + Z_1Z_3 + Z_1Z_L + Z_2Z_3 + Z_3Z_L} \quad \text{----- (1.30)}$$

Now the short circuit current  $I_0$  will be calculated by short circuiting the output terminals as shown in figure (1.31). Loop method may be used to calculate the short circuit current  $I_0$ .

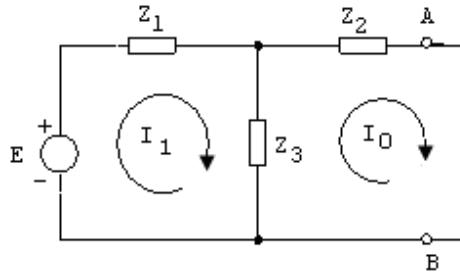


Fig. 1.31

Loop equations are given by:

$$\begin{bmatrix} (Z_1 + Z_3) & -Z_3 \\ -Z_3 & (Z_2 + Z_3) \end{bmatrix} \begin{bmatrix} I_1 \\ I_0 \end{bmatrix} = \begin{bmatrix} E \\ 0 \end{bmatrix}$$

$$I_0 = \frac{\begin{vmatrix} (Z_1 + Z_3) & E \\ -Z_3 & 0 \end{vmatrix}}{\begin{vmatrix} (Z_1 + Z_3) & -Z_3 \\ -Z_3 & (Z_2 + Z_3) \end{vmatrix}} = \frac{EZ_3}{(Z_1 + Z_3)(Z_2 + Z_3) - Z_3^2}$$

$$\text{or} \quad I_0 = \frac{EZ_3}{Z_1Z_2 + Z_1Z_3 + Z_1Z_L + Z_2Z_3} \quad \text{----- (1.31)}$$

The impedance  $Z_0$  is obtained by removing the load impedance in the given network. It is given by:

$$\begin{aligned} Z_0 &= Z_2 + Z_1 \parallel Z_3 \\ &= Z_2 + \frac{Z_1 Z_3}{Z_1 + Z_3} = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_1 Z_3}{Z_1 + Z_3} \end{aligned} \quad \text{----- (1.32)}$$

The load current can also be calculated using the Norton's equivalent circuit (fig. 1.30 b) as:

$$I_L = \frac{Z_0 \cdot Z_L}{(Z_0 + Z_L)} \frac{I_0}{Z_L} = \frac{Z_0 I_0}{(Z_0 + Z_L)} \quad \text{----- (1.33)}$$

Putting the values of  $Z_0$  and  $I_0$  from the equations (1.32) & (1.31) in equation (1.33) we get the value of  $I_L$  as:

$$I_L = \frac{E Z_3}{Z_1 Z_2 + Z_1 Z_3 + Z_1 Z_L + Z_2 Z_3 + Z_3 Z_L} , \text{ which is same as}$$

calculated directly from the given network. This proves the Norton's theorem.

Thevenin's and Norton's equivalent circuit of a given network produces same amount of current and voltage in the load impedance. Hence these theorems are the dual of each other. Therefore, either of the two theorems can be applied for the network analysis.

**Example 1.7** Draw Norton's equivalent of the network and find the current in  $2\Omega$  resistance connected between AB branch in the figure (1.32).

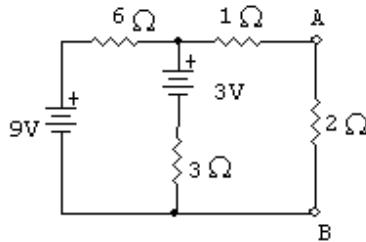


Fig. 1.32

**Solution:** To draw the Norton's equivalent, the short circuit current in AB branch is obtained by short circuiting these terminals as shown in figure (1.33). In this figure the short circuit current will be  $I_2$  which may be obtained by the loop method.

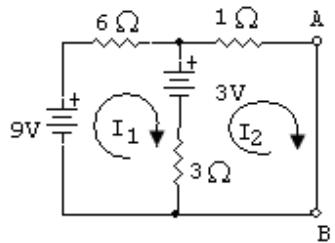


Fig. 1.33

The loop equation is given as:  $[R][I] = [I]$

$$\begin{bmatrix} 9 & -3 \\ -3 & 4 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 6 \\ 3 \end{bmatrix}$$

$$\text{And } I_2 \text{ is given by: } I_2 = \frac{\begin{vmatrix} 9 & 6 \\ -3 & 3 \end{vmatrix}}{\begin{vmatrix} 9 & -3 \\ -3 & 4 \end{vmatrix}} = \frac{27+18}{36-9} = \frac{45}{27} = \frac{5}{3} A$$

The resistance  $R_0$  is measured at the output terminals, removing the  $2\Omega$  resistance between AB branch and short circuiting the voltage sources in the network.

$R_0 = 1 + \frac{3 \times 6}{3+6} = 3\Omega$ . The Norton's equivalent is, therefore, shown in figure (1.34).

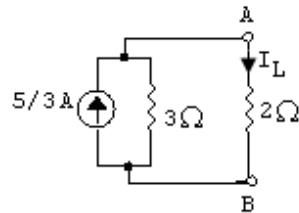


Fig. 1.34

The required current  $I_L$  through  $2\Omega$  resistance is given by:

$$I_L = \frac{5}{3} \cdot \frac{2 \times 3}{2+3} \cdot \frac{1}{3} = \frac{2}{3} A$$

**1.4.4 Reciprocity Theorem:** This theorem states that when an ideal voltage source is applied to one loop of the given network of linear impedances, produces a current in the second loop, then the same amount of current will be produced in the first loop of the given network if that ideal voltage source is applied to the second loop.

**Proof:** To prove this theorem, we consider a network shown in figure (1.35), in

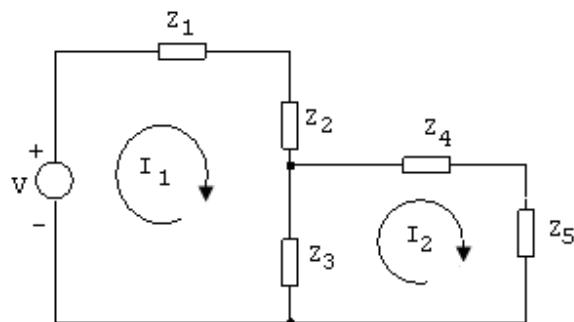


Fig. 1.35

which an ideal voltage source  $V$  is introduced in loop 1 and current  $I_2$  is produced in loop 2. Again, we introduce the ideal voltage source  $V$  in the loop 2 and  $I'_1$  current is produced in loop 1 as shown in figure (1.36).

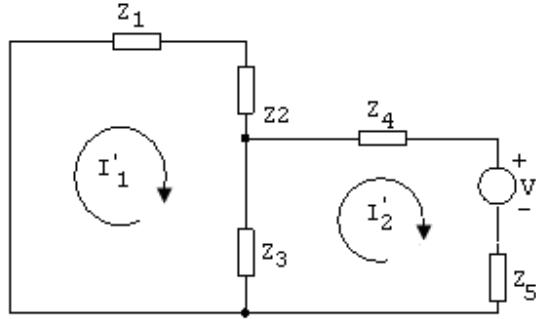


Fig. 1.36

According to this theorem,  $|I_2| = |I'_1|$ .

To prove this we find the current  $I_2$  from figure (1.35). For this loop method is applied to get the loop equations which are given the matrix form as:

$$\begin{bmatrix} (Z_1 + Z_2 + Z_3) & -Z_3 \\ -Z_3 & (Z_3 + Z_4 + Z_5) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V \\ 0 \end{bmatrix} \quad \text{----- (1.34)}$$

The current  $I_2$  is calculated using Cramer's rule as:

$$I_2 = \frac{\begin{vmatrix} (Z_1 + Z_2 + Z_3) & V \\ -Z_3 & 0 \end{vmatrix}}{(Z_1 + Z_2 + Z_3)(Z_3 + Z_4 + Z_5) - Z_3^2} = \frac{Z_3 \cdot V}{(Z_1 + Z_2 + Z_3)(Z_3 + Z_4 + Z_5) - Z_3^2} \quad \text{----- (1.35)}$$

Similarly, we get the mesh equations in the matrix form from the fig. (1.36)

$$\begin{bmatrix} (Z_1 + Z_2 + Z_3) & -Z_3 \\ -Z_3 & (Z_3 + Z_4 + Z_5) \end{bmatrix} \begin{bmatrix} I'_1 \\ I'_2 \end{bmatrix} = \begin{bmatrix} 0 \\ -V \end{bmatrix} \quad \text{----- (1.36)}$$

The current  $I'_1$  is calculated using Cramer's rule as:

$$I'_1 = \frac{\begin{vmatrix} 0 & -Z_3 \\ -V & (Z_3 + Z_4 + Z_5) \end{vmatrix}}{(Z_1 + Z_2 + Z_3)(Z_3 + Z_4 + Z_5) - Z_3^2} = \frac{-Z_3 \cdot V}{(Z_1 + Z_2 + Z_3)(Z_3 + Z_4 + Z_5) - Z_3^2} \quad \text{----- (1.37)}$$

From the equations (1.35) & (1.37), it is clear that  $|I_2| = |I_1|$

Hence the Reciprocity theorem is established.

It follows from Reciprocity theorem that in any linear network containing linear impedances and sources, the ratio of voltage introduced in one loop to the current in any second loop is the same as the ratio of voltage introduced in second loop and the current introduced in first loop, other sources being replaced by their internal impedances.

**Example 1.8** Verify the Reciprocity theorem in the circuit shown below. The values of all the resistances in the circuit are given in ohms.

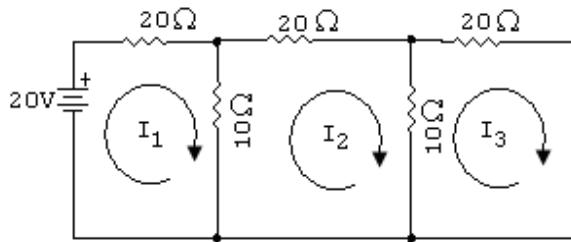


Fig. 1.37

Solution: We find the current  $I_3$  in the third loop using loop method, when 20 V source is connected in the first loop.

$$\begin{bmatrix} 30 & -10 & 0 \\ -10 & 40 & -10 \\ 0 & -10 & 30 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 20 \\ 0 \\ 0 \end{bmatrix} \quad \dots \quad (1.38)$$

$$I_3 = \frac{\begin{vmatrix} 30 & -10 & 20 \\ -10 & 40 & 0 \\ 0 & -10 & 0 \end{vmatrix}}{\begin{vmatrix} 30 & -10 & 0 \\ -10 & 40 & -10 \\ 0 & -10 & 30 \end{vmatrix}} = \frac{30[0] + 10[0] + 20[100]}{30[40 \times 30 - 100] + 10[(-10) \times 30] + 0} = \frac{2000}{30000} = \frac{1}{15} = 67mA$$

Now we apply the source in the third loop as given in the figure (1.38) and find the current  $I'_1$  in the first loop as:

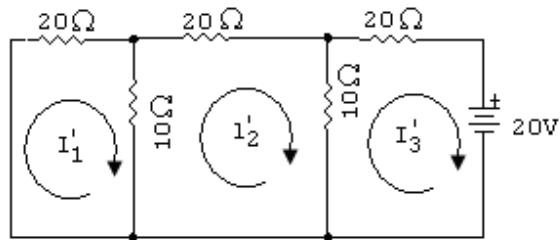


Fig. 1.38

$$I_1 = \frac{\begin{vmatrix} 0 & -10 & 0 \\ 0 & 40 & -10 \\ -20 & -10 & 30 \\ 30 & -10 & 0 \\ -10 & 40 & -10 \\ 0 & -10 & 30 \end{vmatrix}}{30[40 \times 30 - 100] + 10[(-10) \times 30] + 0} = \frac{0 + 10[-200]}{30[40 \times 30 - 100] + 10[(-10) \times 30] + 0} = \frac{-2000}{30000} = \frac{-1}{15} = -67mA$$

Here  $|I_3| = |I_1|$  hence the network is reciprocal.

**1.4.5 Millman's Theorem:** This theorem states that if several voltage sources in series with impedances are connected as shown in figure (1.39 a), then the equivalent circuit may be represented by a voltage source  $V_m$  and an impedance  $Z_m$  in series with it as shown in figure (1.39 b). The value of voltage source  $V_m$  is given by:

$$V_m = \frac{V_1 Y_1 + V_2 Y_2 + V_3 Y_3 + \dots + V_N Y_N}{Y_1 + Y_2 + Y_3 + \dots + Y_N} = \frac{\sum_{I=1}^N V_I Y_I}{\sum_{I=1}^N Y_I}$$

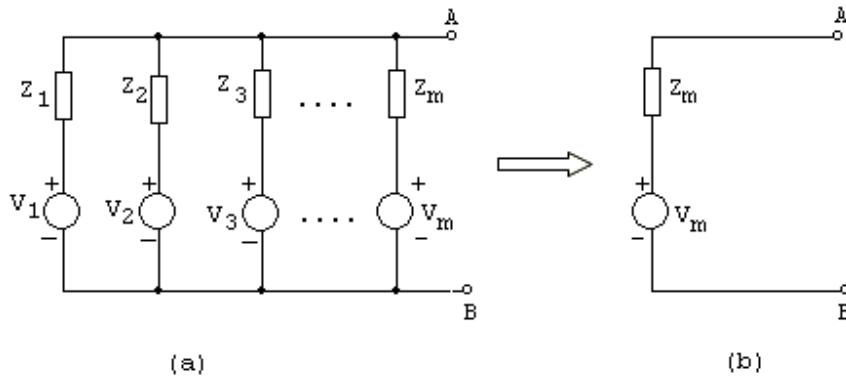


Fig. 1.39

and  $Z_m = \frac{1}{Y_1 + Y_2 + Y_3 + \dots + Y_N}$ , and  $Y$  are the admittances ( $Z = \frac{1}{Y}$ ).

**Proof:** We replace each voltage source with its impedance in series, with current source and its impedance in parallel as shown in figure (1.40 a).

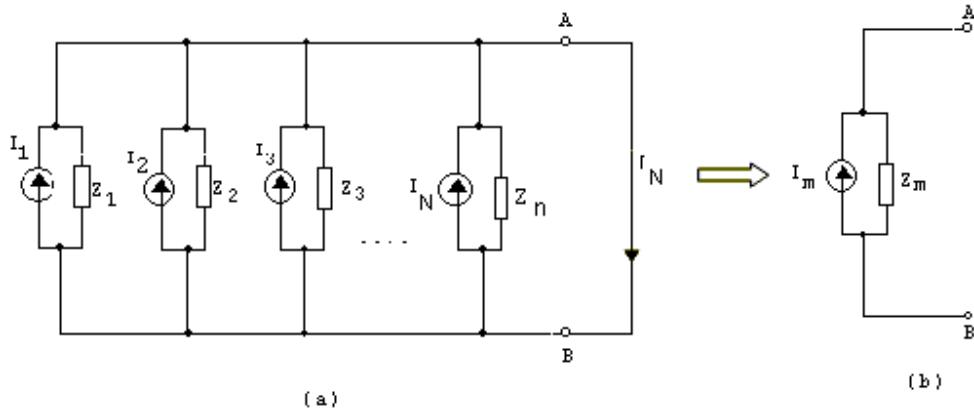


Fig. 1.40

The short circuit current  $I_m$  is given by:  $I_m = I_1 + I_2 + I_3 + \dots + I_n$

$$\begin{aligned} I_m &= \frac{V_1}{Z_1} + \frac{V_2}{Z_2} + \frac{V_3}{Z_3} + \dots + \frac{V_N}{Z_N} \\ &= V_1 Y_1 + V_2 Y_2 + V_3 Y_3 + \dots + V_N Y_N = \sum_{I=1}^N V_I Y_I \end{aligned} \quad \text{----- (1.39)}$$

Impedance  $Z_m$  at the output terminals when all the sources have been removed and output

is open, is given by:  $\frac{1}{Z_m} = \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \dots + \frac{1}{Z_N}$

or 
$$Y_m = Y_1 + Y_2 + Y_3 + \dots + Y_N = \sum_{I=1}^N Y_I$$

or 
$$Z_m = \frac{1}{Y_m} = \frac{1}{\sum_{I=1}^N Y_I} \quad \text{----- (1.40)}$$

The Norton's equivalent of this network is given in figure (1.40b), which may further be converted to its Thevenin's equivalent. The Thevenin's voltage  $V_m$  is given by:

$$V_m = I_m \cdot Z_m = \frac{I_m}{Y_m} = \frac{\sum_{I=1}^N V_I Y_I}{\sum_{I=1}^N Y_I}$$

and  $Z_m$  is given by the equation (1.40). The Thevenin's equivalent will be as shown in figure (1.39 b).

Hence Millman's theorem is proved.

**Example 1.9** Calculate the load current  $I_L$  in the circuit of figure (1.41), using Millman's theorem.

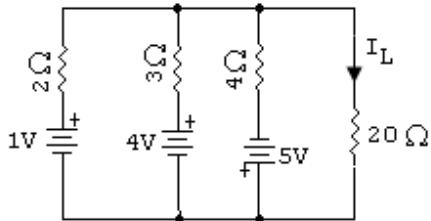


Fig. 1.41

**Solution:** According to Millman's theorem, the given circuit may be represented by a voltage source  $V$  and an impedance  $Z$  in series with it as shown in figure (1.42).

The value of  $V$  is given by:

$$V = \frac{V_1 Y_1 + V_2 Y_2 + V_3 Y_3}{Y_1 + Y_2 + Y_3} = \frac{\frac{1}{2} + \frac{4}{3} - \frac{5}{4}}{\frac{1}{2} + \frac{1}{3} + \frac{1}{4}} = \frac{\frac{6+16-15}{12}}{\frac{6+4+3}{12}} = \frac{7}{13} \text{ volts}$$

$$Z = \frac{1}{Y_1 + Y_2 + Y_3} = \frac{1}{\frac{1}{2} + \frac{1}{3} + \frac{1}{4}} = \frac{1}{\frac{6+4+3}{12}} = \frac{12}{13} \Omega$$

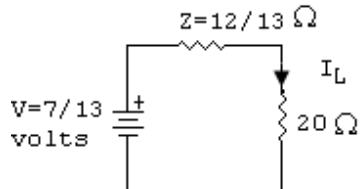


Fig. 1.42

The current  $I_L$  is given by:

$$I_L = \frac{7/13}{(12/13) + 20} = \frac{7}{273} = 25.7 \text{ mA}$$

**1.4.6 Maximum Power Transfer Theorem:** This theorem states that when a voltage source is connected to load impedance, then maximum power will be transferred from the voltage source to the load impedance, if load impedance is equal to the complex conjugate of source impedance.

**Proof:** Let us consider an a.c. voltage source  $V_S$  (having  $Z_S$  as source impedance) is connected to a load impedance  $Z_L$  as shown in figure (1.43).

It is now to be proved that the maximum power will be transferred from source  $V_S$  to load impedance  $Z_S$  if  $Z_L = Z_S^*$  ----- (1.41)

We know  $Z_S = R_S + jX_S$  and  $Z_L = R_L + jX_L$   
where  $R_S$  &  $R_L$  are the resistive parts of  $Z_S$  &  $Z_L$  respectively and  $X_S$  &  $X_L$

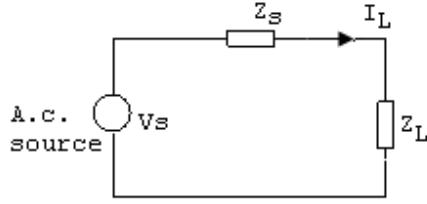


Fig. 1.43

are their corresponding reactive parts.

$$\text{Load current } I_L \text{ is given by: } I_L = \frac{V_s}{(Z_S + Z_L)} = \frac{V_s}{(R_s + R_L) + j(X_s + X_L)} \quad \text{----- (1.42)}$$

$$\text{Voltage across } Z_L \text{ is: } V_L = I_L \cdot Z_L = \frac{V_s \cdot (R_L + jX_L)}{[R_s + R_L] + j(X_s + X_L)]}$$

Power delivered to the load is given by:  $P = \text{Re alPart}(V_L I_L^*)$

$$\begin{aligned} I_L^* &= \frac{V_s}{(R_s + R_L) - j(X_s + X_L)} \\ V_L \cdot I_L^* &= \frac{V_s^2 (R_L + jX_L)}{[(R_s + R_L)^2 + (X_s + X_L)^2]} \\ \text{So } P &= \frac{V_s^2 R_L}{(R_s + R_L)^2 + (X_s + X_L)^2} \end{aligned} \quad \text{----- (1.43)}$$

To find the condition for maximum power delivered to the load, first differentiation of power  $P$  is put equal to zero. Here power varies with load resistance  $R_L$  and also with load reactance  $X_L$ . The variation of power with  $X_L$  (keeping  $R_L$  constant) is first considered.

We find  $\frac{dP}{dX_L}$  and put it equal to zero.

$$\frac{dP}{dX_L} = \frac{-2V_s^2 R_L (X_L + X_s)}{[(R_L + R_s)^2 + (X_L + X_s)^2]^2} = 0 \quad \text{----- (1.44)}$$

This will be equal to zero if  $(X_L + X_s) = 0$  or  $X_L = -X_s$ .

By putting  $X_L = -X_s$  in equation (1.44), we get

$$P = \frac{V_s^2 R_L}{(R_s + R_L)^2} \quad \text{----- (1.45)}$$

Again we consider the variation of power with  $R_L$ , here we find  $\frac{dP}{dR_L}$  and put it equal to

zero as:

$$\frac{dP}{dR_L} = \frac{V_s^2 [(R_s + R_L)^2 - 2R_L(R_s + R_L)]}{(R_s + R_L)^4} = 0$$

or  $\frac{V_s^2 [R_s^2 + R_L^2 + 2R_s R_L - 2R_L^2 - 2R_s R_L]}{(R_s + R_L)^4} = 0$

or  $\frac{V_s^2 [R_s^2 - R_L^2]}{(R_s + R_L)^4} = 0$

The left hand side of this equation will be zero when either  $V_s = 0$  or  $[R_s^2 - R_L^2] = 0$ .  $V_s$  can not be equal to zero as it is a given voltage source. So  $[R_s^2 - R_L^2] = 0$  or  $R_s = R_L$ .

Thus the power delivered to the load will be maximum when the resistive part of the load impedance are equal to the resistive part of the source impedance; also reactance of the load impedance must be equal but opposite in sign to the reactance of the source impedance.

i.e.  $R_L + j X_L = R_s - j X_s$   
or  $Z_L = Z_s^*$

In other words one can say that the maximum power will be delivered to the load impedance, when load impedance is equal to the complex conjugate of source impedance. This was to be proved.

It is further interesting to note that if d.c. source  $V_s$  having source resistance  $R_s$  is considered then the condition for the maximum power will be transferred if  $R_s = R_L$  which may be proved in the similar fashion as discussed above.

The expression for maximum power delivered to the load is given by:

$$P_{\max} = \frac{V_s^2 R_L}{(2R_L)^2} = \frac{V_s^2}{4R_L}$$

This power is also known as available power.

**Example 1.10** Find the value of  $R_L$  for which power delivered to it, is maximum in the figure(1.44). Determine the maximum power.

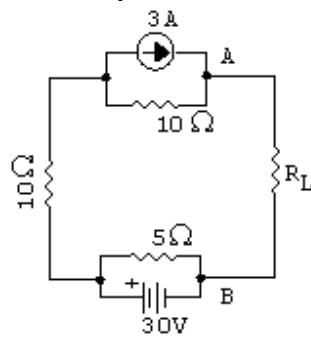


Fig. 1.44

Solution: This circuit is replaced into its Norton's equivalent form. For this find short circuit current by short circuiting the AB terminals as shown in figure (1.45). Short circuit current may be obtained using Superposition theorem.

(i) Consider only current source of 3 A, and 30 V source is shorted, the short circuit current  $I'$  is given by:  $I' = \frac{3A \times 5}{10} = 1.5A$

(ii) Consider only 30V source, and 3A source is open circuited, we get the short circuit current  $I''$  as:  $I'' = \frac{30V}{10+5} = 1.5A$

Net short circuit current  $I_0$  is given by:  $I_0 = I' + I'' = 1.5 + 1.5 = 3A$

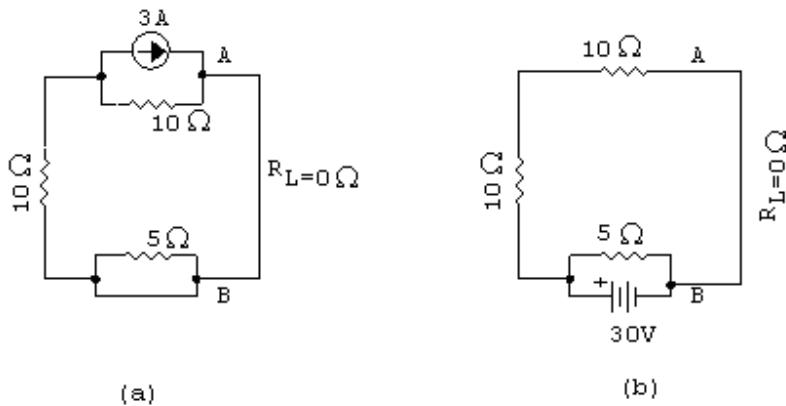


Fig. 1.45

The open circuit resistance  $R_s$  (across AB terminals) is obtained by short circuiting the voltage source and open circuiting the current source as:

$$R_s = 10 + 10 = 20\Omega.$$

The circuit may be replaced in Noton's and Thevenin's equivalent forms as shown in figure (1.46).

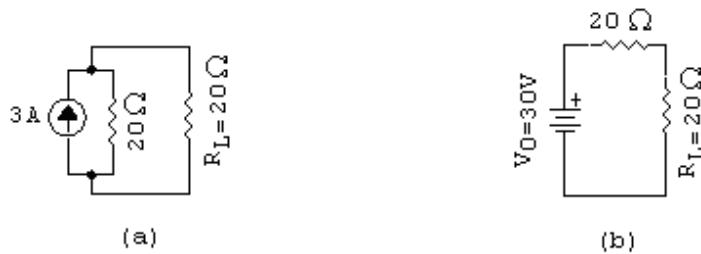


Fig. 1.46

The value of  $R_L$  for maximum power transfer should equal to source resistance  $R_s$ . So  $R_L=20\Omega$  and maximum power  $P_{max} = \frac{V_0^2}{4R_L} = \frac{(60)^2}{4 \times 20} = 45Watt$

**1.4.7 Star – Delta Conversion:** Some times network analysis becomes simple if T – network (ref. figure 1.47 a) is converted to  $\pi$  – network (ref. figure 1.47 b) and vice versa. T – Network may be redrawn as a star network

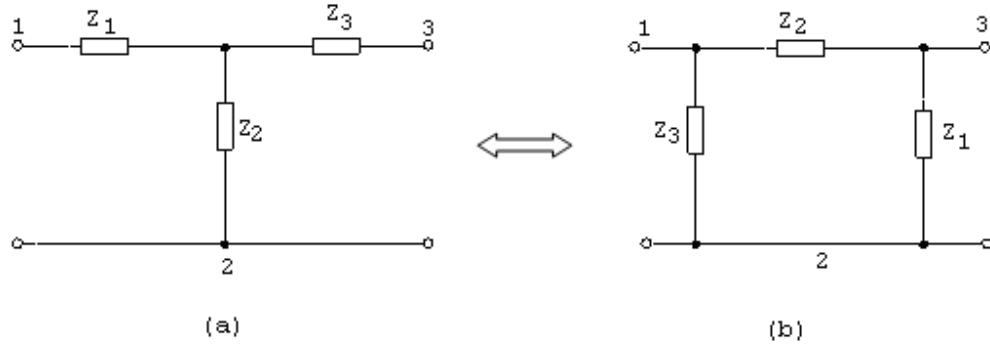


Fig. 1.47

or Y – network and  $\pi$  – network may be redrawn as mesh or delta (i.e.  $\Delta$ ) network as shown in figure (1.48). So this conversion is known as star to delta and vice versa (or T to  $\pi$  and vice versa).

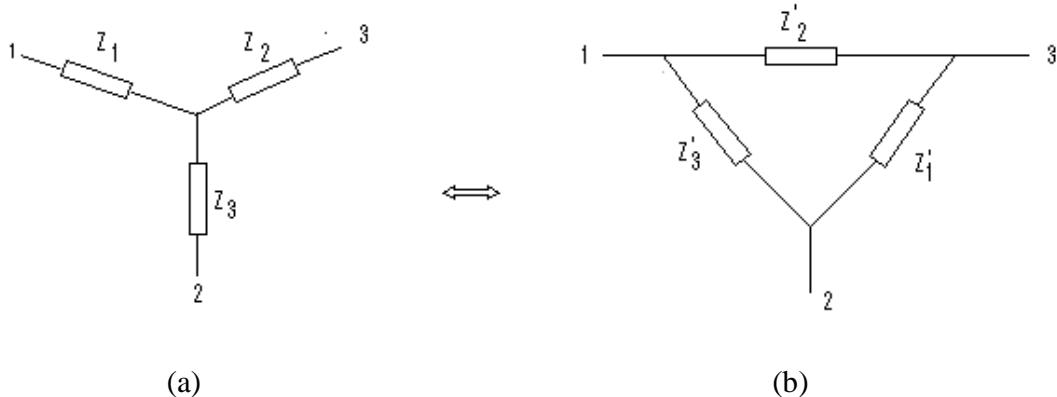


Fig. 1.48

**(i) Delta to Star conversion:** Consider a delta network and a star network shown in figure (1.48). The two networks will said to be equal if the impedance offered between any two points of one network is equal to impedance offered between the corresponding two points of the other network.

Impedance offered between 1 & 2 terminals of star network (fig. 1.48a) is given by:

$$Z_{12} = Z_1 + Z_2$$

Impedance offered between 1 & 3 terminals of star network (fig. 1.48 a) is given by:

$$Z_{13} = Z_1 + Z_3$$

Impedance offered between 2 & 3 terminals of star network (fig. 1.48a) is given by:

$$Z_{23} = Z_2 + Z_3$$

Similarly, Impedance offered between 1 & 2 terminals of delta network (fig. 1.48 b) is given by:  $Z_{12} = Z_3 \parallel (Z_1 + Z_2) = \frac{(Z_1 + Z_2)Z_3}{Z_1 + Z_2 + Z_3}$

Impedance offered between 1 & 3 terminals of delta network (fig. 1.48 b) is given by:  $Z_{13} = Z_2 \parallel (Z_1 + Z_3) = \frac{(Z_1 + Z_3)Z_2}{Z_1 + Z_2 + Z_3}$

Impedance offered between 2 & 3 terminals of delta network (fig. 1.48 b) is given by:  $Z_{23} = Z_1 \parallel (Z_2 + Z_3) = \frac{(Z_2 + Z_3)Z_1}{Z_1 + Z_2 + Z_3}$

The two networks will be equal if the impedance between two points of one network is equal to impedance between the corresponding two points.

$$\text{So } Z_1 + Z_2 = \frac{(Z_1 + Z_2)Z_3}{Z_1 + Z_2 + Z_3} \quad \text{----- (1.46)}$$

$$Z_1 + Z_3 = \frac{(Z_1 + Z_3)Z_2}{Z_1 + Z_2 + Z_3} \quad \text{----- (1.47)}$$

$$Z_2 + Z_3 = \frac{(Z_2 + Z_3)Z_1}{Z_1 + Z_2 + Z_3} \quad \text{----- (1.48)}$$

Adding equations (1.46) & (1.47) and subtracting (1.48) from it we get:

$$2Z_1 = \frac{1}{(Z_1 + Z_2 + Z_3)} [Z_1Z_3 + Z_2Z_3 + Z_1Z_2 + Z_2Z_3 - Z_1Z_2 - Z_1Z_3]$$

$$\text{or } Z_1 = \frac{1}{(Z_1 + Z_2 + Z_3)} [Z_2Z_3] \quad \text{----- (1.49)}$$

Similarly, adding equations (1.46) & (1.48) and subtracting (1.47) from it we get:  $Z_2 = \frac{1}{(Z_1 + Z_2 + Z_3)} [Z_1Z_3]$  ----- (1.50)

Also, adding equations (1.47) & (1.48) and subtracting (1.46) from it, we get:

$$Z_3 = \frac{1}{(Z_1 + Z_2 + Z_3)} [Z_1Z_2] \quad \text{----- (1.51)}$$

These three equations give the values of impedances of star network in terms of the impedances of delta network. The converted star network of the given delta network may be shown by the dotted lines in figure (1.49).

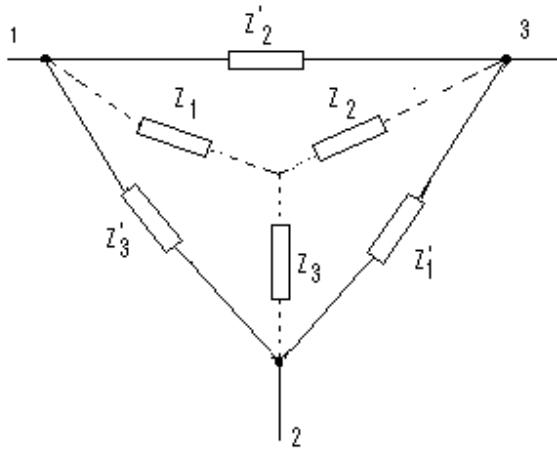


Fig. 1.49

From this figure it is clear that the arms of the star network are obtained by multiplying the impedances of adjacent arms of delta network divided by the sum of all the impedances connected in the delta network.

**(ii) Star to Delta Conversion:** From the equations (1.49) to (1.51) obtained above, we may get impedances of the Delta network in terms of impedances of star network. This can be done by multiplying the three equations as:

$$Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 = \frac{1}{(Z'_1 + Z'_2 + Z'_3)^2} [Z'_1 Z'_2 (Z'_3)^2 + Z'_1 Z'_3 (Z'_2)^2 + Z'_2 Z'_3 (Z'_1)^2]$$

or

$$= \frac{Z'_1 Z'_2 Z'_3}{(Z'_1 + Z'_2 + Z'_3)} \quad \text{----- (1.52)}$$

From equations (1.52) & (1.49) we get :

$$Z'_1 = \frac{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3}{Z_1}$$

Similarly from equations (1.52) & (1.50) we get:

$$Z'_2 = \frac{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3}{Z_2}$$

Also from equations (1.52) & (1.51) we get:

$$Z'_3 = \frac{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3}{Z_3}$$

These three equations give the values of impedances of delta network in terms of the impedances of star network. The converted delta network of the given star network may be shown by the dotted lines in figure (1.50).

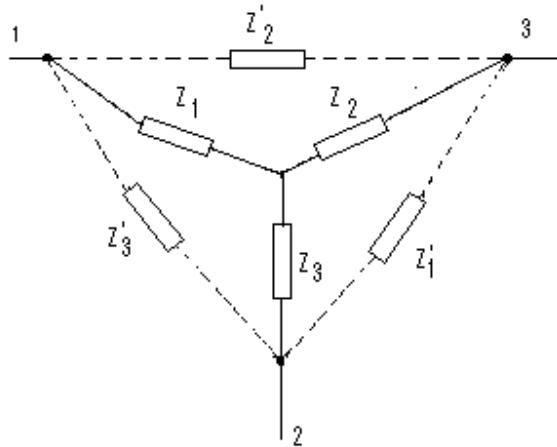


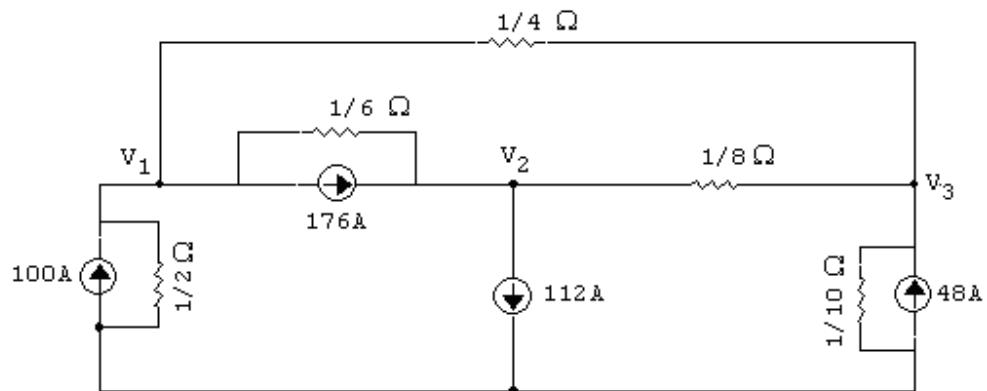
Fig. 1.50

From this figure it is clear that the arms of the delta network are obtained by getting the factor  $\sum Z_1 Z_2$  of the star network divided by the impedance of the opposite arm in the star network.

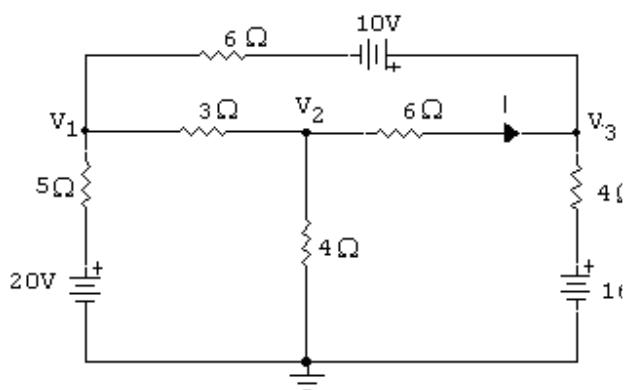
### Problems:

1. State and Explain Kirchoff's laws.
2. Discuss the model for the battery, and show that it is equal to a voltage source and a resistance in series with it. Also explain the terms open circuit voltage and short circuit current.
3. What are ideal voltage source and ideal current source? Prove that for good voltage source the source resistance should be small enough than the load resistance, whereas for good current source the source resistance should be larger than load resistance.
4. Discuss in detail, Node method of network analysis by taking a suitable network.
5. Discuss in detail, Loop method of network analysis by taking a suitable network.
6. State and prove Superposition Theorem.
7. State and prove Thevenin's Theorem.
8. State and prove Norton's Theorem.
9. State and prove Reciprocity Theorem.
10. State and prove Millman's Theorem.
11. Discuss the condition for maximum power transfer from an a.c. source to load impedance.
12. Define and compare Thevenin's & Norton's Theorem.
13. Show that a d.c. source having a source resistance connected to load resistance delivers maximum power to the load resistance when source resistance is equal to load resistance. Also find the expression for maximum power.
14. Show that the maximum power will be delivered from an a.c. source to the load impedance when load impedance is equal to the complex conjugate of source impedance.

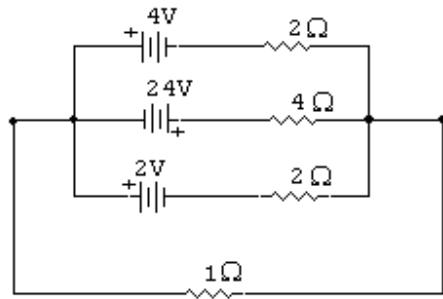
15. How a delta network is converted to star network and vice versa?
16. Explain  $\pi - T$  transformation of network.
17. Explain  $T - \pi$  transformation of network.
18. A battery has an open circuit voltage of 12 volts and its source resistance as  $3\Omega$ . Represent the battery by means of two equivalent circuit elements. Show that these two equivalent circuits draw same amount of current in the load resistance of  $9\Omega$  connected to the terminals of the battery.
19. Two equal resistances (each of  $1M\Omega$ ) in series are connected to the terminals of 75volts source. A multimeter having a sensitivity of  $20K\Omega/\text{volts}$  is used to measure the voltage across one of the series resistance of  $1M\Omega$ . The range of the voltmeter used is 50volts. What will be the reading of the voltmeter?  
(Ans. 25volts)
20. Solve for the node voltages of the circuit given below.  
(Ans.  $V_1 = -2V, V_2 = 6V, V_3 = 4V$ )



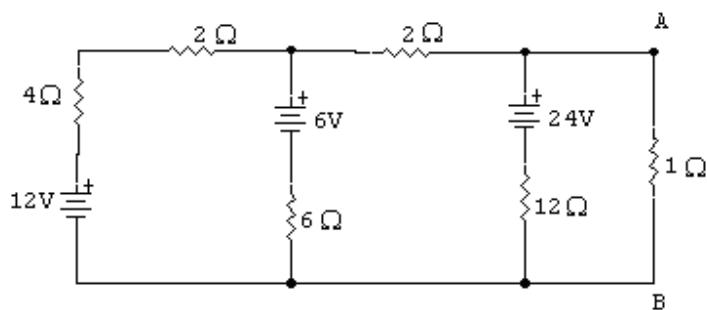
21. Using the node method find the value of current I flowing through  $6\Omega$  resistance in the circuit given below.



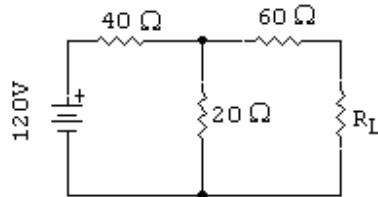
22. Using Millman's theorem, find the value of current flowing through  $1\Omega$  resistance in the given circuit.  
(Ans. 1.33 A)



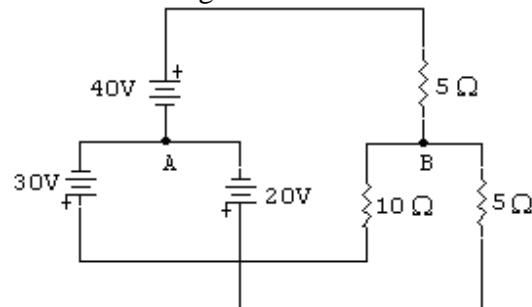
23. Using Norton's theorem, compute current through  $1\Omega$  resistance in the given circuit. (Ans. 2.8 A)



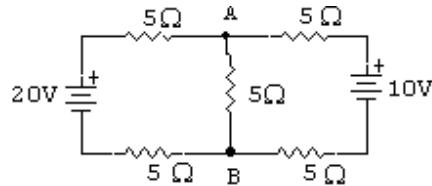
24. In the circuit shown below, find the current flowing through the load resistance  $R_L$  of  $10\Omega$ . For what value of  $R_L$ , the power delivered to the load is maximum? Also compute the maximum power. (Ans. 0.48A,  $73.3\Omega$ , 5.45watt)



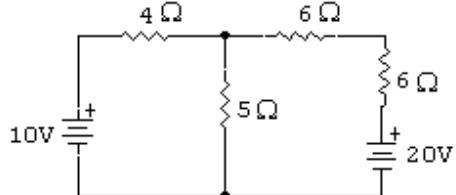
25. Using Millman's theorem find the current through a resistance of  $25\Omega$  connected between A & B points in the circuit given below. (Ans. 1A)



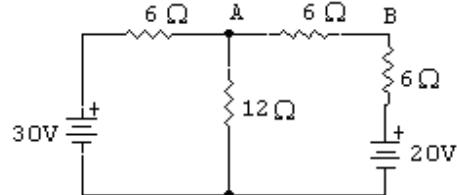
26. Apply Superposition theorem to find the voltage across AB branch in the given circuit. Verify the result using Loop method also. (Ans. 10 volts)



27. Verify the Reciprocity theorem in the circuit shown below.

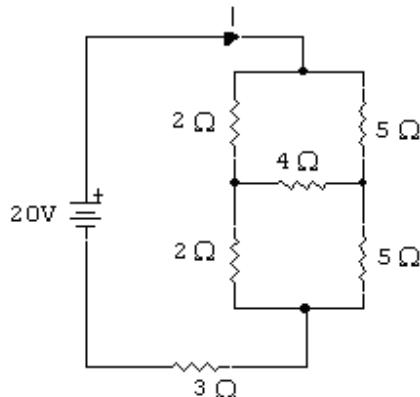


28. Using Superposition theorem, calculate the current through  $6\Omega$  resistance in the AB branch in the circuit shown in the figure. (Ans. 7/8A from A to B)

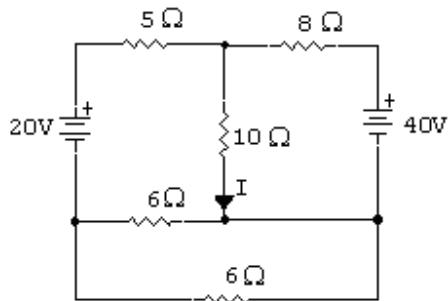


29. Consider the circuit shown below. Determine total impedance of the circuit, current  $I$  flowing through the circuit, power delivered by the source.

(Ans.  $5.86\Omega$ ,  $3.41A$ ,  $68.1Watt$ )

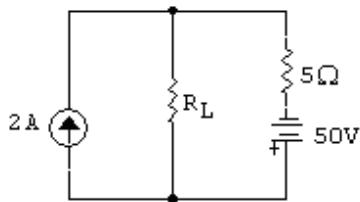


30. Using Superposition theorem find the current  $I$  flowing through  $10\Omega$  resistance in the given circuit. (Ans. 2.14A)



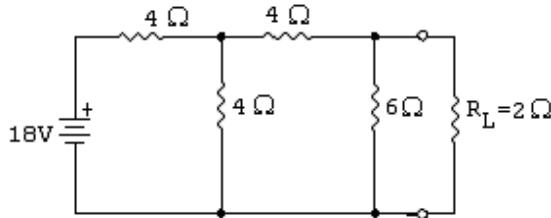
31. Find the value of  $R_L$  for which power delivered to it, is maximum as in the figure given below. Determine the maximum power.

(Ans.  $R_L=5\Omega$ ,  $P_{max}=80\text{Watt}$ )



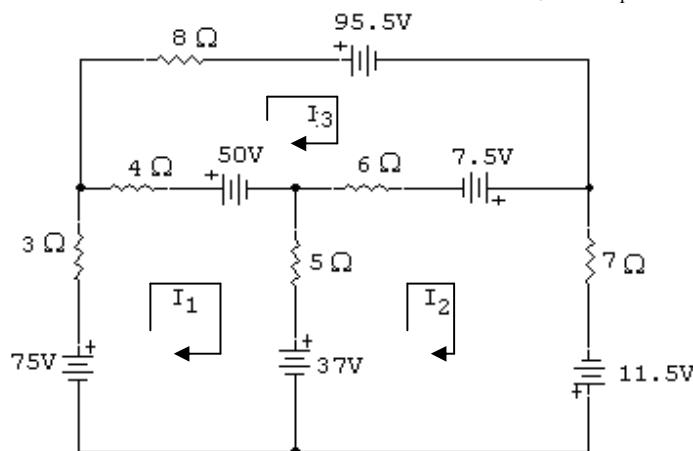
32. Find the current flowing through  $R_L$  in the network given below, using Thevenin's theorem.

(Ans.  $9/5\text{A}$ )



33. Find the loop currents in the circuit given below.

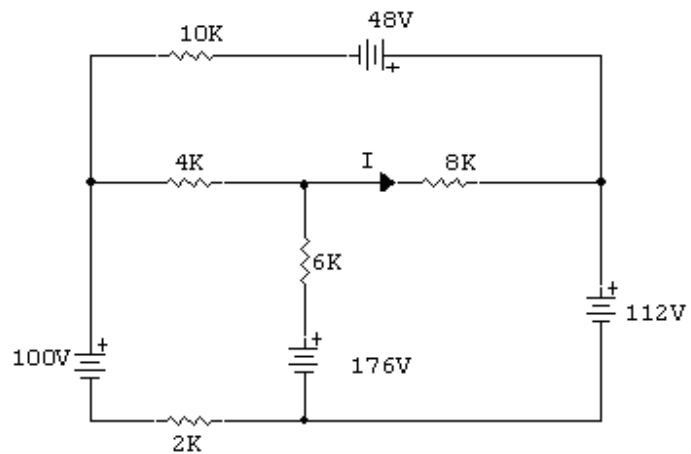
(Ans.  $I_1 = -1\text{A}, I_2 = 2\text{A}, I_3 = -5\text{A}$ )



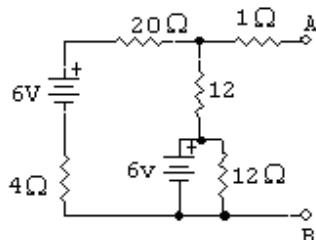
34. In problem 33, if the values of the voltage sources are doubled than show that the loop currents are also doubled.

35. Find the current  $I$  flowing through  $8\text{K}\Omega$  resistance in the circuit shown in the figure. Use loop method to solve the problem.

(Ans.  $2\text{mA}$ )

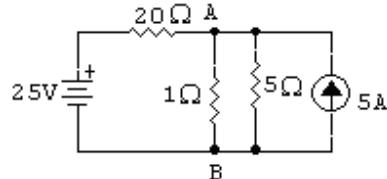


36. Obtain Thevenin's equivalent of the network shown in the figure.

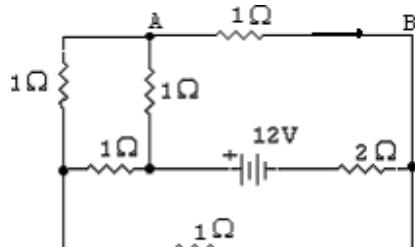


(Ans.  $V_0 = 6\text{V}$ ,  $R_0 = 9\Omega$ )

37. Define Norton's theorem and calculate the current flowing through  $1\Omega$  resistance connected between AB terminals of the circuit shown below. (Ans. 5A)



38. Find the current I in AB branch of the circuit shown below.



(Ans. 2A)

# 2

## Two – Port Network

A network contains active and passive elements connected in the form of a circuit. Usually, a network has one pair of terminals for Input and other pair for the output. A pair of Input terminals of the network is called as Input port and the pair of the output terminals is called as the output port. Such a network is called as two port network. If the elements in the network are linear, the network is known as linear two port network. To understand the characteristics or to analyse a linear two port network, consider a black box as shown in figure 2.1. The 1, 1 terminals of the black box is known as input port and 2, 2 terminals is known as output port.

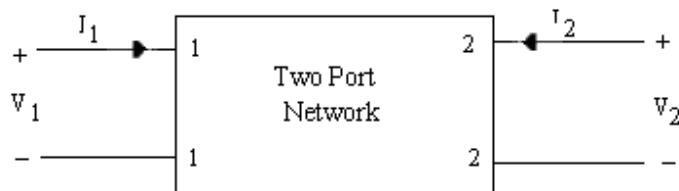


Fig. 2.1

In this network  $V_1, I_1$  are the Input voltage and current; and  $V_2, I_2$  are the output voltage and current. Any pair of variables may be arbitrarily chosen as independent variables, and other variables (dependent variables) may be obtained as a function of independent variables that is dependents variables may assumed to be the functions of independent variables.

**2.1 Impedance Parameters:** A linear two port network represented by black box is considered, having  $I_1$  and  $I_2$  as independent variables and  $V_1$  and  $V_2$  as dependent variables.

$$V_1 = f_1(I_1, I_2)$$

$$V_2 = f_2(I_1, I_2)$$

----- (2.1)

The changes in the dependent variables may be given by:

$$\begin{aligned} dV_1 &= \frac{\partial V_1}{\partial I_1} dI_1 + \frac{\partial V_1}{\partial I_2} dI_2 \\ dV_2 &= \frac{\partial V_2}{\partial I_1} dI_1 + \frac{\partial V_2}{\partial I_2} dI_2 \end{aligned} \quad (2.2)$$

The partial derivatives in these equations become constant with operation over linear region of the device curve with constant slope.

The equations may, therefore, be written as:

$$\begin{aligned} V_1 &= Z_{11} I_1 + Z_{12} I_2 \\ V_2 &= Z_{21} I_1 + Z_{22} I_2 \end{aligned} \quad (2.3)$$

In the matrix form it is given by:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (2.4)$$

Where Z's are the impedance (resistance for d. c.) parameters, which may be defined as:

$$Z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0}, \text{ is the input impedance when output is open}$$

circuited or open- circuit input impedance.

$$Z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0}, \text{ is the reverse transfer impedance when}$$

input is open circuited or open circuit reverse transfer impedance.

$$Z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0}, \text{ is the forward transfer impedance when}$$

output is open circuited or open circuit forward transfer impedance.

$$\text{and } Z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0}, \text{ is the output impedance when input is open}$$

circuited or open circuit output impedance.

These Z parameters also known as open circuit parameters, since in these parameters either input or output is open circuited. The equivalent circuit of the network using Z- parameters may be drawn as given below:

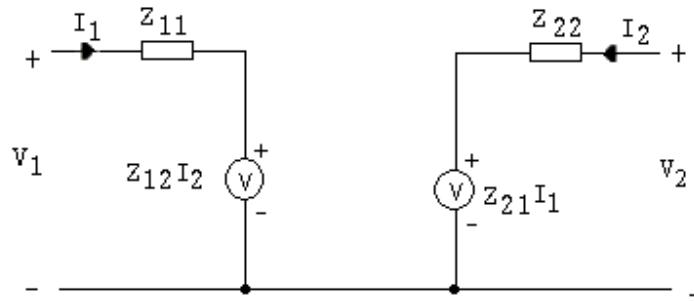


Fig. 2.2

**2.2 Admittance Parameters:** The admittance parameters of a linear two port network may also be defined in the similar fashion as the impedance parameters discussed above. In the admittance parameters, variables  $V_1$  &  $V_2$  are assumed independent variables and  $I_1$  &  $I_2$  as the dependent variables. The dependent variables  $I_1$  &  $I_2$  may be defined as a linear function of Independent variables  $V_1$  &  $V_2$  as

$$\begin{aligned} I_1 &= f_1(V_1, V_2) \\ I_2 &= f_2(V_1, V_2) \end{aligned} \quad \text{----- (2.5)}$$

and

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2 \quad \text{----- (2.6)}$$

In the matrix form it is given by :

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad \text{----- (2.7)}$$

Where  $Y$ 's are the admittance (conductance for d. c.) parameters, which may be defined as :

$$Y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0}, \text{ is the input admittance when output is short circuited or short- circuit input admittance.}$$

$$Y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0}, \text{ is the reverse transfer admittance when input is short circuited or short circuit reverse transfer admittance.}$$

$$Y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0}, \text{ is the forward transfer admittance when output is short circuited or short circuit forward transfer admittance.}$$

and  $Y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0}$ , is the output admittance when input is short circuited or short circuit output admittance.

These  $Y$  – parameters are also called as short circuit parameters as given in the network either input or output is shorted. The equivalent circuit of the network using  $Y$ - parameters is given in figure 2.3.

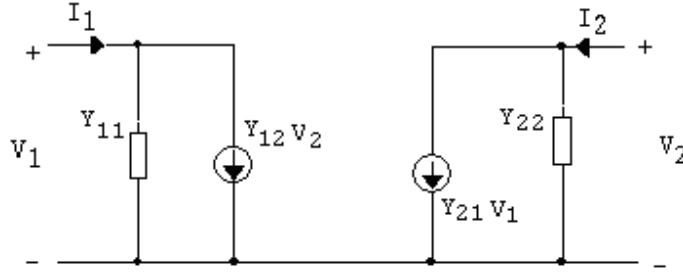


Fig. 2.3

**2.3 Hybrid Parameters:** Hybrid parameters may be defined by using  $I_1$  &  $V_2$  as Independent variables and  $V_1$  &  $I_2$  as dependent variables. The equations are given:

$$\begin{aligned} V_1 &= H_{11} I_1 + H_{12} V_2 \\ I_2 &= H_{21} I_1 + H_{22} V_2 \end{aligned} \quad \text{----- (2.8)}$$

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \quad \text{----- (2.9)}$$

where  $H_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0}$ , is known as input impedance when output is shorted, or short circuit input impedance.

$H_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0}$ , is known as reverse transfer voltage ratio when input is open circuited or open circuit reverse transfer voltage ratio.

$H_{21} = \left. \frac{I_2}{I_1} \right|_{V_2=0}$ , is the forward transfer current ratio when input is open circuited or open circuit forward transfer current ratio.

$H_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0}$ , is the output admittance when input is open circuited or open circuit output admittance.

The  $H$ - parameters are known as hybrid parameters as these parameters have the mixed dimensions. The equivalent circuit of the network is given in figure 2.4.

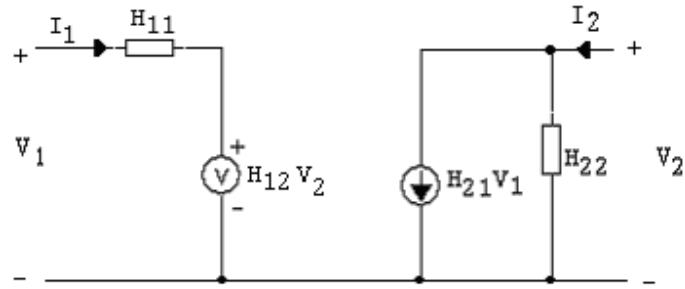


Fig. 2.4

**2.4 Inverse hybrid or  $H'$  Parameters:** In these parameters,  $V_1$  &  $I_2$  are assumed as independent variables and  $I_1$ ,  $V_2$  as dependent variables. The dependent equations may be given by:

$$\begin{aligned} I_1 &= H_{11}' V_1 + H_{12}' I_2 \\ V_2 &= H_{21}' V_1 + H_{22}' I_2 \end{aligned} \quad \text{----- (2.10)}$$

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} H_{11}' & H_{12}' \\ H_{21}' & H_{22}' \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} \quad \text{----- (2.11)}$$

where  $H_{11}' = \left. \frac{I_1}{V_1} \right|_{I_2=0}$ , is the open circuit input admittance.

$H_{12}' = \left. \frac{I_1}{I_2} \right|_{V_1=0}$ , is the short circuit reverse transfer current ratio.

$H_{21}' = \left. \frac{V_2}{V_1} \right|_{I_2=0}$ , is the open circuit forward transfer voltage ratio.

$H_{22}' = \left. \frac{V_2}{I_2} \right|_{V_1=0}$ , is the short circuit output impedance.

The equivalent circuit of the network using  $H'$ -parameters are given in figure 2.5.

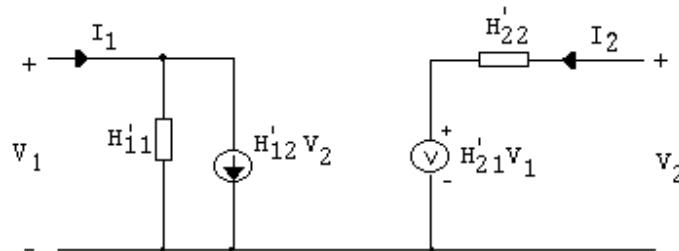


Fig. (2.5)

**2.5 Transmission parameters:** The Transmission Parameters are obtained by considering the variables of Input port as dependent variables and variables of output port as Independent variables, as given below:

$$V_1 = AV_2 - BI_2 \quad \text{----- (2.12)}$$

$$I_1 = CV_2 - DI_2 \quad \text{----- (2.12)}$$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad \text{----- (2.13)}$$

It is customary to choose  $-I_2$  in place of  $I_2$  as these parameters are used to find the overall parameters of a cascaded two port network. Transmission parameters are also called  $T$  or  $A, B, C, D$ , parameters.

where  $A = \left. \frac{V_1}{V_2} \right|_{I_2=0}$ , is open circuit reverse transfer voltage ratio.

$B = \left. \frac{V_1}{-I_2} \right|_{V_2=0}$ , is short circuit reverse transfer impedance.

$C = \left. \frac{I_1}{V_2} \right|_{I_2=0}$ , is open circuit reverse transfer admittance.

$D = \left. \frac{I_1}{-I_2} \right|_{V_2=0}$ , is short circuit reverse transfer current ratio.

**2.6 Inverse Transmission or  $T'$ -Parameters:** Inverse Transmission or  $T'$ -parameters may be defined by using  $V_1$  &  $-I_1$  as Independent variables and  $V_2$  &  $I_2$  as dependent variables. The equations are given as:

$$V_2 = A'V_1 - B'I_1 \quad \text{----- (2.14)}$$

$$I_2 = C'V_1 - D'I_1$$

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} \begin{bmatrix} V_1 \\ -I_1 \end{bmatrix} \quad \text{----- (2.15)}$$

where  $A' = \left. \frac{V_2}{V_1} \right|_{I_1=0}$ , is open circuit forward transfer voltage ratio.

$B' = \left. \frac{V_2}{-I_1} \right|_{V_1=0}$ , is short circuit forward transfer impedance.

$$C' = \left. \frac{I_2}{V_1} \right|_{I_1=0}, \text{ is open circuit forward transfer admittance.}$$

$$D' = \left. \frac{I_2}{-I_1} \right|_{V_1=0}, \text{ is short circuit forward transfer current ratio.}$$

**Example 2.1** Find Z and H Parameters of the Passive T-Network given in figure (2.6).

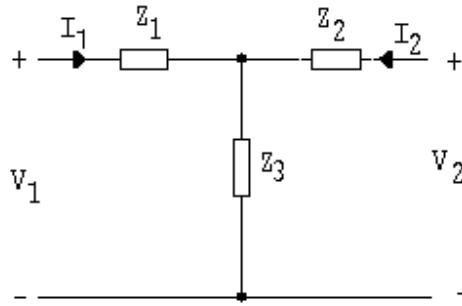


Fig. (2.6)

Solution: 1. Z - Parameters

$$(i) Z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0} \text{ Since } I_2=0 \text{ (output is open circuited),}$$

so  $V_I = I_I(Z_I + Z_3)$

$$\text{or } Z_{11} = \frac{V_1}{I_1} = Z_1 + Z_3$$

$$(ii) Z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0} \text{ Since } I_1=0, \text{ the voltage across } Z_3 \text{ will be equal to } V_I$$

So  $V_I = Z_3 I_2$

or  $Z_{12} = \frac{V_1}{I_2} = Z_3$

$$(iii) Z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0} \text{ To find } Z_{21}, \text{ output port is open circuited } (I_2 = 0), \text{ the voltage}$$

across  $Z_3$  will be equal to  $V_2$  which is given by

$$V_2 = Z_3 I_I$$

or  $Z_{21} = \frac{V_2}{I_1} = Z_3$

$$(iv) \quad Z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0} \quad Z_{22} \text{ is obtained by open circuiting the input port .}$$

$$\text{So } V_2 = I_2 (Z_2 + Z_3)$$

$$Z_{22} = \frac{V_2}{I_2} = Z_2 + Z_3$$

2. H-Parameters:

$$(i) \quad H_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0} \quad \text{By short circuiting the output port, the network becomes as}$$

shown in the fig. (2.7)

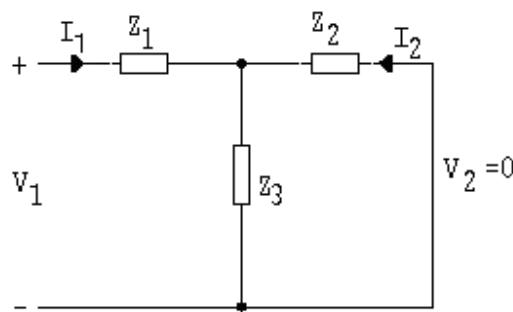


Fig. 2.7

$$\text{So } V_1 = I_1 [Z_1 + Z_2 \| Z_3 ]$$

$$H_{11} = \frac{V_1}{I_1} = \frac{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3}{Z_2 + Z_3}$$

$$(ii) \quad H_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0} \quad \text{Since } I_1 = 0, \text{ so the voltage across } Z_3 \text{ will be equal to voltage}$$

at the input port.

The equations are :

$$V_1 = Z_3 I_2 \quad \text{and} \quad V_2 = I_2 (Z_2 + Z_3)$$

$$\text{So } H_{12} = \frac{V_1}{V_2} = \frac{Z_3}{Z_2 + Z_3}$$

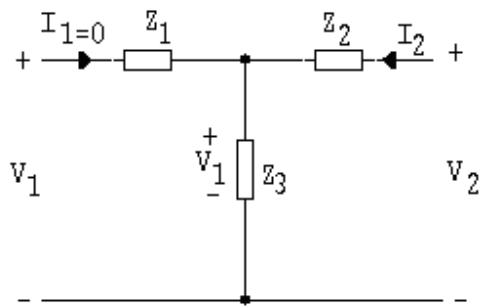


Fig. (2.8)

$$(iii) H_{21} = \left. \frac{I_2}{I_1} \right|_{V_2=0}$$

The corresponding diagram is shown below:

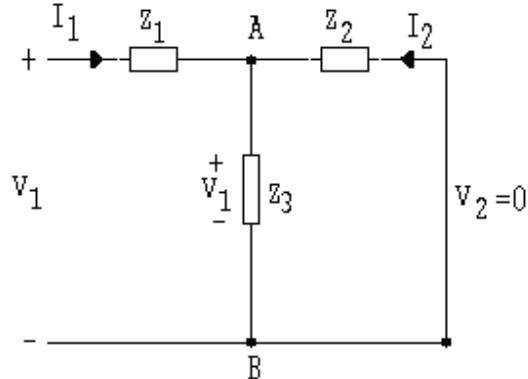


Fig.2.9

Voltage across  $AB$  points is  $V_{AB} = I_1 [Z_2 \parallel Z_3] = \frac{Z_2 Z_3}{Z_2 + Z_3} I_1$

$$I_2 = -\frac{V_{AB}}{Z_2} = -\frac{Z_3 I_1}{(Z_2 + Z_3)}$$

or  $H_{21} = \frac{I_2}{I_1} = -\frac{Z_3}{(Z_2 + Z_3)}$

$$(iv) H_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0}$$

Since  $I_1=0$  (Ref. Fig.2.8)

So  $V_2 = I_2 (Z_2 + Z_3)$

or  $H_{22} = \frac{I_2}{V_2} = \frac{1}{Z_2 + Z_3}$

**Example. 2.2** Find  $H'$  parameters of the given  $\Pi$  - network.

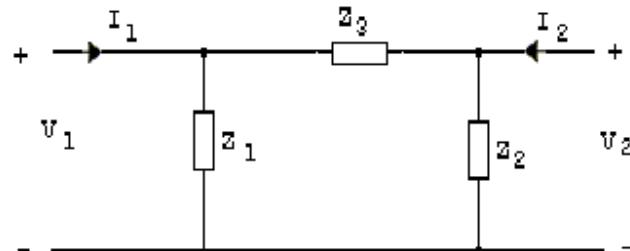


Fig. 2.10

Solution: (i)  $H'_{11} = \left. \frac{I_1}{V_1} \right|_{I_2=0}$

The relation between  $V_1$  and  $I_1$  when  $I_2 = 0$ , is given by:

$$V_1 = I_1 [Z_1 \parallel (Z_2 + Z_3)]$$

or  $V_1 = I_1 \left[ \frac{Z_1(Z_2 + Z_3)}{Z_1 + Z_2 + Z_3} \right]$

or  $H_{11} = \frac{I_1}{V_1} = \frac{Z_1 + Z_2 + Z_3}{Z_1 Z_2 + Z_1 Z_3}$

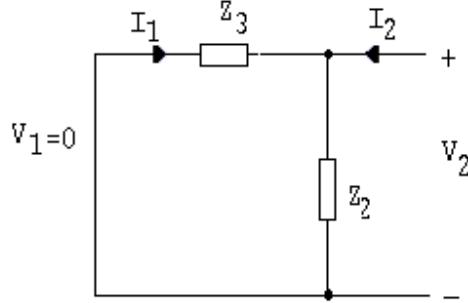


Fig. 2.11

(ii)  $H_{12} = \frac{I_1}{I_2} \Big|_{V_2=0}$

$$V_2 = I_2 \left( \frac{Z_2 Z_3}{Z_2 + Z_3} \right) \text{ and } I_1 = -\frac{V_2}{Z_3}$$

Combining these two equations, we get

$$I_1 = -\frac{Z_2}{(Z_2 + Z_3)} I_2 \quad \text{or} \quad H_{12} = \frac{I_1}{I_2} = -\frac{Z_2}{Z_2 + Z_3}$$

(iii)  $H_{21} = \frac{V_2}{V_1} \Big|_{I_2=0}$  When  $I_2 = 0$ , the relation between  $V_1$  and  $V_2$  is

given by:

$$V_2 = \frac{V_1}{(Z_2 + Z_3)} Z_2 \quad \text{or} \quad H_{21} = \frac{V_2}{V_1} = \frac{Z_2}{(Z_2 + Z_3)}$$

(iv)  $H_{22} = \frac{V_2}{I_2} \Big|_{V_1=0}$  The relation between  $V_2$  &  $I_2$  when  $V_1 = 0$  is given

by (Ref. Fig. 2.11).

$$V_2 = I_2 \frac{Z_2 Z_3}{Z_2 + Z_3} \quad \text{or} \quad H_{22} = \frac{V_2}{I_2} = \frac{Z_2 Z_3}{Z_2 + Z_3}$$

**Example 2.3** Find the transmission Parameters of the network given in figure 2.12. The network is excited by a sinusoidal signal of  $10^4$  radians /sec.

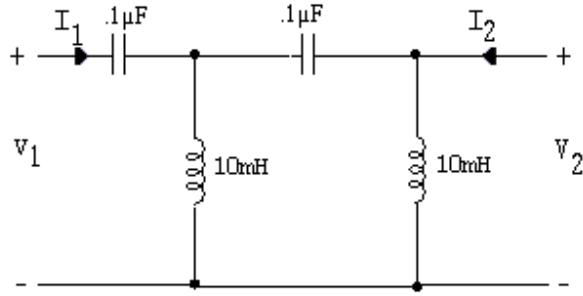


Fig 2.12

Solution: Since the network is excited by a sinusoidal signal of frequency  $10^4$  radians / sec, the inductive reactance of  $10 \text{ mH}$  inductance is

$$\omega L = 10^4 \times 10 \times 10^3 = 100 \Omega$$

and capacitive reactance of  $.1\mu\text{F}$  capacitance is

$$\frac{1}{\omega C} = \frac{1}{10^4 \times 1 \times 10^{-6}} = 100 \Omega$$

So the network is replaced by the Impedance of  $100 \Omega$  each as given in the figure 2.13

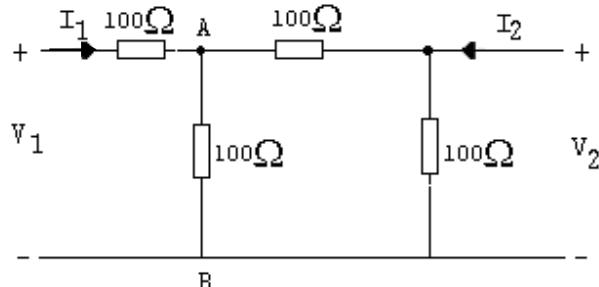


Fig. 2.13

The transmission parameters of this network may be obtained as follows:

$$(i) \quad A = \left. \frac{V_1}{V_2} \right|_{I_2=0} \quad \text{From the Fig.(2.13) voltage across } AB \text{ terminals is given}$$

$$\text{as} \quad V_{AB} = I_1 (100 \parallel 200) = I_1 \left( \frac{200}{3} \right)$$

$$\text{and} \quad V_2 = \frac{V_{AB} \times 100}{(100 + 100)} = \frac{V_{AB}}{2}$$

$$\text{or} \quad V_2 = I_1 \left( \frac{100}{3} \right) \quad \dots\dots (2.16)$$

$$\text{also from fig.2.13} \quad V_1 = I_1 [100 + 100 \parallel 200] = I_1 \left[ 100 + \frac{200}{3} \right]$$

$$\text{or} \quad V_1 = I_1 \left( \frac{500}{3} \right) \quad \dots\dots (2.17)$$

From equations (2.16) & (2.17) we get  $V_1 = 5V_2$

$$\text{or } A = \frac{V_2}{V_1} = 5$$

$$(ii) \quad B = \left. \frac{V_1}{-I_2} \right|_{V_2=0} \quad \text{By short circuiting the output terminals we have the}$$

network as:

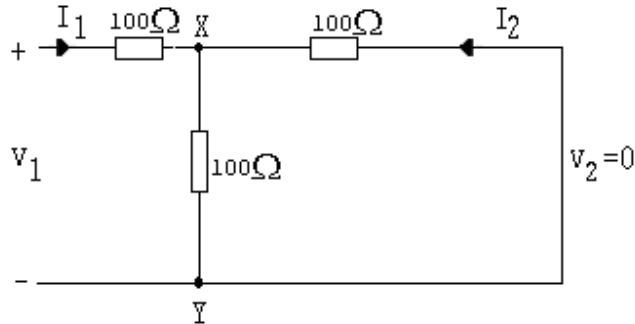


Fig. 2.14

The output current  $I_2$  is given by:  $-I_2 = \frac{V_{xy}}{100}$  and

$$V_{xy} = I_1(100 \parallel 100) = I_1(50) \text{ or } -I_2 = \frac{I_1}{2}$$

$$\text{However } V_1 = I_1[100 + 50] = 150 I_1$$

$$V_1 = -150 \times 2 I_2 = -300 I_2$$

$$B = \frac{V_1}{-I_2} = 300 \Omega$$

$$(iii) \quad C = \left. \frac{I_1}{V_2} \right|_{I_2=0} \quad \text{The relation between } I_1 \text{ & } V_2 \text{ when } I_2 = 0 \text{ is given in}$$

the calculation of  $A$  parameter as  $V_2 = I_1 \frac{100}{3}$

$$\text{so } C = \frac{I_1}{V_2} = \frac{3}{100} \text{ mhos}$$

$$(iv) \quad D = \left. \frac{I_1}{-I_2} \right|_{V_2=0} \quad \text{The relation between } I_1 \text{ & } I_2 \text{ for } V_2 = 0 \text{ is given in the}$$

calculation of  $B$  parameters of the network shown above as:

$$I_2 = -\frac{I_1}{2} \quad \text{or} \quad D = \frac{I_1}{-I_2} = 2$$

**2.7 Transformation of Parameters:** For a given linear two port network sometimes one type of parameters is calculated, by considering the suitable independent as well as dependent variables. But for many reasons, other type of parameters also required; which may be calculated

by using the transformation of parameters. The transformation of parameters is just a mathematical transformation, which may be understood by considering an example.

Suppose the Z-parameters of a linear two port network are given and these are to be transformed into its equivalent Y-parameters.

The Z parameters of a linear two port network are given by the equations:

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \quad \dots \quad (2.18)$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \quad \dots \quad (2.19)$$

The required equations for Y-parameters are

$$I_1 = Y_{11} V_1 + Y_{12} V_2 \quad \dots \quad (2.20)$$

$$I_2 = Y_{21} V_1 + Y_{22} V_2 \quad \dots \quad (2.21)$$

The equations (2.18) and (2.19) may be rewritten as

$$I_1 = \frac{1}{Z_{11}} V_1 - \frac{Z_{12}}{Z_{11}} I_2 \quad \dots \quad (2.22)$$

$$I_2 = \frac{1}{Z_{22}} V_2 - \frac{Z_{21}}{Z_{22}} I_1 \quad \dots \quad (2.23)$$

From equations (2.22) and (2.23) we get

$$\begin{aligned} I_1 &= \frac{1}{Z_{11}} V_1 - \frac{Z_{12}}{Z_{11}} \left( \frac{1}{Z_{22}} V_2 - \frac{Z_{21}}{Z_{22}} I_1 \right) \\ I_1 \left( \frac{Z_{11} Z_{22} - Z_{12} Z_{21}}{Z_{11} Z_{22}} \right) &= \frac{1}{Z_{11}} V_1 - \frac{Z_{12}}{Z_{22} Z_{11}} V_2 \end{aligned}$$

$$\text{or } I_1 = \frac{Z_{22}}{(Z_{11} Z_{22} - Z_{12} Z_{21})} V_1 - \frac{Z_{12}}{Z_{11} Z_{22} - Z_{12} Z_{21}} V_2 \quad \dots \quad (2.24)$$

$$I_2 = \frac{1}{Z_{22}} V_2 - \frac{Z_{21}}{Z_{22}} \left( \frac{1}{Z_{11}} V_1 - \frac{Z_{12}}{Z_{11}} I_1 \right)$$

$$I_2 \left( \frac{Z_{11} Z_{22} - Z_{12} Z_{21}}{Z_{11} Z_{22}} \right) = \frac{1}{Z_{22}} V_2 - \frac{Z_{21}}{Z_{11} Z_{22}} V_1$$

$$\text{or } I_2 = -\frac{Z_{21}}{(Z_{11} Z_{22} - Z_{12} Z_{21})} V_1 + \frac{Z_{11}}{Z_{11} Z_{22} - Z_{12} Z_{21}} V_2 \quad \dots \quad (2.25)$$

Comparing the coefficients of  $V_1$  and  $V_2$  in equations (2.24) and (2.25) with (2.20) and (2.21) respectively we get

$$\begin{aligned} Y_{11} &= \frac{Z_{22}}{Z_{11} Z_{22} - Z_{12} Z_{21}} & Y_{12} &= \frac{Z_{12}}{Z_{11} Z_{22} - Z_{12} Z_{21}} \\ Y_{21} &= \frac{-Z_{21}}{Z_{11} Z_{22} - Z_{12} Z_{21}} & Y_{22} &= \frac{Z_{11}}{Z_{11} Z_{22} - Z_{12} Z_{21}} \end{aligned} \quad \dots \quad (2.26)$$

These are the required parameters in terms of the given Z-parameters.

The transformation of different parameters is shown in the form of a Table given below.

Table 2.1 Transformation of parameters:

	Z	Y	H	$H'$	T	$T'$
[Z]	$Z_{11} \quad Z_{12}$	$\frac{Y_{22}}{\Delta Y} \quad \frac{-Y_{12}}{\Delta Y}$	$\frac{\Delta H}{H_{22}} \quad \frac{H_{12}}{H_{22}}$	$\frac{1}{H_{11}} \quad \frac{-H_{12}}{H_{11}}$	$\frac{A}{C} \quad \frac{\Delta T}{C}$	$\frac{D}{C} \quad \frac{1}{C}$
	$Z_{21} \quad Z_{22}$	$\frac{-Y_{21}}{\Delta Y} \quad \frac{Y_{11}}{\Delta Y}$	$\frac{-H_{21}}{H_{22}} \quad \frac{1}{H_{22}}$	$\frac{H_{21}}{H_{11}} \quad \frac{\Delta H}{H_{11}}$	$\frac{1}{C} \quad \frac{D}{C}$	$\frac{\Delta T}{C} \quad \frac{A}{C}$
[Y]	$\frac{Z_{22}}{\Delta Z} \quad \frac{-Z_{12}}{\Delta Z}$	$Y_{11} \quad Y_{12}$	$\frac{1}{H_{11}} \quad \frac{-H_{12}}{H_{11}}$	$\frac{\Delta H}{H_{22}} \quad \frac{H_{12}}{H_{22}}$	$\frac{D}{B} \quad \frac{-\Delta T}{B}$	$\frac{A}{B} \quad \frac{-1}{B}$
	$\frac{-Z_{21}}{\Delta Z} \quad \frac{Z_{11}}{\Delta Z}$	$Y_{21} \quad Y_{22}$	$\frac{H_{21}}{H_{11}} \quad \frac{\Delta H}{H_{11}}$	$\frac{-H_{21}}{H_{22}} \quad \frac{1}{H_{22}}$	$-\frac{1}{B} \quad \frac{A}{B}$	$\frac{-\Delta T}{B} \quad \frac{D}{B}$
[H]	$\frac{\Delta Z}{Z_{22}} \quad \frac{Z_{12}}{Z_{22}}$	$\frac{1}{Y_{11}} \quad \frac{-Y_{12}}{Y_{11}}$	$H_{11} \quad H_{12}$	$\frac{H_{22}}{\Delta H} \quad \frac{-H_{12}}{\Delta H}$	$\frac{B}{D} \quad \frac{\Delta T}{D}$	$\frac{B}{A} \quad \frac{1}{A}$
	$\frac{-Z_{21}}{Z_{22}} \quad \frac{1}{Z_{22}}$	$\frac{Y_{21}}{Y_{11}} \quad \frac{\Delta Y}{Y_{11}}$	$H_{21} \quad H_{22}$	$\frac{-H_{21}}{\Delta H} \quad \frac{H_{11}}{\Delta H}$	$-\frac{1}{D} \quad \frac{C}{D}$	$\frac{-\Delta T}{A} \quad \frac{C}{A}$
[H']	$\frac{1}{Z_{11}} \quad \frac{-Z_{12}}{Z_{11}}$	$\frac{\Delta Y}{Y_{22}} \quad \frac{Y_{12}}{Y_{22}}$	$\frac{H_{22}}{\Delta H} \quad \frac{-H_{12}}{\Delta H}$	$H'_{11} \quad H'_{12}$	$\frac{C}{A} \quad \frac{-\Delta T}{A}$	$\frac{C}{D} \quad \frac{-1}{D}$
	$\frac{Z_{21}}{Z_{11}} \quad \frac{\Delta Z}{Z_{11}}$	$\frac{-Y_{21}}{Y_{22}} \quad \frac{1}{Y_{22}}$	$\frac{-H_{21}}{\Delta H} \quad \frac{H_{11}}{\Delta H}$	$H'_{21} \quad H'_{22}$	$\frac{1}{A} \quad \frac{B}{A}$	$\frac{\Delta T}{D} \quad \frac{B}{D}$
[T]	$\frac{Z_{11}}{Z_{21}} \quad \frac{\Delta Z}{Z_{21}}$	$\frac{-Y_{22}}{Y_{21}} \quad \frac{-1}{Y_{21}}$	$\frac{-\Delta H}{H_{21}} \quad \frac{-H_{11}}{H_{21}}$	$\frac{1}{H'_{21}} \quad \frac{H'_{22}}{H'_{21}}$	$A \quad B$	$\frac{D}{\Delta T} \quad \frac{B}{\Delta T}$
	$\frac{1}{Z_{21}} \quad \frac{Z_{22}}{Z_{21}}$	$\frac{-\Delta Y}{Y_{21}} \quad \frac{-Y_{11}}{Y_{21}}$	$\frac{-H_{22}}{H_{21}} \quad \frac{-1}{H_{21}}$	$\frac{H'_{11}}{H'_{21}} \quad \frac{\Delta H}{H'_{21}}$	$C \quad D$	$\frac{C}{\Delta T} \quad \frac{A}{\Delta T}$
$[T']$	$\frac{Z_{22}}{Z_{12}} \quad \frac{\Delta Z}{Z_{12}}$	$\frac{-Y_{11}}{Y_{12}} \quad \frac{-1}{Y_{12}}$	$\frac{1}{H_{12}} \quad \frac{H_{11}}{H_{12}}$	$\frac{-\Delta H}{H_{12}} \quad \frac{-H_{22}}{H_{12}}$	$\frac{D}{\Delta T} \quad \frac{B}{\Delta T}$	$A' \quad B'$
	$\frac{1}{Z_{12}} \quad \frac{Z_{11}}{Z_{12}}$	$\frac{-\Delta Y}{Y_{12}} \quad \frac{-Y_{22}}{Y_{12}}$	$\frac{H_{22}}{H_{12}} \quad \frac{\Delta H}{H_{12}}$	$\frac{-H'_{11}}{H'_{12}} \quad \frac{-1}{H'_{12}}$	$\frac{C}{\Delta T} \quad \frac{A}{\Delta T}$	$C' \quad D'$

Where

$$\Delta Z = Z_{11}Z_{22} - Z_{12}Z_{21}$$

$$\Delta H = H_{11}H_{22} - H_{12}H_{21}$$

$$\Delta T = AD - BC$$

$$\Delta Y = Y_{11}Y_{22} - Y_{12}Y_{21}$$

$$\Delta H' = H'_{11}H'_{22} - H'_{12}H'_{21}$$

$$\Delta T' = A'D' - B'C'$$

**Example 2.4** Determine the Z-parameters of the symmetric lattice network given in Fig. (2.15) and then transform them to Y-parameters.

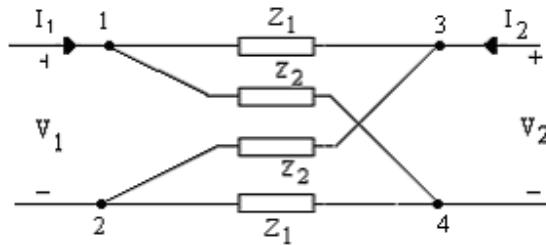


Fig. 2.15

Solution:

**Z-Parameters:** The network shown in figure is symmetric lattice since all the terminals of the network are connected to  $Z_1$  &  $Z_2$  impedances. For simplicity the network may be redrawn as shown in fig. (2.16).

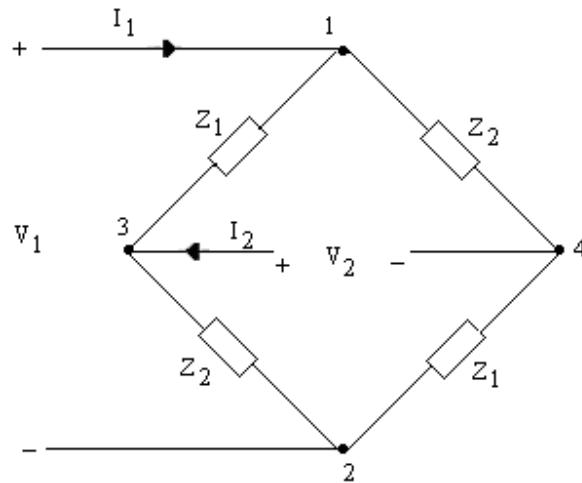


Fig. 2.16

The Z-parameters may be calculated as follows:

$$Z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0} \quad \text{Since } I_2 = 0, \text{ the current } I_1 \text{ is equally distributed in the } 1, 3, 2 \& 1, 4, 2 \text{ branch. i.e. } I_1/2 \text{ current will flow in both the two branches.}$$

$$\text{So } V_1 = \frac{I_1}{2}(Z_1 + Z_2) \quad \text{or} \quad Z_{11} = \frac{V_1}{I_1} = \frac{Z_1 + Z_2}{2}$$

$$Z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0}$$

Similarly  $Z_{22}$  may be calculated by keeping  $I_1 = 0$ , so the current  $I_2$  will be equally distributed in 3, 1, 4 and 3, 2, 4 branches.

Therefore  $V_2 = \frac{I_2}{2}(Z_1 + Z_2)$  or  $Z_{22} = \frac{V_2}{I_2} = \frac{Z_1 + Z_2}{2}$

$$Z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0} \quad \text{In this case the distribution of current will be as shown in fig.}$$

(2.17).

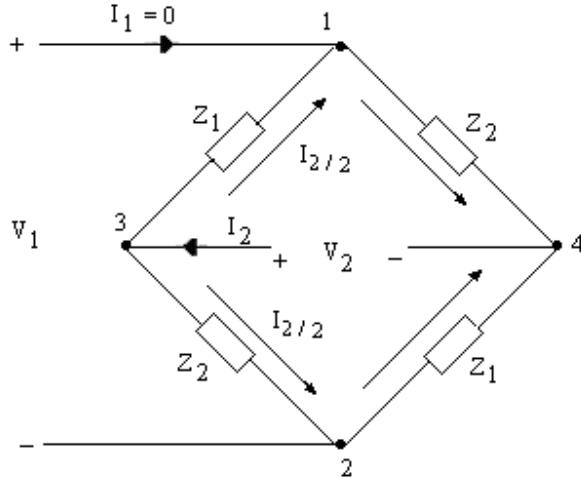


Fig. 2.17

Voltage  $V_I$ , which is the algebraic sum of voltages across  $Z_1$  &  $Z_2$ , is given by:

$$V_I = -\frac{I_2}{2}Z_1 + \frac{I_2}{2}Z_2 \quad \text{or} \quad Z_{12} = \frac{V_I}{I_2} = \frac{Z_2 - Z_1}{2}$$

$$Z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0} \quad \text{which may in the similar fashion be obtained as:}$$

$$V_2 = -\frac{I_1}{2}Z_1 + \frac{I_1}{2}Z_2 \quad \text{or} \quad Z_{21} = \frac{V_2}{I_1} = \frac{Z_2 - Z_1}{2}$$

**Y-parameters:** We have calculated Z-parameters of the symmetric lattice network, which may be transformed in to Y-parameters. From the table 2.1 Y -parameters in terms of Z- parameters are given by:

$$Y_{11} = \frac{Z_{22}}{\Delta Z}, \quad Y_{22} = \frac{Z_{11}}{\Delta Z}, \quad Y_{12} = -\frac{Z_{12}}{\Delta Z} \quad \text{and} \quad Y_{21} = -\frac{Z_{21}}{\Delta Z}$$

Where  $\Delta Z = Z_{11}Z_{22} - Z_{12}Z_{21}$  putting the values of Z-parameters as calculated above we get  $\Delta Z = (\frac{Z_1 + Z_2}{2})^2 - (\frac{Z_2 - Z_1}{2})^2 = \frac{1}{4}[Z_1^2 + Z_2^2 + 2Z_1Z_2 - Z_2^2 - Z_1^2 - Z_1Z_2] = Z_1Z_2$

$$\text{So } Y_{11} = \frac{Z_{22}}{\Delta Z} = \frac{(Z_1 + Z_2)/2}{Z_1Z_2} = \frac{Z_1 + Z_2}{2Z_1Z_2} = Y_{22} \quad \text{since } Z_{11}=Z_{22}$$

$$Y_{12} = -\frac{Z_{12}}{\Delta Z} = -\frac{(Z_2 - Z_1)/2}{Z_1 Z_2} = \frac{Z_1 - Z_2}{2Z_1 Z_2} = Y_{21} \quad \text{since } Z_{12}=Z_{21}$$

**Example 2.5** The Z-parameters of a linear two port network are  $Z_{11} = 40 \Omega$ ,  $Z_{12} = Z_{21} = 20 \Omega$  and  $Z_{22} = 30 \Omega$ . Compute the transmission parameters of the network.

Solution: The network equation using Z-parameters are given by:

$$V_1 = 40 I_1 + 20 I_2 \quad \text{----- (2.27)}$$

$$V_2 = 20 I_1 + 30 I_2 \quad \text{----- (2.28)}$$

The T-parameter equations are given by:

$$V_1 = AV_2 - BI_2 \quad \text{----- (2.29)}$$

$$I_1 = CV_2 - DI_2 \quad \text{----- (2.30)}$$

The equations (2.27) & (2.28) may be converted in the form of equations (2.29) & (2.30) respectively.

$$V_1 = \frac{40(V_2 - 30I_2)}{20} + 20I_2$$

$$\text{or} \quad V_1 = 2V_2 - 40I_2 \quad \text{----- (2.31)}$$

$$\text{and} \quad I_1 = \frac{V_2}{20} - \frac{3}{2}I_2 \quad \text{----- (2.32)}$$

Comparing eqs. (2.31) & (2.32) with eqs. (2.29) & (2.30) respectively, the required parameters are given as:

$$A = 2 \quad B = 40 \Omega \quad C = 1/20 \text{ mhos} \quad D = 3/2$$

**2.8 Interconnection of Two Port Networks:** Figure (2.18) shows the two networks  $P_1$  and  $P_2$  whose voltage and current variables are given. These two networks may be connected in a number of ways so that the resulting network is also a two port network. The overall parameters of such a two port network may be calculated in different ways.

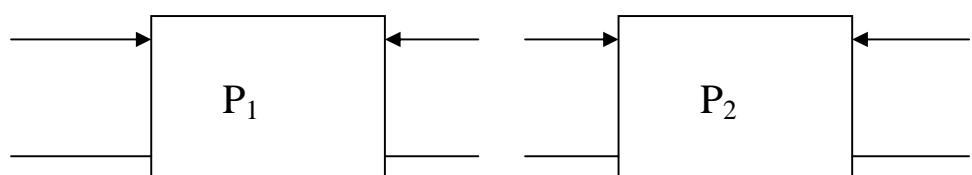


Fig.2.18

**(i) Cascade connection of two networks:** The two networks are said to be connected in cascaded mode, if the output of one network is connected to the Input of other network as shown in the figure (2.19). The overall parameters of the network may be obtained as follows:

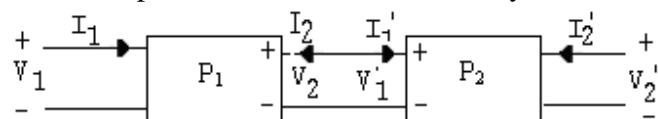


Fig. 2.19

The T-parameter equations of the two networks  $P_1$  and  $P_2$  are given by:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad \dots \quad (2.33)$$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad \dots \quad (2.33)$$

Since  $V_2 = V_1'$  and  $I_2 = -I_1'$  so the matrix equation (2.33) may be rewritten as:

$$\begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_1' \\ -I_1' \end{bmatrix} \quad \dots \quad (2.34)$$

From equations (2.33) and (2.34) we get the overall parameters of the cascaded networks:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad \dots \quad (2.35)$$

From this equation it is clear that the overall  $[T]$  parameters of the cascaded parameters are obtained by matrix multiplication of the  $T$ -parameters of the individual networks i.e.

$$[T] = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix}$$

**(ii) Parallel Connection:** - Let us connect the two networks  $P_1$  &  $P_2$  in parallel as shown in the fig. (2.20). The  $Y$ -parameters of the network  $P_1$  &  $P_2$  are given by the equations:

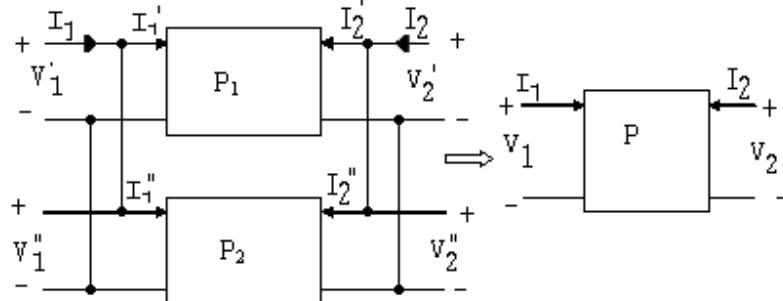


Fig. 2.20

$$I_1' = Y_{11}'V_1' + Y_{12}'V_2' \quad \& \quad I_2' = Y_{21}'V_1' + Y_{22}'V_2' \quad \text{for } P_1 \quad \dots \quad (2.36)$$

$$I_1'' = Y_{11}''V_1'' + Y_{12}''V_2'' \quad \& \quad I_2'' = Y_{21}''V_1'' + Y_{22}''V_2'' \quad \text{for } P_2 \quad \dots \quad (2.37)$$

Since inputs of two network are connected in parallel,

$$\text{so } V_1' = V_1'' = V_1 \text{ (say)} \quad I_1' + I_1'' = I_1 \text{ (say)}$$

$$\text{also } V_2' = V_2'' = V_2 \text{ (say)} \quad I_2' + I_2'' = I_2 \text{ (say)}$$

Combining equations (2.36) & (2.37) we get:

$$I_1 = I_1' + I_1'' = (Y_{11}' + Y_{11}'')V_1 + (Y_{12}' + Y_{12}'')V_2 \quad \dots \quad (2.38)$$

$$I_2 = I_2' + I_2'' = (Y_{21}' + Y_{21}'')V_1 + (Y_{22}' + Y_{22}'')V_2 \quad \dots \quad (2.39)$$

So overall  $Y$ -parameters of the two networks connected in parallel may be obtained by adding the  $Y$ -parameters of the individual network i.e.

$$Y_{11} = Y'_{11} + Y''_{11} \quad Y_{12} = Y'_{12} + Y''_{12}$$

$$Y_{21} = Y'_{21} + Y''_{21} \quad Y_{22} = Y'_{22} + Y''_{22}$$

**(iii) Series connection:** In series connection of two port networks, the inputs and outputs of the two different two port networks are connected as shown in fig.(2.21)

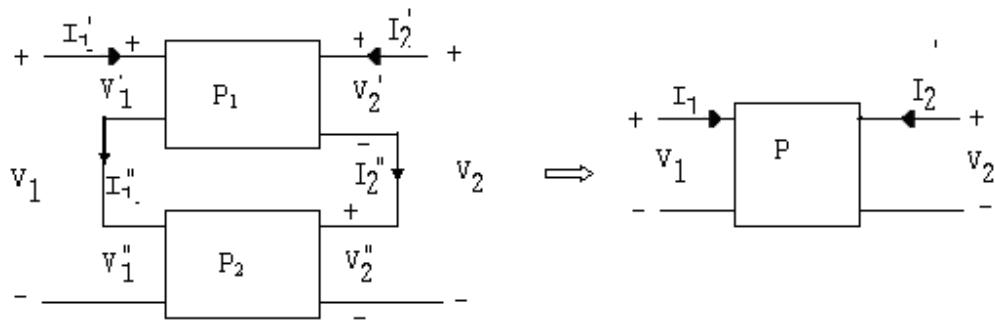


Fig. 2.21

From this figure, we have following relations from the series connection of two port networks ( $P_1$  &  $P_2$ )

$$V_1 = V'_1 + V''_1 \quad I_1 = I'_1 = I''_1 \quad \dots \quad (2.40)$$

$$V_2 = V'_2 + V''_2 \quad I_2 = I'_2 = I''_2 \quad \dots \quad (2.41)$$

By doing similar calculations, as is in parallel combination discussed above; it can very easily be proved that  $Z$ -parameters of the series combination of two networks are equal to the sum of corresponding  $z$ -parameters of individual networks i.e.

$$Z_{11} = Z'_{11} + Z''_{11} \quad Z_{12} = Z'_{12} + Z''_{12}$$

$$Z_{21} = Z'_{21} + Z''_{21} \quad Z_{22} = Z'_{22} + Z''_{22}$$

**Example 2.6** Find  $Y$ -parameters of the twin T-network of the given figure (2.22). Plot  $Y_{12}$  as a function of frequency.

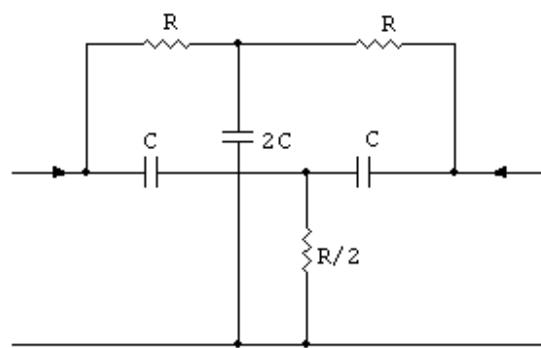


Fig. 2.22

Solution: The given twin T- network is the parallel combination of the two individual T-networks, which is clear from the given circuit shown the fig. (2.23).

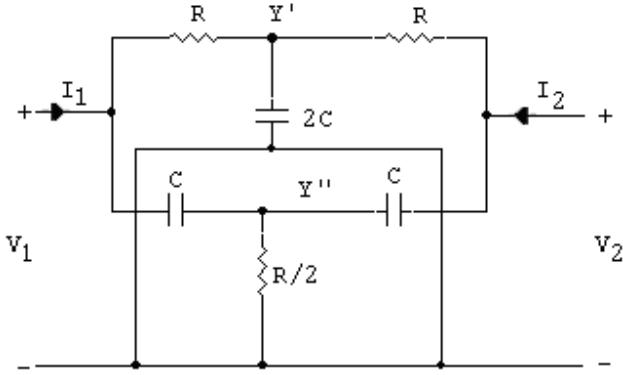


Fig. 2.23

The Y-parameters of this T- network may be given by:

$$Y_{11} = Y'_1 + Y''_1 \quad Y_{12} = Y'_1 + Y''_2$$

$$Y_{21} = Y'_2 + Y''_1 \quad Y_{22} = Y'_2 + Y''_2$$

Y-parameters of the upper T- network may easily be obtained and are given by:

$$Y'_1 = Y''_1 = \frac{R + \frac{i}{2j\omega C}}{\left[ R^2 + \frac{R}{2j\omega C} + \frac{R}{2j\omega C} \right]} = \frac{(1 + 2j\omega CR)}{2R(1 + j\omega CR)}$$

$$Y'_2 = Y''_2 = -\frac{\frac{1}{2j\omega C}}{\frac{1}{2j\omega C} [2R + 2j\omega CR^2]} = -\frac{1}{2R(1 + j\omega CR)}$$

Y-parameters of the lower T- network are given by:

$$Y''_1 = Y''_2 = \frac{\left[ \frac{R}{2} + \frac{1}{j\omega C} \right]}{\left[ -\frac{1}{\omega^2 C^2} + \frac{R}{2j\omega C} + \frac{R}{j\omega C} \right]} = \frac{(2 + j\omega CR)j\omega C}{2(1 + j\omega CR)}$$

$$Y''_1 = Y''_2 = \frac{-\frac{R}{2}}{\frac{2(1 + j\omega CR)}{2j^2\omega^2 C^2}} = \frac{\omega^2 C^2 R^2}{2R(1 + j\omega CR)}$$

The required Y- parameters of the given Twin T- network are given by:

$$\begin{aligned}
 Y_{11} = Y_{22} &= Y_{11}' + Y_{11}'' = \frac{(1+2j\omega CR)}{2R(1+j\omega CR)} + \frac{(2+j\omega CR)j\omega C}{2(1+j\omega CR)} \\
 &= \frac{1+2j\omega CR + 2j\omega CR - \omega^2 C^2 R^2}{2R(1+j\omega CR)} \\
 &= \frac{(1-\omega^2 C^2 R^2) + 4j\omega CR}{2R(1+j\omega CR)} \\
 Y_{12} = Y_{21} &= Y_{12}' + Y_{21}'' = -\frac{1}{2R(1+j\omega CR)} + \frac{\omega^2 C^2 R^2}{2R(1+j\omega CR)} \\
 &= \frac{\omega^2 C^2 R^2 - 1}{2R(1+j\omega CR)}
 \end{aligned}$$

If a graph is plotted between  $Y_{12}$  as a function of frequency ( $\omega$ ), we get a curve as shown in fig.2.24. The following inference is obtained from this curve.

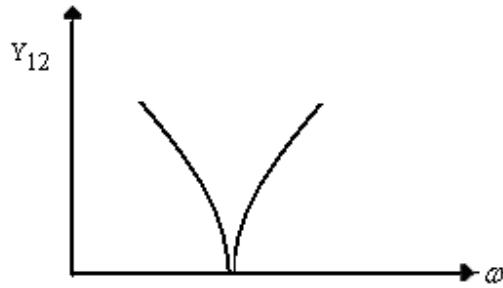


Fig. 2.24

At  $\omega^2 C^2 R^2 = 1$  or  $\omega = \frac{1}{RC}$

$$Y_{12} = 0$$

$Y_{12}$  decreases with  $\omega$  till  $\omega^2 C^2 R^2 < 1$ , but increased with  $\omega$  when  $\omega^2 C^2 R^2 > 1$ . So we may say that the twin T- network behaves like a band pass filter.

**Example 2.7** Find Z- parameters of the given Bridged T- network. Draw also its equivalent circuit.

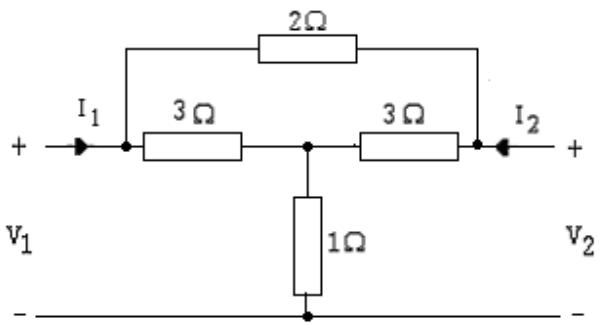


Fig. 2.25

**Solution:** It is a bridged T- network since a resistance ( $2 \Omega$ ) is connected between the Input and Output ports. This network may be redrawn as shown (Fig. 2.26):

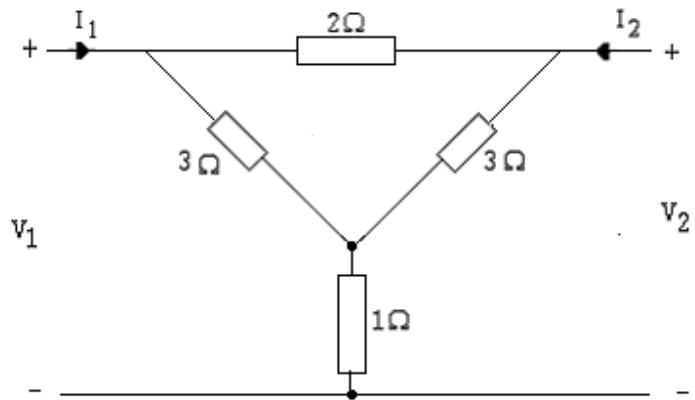


Fig. 2.26

It is clearly seen that this network contains the Delta network, which may converted to its equivalent star network as.

$$R_A = \frac{2 \times 3}{2 + 3 + 3} = \frac{6}{8} = \frac{3}{4} \Omega ; \quad R_B = \frac{3}{4} \Omega ; \quad R_C = \frac{3 \times 3}{8} = \frac{9}{8} \Omega$$

This circuit may further be redrawn as shown in fig. (2.27):

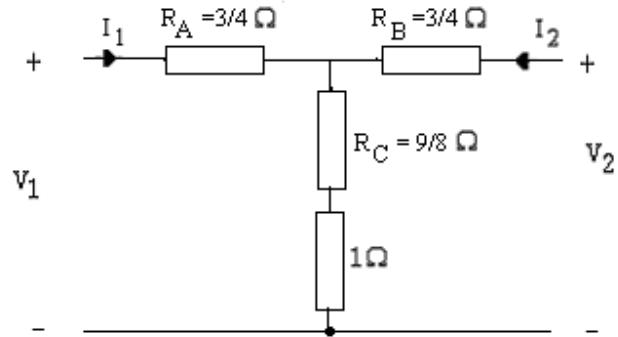


Fig. 2.27

The circuit of figure 2.27 may also be reduced as shown in figure 2.28, Z- parameters of this T- network are calculated as:

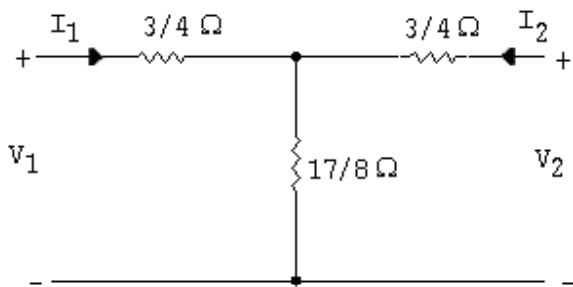


Fig. 2.28

$$Z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0} \quad \text{i.e.} \quad V_1 = I_1 \left( \frac{3}{4} + \frac{17}{8} \right) \quad \text{or} \quad Z_{11} = \frac{V_1}{I_1} = \frac{23}{8} \Omega$$

$$Z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0} \quad \text{i.e.} \quad V_1 = I_2 \left( \frac{17}{8} \right), \quad \text{or} \quad Z_{12} = \frac{V_1}{I_2} = \frac{17}{8} \Omega$$

$$Z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0} \quad \text{i.e.} \quad V_2 = I_1 \left( \frac{17}{8} \right), \quad \text{or} \quad Z_{21} = \frac{V_2}{I_1} = \frac{17}{8} \Omega$$

$$Z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0} \quad \text{i.e.} \quad V_2 = I_2 \left( \frac{3}{4} + \frac{17}{8} \right), \quad \text{or} \quad Z_{22} = \frac{V_2}{I_2} = \frac{23}{8} \Omega$$

From the calculated Z-parameters of the given network, the network equations are given as:  $V_1 = \frac{23}{8}I_1 + \frac{17}{8}I_2$  &  $V_2 = \frac{17}{8}I_1 + \frac{23}{8}I_2$

The equivalent circuit of the given network is (fig. 2.29):

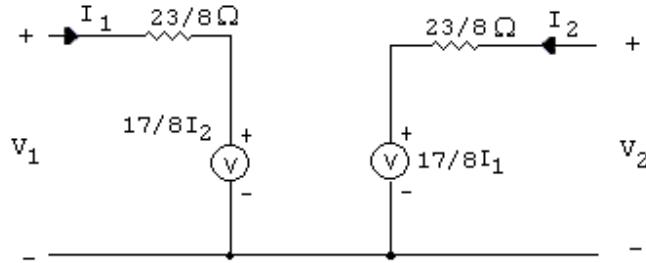


Fig. 2.29

**Example 2.8** Find the Z-parameters of the given circuit. All resistance values are in ohms.

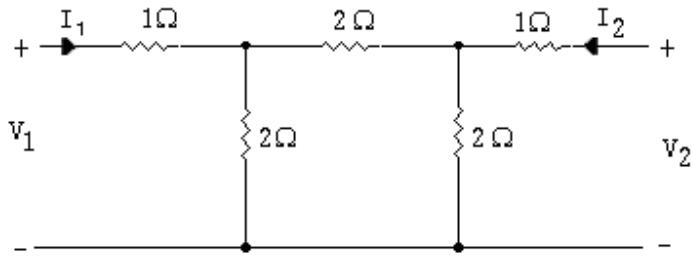


Fig. 2.30

**Solution:** The given circuit may be redrawn as:

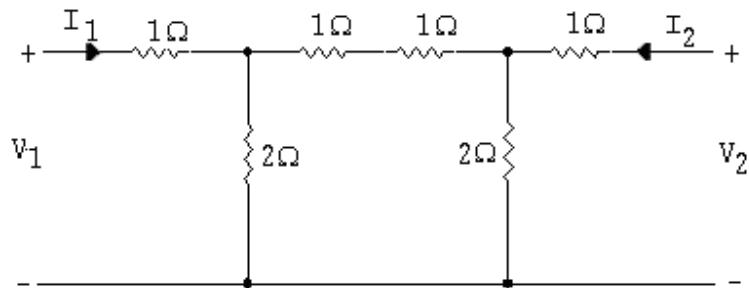


Fig. 2.31

This circuit is a cascaded network of the two T- networks. So we first find the T-parameters of the two networks individually and after matrix multiplication of these T-parameters, the overall T- parameters of the cascaded network are obtained.

The two networks are identical, so we calculate T- parameters of one network (Fig. 2.32 ) as follows:

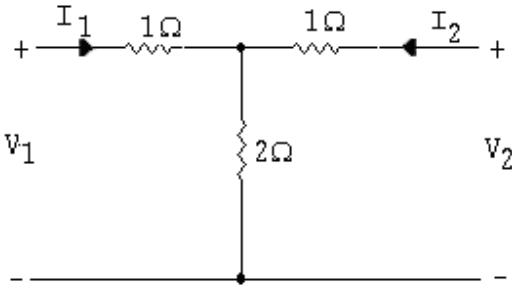


Fig. 2.32

$$A = \left. \frac{V_1}{V_2} \right|_{I_2=0} \quad \text{From the fig.2.32} \quad V_2 = I_1 \cdot 2 \quad \text{and} \quad V_1 = (2 + 1)I_1$$

$$\text{so} \quad A = \frac{V_1}{V_2} = \frac{3}{2}$$

$$B = \left. \frac{V_1}{-I_2} \right|_{V_1=0} \quad \text{From the fig.2.32} \quad V_1 = I_1 \cdot (1 + \frac{1 \times 2}{3}) = \frac{5}{2}I_1$$

$$\text{and} \quad -I_2 = \frac{2}{3}I_1$$

$$\text{so} \quad B = \frac{V_1}{-I_2} = \frac{5}{2} \Omega$$

$$C = \left. \frac{I_1}{V_2} \right|_{I_2=0} \quad \text{From the fig.2.32} \quad V_2 = I_1 \cdot 2 \quad \text{or} \quad C = \frac{I_1}{V_2} = \frac{1}{2} \text{ mhos}$$

$$D = \left. \frac{I_1}{-I_2} \right|_{V_2=0} \quad \text{and} \quad -I_2 = \frac{2}{3}I_1 \quad \text{or} \quad D = \frac{I_1}{-I_2} = \frac{3}{2}$$

The overall T-parameters of the cascaded network (given network) are obtained by matrix multiplications.

$$\begin{bmatrix} \frac{3}{2} & \frac{5}{2} \\ \frac{2}{2} & \frac{2}{2} \\ \frac{1}{2} & \frac{3}{2} \\ \frac{2}{2} & \frac{2}{2} \end{bmatrix} \begin{bmatrix} \frac{3}{2} & \frac{5}{2} \\ \frac{2}{2} & \frac{2}{2} \\ \frac{1}{2} & \frac{3}{2} \\ \frac{2}{2} & \frac{2}{2} \end{bmatrix} = \begin{bmatrix} \frac{7}{2} & \frac{15}{2} \\ \frac{2}{3} & \frac{2}{7} \\ \frac{3}{2} & \frac{7}{2} \end{bmatrix}$$

The T-parameter equations of the network are therefore given by:

$$V_1 = \frac{7}{2}V_2 - \frac{15}{2}I_2$$

$$I_1 = \frac{3}{2}V_2 - \frac{7}{2}I_2$$

These two equations may be rewritten in the form of Z-parameter equations.

$$\frac{3}{2}V_2 = I_1 + \frac{7}{2}I_2 \quad \text{or} \quad V_2 = \frac{2}{3}I_1 + \frac{7}{3}I_2$$

$$V_1 = \frac{7}{3}I_1 + \frac{2}{3}I_2$$

Comparing these two equations with Z-Parameter equations we get the Z-parameters of the given network.

$$Z_{11} = Z_{22} = \frac{7}{3}\Omega \quad Z_{12} = Z_{21} = \frac{2}{3}\Omega$$

**2.9 Dependent sources:** So far we have discussed the characteristics of the Passive network having passive elements connected to it. Now the active network having the active elements will be discussed. The active elements used in the network may very likely be transistor, operational amplifiers etc. However, the controlled or dependent Source considered as the basic active element, may be classified as:

- (i) Voltage Controlled Voltage Source (VCVS)
- (ii) Voltage Controlled Current Source (VCCS)
- (iii) Current Controlled Current Source (CCCS)
- (iv) Current Controlled Voltage Source (CCVS)

**(i) Voltage Controlled Voltage Source (VCVS):** It is an ideal voltage source whose voltage is dependent on the input voltage. The network equation may be written by considering following H or T-parameters of the network.

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \mu & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} \Leftrightarrow \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \frac{1}{\mu} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

$$I_1 = 0$$

&  $V_2 = \mu V_1$  Input is open circuited and output is Ideal voltage source, which will depend on the input voltage.

The equivalent network may be drawn as given in Fig. (2.33).

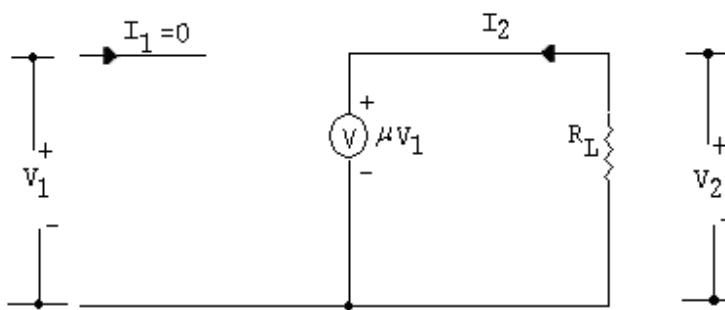


Fig. 2.33

It has input power as zero (since  $I_1 = 0$ ) and has the finite output power as a load resistance is connected to its output terminals. So there is a power gain and hence it is an active element/device. VCVS may also be called as Voltage Amplifier and  $\mu$  is called as the amplification factor.

**(ii) Voltage Controlled Current Source (VCCS):** It is an ideal current source whose current is controlled by the Input voltage. The network equation assuming the  $Y$ - or  $T$ -parameters may be given by:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ g_m & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \Leftrightarrow \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & -1/g_m \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

$I_1 = 0$  : Input is open circuited.

$I_2 = g_m V_1$  : Output is a current source, whose value may be controlled by input voltage.

The network may be shown as:

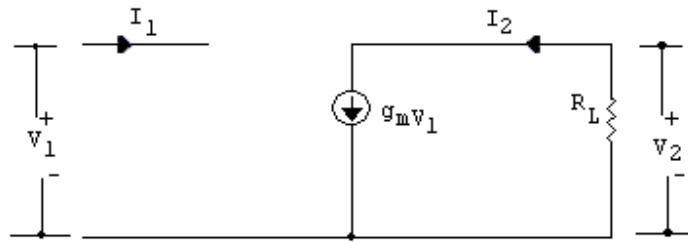


Fig. 2.34

$g_m$  is called as the Transconductance which when multiplied with the input voltage; it gives the magnitude of the Ideal Current Source. It is also the active network since Input Power is zero and output power is finite as output terminals are connected to some load resistance.

**(iii) Current Controlled Current Source (CCCS):** The current controlled current source (CCCS) is an ideal current source whose current is controlled by the input current. It is a Current amplifier, whose network equation may be given by the  $H$ -parameters as:

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \alpha & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \Leftrightarrow \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 1/\alpha \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

$V_1 = 0$  : Input is short circuited.

$I_2 = \alpha I_1$  : Output is the current source, which is controlled by the input current.  $\alpha$  is the current gain of the current amplifier. The equivalent circuit of this network is given in fig. (2.35).

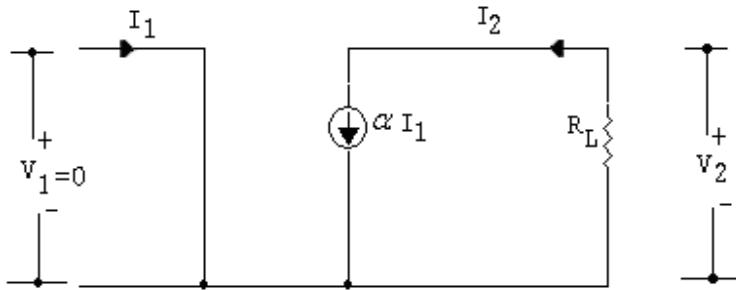


Fig. 2.35

It is also an active network, which may be proved as above.

**(iv) Current Controlled Voltage Source (CCVS):** It is an ideal voltage source whose voltage is controlled by the Input current source. The network equation of CCVS may be given by using Z- parameters as given below:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ r_m & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \Leftrightarrow \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 1/r_m & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

$V_1 = 0$  &  $V_2 = r_m I_1$  Input is short circuited and output is a voltage source whose voltage depends on the input current.

The network may be shown as:

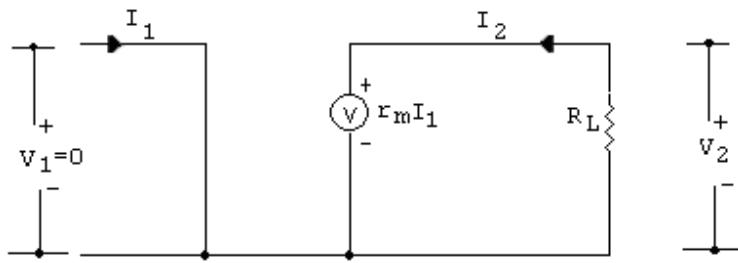


Fig. 2.36

Here  $r_m$  is the trans-resistance which when multiplied by the Input current converts into its output voltage. This too is an active element.

**2.10 Reciprocity:** Passive linear two port network are reciprocal because they exhibit the

property of reciprocity. According to reciprocity theorem the ratio  $\left. \frac{V_1}{I_2} \right|_{V_2=0} = \left. \frac{V_2}{I_1} \right|_{V_1=0}$

The condition of reciprocity of passive network can be obtained by defining any parameters.

(i) Reciprocity condition for Z- parameters: The Z - parameters equation of a network (passive) is given by:

$$\begin{aligned} V_1 &= Z_{11} I_1 + Z_{12} I_2 \\ V_2 &= Z_{21} I_1 + Z_{22} I_2 \end{aligned} \quad \text{----- (2.42)}$$

Putting  $V_2 = 0$  in equation (2.42), it is obtained:

$$I_1 = \frac{-Z_{22}}{Z_{21}} I_2 \quad \& \quad V_1 = -\frac{Z_{11}Z_{22}}{Z_{21}} I_2 + Z_{12} I_2$$

$$\frac{V_1}{I_2} = \frac{Z_{12}Z_{21} - Z_{11}Z_{22}}{Z_{21}}$$

Putting  $V_1 = 0$  in equation (2.42) it is obtained:

$$I_2 = -\frac{Z_{11}}{Z_{12}} I_1 \quad \text{or} \quad V_2 = Z_{21} I_1 - \frac{Z_{11}Z_{22}}{Z_{12}} I_1$$

$$\frac{V_2}{I_1} = \frac{Z_{12}Z_{21} - Z_{11}Z_{22}}{Z_{12}} \quad \text{If the network is reciprocal then } \frac{V_1}{I_2} \text{ should be equal}$$

to  $\frac{V_2}{I_1}$ , which is possible if  $Z_{12} = Z_{21}$ . This is the condition of reciprocity.

The condition for reciprocity for the network (passive) represented by other parameters may also be calculated in the similar fashion.

The network is reciprocal if

$$Z_{12} = Z_{21} \quad \text{in Z-parameters} \quad Y_{12} = Y_{21} \quad \text{in Y-parameters}$$

$$H_{12} = -H_{21} \quad \text{in H-parameters} \quad H'_{12} = -H'_{21} \quad \text{in H'-parameters}$$

$$AD - BC = 1 \quad \text{in T-parameters} \quad A'D' - B'C' = 1 \quad \text{in T'-parameters}$$

The reciprocity theorem, however, in general does not hold well in active network.

**2.11 Ideal Transformer:** Ideal transformer is one, in which there is no loss of Power, i.e. input power is equal to output power. If  $n$  is the turn ratio, then the ratio of Input to the output voltage is given by:

$$\frac{V_1}{V_2} = n \quad \text{or} \quad V_1 = n V_2$$

and the ratio of the output current to the Input current is given by:

$$\frac{I_2}{I_1} = -n \quad \text{or} \quad I_2 = -n I_1$$

So the  $H$ -parameters of the ideal transformer may be given by:

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & n \\ -n & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \quad \text{and its equivalent T-parameters are given by}$$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} n & 0 \\ 0 & 1/n \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

It cannot be represented by the Z or Y-parameters, since input and output resistances of ideal transformer are zero.

**2.12 Impedance Converter:** Let us consider a two port network terminated by an impedance  $Z_L$  to its output port. The equivalent impedance of this network presented at the Input port is given by

$$Z_{in} = (\text{Constant}) Z_L$$

Such a network is called as the Impedance Converter. So Impedance Converter may be defined as a network whose input impedance is the load impedance terminated at the output port multiplied by constant quantity. The constant quantity is called as converter factor.

Impedance Converter may be classified as:

- (i) Positive Impedance Converter (PIC)
- (ii) Negative Impedance Converter (NIC)

**(i) Positive Impedance Converter (PIC):** If the conversion factor discussed above is a +ve quantity, it is called as positive Impedance Converter.

An ideal transformer may be considered as +ve impedance converter. The  $H$ -parameter matrix of an ideal transformer is given by:

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & n \\ -n & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

i.e.  $V_1 = nV_2$  and  $I_2 = -nI_1$  or  $I_1 = -\frac{1}{n}I_2$

$$\frac{V_1}{I_1} = -n^2 \frac{V_2}{I_2} = n^2 Z_L \quad (\text{since } Z_L = -\frac{V_2}{I_2})$$

$$Z_{in} = n^2 Z_L \quad (Z_{in} \text{ is the input impedance})$$

$n$  is the turn ratio,  $n^2$  is definitely a +ve quantity. So ideal transformer may be known as +ve Impedance converter.

**(ii) Negative Impedance Converter (NIC):** If in the Impedance converter, the conversion factor is a negative quantity then it is called as negative impedance converter. It is further of two types:

- (i) Voltage Inversion Type -ve Impedance Converter (VNIC)
- (ii) Current Inversion type -ve Impedance Converter (CNIC)

**VNIC:** Consider the  $H$ -Parameter matrix of a two port network as:

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & -K_1 \\ -K_2 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

i.e.  $V_1 = -K_1 V_2$

(Negative sign indicate that the voltage at the output port is inverted)

$$I_2 = -K_2 I_1 \quad \text{or} \quad I_1 = -\frac{1}{K_2} I_2$$

$$\frac{V_1}{I_1} = K_1 K_2 \frac{V_2}{I_2} \quad \text{or} \quad Z_{in} = -K_1 K_2 Z_L \quad (\text{since } Z_L = -\frac{V_2}{I_2})$$

It is clear from the above discussion that the load impedance ( $Z_L$ ) when multiplied by a negative quantity ( $-K_1 K_2$ ) gives us the input impedance. Hence it is known as VNIC.

**CNIC:** Consider the  $H$ -parameter equation of a network given by:

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & K_1 \\ K_2 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$$V_1 = K_1 V_2$$

$$I_2 = K_2 I_1 \quad \text{or} \quad I_1 = \frac{1}{K_2} I_2$$

(since normally  $I_2$  should -ve, in this case  $I_1$  &  $I_2$  are of same sign, hence current inversion type network)

$$\frac{V_1}{I_1} = K_1 K_2 \frac{V_2}{I_2} \quad \text{or} \quad Z_{in} = -K_1 K_2 Z_L \quad (\text{since } Z_L = -\frac{V_2}{I_2}).$$

**2.13 Gyrator:** Gyrator is a two port network, which when terminated a load Impedance  $Z_L$  at the output port, hen the Input Impedance is inversely proportional to the load impedance.

$$\text{i.e.} \quad Z_{in} \propto \frac{1}{Z_L} \quad \text{or} \quad z_{in} = K \frac{1}{Z_L}$$

where  $K$  is called as the Gyrator constant. The parameters of the network are given as;

$$V_1 = -r I_2 \quad \& \quad V_2 = r I_1 \quad \text{or} \quad I_1 = \frac{1}{r} V_2$$

$$\frac{V_1}{I_1} = -r^2 \frac{I_2}{V_2} = r^2 \frac{1}{Z_L} \quad \text{or} \quad Z_{in} = r^2 \frac{1}{Z_L}$$

$r^2$  is called as the Gyrator Constant. If the load impedance is of capacitive nature ( $Z_L = \frac{1}{j\omega C}$ )

then input impedance will be of inductive nature.

i.e.  $Z_{in} = j\omega C r^2$  ( since  $Cr^2$  has the dimension of inductance).

Similarly if the load is of inductive nature then the input impedance will be of capacitive nature.

**2.14 Cascading of two Gyrators:** If two gyrators are cascaded, the overall response of the network (cascaded network) may be obtained by matrix multiplication of T-parameter matrices of individual gyrators.

Consider the T-parameter matrix of individual gyrators:

$$\text{Gyrator I} \quad \begin{bmatrix} 0 & nr \\ \frac{1}{nr} & 0 \end{bmatrix}$$

$$\text{Gyrator II} \quad \begin{bmatrix} 0 & r \\ \frac{1}{r} & 0 \end{bmatrix}$$

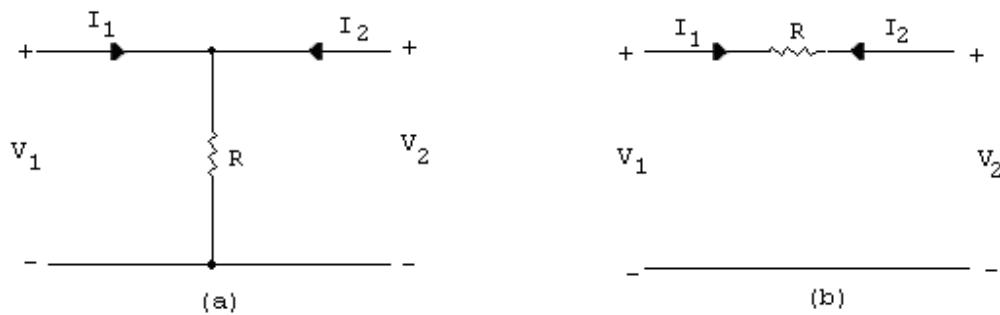
Matrix multiplication of gyrator I and gyrator II

$$\begin{bmatrix} 0 & nr \\ \frac{1}{nr} & 0 \end{bmatrix} \begin{bmatrix} 0 & r \\ \frac{1}{r} & 0 \end{bmatrix} = \begin{bmatrix} n & 0 \\ 0 & \frac{1}{n} \end{bmatrix}$$

is equal to the T-parameter equation of an ideal transformer. So the network of two cascaded gyrators is equivalent to an ideal transformer.

### Problems:

1. What do you understand by Two Port Network? Define H- and T-parameters of a two port network. Find the condition of reciprocity for these parameters.
2. What do you mean by Impedance converter? Explain positive and negative impedance converter. How will you transform the parameters of voltage inversion type negative impedance converter into its equivalent transmission parameters?
3. Find the open- circuit and short circuit parameters of a two port network.
4. Discuss H-parameters of a two port network. Draw its equivalent circuit.
5. Explain the active two port network. What are voltage controlled current source (VCVS) and current controlled voltage source (CCVS)? Show that when CCVS and VCCS are cascaded it behaves like current controlled current source (CCCS).
6. What do you understand by dependent sources? Discuss voltage and current amplifiers in the form of two port network. Show that they are active elements.
7. Discuss voltage control current source (VCCS) and current control voltage source (CCVS). Show that when a VCCS and a CCVS are cascaded, it works as a voltage amplifier.
8. Define gyrator. Show that the two cascaded gyrators can be simulated as an ideal transformer.
9. Define open circuit and short circuit parameters of a two port network. What is transformation of parameters? How can open circuit parameters be converted into its equivalent H-parameters
10. How will you transform H parameters of a passive network into its equivalent Inverse Transmission ( $H'$ ) parameters?
11. What do you understand by dependent sources? By considering a suitable example, explain voltage and current amplifiers.
12. Show that the H-parameters of the two port network will not exist in  $Z_{11}=0$ .
13. Show that Z-parameters of the series combination of two 'Two Port Networks' are equal to the sum of Z-parameters.
14. Show that when two 'Two Port Networks' are connected in parallel; the Y-parameters of the combined two port network may be obtained by adding the Y-parameters of the individual network.
15. Find Z, Y and H parameters of the given two port networks (a) and (b) shown below.



Ans: (a)  $Z_{11} = Z_{12} = Z_{21} = Z_{22} = R$ , Y – parameters does not exist,  $H_{11} = 0$ ,

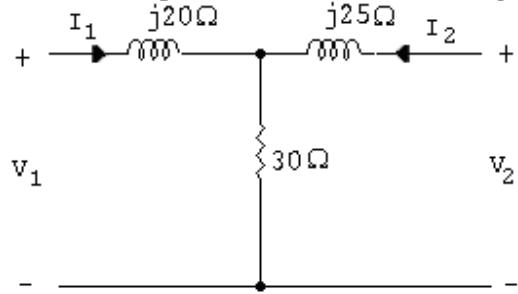
$$H_{12} = -H_{21} = 1, H_{22} = \frac{1}{R}$$

: (b) Z – parameters does not exist,

$$Y_{11} = Y_{22} = \frac{1}{R} \quad \text{, } Y_{12} = Y_{21} = -\frac{1}{R} \quad \text{, } H_{11} = R \Omega,$$

$$H_{12} = -H_{21} = 1, \quad H_{22} = \frac{1}{R}.$$

16. Determine Z and Y-parameters of the network given below.



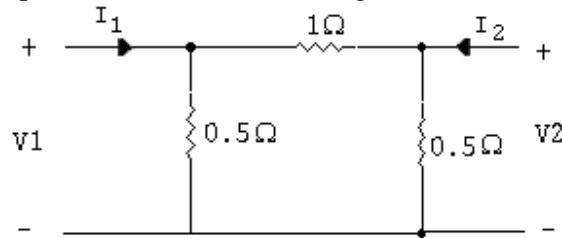
$$\text{Ans.: } Z_{11} = 10(3+2j) \Omega, \quad Z_{12} = Z_{21} = 30 \Omega, \quad Z_{22} = 5(6+j5) \Omega$$

$$Y_{11} = \frac{(6+j5)}{10(27j-10)} \quad \text{, } Y_{12} = Y_{21} = \frac{-3}{5(27j-10)} \quad \text{, } Y_{22} = \frac{(3+2j)}{5(27j-10)}$$

17. A two port network has the following Z-parameters  $Z_{11}=10 \Omega$ ,  $Z_{12}=Z_{21}=5\Omega$  and  $Z_{22}=12\Omega$ . Calculate the Y-parameters of the network. Also show its equivalent Y-parameter network.

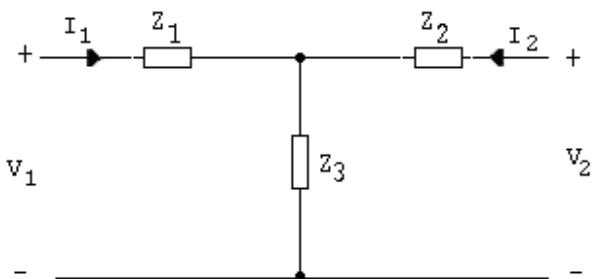
$$\text{Ans.: } Y_{11} = 0.1263 \quad \text{, } Y_{12} = Y_{21} = -0.053 \quad \text{, } Y_{22} = 0.1053$$

18. Find the T-parameters of the network given below. Show that the network is reciprocal.



$$\text{Ans.: } A = D = 3, \quad C = 8 \quad \text{, } B = 1 \Omega$$

19. Find Y, H, and T-parameters of the given network.



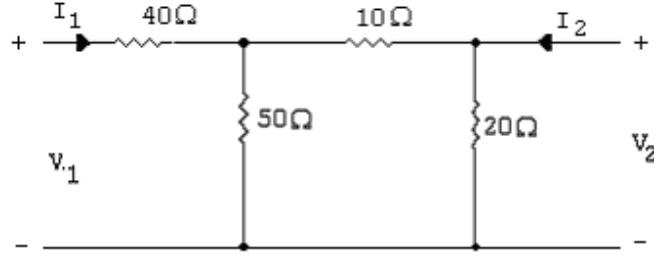
$$\text{Ans.: } Y_{11} = \frac{Z_2 + Z_3}{Z_1 Z_2 + Z_2 Z_3 + Z_1 Z_3} \quad \text{, } Y_{12} = Y_{21} = \frac{-Z_3}{Z_1 Z_2 + Z_2 Z_3 + Z_1 Z_3}$$

$$Y_{22} = \frac{Z_1 + Z_3}{Z_1 Z_2 + Z_2 Z_3 + Z_1 Z_3} \quad \text{or} : H_{11} = \frac{1}{Z_1 + Z_3} \quad \text{or} ,$$

$$H_{22} = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_1 Z_3}{Z_1 + Z_3} \Omega , \quad H_{12} = \frac{-Z_3}{Z_1 + Z_3} = -H_{21} , \quad A = \frac{Z_3}{Z_1 + Z_3} ,$$

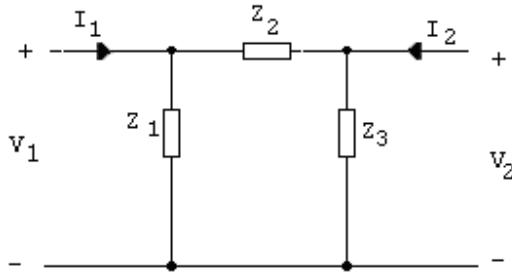
$$B = \frac{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3}{Z_3} \Omega , \quad C = \frac{1}{Z_3} \quad \text{or} , \quad D = \frac{Z_3}{Z_2 + Z_3}$$

20. Find H-parameters of the network.



$$\text{Ans.: } H_{11} = 48.33 \Omega , \quad H_{12} = 0.83 = -H_{21} , \quad H_{22} = 0.067 \quad \text{or}$$

21. Find H, Z, Y and T- parameters of the given  $\Pi$  network.



$$\text{Ans.: } H_{11} = \frac{Z_1 Z_2}{Z_1 + Z_2} \Omega , \quad H_{12} = \frac{Z_1}{Z_1 + Z_2} = -H_{21} , \quad H_{22} = \frac{Z_1 + Z_2 + Z_3}{(Z_1 + Z_2) Z_3} \quad \text{or}$$

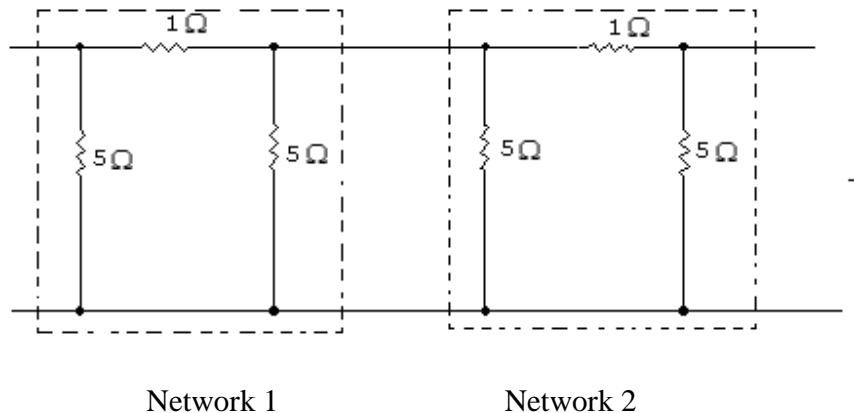
$$Z_{11} = \frac{Z_1 (Z_2 + Z_3)}{Z_1 + Z_2 + Z_3} \Omega , \quad Z_{12} = Z_{21} = \frac{Z_1 Z_3}{Z_1 + Z_2 + Z_3} \Omega ,$$

$$Z_{22} = \frac{Z_3 (Z_1 + Z_2)}{Z_1 + Z_2 + Z_3} \Omega ; \quad A = \frac{Z_2 + Z_3}{Z_3} , \quad B = Z_2 \Omega ,$$

$$C = \frac{Z_1 + Z_2 + Z_3}{Z_1 Z_3} \quad \text{or} , \quad D = \frac{Z_1 + Z_2}{Z_1} : \quad Y_{11} = \frac{Z_1 + Z_2}{Z_1 Z_2} \quad \text{or} ,$$

$$Y_{12} = Y_{21} = \frac{-1}{Z_2} \quad \text{or} , \quad Y_{22} = \frac{Z_{21} + Z_3}{Z_2 Z_3} \quad \text{or} .$$

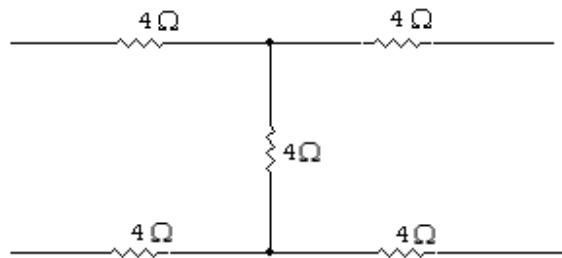
22. Two identical  $\pi$  - networks are cascaded together as shown in the figure given below. Find the H – parameters of this cascaded network. Show that this network is reciprocal.



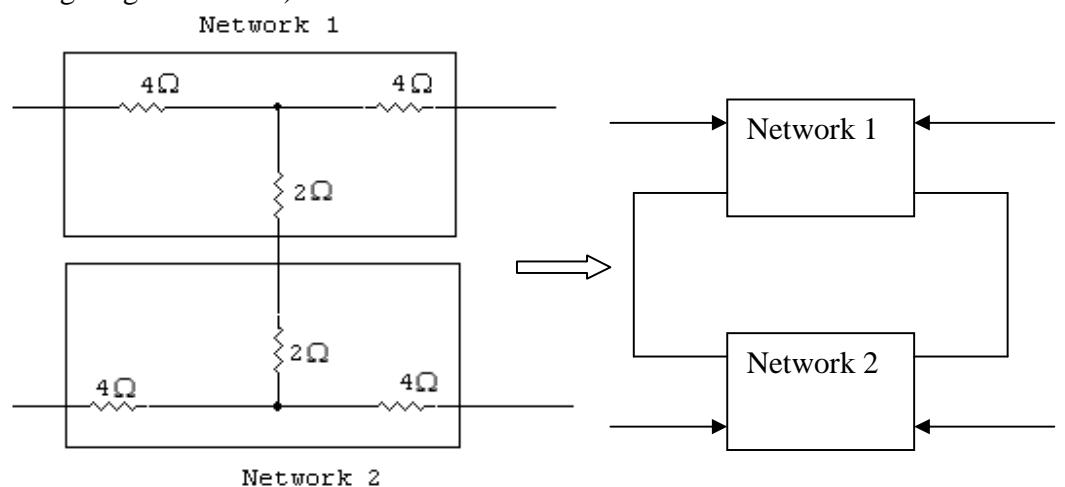
(Hint: First find the A, B, C, D parameters of the one given  $\pi$ - network (identical). Overall T - parameters of the cascaded network are obtained by matrix multiplication of the individual  $\pi$  - network. These parameters may further be transformed to H – parameters.)

Ans.:  $H_{11} = \frac{60}{47} \Omega$ ,  $H_{12} = -H_{21} = \frac{25}{47}$ ,  $H_{22} = \frac{132}{47}$

23. Find T' – parameters of the given network.



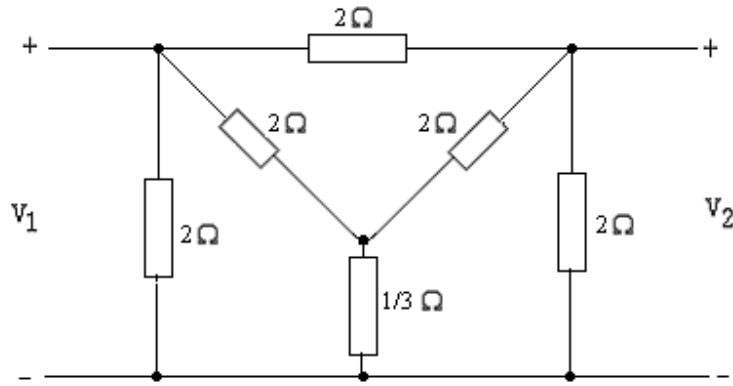
(Hint: This circuit is a series combination of two identical T- networks shown in the figure given below.)



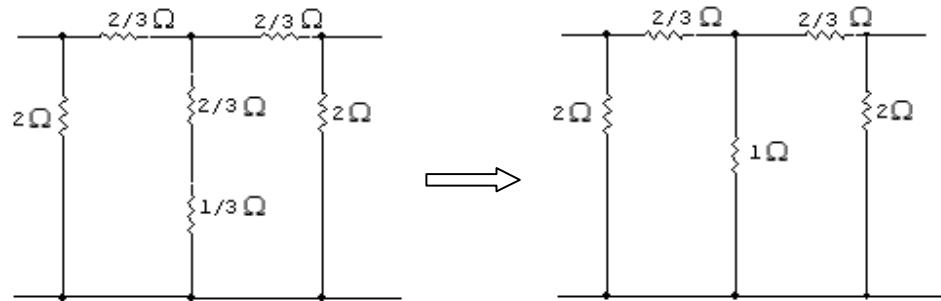
Find the Z – parameters of the individual T-network; by adding the Z-parameters of the two networks, the overall Z-parameters of the given network are obtained, which may further be transformed to  $T$  – parameters.)

$$\text{Ans.: } A' = 3 = D', \quad B' = 32 \Omega, \quad C' = \frac{1}{4} \quad \square.$$

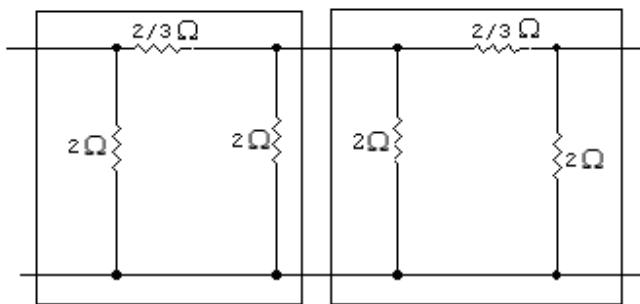
24. Find T - parameters of the network shown below.



Hint: The network may be redrawn using the delta to star conversion of upper delta network as:



This network may further be shown as a cascaded network of two identical  $\pi$  – networks as:



Network 1

Network 2

Ans.:  $A = \frac{23}{9} = D$ ,  $B = \frac{16}{9} \Omega$ ,  $C = \frac{28}{9}$   $\square$ .

---

# 3

## Networks with time Varying Sources

So far the analysis of networks containing only batteries and resistances has been discussed. In this chapter the network with time varying sources, resistances and other elements like inductances capacitances and transformers, etc. will also be discussed. The time varying sources are generally of three types, viz., periodic, aperiodic and random. Sine, Square and Triangular waves are periodic, since it repeats after a fixed interval of time. Periodic waves are generally used in the electronic circuits and are of our great interest. A pulse is aperiodic and noise is of random nature.

**3.1 Fourier series:** Any function  $f(t)$  can be expanded using Fourier series, which is expressed as the summation of sinusoidal (sine, cosine or both) terms as given by:

$$f(t) = A_0 + \sum_{n=1}^{\infty} A_n \sin(n\omega t) + \sum_{n=1}^{\infty} B_n \cos(n\omega t) \quad \text{----- (3.1)}$$

where  $A_0 = \frac{1}{T} \int_0^T f(t).dt$  ----- (3.2)

$$A_n = \frac{2}{T} \int_0^T f(t). \sin(n\omega t).dt \quad \text{----- (3.3)}$$

$$B_n = \frac{2}{T} \int_0^T f(t). \cos(n\omega t).dt \quad \text{----- (3.4)}$$

**Example 3.1** Find the first four coefficients of the half wave rectified output, using Fourier series expansion. Characteristics of the wave are:

$$\begin{aligned} f(t) &= E_m \sin \omega t && \text{when } 0 \leq t \leq T/2 \\ f(t) &= 0 && T/2 \leq t \leq T \end{aligned}$$

**Solution:** The coefficients of Fourier series of the half wave rectified output wave are given as:

$$A_0 = \frac{1}{T} \int_0^T E_m \sin(\omega t).dt = \frac{1}{T} \left[ \int_0^{T/2} E_m \sin(\omega t).dt + \int_{T/2}^T (0).dt \right]$$

$$= \frac{E_m}{\pi} \quad \text{----- (3.5)}$$

$$\begin{aligned} A_n &= \frac{2}{T} \left[ \int_0^{T/2} E_m \sin(\omega t) \cdot \sin(n\omega t) dt \right] \\ &= \frac{2E_m}{T} \int_0^{T/2} [\cos((n-1)\omega t) - \cos((n+1)\omega t)] dt \\ &= \frac{2E_m \omega}{2\pi} \left[ \frac{\sin((n-1)\omega t)}{(n-1)\omega} - \frac{\sin((n+1)\omega t)}{(n+1)\omega} \right]_0^{T/2} \\ &= \frac{E_m}{\pi} \left[ \frac{\sin((n-1)\pi)}{(n-1)} - \frac{\sin((n+1)\pi)}{(n+1)} \right] \\ &= 0 \quad (\text{for all values of } n, \text{ except for } n = 1) \end{aligned}$$

For  $n = 1$  denominator of the above equation will be indeterminant. So we calculate  $A_1$  by putting  $n = 1$  directly in equation (3.6) as:

$$\begin{aligned} A_1 &= \frac{2}{T} \int_0^{T/2} E_m \sin \omega t \cdot \sin \omega t dt \\ &= \frac{2E_m}{T} \int_0^{T/2} \sin^2 \omega t dt = \frac{2E_m}{2T} \int_0^{T/2} [1 - \cos 2\omega t] dt \\ &= \frac{E_m}{T} \left[ \frac{T}{2} - \left[ \frac{\sin 2\omega t}{2\omega} \right]_0^{T/2} \right] = \frac{E_m}{T} \left[ \frac{T}{2} - 0 \right] \\ &= \frac{E_m}{2} \quad \text{----- (3.7)} \end{aligned}$$

$B_n$  may be calculated as:

$$\begin{aligned} B_n &= \frac{2}{T} \int_0^{T/2} E_m \sin(\omega t) \cdot \cos(n\omega t) dt \\ &= \frac{2E_m}{T} \int_0^{T/2} \left[ \frac{-\sin((n-1)\omega t) + \sin((n+1)\omega t)}{2} \right] dt \\ &= \frac{E_m \omega}{2\pi} \left[ \frac{\cos((n-1)\omega t)}{(n-1)\omega} - \frac{\cos((n+1)\omega t)}{(n+1)\omega} \right]_0^{T/2} \\ &= \frac{E_m}{2\pi} \left[ \frac{\cos((n-1)\pi)}{(n-1)} - \frac{\cos((n+1)\pi)}{(n+1)} - \frac{1}{(n-1)} + \frac{1}{(n+1)} \right] \\ \text{If } n \text{ is odd, then } B_n &= \frac{E_m}{2\pi} \left[ \frac{1}{(n-1)} - \frac{1}{(n+1)} - \frac{1}{(n-1)} + \frac{1}{(n+1)} \right] = 0 \quad \text{----- (3.8)} \end{aligned}$$

If  $n$  is even, then

$$\begin{aligned}
 B_n &= \frac{E_m}{2\pi} \left[ -\frac{1}{(n-1)} + \frac{1}{(n+1)} - \frac{1}{(n-1)} + \frac{1}{(n+1)} \right] \\
 &= \frac{2E_m}{2\pi} \left[ -\frac{1}{(n-1)} + \frac{1}{(n+1)} \right] \\
 &= \frac{E_m}{\pi} \left[ \frac{-n-1+n-1}{(n^2-1)} \right] = -\frac{2E_m}{(n^2-1)\pi}
 \end{aligned} \quad \text{----- (3.9)}$$

(where  $n$  is even i.e.  $n = 2, 4, 6, 8, \dots$ )

So by putting the values of  $A$ 's and  $B$ 's in equation 3.1 we get the required function for half wave rectified output as:

$$E = \frac{E_m}{\pi} + \frac{E_m}{2} \sin \omega t - \frac{2E_m}{3\pi} \cos 2\omega t - \frac{2E_m}{15\pi} \cos 4\omega t - \frac{2E_m}{35\pi} \cos 6\omega t \dots \quad \text{----- (3.10)}$$

**Example 3.2** Consider a full wave rectified signal of peak value  $E_m$  and period  $T$ . Find its coefficients in the Fourier series expansion.

Solution: The coefficients of Fourier series of the full wave rectified output wave are given as:

$$\begin{aligned}
 A_0 &= \frac{1}{T} \int_0^T E_m \sin(n\omega t) dt = \frac{1}{T} \left[ \int_0^{T/2} E_m \sin(\omega t) dt + \int_{T/2}^T (-)E_m \sin(\omega t) dt \right] \\
 &= \frac{2E_m}{\pi}
 \end{aligned} \quad \text{----- (3.11)}$$

$$\begin{aligned}
 A_n &= \frac{2}{T} \left[ \int_0^{T/2} E_m \sin(\omega t) \cdot \sin(n\omega t) dt + \int_{T/2}^T E_m \sin(\omega t) \cdot \sin(n\omega t) dt \right] \\
 &= \frac{4E_m}{T} \left[ \int_0^{T/2} \sin(\omega t) \cdot \sin(n\omega t) dt \right] \\
 &= \frac{4E_m}{2T} \int_0^{T/2} [\cos(n-1)\omega t - \cos(n+1)\omega t] dt \\
 &= \frac{2E_m \omega}{2\pi} \left[ \frac{\cos(n-1)\omega t}{(n-1)\omega} - \frac{\cos(n+1)\omega t}{(n+1)\omega} \right]_0^{T/2} \\
 &= \frac{E_m}{\pi} \left[ \frac{\sin(n-1)\pi - \sin 0}{(n-1)} - \frac{\sin(n+1)\pi + \sin 0}{(n+1)} \right] \\
 &= \frac{E_m}{\pi} \left[ \frac{\sin(n-1)\pi}{(n-1)} - \frac{\sin(n+1)\pi}{(n+1)} \right] = 0
 \end{aligned} \quad \text{----- (3.12)}$$

$$\begin{aligned}
B_n &= \frac{2E_m}{T} \int_0^{T/2} E_m \sin(\omega t) \cos(n\omega t) dt \\
&= \frac{4E_m}{T} \int_0^{T/2} \left[ \frac{-\sin((n-1)\omega t) + \sin((n+1)\omega t)}{2} \right] dt \\
&= \frac{2E_m \omega}{2\pi} \left[ \frac{\cos((n-1)\omega t)}{(n-1)\omega} - \frac{\cos((n+1)\omega t)}{(n+1)\omega} \right]_0^{T/2} \\
&= \frac{E_m}{\pi} \left[ \frac{\cos((n-1)\pi)}{(n-1)} - \frac{\cos((n+1)\pi)}{(n+1)} - \frac{1}{(n-1)} + \frac{1}{(n+1)} \right]
\end{aligned}$$

If  $n$  is odd, then  $B_n = \frac{E_m}{\pi} \left[ \frac{1}{(n-1)} - \frac{1}{(n+1)} - \frac{1}{(n-1)} + \frac{1}{(n+1)} \right] = 0$  ----- (3.13)

If  $n$  is even, then  $B_n = \frac{E_m}{\pi} \left[ -\frac{1}{(n-1)} + \frac{1}{(n+1)} - \frac{1}{(n-1)} + \frac{1}{(n+1)} \right]$

$$\begin{aligned}
&= \frac{2E_m}{2\pi} \left[ -\frac{1}{(n-1)} + \frac{1}{(n+1)} \right] \\
&= \frac{2E_m}{\pi} \left[ \frac{-n-1+n-1}{(n^2-1)} \right] = -\frac{4E_m}{(n^2-1)\pi} \quad \text{----- (3.14)}
\end{aligned}$$

(where  $n$  is even i.e.  $n = 2, 4, 6, 8, \dots$ )

So by putting the values of A's and B's in equation 3.1, the required function for full wave rectified output is obtained as:

$$E = \frac{2E_m}{\pi} - \frac{4E_m}{3\pi} \cos 2\omega t - \frac{4E_m}{15\pi} \cos 4\omega t - \frac{4E_m}{35\pi} \cos 6\omega t \dots \quad \text{----- (3.15)}$$

**Example 3.3** Consider a symmetrical triangular wave of peak value  $E_m$  and period  $T$  as shown in figure (3.1). Find its coefficients in the Fourier series.

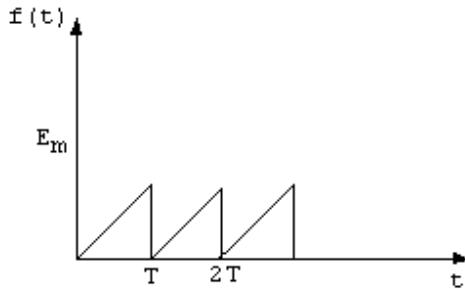


Fig. 3.1

$$\begin{aligned} \text{Solution: let } f(t) = X + Y.t & \quad \text{at } t=0 \quad f(t)=0 \text{ So } X=0 \\ & \quad \text{at } t=T \quad f(t)=E_m \\ E_m = YT & \quad \text{or } Y=(E_m)/T \end{aligned}$$

$f(t) = (\frac{E_m}{T})t$  is the equation of the triangular wave. So the coefficients of Fourier series of this wave are given as:

$$\begin{aligned} A_0 &= \frac{1}{T} \int_0^T \frac{E_m}{T} \cdot t \cdot dt = \frac{E_m}{T^2} \left[ \frac{T^2}{2} \right] = \frac{E_m}{2} \quad \text{----- (3.16)} \\ A_n &= \frac{2}{T} \left[ \int_0^T \frac{E_m}{T} \cdot t \cdot \sin(n\omega t) \cdot dt \right] \\ &= \frac{2E_m}{T^2} \int_0^T t \cdot \sin(n\omega t) \cdot dt \\ &= \frac{2Em}{T^2} \left[ \frac{-t \cos(n\omega t)}{n\omega} + \int_0^T \frac{1 \cdot \cos(n\omega t)}{n\omega} \cdot dt \right] \\ &= \frac{2E_m}{T^2} \left[ \frac{-t \cos(n\omega t)}{n\omega} + \frac{\sin(n\omega t)}{n^2 \omega^2} \right]_0^T \\ &= \frac{2E_m}{T^2} \left[ \frac{-TCos(2n\pi)}{n\omega} + \frac{\sin(2n\pi)}{n^2 \omega^2} \right] \\ &= -\frac{2E_m}{T^2} \left[ \frac{TCos(2n\pi)}{n\omega} \right] = -\frac{2E_m}{n\omega} \cos 2n\pi \\ &= -\frac{E_m}{n\pi} \quad (\text{since } \cos 2n\pi = 1 \text{ for all values of } n) \end{aligned}$$

$$\begin{aligned} B_n &= \frac{2}{T} \left[ \int_0^T \frac{E_m}{T} \cdot t \cdot \cos(n\omega t) \cdot dt \right] \\ &= \frac{2E_m}{T^2} \left[ \frac{t \sin(n\omega t)}{n\omega} - \int_0^T \frac{1 \cdot \sin(n\omega t)}{n\omega} \cdot dt \right] \\ &= \frac{2E_m}{T^2} \left[ \frac{t \sin(n\omega t)}{n\omega} + \frac{\cos(n\omega t)}{n^2 \omega^2} \right]_0^T \\ &= \frac{2E_m}{T^2} \left[ \frac{TSin(2n\pi)}{n\omega} + \frac{\cos(2n\pi)}{n^2 \omega^2} - \frac{1}{n^2 \omega^2} \right] \end{aligned}$$

$$= \frac{2E_m}{n^2 \omega^2 T^2} [Cos(2n\pi) - 1] = \frac{2E_m}{2n^2 \pi^2} [1 - 1] = 0 \quad \text{----- (3.17)}$$

So by putting the values of  $A$ 's and  $B$ 's in equation 3.1, the required Fourier series of the triangular wave is as:  $E = \frac{E_m}{2} - \frac{E_m}{\pi} Sin\omega t - \frac{E_m}{2\pi} Sin2\omega t - \frac{E_m}{3\pi} Sin3\omega t \dots \dots$

**Example 3.4** Find the Fourier series expansion of the square wave shown in figure (3.2).

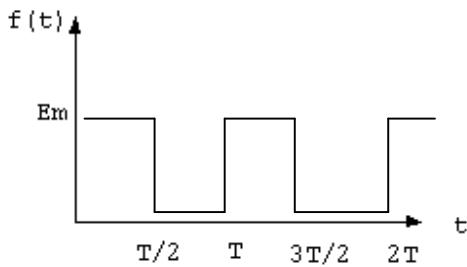


Fig. 3.2

Solution: The coefficients of Fourier series of the square wave are defined as:

$$A_0 = \frac{1}{T} \int_0^T f(t) dt = \frac{1}{T} \left[ \int_0^{T/2} E_m dt + \int_{T/2}^T (0) dt \right]$$

$$= \frac{E_m}{T} \left[ \frac{T}{2} \right] = \frac{E_m}{2}$$

$$A_n = \frac{2}{T} \left[ \int_0^{T/2} E_m \cdot Sin(n\omega t) dt + \int_{T/2}^T (0) \cdot Sin(n\omega t) dt \right] = \frac{2E_m}{n\omega T} [-Cos(n\omega t)]_0^{T/2}$$

$$= \left( \frac{2E_m}{n\omega T} \right) [1 - Cos(n\omega T / 2)]$$

$$= \left( \frac{2E_m}{n\pi} \right) [1 - Cos(n\pi)] = 0 \text{ for even values of } n$$

$$= \left( \frac{2E_m}{n\pi} \right) \text{ for odd values of } n$$

$$B_n = \frac{2}{T} \left[ \int_0^{T/2} E_m \cdot Cos(n\omega t) dt + \int_{T/2}^T (0) Cos(n\omega t) dt \right]$$

$$= \left( \frac{2E_m}{n\omega T} \right) [Sin(n\omega t)]_0^{T/2} = \left( \frac{2E_m}{n\omega T} \right) Sin\left(\frac{n\omega T}{2}\right) = \frac{E_m}{n\pi} Sin(n\pi) = 0 \text{ for all values of } n.$$

So by putting the values of  $A$ 's and  $B$ 's in this equation, the required Fourier series of the Square wave is given as:

$$f(t) = \frac{E_m}{2} + \frac{2E_m}{\pi} \sin(\omega t) + \frac{2E_m}{3\pi} \sin(3\omega t) + \frac{2E_m}{5\pi} \sin(5\omega t) + \frac{2E_m}{7\pi} \sin(7\omega t) + \dots$$

**3.2 Sinusoidal Signal applied to different elements:** When an A.C. signal  $E(t) = E_m \sin \omega t$  is applied to a simple resistance, according to Ohm's Law one may obtain the instantaneous value of the current flowing through the circuit as:

$$\begin{aligned} I(t) &= \frac{E(t)}{R} = \frac{E_m}{R} \sin \omega t \\ &= I_m \sin \omega t \quad (I_m \text{ is the peak value of current}) \end{aligned}$$

Thus the current wave form is the exact replica of the voltage, i.e., both are in the same phase. But when an A.C. source is applied to any combination of resistance, inductance and capacitance, we get the current and voltage are having certain phase difference. Phase relation between the current flowing through and voltage applied across the circuit may best be understood if the Impedances and reactances are represented on the complex plain.

When an A.C. signal  $E(t) = E_m \sin \omega t$  is applied across an inductance  $L$ , the instantaneous value of the current flowing through the circuit is given by:

$$\begin{aligned} I(t) &= \frac{1}{L} \int E(t) dt = \frac{1}{L} \int (E_m \sin \omega t) dt \\ &= \frac{E_m}{L} \cdot \frac{-\cos \omega t}{\omega} = \left( \frac{E_m}{\omega L} \right) \sin \left( \omega t - \frac{\pi}{2} \right) \quad \text{----- (3.18)} \end{aligned}$$

It is clear from this equation that the current is lagging by an angle of  $90^\circ$  with the voltage. The quantity  $\left( \frac{E_m}{\omega L} \right)$  is known as the peak value of the current. It is customary to represent the magnitude as well as the phase relation between the voltage and the current in a graphical form. Such a graphical form is known as phasor diagram.

The phasor diagram is generally represented on the complex plain, as shown in figure (3.3). When a quantity coincides with the  $X$ -axis (real axis), it is known as real quantity. The quantity on  $X$ -axis when multiplied by  $j$  ( $(j = \sqrt{-1})$ , makes it purely imaginary quantity. It rotates by an angle of  $90^\circ$  in the anti-clock wise direction. However, when the real quantity is divided by  $j$  or multiplied by  $(-j)$  it rotates in the clock wise direction by  $90^\circ$ .

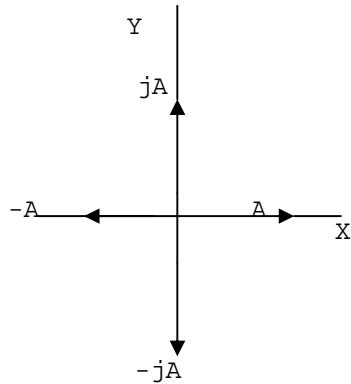


Fig. 3.3

From the equation (3.18), it is clear that the voltage  $E$ , when divided by  $\omega L$ , the correct magnitude of the current is obtained. In order to rotate the phase by  $-90^\circ$  the magnitude of current is further divided by  $j$  as:

$$I = \frac{E}{j\omega L} \quad \text{and} \quad \angle I = \angle E - \frac{\pi}{2}$$

The imaginary quantity ( $j\omega L$ ) is called the inductive reactance of the inductance  $L$ .

The current is lagging behind the voltage by an angle of  $90^\circ$  as shown in figure (3.4). This is the phase relation between the current and voltage.

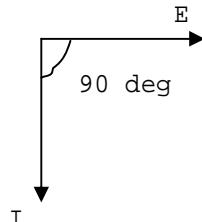


Fig. 3.4

Similarly the reactance of a capacitance is  $\frac{1}{j\omega C}$  or  $\frac{-j}{\omega C}$ , which is also an imaginary quantity represented on the imaginary axis. The current flowing through the capacitance  $C$  when an A.C. signal of voltage  $E$  is applied across the capacitance is given by:

$$I = \frac{E}{(1/j\omega C)} = j\omega CE$$

$$\text{or} \quad \angle I = \angle E + \frac{\pi}{2}$$

The current is  $90^\circ$  ahead by the voltage as is shown in figure (3.5).

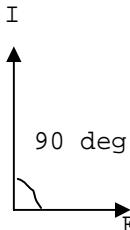


Fig. 3.5

The impedance of a series combination of a resistance  $R$  and an inductance  $L$  is given by  $Z = R + j\omega L$  or  $|Z| = \sqrt{R^2 + (\omega L)^2}$

The phase angle  $\theta$  the impedance makes with the resistive component  $R$  is given by:  $\theta = \tan^{-1}(\frac{\omega L}{R})$

The impedance  $Z$  is written as:  $Z = |Z| \angle \tan^{-1}(\frac{\omega L}{R})$

The current flowing through this combination is given by:

$$I = \frac{E}{Z} = \frac{E}{R + j\omega L} \quad \text{or} \quad \angle I = \angle E - \tan^{-1}(\frac{\omega L}{R})$$

The current is lagging behind with the voltage by an angle  $\tan^{-1}(\frac{\omega L}{R})$ .

The impedance of a series combination of a resistance  $R$  and an capacitance  $C$  is given by  $Z = R + \frac{1}{j\omega C}$  or  $|Z| = \sqrt{R^2 + (1/\omega C)^2}$

The phase angle  $\theta$  the impedance makes with the resistive component  $R$  is given by:  $\theta = \tan^{-1}(\frac{1}{\omega CR})$

The impedance  $Z$  is written as:  $Z = |Z| \angle \tan^{-1}(\frac{1}{\omega CR})$

The current flowing through this combination is given by:

$$I = \frac{E}{Z} = \frac{E}{R + (1/j\omega C)} = \frac{E(j\omega C)}{1 + j\omega CR} \quad \text{or} \quad \angle I = \angle E + \frac{\pi}{2} - \tan^{-1}(\omega CR)$$

The phase difference between current and voltage is  $\frac{\pi}{2} - \tan^{-1}(\omega CR)$ .

**Example 3.5** An A.C. signal of 20 volts and frequency 200Hz as applied to a circuit consisting of  $10 \text{ mH}$  inductance and  $10 \Omega$  resistance in series with it. Find the magnitude and phase of the current.

Solution: The impedance  $Z$  of series combination is given by:

$$Z = R + j2\pi f \cdot L = 10 + jx2x3.14x200x10x10^{-3} = 10 + jx12.56$$

$$|Z| = \sqrt{(10)^2 + (12.56)^2} = 16\Omega \quad \text{and} \quad \theta = \tan^{-1}\left(\frac{12.56}{10}\right) = 51.47^0$$

Current  $|I| = \frac{20}{16} = 1.25 \text{ amp}$

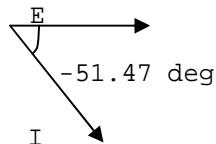


Fig. 3.6

And phase difference  $\phi = \angle I - \angle V = -51.47^0$

**Example 3.6** Consider a series R – C circuit having  $R = 1.5K\Omega$  and  $C = 0.2\mu F$  is excited by a sinusoidal signal of 20 volts and frequency 2 KHz. Find the magnitude and phase of the current.

Solution: The impedance of the R – C circuit is given by:

$$Z = R - \frac{j}{\omega C} = 1500 - \frac{j}{2x3.14x2000x0.2x10^{-6}}$$

$$= 1500 - \frac{j10^4}{25.12} = 1500 - j398.1$$

$$|Z| = \sqrt{(1500)^2 + (398.1)^2} = 1552\Omega$$

$$\theta = -\tan^{-1}\left(\frac{398.1}{1500}\right) = -14.86^0$$

So  $Z = 1552\Omega \angle -14.86^0$

The current is given by:  $I = \frac{20}{1552 \angle -14.86^0} = 12.9mA \angle 14.86^0$

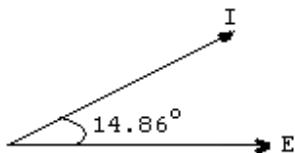


Fig. 3.7

The phasor diagram is given in figure 3.7.

**Example 3.7** Consider a sinusoidal signal of peak value of 20 volts with frequency of 2000 radians/sec is applied to a circuit shown in figure (3.8).  $L=20 \text{ mH}$ ,  $C_1=C_2=0.2 \mu F$ ,  $R=100 \Omega$ . Calculate the total current  $I$  and the currents  $I_1$  &  $I_2$  in the two branches.

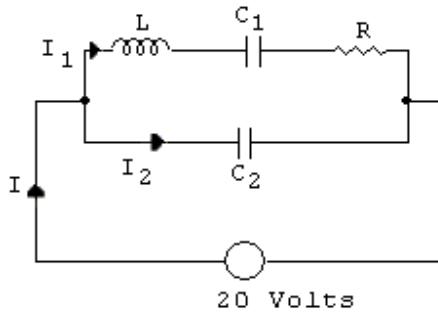


Fig. 3.8

Solution: Impedance  $Z_1$  of the series branch is given by:

$$\begin{aligned} Z_1 &= R + j(\omega L - \frac{1}{\omega C_1}) = 100 + j(2000 \times 20 \times 10^{-3} - \frac{1}{2000 \times 0.2 \times 10^{-6}}) \\ &= 100 + j(40 - \frac{10^4}{4}) = 100 - j(2460) = 2.46 K\Omega \angle -87.67^\circ \end{aligned}$$

Current  $I_1$  in this series branch is given by:

$$I_1 = \frac{20}{Z_1} = \frac{20}{2.46 K\Omega \angle -87.67^\circ} = 8.13 mA \angle 87.67^\circ$$

$$\begin{aligned} \text{Impedance of the capacitor branch } Z_2 &= \frac{-j}{\omega C_2} = \frac{-j}{2000 \times 0.2 \times 10^{-6}} = \frac{-j10^4}{4} \\ &= -2500j = 2.5 K\Omega \angle -\pi/2 \end{aligned}$$

Current  $I_2$  in this branch is given by:

$$I_2 = \frac{20}{2.5 K\Omega \angle -\pi/2} = 8mA \angle \pi/2$$

Admittance of  $Z_1$  &  $Z_2$  impedances is given by:

$$\begin{aligned} Y &= \frac{1}{Z} = \frac{1}{Z_1} + \frac{1}{Z_2} = \frac{1}{2.46 K\Omega \angle -87.67^\circ} + \frac{1}{2.5 K\Omega \angle -\pi/2} \\ &= 0.00041 \angle 87.67^\circ + 0.0004 \angle \pi/2 \\ &= [0.000017 + j0.00081] + [j0.0004] = 0.000017 + j0.00081 \\ &= 0.00081 \angle 88.8^\circ \end{aligned}$$

$$\text{Total impedance } Z = \frac{1}{0.00081 \angle 88.8^\circ} = 1.23 K\Omega \angle -88.8^\circ$$

$$\text{Total current } I = \frac{20}{1.23 K\Omega \angle -88.8^\circ} = 16.1 mA \angle 88.8^\circ$$

**3.3 R – L Low pass filter:** Consider a circuit shown in figure (3.9), in which an A.C. signal  $E$  is applied across the series combination of resistance  $R$  and Inductance  $L$ .

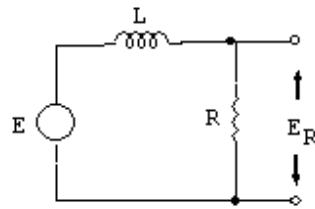


Fig. 3.9

The output is taken across the resistance R, which is given by:

$$E_R = \frac{E \cdot R}{(R + j\omega L)} = \frac{E}{\left(1 + \frac{j\omega L}{R}\right)} \quad \text{----- (3.19)}$$

The quantity  $\frac{L}{R}$  has the dimension of time and is represented by  $\tau$ .

So  $|E_R| = \frac{|E|}{\sqrt{(1 + \omega^2 \tau^2)}}$  or  $\frac{|E_R|}{|E|} = \frac{1}{\sqrt{(1 + \omega^2 \tau^2)}}$  ----- (3.20)

Now a graph between  $\left|\frac{E_R}{E}\right|$  and the frequency  $\omega$  is plotted as shown in figure (3.10). This graph is known as the frequency response curve of the circuit.

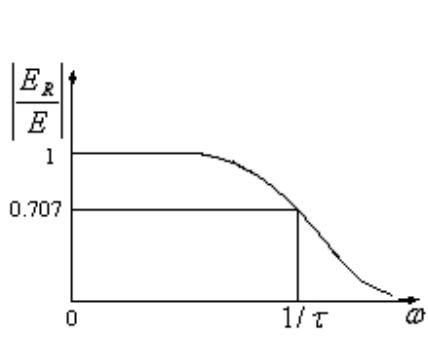
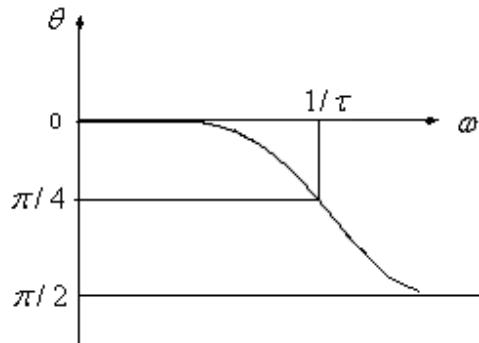


Fig. 3.10 (a)



(b)

From this graph it is clear that if the input frequency is low enough then the output of the circuit will be almost the same as the input signal; and if the frequency of the input signal is high enough then the output is attenuated i.e. only a small amount of input reaches at the output. Hence the circuit behaves like a low pass filter. In other words we may say that this circuit is suitable to separate the signal of low frequency from a mixer of signals of low and high frequencies. The best use of this circuit is to detect a signal of low frequency from the high frequency noise. Its behaviour may also be explained if the reactance of the inductance is considered. It offers low reactance at low frequency and acts as an on switch, thus allows the input signal to pass to the output. However, it offers high reactance for the high frequency acting as an open switch.

resulting thereby an attenuation of the input signal. In the equation (3.20), if  $\omega = \frac{1}{\tau} = \frac{R}{L}$ ,

then  $\left| \frac{E_R}{E} \right|$  will be equal to  $\frac{1}{\sqrt{2}}$  or 0.707, which is known as cutoff frequency  $\omega_0$  or  $-3db$  (decibel)<sup>1</sup> point.

The voltage gain in  $db$  is defined as:

$$\text{Voltage gain (in } db) = 20 \log_{10} (A_V)$$

$$\text{If } A_V = \frac{1}{\sqrt{2}} \text{ then } 20 \log_{10} (A_V) = 20 \log_{10} \left( \frac{1}{\sqrt{2}} \right) = -\frac{20}{2} \log_{10} 2 = -3db.$$

$$\text{The cutoff frequency is given by: } \omega_0 = \frac{1}{\tau} = \frac{R}{L} \text{ radians/sec or } f_0 = \frac{1}{2\pi} \cdot \frac{R}{L} \text{ Hz.}$$

Putting the value of  $\omega_0$  or  $f_0$  in equation (3.20), it is obtained:

$$\frac{|E_R|}{|E|} = \frac{1}{\sqrt{[1 + (\omega/\omega_0)^2]}} = \frac{1}{\sqrt{[1 + (f/f_0)^2]}}$$

So beyond cutoff frequency  $\omega_0$  or  $-3db$  point, the gain (ratio of the output signal to the input signal) of the circuit decreases and becomes zero as  $\omega \rightarrow \infty$ . From this equation it is clear that when the frequency is increased by 10 fold beyond cutoff ( $\omega/\omega_0 = 10$ ), the gain decreases 10 times.

$$\text{So } \frac{|E_R|}{|E|} = \frac{1}{\sqrt{[1 + (\omega/\omega_0)^2]}} = \frac{1}{\sqrt{1+100}} \cong \frac{1}{10} \text{ or } 20db$$

$$\text{As } 20 \log_{10} \left( \frac{1}{10} \right) = -20 \log_{10} 10 = -20db; \text{ or when the frequency is increased}$$

$$\text{by two fold } (\omega/\omega_0 = 2) \text{ the gain decreases 2 times } \left( \frac{|E_R|}{|E|} = \frac{1}{\sqrt{[1 + (\omega/\omega_0)^2]}} = \frac{1}{\sqrt{1+4}} \cong \frac{1}{2} \right)$$

or  $6db$  ( $20 \log_{10} \left( \frac{1}{2} \right) = -20 \log_{10} 2 = -6db$ ). In other words the gain rolls off beyond cutoff at the rate of  $20db/decade$  or  $6db/octave$ ; octave signifies a two fold increase in frequency.

The phase relation between the input and the output may be obtained from the equation (3.19) as:  $\angle E_R = \angle E - \tan^{-1} \left( \frac{\omega L}{R} \right)$  or the phase difference between the output and input is given by:

<sup>1</sup> For more details please see appendix – I.

$$\theta = -\tan^{-1}\left(\frac{\omega L}{R}\right) = -\tan^{-1}(\omega/\omega_0)$$

The graph plotted between  $\theta$  and  $\omega$ , known as phase response curve is shown in figure (3.10b). From this curve it is clear that the phase difference is equal to  $(-\frac{\pi}{4})$  at the cutoff frequency.

**3.4 R – C Low pass filter:** Low pass filter can also be designed using the series combination of resistance R and capacitance C as shown in figure (3.11).

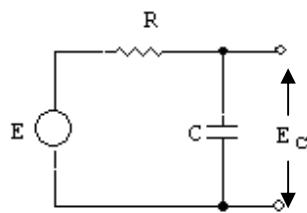


Fig. 3.11

The output voltage is taken across the capacitance  $C$ , which is given by:

$$E_C = \frac{E(1/j\omega C)}{(R + \frac{1}{j\omega C})} = \frac{E}{(1 + j\omega CR)}$$

The value of  $CR$  has the dimension of time and is represented by  $\tau$ .

$$\text{So } \frac{E_C}{E} = \frac{1}{(1 + j\omega\tau)} \quad \text{or} \quad \left| \frac{E_C}{E} \right| = \frac{1}{\sqrt{(1 + \omega^2\tau^2)}} \quad \text{----- (3.21)}$$

This equation is identical with equation (3.20), hence frequency response and phase response curves will be the same as that of R-L low pass filter. This circuit is therefore called as R – C low pass filter. The cut off frequency is given by:

$$\omega_0 = \frac{1}{\tau} = \frac{1}{CR} \text{ radians/sec} \quad \text{or} \quad f_0 = \frac{1}{2\pi CR} \text{ Hz.}$$

The phase difference between the output and input is given by:

$$\theta = -\tan^{-1}(\omega\tau) = -\tan^{-1}(\omega CR) = -\tan^{-1}(\omega/\omega_0)$$

$$\text{So at } \omega = \omega_0 \quad \theta = (-\pi/4).$$

**Example 3.8** Find the value of capacitance in the RC low pass filter to obtain the cut off frequency of  $1.5 \text{ KHz}$ . The value of the resistance is given as  $R = 2 \text{ K}\Omega$ .

Solution: The cut off frequency is given by  $f_0 = \frac{1}{2\pi RC}$

$$\text{or } C = \frac{1}{2\pi Rf_0} = \frac{1}{2 \times 3.14 \times 1500 \times 2000} = \frac{10^{-6}}{18.84} = .05 \mu F$$

**3.5 R – L High pass filter:** A series combination of a resistance and an Inductance L can also act as High pass filter if the output voltage is taken across inductance in place of resistance as shown in figure (3.12).

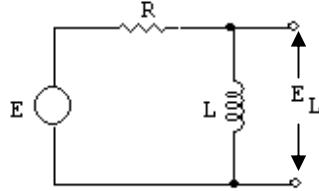


Fig. 3.12

The output voltage across the inductance  $L$  is given by:

$$E_L = \frac{E \cdot (j\omega L)}{(R + j\omega L)} = \frac{E \left( \frac{j\omega L}{R} \right)}{\left( 1 + \frac{j\omega L}{R} \right)} \quad \text{or} \quad \frac{E_L}{E} = \frac{(j\omega \tau)}{(1 + j\omega \tau)} \quad \dots\dots (3.22)$$

as  $L/R$  has the dimension of time denoted by  $\tau$ .

$$\text{So} \quad \left| \frac{E_L}{E} \right| = \frac{|E| \cdot (\omega \tau)}{\sqrt{(1 + \omega^2 \tau^2)}} \quad \text{or} \quad \frac{|E_L|}{|E|} = \frac{\omega \tau}{\sqrt{(1 + \omega^2 \tau^2)}} \quad \dots\dots (3.23)$$

Now a graph between  $\left| \frac{E_L}{E} \right|$  and the frequency  $\omega$  is plotted as shown in figure (3.13a). From this graph it is clear that if the input frequency is high enough then the output of the circuit will be almost the same as the input signal; and if the frequency of the input signal is low enough then the output is attenuated i.e. only a small amount of input reaches at the output. Hence the circuit behaves like a high pass filter. This circuit can be used to detect a signal of high frequency from the low frequency noise. Its behaviour may also be explained if the reactance of the inductance is considered. It offers low reactance at low frequency and acts as an on switch, thus the output across the inductance is almost negligibly small. However, it offers high reactance for the high frequency, the output works like an open circuited and the output is same as the input.

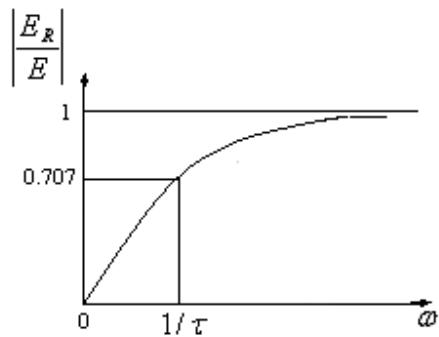
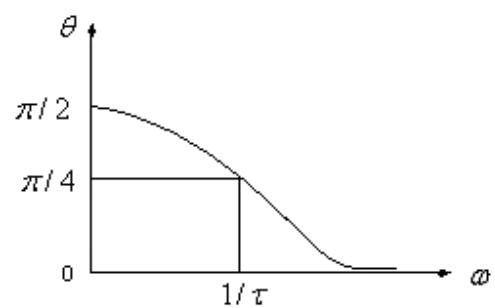


Fig. 3.13 (a)



(b)

In the equation (3.23), if we put  $\omega = \frac{1}{\tau} = \frac{R}{L}$  then  $\left| \frac{E_L}{E} \right|$  will be equal to  $\frac{1}{\sqrt{2}}$  or 0.707, which is known as higher cutoff frequency  $\omega_0$  or -3db point. It can be shown that the gain of this circuit increases at the rate of 20db/decade below the cut off frequency.

At the cut off frequency  $\left| \frac{E_L}{E} \right|$  is given by:

$$\left| \frac{E_L}{E} \right| = \frac{(\omega/\omega_0)}{\sqrt{[1+(\omega/\omega_0)^2]}} = \frac{(f/f_0)}{\sqrt{[1+(f/f_0)^2]}} \quad \text{----- (3.24)}$$

The phase relation between the input and the output may be obtained from the equation (3.19) as:  $\angle E_L = \angle E + \frac{\pi}{2} - \tan^{-1}(\frac{\omega L}{R})$  or the phase difference between the output and input is given by:

$$\theta = \frac{\pi}{2} - \tan^{-1}(\frac{\omega L}{R}) = \frac{\pi}{2} - \tan^{-1}(\omega/\omega_0) = \frac{\pi}{2} - \tan^{-1}(f/f_0)$$

The graph plotted between  $\theta$  and  $\omega$ , known as phase response curve is shown in figure (3.13 b). From this curve it is clear that the phase difference is equal to  $\frac{\pi}{4}$  at the cutoff frequency.

**3.6 R – C High pass filter:** High pass filter may also be designed using the series combination of resistance R and capacitance C as shown in figure (3.14).

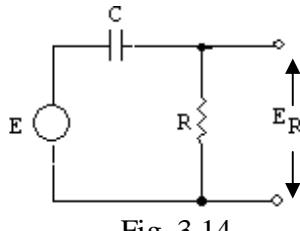


Fig. 3.14

The output voltage is taken across the resistance R, which is given by:

$$E_R = \frac{E.R}{(R + \frac{1}{j\omega C})} = \frac{E.j\omega CR}{(1 + j\omega CR)}$$

The value of CR has the dimension of time and is represented by  $\tau$ .

So  $\frac{E_R}{E} = \frac{j\omega\tau}{(1 + j\omega\tau)}$  or  $\left| \frac{E_R}{E} \right| = \frac{\omega\tau}{\sqrt{(1 + \omega^2\tau^2)}}$  ----- (3.25)

This equation is identical with equation (3.23), hence frequency response and phase response curves will be the same as that of R-L High pass filter. This circuit is,

therefore, called as R – C High pass filter. The cut off frequency is given by:

$$\omega_0 = \frac{1}{\tau} = \frac{1}{CR} \text{ radians/sec or} \quad f_0 = \frac{1}{2\pi CR} \text{ Hz.}$$

The phase difference between the output and input is given by:

$$\theta = \frac{\pi}{2} - \tan^{-1}(\omega\tau) = \frac{\pi}{2} - \tan^{-1}(\omega/\omega_0) = \frac{\pi}{2} - \tan^{-1}(f/f_0)$$

**3.7 Band Pass Filter or Series R – L – C Circuit:** Series combination of R, L, & C elements connected to an A.C. signal as shown in figure (3.15) behaves as Band pass filter.

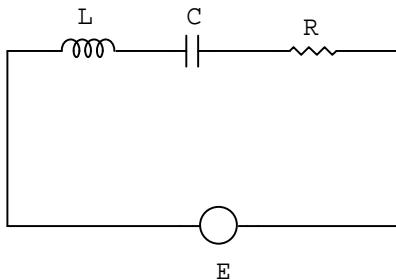


Fig. 3.15

The impedance of the circuit is given by:

$$Z = R + j\omega L + \frac{1}{j\omega C} = R + j(\omega L - \frac{1}{\omega C}) \quad \text{----- (3.26)}$$

The series R-L-C circuit is said to resonant if the current and voltage are in the same phase. This is possible when the impedance becomes purely resistive or reactive components are zero.

$$\begin{aligned} \text{i.e.} \quad \omega L - \frac{1}{\omega C} &= 0 \quad \text{or} & \omega L &= \frac{1}{\omega C} \\ \omega^2 &= \frac{1}{LC} \quad \text{or} & \omega &= \frac{1}{\sqrt{LC}} \end{aligned}$$

This frequency is known as resonance frequency denoted by  $\omega_0 = \frac{1}{\sqrt{LC}}$  or  $f_0 = \frac{1}{2\pi\sqrt{LC}}$ . So one may say that at resonance frequency the impedance is minimum (resistive), consequently the current in the circuit is maximum, i.e.  $I_{\max} = \frac{E}{R}$ . At frequency lower than the resonance frequency, the capacitive reactance is large compared

to the inductive reactance ( $\frac{1}{\omega C} > \omega L$ ) and thus total reactance is capacitive in nature. At frequency higher than the resonance frequency, inductive reactance is large compared to the capacitive reactance ( $\omega L > \frac{1}{\omega C}$ ) and the circuit is inductive. The current flowing through the series R – L – C circuit is given by:

$$I = \frac{E}{R + j(\omega L - \frac{1}{\omega C})} = \frac{E \cdot j \omega C}{(1 - \omega^2 LC) + j \omega CR} \quad \text{----- (3.27)}$$

$$|I| = \frac{|E| \omega C}{\sqrt{(1 - \omega^2 LC)^2 + \omega^2 C^2 R^2}} \quad \text{----- (3.28)}$$

The phase relation between voltage and current is given by:

$$\theta = \angle I - \angle E = \frac{\pi}{2} - \tan^{-1} \left[ \frac{\omega CR}{(1 - \omega^2 LC)} \right] \quad \text{----- (3.29)}$$

The frequency and phase response curve are shown in figure (3.16).

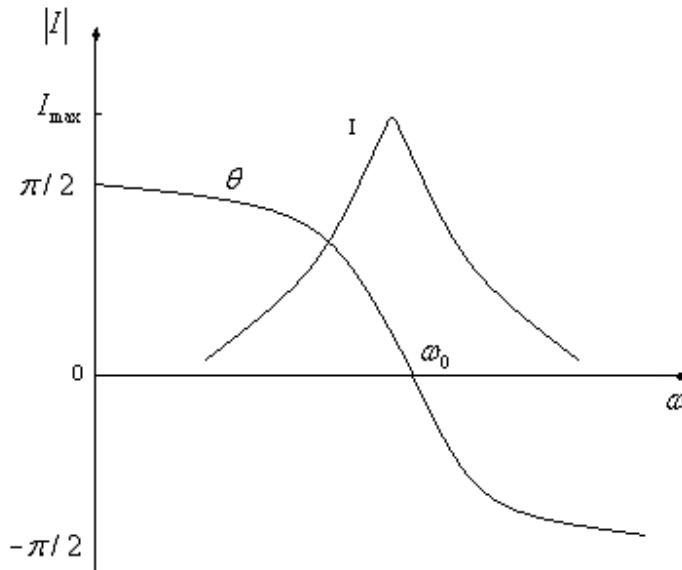


Fig. 3.16

From this figure it is clear that the current is maximum at the resonant frequency  $\omega_0$ , it decreases in the similar fashion on either side of the resonant frequency  $\omega_0$ . The circuit therefore, acts as band pass filter if we consider the voltage as the input and the current as the output. When the frequency is equal to  $\omega_1$  or  $\omega_2$ , then the current is  $\frac{I_{\max}}{\sqrt{2}} = \frac{E}{\sqrt{2}R}$ .

Thus 
$$\frac{E}{\sqrt{R^2 + \left[ \omega L - \frac{1}{\omega C} \right]^2}} = \frac{E}{\sqrt{2}R} \quad \text{----- (3.30)}$$

or 
$$\sqrt{R^2 + \left[ \omega L - \frac{1}{\omega C} \right]^2} = \sqrt{2}R \quad \text{----- (3.31)}$$

or 
$$R^2 + \left[ \omega L - \frac{1}{\omega C} \right]^2 = 2R^2$$

or 
$$\left[ \omega L - \frac{1}{\omega C} \right]^2 = R^2$$

or 
$$\left[ \omega L - \frac{1}{\omega C} \right] = \pm R \quad \text{----- (3.32)}$$

since  $\omega_2 > \omega_1$ , then 
$$\left[ \omega_1 L - \frac{1}{\omega_1 C} \right] = -R \quad \text{----- (3.33)}$$

and 
$$\left[ \omega_2 L - \frac{1}{\omega_2 C} \right] = R \quad \text{----- (3.34)}$$

Adding equations (3.33) & (3.34) we get 
$$(\omega_1 + \omega_2)L - \frac{1}{C} \left( \frac{\omega_1 + \omega_2}{\omega_1 \omega_2} \right) = 0$$

or 
$$\omega_1 \omega_2 = \frac{1}{LC}$$

Subtracting equation (3.33) from (3.34), one may get:

$$(\omega_2 - \omega_1)L + \frac{1}{C} \left( \frac{\omega_2 - \omega_1}{\omega_1 \omega_2} \right) = 2R$$

or 
$$(\omega_2 - \omega_1) \left( L + \frac{1}{C \omega_1 \omega_2} \right) = 2R$$

or 
$$(\omega_2 - \omega_1) \cdot 2L = 2R \quad \text{or} \quad (\omega_2 - \omega_1) \cdot \frac{R}{L} \quad \text{----- (3.35)}$$

$\omega_2 - \omega_1$  is known as the Band Width ( $\Delta\omega$ ) and is the band of frequency which lies between two points of either side of resonant frequency where the current falls to  $\frac{1}{\sqrt{2}}$  of its resonant value.

The Q-factor of this series circuit is 
$$Q = \frac{\omega_0 L}{R} \quad \text{----- (3.36)}$$

From equations (3.35) & (3.36), we have 
$$Q = \frac{\omega_0}{(\omega_2 - \omega_1)}$$

$$\text{or} \quad Q = \frac{\omega_0}{\Delta\omega} \quad \text{or} \quad Q = \frac{f_0}{\Delta f} \quad \text{----- (3.37)}$$

From this equation it is clear that greater is the value of quality factor  $Q$ , smaller is the bandwidth and more sharper is the resonance.

**3.8 Band Rejection Filter or Parallel R – L – C Circuit:** The parallel combination inductance  $L$  having a small leakage resistance  $R$  and capacitance  $C$  connected to an A.C. signal as shown in figure (3.17), forms a band rejection filter.

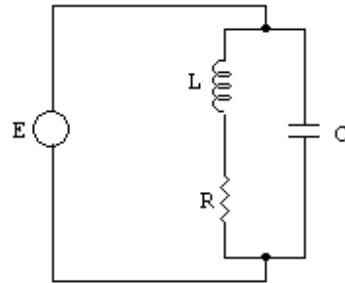


Fig. 3.17

The impedance of this circuit is given by:

$$Z = \frac{(R + j\omega L) \cdot \left(\frac{1}{j\omega C}\right)}{\left[R + j\omega L + \frac{1}{j\omega C}\right]} = \frac{(R + j\omega L)}{\left[(1 - \omega^2 LC) + j\omega RC\right]} \quad \text{----- (3.38)}$$

The inductance  $L$  may assume to be of high quality factor, so  $\omega L \gg R$  and the impedance is approximated as:

$$Z = \frac{j\omega L}{\left[(1 - \omega^2 LC) + j\omega RC\right]} \quad \text{----- (3.39)}$$

$$|Z| = \frac{\omega L}{\sqrt{\left[(1 - \omega^2 LC)^2 + \omega^2 R^2 C^2\right]}} \quad \text{----- (3.40)}$$

The impedance of the circuit will be maximum and purely resistive if:

$$1 - \omega^2 LC = 0 \quad \text{or} \quad \omega = \frac{1}{\sqrt{LC}} = \omega_0$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad \text{----- (3.41)}$$

The circuit is said to be in resonance and  $\omega_0$  is called as resonance frequency. The impedance at resonance frequency is  $L/CR$  which is infinite for ideal inductance.

The current flowing through the parallel circuit will be small at resonance frequency and it increases on either side of the resonance frequency as shown in figure (3.18).

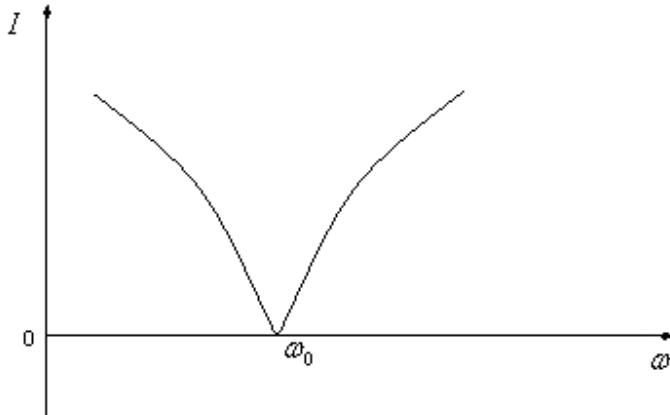


Fig. 3.18

It is clear from this figure that the circuit eliminates a particular band of frequency hence the name band rejection filter. At two frequencies  $\omega_1$  and  $\omega_2$  on either side of the resonance frequency, the magnitude of the impedance is  $(1/\sqrt{2})$  times the impedance at resonance frequency.

$$\begin{aligned} \text{i.e. } & \frac{\omega L}{\sqrt{(1-\omega^2 LC)^2 + \omega^2 C^2 R^2}} = \frac{L}{\sqrt{2} CR} \\ \text{or } & \sqrt{(1-\omega^2 LC)^2 + \omega^2 C^2 R^2} = \sqrt{2} \omega CR \\ \text{or } & (1-\omega^2 LC)^2 + \omega^2 C^2 R^2 = 2\omega^2 C^2 R^2 \\ \text{or } & 1 - \omega^2 LC = \omega CR \end{aligned} \quad \text{----- (3.42)}$$

This quadratic equation may be solved for  $\omega$  which will have two roots given by:

$$\omega_1 = \left[ \frac{1}{\sqrt{LC}} \right] - \frac{R}{2L} \quad \text{and} \quad \omega_2 = \left[ \frac{1}{\sqrt{LC}} \right] + \frac{R}{2L}$$

$$\text{The band width} \quad \Delta\omega = \omega_2 - \omega_1 = \frac{R}{L}$$

The quality factor  $Q$  of the circuit is given by

$$Q = \frac{\omega_0}{\Delta\omega} = \frac{\omega_0 L}{R} = \frac{1}{\sqrt{LC}} \cdot \frac{L}{R} = \sqrt{\frac{L}{C} \cdot \frac{1}{R}}$$

**Example 3.9** Calculate the Q-factor and the Band width of the Band Rejection filter (Parallel Resonant Circuit). Given  $L = 200 \text{ mH}$ ,  $R = 20 \Omega$  and  $C = 100 \text{ pf}$ .

Solution: The resonance frequency  $f_0$  is given by:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$\begin{aligned}
&= \frac{1}{2 \times 3.14 \times \sqrt{200 \times 10^{-3} \times 100 \times 10^{-12}}} = \frac{1}{6.28 \times \sqrt{20 \times 10^{-12}}} \\
&= \frac{10^6}{6.25 \times 4.47} = 35.6 \text{ KHz}
\end{aligned}$$

The quality factor  $Q$  is given by:

$$\begin{aligned}
Q &= \frac{\omega_0 L}{R} = \frac{2 \times 3.14 \times 35.6 \times 10^3 \times 200 \times 10^{-3}}{20} \\
&= 20 \times 3.14 \times 35.6 = 2240
\end{aligned}$$

Band width  $BW$

$$BW = \frac{f_0}{Q} = \frac{35.6 \times 10^3}{2240} = 15.9 \text{ Hz}$$

**3.9 Transient Response:** when an inductance or a capacitor is connected to a d.c. source, the inductance or capacitor starts charging and the voltage or current is build up gradually in the element. Ultimately it attains the steady state. Now when the source is switched off, the current or voltage stored in the elements gradually decreases. The process of gradually increasing and decreasing of the current or voltage in the inductance or capacitance is known as the transient response of the circuit. We shall now study the transient response of R – C and R – L circuits.

**3.9.1 Transient Response of R – C circuit:** Let us consider a circuit consisting of a resistance  $R$  and a capacitance  $C$  connected to a d.c. source through a SPDT switch as shown in figure (3.19). The switch has two positions such that when it is thrown to position  $A$  as shown in figure (3.19a) the capacitor starts charging through  $R$  with the source  $E$ . When the switch is thrown to position  $B$  as shown in figure (3.19b) the capacitor starts discharging.



Fig. 3.19 (a)

(b)

**(i) Charging of Capacitance:** Initially the switch is thrown to position  $A$ , the capacitor will start charging through  $R$ . The current  $I$  flowing through the circuit is given by:

$$I = \frac{dq}{dt}$$

Applying the KVL to the circuit we get:

$$RI + \frac{q}{C} = E \quad \text{or} \quad R \frac{dq}{dt} + \frac{q}{C} = E$$

$$\text{or } R \frac{dq}{dt} = E - \frac{q}{C} \quad \text{or } dt = \frac{Rdq}{E - \frac{q}{C}} = -RC \frac{-(1/C) dq}{E - \frac{q}{C}}$$

Integrating on both sides  $\int dt = -RC \int \frac{-(1/C) dq}{E - \frac{q}{C}}$

$$\text{or } t = -RC \ln(E - \frac{q}{C}) + A \quad \text{----- (3.43)}$$

where  $A$  is a constant of integration, its value may be obtained from the initial conditions.

At time  $t = 0$ ,  $q = 0$  so  $A = RC \ln E$  ----- (3.44)

From equation (3.43) and (3.44),  $t = -RC \ln(E - \frac{q}{C}) + RC \ln E$

$$\text{or } t = -RC \ln \left( \frac{E - \frac{q}{C}}{E} \right) \quad \text{or} \quad -\frac{t}{RC} = \ln \left( \frac{E - \frac{q}{C}}{E} \right)$$

$$\text{or } \left( \frac{E - \frac{q}{C}}{E} \right) = e^{-t/RC} \quad \text{or} \quad q = CE(1 - e^{-t/RC}) = q_0(1 - e^{-t/RC})$$

(Where  $q_0$  is the maximum charge, the capacitor can attain;  $q_0 = CE$ )

$$\begin{aligned} \text{The current } I \text{ is given by: } I &= \frac{dq}{dt} = \frac{d}{dt} [q_0(1 - e^{-t/RC})] \\ &= \frac{q_0}{RC} \cdot e^{-t/RC} = \frac{E}{R} e^{-t/RC} = I_0 e^{-t/RC} \end{aligned} \quad \text{----- (3.45)}$$

where  $I_0 = \frac{E}{R}$ , is the maximum or initial value of current.

At time  $t = 0$ ,  $I = I_0$

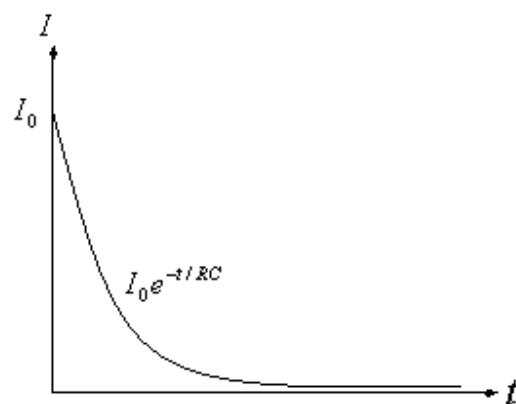


Fig. 3.20

and at  $t = \infty$ ,  $I = 0$ . Figure (3.20) shows the transient response of R – C circuit, the current during the charging of capacitor  $C$ .

**(ii) Discharging of Capacitance:** After charging the capacitor, the switch is thrown to position  $B$  as shown in figure (3.19b). The capacitor will start discharging through resistance  $R$ .

Now applying the KVL to the circuit we get:  $RI + \frac{q}{C} = 0$

$$\text{or } R \frac{dq}{dt} + \frac{q}{C} = 0 \quad (\text{since } I = \frac{dq}{dt})$$

$$\text{or } \frac{dq}{q} = \frac{-dt}{RC} \quad \text{or} \quad \int \frac{dq}{q} = \int \frac{-dt}{RC} \quad \dots\dots\dots (3.46)$$

$$\text{or } \ln q = \frac{-t}{RC} + B \quad \dots\dots\dots (3.47)$$

(Where  $B$  is a constant of Integration which may be obtained from the initial conditions)

$$\text{At } t = 0, q = q_0 \text{ and thus} \quad B = \ln q_0 \quad \dots\dots\dots (3.48)$$

$$\text{From equations (3.47) \& (3.48) it is obtained : } \ln q = \frac{-t}{RC} + \ln q_0$$

$$\ln \frac{q}{q_0} = \frac{-t}{RC} \quad \text{or} \quad q = q_0 e^{-t/RC} \quad \dots\dots\dots (3.49)$$

$$\text{The current } I \text{ is given by: } I = \frac{dq}{dt} = \frac{d}{dt} [q_0 \cdot e^{-t/RC}] = \frac{-E}{R} e^{-t/RC}$$

$$\text{or} \quad I = -I_0 e^{-t/RC} \quad \dots\dots\dots (3.50)$$

where  $I_0 = E/R$  is the initial value of current, at  $t = 0, I = -I_0$  and at  $t = \infty, I = 0$ . Figure (3.21) shows the transient response of R – C circuit, the current during the discharging of capacitor  $C$ .

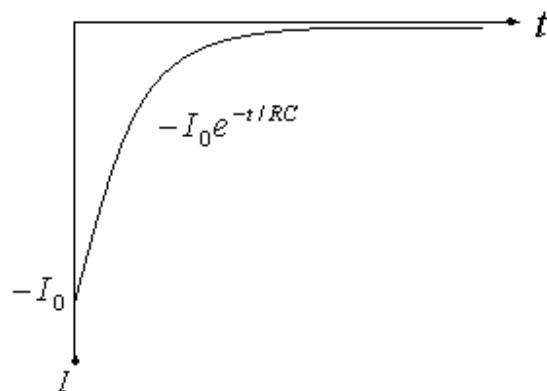


Fig. 3.21

**3.9.2 Transient Response of R – L circuit:** Let us consider a circuit consisting of a resistance  $R$  and an inductance  $L$  connected to a d.c. source through a SPDT switch as shown in figure (3.22). The switch has two positions such that when it is thrown to position  $A$  as shown in figure 3.22 a,

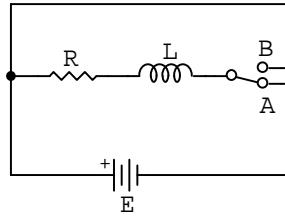
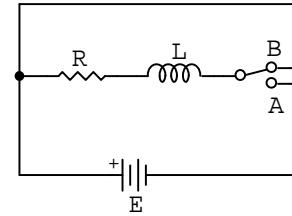


Fig. 3.22 (a)



(b)

the source  $E$  gets connected to the series combination of resistance and inductance  $L$ . When the switch is thrown to position  $B$  as shown in figure (3.22b), the current induced in the coil decays through the resistance.

**(i) Rising of current:** Initially the switch is thrown to position  $A$ , the current starts to flow and a flux is induced in the coil. The induced e.m.f. in the coil opposes the rising of the current in the coil. The current  $I(t)$  thus in the coil attain its steady value gradually. Applying KVL to the circuit we get:

$$\begin{aligned} L \frac{dI(t)}{dt} + RI(t) &= E \\ \text{or } L \frac{dI}{dt} &= E - RI \quad \text{or} \quad \frac{dI}{E - RI} = \frac{dt}{L} \quad \text{----- (3.51)} \\ \text{or } \int \frac{dI}{E - RI} &= \int \frac{dt}{L} \text{ or} \quad -\frac{1}{R} \ln(E - RI) = -\frac{t}{L} + A \end{aligned}$$

where  $A$  is a constant of Integration which may be obtained from the initial conditions;

$$\text{at } t = 0, I = 0 \quad \text{and} \quad A = \frac{-1}{R} \ln E \quad \text{----- (3.52)}$$

From equations (3.51) and (3.52) we get:

$$\begin{aligned} -\frac{1}{R} \ln(E - RI) &= -\frac{t}{L} - \frac{1}{R} \ln E \quad \text{or} \quad \ln \frac{(E - RI)}{E} = -\frac{R}{L} t \\ \text{or } \frac{RI}{E} &= 1 - e^{-\frac{R}{L} t} \quad \text{or} \quad I = \frac{E}{R} \left( 1 - e^{-\frac{R}{L} t} \right) \\ I &= I_0 \left( 1 - e^{-\frac{R}{L} t} \right) \quad \text{----- (3.53)} \end{aligned}$$

$I_0$  is the maximum value of current which is equal to  $\frac{E}{R}$ . The rising of the current in the inductance is shown in figure (3.23).

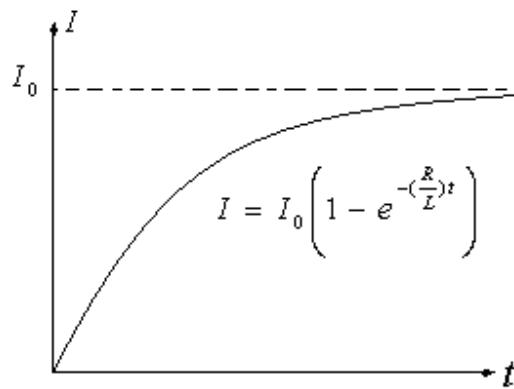


Fig. 3.23

**(ii) Decay of current:** After attaining the maximum value of current  $I_0 = \frac{E}{R}$ , the switch is thrown to position B as shown in figure (3.22 b). The current  $I$  in the circuit will decay from maximum value to zero. The equation (3.51) may be written as:

$$\begin{aligned} L \frac{dI(t)}{dt} + RI(t) &= 0 \\ \text{or} \quad L \frac{dI}{dt} &= -RI \quad \text{or} \quad \frac{dI}{I} = -\frac{R}{L} dt \quad \text{----- (3.54)} \\ \text{or} \quad \int \frac{dI}{I} &= -\int \frac{R}{L} dt \quad \text{or} \quad \ln I = -\frac{R}{L} t + B \end{aligned}$$

$B$  is a constant of Integration which may be obtained from the initial conditions; at  $t = 0$ ,  $I = I_0$  and  $B = \ln I_0$  ----- (3.55)

$$\text{or} \quad \ln I = -\frac{R}{L} t + \ln I_0 \quad \text{or} \quad \ln \frac{I}{I_0} = -\frac{R}{L} t$$

$$\text{or} \quad I = I_0 e^{-\left(\frac{R}{L}\right)t} \quad \text{----- (3.56)}$$

The decay of current is shown in figure (3.24).

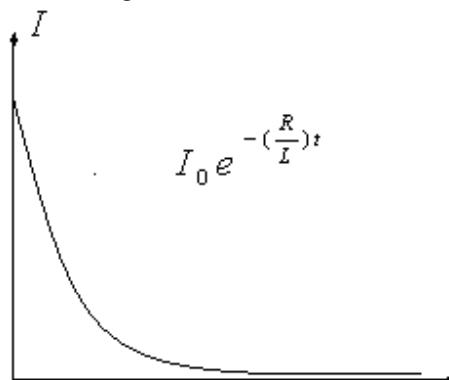


Fig. 3.24

**Example 3.10** An inductance of 10 Henry and resistance 20  $\Omega$  is connected to d.c. signal of 20 volts. Calculate (i) steady current in the circuit, (ii) the rate of change of current at the instant of closing the circuit and (iii) time to get the 90% of the steady current.

Solution: The current in the R – L circuit is given by:

$$I = I_0 \left( 1 - e^{-\left(\frac{R}{L}\right)t} \right)$$

(i) The steady state current  $I_0 = \frac{E}{R} = \frac{20}{20} = 1 \text{ amp.}$

(ii)  $\frac{dI}{dt} = \frac{R}{L} e^{-(R/L)t}$  and  $\left. \frac{dI}{dt} \right|_{t=0} = \frac{R}{L} \cdot e^{-0} = \frac{20}{10} = 2 \text{ amp/sec}$

(iii)  $R/L = 20/10 = 2$

$$0.9I_0 = I_0 \left( 1 - e^{-\left(\frac{R}{L}\right)t} \right)$$

$$\begin{aligned} 0.9 &= 1 - e^{-2t} & \text{or} & \quad e^{-2t} = 0.1 \\ e^{2t} &= 10 & \text{or} & \quad 2t = \ln(10) \end{aligned}$$

$$t = \frac{\ln(10)}{2} = \frac{2.30}{2} = 1.15 \text{ Sec}$$

**3.10 Differentiating and Integrating Circuit:** Differentiation and Integration with respect to time are the important operations of signal processing. Capacitance and Inductance may perform these operations if we define input and output variables properly. Capacitance is generally used for these operations as practical inductors have some resistance. We shall, therefore, discuss R – C differentiating and integrating circuits.

**3.10.1 R – C Differentiating Circuit:** Consider a capacitance  $C$  is charged with a voltage source  $E_I$ , then the current flowing through the capacitance is given by:

$$I = C \left( \frac{dE_I}{dt} \right) \quad \text{----- (3.57)}$$

This equation clearly indicates that the current forms the differentiation of

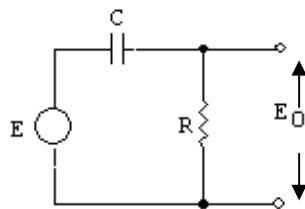


Fig. 3.25

To measure the current a resistance  $R$  is connected in series with the capacitance  $C$  as shown in figure (3.25). The voltage across the resistance is proportional to the

differentiation of the input signal which can be given by:

$$E_0 = RI = RC \left( \frac{dE_I}{dt} \right) \quad \text{----- (3.58)}$$

This circuit may thus be called as the differentiating circuit. The R – C Differentiating Circuit is identical with the R – C high pass filter.

**3.10.2 R – C Integrating Circuit:** When a current  $I$  is passed through a capacitance, then the voltage across the capacitance  $E_0$  is given by:

$$E_0 = \frac{1}{C} \int Idt \quad \text{----- (3.59)}$$

This voltage is proportional to the integration of the input current  $I$ . Now we consider the R – C network as shown in figure (3.26a), a signal  $E$

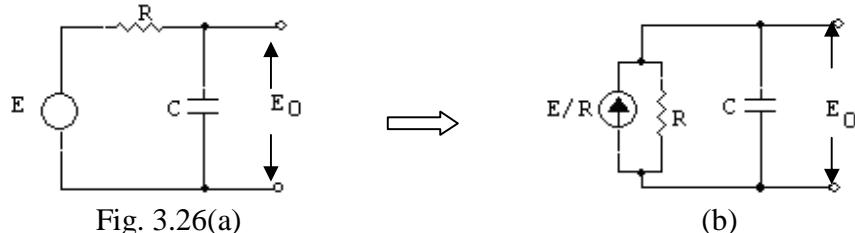


Fig. 3.26(a)

(b)

is applied to the input terminals and voltage  $E_0$  is measured across the capacitance  $C$ . The input signal  $E$  is converted to the current source  $I$  (conversion of Thevenin's equivalent to Norton's equivalent). The current  $I$  is given by:  $I = E/R$

$$\text{So} \quad E_0 = \frac{1}{C} \int \left( \frac{E}{R} \right) dt = \frac{1}{RC} \int Edt \quad \text{----- (3.60)}$$

The equation (3.60) clearly indicates that the output voltage across the capacitance is proportional to the input voltage  $E$ . Hence this circuit is called as an Integrator. The integrator circuit is identical to the R – C low pass filter.

### Problems:

1. Prove that the Fourier Series expansion of the half wave rectified output is given by:

$$E = \frac{E_m}{\pi} + \frac{E_m}{2} \sin \omega t - \frac{2E_m}{3\pi} \cos 2\omega t - \frac{2E_m}{15\pi} \cos 4\omega t - \frac{2E_m}{35\pi} \cos 6\omega t \dots \dots$$

where  $f(t) = E_m \sin \omega t$  when  $0 \leq t \leq T/2$

$f(t) = 0$  when  $(T/2) \leq t \leq T$

2. Prove that the Fourier Series expansion of the Full wave rectified output is given by:

$$E = \frac{2E_m}{\pi} - \frac{4E_m}{3\pi} \cos 2\omega t - \frac{4E_m}{15\pi} \cos 4\omega t - \frac{4E_m}{35\pi} \cos 6\omega t \dots \dots$$

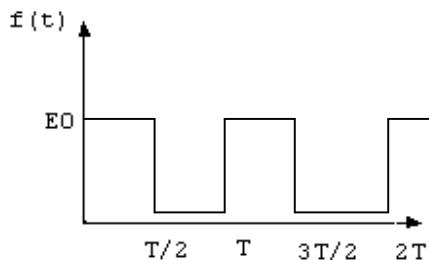
where  $f(t) = E_m \sin \omega t$  when  $0 \leq t \leq T/2$

$$f(t) = -E_m \sin \omega t \quad \text{when } (T/2) \leq t \leq T$$

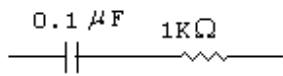
3. Consider a symmetrical triangular wave of peak value  $E_m$  and period  $T$ . Show that the Fourier Series expansion of the wave is given by:

$$E = \frac{E_m}{2} - \frac{E_m}{\pi} \sin \omega t - \frac{E_m}{2\pi} \sin 2\omega t - \frac{E_m}{3\pi} \sin 3\omega t \dots$$

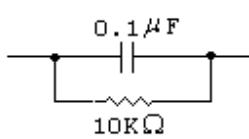
4. Find the Fourier series expansion of the square wave shown in figure given below.



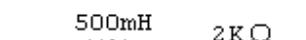
5. Discuss (i) R – L low pass filter, (ii) R – C Low pass filter. Draw the frequency and phase response curves of these filters. Find the expression of cut-off frequency in each case.
6. Discuss (i) R – L High pass filter, (ii) R – C High pass filter. Draw the frequency and phase response curves of these filters. Find the expression of cut-off frequency in each case.
7. Explain the working of R – C integrator circuit.
8. Explain the working of R – C differentiator circuit.
9. Show that the output across the resistance in an R – C circuit is the differential of the input signal.
10. Show that the output across the capacitance in an R – C circuit is the integration of the input signal.
11. Discuss the transient response of an R – C circuit.
12. Discuss the transient response of an R – L circuit.
13. Show that the series R – L – C circuit behaves as a band pass filter. Draw the frequency and phase response curve of this series circuit. Find the expression for the band width also.
14. Show that the parallel R – L – C circuit behaves as a band rejection filter. Draw its frequency and phase response curve. Find the expression for the band width also.
15. Find the impedances of the following network at 1 KHz frequency.



(a)



(b)



(c)

Ans.(a)  $1.88K\Omega \angle -57.9^\circ$ , (b)  $8.48K\Omega \angle -32.13^\circ$ , (c)  $3.72K\Omega \angle 57.5^\circ$

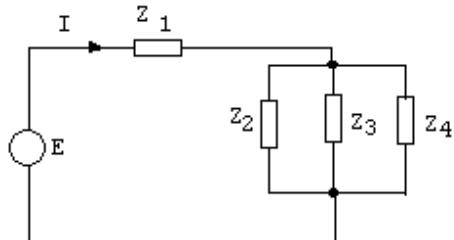
16. Three impedances  $Z_1 = 125\angle -38^\circ$ ,  $Z_2 = 213.5\angle 62^\circ$  and  $Z_3 = 83\angle 54.5^\circ$  are connected in series. What is the total impedance of the circuit?

Ans.  $305\Omega\angle -36^\circ$

17. A series R L circuit is excited by an sinusoidal voltage of magnitude 20volts and frequency 1.5KHz. If  $R = 2\Omega$  and  $L = 200 \text{ mH}$ . Find the magnitude and phase of the current flowing through the circuit.

Ans.  $7.2mA\angle -43.29^\circ$

18. Consider the circuit shown in figure given below, in which  $Z_1 = 14.4\angle 45^\circ$ ,  $Z_2 = 25\angle 53.1^\circ$ ,  $Z_3 = 5\angle -53.1^\circ$  &  $Z_4 = 10\angle 36.9^\circ$ . Find (i) the impedance of the circuit, (ii) total amount of current drawn if the signal E is of 10 volts source, (iii) phase of the current I with respect to the applied voltage.



Ans.:  $16.6\Omega\angle 31.87^\circ$ ,  $0.6\text{amp}$ , phase angle  $-31.87^\circ$

19. A series RLC circuit is excited by a sinusoidal signal  $E = E_m \sin \omega t$ .  $R = 20\Omega$ ,  $L = 20\text{mH}$ ,  $C = 0.2\mu\text{F}$ ,  $E_m = 20$  volts and  $\omega = 2 \times 10^4$  radians/sec. Find the magnitude and phase of the current.

Ans.  $I = 53.3mA\angle -86.9^\circ$

20. An inductor of  $200 \text{ mH}$  and resistance  $2\Omega$  is connected to a d.c. source. Calculate the time in which the current attains half of its steady current after making the circuit.

Ans.  $0.0693 \text{ Sec}$

21. A series LCR circuit has the following parameters; Quality factor  $Q = 120$ ,  $C = 200 \mu\text{F}$ ,  $L = 150 \mu\text{H}$ . Calculate the Band width.

Ans.  $7.7 \text{ KHz}$

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# 4

# Physics of Semiconductors

In this chapter the physical behaviour of semiconductors and semiconductor diodes has been discussed. Semiconductors have some useful properties and thus extensively being used in electronics. Semiconductor devices such as diodes, transistors, integrated circuits etc have brought a revolution in the modern world.

**4.1 Semiconductors:** The elements whose resistivity or conductivity lies in between that of the conductors and insulators are known as semiconductors. The resistivity of good conductor (such as copper) is approximately  $1.7 \times 10^{-8} \Omega m$  and that of insulator (Glass) is  $9 \times 10^{11} \Omega m$ . Germanium, Silicon, Selenium, Carbon etc has the resistivity  $10^{-4} \Omega m$  to  $10.5 \Omega m$ , which is quite high as compared to conductor (Copper) and is quite low as compared to insulator (glass). Hence these are known as semiconductors. The resistivity of the element is not the only factor which decides if the particular material is semiconductor. There are certain alloys which behave like the semiconductors i.e. their resistivity lies within the range of semiconductors. The alloys like Cadmium Sulphide (CdS), Lead Sulphide (PbS), Gallium arsenide (GaAs), etc are also semiconductors which are being used to fabricate the solid state devices.

Following are few of the essential characteristics of the semiconductors:

- (i) Semiconductors have negative temperature co-efficient of resistance that is, its resistivity decreases with the increase in temperature.
- (ii) The conductivity of the semiconductors can extensively be increased if the additional impurities of suitable metals are introduced in it.

The difference in behaviour of conductors, semiconductors and insulators can best be explained on the basis of energy band structure of solids. The range of energies possessed by an electron in a solid is known as band. The electron in the outer most orbit of an atom is known as valence electron. The energy band occupied by the valence electron is called as valence band. This band may be completely or partially filled. The valence band is the highest occupied band. The electrons which have left the valence band are called the conduction electrons and are weakly bound to the nucleus. The band occupied by these electrons is called the conduction band. Thus in the conduction band the electrons can move freely and will be responsible for the current flow. The conduction band is separated from the valence band by certain energy gap which has no allowed energy levels. This gap between the valence and the conduction band is known

as bad gap or forbidden gap. Figure (4.1) shows the energy band picture of insulators, conductors and semiconductors.

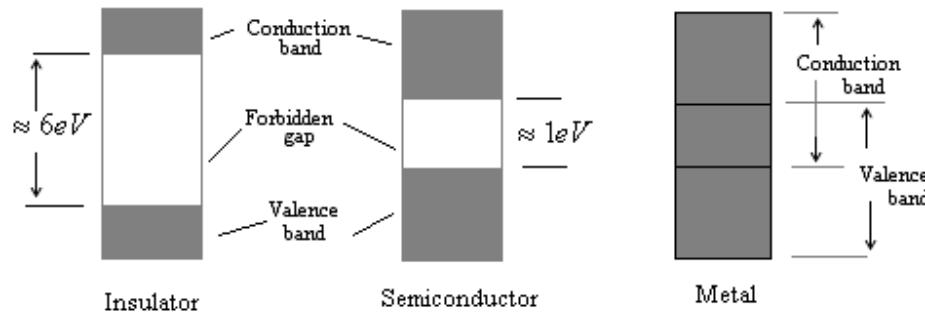


Fig. 4.1

It is clear from this figure that in case of insulators, there is a large forbidden gap between the valence and conduction bands. This band gap is of the order of several electron volts. In this case the valence band is full while the conduction band is empty. Therefore, a very high electric field is required for the electrons to move from valence band to conduction band. That is why the electrical conductivity of insulators is very poor.

In case of conductors the valence and conduction band overlap each other. Due to this overlapping a large number of free electrons are available in the conduction band and constitute an electric current. The conductors show the positive temperature coefficient of resistance i.e. the resistivity of the conductors increases with the increase of the temperature. This is because that the electrons are already in the conduction band and when the temperature of the conductors is increased; the electrons in the conduction band become thermally agitated and their energy is wasted in colliding with the other electrons in the conduction band.

The forbidden gap in case of semiconductors is of the order of one eV. Hence at room temperature some of the electrons in the valence band will have sufficient energy to jump from valence band to conduction band. In this way the conductivity of the semiconductors will be more than the insulators and smaller than the conductors. The semiconductors have almost full valence band and partially filled conduction band. The most commonly used semiconductors are germanium and silicon. The band gap energy of the germanium is 0.7 eV and 1.12 eV for silicon. The semiconductors show negative temperature coefficient of resistance; as the temperature is increased the more number of electrons will get into the conduction band which results the flow of current.

The semiconductors may be classified in to two categories:

- (i) Intrinsic Semiconductors
- (ii) Extrinsic or Doped Semiconductors

**4.1.1 Intrinsic Semiconductors:** Extremely pure form of a semiconductor is known as Intrinsic Semiconductor. The most commonly used semiconductors are Germanium and Silicon, which lies in the IV group of the periodic table. The atomic number of Germanium is 32, so it has 32 electrons, 2 electrons in the first orbit, 8 in the second orbit and 4 in the outer most orbit. Similarly the atomic number of Silicon is 14, and has 14 electrons; 2 electrons are in the first orbit, 8 electrons in the second orbit and 4 electrons in the outer most orbit. Both Germanium and Silicon have the crystalline structure.

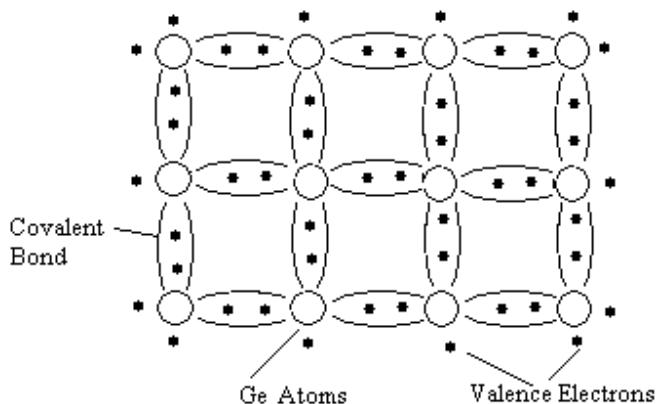


Fig. 4.2

Figure (4.2) shows that germanium (or silicon) atoms are held through covalent bonds. Each of the four electrons in a germanium (or silicon) atoms are shared by the valence electrons of four adjacent germanium (or silicon) atoms. The covalent bonds thus provide the binding force between the neighbouring atoms. The outer most orbits of atoms seem to be complete having 8 (shared) electrons. Consequently, the pure semiconductors (Ge or Si) behave as perfect insulator at  $0^0$  K. When the temperature is increased, some of the covalent bond is broken, the electrons are released and move to the conduction band. The empty space is left behind in the valence band. This empty space is known as hole and has the charge equal to that of an electron but opposite in sign. Thus each broken bond creates an electron-hole pair. The holes move through the crystal lattice in the random fashion as the free electrons and contribute to the current flow when an electric field is applied. Both these carriers drift in opposite directions giving rise to conventional current in the direction of flow of holes or in the direction opposite to the flow of electrons.

It is worthwhile to mention the following points with regards to the intrinsic semiconductor:

- (1) When a covalent bond breaks an electron – hole pair is created. So in an intrinsic semiconductor the number of electrons and number of holes are equal.
- (2) In the semiconductors the current flow is due to both the charge carriers unlike in the case of metals in which the current flow is only due electrons.

(3) At any finite temperature, some bonds break which result in the generation of electron – hole pairs and some bonds may be reforming. The process of remaking the bond is known as recombination. At a given temperature, an equilibrium will be setup between the generation of electron – hole pairs and recombination of them. The hole concentration  $p$  must be equal to the electron concentration  $n$ , so that  $n = p = n_i$ , where  $n_i$  is called the concentration of electron – hole pairs in the intrinsic or pure semiconductor.

(4) The carrier concentration in a semiconductor at a temperature is given by:

$$n_i^2 = A_0 T^3 e^{-E_g / KT} \quad \text{----- (4.1)}$$

where  $A_0$  is a constant for a given material,  $E_g$  is the band gap energy,  $K$  is the Boltzmann constant and  $T$  is the temperature in Kelvin.

**4.1.2 Extrinsic or Doped Semiconductors:** If a small amount of impurity (one atom in  $10^8$  atoms) is added to the intrinsic semiconductor, it significantly increases the conductivity of the semiconductor. The semiconductor thus formed is known as extrinsic or doped semiconductor. The extrinsic semiconductors may further be classified in two categories depending upon the type of impurity being added to the intrinsic semiconductors.

- (i) N – type semiconductor
- (ii) P – type semiconductor

**N – type semiconductor:** When the atoms of V group (pentavalent) such as antimony, phosphorous or arsenic, having 5 electrons in its outer most orbit, are introduced as impurity in the intrinsic semiconductor, impurity atoms will displace few of the host atoms of the intrinsic semiconductor and form an N – type semiconductor. In the crystal structure four valence electrons of the impurity atoms will form the covalent bonds with four atoms of the intrinsic semiconductor and one electron finds no space in the covalent bond and remains free to move randomly in the crystal lattice. The impurity thus is called donor type impurity since each impurity atom donates a free electron to the crystal lattice. The semiconductor formed by introducing the donor type of impurity is called as N – type semiconductor. Figure (4.3) shows the crystal lattice of germanium with pentavalent impurity.

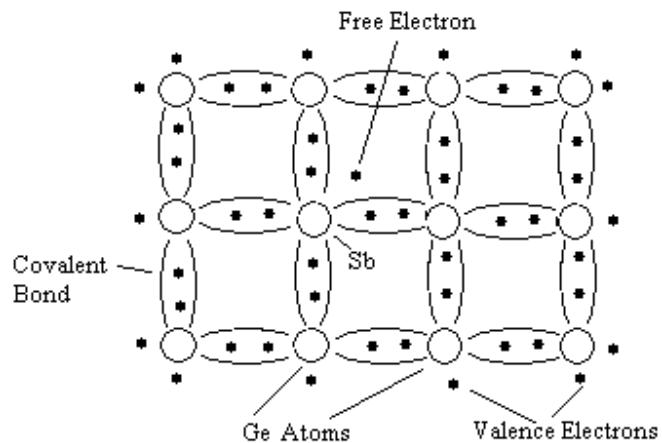


Fig. 4.3

Figure (4.4) shows the energy band diagram of N – type semiconductor. The addition of donor impurities in the intrinsic semiconductor introduces the allowable energy level just below the bottom of the conduction band. The gap between this level and the conduction band is very small  $\sim 0.01$  eV in germanium (0.05 eV in Silicon); therefore, at room temperature almost all the donor electrons get into the conduction band. This increases the free electron concentration  $n$  in the crystal. This also reduces the hole concentration  $p$  due to recombination, as the rate of recombination of electrons with hole is increased. However, the product  $np$  remains constant. In this way the number of electrons in the crystal is more than the number of holes, i.e., the electrons are the majority charge carriers and holes are the minority charge carriers.

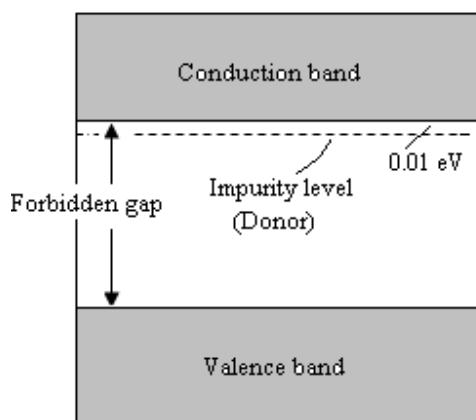


Fig. 4.4

**P – type semiconductor:** If on the contrary, the atoms of III group (trivalent) such as boron, gallium or indium, having 3 electrons in its outer most orbits, are introduced as impurity in the intrinsic semiconductor, impurity atoms will displace the atoms of the

intrinsic semiconductor and forms P – type semiconductor. In the crystal structure three valence electrons of the impurity atoms will form the covalent bonds with three atoms of the intrinsic semiconductor and the fourth covalent bond will be incomplete resulting thereby, the deficiency of an electron which constitutes a hole. The impurity thus is called the acceptor type impurity since it has the tendency to accept an electron in forming the covalent bond. The semiconductor formed by introducing the acceptor type of impurity is called as P – type semiconductor. Figure (4.5) shows the crystal lattice of germanium with trivalent impurity.

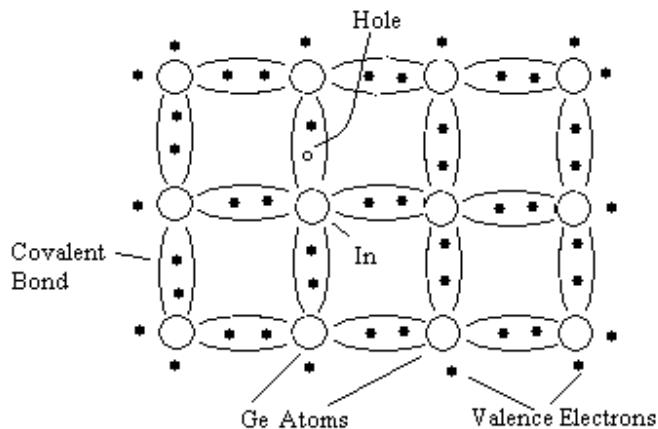


Fig. 4.5

Figure (4.6) shows the energy band diagram of P – type semiconductor. The addition of acceptor impurities in the intrinsic semiconductor introduces the allowable energy level just above the top of the valence band. A very small amount of energy is needed for an electron to leave the valence band and occupy the acceptor level. This increases the hole concentration  $p$  in the crystal. In this way the number of holes in the crystal is more than the number of electrons, i.e., the holes are the majority charge carriers and electrons are the minority charge carriers in P – type semiconductor. The product  $np$ , however, remains constant.

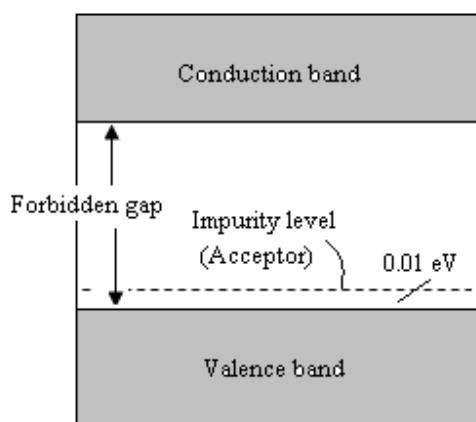


Fig. 4.6

**4.2 Effect of Temperature on extrinsic Semiconductors:** To discuss the effect of temperature on the extrinsic semiconductor, we consider an N – type semiconductor. At room temperature the electrons are the majority charge carriers and holes are the minority charge carriers. On increasing the temperature of the semiconductor, more electron hole pairs will be created. This will increase the population of holes in the semiconductor. A temperature may reach when number of broken covalent bonds is very large such that the number of electrons is almost equal to number of holes. The extrinsic semiconductor will then behave like an intrinsic semiconductor. Similarly it can be proved that the P – type semiconductor too will behave as intrinsic semiconductor at higher temperature.

### 4.3 Concentration of Holes and Electrons in Extrinsic Semiconductor:

From the above discussion it is clear that the introduction of donor impurities in intrinsic semiconductor decreases the number of holes below that in the intrinsic semiconductor. Similarly the introduction of acceptor impurities in intrinsic semiconductor decreases the number of free electrons below that in the intrinsic semiconductor. A theoretical analysis reveals that under thermal equilibrium, the product of the free electron and hole concentration is constant. It is independent of the doping concentration. This relationship is called the law of mass action and is given by:

$$np = n_i^2 \quad \text{----- (4.2)}$$

where  $n_i$  is the intrinsic concentration which is a function of temperature given by equation (4.1).

The densities of  $n$  and  $p$  may further be inter-related using the law of electrical neutrality. In an N – type semiconductor, each donor atom donates a free electron which moves randomly in the crystal lattice. The donor atom becomes a positive ion fixed in the lattice. Similarly in a P – Type semiconductor, each acceptor atom accepts one electron and becomes a negative ion. The hole created due to the acceptance of electron moves freely in the crystal lattice. Since the crystal as a whole must be electrically neutral, the positive and negative charge must be equal:

$$N_D + p = N_A + n \quad \text{----- (4.3)}$$

Consider an N – type semiconductor having no acceptor atom ( $N_A = 0$ ) and  $n >> p$  (number of free electrons is much larger than the number of holes), equation (4.3) becomes:  $n \approx N_D$  ----- (4.4)

In an N – type semiconductor, the number of free electrons is approximately equal to the density of donor atoms.

Similarly it can be proved that the number of holes in P – type semiconductor is equal to the density of acceptor atoms.

$$\text{i.e.,} \quad p \approx N_A \quad \text{----- (4.5)}$$

To be more specific, the subscript  $n$  or  $p$  is introduced to the concentrations of free electrons  $n$  and holes  $p$ , to show whether these concentrations belong to N – type or P – type semiconductors

i.e.  $n_n$  and  $p_n$  show respectively the electron and hole concentrations in N – type semiconductor.

and  $n_p$  and  $p_p$  show respectively the electron and hole concentrations in  $P -$  type semiconductor.

Using these conventions, in  $N -$  type semiconductor  $n_n = N_D$  and  $p_n = \left(\frac{n_i^2}{N_D}\right)$ , since  $n_n p_n = n_i^2$ .

Similarly in  $P -$  type semiconductor  $p_p = N_A$  and  $n_p = \left(\frac{n_i^2}{N_A}\right)$ , since  $n_p p_p = n_i^2$ .

**4.4 Currents in semiconductors:** Two types of currents flow in the semiconductors (i) diffusion current & (ii) drift current.

**(i) Diffusion Current:** The diffusion phenomenon also comes into play in the semiconductors, due to which the charge carriers may diffuse from higher concentration to lower concentration. The movement of charge carriers will constitute the current, which is known as diffusion current. Consider a semiconductor in which carrier concentration is not uniform. Let the hole concentration  $p$  decreases with the increase of  $x$ . The holes will diffuse in the positive direction of  $x -$  axis which results the flow of diffusion current in the semiconductor. The current density for holes  $J_p$  will be proportional to the concentration gradient for holes  $\left(\frac{\partial p}{\partial x}\right)$ , which is given by:

$$J_p = -qD_p \left(\frac{\partial p}{\partial x}\right) \quad \text{----- (4.6)}$$

where  $q$  is electronic charge and  $D_p$  is the proportionality constant known as diffusion constant for holes. The negative sign in this equation indicates that the concentration gradient decreases with increase of  $x$ .

The equation for current density for electrons  $J_n$  may also be given in the similar fashion if the variation of electron concentration is considered in the semiconductor crystal.

$$J_n = qD_n \left(\frac{\partial n}{\partial x}\right) \quad \text{----- (4.7)}$$

$D_n$  is called as the diffusion constant for electrons and  $\left(\frac{\partial n}{\partial x}\right)$  is concentration gradient for electrons.

**(ii) Drift Current:** The other type of current is the drift current that would flow due to the movements of charge carriers in an applied electric field across the semiconductor. It is well known that if the field is not too large then the velocity  $v$  attained by the charge carriers (drift velocity) will be proportional to the applied electric field  $E$  i.e.  $v \propto \mu E$  or  $v = \mu E$ .  $\mu$  is called the mobility of the charge carriers, which may be defined as the velocity attained by the charge carriers in an unit electric field.

Let  $v_n$  and  $v_p$  are the drift velocities of electrons and holes respectively in the electric field  $E$  applied across the semiconductor, which are given by:

$$v_n = \mu_n E$$

$$\text{and} \quad v_p = \mu_p E$$

where  $\mu_n$  and  $\mu_p$  are the mobility for electrons and holes respectively. Because of the drift velocities of electrons and holes in the semiconductor, the current called as the Drift current will flow. The drift current density for electrons  $J_n$  and holes  $J_p$  are given by:

$$J_n = nqv_n = nq\mu_n E \quad \dots \dots \dots (4.8)$$

$$J_p = pqv_p = pq\mu_p E \quad \dots \dots \dots (4.9)$$

where  $n$  and  $p$  are number of electrons and holes respectively. The total current density  $J$  is given by:

$$J = J_n + J_p = q(n\mu_n + p\mu_p)E$$

The overall conductivity of the semiconductor containing electrons and holes is given by:  $\sigma = \frac{J}{E} = q(n\mu_n + p\mu_p)$

For intrinsic semiconductors  $n = p = n_i$ , so the conductivity of the intrinsic semiconductor is given by :

$$\sigma_{int} = qn_i(\mu_n + \mu_p)$$

Conductivity of the  $N$ -Type semiconductor is :

$$\sigma_{N-type} = qn\mu_n = q\mu_n N_D$$

$N_D$  is the density of ionized donor atoms.

Conductivity of the  $P$ -Type semiconductor is :

$$\sigma_{P-type} = qp\mu_p = q\mu_p N_A$$

$N_A$  is the density of ionized acceptor atoms.

The total current densities for electrons and holes are given by:

$$J_{Tn} = q(n\mu_n E + D_n \frac{\partial n}{\partial x})$$

$$\text{and} \quad J_{Tp} = q(p\mu_p E - D_p \frac{\partial p}{\partial x}) \quad \dots \dots \dots (4.10)$$

**4.5 Properties of Ge and Si:** Some important properties of Ge and Si semiconductors are shown in form of table given below:

Table 4.1

Property	Symbols	Units	Ge	Si
Atomic No.	Z		32	14
Atomic Weight	W		72.6	28.1
Density	g	Kg/m <sup>3</sup>	5.32x10 <sup>3</sup>	2.33x10 <sup>3</sup>
Atomic Concentration		atoms/ m <sup>3</sup>	4.4x10 <sup>28</sup>	5x10 <sup>28</sup>
Dielectric constant	$\epsilon_r$		16	12
Band gap at 0 <sup>0</sup> K	E <sub>go</sub>	eV	0.785	1.21
Band gap at 300 <sup>0</sup> K	E <sub>g</sub>	eV	0.72	1.1
Intrinsic carriers	n <sub>i</sub>	Carriers/m <sup>3</sup>	2.5x10 <sup>19</sup>	1.5x10 <sup>16</sup>
Intrinsic resistivity	$\rho$	Ohm-m	0.45	2300
Mobility of electrons	$\mu_n$	m <sup>2</sup> /sec-volt	0.38	0.13
Mobility of holes	$\mu_p$	m <sup>2</sup> /sec-volt	0.18	0.05
Diff. const. for electrons	D <sub>n</sub>	m <sup>2</sup> /sec	9.9x10 <sup>-3</sup>	3.4x10 <sup>-3</sup>
Diff. const. for holes	D <sub>p</sub>	m <sup>2</sup> /sec	4.7x10 <sup>-3</sup>	1.3x10 <sup>-3</sup>

It may be mentioned here that the band gap (E<sub>g</sub>) of Ge or Si varies with temperature given by:

$$Eg(T) = 1.21 - 3.60 \times 10^{-4} \cdot T \quad \text{for Si}$$

$$Eg(T) = 0.785 - 2.23 \times 10^{-4} \cdot T \quad \text{for Ge}$$

where  $T$  is the temperature in *Kelvin*.

**Example 4.1** (a) Find the resistivity of the intrinsic germanium crystal at 300<sup>0</sup> K. (b) What will be the resistivity of this germanium crystal if the donor impurity of 1 atom per 10<sup>8</sup> germanium atoms is introduced? Given that  $n_i = 2.5 \times 10^{19}$  atoms/m<sup>3</sup>,  $\mu_n = 0.38$  m<sup>2</sup>/volt-sec,  $\mu_p = 0.18$  m<sup>2</sup>/volt-sec, Atomic conc. of Ge = 4.4x10<sup>28</sup> atoms/m<sup>3</sup>.

Solution: (a) The conductivity of the intrinsic germanium is given by:

$$\begin{aligned} \sigma_{\text{int}} &= qn_i(\mu_n + \mu_p) = 1.6 \times 10^{-19} \times 2.5 \times 10^{19} (0.38 + 0.18) \\ &= 1.6 \times 2.5 \times 5.6 = 2.24 \quad \text{mhos/m} \end{aligned}$$

The resistivity of the intrinsic germanium is given by:

$$\begin{aligned} \rho &= \frac{1}{\sigma} = \frac{1}{2.24} = 0.45 \quad \Omega \cdot \text{m} \\ (\text{b}) \quad N_D &= \frac{4.4 \times 10^{28}}{10^8} = 4.4 \times 10^{20} \\ \sigma_{N\text{-type}} &= q\mu_n N_D = 1.6 \times 10^{-19} \times 0.38 \times 4.4 \times 10^{20} \\ &= 26.752 \quad \text{mhos/m} \\ \rho_{N\text{-type}} &= \frac{1}{\sigma_{N\text{-type}}} = \frac{1}{26.752} = 0.037 \quad \Omega \cdot \text{m} \end{aligned}$$

**Example 4.2** (a) Pure germanium crystal has the resistivity of  $0.45 \Omega\text{-m}$ . How much donor impurity should be added to Ge crystal so that its resistivity decreases to 10% of the original value? (b) Find the values of  $n$  and  $p$  in this  $N$ -type Ge crystal. Given that  $\mu_n = 0.38 \text{ m}^2/\text{volt}\cdot\text{sec}$ ,  $n_i = 2.5 \times 10^{19} \text{ atoms/m}^3$

Solution: (a)  $\rho = \frac{1}{\sigma} = 0.045 \quad \text{and} \quad \sigma = q\mu_n N_D$

So  $\frac{1}{0.045} = 1.6 \times 10^{-19} \times 0.38 \times N_D$

or  $N_D = \frac{1}{0.045 \times 1.6 \times 10^{-19} \times 0.38} = \frac{10^{19}}{0.274}$   
 $= 3.65 \times 10^{20} \text{ atoms/m}^3$

(b)  $n \approx N_D = 3.65 \times 10^{20} \text{ atoms/m}^3$

$$p = \frac{n_i^2}{N_D} = \frac{(2.5 \times 10^{19})^2}{3.65 \times 10^{20}}$$

$$= \frac{6.25 \times 10^{18}}{3.65} = 1.71 \times 10^{18} \text{ atoms/m}^3$$

**Example 4.3** An  $N$ -type Ge crystal is .02m long and has a cross section of  $0.002\text{m} \times 0.002 \text{ m}$ . A current of  $10 \text{ mA}$  flows through the crystal, when a 2 volt battery is applied across it. Find (a) doping concentration  $N_D$  and (b) Drift velocity of the charge carriers. ( $\mu_n = 0.38 \text{ m}^2/\text{volt}\cdot\text{sec}$ )

Solution: (a) Resistance  $R$  of the Ge crystal is:  $R = \frac{2\text{volt}}{10\text{mA}} = 200\Omega$   
 $L = 0.02 \text{ m} \quad \text{area} \quad A = 0.0002 \times 0.0002 = 4 \times 10^{-8} \text{ m}^2$

Resistivity of the crystal  $\rho = \frac{RA}{L} = \frac{200 \times 4 \times 10^{-8}}{.02} = 4 \times 10^{-4} \Omega\text{-m}$

Conductivity  $\sigma = \frac{1}{\rho} = \frac{1}{4 \times 10^{-4}} = 2500 \text{ mhos/m}$

Since the resistivity of the crystal is very large so it is heavily doped crystal. The approximate formula may be used:  $\sigma_{N\text{-type}} = qn\mu_n = q\mu_n N_D$

so  $N_D = \frac{\sigma}{q\mu_n} = \frac{2500}{1.6 \times 10^{-19} \times 0.38} = 4.11 \times 10^{22} \text{ atoms/m}^3$

(b) Electric field  $E = \frac{\text{Volts}}{\text{length}} = \frac{2}{0.02} = 100 \text{ volts/m}$

Drift velocity of charge carriers

$$v = \mu_n E = 0.38 \times 100 = 38 \text{ m/sec}$$

**4.6 P–N Junction Diode:** The properties of  $N$  – type and  $P$  – Type semiconductors have been studied in the preceding sections. In this section the behaviour of the combination of the two types of extrinsic semiconductors will be discussed. If a  $P$  – type semiconductor is combined with the  $N$  – Type semiconductor such that the crystal structure is continuous, then a P-N junction is formed. The device thus formed is called a  $P$ - $N$  junction diode or semiconductor diode. A useful  $P$  –  $N$  junction cannot be produced by simply placing the two semiconductors together or by welding etc., because it gives rise to discontinuous crystal structure. Special fabrication techniques are adopted to form a  $P$  –  $N$  junction diode.

To understand the working of a  $P$  –  $N$  junction diode, let us consider a hypothetical case where a  $P$  – type semiconductor is brought in physical contact with the  $N$  – type semiconductor to form a junction diode as shown in figure (4.7). Both the  $P$  – and  $N$  – type semiconductors are separately electrically neutral. On the left side of the junction, the  $P$  – type crystal consists of the majority charge carrier holes and immobile acceptor ions. The acceptor ion is indicated by negative sign, because after the acceptor atom accepts an electron it becomes a negative ion. Similarly on the left side of the junction, the  $N$  – type semiconductor consists of majority charge carriers as electrons and the immobile donor ions. The donor ion is represented by the positive sign, because after a donor atom donates an electron, it becomes a positive ion. In addition, the  $P$  – type crystal also has the electrons as the minority charge carriers and  $N$  – type semiconductor has the holes as minority charge carriers.

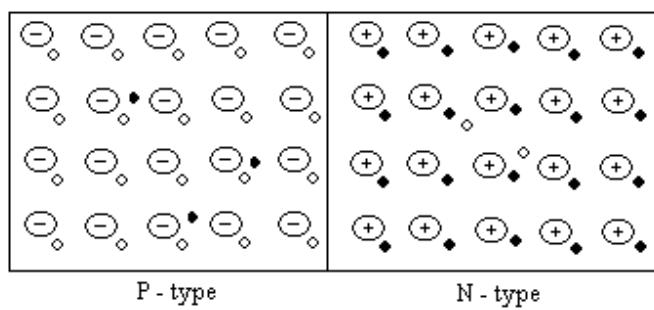


Fig. 4.7

A concentration gradient of holes will exist across the junction as the concentration of holes decreases from  $P$  – region to  $N$  – region. Similarly concentration gradient of electrons across the junction will also exist as the concentration of electrons decreases from  $N$  – region to  $P$  – region.

Because of the concentration gradients, holes will diffuse from  $P$  – region to  $N$  – region and electrons will diffuse from  $N$  – region to  $P$  – region. During the diffusion of holes from  $P$  to  $N$ , and diffusion of free electrons from  $N$  to  $P$ , some holes and some free electrons recombine. Each recombination leads the elimination of an electron – hole pair. In this process, the acceptor ions of  $P$  – region and donor ions of  $N$  – region in the neighbourhood of the junction are left uncompensated.

In the neighbourhood of the junction, the region which contains only uncompensated acceptor and donor ions, is called the depletion region, space charge

region or the transition region (fig. 4.8). The depletion region is devoid of mobile charge carriers. An electric field will develop across the junction due to these uncompensated ions, which will create a potential barrier or potential hill at the junction. The approximate value of the potential barrier is 0.3 V for *Ge* and 0.7 V for *Si* at room temperature. Further diffusion of the majority charge carriers from *P* to *N* and vice-versa is discouraged by the potential barrier. The total recombination of electron – hole pairs is, therefore, not possible. There will be some majority carriers in both the regions having sufficient energy to surmount the potential hill and may cross the junction. However, the potential barrier will encourage the drifting of minority charge carriers from one region to other. An equilibrium known as thermal equilibrium will be set up in the junction such that the drift of minority carriers across the junction is counter balanced by the diffusion of same number of majority carriers across the junction. It may be noted that no external battery has been applied across the junction so far or the junction is open circuited.

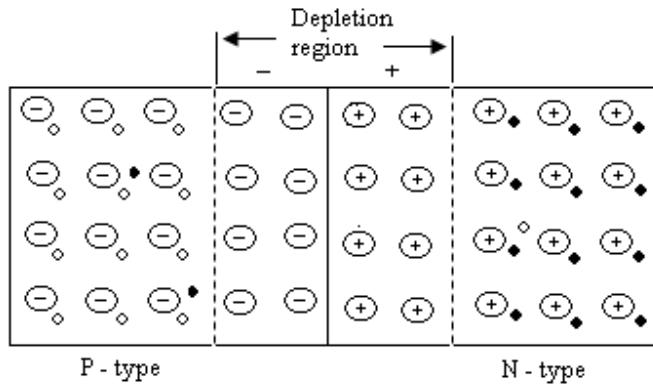


Fig. 4.8

Now we connect a battery such that positive terminal of the battery is connected to *P* – side of the diode and negative terminal of the battery to the *N* – side as shown in figure (4.9). The diode in this condition is said to be biased in forward bias. The reduction in the built-in potential is due to the applied voltage forcing more electrons into the n-type region and more holes into the p-type region, thus covering some of the fixed charges and narrowing the depletion layer. Since the total uncovered charge is reduced, the built-in potential must be lower. Remembering that the built-in potential opposes the flow of majority carriers across the junction, a reduction in the potential makes it easier for holes in the p-type region to cross the junction and for electrons in the n-type region to cross the junction in the opposite direction.

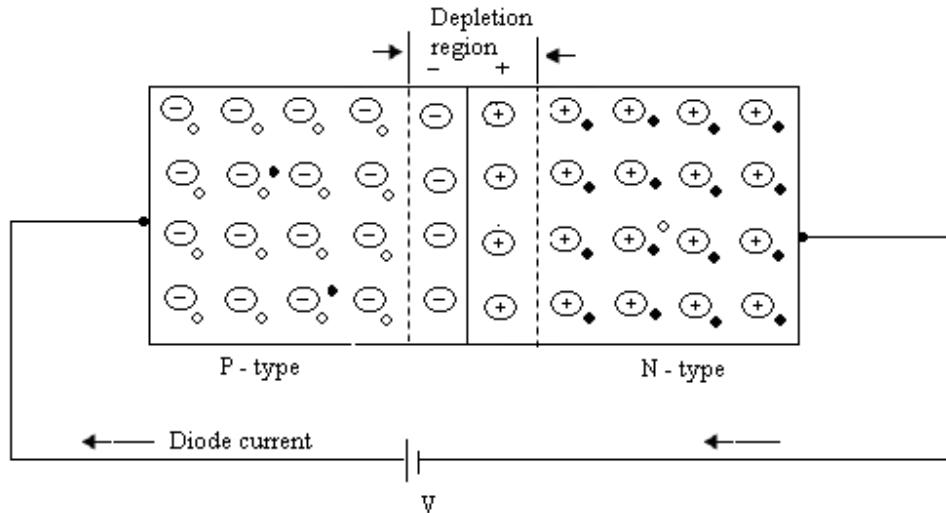


Fig. 4.9

In the  $N$  region where the electrons combine with the equal number of holes from the  $p$  region, then equal number of electrons arrives from the negative terminal of the battery and enters the  $N$  region to replace electrons lost by combination with holes near the junction. These electrons move towards the junction at the left, where these electrons combine with the new holes. This process thus goes on and large amount of current flows.

If the terminals of the battery connected to the diode is reversed that is positive terminal of the battery is connected to the  $N$  region and negative terminal to the  $P$  region, then the diode is said to be biased in the reverse bias. Figure (4.10a) shows the biasing of the diode in the reverse direction. In this condition majority charge carrier holes in  $P$  region are attracted towards the negative terminal of the battery. The majority charge carrier electrons in  $N$  region are attracted towards the positive terminal of the battery. Thus these majority charge carriers move away from the junction. This action widens the depletion region and increases the potential hill. The increased barrier potential almost completely stops the flow of majority charge carriers from one region to other. However, it will help the minority charge carriers to flow across the junction. The current that is possible to flow in the reverse bias is due to the minority charge carriers only. The minority charge carriers are minority in number hence a very small amount of current (in the range of  $10^{-6}$  to  $10^{-9}$  amperes) flows in this bias. The generation of minority charge carriers depends upon the temperature. So at the fixed temperature the reverse current is almost constant and is independent of potential of the external battery.

The symbolic representation of the  $P\text{--}N$  junction diode is shown in the figure (4.10b). It is a two terminal device, the  $P$  side of which is known as anode and  $N$  side is called as cathode. The arrow in the symbol represents the direction of the conventional current to flow when the diode is in forward bias.

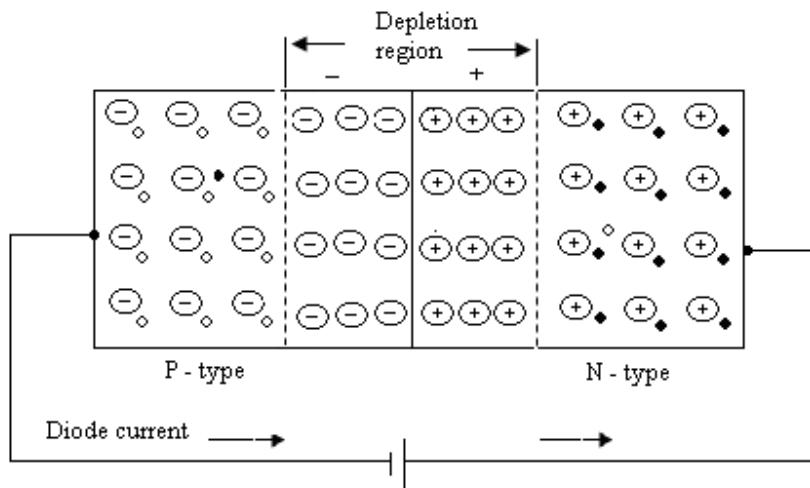


Fig 4.10 (a)

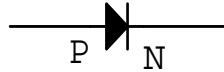


Fig. 4.10(b)

The V – I characteristic curve of the diode both in the forward and reverse bias is shown in figure (4.11). In the forward bias practically a very small current flows until the applied voltage is equal barrier potential of the diode (0.3 V for Ge and 0.7 V for Si). When there is small increase in the applied voltage beyond the barrier potential, a sharp increase in the current is observed. The voltage at which the current starts to increase rapidly is known as cut – in or knee voltage represented by  $V_\gamma$ . The effect of potential barrier is more pronounced when applied voltage is less than the barrier potential, hence a very small current. When the applied voltage is greater than the potential barrier of the diode, the effect of potential hill is nullified and current flows due to majority charge carriers, hence the large current.

In the reverse bias a very small amount of current flows due to the minority charge carriers. This current is known as reverse saturation current or leakage current. When the reverse voltage is increased beyond certain limit known as break down voltage, the minority carriers drifting across the junction acquire enough energy to ionize the atoms in the depletion region and produce more charge carriers; resulting a large current to flow. This region of the characteristics is called the avalanche break down. Ordinary diodes are never used in this break down region, since the excessive current in the diode rises its temperature to a very high value and thus the diode may be damaged. Special types of diodes known as Zener diodes are designed which work in the break down region only. These diodes are discussed in section 4.12 of this chapter.

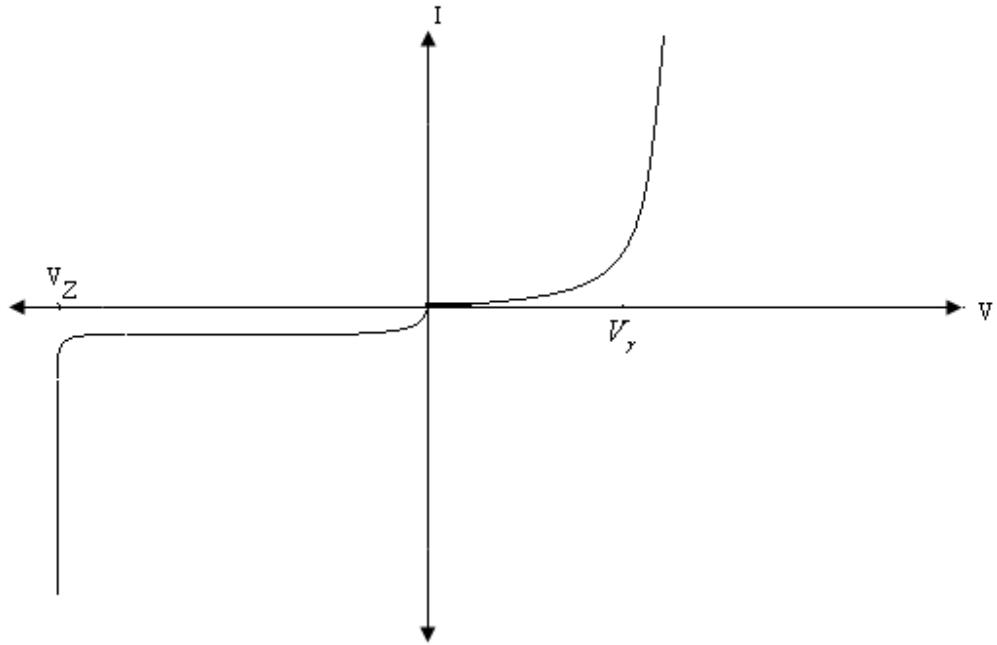


Fig. 4.11

The  $V - I$  characteristics of the junction diode may also be expressed in the form of a equation given by:

$$I = I_s [e^{(qV / \eta KT)} - 1] \quad \text{----- (4.11)}$$

Where  $I_s$  is called the reverse saturation of the diode,  $K$  is the Boltzmann constant and its value is  $1.38 \times 10^{-23}$  J/K,  $q$  is the electron charge which is equal to  $1.6 \times 10^{-19}$  Coulomb,  $T$  is temperature in  $^{\circ}\text{K}$ ,  $\eta$  is a constant whose value depends on the material of the diode and the quality of the junction, its value is 1 for Ge and 1 to 2 for Si.

The term  $(KT/q)$  has the dimension of voltage known as thermal voltage is denoted by  $V_T$ . The value of  $V_T$  is given by  $V_T = \frac{KT}{q} \approx \frac{T}{11,600}$

At room temperature ( $T = 300 \text{ } ^{\circ}\text{K}$ )  $V_T = 0.026 \text{ volt} = 26 \text{ mV}$ .

The equation (4.11) may be rewritten as:

$$I = I_s [e^{(V / \eta V_T)} - 1] \quad \text{----- (4.12)}$$

From this equation it is clear that when the diode is in forward bias and  $V > V_T$ , the value of  $e^{(V / \eta V_T)} \gg 1$ , the equation (4.12) may be approximated as:

$$I = I_s [e^{(V / \eta V_T)}] \quad \text{----- (4.13)}$$

The current, therefore, rises exponentially; this verifies the nature of the  $V - I$  characteristics of the diode in the forward direction.

When the diode is in reverse bias, the voltage  $V$  will be negative. The equation (4.12) will be written as:

$$I = I_s \left[ \frac{1}{e^{V/\eta V_T}} - 1 \right] \quad \text{----- (4.14)}$$

For large value of  $V$ ,  $I \approx -I_s$  i.e. the reverse saturation current will be independent of  $V$ .

**Example 4.4** The saturation current density of a P – N junction Ge diode is  $220 \text{ mA/m}^2$  at  $300^\circ\text{K}$ . Find the voltage that would have to be applied to cause a forward current density of (i)  $10^3 \text{ A/m}^2$  and (ii)  $10^4 \text{ A/m}^2$  to flow.

Solution: we know  $\frac{I}{A} = \frac{I_s}{A} [e^{(V/\eta V_T)} - 1]$   
or  $J = J_s [e^{(V/\eta V_T)} - 1] = J_s \left[ e^{\frac{11600 \cdot xV}{300}} - 1 \right]$

$$\eta = 1 \text{ for Ge, } V_T = (T/11600) \text{ and } T = 300$$

$$\text{or } \frac{J}{J_s} \equiv e^{38.67xV}$$

(i) case  $J = 10^3 \text{ A/m}^2$   $J_s = 220 \text{ mA/m}^2 = 0.22 \text{ A/m}^2$   
 $e^{38.67xV} = \frac{100000}{22} = 4545.45$   
 $V = \frac{\ln(4545.45)}{38.67} = \frac{8.42}{38.67} = 0.217 \text{ volts}$

(ii) case  $J = 10^4 \text{ A/m}^2$   $J_s = 220 \text{ mA/m}^2 = 0.22 \text{ A/m}^2$   
 $e^{38.67xV} = \frac{1000000}{22} = 45454.5$   
 $V = \frac{\ln(45454.5)}{38.67} = \frac{10.72}{38.67} = 0.277 \text{ volts}$

**Example 4.5** A silicon diode operates at a forward voltage of 0.4 Volt. Calculate the factor by which the current is multiplied when the temperature is increased from  $27^\circ\text{C}$  to  $125^\circ\text{C}$ .

Solution:  $V_{T1}$  at  $27^\circ\text{C}$  is given by:

$$V_{T1} = \frac{T}{11600} = \frac{(273+27)}{11600} = \frac{300}{11600} = 0.026 \text{ Volts}$$

$V_{T2}$  at  $125^\circ\text{C}$  is given by:

$$V_{T2} = \frac{T}{11600} = \frac{(273+125)}{11600} = \frac{398}{11600} = 0.034 \text{ Volts}$$

Now  $I_1 = I_s (e^{\frac{V}{\eta V_{T1}}} - 1) = I_s (e^{\frac{0.4}{2 \times 0.026}} - 1) = I_s (e^{7.69} - 1) = 2185.41 I_s$

$$I_2 = I_s (e^{\frac{V}{\eta V_{T1}}} - 1) = I_s (e^{\frac{0.4}{2 \times 0.034}} - 1) = I_s (e^{5.88} - 1) = 356.81 I_s$$

$$\text{Multiplication factor} = \frac{I_1}{I_2} = \frac{2185.4I_s}{356.81I_s} = 6.12$$

## 4.7 Temperature Dependence of Reverse Saturation current of the Diode:

**Diode:** The reverse saturation current of the diode is very much dependent on temperature and very important factor to be studied. Its theoretical variation with temperature is approximately given by:

$$I_s = K' T^m e^{-\left(\frac{qV_{g0}}{\eta KT}\right)} = K' T^m e^{-\left(\frac{V_{g0}}{\eta V_T}\right)} \quad \dots \dots \quad (4.15)$$

Where  $K'$  is a constant,  $qV_{g0}$  is the forbidden gap energy in Joules:

$\eta = 1$	$m = 2$	$V_{g0} = 0.785 \text{ V}$	for Ge
$\eta = 2$	$m = 1.5$	$V_{g0} = 1.12 \text{ V}$	for Si

Taking logarithms on both sides of the equation (4.15) and differentiating, we get :

$$\begin{aligned} \ln I_s &= \ln K' + m \ln T - \frac{qV_{g0}}{\eta KT} \\ \frac{1}{I_s} \left( \frac{dI_s}{dT} \right) &= \frac{m}{T} + \frac{qV_{g0}}{\eta K} \cdot \frac{1}{T^2} \\ \frac{dI_s}{dT} &= \frac{I_s}{T} \left[ m + \frac{qV_{g0}}{\eta KT} \right] \end{aligned} \quad \dots \dots \quad (4.16)$$

From this equation it can be shown that  $I_s$  varies with temperature by 8% per degree Celsius for Si and 11% per degree Celsius for Ge. The experimental data is slightly different from this theoretical variation. The experimental variation is about 7% per degree Celsius in temperature for both Ge and Si. Since  $(1.07)^{10} \approx 2.0$ , it is therefore concluded that for every  $10^0\text{C}$  rise in temperature the reverse saturation approximately doubles. This statement can be put in the form of a equation given by:

$$I_{s2} = I_{s1} \cdot 2^{\frac{(T_2 - T_1)}{10}}$$

Where  $I_{s2}$  and  $I_{s1}$  are the values of  $I_s$  at temperatures  $T_2$  and  $T_1$  respectively. The reason for the discrepancy between the theoretical and experimental results is that, in a physical diode there is a component of reverse saturation current  $I_s$  due to leakage over the surface that has not been taken into account. This component of  $I_s$  is independent of temperature. The diode may assume to be shunted with a resistance  $R$  as shown in figure (4.12). The component of reverse saturation current over the surface is given by:

$$I_2 = I_s - I_1$$

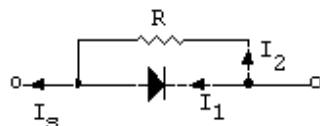


Fig. 4.12

**Example 4.6** Calculate theoretically the factor by which the reverse saturation current of a Ge diode be multiplied when the temperature of the diode is increased from  $27^0\text{C}$  to  $75^0\text{C}$ .

Solution:  $I_s$  at  $27^0\text{C}$  ( $300^0\text{K}$ ) is given by:

$$I_{s1} = K' x (300)^2 e^{-\left(\frac{11600 \times 0.785}{300}\right)} = K' x (300)^2 e^{-\left(\frac{9106}{300}\right)}$$

$I_s$  at  $75^0\text{C}$  ( $348^0\text{K}$ ) is given by:

$$I_{s2} = K' x (348)^2 e^{-\left(\frac{11600 \times 0.785}{348}\right)} = K' x (348)^2 e^{-\left(\frac{9106}{348}\right)}$$

$$\begin{aligned} \text{Multiplication factor} &= \frac{I_{s2}}{I_{s1}} = \left(\frac{348}{300}\right)^2 \frac{e^{\left(\frac{9106}{300}\right)}}{e^{\left(\frac{9106}{348}\right)}} = 1.3456 \frac{e^{30.35}}{e^{26.167}} \\ &= 88.19 \end{aligned}$$

**Example 4.7** It is predicted that, for Ge diode the reverse saturation  $I_s$  should increase at the rate of 11% per degree Celsius rise in temperature. Experimentally it was found that in the diode the reverse saturation current is  $5 \mu\text{A}$  at a reverse voltage of 10 volts, and it increases by 7% per degree Celsius rise in temperature. What is the value of leakage resistance shunting the diode?

Solution: From the figure (4.12)

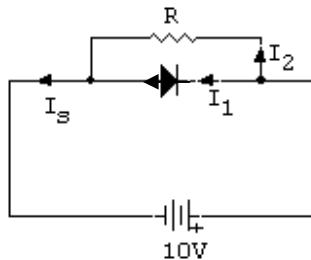


Fig.4.13

$$I_2 = I_s - I_1 \quad \text{or} \quad I_1 + I_2 = 5 \times 10^{-6}$$

According to the problem  $I_s$  is increased by 7% so  $I_s = 1.07 \times 5 \mu\text{A}$

And  $I_1$  is increased by 11 % so  $I_1 = 1.11 \times I_1$

$$\begin{aligned} I_2 &= 1.07 \times 5 \times 10^{-6} - 1.11 \times I_1 \\ &= 5.35 \times 10^{-6} - 1.11(5 \times 10^{-6} - I_2) \end{aligned}$$

$$\text{or} \quad = (0.2/11) \times 10^{-6} = 1.82 \mu\text{A}$$

$$\text{Therefore} \quad R = \frac{10 \text{ volt}}{1.82 \mu\text{A}} = 5.5 \text{ M}\Omega$$

**4.8 Diode Resistance:** The characteristic curve of the diode is non-linear so the diode is called as the non-linear device. Its resistance value changes at different point of the curve. The two types of resistances for the diode may be defined namely: (i) D.C. or Static Resistance (ii) A.C or Dynamic resistance

**D.C. or Static Resistance:** It is defined as the ratio of the voltage and current at any point on the characteristic curve of the diode. This resistance is equal to the reciprocal of the slope of the line joining the operating point to the origin. The static resistance varies with voltage and current and is not a useful parameter. The forward resistance (static)  $R_f$  of the diode is very small and reverse resistance  $R_r$  is very high.

**A.C. or Dynamic Resistance:** The very useful parameter for the diode is the dynamic or A.C. or incremental resistance, which is defined as the reciprocal of the slope of the V – I characteristic curve i.e.  $r_{a.c.} \equiv \frac{dV}{dI}$ . The dynamic resistance is not constant but depends upon the operating voltage.

$$\text{The diode equation is given by: } I = I_s [e^{(V/\eta V_T)} - 1]$$

Differentiating this equation with V, we get:

$$\frac{dI}{dV} = \frac{I_s e^{(V/\eta V_T)}}{\eta V_T} = \left( \frac{I + I_s}{\eta V_T} \right) \quad \text{----- (4.17)}$$

$\frac{dI}{dV}$  is called the incremental conductance denoted by g. The reciprocal of g is called the incremental resistance or a.c. resistance denoted by  $r_{a.c.}$ , which is given by:

$$r_{a.c.} = \left( \frac{\eta V_T}{I + I_s} \right) \approx \frac{\eta V_T}{I} \quad \text{----- (4.18)}$$

As  $I_s$  very small comparative to forward current I, hence neglected.

**Example 4.8** Find the static and dynamic resistance of a P – N junction Ge diode for an applied voltage of 0.2 Volt. Temperature =  $27^0\text{C}$  and reverse saturation current is  $2 \mu\text{A}$ .

Solution: We know  $I = I_s [e^{(V/\eta V_T)} - 1]$

$$\eta = 1 \text{ for Ge, } I_s = 2 \times 10^{-6} \text{ A, } V_T = T/11600 \text{ and } T = 273 + 27 = 300$$

$$\begin{aligned} \text{or } I &= 2 \times 10^{-6} \left[ e^{\frac{11600 \times V}{300}} - 1 \right] = 2 \times 10^{-6} [e^{38.67 \times 0.2} - 1] \\ &= 2 \times 10^{-6} \times (2284.72 - 1) \\ &= 0.004567 = 4.567 \text{ mA} \end{aligned}$$

$$\text{Static resistance } r_{d.c.} = \frac{V}{I} = \frac{0.2 \times 10^3}{4.567} = 43.8 \Omega$$

$$\begin{aligned} \text{Dynamic resistance } r_{a.c.} &= \left( \frac{V_T}{I + I_s} \right) \approx \frac{V_T}{I} = \frac{25.8 \text{ mV}}{4.4567 \text{ mA}} \\ &= 5.7 \Omega \end{aligned}$$

**4.9 Ideal Diode:** The P – N junction diode has been discussed in detail. It offers a low resistance in forward bias (i.e.  $R_f$  is low) and offers high resistance in reverse bias

(i.e.  $R_r$  is high). The perfect or ideal diode may, however, be defined as a diode which offers zero resistance to the current flow in forward bias, the current in the diode is limited by the applied potential. On the other hand, it offers infinite resistance to the current flow in the reverse bias or the current is zero. The ideal diode is purely an imaginary quantity and practically such diodes are not available. These diodes behave as ON switch in the forward bias and OFF switch in the reverse bias as shown in figure (4.14).

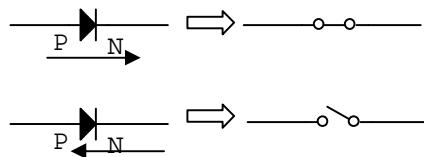


Fig. 4.14

The characteristic curve of the ideal diode is shown in figure (4.15), which coincides with  $V$  and  $I$  axes. ( $I > 0$  for  $V = 0$ , and  $I = 0$  for  $V < 0$ )

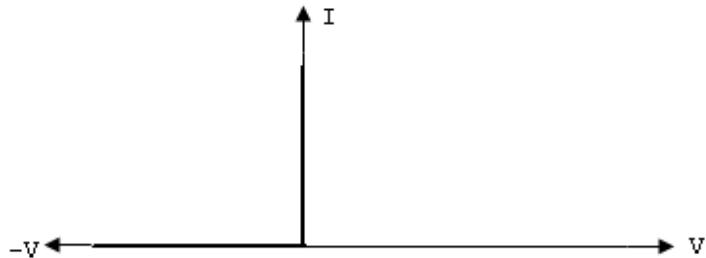


Fig. 4.15

**4.10 Circuit Model for Junction Diode:** It is well known that a voltage drop across the diode is observed in the forward bias. This voltage drop is about 0.7 V for Si diode and 0.3 V for Ge diode for a forward current of 1mA. Thus if we are dealing with voltage like hundreds of volts in the circuit containing the diodes, this voltage drop of about 0.7 V or 0.3 V may assumed to be negligibly small. For the approximate calculations in the circuit the diodes may be assumed as the ideal diodes discussed above. On the contrary if the applied voltage is comparable to the forward voltage drop of the diodes, then junction diodes may not be approximated as ideal diodes but a battery of knee voltage  $V_\gamma$  is assumed to be connected in series with the ideal diode as shown in figure (4.16). This model is known as the piecewise linear model or the approximate model of the junction diode.

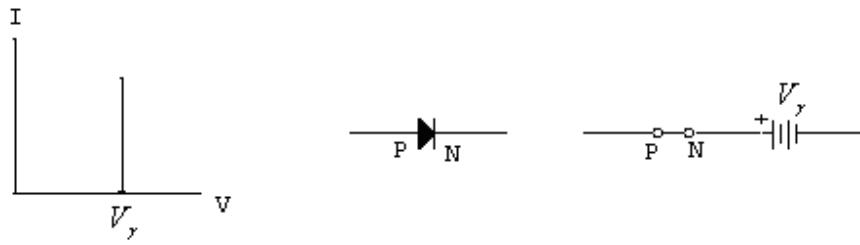


Fig. 4.16

For more accurate calculations, we use the model shown in figure (4.17), in which a small resistance  $r$  is also included in the model. The non-linear  $V - I$  relationship of the junction diode is here approximated a straight line of slope ( $1/r$ ).

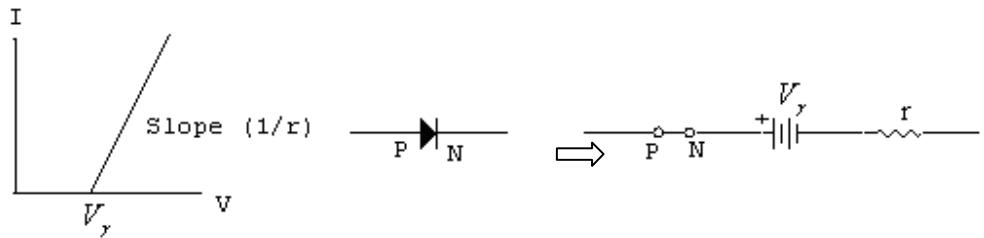


Fig. 4.17

**Example 4.9** In the figure (4.18) the diode is reverse biased. (a) If the diode is ideal what is the voltage across it? (b) If the diode has a reverse current of 0.25 mA at  $-50$  Volts, what is the voltage across the diode?

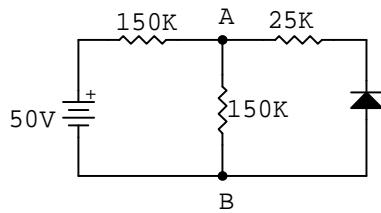


Fig. 4.18

Solution: The Thevenin's equivalent of this circuit is given by (fig. 4.19):

$$V_{AB} = \frac{50V \times 150K}{(150 + 150)K} = 25V$$

$$R_{AB} = \frac{150K \times 150K}{(150 + 150)K} = 75K\Omega$$

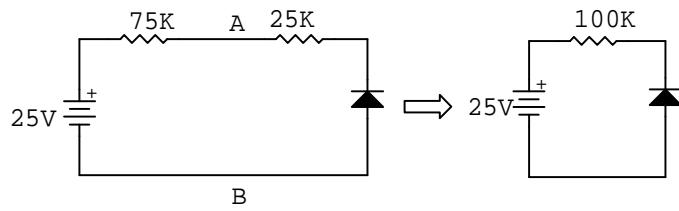


Fig. 4.19

- (a) In the first case when the diode is ideal (behaves as an open switch), the voltage across the diode will be equal to the open circuit voltage i.e. 25 Volts.
- (b) In the second case diode resistance in reverse bias is

$$R_r = \frac{50}{0.25 \times 10^{-3}} = 200 K\Omega$$

Now the diode can be replaced by a resistance of  $200 K\Omega$  as shown in figure (4.20).

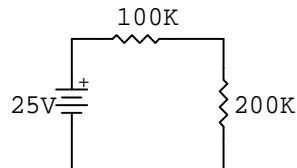


Fig. 4.20

The voltage across the diode ( $200 K\Omega$  resistance) is given by:

$$V_o = \frac{25V \times 200K}{300K} = \frac{50}{3} = 16.67 \text{ volts}$$

**Example 4.10** The Si diode in the given figure (4.21) has a current of  $2\mu A$  for a reverse voltage of 100 volts. If the diode is approximated by a battery of 0.7 volt, what is the output wave form across  $1M\Omega$  resistance?

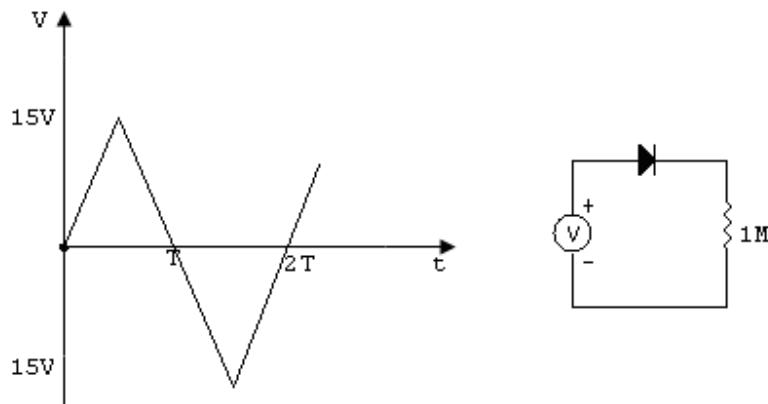


Fig. 4.21

Solution: In the forward bias, the diode will have the voltage drop of 0.7 Volt so the output will increase only up to  $15 - 0.7 = 14.3$  volt.

In the reverse bias, the diode will behave like a resistance of  $(100\text{Volt}/2\mu\text{A}) 50 \text{ M}\Omega$ . So voltage across 1 M $\Omega$  resistance is  $\frac{15V \times 1M}{(50+1)M} = 0.29$  volt.

In the negative half cycle of the input wave, output will increase only up to 0.29 volts. The output wave form is, therefore, given in figure (4.22).

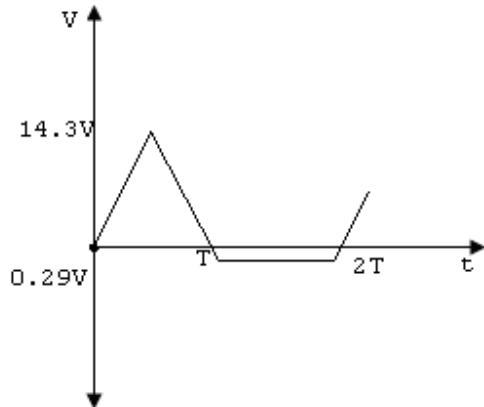


Fig.4.22

**4.11 Junction Capacitances:** Two types of Junction capacitances are observed in the P N junction diode. These capacitances are:

- (i) Transition or Depletion region capacitance ( $C_T$ ) and
- (ii) Diffusion capacitance or Storage capacitance ( $C_D$ ).

Both types of capacitances are present in forward and reverse bias region. But the transition capacitance is more effective in reverse bias and diffusion capacitance is more effective in forward bias. These capacitances are very small in magnitude so they are sensitive at high frequencies. At low frequencies their reactance are very high hence behave like an open circuit, but at high frequencies their reactance are finite and introduce impedances in the circuit.

**(i) Transition Capacitance:** In the reverse bias there is a depletion region that behaves essentially like an insulator between the layers of opposite charges. So it will behave like a parallel plate capacitor whose value is given by:  $C = \frac{\epsilon A}{W}$ , where  $\epsilon$  is

the permittivity of the dielectric (insulator), A is the area of the plates, W is the distance between the parallel plates (or width of the depletion region). As is well known the width of the depletion region increases with the increase of the reverse bias; a decrease in the transition capacitance with the increase of the reverse bias will be observed. This property of the diode is used in the construction of special types of diode called Varactor diodes or Varicaps.

**(ii) Diffusion Capacitance:** The diffusion capacitance  $C_D$  is observed in the junction diode when it is in forward bias. It is caused by the injected charge stored on both sides of the junction just outside the space charge region. It is basically the rate of change of injected charge with voltage. The increased level of current will result in the increased level of diffusion capacitance.

The capacitive effect of the junction diode is represented by a capacitance in parallel with the ideal diode as shown in figure (4.23).

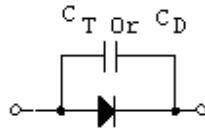


Fig. 4.23

**4.12 Zener Diodes:** Zener diodes also called as Avalanche diodes are the heavily doped P – N junction diodes which work in the reverse bias and operate in the break down region. Ordinary diodes are never used in the break down region, since the excessive current in the diode rises its temperature to a very high value and hence the diode may be damaged. It has been observed that when the reverse voltage of the diode is increased beyond certain limit then two types of break downs are possible. (i) Avalanche Break Down; & (ii) Zener Break Down.

**(i) Avalanche Break Down:** When the reverse voltage of the heavily doped junction diode reaches a certain limit, the electric field is quite intense and the minority carriers in this field are accelerated and get sufficient velocity to collide with the ions in the depletion region resulting thereby the liberation of electron – hole pairs. These liberated carriers also gain enough velocities to dislodge other electron – hole pairs. This cumulative process is referred to avalanche multiplication. This leads a large reverse current and the diode is said to be in the avalanche breakdown region.

**(ii) Zener Break Down:** The Zener break down does not occur by the collision of carriers with semiconductor ions as in the case of avalanche breakdown, but the breaking of covalent bonds occurs by the strong field set up in the depletion region due to the applied reverse bias. Thus a large reverse current is produced.

The V – I characteristic of a Zener diode is shown in figure (4.24). It is clear from this curve that in forward bias its characteristics are the same as that of the ordinary diode. In the reverse bias, a constant reverse current flows until the break down voltage is reached. This breakdown voltage is known as Zener voltage ( $V_z$ ). The Zener voltage may be different for different Zener diodes depending upon the amount of doping in the diode. A heavily doped diode has a narrow depletion region and the breakdown occurs at low voltage and hence the low Zener voltage. For lightly doped diodes the breakdown occurs at high voltage. The Zener diodes having the break down voltage from 1.8 volts to 200 volts are available with power rating of  $\frac{1}{4}$  watt to 200 watts. In high voltage Zener diodes the avalanche multiplication is more pronounced and in the low voltage diodes Zener

breakdown is effective. However, in the diodes of Zener voltages between 5 volts to 8 volts both types of breakdown occur.

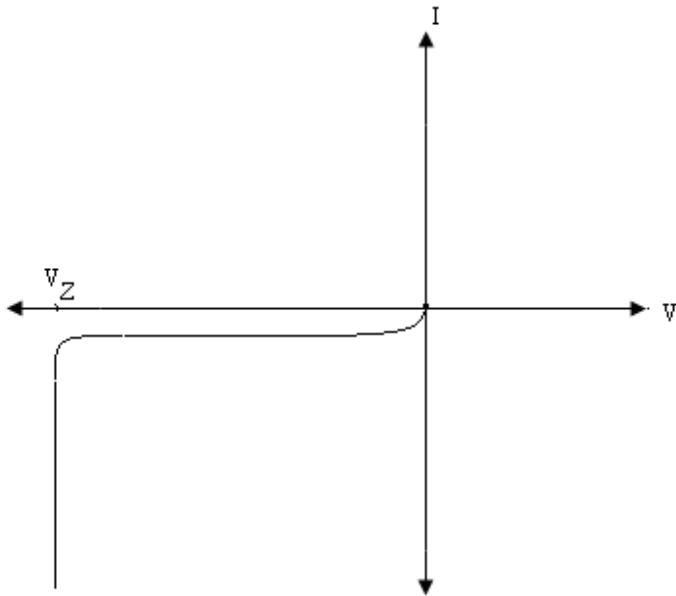


Fig. 4.24

The Zener diodes are used as voltage regulator i.e. a constant voltage equal to the Zener voltage may be obtained with these diodes. Its symbolic representation is the same as that of ordinary diode with the only difference that the bar is replaced by a symbol  $Z$  (fig. 4.25 a). Its equivalent circuit may be represented by a battery equal to Zener potential (fig. 4.25 b). The accurate equivalent circuit includes a small dynamic resistance in series with the battery, as shown in figure (4.25 c).

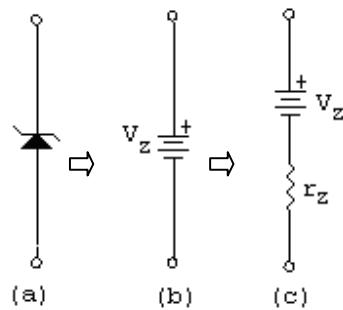


Fig. 4.25

**4.13 Light Emitting Diodes:** Light emitting diodes (LED's) are specially doped P N junction diodes, which emit light when a proper forward bias is applied across the diodes. In the forward biasing of the diodes the electrons from N – type semiconductor move across the junction and enter P – type semiconductor. These electrons combine with holes. This recombination requires that the energy possessed by the free electrons be transferred to some other form. In all semiconductor P N junctions some of this energy

will be given off as heat and some in the form of light energy. In Si and Ge diodes this energy is given off more in the form of heat and very negligible amount of energy is transferred in the form of light. However, the energy is given up in the form of visible lights than the heat if the diodes are designed by the Gallium Phosphide or Gallium Arsenide Phosphide semiconductor materials. The LED's fabricated by Gallium Phosphide produces visible red light and Gallium Arsenide Phosphide semiconductor produces visible green light. Infrared LED's are designed by Gallium Arsenide semiconductors which emit invisible infrared light in forward bias. The LED is represented by the simple diode in addition emission of light is also shown (fig.4.26). The LED's are used as display devices and are available in different shape and size.

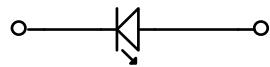


Fig. 4.26

**4.14 Photodiodes:** If the radiations are allowed to fall on the junction of a P – N diode, the reverse current varies linearly with the radiations. The device which exhibits this property is known as Photodiode. This device is embedded in a plastic cover having a window for the light to fall on the junction as shown in the figure (4.27). It is well known

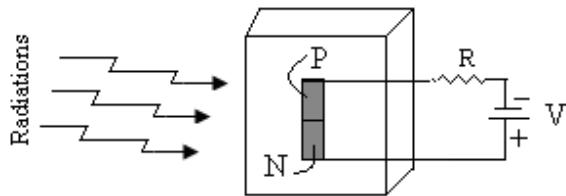


Fig. 4.27

that when the diode is in reverse bias, then reverse saturation current flows in the diode which is generated due to the minority charge carriers. When the light energy incident on the junction, generation of minority carriers are increased thereby increasing the reverse current. The dark current of the photodiode is that current which is obtained when no photons are incident on the junction. Figure (4.28) shows the characteristics of photodiode for different intensity of light given in foot candles.

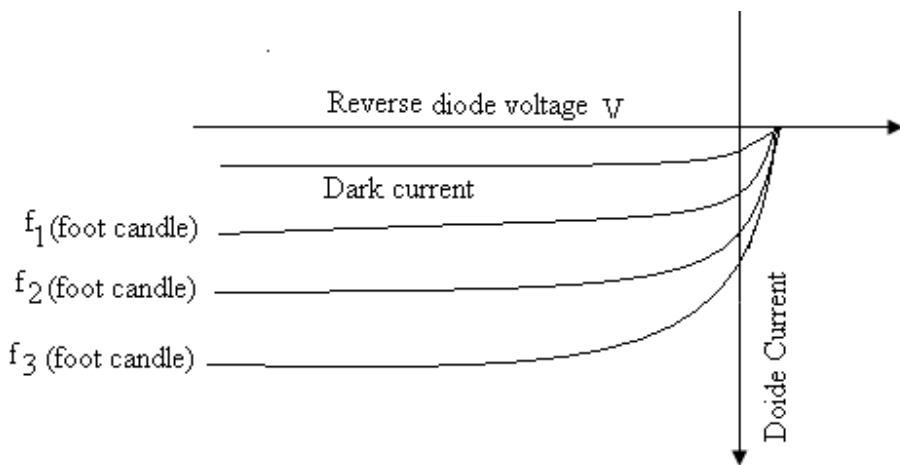
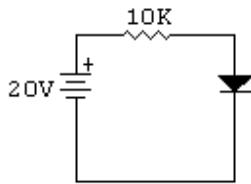


Fig. 4.28

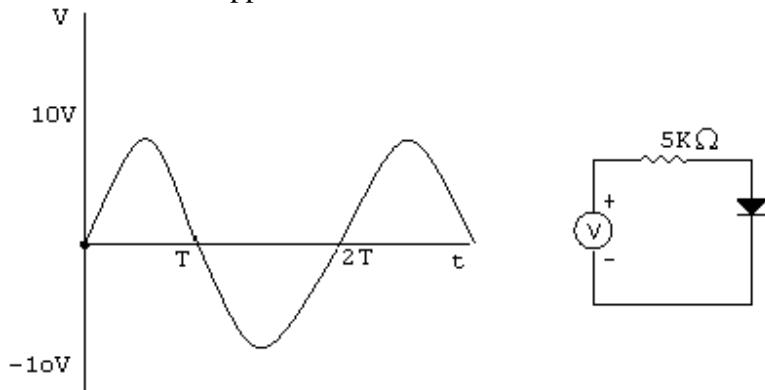
### Problems:

1. What is the difference between metal, insulator and semiconductor? Discuss on the basis of energy band diagram.
2. What is a semiconductor? Distinguish between intrinsic and extrinsic semiconductor?
3. What do you understand by intrinsic and extrinsic semiconductors? Give the energy band description of semiconductors and discuss the effect of temperature on it.
4. What are N type and P type semiconductors? Discuss the effect of temperature on the extrinsic semiconductor.
5. Discuss the currents in extrinsic semiconductors. Find the expression for the total current density in the extrinsic semiconductor.
6. What is drift current? Derive an expression for drift current density and conductivity in a semiconductor.
7. What is diffusion current? Drive the expression for diffusion current density for holes and electrons.
8. What is a junction diode? Explain the working of a P – N junction diode under forward and reverse biasing. Draw the V – I characteristic curve of the junction diode.
9. What are P and N type semiconductor? How they are used to form the junction diode. Discuss how the depletion region is formed in a junction diode.
10. Discuss the effect of temperature on the reverse saturation current of the junction diode.
11. What do you understand by static and dynamic resistance of a junction diode? Find the expression for the dynamic resistance.
12. What is the difference between an ideal diode and a practical diode? Discuss the circuit models for the junction diode.
13. Write short notes on the following:
  - (i) Junction capacitances

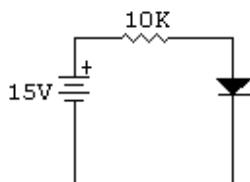
- (ii) Photodiode  
 (iii) Light emitting diode
14. Discuss the physical mechanism of breakdowns in a junction diode. Explain the working and characteristics of Zener diode.
15. (a) Show that the resistivity of the intrinsic Si crystal at  $300^0$  K is  $0.45\Omega\text{-m}$  (b) what will be the resistivity of this Si crystal if the donor impurity of 1 atom per  $10^8$  Si atoms is introduced? Given that  $n_i = 1.5 \times 10^{16} \text{ atoms/m}^3$ ,  $\mu_n = 0.13 \text{ m}^2/\text{volt}\text{-sec}$ ,  $\mu_p = 0.05 \text{ m}^2/\text{volt}\text{-sec}$ , Atomic conc. of Si =  $5.0 \times 10^{28} \text{ atoms/m}^3$ .  
 Ans.  $0.037 \Omega\text{-m}$
16. Find the density of impurity atoms that must be added to intrinsic Si wafer to convert it to (i)  $0.2 \Omega\text{-m}$  P – type Silicon.  
 (ii)  $0.2 \Omega\text{-m}$  N – type Silicon.  
 Given for Si  $\mu_n = 0.13 \text{ m}^2/\text{volt}\text{-sec}$ ,  $\mu_p = 0.05 \text{ m}^2/\text{volt}\text{-sec}$ .  
 Ans.  $N_A = 6.25 \times 10^{20}/\text{m}^3$ ,  $N_D = 2.4 \times 10^{20}/\text{m}^3$
17. Calculate the density of donor atoms to be added to an intrinsic semiconductor to produce N – type semiconductor of  $4500 \text{ mhos/m}$ . Given  $\mu_n = 0.385 \text{ m}^2/\text{volt}\text{-sec}$ .  
 Ans.  $N_D = 73 \times 10^{21}/\text{m}^3$
18. Mobilities of electrons and holes in intrinsic Ge crystal at room temperature are  $0.38 \text{ m}^2/\text{volt}\text{-sec}$  and  $0.18 \text{ m}^2/\text{volt}\text{-sec}$  respectively. If the densities of electrons and holes are  $2.5 \times 10^{19}/\text{m}^3$  and  $1.5 \times 10^{16}/\text{m}^3$  respectively. Calculate electrical conductivity and resistivity of Ge.  
 Ans.  $1.35 \text{ mhos/m}$ ,  $0.74 \text{ ohm-m}$
19. A forward biased P N junction diode requires 1 volt to pass a current of  $300 \text{ mA}$ . The same junction requires  $200 \text{ volts}$  to pass  $20 \mu\text{A}$  current in reverse bias. Find the forward and reverse resistance of the diode.  
 Ans.  $R_f = 3.33 \Omega$ ,  $R_r = 10 \text{ M}\Omega$
20. Sketch the output voltage across  $10 \text{ k}\Omega$  resistance of the circuit shown in the figure given below. Use ideal diode approximation.
- 
- The graph shows a triangular wave voltage  $V$  versus time  $t$ . The peak-to-peak voltage is  $30 \text{ V}$ , with  $15 \text{ V}$  above ground and  $-15 \text{ V}$  below ground. The period of the triangle is  $T$ , and the half-period is  $T/2$ . The circuit diagram to the right shows a  $15 \text{ V}$  DC voltage source connected in series with a diode and a  $10 \text{ k}\Omega$  resistor, which is then connected to ground.
21. A forward biased Ge diode is connected as shown in figure given below. Find the voltage across the diode if the reverse saturation current is  $10 \mu\text{A}$ .  
 Ans.  $0.138 \text{ Volt}$



22. Sketch the output voltage across the diode of the circuit shown in the figure given below. Use ideal diode approximation.

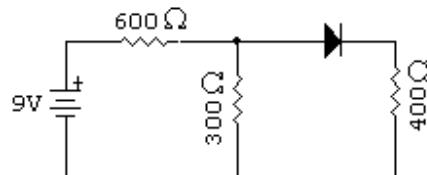


23. In the figure given below the diode is made of Ge and has a forward current of 10 mA at 1 volt. (a) How much current flows if the diode is considered ideal? (b) How much current flows if the diode is considered by a battery and a resistance in series with it?



Ans. (a) 1.5 mA, (b) 1.4 mA

24. A Si diode is used in the circuit shown in the figure given below. Determine the voltage across  $400\ \Omega$  resistance, if the diode is approximated by a battery of potential 0.7 volt.



Ans. 1.53 volt

25. A Si diode at room temperature of  $27^{\circ}\text{C}$ , conduct 1 mA current at 0.7 volt. Now the voltage is increased to 0.9 volt. Calculate the diode current and the reverse saturation current. Given  $\eta = 2$ .

Ans. 0.046 A, 1.4 nA

26. A Ge diode operates at a forward voltage of 0.25 Volt. Calculate the factor by which the current is multiplied when the temperature is increased from  $27^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ . Ans. 17.8
27. For what voltage will the reverse current in a Ge diode attain a value of 90% of its saturation value at  $300^{\circ}\text{K}$ ? What will now be the current if  $I_s = 10\mu\text{A}$  and the forward voltage of the magnitude calculated above is applied? Ans.: - 60 mV, 91  $\mu\text{A}$
28. (a) Calculate theoretically the factor by which the reverse saturation current of a Ge diode be multiplied when the temperature of the diode is increased from 25 to  $85^{\circ}\text{C}$ .  
(b) Repeat the calculations of part (a) for Si diode whose temperature is increased from 25 to  $150^{\circ}\text{C}$ . Ans.: 244.73 , 1739
-

# 5 Applications of Diodes

In the forgoing chapter of this book, the details of the semiconductors and different types of diodes have been discussed. The applications of the semiconductor diodes such as rectifiers, filters circuits, voltage multiplier circuits, clipping, clamping Log antilog circuits will be discussed in this chapter. Zener diode as the voltage regulator circuit will also be discussed in this chapter.

**5.1 Rectifier Circuits:** Many electronic equipments work with d.c. power supply. The line voltage available from the power plugs is a.c. voltage (220 Volts & 50Hz frequency). A circuit which converts a.c. voltage to d.c. voltage is required. Such a circuit is called the rectifier circuit. The nonlinear elements like vacuum diodes or semiconductor diodes may be used for the rectification of the supply. There are two types of rectifier circuits (i) Half Wave Rectifier & (ii) Full Wave Rectifier. In the following articles these circuits will be discussed in detail using the semiconductor diodes.

**5.1.1 Half Wave Rectifier :** Consider a circuit shown in the figure (5.1). In this circuit a sinusoidal voltage  $E_s = E_m \sin \omega t$ , obtained from the transformer, is applied to a series combination of the diode  $D_1$  and a load resistance  $R_L$ .  $E_m$  is the peak voltage of the signal and  $\omega = 2\pi f$  is the frequency of the a.c. mains in radians and  $f$  is the mains frequency in Hz. The transformer used here may be step up or step down transformer which is chosen according to the required d.c. supply. If the a.c. mains supply (220 volts, 50 Hz) is to be rectified, then it may directly be applied to the series combination of diode and load resistance.

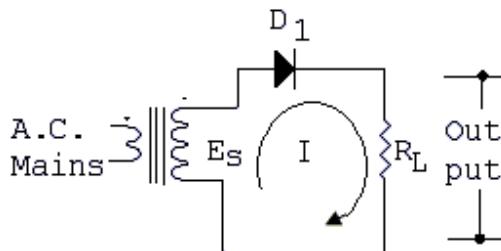


Fig. 5.1

To discuss its operation, assume that the peak value of voltage  $E_m$  is large enough than the cut in voltage of the diode, so that the diode behaves like an ideal diode. During the positive half cycle of the input wave  $E_s$ , the diode is in forward bias and works as a closed switch. Therefore, applied voltage appears across the load resistance  $R_L$ . However, during the negative half cycle of the input wave, the diode is in reverse bias and it acts as an open switch. In this case, no current flows through the circuit and voltage across the load resistance  $R_L$  is zero. The input, output waves of the circuit is shown in the fig. (5.2).

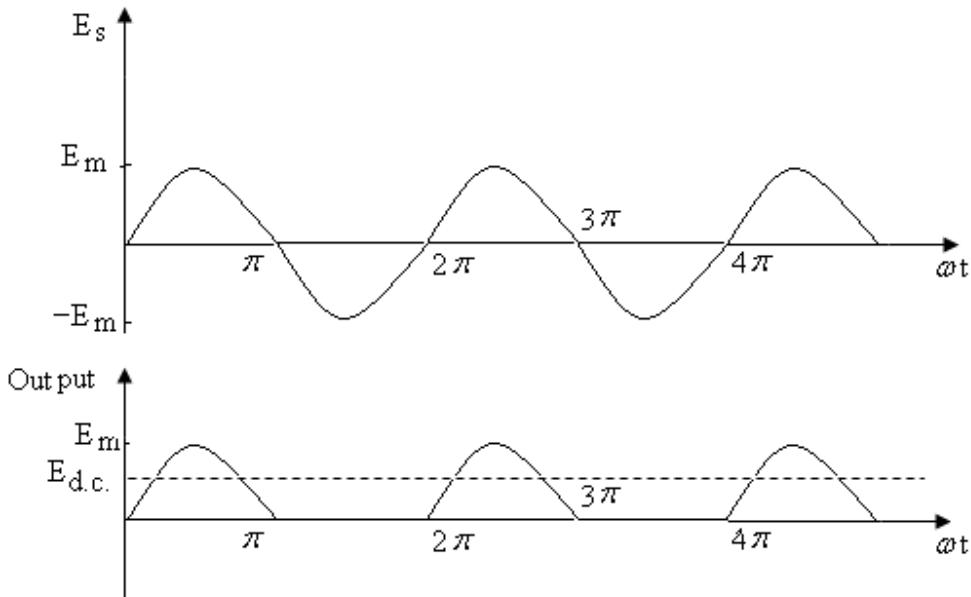


Fig. 5.2

From this figure it is clear that the current in the load resistance flows only during positive half cycle of the input wave and is zero during the negative half cycle, i.e., the current is unidirectional. Hence the circuit is called a half wave rectifier.

**Analysis:** The input a.c. voltage is given by  $E_s = E_m \sin \omega t$

Since the current in the load resistance is unidirectional, so we take the average value of the voltage across the resistance. It may be given as:

$$E_{d.c.} = \frac{1}{T} \int_0^{T/2} E_m \sin \omega t \, dt = \frac{E_m}{\pi} \quad \text{since } T = \frac{2\pi}{\omega}$$

The d.c. current flowing through the load resistance  $R_L$  is given by:

$$\begin{aligned} I_{d.c.} &= \frac{E_{d.c.}}{R_L} = \frac{E_m}{\pi R_L} \\ &= \frac{I_m}{\pi} \quad \text{(where } I_m = \frac{E_m}{R_L} \text{ is the peak current)} \end{aligned}$$

The output voltage across the load resistance may be given by the Fourier analysis as:

$$E_{out} = \frac{E_m}{\pi} + \frac{E_m}{2} \sin \omega t - \frac{2E_m}{3\pi} \cos 2\omega t - \frac{2E_m}{15\pi} \cos 4\omega t - \frac{2E_m}{31\pi} \cos 6\omega t - \dots \quad (5.1)$$

From equation (5.1), it may be seen that the first term of the equation is the same as  $E_{d.c.}$  as calculated above. In addition to this term there are other terms of frequency  $\omega$  and its higher harmonics. So the output voltage across the load resistance has the required voltage ( $E_{d.c.}$ ) and other unwanted components called the ripple.

The root mean square value of the output voltage may be given by:

$$\begin{aligned}
E_{r.m.s.}^2 &= \frac{1}{T} \int_0^{T/2} E_s^2 dt \\
&= \frac{1}{T} \int_0^{T/2} E_m^2 \sin^2 \omega t dt = \frac{E_m^2}{4} \\
\text{or } E_{r.m.s.} &= \frac{E_m}{2} \quad \text{----- (5.2)}
\end{aligned}$$

The total power delivered to the load resistance is:

$$P_{in} = \frac{E_{r.m.s.}^2}{R_L} = \frac{E_m^2}{4R_L} \quad \text{----- (5.3)}$$

The d.c. power delivered to the load is:

$$P_{d.c.} = \frac{E_{d.c.}^2}{R_L} = \frac{E_m^2}{\pi^2 R_L} \quad (\text{Putting } E_{d.c.} = \frac{E_m}{\pi})$$

Therefore, power delivered in load resistance due to unwanted components i.e. ripple may be given as:

$$\begin{aligned}
P_{\text{ripple}} &= P_{in} - P_{d.c.} \\
&= \frac{E_{r.m.s.}^2}{R_L} - \frac{E_{d.c.}^2}{R_L} \quad \text{----- (5.4)}
\end{aligned}$$

The  $P_{\text{ripple}}$  is equal to  $\frac{E_{a.c.}^2}{R_L}$ . The equation (5.4) may be rewritten as:

$$\frac{E_{a.c.}^2}{R_L} = \frac{E_{r.m.s.}^2}{R_L} - \frac{E_{d.c.}^2}{R_L} \quad \text{or} \quad \gamma = \frac{E_{a.c.}}{E_{d.c.}} = \sqrt{\left(\frac{E_{r.m.s.}^2}{E_{d.c.}^2} - 1\right)}$$

Where  $\gamma$  is the ripple factor and is defined as the ratio of the a.c. components to the d.c. components at the output.

Putting the values of  $E_{d.c.}$  and  $E_{r.m.s.}$  respectively we get:

$$\gamma = \sqrt{\left(\frac{\pi^2}{4} - 1\right)} = 1.21$$

From this equation, it is clear that  $\gamma$  is more than 1, which indicates that at the output, the unwanted a.c. components (ripple) are more than the wanted d.c. components. Hence the half wave rectifier being a poor circuit for rectification is not of much practical use.

**Rectifier Efficiency:** It is useful to define the quantity called the rectifier efficiency, which is defined as:

Rectifier Efficiency  $\eta = (\text{d.c. power input to load}) / (\text{Input power delivered to load})$

$$\begin{aligned}
&= \frac{P_{d.c.}}{P_{in}} \times 100 \% \\
&= \frac{(E_m^2 / \pi^2 R_L)}{(E_m^2 / 4R_L)} \times 100 = \frac{4}{\pi^2} \times 100 = 40.6 \%
\end{aligned}$$

This means, for half wave rectifier, under ideal conditions, only 40.6 % of the a.c. input power is converted into d.c. power in the load resistance.

**Example 5.1** A 12 volt a.c. from the secondary of a transformer is applied to the input of a half wave rectifier circuit having  $10\text{K}\Omega$  load resistance. If the diode is ideal, find:

- (i) Peak value of the a.c. signal
- (ii) D.C. output voltage
- (iii) Peak value of the current through the load resistance
- (iv) Average value of the current through the load resistance
- (v) PIV of the diode

Solution: Given  $E_{r.m.s.} = 12$  Volts,  $R_L = 10\text{K}\Omega$

$$(i) E_m = \sqrt{2}E_{r.m.s.} = 1.414 \times 12 = 16.97 \text{ volts}$$

$$(ii) E_{d.c.} = \frac{E_m}{\pi} = \frac{16.97}{3.14} = 5.4 \text{ volts}$$

$$(iii) I_m = \frac{E_m}{R_L} = \frac{16.97}{10000} = 1.7 \text{ mA}$$

$$(iv) I_{d.c.} = \frac{E_{d.c.}}{R_L} = \frac{5.4}{10000} = 540 \mu\text{A}$$

$$(v) \text{PIV of the diode} = E_m = 16.97 \text{ Volts}$$

**Example 5.2** A P – N junction diode having forward resistance  $R_f = 25\Omega$ , is used in half wave rectifier circuit. The input applied signal is given by  $E_s = 25\sin(100\pi t)$ . If the load resistance  $R_L$  is  $500\Omega$ , then calculate  $I_m$ ,  $I_{r.m.s.}$ ,  $E_{d.c.}$ , d.c. current following through the load resistance and the rectifier efficiency.

Solution: The peak value of the input a.c. is given  $E_m = 25$  Volts

$$I_m = \frac{E_m}{R_f + R_L} = \frac{25}{(25 + 500)} = 0.0476 \text{ A} = 47.6 \text{ mA}$$

$$I_{r.m.s.} = \frac{I_m}{2} = \frac{47.6}{2} = 23.8 \text{ mA}$$

$$E_{d.c.} = \frac{E_m \times R_L}{(R_f + R_L)\pi} = \frac{25 \times 500}{525 \times 3.14} = 7.58 \text{ volts}$$

$$I_{d.c.} = \frac{E_{d.c.}}{R_L} = \frac{7.58}{500} = 15.17 \text{ mA}$$

$$\text{Rectifier Efficiency} \quad \eta = \frac{P_{d.c.}}{P_{in}} \times 100$$

$$P_{d.c.} = I_{d.c.}^2 R_L = (15.17)^2 \times 500 = 0.115 \text{ watt}$$

$$P_{in} = I_{r.m.s.}^2 \times (R_L + R_f) = (23.8)^2 \times 525 = 0.2974 \text{ watt}$$

$$\eta = \frac{P_{d.c.}}{P_{in}} = \frac{0.115}{0.2974} \times 100 = 38.67\%$$

**5.1.2 Full Wave Rectifier:** Figure (5.3) shows the circuit diagram of full wave rectifier. It consists of a centre tapped transformer and two diodes D<sub>1</sub> and D<sub>2</sub> in addition to the load resistance R<sub>L</sub>. The centre tapped transformer converts a sinusoidal signal into two equal sinusoidal signals which are 180° out of phase. In order to understand the operation of this circuit, we consider the diodes are ideal. The two signals E<sub>S1</sub> and E<sub>S2</sub> obtained from the transformer are being applied to the two diodes D<sub>1</sub> and D<sub>2</sub>. During first half cycle of the input wave (E<sub>S</sub>), point A is positive and B is negative with respect to the common terminal. The diode D<sub>1</sub>, therefore, conducts and D<sub>2</sub> is in reverse bias. This causes I<sub>b1</sub> current to flow through the diode D<sub>1</sub> and load resistance R<sub>L</sub>. During the other half cycle, diode D<sub>2</sub> conducts and diode D<sub>1</sub> is in reverse bias. This caused I<sub>b2</sub> current to flow through the diode D<sub>2</sub> and load resistance R<sub>L</sub>.

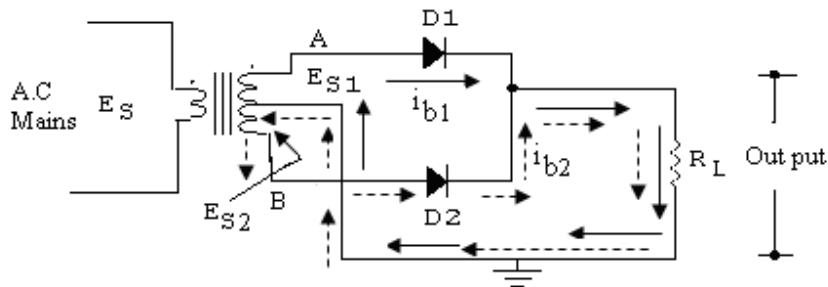


Fig 5.3

Fig. (5.4) shows the input and output waves of the full wave rectifier circuit,

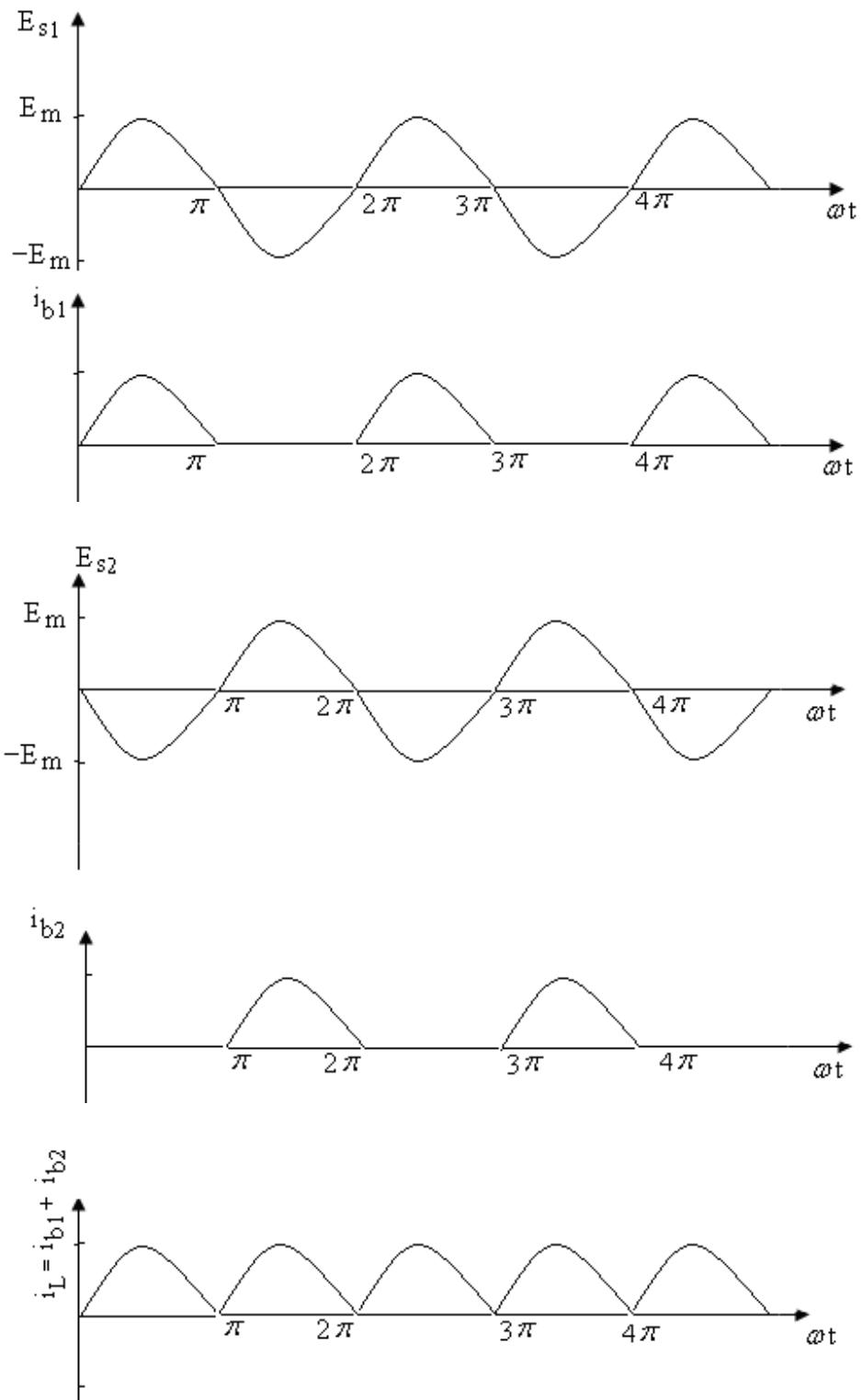


Fig. 5.4

From these wave shapes, it is clear that the direction of current in the load resistance is same for both the half cycles of the output wave. Hence, the circuit is called as full wave rectifier.

**Analysis:** In this circuit the centre tapped terminal of the transformer is used as the common terminal of two voltages  $E_{S1}$  and  $E_{S2}$  which are 180° out of phase.

$$\text{Let } E_{S1} = -E_{S2} = E_m \sin \omega t$$

The average value (d.c.) of the voltage across the load resistance for the full wave rectifier is given by:

$$\begin{aligned} E_{d.c.} &= \frac{1}{T} \left[ \int_0^{\frac{T}{2}} E_{S1} dt + \int_{\frac{T}{2}}^T E_{S2} dt \right] \\ &= \frac{1}{T} \left[ \int_0^{\frac{T}{2}} E_m \sin \omega t dt - \int_{\frac{T}{2}}^T E_m \sin \omega t dt \right] \end{aligned}$$

$$\text{which may be simplified as } = \frac{2 E_m}{\pi}.$$

The r.m.s. value of the voltage across the load resistance is given by:

$$\begin{aligned} E_{r.m.s.}^2 &= \frac{1}{T} \left[ \int_0^{\frac{T}{2}} E_{S1}^2 dt + \int_{\frac{T}{2}}^T E_{S2}^2 dt \right] \\ &= \frac{1}{T} \left[ \int_0^{\frac{T}{2}} E_m^2 \sin^2 \omega t dt + \int_{\frac{T}{2}}^T E_m^2 \sin^2 \omega t dt \right] = \frac{E_m^2}{2} \\ \text{or } E_{r.m.s.} &= \frac{E_m}{\sqrt{2}} \end{aligned}$$

From the Fourier analysis the voltage across the load resistance is given by:

$$E_L = \frac{2E_m}{\pi} - \frac{4E_m}{3\pi} \cos 2\omega t - \frac{4E_m}{15\pi} \cos 4\omega t - \frac{4E_m}{31\pi} \cos 6\omega t - \dots \quad \text{----- (5.5)}$$

It is clear from this equation that first term of the output voltage across the load resistance is the same as that of  $E_{d.c.}$ , calculated above. Further the lowest frequency term (ripple) in the full wave rectifier circuit is twice the frequency of supply signal.

The ripple factor  $\gamma$  is calculated as:

$$\begin{aligned}
\gamma &= \sqrt{\left(\frac{E_{r.m.s.}^2}{E_{d.c.}^2} - 1\right)} = \sqrt{\left(\frac{E_m^2/2}{4E_m^2/\pi^2} - 1\right)} \\
&= \sqrt{\left(\frac{\pi^2}{8} - 1\right)} = 0.48 \quad \text{----- (5.6)}
\end{aligned}$$

It clearly indicates that  $\gamma$  being less than unity has the d.c. components (desired) in the output more than the a.c. components (undesired).

**Rectifier Efficiency:** This is calculated as:

$$\begin{aligned}
\eta &= \frac{P_{d.c.}}{P_{in}} \times 100 \% \\
&= \frac{(4E_m^2/\pi^2 R_L)}{(E_m^2/2R_L)} \times 100 = \frac{8}{\pi^2} \times 100 = 81.2 \%
\end{aligned}$$

Thus for full wave rectifier 81.2 % of the a.c. input power is converted to d.c. output power.

**5.2 Peak Inverse Voltage (PIV):** Peak inverse voltage of a rectifier diode in a circuit is the maximum reverse voltage across the diode. For the rectifier circuit PIV of the diodes used should be less than the break down voltage of the diode. It can be seen from the circuit of half wave rectifier that PIV of the diode used is equal to peak voltage of the applied input a.c. i.e.  $+E_m$ . But in case of full wave rectifier PIV of each diode used is twice the peak voltage of the applied a.c. ( $+2E_m$ ). It is clear from the figure (5.5) of the full wave rectifier that during +ve half cycle of the input wave, the diode is in forward bias and the voltage at the point C may thus reaches to  $+E_m$  and at point B it is  $-E_m$ . So the total reverse voltage across the diode  $D_2$  is  $2E_m$ . Similarly it can be seen that during -ve half cycle PIV of the diode is also  $+2E_m$ . From the above discussion it is clear that in full wave rectifier circuit, we should use the diodes whose break down voltage is greater than  $+2E_m$  (i.e. double the peak value of the input a.c. voltage).

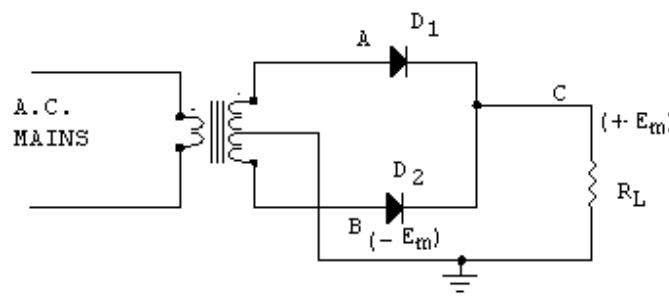


Fig. 5.5

**Disadvantage of Full Wave Rectifier:** The full wave rectifier circuit has the following disadvantages:

- (i) As discussed above, the PIV of the diode used in the circuit is  $+2E_m$ . So such diodes whose break down voltage is greater than  $2E_m$  is to be chosen for this purpose.
- (ii) In this circuit, especially designed transformer called centre tapped transformer is to be used. To rectify the a.c. mains voltage a center tapped transformer of 220-0-220 volts is to be used. However, in case of half wave rectifier circuit, transformer is not to be used if an a.c. main is to be rectified.
- (iii) Since centre terminal of the centre tapped transformer is used as a common terminal (or ground terminal) -ve d.c. output voltage may not be obtained by simply reversing the output terminals; but will be obtained by reversing the diode connections.

**Example 5.3** A full wave rectifier circuit has the input signal  $E_s = 100\sin(100\pi t)$ ,  $R_L = 900 \Omega$  and each diode has the forward resistance of  $100 \Omega$ . Calculate

- (i) Peak value of the current through the load resistance,
- (ii) D.C. load current,
- (iii) D.C. output voltage
- (iv) Rectifier Efficiency

Solution: Given  $E_m = 100$  Volts,  $R_L = 900 \Omega$ ,  $R_f = 100\Omega$

$$(i) I_m = \frac{E_m}{R_L + R_f} = \frac{100}{900 + 100} = 100mA$$

$$(ii) I_{d.c.} = \frac{2I_m}{\pi} = \frac{2 \times 100}{3.14} = 63.7mA$$

$$(iii) E_{d.c.} = I_{d.c.} R_L = 63.7mA \times 900 = 57.3 \text{ Volts}$$

$$(iv) \text{Rectifier Efficiency } \eta = \frac{P_{d.c.}}{P_{in}} \times 100$$

$$P_{d.c.} = I_{d.c.}^2 R_L = (63.7)^2 \times 900 = 3.65 \text{ watt}$$

$$P_{in} = I_{r.m.s.}^2 \times (R_L + R_f) = \frac{I_m^2}{\sqrt{2}\sqrt{2}} \times 1000 = \frac{100 \times 100 \times 1000 \times 10^{-6}}{2} = 5 \text{ watt}$$

$$\eta = \frac{P_{d.c.}}{P_{in}} = \frac{3.65}{5} \times 100 = 73\%$$

**Example 5.4** A 15 – 0 – 15 volts transformer is used for full wave rectifier circuit. Each diode has a forward resistance of  $10\Omega$ . The load resistance is  $600 \Omega$ . Find  $E_{d.c.}$ ,  $I_{d.c.}$ ,  $I_{r.m.s.}$ , and rectifier efficiency  $\eta$ .

Solution:  $R_f = 10 \Omega$ ,  $R_L = 600 \Omega$ ,  $E_{r.m.s.} = 15$  Volts

$$E_m = 15 \times \sqrt{2} = 21.21 \text{ volts}$$

$$E_{d.c.} = \frac{2E_m}{(R_f + R_L)} \cdot R_L = \frac{2 \times 21.21 \times 600}{(10 + 600)} = 41.72 \text{ volts}$$

$$I_{d.c.} = \frac{E_{d.c.}}{R_L} = \frac{41.72}{600} = 69.5mA$$

$$I_{r.m.s.} = \frac{E_m}{\sqrt{2}(R_f + R_L)} = \frac{21.21}{1.414 \times 610} = 24.6mA$$

$$\eta = \frac{0.812}{(R_f + R_L)} \cdot R_L = \frac{0.812}{(1 + \frac{R_f}{R_L})}$$

$$= \frac{0.812}{(1 + \frac{20}{600})} \times 100 = \frac{0.812 \times 30 \times 100}{31} = 78.6\%$$

**5.3 Bridge Rectifier:** The disadvantages that we have in case of full wave rectifier will be removed in the Bridge Rectifier. The basic circuit diagram of bridge rectifier is shown in Fig. (5.6). This circuit has four diodes connected in the four arms of a bridge, hence the name bridge rectifier. To understand the working of this circuit let us consider that during +ve half cycle of the input  $E_s$ , the point A is +ve with respect to B. In this condition, diodes D<sub>1</sub> and D<sub>3</sub> conducts and diodes D<sub>2</sub> and D<sub>4</sub> are in reverse bias. The current flows in the load resistance  $R_L$ , in the direction of arrow as shown in fig. (5.6a). During the next half cycle the point B is +ve with respect to A and thus diodes D<sub>2</sub> and D<sub>4</sub> conducts and diodes D<sub>1</sub> and D<sub>3</sub> goes in reverse bias. This also causes the flow of current through the load resistance  $R_L$  in the same direction which is shown by dotted lines in the figure 5.6(b).

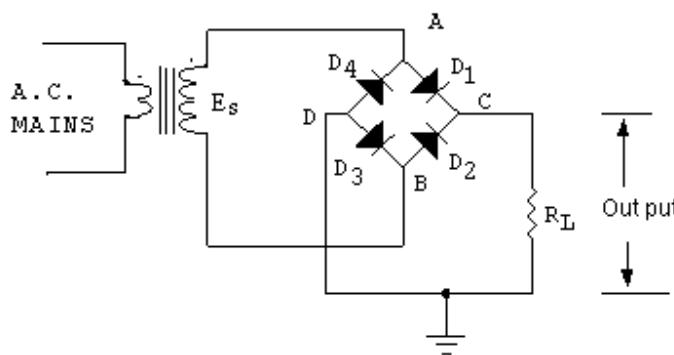


Fig. 5.6

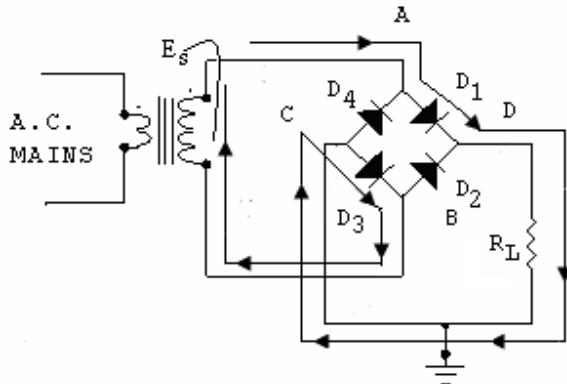


Fig. 5.6(a)

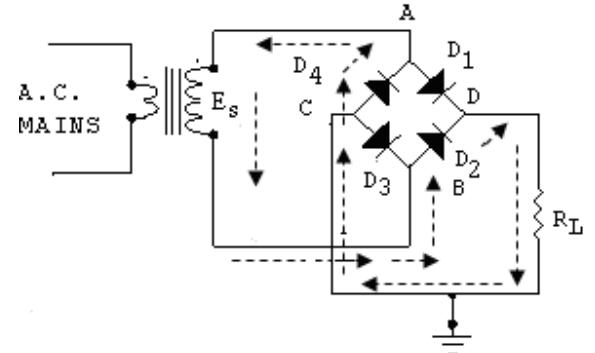


Fig. 5.6(b)

The output wave form of the bridge rectifier is essentially the same as in the case of full wave rectifier.

#### Advantages of Bridge Rectifier:

- (i) No especially designed center tapped transformer is required in the bridge rectifier circuit.
- (ii) There is no common terminal (common between input and output), so -ve supply may be obtained just by reversing the output terminals.
- (iii) The peak inverse voltage across any of the four diodes in the bridge rectifier circuit is equal to  $E_m$  and not  $+2E_m$  as in the case of full wave rectifier.
- (iv) For the same output voltage, the transformer secondary line – to – line voltage, in the bridge rectifier should be one half of that used for full wave rectifier. Thus bridge rectifier supply large amount of d.c. power.

**Example 5.5** The forward resistance of each diode used in bridge rectifier is  $10\ \Omega$ . The a.c. voltage used to the input is 230 volts and load current is  $1K\ \Omega$ . Find  $E_{d.c.}$ ,  $I_{d.c.}$ ,  $I_m$ , a.c. current to the load  $I_{r.m.s.}$  and PIV of the diodes used in the circuit.

Solution:  $E_{r.m.s.} = 230\text{ Volts}$   $R_f = 10\Omega$   $R_L = 1000\ \Omega$

$$E_m = 230\sqrt{2} = 325.22\text{ Volts}$$

$$E_{d.c.} = \frac{2E_m x R_L}{(2R_f + R_L)\pi} = \frac{2 \times 325.22 \times 1000}{(20 + 1000) \times 3.14} = 203.1\text{ Volts}$$

(Here  $2R_f$  is used in place of  $R_f$  as two diodes go in forward bias at a time)

$$I_{d.c.} = \frac{E_{d.c.}}{R_L} = \frac{203.1}{1000} = 203.1mA$$

$$I_m = \frac{E_m}{(2R_f + R_L)} = \frac{325.22}{(20 + 1000)} = 319mA$$

PIV of the diodes =  $E_m = 325.22$  Volts

**5.4 Filter Circuits:** In the preceding section we have studied the rectifier circuits. The rectified output contains a large amount of unwanted a.c. components (ripples) in addition to the d.c. voltage. The ripple can be eliminated or considerably reduced by using a filter circuit between the output of the rectifier and the load resistance. We shall now study the different commonly used filter circuits.

**5.4.1 Half Wave Rectifier with Shunt Capacitor Filter:** Figure (5.7) shows the circuit diagram of a half wave rectifier with shunt capacitor filter. In this circuit a capacitor C is connected in parallel (in shunt) with  $R_L$  hence it is called shunt capacitor filter. The operation of this circuit may be explained as follows:

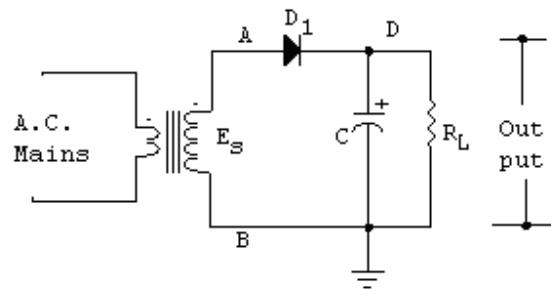


Fig. 5.7

During the voltage rise of +ve half cycle of the input wave  $E_s$ , the diode conducts and the output follows as the input voltage at point A. The capacitor C starts charging and thus it charges to the maximum of peak voltage  $E_m$  of the input wave  $E_s$ . Further during the decrease of the input wave from  $E_m$  to zero of the same half cycle, the diode D is in reverse bias. The output seems to be disconnected from the point A and the capacitor C will now start discharging through the load resistance  $R_L$ . The  $R_LC$  time constant is chosen large enough compared to half the time period of the input wave, so that the capacitor C is not completely discharged. As soon as the input voltage again becomes greater than the output voltage (during the next +ve half cycle) the diode again conducts and capacitor C starts charging further. In this way the cycle repeats. The input and output wave with shunt capacitor filter is shown in Fig. (5.8).

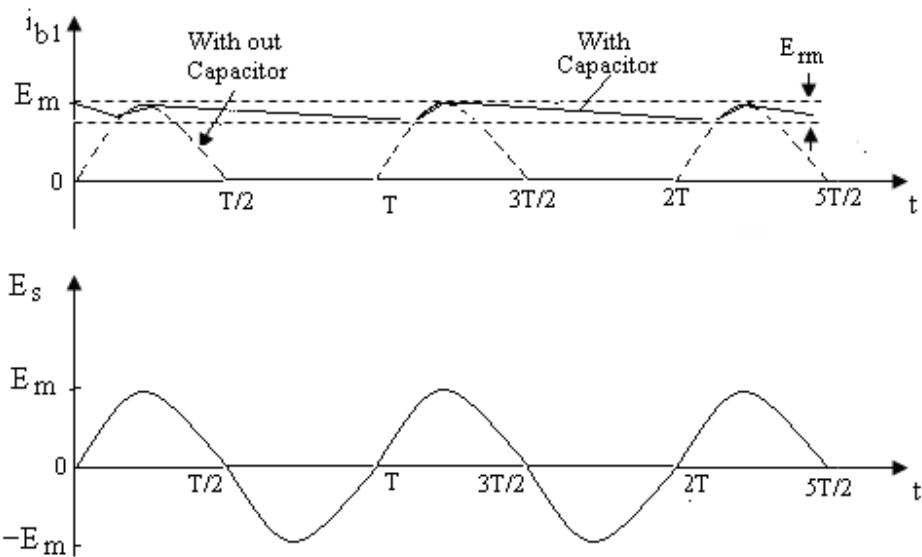


Fig. 5.8

The discharging path will depend on the  $R_L C$  time constant. Since it is large, the discharging path will therefore, seem to be almost linear.

**Calculation of ripple factor:** Given input signal is  $E_s = E_m \sin \omega t$

The total change in the output (ripple voltage) is shown in Fig. (5.8). The average value of this triangular wave is approximately half the total change in the output wave ( $E_R$ ),

$$\text{which is given by: } E_{d.c.} = E_m - \frac{E_R}{2} . \quad \text{--- (5.7)}$$

For the good filtering action the discharge period  $T_2$  should be very much greater than the charging period  $T_1$  i.e.

$T_2 \gg T_1 \approx T$  (say) where  $T$  is the time period of the one complete cycle.

For simplicity of analysis the ripple voltage is approximated the exact triangular wave as shown in Fig.(5.9).

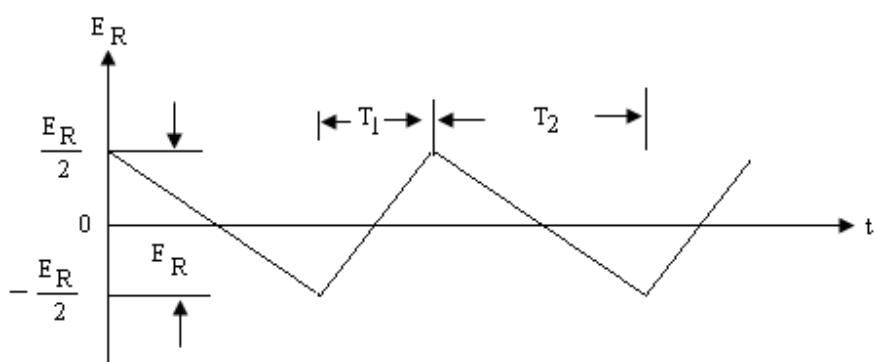


Fig. 5.9

The equation of the Triangular wave is given by:

$$E = A_1 + A_2 \cdot t \quad \text{----- (5.8)}$$

where  $A_1$  and  $A_2$  are constants which may be obtained from the boundary conditions:

$$E = \frac{E_R}{2} \quad \text{at } t = 0 \quad \text{and} \quad E = -\frac{E_R}{2} \quad \text{at } t = T \quad \text{----- (5.9)}$$

$$\text{so we get from equations (5.8) \& (5.9)} \quad A_1 = \frac{E_R}{2} \quad \& \quad A_2 = -\frac{E_R}{T}$$

$$\text{The wave equation (5.8) will become} \quad E = \frac{E_R}{2} - \frac{E_R}{T} \cdot t$$

The r.m.s. value of the ripple voltage is given by:

$$\begin{aligned} E_{r.m.s.}^2 &= \frac{1}{T} \int_0^T E^2 dt \\ &= \frac{E_R^2}{T} \int_0^T \left[ \frac{1}{2} - \frac{t}{T} \right]^2 dt \\ &= \frac{E_R^2}{T} \int_0^T \left( \frac{1}{4} + \frac{t^2}{T^2} - \frac{t}{T} \right) dt = \frac{E_R^2}{12} \end{aligned}$$

$$\text{or} \quad E_{r.m.s.} = \frac{E_R}{2\sqrt{3}} \quad \text{----- (5.10)}$$

During the discharge period  $T_2$ , the capacitor loses the charge  $I_{d.c.} \cdot T_2$  at a constant rate. Hence the change in capacitor voltage  $E_R$  is calculated as:

$$E_R = (\text{Loss of charge}) / (\text{capacity of the capacitor})$$

$$= \frac{I_{d.c.} \cdot T_2}{C} \quad \text{----- (5.11)}$$

It has already been assumed that  $T_2 = T = \frac{1}{f}$  for good filtering action. Where  $f$  is the frequency of the wave in Hz.

$$\text{So} \quad E_R = \frac{I_{d.c.}}{f \cdot C} \quad \text{----- (5.12)}$$

From the equations (5.7) & (5.12) we get :

$$E_{d.c.} = E_m - \frac{I_{d.c.}}{2 f \cdot C}$$

The term  $\frac{1}{2 f \cdot C}$  has the dimension of resistance, which represents the source resistance

of d.c. supply  $E_{d.c.}$ ; and may assumed to be an open circuit voltage. For having the low ripple voltage and ensure good voltage regulation the capacitor  $C$  must be large enough. The ripple factor  $\gamma$  is given by:

$$\gamma = (\text{r.m.s. value of a.c. output})/(\text{d.c. output voltage})$$

$$\begin{aligned}
 &= \frac{E_R}{2\sqrt{3} \cdot E_{d.c.}} && (\text{since } E_R = \frac{I_{d.c.}}{f \cdot C}) \\
 &= \frac{1}{2\sqrt{3} \cdot f \cdot C \cdot R_L} && (\text{where } \frac{E_{d.c.}}{I_{d.c.}} = R_L) \quad \text{-----(5.13)}
 \end{aligned}$$

From this equation it is clear that we may get small ripple content at high load resistance. At no load ( $R_L \rightarrow \infty$ ) the output voltage will be equal to  $E_m$ , the open circuit voltage of the d.c. supply; and we thus say that this circuit behaves like a peak detector. This filter is suitable for low current.

The PIV of the diode used in half wave rectifier with shunt capacitor filter is approximately  $2E_m$  since the point D (in fig. 5.7), the cathode of the diode is at about  $+E_m$  potential and anode goes to  $-E_m$  with respect to common point. Hence the total reverse voltage across the diode is  $2E_m$ .

**Example 5.6** A transformer whose secondary winding is rated at 12 volts r.m.s., is used for half rectifier with shunt capacitor filter. If the value of capacitor  $C = 100 \mu\text{F}$  and load resistance  $R_L = 1\text{K}\Omega$  and frequency  $f = 50 \text{ Hz}$ , determine  $E_{d.c.}$  and  $I_{d.c.}$ , peak to peak ripple voltage at the output, peak forward current in the diode. How do the above change if  $C$  is increased to  $1000 \mu\text{F}$ ? What should be voltage ratings of the capacitor, if 25% variation is allowed in the input a.c. voltage.

Solution:  $C = 100 \mu\text{F}$   $R_L = 1000 \Omega$   $E_{\text{r.m.s.}} = 12 \text{ volts}$   $f = 50 \text{ Hz}$

$$E_m = 12\sqrt{2} = 12 \times 1.414 = 16.97 \text{ Volts}, \quad I_{d.c.} = \frac{E_{d.c.}}{R_L}$$

$$E_{d.c.} = E_m - \frac{I_{d.c.}}{2f \cdot C} = E_m - \frac{E_{d.c.}}{2f \cdot C \cdot R_L}$$

or

$$E_{d.c.} \left(1 + \frac{1}{2f \cdot C \cdot R_L}\right) = E_m \quad \text{and} \quad E_{d.c.} = \frac{E_m}{\left(1 + \frac{1}{2f \cdot C \cdot R_L}\right)}$$

$$E_{d.c.} = \frac{16.97}{1 + \frac{1}{2 \times 50 \times 100 \times 10^{-6} \times 1000}} = \frac{16.97}{1.1} = 15.43 \text{ Volts}$$

$$I_{d.c.} = \frac{E_{d.c.}}{R_L} = \frac{15.43}{1000} = 15.43mA$$

Peak to peak ripple voltage at the output  $E_R$  is given by:

$$E_R = \frac{I_{d.c.}}{f \cdot C} = \frac{15.43 \times 10^{-3}}{50 \times 100 \times 10^{-6}} = 3.086 \text{ Volts}$$

$$\text{Peak forward current in the diode } I_m = \frac{E_m}{R_L} = \frac{16.97}{1000} = 16.97mA$$

Now the value of  $C$  is increased to  $1000 \mu\text{F}$  so put  $C = 1000 \mu\text{F}$  in the above calculations, we get:

$$Ed.c. = \frac{16.97}{1 + \frac{1}{2 \times 50 \times 1000 \times 10^{-6} \times 1000}} = \frac{16.97}{1.1} = 16.8 \text{ Volts}$$

$$I_{d.c.} = \frac{E_{d.c.}}{R_L} = \frac{16.8}{1000} = 16.8mA$$

$$E_R = \frac{I_{d.c.}}{f.C} = \frac{16.8 \times 10^{-3}}{50 \times 1000 \times 10^{-6}} = 0.336 \text{ Volts}$$

$$I_m = \frac{E_m}{R_L} = \frac{16.97}{1000} = 16.97mA$$

If 25% increase in the a.c. signal then peak voltage also increases in the same ratio i.e.

$$E_m = 16.97 + 0.25 \times 16.97 = 21.2 \text{ Volts}$$

So the voltage rating of the capacitor should be greater than 21.2 Volts may be taken of 25 Volts or 50 volts.

**5.4.2 Full Wave Rectifier with Shunt Capacitor Filter:** The circuit diagram of this filter is shown in figure (5.10). The working of this circuit is similar to that of the half wave rectifier with shunt capacitor filter; the only difference between the two is that the circuit works for the half cycles. The input – output wave shaped is given in figure (5.11).

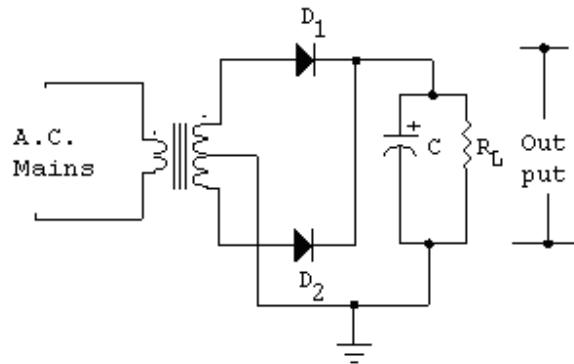


Fig. 5.10

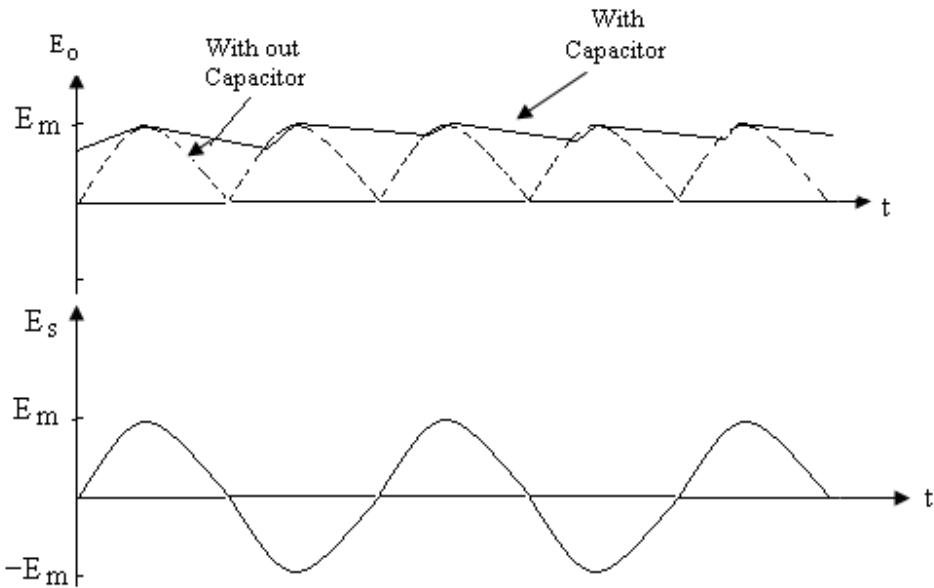


Fig. 5.11

The ripple factor for the full wave rectifier with shunt capacitor filter may also be calculated in the similar fashion as for half wave case simply by replacing  $T_2 \approx T/2$ . Since in this case, the discharge period  $T_2$  must be greater than  $T/2$ . So  $T_2$  is assumed to be equal to  $T/2$ .

The ripple factor  $\gamma$  is given by:

$$\gamma = \frac{1}{4\sqrt{3} \cdot f \cdot C \cdot R_L} \quad \text{----- (5.14)}$$

**5.4.3 Percentage Regulation:** The percentage regulation of a d.c. power supply may be defined as:

Percentage regulation = **(No load voltage – Full load voltage) / Full load voltage**

If the supply designed by the rectifier and filter, then it can be represented by the model of the battery, i. e., a voltage source  $E_i$  (open circuit voltage) and a source resistance  $R_0$  in series with it as given in figure (5.12).

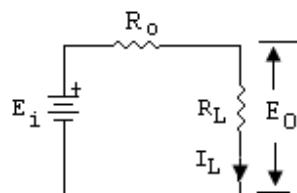


Fig. 5.12

From this figure we get  $E_i = R_0 I_L + E_0$  and  $E_0 = R_L I_L$

or  $E_i - E_0 = R_0 I_L$

$E_i$  = No load voltage  $E_0$  = Full load voltage

$$\text{So Percentage regulation} = \frac{R_0 I_L}{R_L I_L} \times 100\% = \frac{R_0}{R_L} \times 100\%$$

**Example 5.7** A full wave rectifier is supplied with an a.c. signal of 50 – 0 – 50 volts r.m.s. and 50 Hz frequency. A 100  $\mu\text{F}$  capacitor serves as a filter and takes 300 mA load current. What is the d.c. load voltage? Also find the ripple factor.

Solution:  $E_{\text{r.m.s.}} = 50 \text{ Volts}$ ,  $f = 50 \text{ Hz}$ ,  $C = 100 \mu\text{F}$ ,  $I_{\text{d.c.}} = 300 \text{ mA}$

$$E_m = 50 \times \sqrt{2} = 50 \times 1.414 = 70.7 \text{ Volts}$$

For full wave rectifier with shunt capacitor filter is given by:

$$\begin{aligned} E_{\text{d.c.}} &= E_m - \frac{I_{\text{d.c.}}}{4 f C} \\ &= 70.7 - \frac{300 \times 10^{-3}}{4 \times 50 \times 100 \times 10^{-6}} = 70.7 - 15 = 55.7 \text{ Volts} \\ R_L &= \frac{E_{\text{d.c.}}}{I_{\text{d.c.}}} = \frac{55.7}{300 \times 10^{-3}} = 185.7 \Omega \\ \gamma &= \frac{1}{4\sqrt{3} \cdot f \cdot C \cdot R_L} = \frac{1}{4 \times 1.73 \times 50 \times 100 \times 10^{-6} \times 185.7} \\ &= 0.156 = 15.6\% \end{aligned}$$

**Example 5.8** It is required to design full wave rectifier with shunt capacitor filter which is capable of supplying 20 volts d.c. at no load. The regulation of this supply is required to be less than 10% for a full load current of 1 ampere. The maximum ripple is to be less than 3 volts (peak to peak). Find (i) the required secondary rating of the transformer, (ii) the value and voltage rating of the capacitor, (iii) the peak forward current and PIV ratings of the diodes.

Solution: No load voltage  $E_{\text{d.c.}} = 20 \text{ Volts}$ , % regulation = 10%

Percentage regulation = (No load voltage – Full load voltage)  $\times 100 / \text{Full load voltage}$

$$10 = (20 - \text{Full load voltage}) \times 100 / \text{Full load voltage}$$

or Full load voltage = 18.18 volts

The full load voltage should be greater than 18.18 volts say 18.5 Volts

Ripple voltage  $E_R = 3 \text{ Volts}$  (peak to peak)

$$E_R = \frac{I_{\text{d.c.}}}{2 \cdot f \cdot C} = \frac{1 \text{ amp}}{2 \times 50 \times C} = 3 \text{ volts}$$

$$\text{or } C = \frac{1}{300} = 0.003333 F = 3333 \mu\text{F}$$

$$R_L = \frac{E_{\text{d.c.}}}{I_{\text{d.c.}}} = \frac{18.5}{1 \text{ amp}} = 18.5 \Omega$$

$$\text{We know } I_{\text{d.c.}} R_L = E_m - \frac{I_{\text{d.c.}}}{4 f C}$$

$$I_{d.c.} = \frac{E_m}{(R_L + \frac{1}{4.f.C})} \quad \text{or} \quad E_m = I_{d.c.}(R_L + \frac{1}{4.f.C})$$

$$Em = 1(18.5 + \frac{300}{4 \times 50 \times 1}) = 20 \text{ volts}$$

$$Er.m.s. = \frac{Em}{\sqrt{2}} = \frac{20}{1.414} = 14.14 \text{ volts} = 15 \text{ (say)}$$

(i) So secondary of the transformer should be rated as 15 – 0 – 15 volts and current 1amp.

(ii) The value of capacitor C= 3333  $\mu$ F and voltage ratings should greater than 20 volts.

(iii) Peak forward current  $I_m = \frac{E_m}{R_L} = \frac{20}{18.5} = 1.08 \text{ amp}$

PIV of the diodes =  $2E_m = 40$  volts

**5.4.4 Series Inductor Filter:** The circuit diagram of the series inductor filter is shown in figure (5.13). Here an inductance is connected in series with the load resistance. Therefore, it is known as series inductor filter. The signal  $E_I$  has the d.c. components along with the higher harmonics of input frequency  $\omega$ .  $E_I$  is given by:

$$E_I = \frac{2E_m}{\pi} - \frac{4E_m}{3\pi} \cos 2\omega.t - \frac{4E_m}{15\pi} \cos 4\omega.t - \dots$$

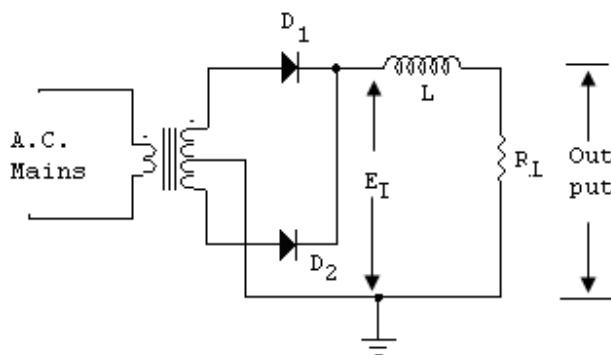


Fig. 5.13

Inductance L is connected to eliminate or reduce the ripple content at the output.

Out of the ripple contents, the second harmonic term  $\frac{4E_m}{3\pi} \cos \omega.t$  is the only effective term. Other terms may be neglected. The inductance offers zero reactance for d.c. components and thus d.c. voltage appears at the output terminals. However, it offers very high reactance for the second and other higher harmonic terms. Thus the inductance attenuates the a.c. components to appear at the output terminals.

Now the ripple for this type of filter is calculated as below:

Peak value of the a.c. components to appear at the output is

$$E_{a.c.} = \frac{4E_m}{3\pi} \cdot \frac{R_L}{(R_L + X_L)} \quad \text{where } X_L = 2j\omega L, \text{ is the inductive}$$

reactance at second harmonic frequency  $2\omega$ . The root mean square value of this ripple content is :

$$E_{r.m.s.} = \frac{4E_m}{3\sqrt{2}\pi} \frac{R_L}{(R_L + X_L)}$$

$$|E_{r.m.s.}| = \frac{4E_m}{3\sqrt{2}\pi} \frac{R_L}{\sqrt{[R_L + 4\omega^2 L^2]}} = \frac{4E_m}{3\sqrt{2}\pi} \sqrt{\left(1 + \frac{4\omega^2 L^2}{R_L^2}\right)}$$

$$\text{If } \frac{4\omega^2 L^2}{R_L^2} \gg 1 \quad \text{then} \quad |E_{r.m.s.}| = \frac{2E_m \cdot R_L}{3\sqrt{2}\pi \cdot \omega \cdot L}$$

$$E_{d.c.} = \frac{2E_m}{\pi}$$

$$\text{The ripple factor } \gamma = \frac{E_{r.m.s.}}{E_{d.c.}} = \frac{2E_m R_L / 3\sqrt{2}\pi\omega}{2E_m} = \frac{1}{3\sqrt{2}} \cdot \frac{R_L}{\omega \cdot L} \quad \text{----- (5.15)}$$

From this equation, it is clear that the ripple factor depends on both the load resistance and the magnitude of the inductances. The ripple factor decrease with the increase of inductance; and also it is smaller for smaller value of  $R_L$ . That is the inductor filter is suitable for higher value of load current.

**Example 5.9** A full wave rectifier with series inductor filter has the load resistance of  $1K\Omega$  and inductor of 25 Henry. The peak value of the applied a.c. signal is 50 volts and frequency 50Hz. Calculate d.c. output voltage, d.c. current to the load resistance and the ripple factor. Diodes used are ideal.

Solution:  $L = 25 \text{ Henry}$   $E_m = 50 \text{ Volts}$   $R_L = 1000 \Omega$   $f = 50 \text{ Hz}$

$$E_{d.c.} = \frac{2E_m}{\pi} = \frac{2 \times 50}{3.14} = 31.85 \text{ Volts}$$

$$I_{d.c.} = \frac{E_{d.c.}}{R_L} = \frac{31.85}{1000} = 31.85mA$$

$$\text{Ripple factor } \gamma = \frac{1}{3\sqrt{2}} \cdot \frac{R_L}{\omega \cdot L} = \frac{R_L}{3\sqrt{2} \times 2\pi f} = \frac{1000}{3 \times 1.414 \times 2 \times 3.14 \times 50} = 0.75$$

**5.4.5 L -Section ( or L-C) Filter:** It has been discussed earlier that the shunt capacitor filter is used for small value of load currents and inductor filter is suitable where we wish to draw large amount of currents. The series combination of inductor and

capacitor used for the filtering action is suitable for all values of the currents. Figure (5.14) shows the circuit diagram of L-section or L-C filter with full wave rectifier.

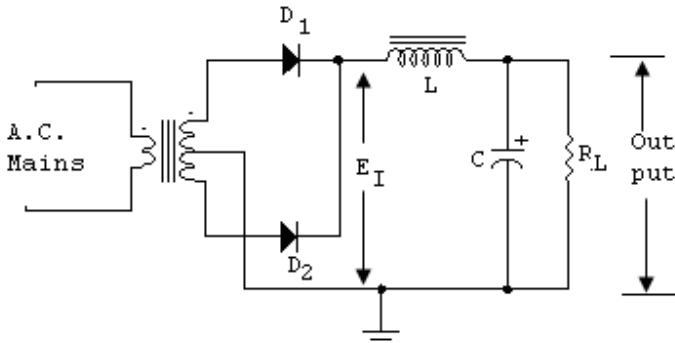


Fig. 5.14

In this circuit, the values of inductance  $L$  and capacitance  $C$  are chosen so that  $X_L$  (inductive reactance) is much greater than  $X_C$  (capacitive reactance) at the ripple frequency. In this way the inductor attenuates the ripple and capacitor bypasses it.

The voltage  $E_I$  available at the input of the L-section filter is given by:

$$E_I = \frac{2E_m}{\pi} - \frac{4E_m}{3\pi} \cos 2\omega.t - \frac{4E_m}{15\pi} \cos 4\omega.t - \dots$$

Higher Harmonic terms (having frequency more than  $2\omega$ ) may be neglected. The effective ripple frequency may be assumed as  $2\omega$ .

$$E_{d.c.} = \frac{2E_m}{\pi}$$

The a.c. components (ripple content) at the output terminals may be given by:

$$E_{a.c.} = \frac{4E_m \cdot (X_C \| R_L)}{3\pi \cdot (X_L + X_C \| R_L)} \cos 2\omega.t$$

It is further assumed that  $X_L$  (inductive reactance at  $2\omega$  frequency) is large enough than the parallel combination of load resistance  $R_L$  and  $X_C$  (capacitive reactance at  $2\omega$  ripple frequency) also  $R_L \gg X_C$ .

$$\text{So } E_{a.c.} = \frac{4E_m \cdot X_C}{3\pi \cdot X_L} \cos 2\omega.t$$

The r.m.s. value of a.c. component is

$$E_{r.m.s.} = \frac{4E_m}{3\sqrt{2}\pi} \frac{X_C}{X_L}$$

Putting  $X_C = \frac{1}{2\omega C}$  (capacitive reactance at  $2\omega$  ripple frequency)

and  $X_L = 2\omega L$  (inductive reactance at  $2\omega$  ripple frequency)

$$\text{we get } E_{r.m.s.} = \frac{4E_m}{3\sqrt{2}\pi\omega^2 \cdot 2\omega L \cdot 2\omega C} = \frac{E_m}{3\sqrt{2}\pi\omega^2 L C}$$

The ripple factor  $\gamma$  is given as:

$$\gamma = \frac{E_{r.m.s}}{E_{d.c.}} = \frac{E_m / (3\sqrt{2}\pi\omega^2 LC)}{2E_m / \pi}$$

or

$$\gamma = \frac{1}{6\sqrt{2}\omega^2 LC} \quad \text{----- (5.16)}$$

It is clear from this equation that the ripple factor is independent of load resistance. So this filter circuit is suitable for all values of currents.

**5.4.6  $\pi$  -Section Filter:** A more common filter is the  $\pi$  -Section Filter shown in figure (5.15). It has a capacitor filter followed by L-section filter and is used to provide

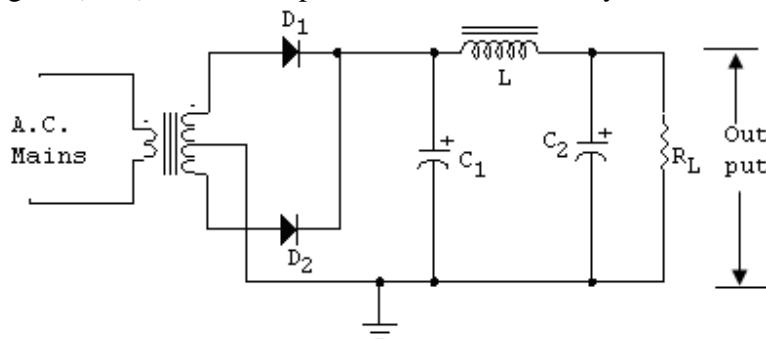


Fig. 5.15

higher d.c. output voltage with low ripple. It is used for medium load currents. The capacitors  $C_1$ ,  $C_2$  and inductance  $L$  form a  $\pi$ -type network, hence it is known as  $\pi$  -Section filter. Here the capacitor  $C_1$  bypasses the ripple frequency, the inductance  $L$  attenuates the ripple and  $C_2$  further bypasses it. So it is assumed that pure d.c. is available at the output.

The r.m.s. value of a.c. components (ripple content) across the capacitor  $C_1$  is given by:

$$E_{r.m.s.} = \frac{I_{d.c.}}{4\sqrt{3}fC_1} = \frac{\pi I_{d.c.}}{2\sqrt{3}\omega C_1} \quad \text{where } \omega = 2\pi f$$

The r.m.s. value of the a.c. voltage across the parallel combination of  $C_2$  and  $R_L$  may be calculated as:

$$E'_{r.m.s.} = \frac{E_{r.m.s.}(X_{C_2} \| R_L)}{(X_L + X_{C_2} \| R_L)} \cong \frac{I_{d.c.} \pi X_{C_2}}{2\sqrt{3}\omega C_1 X_L} \quad (\text{since } X_L \gg X_{C_2} \text{ and } R_L \gg X_{C_2})$$

$$R_L \gg X_{C_2})$$

$$\text{Putting } X_C = \frac{1}{2\omega C} \quad (\text{capacitive reactance at } 2\omega \text{ ripple frequency})$$

$$\text{and } X_L = 2\omega L \quad (\text{inductive reactance at } 2\omega \text{ ripple frequency})$$

$$\text{We get } E'_{r.m.s.} \cong \frac{\pi I_{d.c.}}{8\sqrt{3}\omega^3 C_1 C_2 L}$$

d.c. voltage across the load resistance

$$E_{d.c.} = I_{d.c.} R_L$$

The ripple factor is given by:

$$\gamma = \frac{E'_{r.m.s.}}{E_{d.c.}} = \frac{\pi I_{d.c.}}{8\sqrt{3}\omega^3 C_1 C_2 L I_{d.c.} R_L}$$

or  $\gamma = \frac{\pi}{8\sqrt{3}\omega^3 C_1 C_2 L R_L}$  ----- (5.17)

the ripple factor is inversely proportional to the load resistance.

We can, of course, use more than one section of filters depending upon the extent of ripple reduction as shown in figure (5.16). Each section acts like a voltage divider; the overall attenuation equals the product of the individual attenuation.

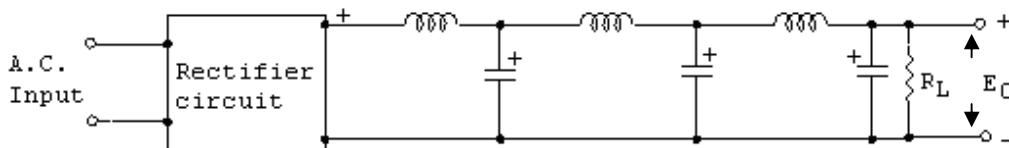


Fig. 5.16

**Example 5.10** A full wave rectifier with  $\pi$  – section filter has the following circuit elements.  $C_1 = C_2 = 20 \mu F$ ,  $L = 20H$ ,  $R_L = 5K\Omega$ , peak value of the a.c. signal 200 volts and frequency = 50 Hz. Find the ripple factor of this circuit.

Solution: The ripple factor  $\gamma$  is given by  $\gamma = \frac{\pi}{8\sqrt{3}\omega^3 C_1 C_2 L R_L}$

or  $\gamma = \frac{3.14}{8x\sqrt{3}(2x3.14x50)^3 x 20x20x10^{-6} x 10^{-6} x 20x5000}$

$$= 0.002 = 0.02\%$$

**5.5 Voltage Multiplier Circuits:** Some times high voltage / low current d.c. supply is required in electronic circuits. Such a supply is needed for accelerating the electrons in a cathode ray tube of CRO. Voltage multiplier circuits are used to design such a supply, it gives a d.c. output which is a multiple of the peak value of the input a.c. signal applied to the circuit.

**5.5.1 Half Wave Voltage Doubler:** As the name indicates it gives d.c. output which is almost double the peak value of the input signal. It is also known as the cascade voltage doubler. The basic circuit diagram of the half wave voltage doubler is shown in figure (5.17a).

It works as follows. During the negative half cycle of the input sinusoidal wave, diode  $D_1$  conducts and the capacitor  $C_1$  charges to the maximum of the peak value of the input wave ( $E_m$ ) with the polarity of the capacitor as shown in figure (5.17). The diode  $D_2$  will be in the reverse bias. Now during the positive half cycle of the input wave, diode  $D_1$  will

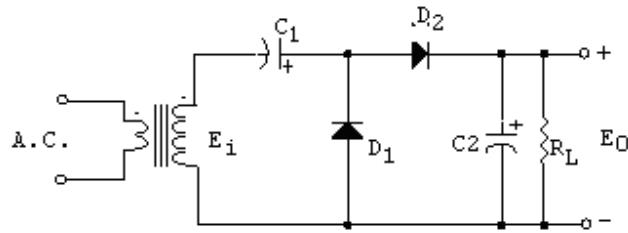


Fig. 5.17

be in reverse bias and diode  $D_2$  conducts as the voltage across the diode  $D_1$  is positive and its magnitude will be approximately equal to double the peak value of the input sinusoidal wave. The capacitor  $C_2$  will charge to steady voltage  $+2E_m$  for the number of cycles of operations. So the output voltage  $E_0$  which is equal to the double of the peak value of the input will be available across the load resistance  $R_L$ . Hence this circuit is known as voltage doubler. The PIV ratings of the diodes used in this circuit, is  $2E_m$ . Half wave voltage doubler has very poor regulation and its ripple content is also high as ripple frequency is equal to the frequency of the input signal.

**5.5.2 Full Wave Voltage Doubler:** The basic circuit diagram of the full wave voltage doubler is shown in figure (5.18). It works as follows.

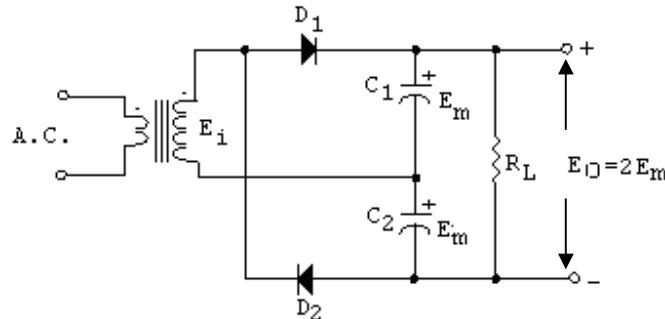


Fig. 5.18

During the first positive half cycle of the input sinusoidal signal of the wave the diode  $D_1$  will conduct and capacitor  $C_1$  charges to the maximum of the peak value  $E_m$  of the wave, with the polarity of the capacitor  $C_1$ . In this case, the diode  $D_2$  will be in reverse bias. Now during the next negative half cycle of the input wave, diode  $D_1$  will be in reverse bias and diode  $D_2$  will conduct and capacitor  $C_2$  will charge to  $E_m$ . The total voltage across the load resistance  $R_L$  will be just double of the peak value of the input wave i.e.  $+2E_m$ . The PIV ratings of the diodes used in this circuit, is  $2E_m$ . The ripple frequency in this circuit is equal to twice the frequency of the input signal (second harmonic terms).

**5.5.3 Half Wave Voltage Multiplier:** The half wave voltage doubler discussed above can be extended to obtain any multiple of the peak value of the input wave i.e.  $3E_m$ ,  $4E_m$ ,  $5E_m$ ,  $6E_m$  etc. The circuit thus obtained may be called as voltage multiplier which is shown in figure (5.19).

The circuit may be explained on the same lines as the half wave voltage doubler. The voltage obtained across A & B terminals is equal to  $2E_m$ , and the voltage across A &

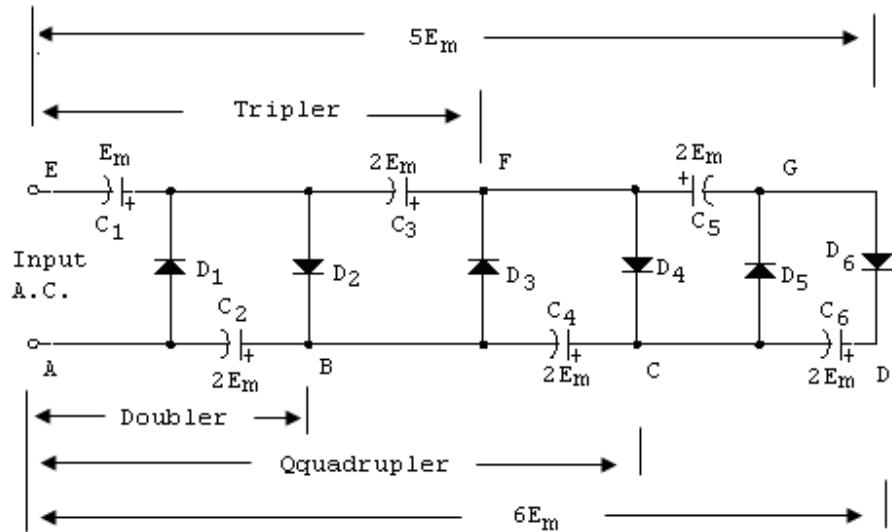


Fig. 5.19

C terminals is equal to  $4Em$  (Quadrupler), and across A & D is  $6Em$ . The voltage across the terminals E & F is  $3Em$  (Tripler), and the voltage across E & G terminals is  $5Em$ .

**Example 5.11** What will be voltage at the output of half wave voltage doubler, if the voltage at the secondary of the transformer is 25 volts? What will be PIV of the diodes used?

Solution:  $E_{r.m.s.} = 25$  volts,

$$\text{Peak value } E_m = \sqrt{2} \times E_{r.m.s.} = 1.414 \times 25 = 35.35 \text{ volts}$$

$$\text{Output voltage of the doubler} = 2.E_m = 2 \times 35.35 = 70.70 \text{ volts}$$

$$\text{PIV of the diodes used} = 2.E_m = 70.70 \text{ volts}$$

**5.6 Clipper Circuits:** The clipping circuits clip off the unwanted portion of the signal without distorting the remaining part of the applied signal. The clipping circuits basically are of two types (i) Series Clipper and (ii) Shunt Clipper. In series clippers the diodes are connected in series with the load resistance and hence the name series clipper. In shunt clippers the diodes are connected in parallel or in shunt with the load resistance. These clippers may further be classified as (i) unbiased and (ii) biased clippers. In unbiased clippers no additional battery is applied to the diodes. However, in case of biased clippers, the diodes are biased with the additional battery of desired magnitude.

The classification of clipper circuits is shown in figure (5.20). Now we shall discuss each of these circuits in detail.

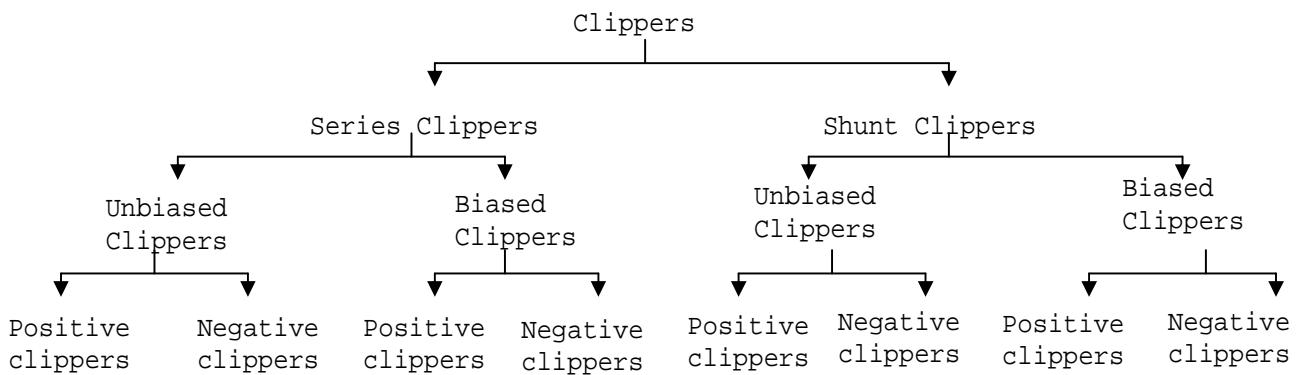


Fig. 5.20

**5.6.1 Unbiased Positive Series Clipper:** This circuit is basically the half wave rectifier as shown in figure (5.21). If the input wave sine, triangular or square wave is applied to the input of the circuit, we get zero output for the positive half cycle of the input wave; and for the negative half cycle output is the same as the input. This is because that the diode goes in reverse bias during positive half cycle of the input wave and during the negative half cycle the diode is forward bias and output follows the input. The input output wave shapes are shown in figure (5.22). From the wave shapes it is clear that this circuit clip off the positive half cycle of the input wave hence the name positive clipper.

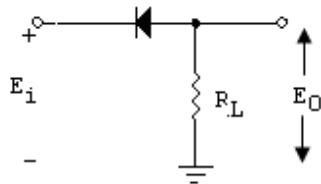


Fig. 5.21

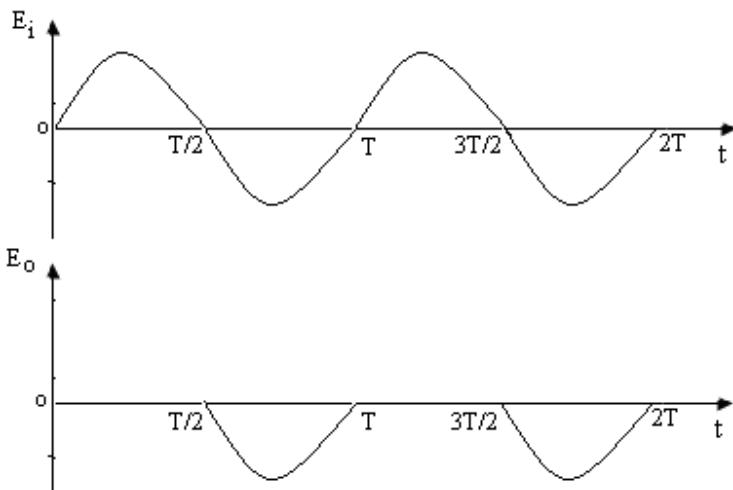


Fig. 5.22

**5.6.2 Unbiased Negative Series Clipper:** If the connections of the diode are reversed as shown in figure (5.23), then the circuit is known as negative unbiased series clipper circuit. It clips off the negative half cycle of the input wave; and the output is the same as the input for negative half cycle. The input output wave shapes are shown in figure (5.24).

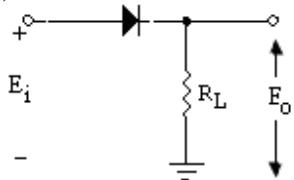


Fig. 5.23

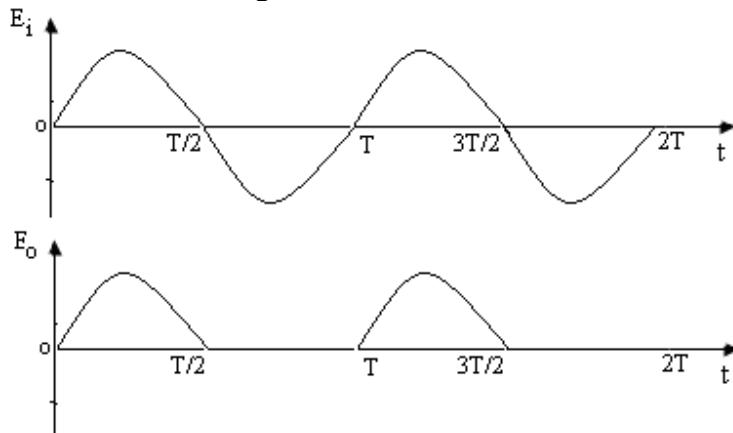


Fig 5.24

**5.6.3 Biased Positive Series Clipper:** The circuit diagram of this clipper is shown in figure (5.25). To explain the working of the circuit let us assume the diode and battery

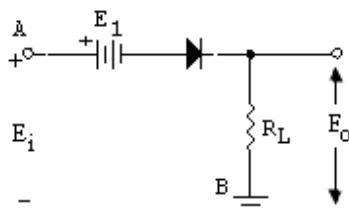


Fig. 5.25

are ideal. During the positive half cycle of the input, the point A is positive with respect to point B and the diode will remain in reverse bias till the cathode of the diode is more negative than  $E_1$ . During the next half cycle of the input wave the diode will remain in reverse bias and the output  $E_o$  is zero. So when the input is positive and beyond  $E_1$ , the output follows the input; and when the input is between zero and  $E_1$  then the output  $E_o$  is zero. It is, therefore, concluded that this circuit has clipped off the portion between zero and  $+E_1$  of the input wave. Hence the name biased positive clipper. The input output wave shapes are given in figure (5.26). It is worth while to mention that the input should be greater than the magnitude of the battery otherwise the clipping will not take place.

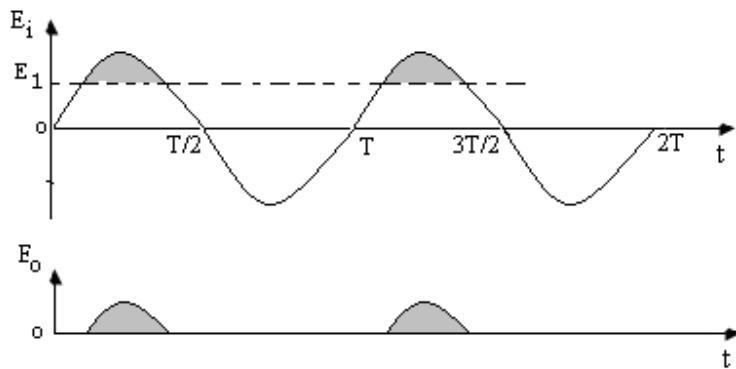


Fig. 5.26

**5.6.4 Biased Negative Series Clipper:** The circuit diagram of this clipper is shown in figure (5.27). To explain the working of the circuit let us assume the diode and

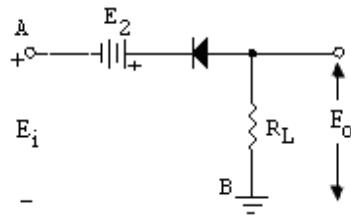


Fig. 5.27

battery are ideal. During the positive half cycle of the input, the point A is positive with respect to point B and the diode will be in reverse bias. During the next half cycle of the input wave the diode will remain in reverse bias till the anode of the diode is more positive than  $E_2$  and the output  $E_o$  will follow the input beyond  $E_2$ . So when the input is positive, the output is zero and when the input is negative and beyond  $-E_2$  then the output follows the input. It is, therefore, concluded that this circuit has clipped off the portion between zero and  $-E_2$  of the input wave. Hence the name biased negative clipper. The input output wave shapes are given in figure (5.28). It is worth while to mention that the input should be greater than the magnitude of the battery otherwise the clipping will not take place.

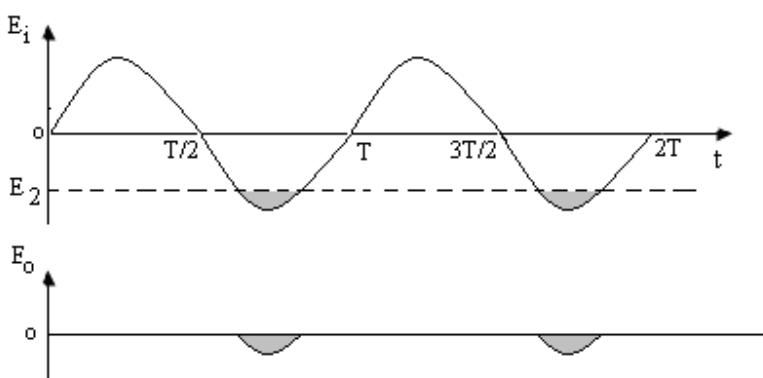


Fig. 5.28

Further if both the circuits of figures (5.25) & (5.27) are combined as shown in figure (5.29), then the clipper will be both sided biased clipper.

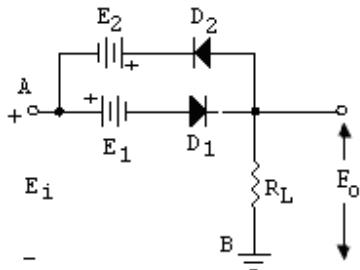


Fig. 5.29

It is very easy to explain the circuit on the similar lines as discussed above. In this circuit the diode  $D_1$  conducts when input is positive and beyond  $E_1$ . The output thus follows the input, clipping off the portion between 0 and  $E_1$ . The diode  $D_2$  will conduct when the input is negative and beyond  $-E_2$ . The output follows the input, clipping off the portion between 0 and  $-E_2$ . The input output wave shapes are shown in figure (5.30).

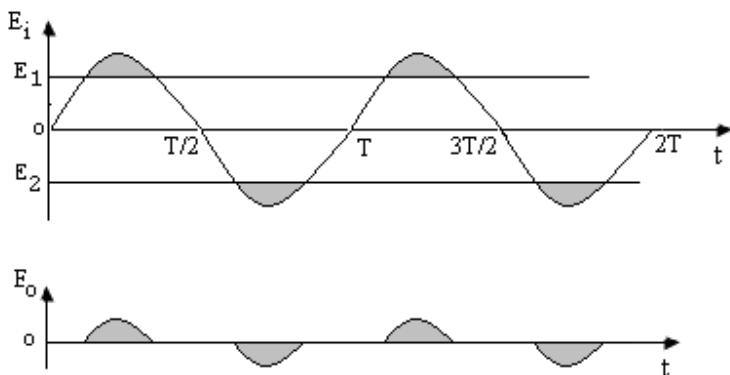


Fig. 5.30

In the clipping circuits discussed above, we have considered the ideal diodes and ideal batteries. Practically it is sometimes important to consider the knee voltage or cut-in voltage  $V_\gamma$  of the diode, its resistance  $r_d$  and also the internal resistance of the battery  $r_b$ . In this situation the  $V_\gamma$  potential will be added with the voltage of the battery that is clipping voltage will be  $E_1 + V_\gamma$  and  $E_2 + V_\gamma$  in double sided series clipper. The transfer characteristics which is the input output relationship, will have less than unity slope at the points  $(E_1 + V_\gamma)$  and  $-(E_2 + V_\gamma)$ . The value of slope is given by  $\frac{R_L}{R_L + r_d + r_b}$ . This will result a distortion in the out put wave forms.

**Example 5.12** Draw the transfer characteristics of the series clipper circuit shown in the figure (5.31a). The values of the circuit parameters are given as:  $E_1 = 1.5$  V,  $E_2 = 2.0$  V,  $R_L = 200 \Omega$ , diode resistance of each diode  $r_d = 20 \Omega$  and internal resistance of each battery  $r_b = 10 \Omega$ . The cut-in voltage of each diode  $V_\gamma = 0.7$  V.

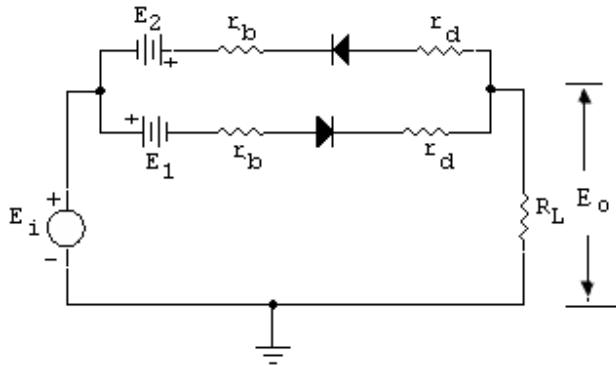


Fig. 5.31a

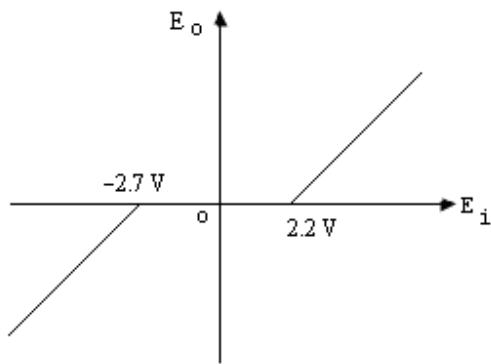


Fig. 5.31b

**Solution:** The break points are  $(E_1 + V_\gamma) = 1.5 + 0.7 = 2.2 \text{ V}$   
 $- (E_2 + V_\gamma) = 2.0 + 0.7 = -2.7 \text{ V}$

The slope at these points is  $\frac{R_L}{R_L + r_d + r_b} = \frac{200}{200 + 20 + 10} = 0.87$

The transfer characteristics are shown in figure (5.31b).

**5.6.5 Unbiased Positive Shunt Clipper:** The circuit diagram for unbiased

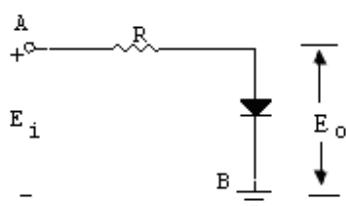


Fig. 5.32

positive shunt clipper is shown in figure (5.32). Its working may very easily be explained as follows. During the positive half cycle of the input wave, the diode is forward biased and will act as an on switch. The output will be zero for the positive half cycle. However,

for the negative half cycle diode is in reverse bias and will act as open switch. The output will therefore, follows the input. So during positive half cycle no output is obtained clipping off this cycle of the input wave. The output is taken in parallel with the diode hence called unbiased positive shunt clipper. The input output wave shapes are shown in figure (5.33).

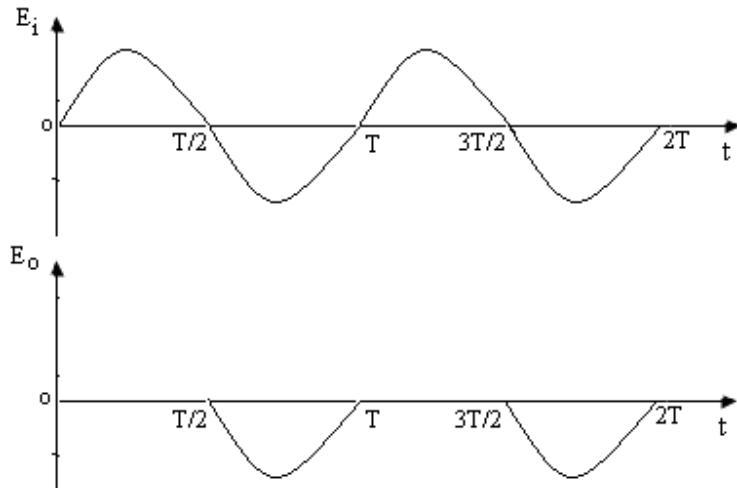


Fig. 5.33

**5.6.6 Unbiased Negative Shunt Clipper:** In this circuit the connections of the diode are reversed as shown in figure (5.34a). This circuit clip off the negative half cycle of the input wave and positive half cycle is obtained without any distortion. The input output wave shapes are shown in figure (5.34 b)

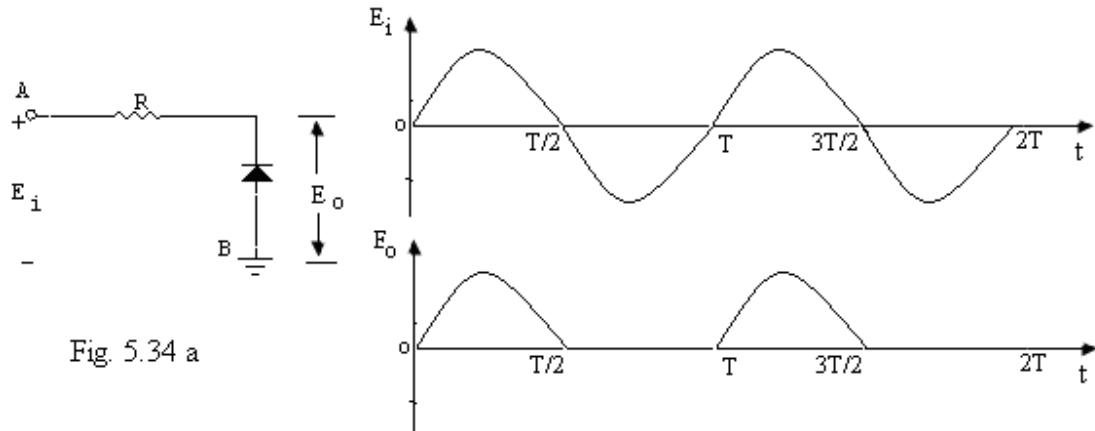


Fig. 5.34 b

**5.6.7 Biased Positive Shunt Clipper:** The circuit diagram of the biased positive

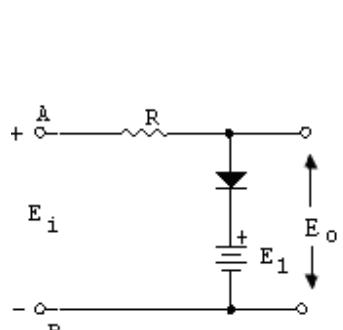


Fig. 5.35 a

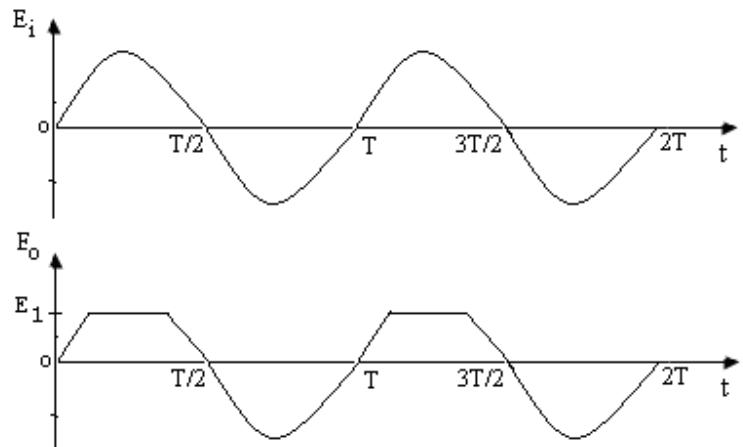


Fig. 5.35 b

clipper is shown in figure (5.35a). It works as follows, during the positive half cycle of the input wave, the diode will be in reverse bias and behaves as an open switch till input is less than or equal to the magnitude of the battery  $E_1$ . In this condition, output follows the input. When the input becomes more positive than  $E_1$ , diode conducts and works as an on switch. The output will equal to  $E_1$ . During the next half cycle the diode will be in reverse bias and output will follow the input. So it is concluded that the portion of the input beyond  $E_1$ , in positive half cycle is clipped off. The input output wave shapes is shown in figure (5.35 b).

**5.6.8 Biased Negative Shunt Clipper:** The circuit diagram of the biased negative clipper is shown in figure (5.36 a). In this circuit the connections of the diode and

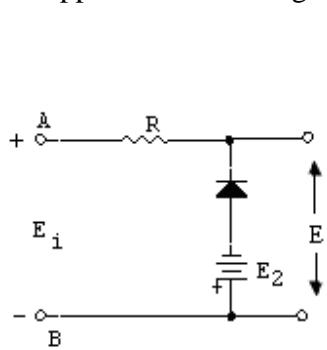


Fig. 5.36 a

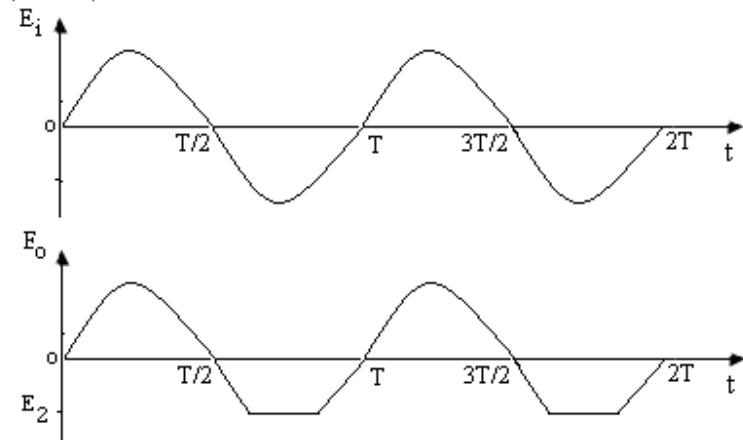


Fig. 5.36 b

battery are reversed. It works as follows, during the positive half cycle of the input wave, the diode will be in reverse bias and behaves as an open switch and the output follows the input. During the next half cycle of the input wave the diode will be in reverse bias till the input is less negative than  $E_2$ . When the input becomes more negative than  $E_2$ , diode conducts and works as an on switch. The output will equal to  $E_2$ . So it is concluded that the portion of the input beyond  $E_2$ , in negative half cycle is clipped off. The input output wave shapes is shown in figure (5.36 b).

Further both the circuits of figures (5.35 a) & (5.36 a) may be combined to get both sided

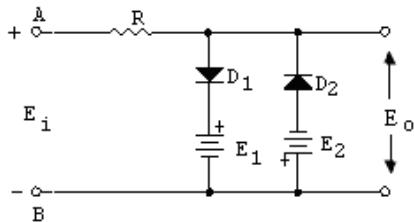


Fig. 5.37 a

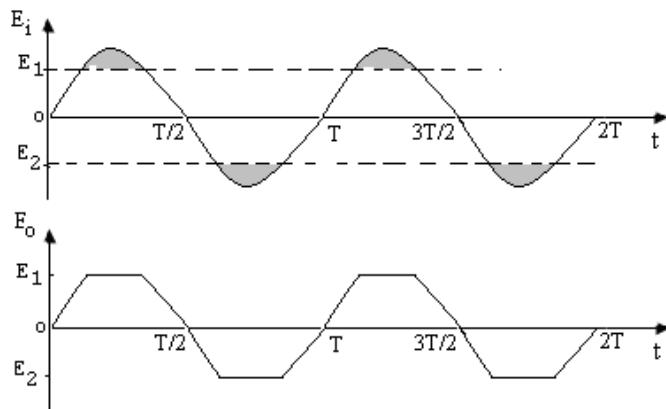


Fig. 5.37 b

biased shunt clipper as shown in figure (5.37 a). It may be explained that the portion beyond  $E_1$  in the positive half cycle of the input, is clipped off and in the negative half cycle the portion beyond  $E_2$  is clipped off. The input output wave shapes are shown in figure (5.37 b).

**Example 5.13:** The diodes connected in the circuit of figure (5.37 a) are not ideal but have some finite forward resistance  $r_d$ . Draw its transfer characteristics and the input output wave forms.

**Solution:** When the input signal is lying between  $E_1$  and  $E_2$ , both the diodes will be in reverse bias and the slope will be unity at the origin. When the input is beyond  $E_1$  or  $E_2$ , the slope at these points  $E_1$  and  $E_2$  will not be zero but will have the slope equal to

$\frac{r_d}{R + r_d}$  which is small positive. So the output will be slightly distorted at the points  $E_1$  &  $E_2$ . The transfer characteristics and its input output wave shapes are given in figure (5.38)

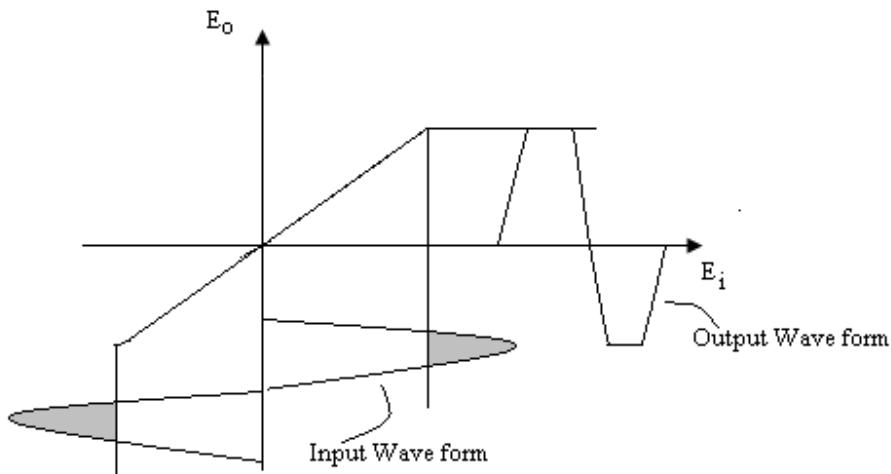


Fig. 5.38

**5.7 Clamping Circuits:** The clamping circuit is used to clamp a signal to a desired d.c. level. The sinusoidal, square or triangular signal normally swings symmetrically about the X- axis with equal magnitude on both sides as shown in figure (5.39). The signal in this condition is said to have the zero average value or its d.c. level is zero. If the signal is lifted upward to touch the negative peak points of the signal to X- axis, the signal is said to have positively clamped at zero d.c. level. If on the contrary the signal is lifted downward to touch the positive peak points of the signal to X- axis, the signal is said to have negatively clamped at zero d.c. level (ref fig. 5.39). The signal may further be lifted upward or down ward to a desired positive or negative voltage ( $E$ ) as shown in figure (5.39). In this condition the signal is said to have clamped at positive  $E$  volts or negative  $E$  volts.

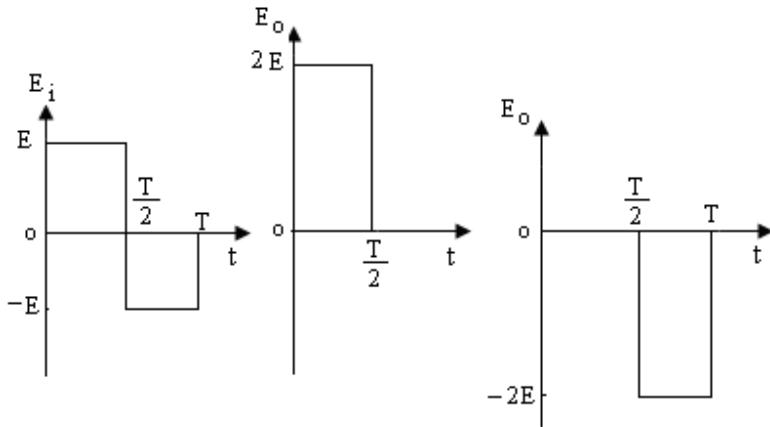


Fig. 5.39

The clamping circuit shown in figure (5.40a) consists of a diode, a capacitance and a resistance. To the input of this circuit we apply a signal whose d.c. level is zero i.e. which swings both sides of X – axis symmetrically. During the first negative half cycle of the input wave  $E_i$ , diode conducts and it behaves as a closed switch. The capacitor C

charges to the peak value of the negative swing ( $E_N$ ) with the polarity shown in figure (5.40a). The values of the capacitor C and resistance R are so chosen so that the RC time constant is large enough so that the capacitor is not immediately discharged. Now during the next positive half cycle of the input wave, diode is in reverse bias and behaves as an open switch. The voltage at the output will be equal to the magnitude ( $E_N + E_P$ ). The cycle repeats and we get the output as shown in figure (5.40b). It is clear from this figure that the output wave touches the negative peak of the signal to the X-axis hence it is positively clamped at zero d.c. level.

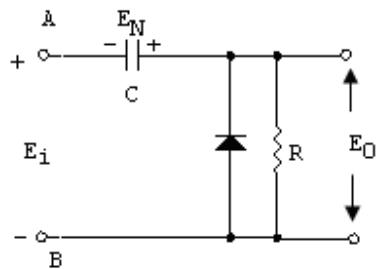


Fig. 5.40 a

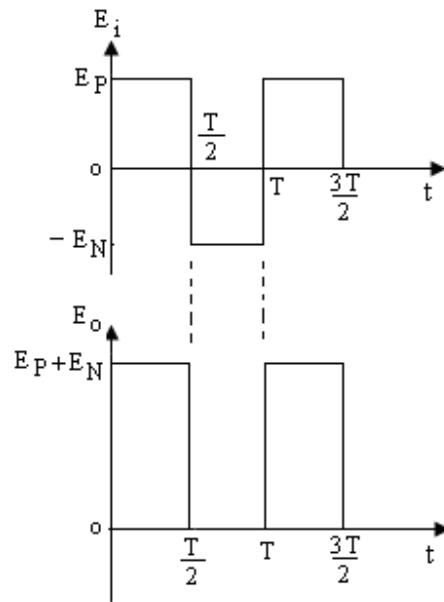


Fig. 5.40 b

If the diode connections are reversed as shown in figure (5.41a), the circuit may easily be explained that the signal is negatively clamped at zero d.c. level (ref. 5.41 b).

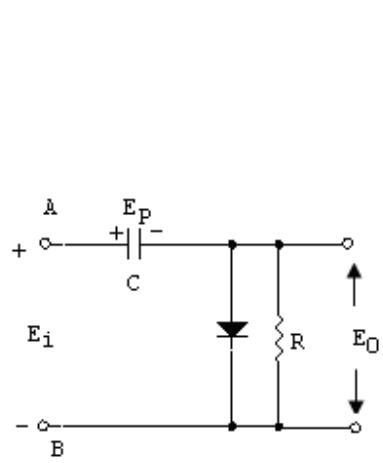


Fig. 5.41 a

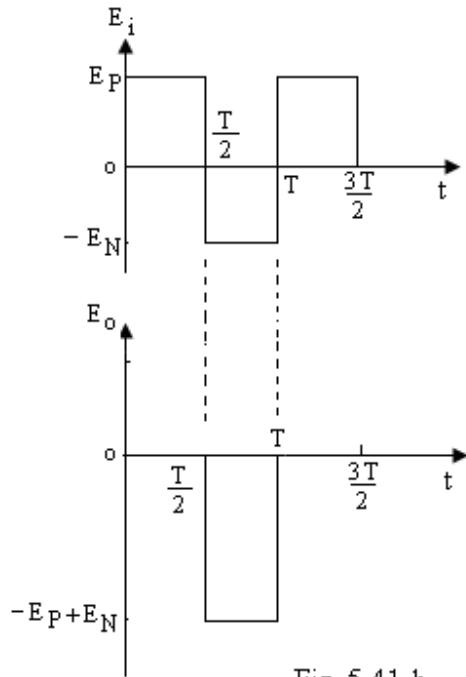


Fig. 5.41 b

Now to clamp the signal at some positive  $E$  volt, then a battery of  $E$  volt may be introduced in series with the diode as shown in figure (5.42 a). Input output signals are shown in figure (5.42 b).

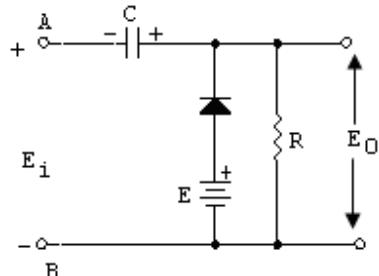


Fig. 5.42 a

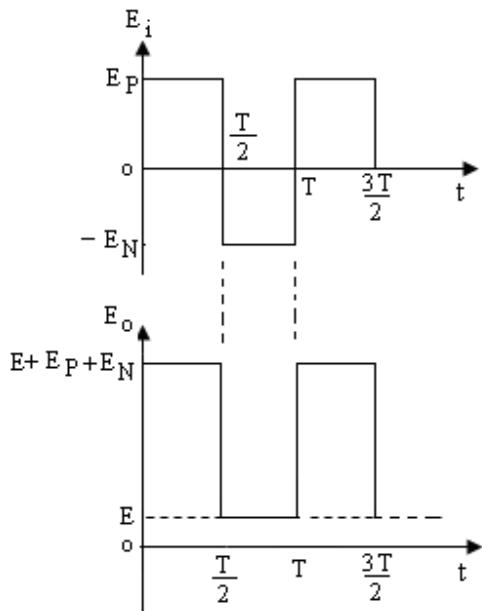


Fig. 5.42 b

Similarly, to clamp the signal at some negative  $E$  volt, then a battery of  $E$  volt may be introduced in series with the diode as shown in figure (5.43 a). Input output signals are shown in figure (5.43 b).

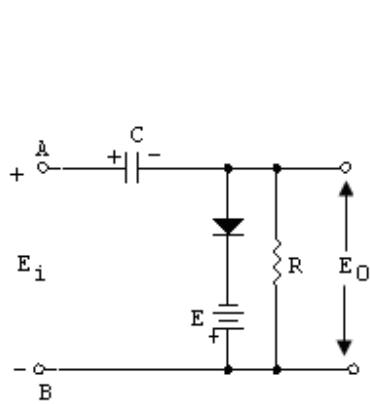


Fig. 5.43 a

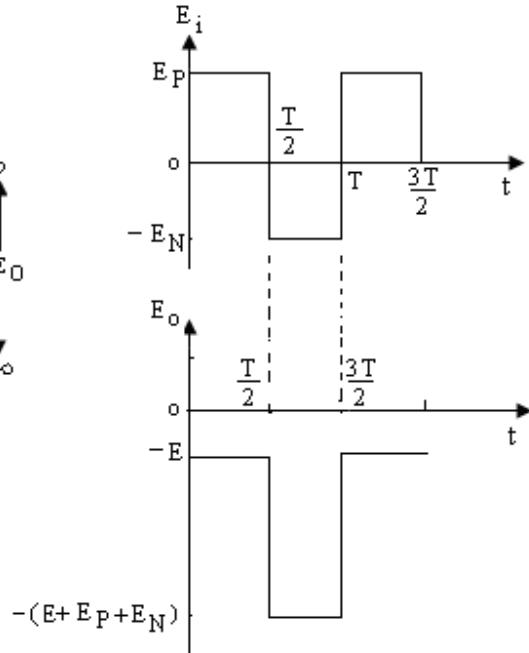


Fig. 5.43 b

**5.8 Log and anti log circuit:** The signal processing operations such as logarithm and antilogarithm can be performed using the p – n junction diode characteristics. As it is well known that the current flowing through the diode is given by

$$I = I_s (e^{V/V_T} - 1) \quad \text{----- (5.18)}$$

where  $V_T$  is the thermal voltage and  $I_s$  is the reverse saturation current which are constants at the particular temperature and semiconductor material. If  $V \gg V_T$ , this equation will of the form

$$I = I_s e^{V/V_T} \quad \text{----- (5.19)}$$

i.e. if a voltage  $V$  is applied across a diode as shown in figure (5.44a), the current flowing through the diode will be proportional to the antilog function

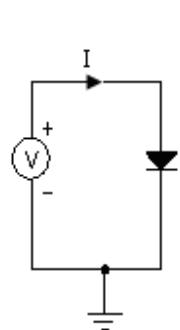


Fig. 5.44 a

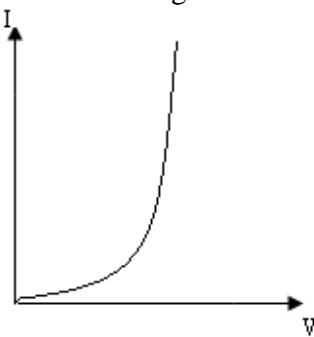


Fig. 5.44 b

of this voltage  $V$ . This circuit may be called as the antilog circuit. Figure (5.43b) shows the antilog function of the input voltage  $V$ .

Taking the log on both sides of equation (5.19), we get:

$$\ln\left(\frac{I}{I_s}\right) = \frac{V}{V_T} \quad \text{or} \quad V = V_T \ln\left(\frac{I}{I_s}\right) \quad \text{----- (5.20)}$$

from this equation it is clear that if a known current  $I$  from a current source

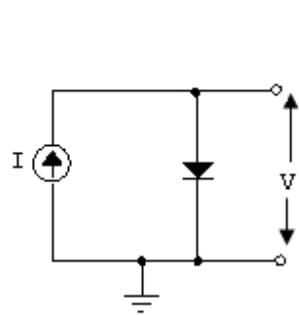


Fig. 5.45a

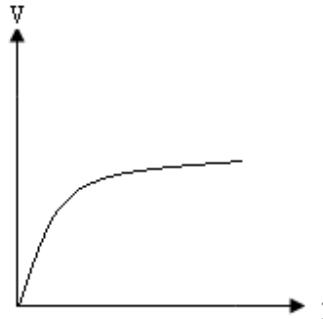


Fig. 5.45 b

is passed through the diode (fig. 5.45 a), then the voltage across the diode will be proportional to the logarithm of current  $I$ . hence this circuit may be called as log circuit. The logarithm function is shown in figure (5.45 b).

**5.9 Zener Diode as Voltage Regulator:** The heavily doped P N junction diodes which work in reverse bias and operate in the break down region, known as Zener diodes have already been discussed in the preceding chapter. Here we shall discuss its most common application as a voltage regulator which provides a constant voltage from a source whose voltage may vary over a sufficient range. A simple voltage regulator circuit using Zener diode is shown in figure (5.46).

In this circuit a series combination of Zener diode and a resistance  $R_s$ , is connected across the unregulated supply  $E_i$ . The regulated output voltage  $E_o$  is available across the parallel combination of Zener diode and the load resistance  $R_L$ . The polarity of the Zener diode is such that it is biased in reverse bias. The Zener diodes of different break down voltages

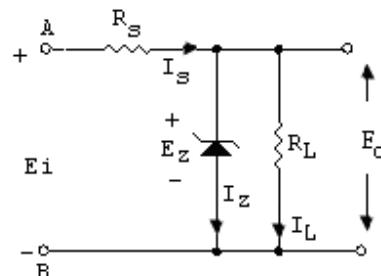


Fig. 5.46

are available in the market, so the diode of required break down voltage  $E_z$  is chosen in the circuit. If the circuit elements are such that the voltage across the Zener diode is less than the Zener break down voltage  $E_z$ , the diode will behave like an off switch.

The output voltage  $E_0$  will be given by  $E_0 = \frac{E_i R_L}{R_s + R_L}$ . The Zener diodes are never used in this state.

If the voltage across the Zener diode is more than or equal to the Zener break down voltage  $E_z$ , the diode is in on state and acts as voltage source of voltage  $E_z$ . The output voltage  $E_0$  will be equal to  $E_z$ . This is the required state for the voltage regulation.

The current drawn  $I_s$  from the unregulated supply is given by  $I_s = I_z + I_L$

$$\text{or } I_z = I_s - I_L \quad \text{where } I_L = \frac{E_i}{R_L} \quad \text{and } I_s = \frac{E_i - E_0}{R_s}$$

The power dissipation of the Zener diode is given by:  $P_z = E_z I_z$ .

As discussed above the Zener diode is used in the breakdown region. The output voltage will be equal to the Zener voltage. This circuit is commonly used as voltage regulator or as a fixed reference source. The regulator circuit gives the constant voltage irrespective of the change in the load resistance  $R_L$  or the change in the unregulated supply  $E_i$ . We shall now find the minimum value of load resistance  $R_L$  and the minimum value of the  $E_i$ . If the load resistance  $R_L$  or unregulated supply is too small the diode will not be in the breakdown region or the Zener will be off.

$$\text{We know } E_0 = E_z = \frac{E_i R_L}{(R_s + R_L)}$$

$$\text{or } (R_s + R_L) E_z = E_i R_L$$

$$\text{or } R_L (E_i - E_z) = R_s E_z$$

$$\text{or } R_{L\min} = \frac{R_s E_z}{(E_i - E_z)},$$

so any load resistance greater than this value will ensure the Zener diode is in the breakdown region or on state.

$$\text{The maximum value of } R_L \text{ may also be calculated. } I_{L\max} = \frac{E_0}{R_L} = \frac{E_z}{R_{L\max}}$$

$$\text{or } I_{L\max} = \frac{E_i - E_z}{R_s} = \frac{E_s}{R_s} = I_s$$

The Zener current is minimum, as  $I_s = I_z + I_L$ .

$$I_{L\min} \text{ may also be given by: } I_{L\min} = I_s - I_{z\max}$$

$$\text{so } R_{L\max} = \frac{E_z}{I_{L\max}}$$

The minimum value of the unregulated supply is to be calculated as follows:

$$\text{We know } E_0 = E_z = \frac{E_i R_L}{(R_s + R_L)}$$

$$\text{and } E_{i\min} = \frac{(R_L + R_s) x E_z}{R_L}$$

The maximum value of  $E_i$  is limited by the maximum Zener current  $I_{z\max}$ . Since

$$I_{z\max} = I_s - I_L.$$

$$\text{Now } E_i = I_s R_s + E_0$$

As  $E_0 = E_z$  is constant, the input voltage will be maximum when  $I_s$  is maximum, so  
 $E_{i\max} = I_{s\max} R_s + E_z$

It is worth while to mention the following points regarding the Zener regulator circuits.

- More than one Zener diodes may be connected in series, and the output voltage will be sum of all the break down voltages of the Zener diodes. Let three Zener diodes  $Z_1, Z_2, Z_3$  are connected in series as shown in figure (5.47), whose values are  $E_{z1} = 6$  volts,  $E_{z2} = 12$  volts,  $E_{z3} = 15$

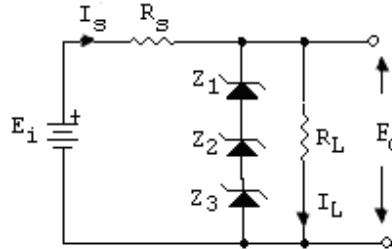


Fig. 5.47

volt. The output voltage will be 33 volts, provided the circuit parameters are properly chosen, so that the voltage across the load resistance is more than 33 volts, when diodes are assumed in off state.

- The Zener diodes are never connected in parallel, as in the break down region the Zener diodes behave like ideal voltage source.
- The Zener diodes may be connected in series back to back as shown in figure (5.48a). This circuit will behave like the shunt clipper circuit. Input

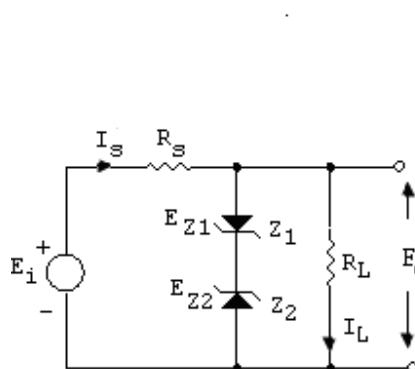


Fig. 5.48 a

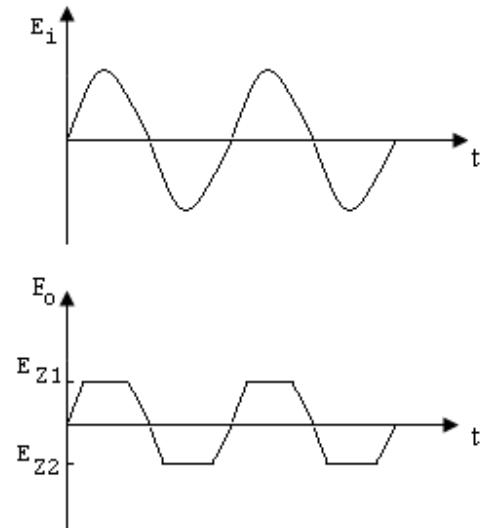


Fig. 5.48 b

signal connected to this circuit is a varying signal whose peak value should be greater than break down voltage of each diode. During the positive half cycle of the input signal the diode  $Z_1$  will be in forward and will work like an ordinary diode. The Zener diode  $Z_2$  will be in reverse bias till the input is less than its break down voltage, in this condition the

output follows the input. But when the input is greater than the break down voltage of  $Z_2$ , a constant voltage equal to  $E_{z2}$  will be maintained across the output. Thus it clips off the portion of the input signal beyond  $E_{z2}$ . Similarly it can be shown that this circuit clips off the portion of the negative half cycle beyond  $E_{z1}$ , as the process is reverse in this case. The input output wave shapes are shown in figure (5.48 b).

**Example 5.14** The Zener diode regulator circuit shown in figure (5.49) has the following parameters.  $E_i = 20$  volts,  $R_s = 1K\Omega$ ,  $E_z = 8.2$  volts and  $R_L = 2K\Omega$ . Find  $E_0$ ,  $E_s$ ,  $I_z$ . If the maximum wattage of the Zener diode is 35 mW, then suggest whether this diode will work or not.

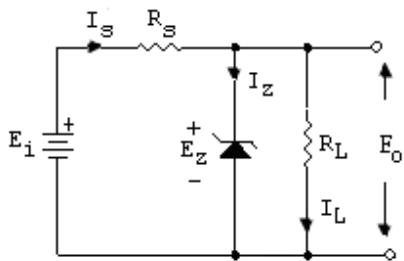


Fig. 5.49

Solution: If the Zener diode is in the off state, the voltage across the load resistance  $R_L$  is given by:

$$E = \frac{20V \times 2K\Omega}{(1+2)K\Omega} = 13.33V$$

This voltage is greater than the break down voltage of the Zener diode, the diode will go in the on state and out put voltage will be equal to the  $E_z$ .

So  $E_0 = E_z = 8.2$  Volts

and voltage across  $R_s$  is  $E_s = 20 - 8.2 = 11.8$  volts

The current following through the resistance  $R_s$  is  $I_s = \frac{11.8V}{1K\Omega} = 11.8mA$

The current following through the resistance  $R_L$  is  $I_L = \frac{8.2V}{2K\Omega} = 4.1mA$

The current following through the Zener diode is

$$I_z = I_s - I_L = 11.8 - 4.1 = 7.7mA$$

Power of the Zener diode  $P_z = E_z \times I_z = 7.7 mA \times 8.2 \text{ volts} = 63.14 \text{ mW}$

This is the required power of the Zener diode. So we have to use the Zener diode whose maximum power is greater than 63.14 mW. But in the given problem, the required power of the Zener diode is less than the given power 35 mW. So the Zener diode of 35 mW power will not work. The Zener diode of higher than 63.14 mW should be used.

**Example 5.15** The Zener diode regulator circuit shown in figure (5.50) has the following parameters.  $E_i = 35$  volts,  $R_s = 1.2 K\Omega$ ,  $E_z = 12$  volts and maximum Zener current is 10mA. Find the range of  $R_L$  so that  $E_0$  remains to be constant to 12 volts.

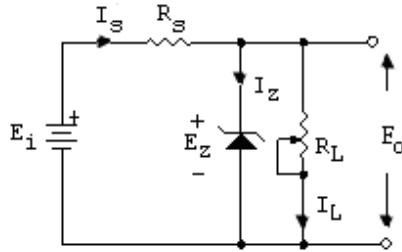


Fig. 5.50

Solution: The minimum value of \$R\_L\$ is given by:

$$R_{L\min} = \frac{R_s E_z}{(E_i - E_z)} = \frac{1200 \times 12}{35 - 12} = 626\Omega$$

The current flowing through the resistance \$R\_s\$ is then given by:

$$I_s = \frac{E_i - E_z}{R_s} = \frac{(35 - 12) \text{volts}}{1.2K\Omega} = 19.2mA$$

The minimum value of \$I\_L\$ is

$$I_{L\min} = I_s - I_{z\max} = 19.2 - 10 = 9.2mA$$

The maximum value of \$R\_L\$ is

$$R_{L\max} = \frac{E_z}{I_{L\min}} = \frac{12 \text{volts}}{9.2mA} = 1.3K\Omega$$

### Problems:

1. Draw a circuit diagram of a full wave rectifier along with a series inductor (choke) filter and obtain a formula for the ripple factor.
2. Give the circuit diagram and describe the working of a full wave rectifier with shunt capacitor filter. Why for very low ripple the output current should be very small?
3. Explain, giving the circuit diagram, the working of a full wave rectifier. Obtain the expressions for average, r.m.s. value of the output voltage, efficiency and ripple factor.
4. Drive the expressions for (a) average and (b) r.m.s. value of the output voltage of a half wave rectifier. Find the expression of rectifier efficiency and ripple factor for half wave rectifier.
5. Describe the circuit diagram and explain the working of half wave rectifier. Explain the ripple voltage and ripple factor for the same.
6. Give the circuit diagram of a full wave rectifier with an L-Section filter and explain its working. Find the expression for the ripple factor.
7. Give the circuit diagram of a full wave rectifier with \$\pi\$- section filter and explain its working. Find the expression for the ripple factor.
8. What do you mean by the peak inverse voltage of the diode? Show that when a capacitor is connected across the load resistance of a half wave rectifier circuit, and then the peak inverse voltage of the diode is approximately twice the peak voltage of the input signal.

9. Discuss the bridge rectifier circuit with neat circuit diagram. What are its merits and demerits? Show that the PIV of the diodes used in bridge rectifier is equal to the peak value of the input signal.
10. Discuss the circuit of the full wave rectifier and explain its working. Mention its advantages and disadvantages. Show that PIV of the diodes used in this circuit is equal to twice the peak value of the input signal.
11. Making the suitable approximations, determine the d.c. output voltage as well as ripple factor of the half wave rectifier with shunt capacitor filter.
12. Making the suitable approximations, determine the d.c. output voltage as well as ripple factor of the full wave rectifier with shunt capacitor filter. Show that its value is approximately half the value calculated for half wave rectifier.
13. What do you mean by clipping circuits? Mention various types of clipping circuits. Discuss double sided biased series clipper.
14. Discuss various types of shunt clipper with the help of suitable circuit diagrams.
15. Discuss half wave voltage doubler with a suitable diagram. Show that the PIV of the diodes used in this circuit is twice the peak value of the input signal.
16. Discuss the voltage multiplier circuit.
17. Discuss full wave voltage doubler with suitable circuit diagram. What are its advantages?
18. What do you understand by Clamper? Discuss a clamper circuit with suitable circuit diagram.
19. What is Zener diode? Explain how the Zener diode is used as a voltage regulator.
20. Prove that r.m.s. value of the triangular ripple wave is  $\frac{E_R}{2\sqrt{3}}$ , where  $E_R$  is the peak value of the ripple.

21. A 200 volts a.c. signal of frequency 50 Hz is applied to the half wave rectifier circuit having load resistance  $500 \Omega$ . If the diode used in the circuit is ideal then find d.c. output voltage across the load resistance, d.c. and r.m.s. current flowing through the load resistance.

Ans. 90 Volts, 180 mA, 141.4 mA

22. Repeat the problem 21, assuming the diode has the forward resistance of  $20 \Omega$ .

Ans. 86.6 volts, 173.2 mA, 141.4 mA

23. A full wave rectifier is to supply 30 volts d.c. across the load resistance of  $1K\Omega$ . Find (a) r.m.s. value voltage of the transformer, (b) peak diode current and (c) power rating of the transformer.

Ans. 33 – 0 – 33 volts transformer, 33mA, 1.1 watt

24. A 20 – 0 – 20 volts transformer is used for full wave rectifier circuit. Each diode has a forward resistance of  $20\Omega$ . The load resistance is  $2K\Omega$ . Find  $E_{d.c.}$ ,  $I_{d.c.}$ ,  $I_{r.m.s.}$ , and rectifier efficiency  $\eta$ .

Ans. 17.8 volts, 8.9mA, 9.9 mA, 80.4%

25. A center tap transformer having 20 volts r.m.s. on each side of the center terminal is used in full wave rectifier with shunt capacitor filter. If frequency of the input a.c. is 50Hz, the load resistance is  $300 \Omega$  and capacity of the shunt capacitor is  $470\mu F$ , find the d.c. load voltage and the ripple factor.

Ans. 27.3 volts, 2.1%

26. A full wave rectifier with shunt capacitor filter has the following parameters.  $E_{d.c.} = 50$  volts,  $I_{d.c.} = 277\text{mA}$ ,  $I_{r.m.s.} = 289 \text{ mA}$  and  $f = 50\text{Hz}$ . Find the value of ripple factor and the capacity of the capacitor.

Ans. 27.6%,  $58\mu\text{F}$

27. A full wave rectifier with shunt capacitor filter is to supply a  $200\Omega$  load with 150 mA current. What should be voltage rating of the transformer at 50 Hz frequency, to have a ripple factor of 0.04?

Ans.  $23 - 0 - 23 \text{ V}$

28. A full wave rectifier circuit is connected to a  $\pi$ - section filter, having two  $100\mu\text{F}$  capacitors and a  $5 \text{ H}$  inductor. Find the value of ripple content if the frequency of the a.c. mains is 50 Hz and load connected at the output is  $150\Omega$ .

Ans. 0.098%

29. Find the maximum and minimum values of Zener current in a Zener regulator circuit. Given  $R_s = 3.5\text{K}\Omega$ ,  $R_L = 5\text{K}\Omega$ ,  $E_z = 15 \text{ Volts}$  and the input varies from 35 volts to 55 volts.

Ans. 8.43mA, 2.7mA

30. If in Zener diode regulator circuit,  $R_s = 1\text{K}\Omega$ ,  $E_z = 12 \text{ Volts}$ ,  $R_L=3\text{K}\Omega$  and  $E_i = 30$  volts, find the output voltage, the voltage across the series resistance  $R_s$  and also the Zener current.

Ans. 12 volts, 18 volts, 14mA

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# 6

## Junction Transistors

W. Schockley, J. Bardeen and W. H. Brattain of Bell Telephone Laboratories, U.S.A. in 1948 invented an important semiconductor device named as transistor which is now most commonly being used in electronic instruments. The junction transistor is also called Bipolar Junction Transistor (BJT) because the current flows in it due to both types of charge carriers electrons and holes. Transistors have the advantages that its size is very small, works on low applied voltage and capable of producing large amplifications. Physical behaviour of transistors including V – I characteristics will be studied in this chapter.

**6.1 The Transistor:** Junction transistors are made up of two PN junctions of Si or Ge, forming PNP or NPN transistors. The PNP transistor is formed by sandwiching a thin N – layer between two P – layers. Similarly an NPN transistor is formed by sandwiching a thin P – layer between two N – layers. These two types of transistors with their symbols are shown in figure (6.1). The three regions of the transistor are known as emitter, base and collector. The emitter is heavily doped, base region is thin and very lightly or sparingly doped and the collector is moderately doped. Three currents flow in the transistor namely emitter current  $I_E$ , base current  $I_B$  and collector current  $I_C$ . Conventionally, it is assumed that all the three currents are entering the junctions irrespective of the types of the transistor. That is whether the transistor is PNP or NPN, the current entering the junction is positive and leaving the junction is negative. If the actual current in either type of transistors is entering the junction, the current is taken as positive otherwise negative.

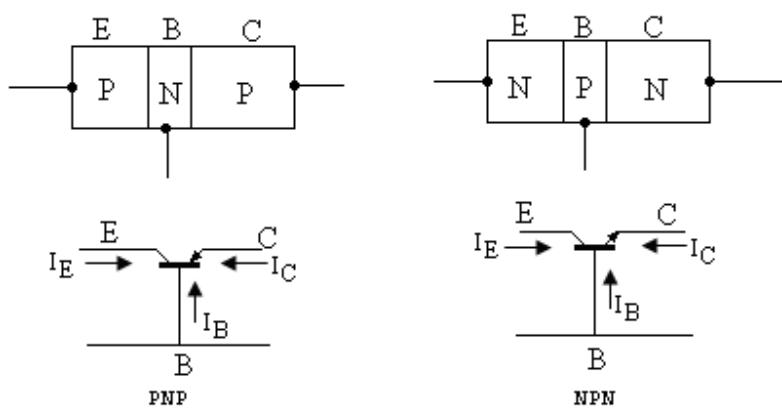


Fig. 6.1

From the figure (6.1)  $I_E + I_B + I_C = 0$

The symbol  $V_{EB}$  represents the potential across the emitter base junction,  $V_{CB}$  the potential across collector base junction and  $V_{CE}$  the potential across collector and emitter junction. Normally the transistor is biased in the active region, in which emitter base junction is kept in forward bias and collector base junction in the reverse bias. Input circuit has low resistance as the emitter base junction is forward biased and output circuit has high resistance as collector base junction is biased in the reverse bias. The transistor therefore, transfers the resistor from input circuit to output circuit, hence the name Transistor (**Transfer + Resistor = Transistor**). The working of both the two types of transistors is the same with the difference that the role of electrons and holes are reversed in these transistors.

**6.1.1 Minority Carrier Concentration in a Transistor:** Let us consider a PNP transistor which is open circuited so that all the transistor currents are zero. Further it is assumed that the transistor is having perfectly symmetrical junctions. The symmetrical junctions we mean that the emitter and collector junctions are having identical physical dimensions and doping concentrations. The barrier height at the emitter junction  $J_E$  and collector junction  $J_C$  will be equal as shown in figure 6.2 (a). The narrow space charge regions at the junctions are neglected.

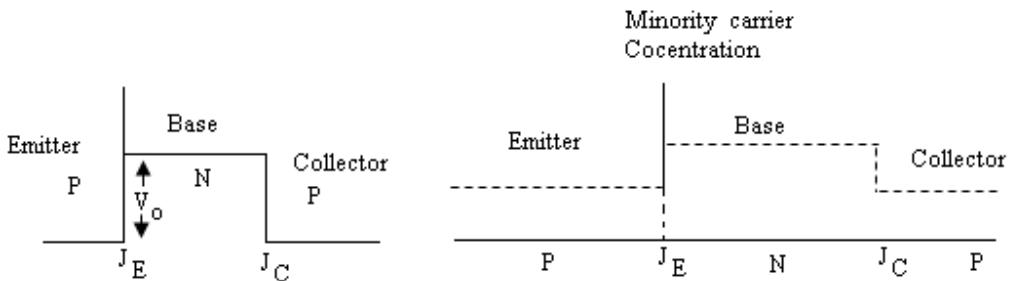


Fig. 6.2 a

Fig. 6.2 b

The majority charge carrier concentration in each region will be equal to the corresponding doping level.

i.e.,  $p = N_A$  in p – type semiconductor,  
and  $n = N_D$  in n – type semiconductor.

The minority carrier concentration can be calculated from the law of mass action  
 $np = n_i^2$

Thus the number of electrons (minority carriers) in p type semiconductor or

$$\text{emitter is given by: } n_p = \frac{n_i^2}{N_A} = n_{po},$$

the suffix  $p$  represents the p type semiconductor and  $n_{po}$  represents the minority carrier electron in p type emitter in thermal equilibrium.  $N_A$  is the acceptor concentration in p type emitter.

Similarly the number of holes (minority carriers) in n type semiconductor or base is given by:  $p_n = \frac{n_i^2}{N_D} = p_{no}$ ,

$p_{no}$  represents the minority carrier holes in n type base in thermal equilibrium.  $N_D$  is the donor concentration in the n type base.

Generally in a transistor base is lightly doped  $N_A >> N_D$ , this implies  $p_{no} \gg n_{po}$

The no. of minority charge carriers (electrons) in p – type collector can also be given as:  $n_{po} = \frac{n_i^2}{N_A}$  where  $N_A$  is the acceptor concentration in the p type collector. The minority carrier concentrations in the three regions in thermal equilibrium state are therefore, depicted in figure 6.2(b). These concentrations will vary with the application of biasing voltages to the transistor junctions.

**6.2 The Transistor in active region:** Internal physical behaviour of the transistor will be discussed by considering the transistor (PNP) in the active region i.e. emitter base junction is biased in forward bias and collector base junction is biased in reverse bias, which is shown in figure 6.3(a). The variation of potential barrier with biasing of the transistor is shown in figure 6.3(b). The dotted lines show this variation in open circuit condition of the transistor; the solid lines, however, show this variation after the application of biasing voltages. The space charge regions at the emitter junction  $J_E$  and at the collector junction  $J_C$  are not shown, as it is assumed to be negligibly small. The forward biasing of the emitter junction lowers barrier potential  $V_0$  by an amount equal to the magnitude of the applied emitter base voltage  $|V_{EB}|$ , where as the reverse biasing of the collector junction increases the barrier potential by the amount equal to the magnitude of the applied collector base voltage  $|V_{CB}|$  as depicted in figure 6.3(b). The lowering of the emitter base potential barrier permits the injection of minority carrier holes of the emitter region to the base region; and the minority carrier electrons of the base region are injected in to the emitter region.

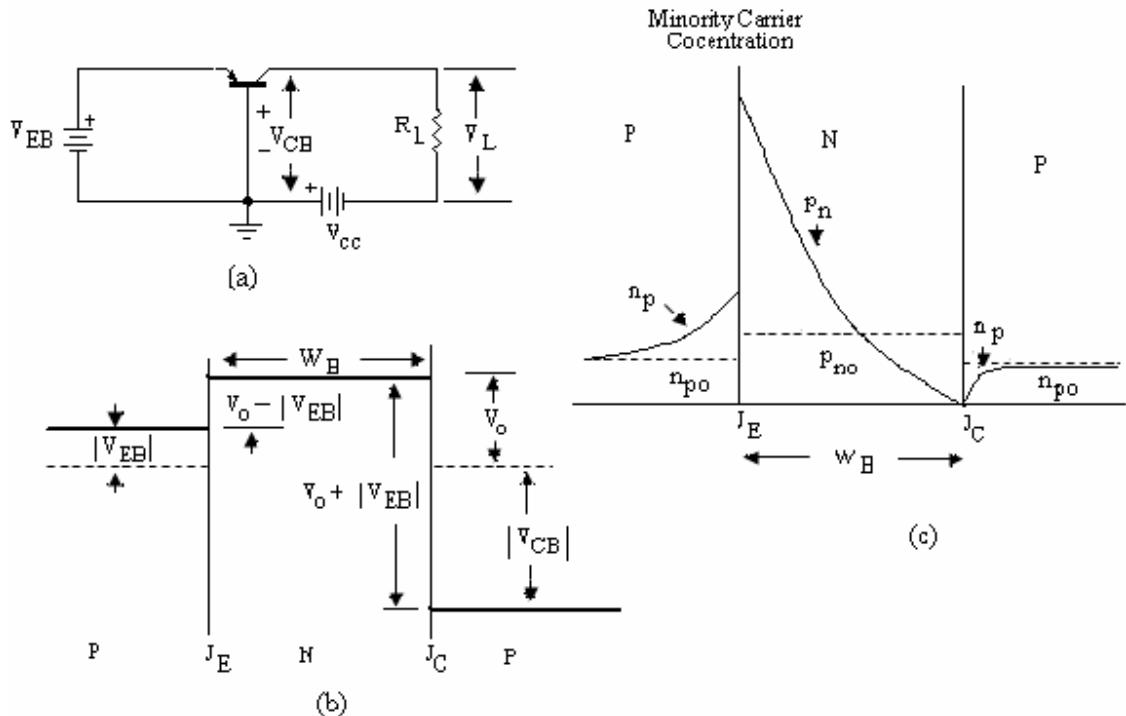


Fig. 6.3

The minority carrier electrons in the emitter ( $n_p$ ) rises exponentially from thermal equilibrium concentration  $n_{p0}$  to  $n_p(0)$  at the emitter junction  $J_E$  (where  $x = 0$ ), given by:

$$p_n(0) = p_{n0} e^{\frac{V_{EB}}{V_T}} \quad \dots \quad (6.1)$$

The minority carrier holes in the base ( $n_p$ ) also rises exponentially from thermal equilibrium concentration  $p_{n0}$  to  $p_n(0)$  at the emitter junction  $J_E$  (where  $x = 0$ ), given by:

$$n_p(0) = n_{p0} e^{\frac{V_{EB}}{V_T}} \quad \dots \quad (6.2)$$

as  $p_{n0} \gg n_{p0}$ , so  $p_n(0) \gg n_p(0)$ .

Similarly minority carrier holes in the base  $p_n$  and electrons in the collector  $n_p$ , near the collector junction  $J_C$  (where  $x = W$ ) are given by:

$$p_n(w) = p_{n0} e^{\frac{V_{CB}}{V_T}} \quad \dots \quad (6.3)$$

$$\text{and} \quad n_p(w) = n_{p0} e^{\frac{V_{CB}}{V_T}} \quad \dots \quad (6.4)$$

As  $V_{CB}$  is negative and  $|V_{CB}| \gg V_T$  so  $p_n(w) = n_p(w) = 0$ . These variations of the minority carriers are depicted by solid lines in figure 6.3(c).

The excess holes in the base diffuse from emitter base junction  $J_E$  to collector base junction  $J_C$  across the base where the electric field intensity  $E$  is zero. The collector base

junction is reverse biased so the electric field intensity  $E$  at the junction  $J_C$  will be positive and large as ( $E = -dV/dx$ ). Due to which the holes are accelerated across the junction. In other words, the holes which reach the junction  $J_C$  fall down the potential barrier, and are therefore collected by the collector.

**6.3 Current Components in a Transistor:** We shall find components of currents in a transistor, which is biased in the active region i.e. the emitter base junction is biased in the forward bias and collector base junction is biased in the reverse bias. Due to the forward biasing of the emitter base junction, majority carrier holes are injected into base region and majority carrier electrons of the base region move into the emitter region. This means emitter current  $I_E$  consists of two types of current (i) hole current  $I_{pE}$  constituted by the movement of holes from emitter to the base, and (ii) electron current  $I_{nE}$  constituted by the movements of electrons from the base region to the emitter region. The forward biasing of the emitter junction increases the population of holes in the base region which will finally produce the collector current. So to have the collector current proportional to the emitter current, the emitter current should only be constituted by the hole current  $I_{pE}$  (i.e.  $I_E \approx I_{pE}$ ) or electron current  $I_{nE}$  should be negligibly small. This is possible when the emitter is heavily doped and base is very lightly doped, which is normally being done in the transistors.

We assume that the injection of electrons into the base region is a low level injection. Hence the minority carrier current  $I_{pE}$  is a hole diffusion current into the base. Its value is proportional to the concentration gradient of holes at  $J_E$  which is given by:

$$I_{pE} = -qD_p A \frac{dp_n}{dx} \quad \text{----- (6.5)}$$

Where  $D_p$  is the diffusion constant for holes,  $A$  is the area of cross section and  $q$  is the charge of an electron.

Similarly  $I_{nE}$ , electron diffusion current is proportional to the concentration gradient of electrons and is given by:

$$I_{nE} = -qD_n A \frac{dn_p}{dx} \quad \text{----- (6.6)}$$

where  $D_n$  is the diffusion constant for electrons. Thus  $I_{nE}$  is proportional to the slope of electron concentration  $n_p$  at the junction  $J_E$ .

The total emitter current is given by  $I_E = I_{pE} + I_{nE}$  ----- (6.7)

The directions of these currents are shown in figure (6.4), which are all positive flowing from emitter to base as these are conventional currents. The holes on crossing the emitter junction diffuse through the base region. In this process, some of the holes combine with the majority carrier electrons in the base region. In this way the number of holes reaching the collector junction will be less than the number of holes emitted at the emitter base junction. To reduce the possibility of this recombination in the base region, the width of the base region is made to be extremely small. Let  $I_{pCl}$  is the hole current at collector junction  $J_C$ , which is due to the holes reaching this junction through the base region. The current ( $I_{pE} - I_{pCl}$ ) is the recombination current which leaves the base as shown in figure

(6.4). The electrons enter the base region from the external circuit through the base lead to supply those charges which have been lost by recombination with the holes injected into base across  $J_E$ .

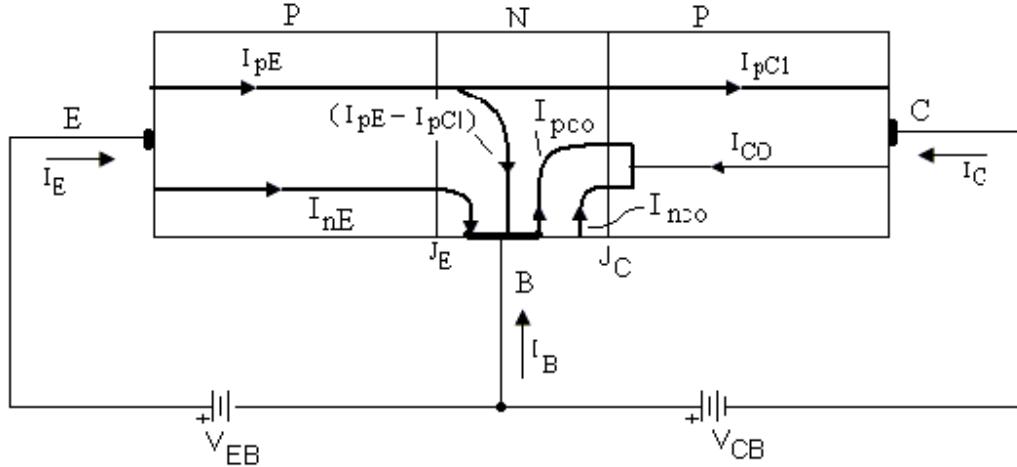


Fig. 6.4

It is further assumed for the time being, that the emitter base junction is open circuited so that  $I_E$  and  $I_{pC1}$  are equal to zero. Under this condition, the collector current  $I_C$  will be equal to the reverse saturation current  $I_{Co}$  of the base collector junction which is working as a simple reverse bias diode. This reverse saturation current  $I_{Co}$  will be the sum of two currents  $I_{Cn0}$  and  $I_{Cp0}$ . The  $I_{Cn0}$  is the current due to the movement of minority charge carrier electrons across  $J_C$  from collector ( p type) to base (n type), while  $I_{Cp0}$  is the current due to the movement of minority charge carrier holes across  $J_C$  from base (n type) to collector ( p type). Thus it may be written as :

$$-I_{Co} = I_{nCo} + I_{pCo} \quad \text{----- (6.8)}$$

(The minus sign is chosen arbitrarily so that  $I_C$  and  $I_{Co}$  will have the same sign.)

We now return to our original situation that emitter base junction is biased in the forward direction. Under this condition  $I_E \neq 0$  and collector current  $I_C$  is given by:

$$I_C = I_{Co} - I_{pC}$$

$$\text{or} \quad I_C = I_{Co} - \alpha I_E \quad \text{----- (6.9)}$$

where  $\alpha$  is defined as the fraction of the total emitter current  $I_E$  that represents the holes reaching the collector after traveling from the emitter through base. Since  $I_{Co}$  is small enough so  $\alpha$  is the ratio of the collector current to the emitter current

In a PNP transistor,  $I_E$  is positive and both  $I_C$  and  $I_{Co}$  are negative, which indicates the actual collector current is opposite to the assumed direction of the collector current shown in figure (6.4). However, in NPN transistor these currents are reversed.

We wish to find out the generalized transistor equation, as the equation (6.9) represents the collector current when the transistor is in the active region and also this current is independent of the collector voltage. To obtain such a generalized equation for

the collector current, which should be valid not only when the collector junction is reversed biased but also valid for any voltage across the  $J_C$ . We replace  $I_{Co}$  of equation (6.9) by the diode current equation.

$$\text{The diode current is given by: } I = I_s \left( e^{\frac{V}{V_T}} - 1 \right) \quad \text{----- (6.10)}$$

Here  $I_s$  is replaced by  $(-I_{Co})$  and  $V$  by  $V_C$ , the voltage across junction from collector to base. The equation (6.9) will become as:

$$I_C = -\alpha I_E + I_{C0} \left( 1 - e^{\frac{V_C}{V_T}} \right) \quad \text{----- (6.11)}$$

If  $V_C$  is negative and larger than  $V_T$ , the equation (6.11) reduces to:

$$I_C = -\alpha I_E + I_{Co}, \text{ which is the equation (6.9).}$$

**6.4 Base - Width Modulation or The Early Effect:** Consider a PNP transistor in active region whose emitter base junction is biased in forward direction and collector base junction is biased in reverse direction. The reverse biasing of the collector base junction in a transistor acts as a sink of minority charge carriers injected into the base region from the emitter region. It is well known that the width of the depletion region or the space charge region near the junction is large when the junction is in inverse bias and this width increases with the increase of reverse bias. So the width of the depletion region  $W$  is large at the collector junction  $J_C$  as compared to this value at the emitter junction  $J_E$ . Since the emitter base junction is in forward bias so the width of the depletion region is negligibly small at the emitter junction  $J_E$ . Since the doping in the base is ordinarily substantially smaller than that into the collector, so the penetration of the transition region in the base near the collector junction  $J_C$  will be larger than that into the collector. Hence, the whole of the depletion region may assume to be in the base region, as shown in figure (6.5a). Let  $W_b$  is the metallurgical base width and  $W$  is the width of the depletion layer. Now as the collector voltage is increased, the space charge layer takes up more of the metallurgical base width  $W_b$ , and as a result, the effective base width  $W'_b$  is decreased and is given by:  $W'_b = W_b - W$ . This effect given by J.M.Early, is known as base narrowing, base width modulation or the Early effect.

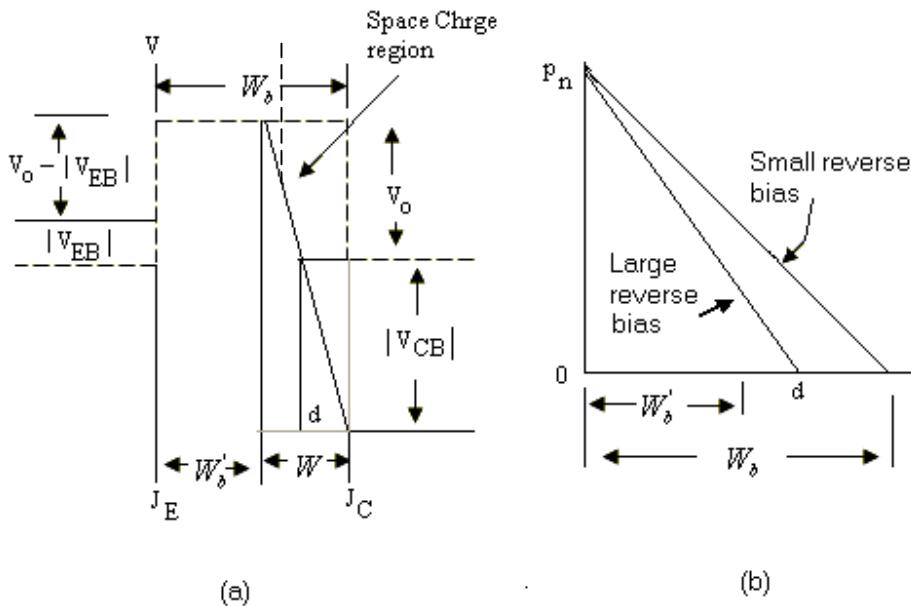


Fig. 6.5

The modulation of the effective base width  $W_b'$  with the increase in the collector voltage has three consequences:

1. The possibility of the recombination within the base is reduced, thereby increasing the collector current. Hence  $\alpha$  increases with the increase of  $|V_{CB}|$ .
2. The concentration gradient of the minority charge carriers in increased within the base region with the increase of  $|V_{CB}|$  and consequently hole current density  $J_E$  and then  $I_E$  increases (Ref. figure 6.5b).
3. For extremely large reverse bias at the collector base junction, the width of the deletion region becomes too large consequently the effective base width reduces to zero, causing voltage break down in the transistor. This breakdown phenomenon is called as ‘punch through’ or ‘reach through’.

**6.5 The Transistor as an Amplifier:** It is well known that the transistor has three terminals namely emitter, base and the collector; hence it is called a three terminal device. While using the transistor, one terminal is used as a reference or common terminal between input and output which is usually grounded. So the transistor may be used in three configurations, namely common base (CB), common emitter (CE) and common collector (CC) configurations. If the base is common between input and output terminals, the transistor is called in common base configuration. Similarly common emitter and common collector configurations may be defined. In any of the three configurations, transistor can provide the power gain (voltage amplification or current amplification) in the circuit. The transistor is, therefore, said to work as an amplifier.

To show that the transistor can work as an amplifier, we consider a transistor in common base configuration shown in figure (6.6), where a load resistance  $R_L$

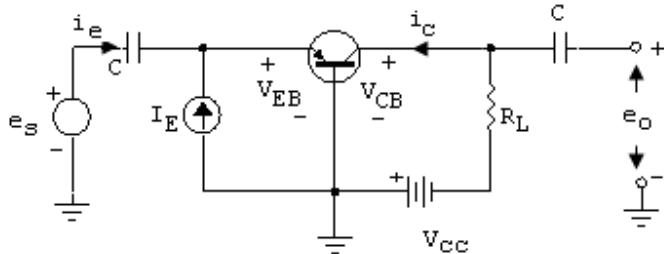


Fig. 6.6

is connected in series with the collector supply voltage  $V_{CC}$ . The transistor is biased in active or linear operating region, such that it remains in active region throughout the change in the emitter current due to the application of the input a.c. signal  $e_s$ . Thus the d.c. biasing of the emitter base junction is shown only by the current source  $I_E$ . The small signal  $e_s$  is connected across the emitter base junction, through a coupling capacitor  $C_c$  for the effective a.c. coupling. Since the emitter base junction is in forward bias, its incremental resistance  $r_e$  is very small of the order of  $25\Omega$ . The variation in emitter current due to  $e_s$  a.c. signal is represented by  $i_e$ , which is given by:

$$i_e = \frac{e_s}{r_e} \quad \text{----- (6.12)}$$

The corresponding change in collector current  $i_c$  will be given by:  $i_c = -\alpha i_e$ . The value of  $\alpha$  is nearly equal to unity. This collector current will flow in the load resistance  $R_L$  which is practically kept as high resistance since the reverse biased CB junction has a high output resistance. The output voltage is given by:

$$e_o = -i_c R_L = \alpha i_e R_L \quad \text{----- (6.13)}$$

$$\text{From equations (6.12) \& (6.13) we get : } e_o = \frac{\alpha e_s R_L}{r_e}$$

$$\text{or } A_V = \frac{e_o}{e_s} = \frac{\alpha R_L}{r_e}$$

$A_V$  is the voltage gain and its value will be of the order of 400 if  $R_L$  is chosen the practical value, as  $10K\Omega$ . The current gain  $\alpha$  is less than or equal to unity. The circuit, therefore, will have finite power gain, which is  $\alpha$  times the voltage gain. Thus the transistor gives the power gain by transferring current from the low resistance emitter circuit to the high resistance collector circuit, which signifies the name of the transistor as the transfer of resistance. The transistor may also be said to work as an amplifier.

**Example 6.1** A transistor having  $\alpha=0.96$  is connected in common base configuration with load resistance  $R_L = 5 K\Omega$ . If the incremental resistance of emitter base junction is  $60 \Omega$ , find the values of current gain, voltage gain and power gain of the amplifier.

**Solution:** The current gain of the amplifier in CB configuration is given by:

$$A_I = \frac{|I_C|}{|I_E|} = \alpha = 0.96$$

$$\text{The voltage gain } A_V \text{ is given by : } A_V = \frac{\alpha R_L}{r_e} = \frac{(0.96)(5000)}{60} = 80$$

The power gain =  $A_V \cdot A_I = 80 \times 0.96 = 76.8$

**6.6 Transistor Characteristics in Common Base Configuration:** Consider the PNP transistor in common base (CB) configuration, as shown in figure (6.7). In this circuit we have two variable voltages namely  $V_{EB}$  and

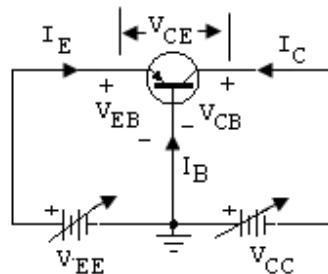


Fig. 6.7

$V_{CB}$  and two currents  $I_E$  and  $I_C$ . Graphs may be plotted by choosing two out of four variables as dependent variables and other two as independent variables. It is customary to choose input current  $I_E$  and output voltage  $V_{CB}$  as independent variables; and input voltage  $V_{EB}$  and output current  $I_C$  as the dependent variables. Thus the dependent variables as the function of independent variables are given by:

$$V_{EB} = f_1(V_{CB}, I_E) \quad \text{----- (6.14)}$$

$$I_C = f_2(V_{CB}, I_E) \quad \text{----- (6.15)}$$

**6.6.1 Input characteristics:** Figure (6.8) shows the plot of emitter to base voltage  $V_{EB}$  versus emitter current  $I_E$  for different collector to base voltage  $V_{CB}$ . The set of these curves are known as the static input characteristic curves or static emitter characteristics.

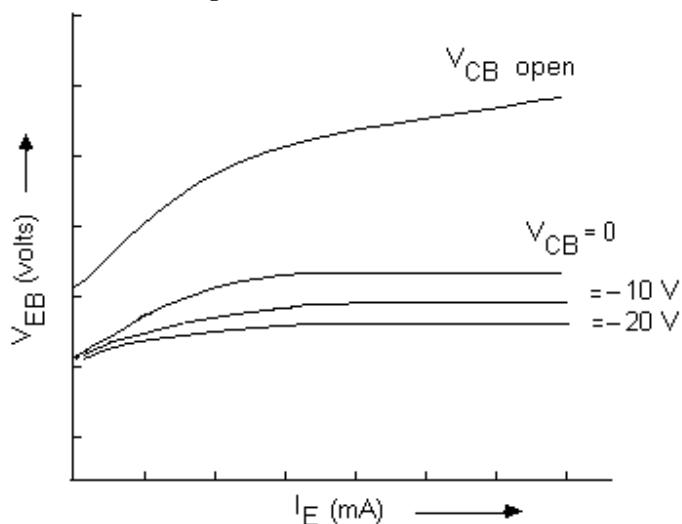


Fig. 6.8

The input characteristics shown in figure (6.8) represent simply the forward characteristics of the diode formed between the emitter and base region, for various collector voltages. It may be noted that there exists a cut in, or threshold voltage  $V_\gamma$ , below which the emitter current is negligibly small. In general this voltage is approximately 0.1 volt for Ge transistors, and 0.5 volt for Si transistors. From the characteristic curves it is clear that there is an increasing trend in the emitter current for the increase in the magnitude of the collector voltage for a constant  $V_{EB}$ . This can be explained on the basis of Early effect that when the magnitude of the collector voltage increases, the effective base width decreases causing thereby an increase in the concentration gradient of minority carriers in the base region due to which emitter current increases.

**6.6.2 Output characteristics:** Figure (6.9) shows the plot of collector to base voltage  $V_{CB}$  versus collector current  $I_C$  for different emitter current  $I_E$ . The set of these curves are known as the static output characteristic curves or static collector characteristics. On the basis of biasing conditions of the two junctions, these output characteristics may be divided into three regions namely active region, saturation region and cutoff region.

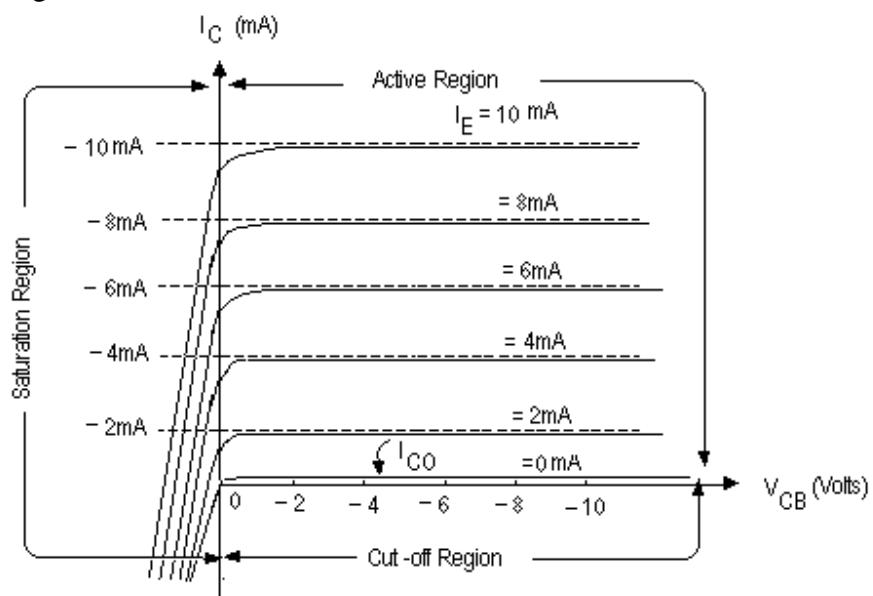


Fig. 6.9

**Active region:** In the active region the collector base junction is biased in the reverse bias whereas the emitter base junction is biased in the forward direction. From the output characteristics, it is clear that when  $I_E = 0$ , the collector current is very small and is equal to the reverse saturation  $I_{CO}$  of the diode formed by the collector base junction. The emitter current  $I_E$  flowing the emitter circuit due to the forward biasing of the emitter base junction causes a fraction of  $I_E$  to flow as collector current given by  $I_C = -\alpha I_E + I_{CO}$ . In the active region, the collector current depends only on the emitter current and is independent of  $V_{CB}$ . However, because of the early effect, there is only a small increase in the collector current (approximately 0.5%) with the increase in the magnitude of the  $V_{CB}$ .

Since  $\alpha \leq 1$ , magnitude of the collector current is slightly less than that of the emitter current.

**Saturation region:** In the saturation region both the emitter base and collector base junctions of the transistor are in forward bias. This region exists to the left side of the ordinate,  $V_{CB} = 0$ , and above  $I_E = 0$  in the output characteristics shown in figure (6.9). In this region, near  $V_{CB} \approx 0$  the magnitude of the collector current decreases to the bottom of the curve and it is known that the bottoming has taken place. Actually,  $V_{CB}$  is slightly positive in this region, this forward biasing of the collector junction leads a large change in the collector current. So there is an exponential rise in the collector current for the small increase in  $V_{CB}$  given by diode equation. This is the reason of the bottoming. The collector current may even become positive if there is a large increase in the forward bias of the collector voltage.

**Cutoff Region:** The collector current  $I_C$  is very small roughly equal to  $I_{C0}$ , for  $I_E = 0$  in the output characteristics shown in figure (6.9), so this curve is slightly above the  $V_{CB}$  axis and passes through the origin. The region below  $I_E = 0$  is known as the cutoff region. In this region both emitter and collector junctions are in reverse bias. In the cutoff region the collector current  $I_C \approx 0$ . So the transistor in the cutoff region is used in switching circuits as the OFF state. Conversely, the ON state in the switching circuits is represented by the saturation region of the transistor.

**6.7 Transistor Characteristics in Common Emitter Configuration:** The common emitter configuration is most commonly used in the transistor circuits. Figure (6.10) shows the PNP transistor in common emitter configuration in which the emitter is common or grounded.

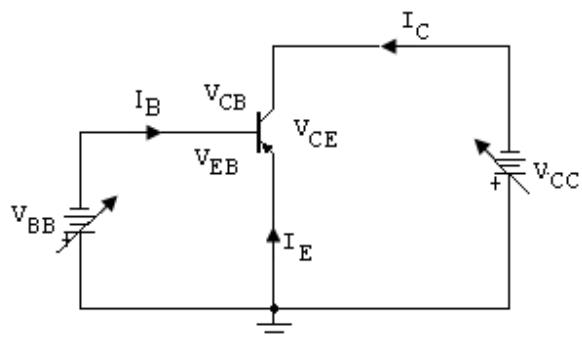


Fig. 6.10

In this configuration too we choose input current  $I_B$  and output voltage  $V_{CE}$  as independent variables; and input voltage  $V_{BE}$  and output current  $I_C$  as the dependent variables. Thus the dependent variables as the function of independent variables are given by:

$$V_{BE} = f_1(V_{CE}, I_B) \quad \text{----- (6.16)}$$

$$I_C = f_2(V_{CE}, I_B) \quad \text{----- (6.17)}$$

**6.7.1 Input characteristics:** Figure (6.11) shows the plot of base current  $I_B$  versus base to emitter voltage  $V_{BE}$  for different collector to emitter voltage  $V_{CE}$ . The set of these curves are known as the static input characteristics for CE configuration. For collector

shorted with emitter (i.e. the curve indicated by  $V_{CE} = 0$ ), the emitter is forward bias and the curve is essentially the forward bias diode characteristic curve. If  $V_{BE}$  becomes zero then both emitter and collector junctions are short circuited, resulting thereby the base current zero. It is clear from these input characteristic curves that there is a decrease in magnitude of base current with the increase in magnitude of  $V_{CE}$  for constant  $V_{BE}$ . In general, if  $V_{BE}$  is held constant there is an increase in magnitude of the  $V_{CB}$  with the increase in  $V_{CE}$ , as  $V_{CE} = V_{CB} + V_{BE}$ . As per early effect, the increase in  $V_{CB}$  results the decrease in effective base width  $W_b$ . There will be less chances of recombination in the base region and thus base current decreases. It may be mentioned here that the break away point (the point where the current breaks away from zero current) in the transistor characteristic curves lies in the range of 0.5 to 0.6 volt for Si transistor and 0.1 to 0.2 for Ge transistor.

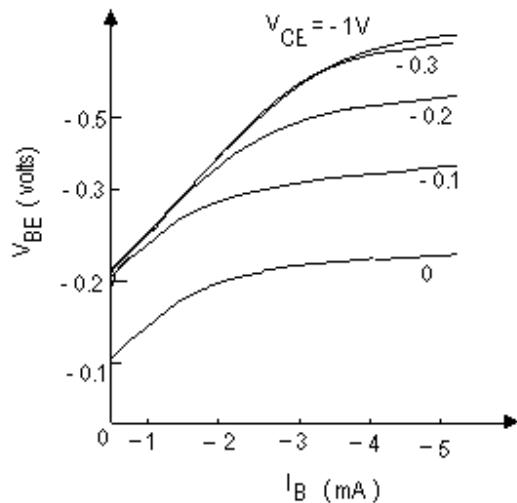


Fig. 6.11

**6.7.2 Output characteristics:** Figure (6.12) shows the plot of collector to emitter voltage  $V_{CE}$  versus collector current  $I_C$  for different base current  $I_B$ . The set of these curves are known as the static output characteristic curves for CE configuration. On the basis of biasing conditions of the two junctions, these output characteristics may be divided in to three regions namely active region, saturation region and cutoff region.

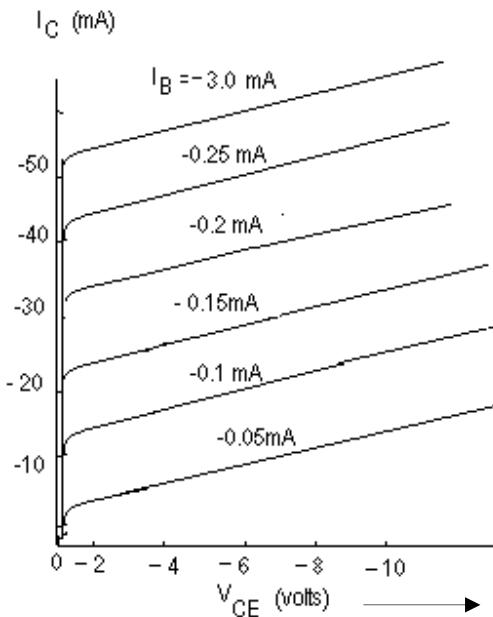


Fig. 6.12

**Active region:** In the active region the collector junction is biased in the reverse bias whereas the emitter junction is biased in the forward direction. The region above  $I_B = 0$ , to the right side of the  $I_C$  axis in figure (6.12) where  $V_{CE}$  is few tenths of a volt, is known as active region. The transistor to be used as an amplifying device, it should be operated in this active region.

As already discussed, the sum of the three transistor currents is zero i.e.

$$I_E + I_B + I_C = 0 \quad \text{----- (6.18)}$$

The value of  $I_E$  from equation (6.9) is given by:

$$I_E = -\frac{I_C}{\alpha} + \frac{I_{C0}}{\alpha} \quad \text{----- (6.19)}$$

From equations (6.18) & (6.19) we get:

$$I_B + I_C - \frac{I_C}{\alpha} + \frac{I_{C0}}{\alpha} = 0$$

or  $I_C \left( \frac{\alpha-1}{\alpha} \right) + \frac{I_{C0}}{\alpha} = -I_B$

or  $I_C = \left( \frac{\alpha}{1-\alpha} \right) I_B + \left( \frac{1}{1-\alpha} \right) I_{C0} \quad \text{----- (6.20)}$

or  $I_C = \beta \cdot I_B + (1 + \beta) \cdot I_{C0} \quad \text{----- (6.21)} \quad \text{where}$

$\beta = \left( \frac{\alpha}{1-\alpha} \right)$ . Since  $I_{C0} \ll I_B$  so  $I_C \approx \beta I_B$ , in the active region. The factor  $\beta$  is called as the current gain defined as the ratio of the collector current to the base current.

If  $\alpha$  were perfectly constant,  $I_C$  would be independent of  $V_{CE}$  (equation 6.20) and the characteristics should have been horizontal. These curves are not horizontal but the large variations in the characteristics are observed, which may be explained on the basis of Early Effect. According to the Early Effect  $\alpha$  increases with the increase of  $V_{CE}$  (as  $V_{BE}$  is small so  $V_{CE} \approx V_{CB}$ ). There is only about 0.5% increase in  $\alpha$  when  $V_{CE}$  increases few volts. The numerical data, however, reveals that there is about 34% increase in  $\beta$

with 0.5% increase in  $\alpha$  (as  $\beta = \frac{\alpha}{1-\alpha}$ ). In view of the fact that  $I_C = \beta I_B$ , this leads a

large increase in the magnitude of collector current. It clearly indicates that the characteristic curves are having some slope rather being horizontal.

**CE Cutoff Region:** In a transistor, cutoff refers to the condition where the collector current is zero or it is very small, approximately equal to the reverse saturation current  $I_{C0}$ . The transistor may, therefore, be in the open circuit condition. The cutoff in the figure (6.12) occurs at the intersection of load line with the base current  $I_B = 0$ . If  $I_B$  is equal to zero then the collector current  $I_C$  will be given by (using equation 6.20):

$$I_C = -I_E = \frac{I_{C0}}{(1-\alpha)} \equiv I_{CEO} \quad \text{----- (6.22)}$$

The symbol  $I_{CEO}$  is the collector current with collector junction reverse biased and base open circuited. This value of collector current in cutoff region is quite large for Ge transistors as  $\alpha$  is generally equal to 0.9 (Ge transistor) and thus

$$I_C \approx \frac{I_{C0}}{1-0.9} \approx 10I_{C0}$$

i.e. the collector current is approximately ten times to that of  $I_{C0}$  for Ge transistor. In order to satisfy the condition for cutoff, the collector current is to be reduced so that it becomes equal to  $I_{C0}$ . To obtain the collector current to be equal to  $I_{C0}$ ,  $I_E$  should be made equal to zero as  $I_C = I_{C0} - \alpha I_E$ . It is found that if a reverse biasing voltage of the order of 0.1 volt is applied across the emitter junction, then Ge transistor will be in cutoff. However, in Si transistors, cutoff occurs at  $V_{BE} = 0$ . It is concluded from the above discussions that the cutoff means  $I_E = 0$ ,  $I_C = I_{C0}$ ,  $I_B = -I_C$  and  $V_{BE}$  is a reverse voltage whose magnitude is of the order of 0.1 volt for Ge transistor and 0 volt for Si transistor (ref. fig. 6.13).

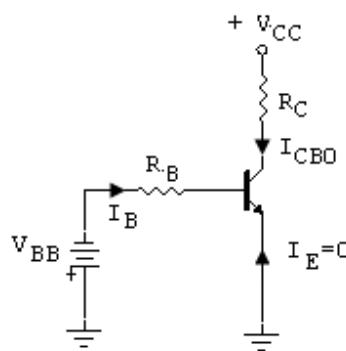


Fig 6.13

The collector current, when the emitter current is zero is represented by  $I_{CBO}$ . This current is larger than  $I_{C0}$  because (i) a large leakage current also flows across the surface not through the junction which is proportional to the voltage across the junction; and (ii) the new carriers may be generated by collision in the transition region of the collector junction leading to breakdown due to avalanche multiplication. At room temperature the  $I_{CBO}$  is of the order of a few microamperes for Ge and a few nano amperes for Si transistor. Since the current  $I_{CBO}$  approximately doubles with the  $10^{\circ}\text{C}$  rise in the temperature as in the case of junction diode. Hence Si transistor can be used up to  $200^{\circ}\text{C}$  and the Ge transistor can be used only up to  $100^{\circ}\text{C}$ .

**CE Saturation Region:** In the saturation region both emitter and collector junctions are in forward bias. The saturation region is very close to zero voltage axis, where the bottoming is taking place i.e. the region where all the curves merge and rapidly fall to the origin. It has been observed that the region to the left of  $0.3\text{ V}$  for Si ( $0.1\text{ V}$  for Ge) is the saturation region. To explain the saturation region in more details, the characteristic curves in between  $0$  to  $-0.5$  volt has been expanded as shown in figure 6.14. From this figure, we find that  $V_{CE}$  and  $I_C$  do not respond appreciably to the variations in the base current, once the base current exceeds the value  $-0.15\text{ mA}$  i.e. these curves are independent of base current and look like approximately the straight lines. The inverse of the slope of the curve in this region is known as common emitter saturation resistance  $R_{CS}$ ,  $R_{CES}$  or  $R_{CE(Sat)}$  given by the ratio  $V_{CE(Sat)} / I_C$ .

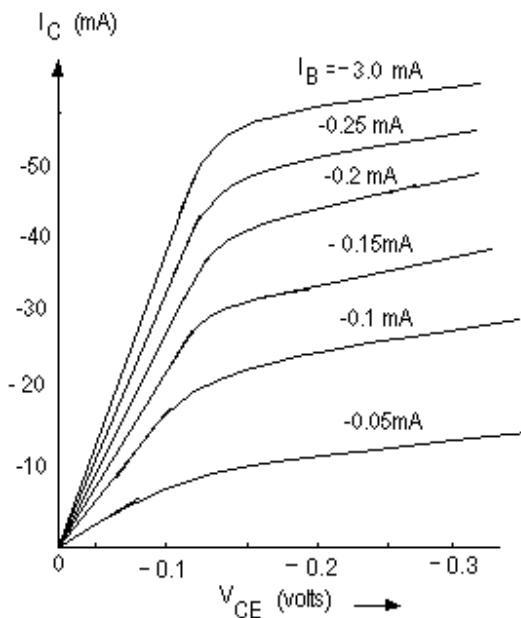


Fig. 6.14

**6.8 Common Emitter Current Gain:** Three different definitions of the current gain of a transistor will be discussed here:

- (i) **Large Signal Current gain  $\beta$ :** This current gain has earlier been defined as  $\beta = \left( \frac{\alpha}{1-\alpha} \right)$ . However, in equation (6.21) we replace  $I_{C0}$  with  $I_{CB0}$  we get,

$$I_C = \beta I_B + (1+\beta) I_{CB0} \quad \text{----- (6.23)}$$

or 
$$\beta = \frac{I_C - I_{CB0}}{I_B - (-I_{CB0})} \quad \text{----- (6.24)}$$

The common emitter cutoff region is defined by  $I_E = 0$ ,  $I_C = I_{CB0}$  and  $I_B = -I_{CB0}$ . The numerator of this equation (6.24) is the increment in the collector current where as denominator is the increment in the base current from the currents of the cut-off region. So  $\beta$  may be defined as the ratio of collector current increment to the base current increment. Thus  $\beta$  represents the large signal current gain of a CE transistor.

- (ii) **D.C. Current Gain  $h_{FE}$ :** The current gain or the d.c. forward transfer current gain or the  $\beta$  d.c. denoted by  $\beta_{d.c.}$  or  $h_{FE}$  is defined as:

$$\beta_{d.c.} \equiv \frac{I_C}{I_B} = h_{FE}. \quad \text{----- (6.25)}$$

- (iii) **Small Signal Current gain:** The quantity  $\beta'$  is defined as the ratio of collector current gain  $\Delta I_C$  to the base current increment  $\Delta I_B$  at the operating point with the fixed  $V_{CE}$ . Thus

$$\beta' \equiv \left. \frac{\partial I_C}{\partial I_B} \right|_{V_{CE}=\text{constant}} = h_{fe} \quad \text{----- (6.26)}$$

$\beta'$  is used for the analysis of small signal amplification hence known as small signal current gain. If  $\beta$  is independent of the magnitude of the current then differentiating equation (6.23) w.r.t.  $I_C$  we get:

$$(I_{CB0} + I_B) \frac{\partial \beta}{\partial I_C} + \beta \frac{\partial I_B}{\partial I_C} = 1$$

or 
$$\frac{\beta}{\beta'} = \left( 1 - (I_{CB0} + I_B) \frac{\partial \beta}{\partial I_C} \right)$$

or 
$$\beta = \beta' \left( 1 - (I_{CB0} + I_B) \frac{\partial \beta}{\partial I_C} \right)$$

or 
$$h_{fe} = \frac{h_{FE}}{\left( 1 - (I_{CB0} + I_B) \frac{\partial \beta}{\partial I_C} \right)} \quad \text{----- (6.24)}$$

as  $\beta = h_{FE}$  and  $\beta' = h_{fe}$ .

It has been observed that over the entire range of  $I_C$ ,  $h_{fe}$  differs from  $h_{FE}$  by less than 20%.

It may, however, be noted this equation (6.24) is true only for the active region. In saturation region,  $h_{fe} \rightarrow 0$  as  $\Delta I_C \rightarrow 0$  for a small increment  $\Delta I_B$ .

**6.9 Common Collector Configuration:** The common collector configuration as will be discussed in the next chapter is mainly used for impedance matching since it has high input impedance and low output impedance. The CC configuration is shown in figure

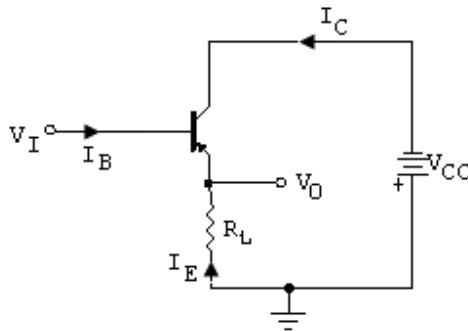


Fig. 6.15

(6.15), in which the load resistance connected between emitter and ground rather than collector and ground. This circuit seems to be similar to the common emitter configuration. From the design point of view, there is no need for a set of common collector characteristics to choose the parameter of the amplifier. For all practical purposes, the output characteristics of the CC configuration are the same as for the CE configuration. For the CC configuration the output characteristics are a plot of  $I_E$  versus  $V_{EC}$  for the different range of base current  $I_B$ . The input current is, therefore, the same both the two types of the configurations. The horizontal voltage axis for CC configuration is obtained by simply changing the sign of the collector to emitter voltage of the CE characteristics. Since  $I_C = \alpha I_E$  and  $\alpha \approx 1$ , so there will not be a remarkable change in the vertical axis.

**Typical junction voltages:** The typical junction voltages of a NPN transistor at  $25^{\circ}\text{C}$  are given in volts, in the form of a table :

Transistor	$V_{BE,\text{cutoff}}$	$V_{BE,\text{cutin}}$	$V_{BE,\text{active}}$	$V_{BE,\text{Sat}}$	$V_{CE,\text{Sat.}}$
Si	0	0.5	0.7	0.8	0.2
Ge	-0.1	0.1	0.2	0.3	0.1

For a PNP transistor the sign of all the entries are reversed. It should be remembered that the transistor to be in the active region, the collector current should be equal to  $\beta I_B$  (neglecting  $I_{C0}$ ); and in the saturation region the base current should be greater than

or equal to  $\frac{I_C}{\beta}$ .

**Example 6.2** (i) Find the values of  $I_B$  and  $I_C$  in the circuit given below (figure 6.16), knowing in which region the transistor is working. The Si transistor with  $\beta = 150$  and  $I_{C0} = 22 \text{ nA}$  is used in the circuit.

(b) Repeat part (i) with  $R_B = 370 \text{ K}\Omega$ .

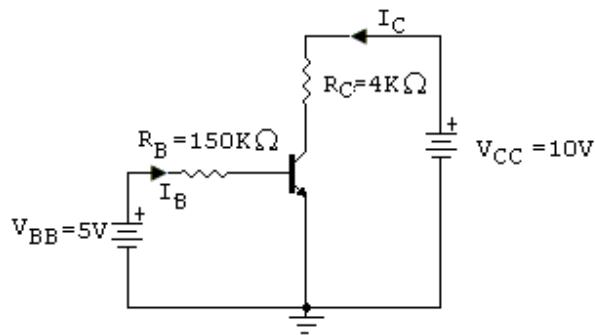


Fig. 6.16

Solution: (i) First of all we find the region in which the transistor is working, whether it is in cutoff, active or saturation region. Since the emitter base junction is in forward bias, it is therefore, clear that the transistor is not in the cutoff region. The transistor may either be in the active or in the saturation region.

Let us assume that the transistor is in the active region. Applying the KVL to the input circuit, we get:

$$V_{BB} = R_B I_B + V_{BE,active}$$

or  $5 V = 150 K \cdot I_B + 0.7 V$

or  $I_B = \frac{5 - 0.7}{150} mA = 28.7 \mu A$

and  $I_C = \beta I_B = 150 \times 28.7 \mu A = 4.3mA$  neglecting  $I_{CO}$ .

Applying KVL to the output circuit we get:

$$V_{CC} = R_C I_C + V_{CE}$$

or  $V_{CE} = 10 V - (4K)(4.3mA) = -7.2 Volts$

But  $V_{CE} = V_{CB} + V_{BE,active}$

or  $V_{CB} = -7.2 - 0.7 = -7.9$

The transistor used in this circuit is NPN, so negative value of  $V_{CB}$  means collector is negative w.r.t. base; and the collector base junction is in forward bias. The transistor is therefore, not in the active region and our assumption is wrong. The transistor is now said to be biased in the saturation region.

Now applying KVL to the input circuit we get:

$$V_{BB} = R_B I_B + V_{BE, Sat}$$

or  $5 V = 150 K \cdot I_B + 0.8 V$

or  $I_B = \frac{5 - 0.8}{150} mA = 28 \mu A$

Applying KVL to the output circuit we get:

$$V_{CC} = R_C I_C + V_{CE, Sat}$$

or  $I_C = \frac{10.0 - 0.2}{4K} = \frac{9.8}{4} mA = 2.45mA$

We check the condition of saturation ( $I_B \geq \frac{I_C}{\beta}$ ), which is true as  $28 \mu A > 1.63 \mu A$ . The required values of  $I_C$  and  $I_B$  are  $2.45 mA$  and  $28 \mu A$ , and the transistor is in saturation.

(ii) Let us assume that the transistor is in the active region. Applying the KVL to the input circuit, we get:

$$V_{BB} = R_B I_B + V_{BE, active}$$

or  $5 V = 370 K. I_B + 0.7 V$

$$\text{or } I_B = \frac{5 - 0.7}{370} mA = 11.62 \mu A$$

$$\text{and } I_C = \beta I_B = 150 \times 11.62 \mu A = 1.74 mA \text{ neglecting } I_{C0}.$$

Applying KVL to the output circuit we get:

$$V_{CC} = R_C I_C + V_{CE}$$

$$\text{or } V_{CE} = 10 V - 4K \times 1.74 mA = 3.04 \text{ Volts}$$

$$\text{But } V_{CE} = V_{CB} + V_{BE, active}$$

$$\text{or } V_{CB} = 3.04 - 0.7 = 2.34 \text{ volts}$$

The positive value of  $V_{CB}$  means the collector is positive w.r.t. base, CB junction is in reverse bias. The transistor is therefore, in the active region, which verifies our assumption; and the required values  $I_B$  and  $I_C$  are  $11.62 \mu A$  and  $1.74 mA$  respectively.

**Example 6.3** For the circuit shown in figure (6.17), assume  $\beta = 100$ . Find

- (i) if the Si transistor is in cutoff, saturation or in active region,
- (ii) output voltage  $V_0$ , and
- (iii) minimum value for  $R_E$  for which the transistor operates in the active region.

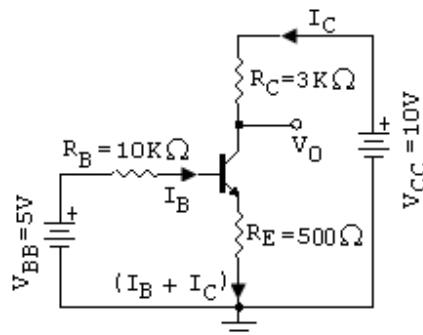


Fig. 6.17

Solution: (i) Suppose the transistor is in saturation region. Applying the KVL to the input and output circuits we get:

$$\begin{aligned} V_{BB} &= R_B I_B + V_{BE, Sat} + R_E(I_B + I_C) \\ 5V &= 10K \cdot I_B + 0.8V + 0.5K(I_B + I_C) \\ 4.2V &= 10.5K \cdot I_B + 0.5K \cdot I_C \quad \text{----- (6.25)} \\ V_{CC} &= R_C I_C + V_{CE, Sat} + R_E(I_B + I_C) \\ 10V &= 3K \cdot I_C + 0.2V + 0.5K(I_B + I_C) \end{aligned}$$

$$9.8V = 3.5K \cdot I_C + 0.5K \cdot I_B \quad \text{----- (6.26)}$$

Solving the equations (6.25) & (6.26) for  $I_B$  and  $I_C$  we get:

$$I_B = 0.28 \text{ mA} \text{ and } I_C = 2.76 \text{ mA}$$

Since  $I_B \geq \frac{I_C}{\beta}$  ( $0.28 \text{ mA} > 0.0276 \text{ mA}$ ), hence the transistor is in saturation.

$$\begin{aligned} \text{(ii)} \quad V_0 &= V_{CC} - R_C I_C = 10V - (3K)(2.76mA) \\ &= 1.72 \text{ volts} \end{aligned}$$

(iii) For the transistor to operate in the active region,  $V_{BE, \text{active}} = 0.7 \text{ V}$  and  $V_{BC}$  should be in the reverse bias (greater than zero say  $0.1V$ ). So the transistor to operate in the active region  $V_{CE}$  should be at least equal to  $0.8 \text{ V}$  (as  $V_{CE} = V_{BE} + V_{CB}$ ). Also in the active region  $I_C = \beta I_B$ , (neglecting  $I_{C0}$ ).

Applying KVL to the input circuit we get:

$$\begin{aligned} V_{BB} &= R_B I_B + V_{BE, \text{Active}} + R_E(1+\beta)I_B \\ 5V &= (10K)I_B + 0.7V + R_E(101)I_B \\ 4.3V &= (10K)I_B + R_E(101)I_B \quad \text{----- (6.27)} \end{aligned}$$

Now applying KVL to the output circuit we get:

$$\begin{aligned} V_{CC} &= (3K)(\beta I_B) + V_{CE} + R_E(1+\beta)I_B \\ 10V &= (3K)(100 I_B) + 0.8V + R_E(101)I_B \\ 9.2V &= (300K)I_B + R_E(101)I_B \quad \text{----- (6.28)} \end{aligned}$$

Solving the equations (6.27) & (6.28) we get  $R_E = 2.42 \text{ k}\Omega$ .

This is the minimum value of  $R_E$  for the transistor to operate in the active region.

**Example 6.4** Find the value of the resistance  $R$  connected between collector and base of a Si transistor with  $\beta = 49$ , shown in figure (6.18). Neglect the reverse saturation collector current of the transistor. Transistor is operated in the active region.

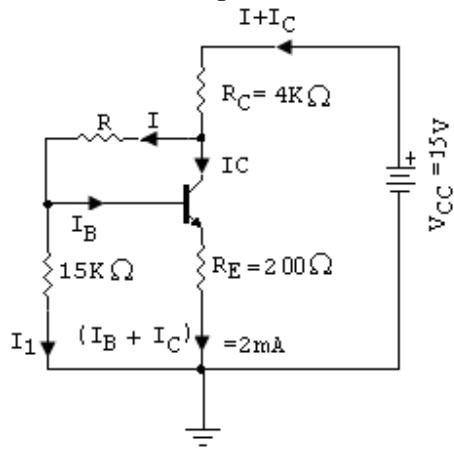


Fig. 6.18

**Solution:** Since  $V_{BE} = 0.7V$ , it indicates that the transistor is in the active region. So  $I_C = \beta I_B$  and  $I_C + I_B = 2 \text{ mA}$  (Given)

$$I_B = (2/50) \text{ mA} = 0.04 \text{ mA} \quad \text{and} \quad I_C = (49) \times (0.04) = 1.96 \text{ mA}$$

$$\begin{aligned} \text{Voltage across } 15K\Omega \text{ resistance } V_i &= V_{BE, \text{Active}} + (0.2K) \times (2 \text{ mA}) \\ &= 0.7 + 0.4 = 1.1 \text{ V} \end{aligned}$$

Current flowing through  $15K\Omega$  resistance  $I_I = \frac{1.1V}{15K\Omega} = 0.0733mA$

Current through resistance R is  $I = I_I + I_B = 0.0733 + 0.04 = 0.1133 mA$

Applying KVL to the input circuit we get:

$$\begin{aligned} V_{CC} &= R_C(I + I_C) + R.I + V_i \\ \text{or } 15V &= (4K)(0.1133 + 1.96)mA + R(0.1133mA) + 1.1V \\ \text{or } R &= 49.49 K\Omega \end{aligned}$$

**Example 6.5** A Si transistor with  $\beta = 100$  is connected as shown in figure (6.19) Find the minimum value of the collector resistance  $R_C$  for which the transistor remains in saturation.

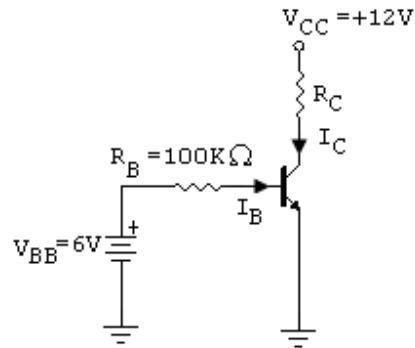


Fig. 6.19

Solution: To have the transistor in saturation region,  $V_{BE} = V_{BE,Sat} = 0.8 V$  and  $V_{CE} = V_{CE,Sat} = 0.2 V$ .

Now applying the KVL to the input circuit we have:

$$\begin{aligned} V_{BB} &= R_B I_B + V_{BE,Sat} \\ 6V &= (100K)(I_B) + 0.8V \\ \text{or } I_B &= \frac{(6 - 0.2)V}{100K\Omega} = 0.052mA \end{aligned}$$

Similarly applying KVL to the input circuit we have:

$$\begin{aligned} V_{CC} &= R_C I_C + V_{CE,Sat} \\ 12V &= R_C I_C + 0.2 \\ \text{or } I_C &= \frac{(12 - 0.2)V}{R_C} = \frac{11.8V}{R_C} \end{aligned}$$

For the transistor to be in the saturation region :

$$\begin{aligned} \beta \cdot I_B &\geq I_C \\ (100)x(0.052mA) &\geq \frac{11.8}{R_C} \\ \text{or } R_C &\geq \frac{11.8V}{5.2mA} \\ \text{or } R_C &\geq 2.27K\Omega \end{aligned}$$

So the required minimum value of  $R_C = 2.27 K\Omega$ .

**Example 6.6** A Si transistor with  $\beta = 30$  is used in the circuit shown in figure (6.20).  $I_{CBO} = 10 nA$  at  $25^{\circ}C$ .

- Find (i)  $V_0$  for  $V_i = 12 V$  and show that the transistor is in saturation for  $R_I = 15 K\Omega$ ,  
(ii) the minimum value of  $R_I$  for which the transistor is in active region for  $V_i = 12 V$ ,  
(iii)  $V_0$  for  $R_I = 15 K\Omega$  and  $V_i = 1 V$  and show that the transistor is in cut-off, and  
(iv) the maximum temperature at which transistor remains in cut-off for  $R_I = 15 K\Omega$  and  $V_i = 1 V$ .

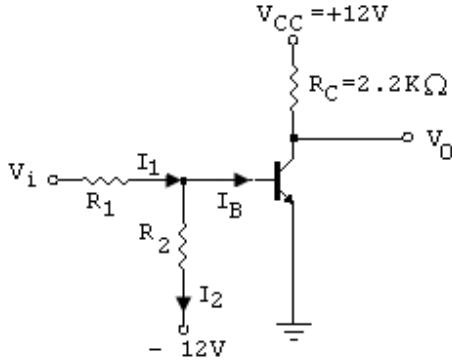


Fig. 6.20

Solution: (i) Let the transistor is in saturation,  $V_{BE, Sat} = 0.8 V$

$$I_1 = \frac{(V_i - 0.8)V}{15K\Omega} = \frac{(12 - 0.8)V}{15K\Omega} = 0.75mA$$

$$I_2 = \frac{(12.0 + 0.8)V}{100K\Omega} = \frac{12.8V}{100K\Omega} = 0.128mA$$

$$I_B = I_1 - I_2 = 0.75 - 0.128 = 0.622 mA$$

Applying KVL to the output circuit, we get:

$$V_{CC} = R_C I_C + V_{CE, Sat}$$

$$12V = (2.2K\Omega) I_C + 0.2$$

or  $I_C = \frac{(12 - 0.2)V}{2.2K\Omega} = \frac{11.8}{2.2K\Omega} = 5.36mA$

$$\frac{I_C}{\beta} = \frac{5.36mA}{30} = 0.179mA$$

Since  $I_B > (I_C/\beta)$  hence the transistor is in saturation.

So  $V_0 = V_{CE, Sat} = 0.2 V$

(ii) Let the transistor is in active region,  $V_{BE, active} = 0.7 V$

$$I_1 = \frac{(V_i - 0.7)V}{R_I} = \frac{(12 - 0.7)V}{R_I} = \frac{11.3V}{R_I}$$

$$I_2 = \frac{(12.0 + 0.7)V}{100K\Omega} = \frac{12.7V}{100K\Omega} = 0.127mA$$

$$I_B = I_1 - I_2 = \frac{11.3V}{R_I} - 0.127mA$$

In the active region  $I_C = \beta I_B$

$$\text{So } I_C = 30 \left( \frac{11.3V}{R_1} - 0.127mA \right) = \frac{339}{R_1} - 3.81mA$$

$$\begin{aligned} \text{From the output circuit } V_{CE} &= V_{CC} - I_C R_C = 12V - \left( \frac{339}{R_1} - 3.81mA \right) (2.2K\Omega) \\ &= 20.38 - \frac{745.8}{R_1} \end{aligned}$$

The transistor will be in the active region if  $V_{CB} \leq -0.5V$  which implies:

$$V_{CB} = V_{CE} - V_{BE} = 20.38 - \frac{745.8}{R_1} - 0.7V = 19.68 - \frac{745.8}{R_1}$$

$$\text{or } 19.68 - \frac{745.8}{R_1} \leq -0.5V$$

$$\text{or } \frac{745.8}{R_1} \leq 20.18V$$

$$\text{or } R_1 \geq 36.95K\Omega \quad \text{So minimum value of } R_1 = 36.95K\Omega$$

(iii) We find  $V_{BE}$  by applying Superposition theorem as:

$$\begin{aligned} V_{BE} &= \frac{(1V)(100K\Omega)}{(100+15)K\Omega} + \frac{(12V)(15K\Omega)}{(100+15)K\Omega} = \frac{100}{115} - \frac{180}{115} = 0.896 - 1.565 \\ &= -0.7V \end{aligned}$$

This implies the transistor is in cut-off region. So  $V_0 = V_{CC} = 12V$

(iv) For the transistor to be in the cut-off region,  $V_{BE} = 0V$  and the base current will be equal to  $I_{CBO}$  which is given by:

$$I_{CBO} = I_2 - I_1 = \frac{12V}{100K\Omega} - \frac{1V}{15K\Omega} = 0.12mA - 0.67mA = 0.053mA$$

The  $I_{CBO}$  varies with temperature as:

$$I_{CBO}(T) = I_{CBO}(T_0) \times 2^{(T-T_0)/10}$$

$$\text{As } T_0 = 25^{\circ}\text{C} \quad \text{so} \quad 0.053mA = (10 \times 10^{-6}mA) \times 2^{(T-25)/10}$$

$$2^{(T-25)/10} = 5300$$

$$\{(T-25)/10\} \log 2 = \log 5300$$

$$(T-25)/10 = 12.37$$

$$T = 148.7^{\circ}\text{C}$$

This is the maximum temperature for which the transistor remains in cut-off.

**Example 6.7** (i) The reverse saturation current of the Ge diode connected in the circuit shown in figure (6.21), is  $2 \mu\text{A}$  at  $25^{\circ}\text{C}$  and increases by a factor of two for every  $10^{\circ}\text{C}$  rise in temperature. If  $V_{BB} = 5V$ , find the maximum allowable value of the resistance  $R_B$  if the transistor is to remain in cut-off at a temperature of  $75^{\circ}\text{C}$ .

(ii) If  $V_{BB} = 1V$  and  $R_B = 50K\Omega$ , how high may the temperature increase before the transistor comes out of cut-off.

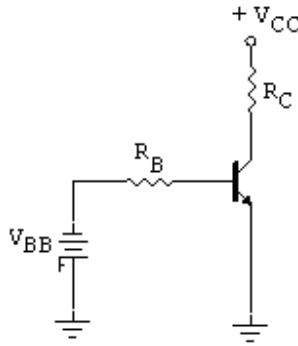


Fig. 6.21

Solution: (i) For the Ge transistor to be in the cut-off region,  $V_{BE} = -0.1V$   
The  $I_{CO}$  varies with temperature as:

$$I_{CO}(T) = I_{CO}(T_0) \times 2^{(T-T_0)/10}$$

Where  $T = 75^{\circ}\text{C}$   $T_0 = 25^{\circ}\text{C}$  and  $I_{CO}(T_0) = 2\mu\text{A}$

$$\text{So } I_{CO}(75) = (2\mu\text{A}) \times 2^{(75-25)/10} = (2\mu\text{A})(2^5) = 64\mu\text{A}$$

In the cut-off region  $I_{CO}(T_0)$  current will flow as the base current, so

$$V_{BB} - V_{BE,Cutoff} = R_B I_{CO}(T)$$

$$5V - 0.1V = R_B(64\mu\text{A})$$

or

$$(ii) \quad V_{BB} - V_{BE,Cutoff} = R_B I_{CO}(T)$$

$$V_{BB} = 1.0 \text{ V}, R_B = 50 \text{ K}\Omega$$

The transistor will come out of cut-off region when  $V_{BE}$  is slightly more than  $-0.1V$  so

$$1 - 0.1 = (50 \text{ K}\Omega) I_{CO}(T)$$

$$I_{CO}(T) = 18 \mu\text{A}$$

$$18\mu\text{A} = (2\mu\text{A}) \times 2^{(T-T_0)/10}$$

$$2^{(T-T_0)/10} = 9\mu\text{A} \quad \text{or} \quad (T - T_0) = 31.7^{\circ}\text{C}$$

$$T = 31.7 + 25 = 56.7^{\circ}\text{C}$$

**6.10 Ebers – Moll Model of a Transistor:** We have already studied the equation which shows the dependence of currents in a transistor upon the junction voltages given by equation (6.11) as:

$$I_C = -\alpha I_E - I_{CO} \left( e^{\frac{V_C}{V_T}} - 1 \right) \quad \text{----- (6.29)}$$

For a physical transistor, the emitter and collector junctions are quite alike, except a little difference in the electrical conductivities of each layer due to their doping levels. Theoretically one may think of using a transistor in an inverted mode, i.e. the role of emitter junction and the collector junction are interchanged. Such an arrangement might not give as effective results as from its normal mode. So we write two current equations

one for the normal mode of operation, replacing  $\alpha$  by  $\alpha_N$  (current gain in normal operation):

$$I_C = -\alpha_N I_E - I_{E0} \left( e^{\frac{V_C}{V_T}} - 1 \right) \quad \text{----- (6.30)}$$

and other for inverted mode of operation, replacing  $\alpha$  by  $\alpha_I$  (current in inverted operation):

$$I_E = -\alpha_I I_C - I_{E0} \left( e^{\frac{V_E}{V_T}} - 1 \right) \quad \text{----- (6.31)}$$

In the inverted mode of operation  $I_E$  has been replaced by  $I_C$  and vice versa,  $V_C$  by  $V_E$  and  $I_{C0}$  by  $I_{E0}$ , as the role of emitter junction and collector junctions are interchanged.  $I_{E0}$  is the emitter junction reverse saturation current. These two equations are defined in figure (6.22) for PNP transistor. For either transistor (PNP or NPN), a positive value of current means that positive charge flows into the junction and a positive  $V_E$  or  $V_C$  means that the corresponding junction is in forward bias. A resistance  $r_{bb'}$ , known as base spreading resistance is supposed to be connected between a point on active base region  $B'$  and the base terminal  $B$  as shown in figure (6.22). The base spreading resistance is the d.c. ohmic resistance of the semiconductor material between the two points. The voltage drop across collector to base terminal differs from  $V_C$  by the potential drop across the base spreading resistance  $r_{bb'}$  i.e.  $V_{CB} = V_C - I_B r_{bb'}$

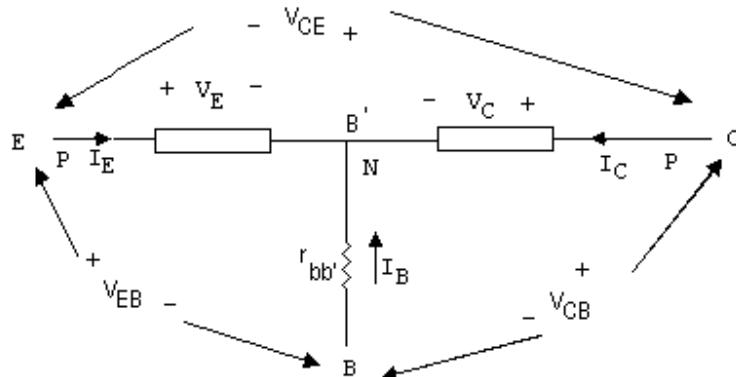


Fig. 6.22

J.J.Ebers and J.L.Moll of Bell Telephone in 1954 proposed a simple transistor model based on the equations (6.30 & 6.31). This model, known as Ebers – Moll model, is shown in figure (6.23a) for a PNP transistor and in figure (6.23b) for NPN transistor.

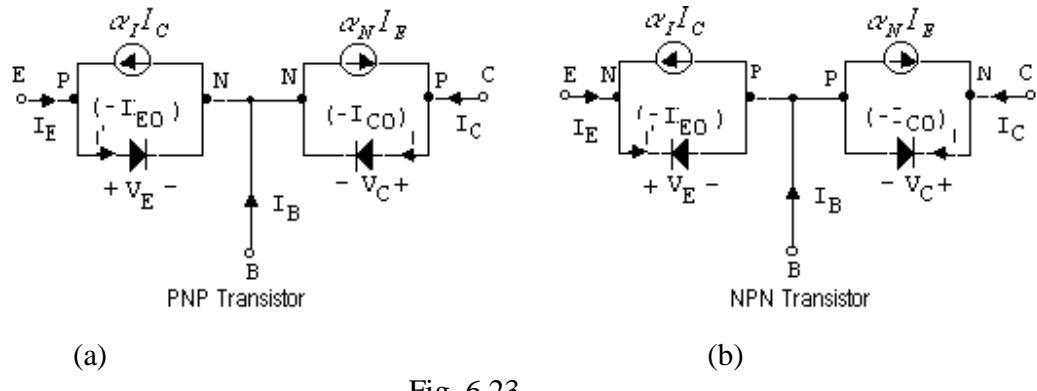


Fig. 6.23

This model consists of two diodes placed back to back with reverse saturation currents  $-I_{C0}$  and  $-I_{E0}$  and two dependent current sources shunting the diodes. For NPN transistor the direction of the diodes are reversed. The corresponding equations for NPN transistor will be same as given in equations (6.30 & 6.31), with the difference that  $V_E$  will be replaced by  $-V_E$  and  $V_C$  by  $-V_C$ , as  $V_E$  and  $V_C$  make the diodes in reverse bias. It should be noted that the base spreading resistance has been neglected from the figure (6.22) and thus eliminating the difference between  $I_{C0}$  and  $I_{CBO}$ .

The model which have been developed in this section are characterized by four parameters  $\alpha_N, \alpha_I, I_{C0}$  and  $I_{E0}$ . However, these parameters are not independent, but are related by the relation:

$$\alpha_N \cdot I_{E0} = \alpha_I \cdot I_{C0} \quad \text{----- (6.32)}$$

This reciprocity condition shows that at least three parameters out of these four parameters are sufficient to find to characterize the static V – I relationship of a transistor.

If the dependent sources from the figure (6.23) are eliminated, then transistor may be represented simply by two diodes placed back to back. This is possible if  $\alpha_N = \alpha_I = 0$ . The current gain  $\alpha$  will be zero if the base width is made much larger than the diffusion length of the injected minority charge carriers in the base region, all the minority carriers will recombine in the base and none will survive to reach the collector. In this condition the transistor action ceases. We therefore, get the conclusion that it is impossible to construct a transistor by simply connecting two diodes back to back.

**Example 6.8** Find the explicit expressions for  $I_C$  and  $I_E$  in terms of  $V_C$  and  $V_E$  from equations (6.30) and (6.31).

Solution: Rewriting the equations (6.30) and (6.31) in the following form:

$$I_C + \alpha_N I_E = -I_{C0} \left( e^{\frac{V_C}{V_T}} - 1 \right) \quad \text{----- (6.30)}$$

$$I_E + \alpha_I I_C = -I_{E0} \left( e^{\frac{V_E}{V_T}} - 1 \right) \quad \text{----- (6.31)}$$

Putting the value of  $I_E$  from equation (6.31) in equation (6.33) we get:

$$I_C + \alpha_N \left[ -\alpha_I I_C - I_{E0} \left( e^{\frac{V_E}{V_T}} - 1 \right) \right] = -I_{C0} \left( e^{\frac{V_C}{V_T}} - 1 \right)$$

or  $I_C (1 - \alpha_N \alpha_I) - \alpha_N I_{E0} \left( e^{\frac{V_E}{V_T}} - 1 \right) = -I_{C0} \left( e^{\frac{V_C}{V_T}} - 1 \right)$

or  $I_C = \frac{\alpha_N I_{E0} \left( e^{\frac{V_E}{V_T}} - 1 \right)}{(1 - \alpha_N \alpha_I)} - \frac{I_{C0} \left( e^{\frac{V_C}{V_T}} - 1 \right)}{(1 - \alpha_N \alpha_I)}$  ----- (6.35)

Similarly by putting the value of  $I_C$  from equation (6.30) in equation (6.34) we get:

$$I_E = \frac{\alpha_I I_{C0} \left( e^{\frac{V_C}{V_T}} - 1 \right)}{(1 - \alpha_N \alpha_I)} - \frac{I_{E0} \left( e^{\frac{V_E}{V_T}} - 1 \right)}{(1 - \alpha_N \alpha_I)} \quad \text{----- (6.36)}$$

These are the required expressions.

**Example 6.9 (i)** A transistor is operating in the cut-off region with both the emitter and collector junctions reversed biased by at least a few tenths of a volt. Prove that the currents are given by:

$$I_E = \frac{I_{E0} (1 - \alpha_N)}{1 - \alpha_N \alpha_I}$$

$$I_C = \frac{I_{C0} (1 - \alpha_I)}{1 - \alpha_N \alpha_I}$$

(ii) Prove that the emitter junction voltage required just to produce cut-off ( $I_E = 0$  and the collector is reversed biased) is:

$$V_E = V_T \ln(1 - \alpha_N)$$

Solution: (i) In the equations (6.35) and (6.36), the values of  $e^{(V_C/V_T)}$  and  $e^{(V_E/V_T)}$  may be put equal to zero as  $V_C$  and  $V_E$  are reversed biased and are larger than  $V_T$ . So we get :

$$I_E = \frac{-\alpha_I I_{C0}}{(1 - \alpha_N \alpha_I)} + \frac{I_{E0}}{(1 - \alpha_N \alpha_I)}$$

As  $\alpha_N I_{E0} = \alpha_I I_{C0}$ , above equation may be modified as :

$$= \frac{I_{E0} - \alpha_N I_{E0}}{(1 - \alpha_N \alpha_I)} = \frac{I_{E0} (1 - \alpha_N)}{(1 - \alpha_N \alpha_I)} \quad \text{----- (6.37)}$$

Similarly we may prove  $I_C = \frac{I_{C0} (1 - \alpha_I)}{1 - \alpha_N \alpha_I}$  ----- (6.38)

(ii) We know  $I_E = -\alpha_I I_C - I_{E0} \left( e^{\frac{V_E}{V_T}} - 1 \right)$

$$I_C = -\alpha_N I_E - I_{C0} \left( e^{\frac{V_C}{V_T}} - 1 \right)$$

Put  $I_E = 0$  and  $e^{(V_C/V_T)} \approx 0$  as  $|V_C| \gg 1$  in the above equations we get:

$$0 = -\alpha_I I_C - I_{E0} \left( e^{\frac{V_E}{V_T}} - 1 \right)$$

or  $\left( 1 - e^{\frac{V_E}{V_T}} \right) = \frac{\alpha_I I_C}{I_{E0}}$  ----- (6.39)

and  $I_C = I_{C0}$

$$\text{So } \left( 1 - e^{\frac{V_E}{V_T}} \right) = \frac{\alpha_I I_{C0}}{I_{E0}} = \alpha_N \quad \text{as } \alpha_N I_{E0} = \alpha_I I_{C0}$$

$$\text{or } V_E = V_T \ln(1 - \alpha_N) \quad \text{Proved.}$$

**Example 6.10** Find both collector and emitter current for a transistor when emitter and collector junctions are reversed biased. Given  $I_{C0} = 5 \mu A$ ,  $I_{E0} = 3.57 \mu A$  and  $\alpha_N = 0.98$ .

$$\text{Solution: We know } \alpha_N I_{E0} = \alpha_I I_{C0} \quad \text{so} \quad \alpha_I = \frac{\alpha_N I_{E0}}{I_{C0}} = \frac{(0.98)(3.57 \mu A)}{5 \mu A} = 0.7$$

From equation (6.35) we get:

$$I_C = \frac{I_{C0}(1 - \alpha_I)}{1 - \alpha_N \alpha_I} = \frac{(5 \mu A)(1 - 0.7)}{(1 - 0.98 \times 0.7)} = 0.48 \mu A$$

From equation (6.34) we get:

$$I_E = \frac{I_{E0}(1 - \alpha_N)}{(1 - \alpha_N \alpha_I)} = \frac{(3.57 \mu A)(1 - 0.98)}{(1 - 0.98 \times 0.7)} = 0.23 \mu A$$

**Example 6.11** Prove that the junction voltages in terms of the transistor currents are

$$\text{given by: } V_C = V_T \cdot \ln \left( 1 - \frac{I_C + \alpha_N I_E}{I_{C0}} \right)$$

$$V_E = V_T \cdot \ln \left( 1 - \frac{I_E + \alpha_I I_C}{I_{E0}} \right)$$

**Solution:** The transistor currents are given by:

$$I_C = -\alpha_N I_E - I_{C0} \left( e^{\frac{V_C}{V_T}} - 1 \right) \quad \text{----- (6.40)}$$

$$I_E = -\alpha_I I_C - I_{E0} \left( e^{\frac{V_E}{V_T}} - 1 \right) \quad \text{----- (6.41)}$$

$$\text{From equation (6.40) we have: } e^{\frac{V_C}{V_T}} = \left( 1 - \frac{I_C + \alpha_N I_E}{I_{C0}} \right)$$

$$\text{or } V_C = V_T \left( 1 - \frac{I_C + \alpha_N I_E}{I_{C0}} \right) \quad \text{----- (6.42)}$$

Similarly from equation (6.41), it may be proved that:

$$V_E = V_T \cdot \ln \left( 1 - \frac{I_E + \alpha_I I_C}{I_{E0}} \right) \quad \text{----- (6.43)}$$

**Example 6.12** (i) Show that the exact expression for the CE output characteristics of a PNP transistor is:

$$V_{CE} = V_T \cdot \ln \left( \frac{\alpha_I}{\alpha_N} \right) + V_T \cdot \ln \left( \frac{I_{C0} + \alpha_N I_B - I_C (1 - \alpha_N)}{I_{E0} + I_B + I_C (1 - \alpha_I)} \right)$$

(ii) If  $I_B \gg I_{E0}$  and  $I_B \gg I_{C0}/\alpha_N$  then

$$V_{CE} = V_T \cdot \ln \left( \frac{1 - \frac{1}{\beta_N} \cdot \frac{I_C}{I_B}}{\frac{1}{\alpha_I} + \frac{1}{\beta_I} \frac{I_C}{I_B}} \right)$$

$$\text{Where } \beta_I = \frac{\alpha_I}{1 - \alpha_I} \quad \text{and} \quad \beta_N = \frac{\alpha_N}{1 - \alpha_N}$$

**Solution:** (i) For the PNP transistor  $V_{CE} = V_C - V_E$ , putting the values of  $V_C$  and  $V_E$  from equations (6.42) & (6.43) we have:

$$\begin{aligned} V_{CE} &= V_C - V_E = V_T \left[ \ln \left( 1 - \frac{I_C + \alpha_N I_E}{I_{C0}} \right) - \ln \left( 1 - \frac{I_E + \alpha_I I_C}{I_{E0}} \right) \right] \\ &= V_T \ln \left[ \left( \frac{I_{C0} - I_C - \alpha_N I_E}{I_{E0} - I_E - \alpha_I I_C} \right) \left( \frac{I_{E0}}{I_{C0}} \right) \right] \quad \text{Further put } -I_E = I_B + I_C \\ &= V_T \ln \left[ \left( \frac{I_{C0} - I_C + \alpha_N I_C + \alpha_N I_B}{I_{E0} + I_B + I_C - \alpha_I I_C} \right) \left( \frac{I_{E0}}{I_{C0}} \right) \right] \\ &= V_T \ln \left[ \left( \frac{I_{C0} - (1 - \alpha_N) I_C + \alpha_N I_B}{I_{E0} + I_B + I_C (1 - \alpha_I)} \right) \left( \frac{I_{E0}}{I_{C0}} \right) \right] \quad \text{Put } \frac{I_{E0}}{I_{C0}} = \frac{\alpha_I}{\alpha_N} \end{aligned}$$

$$\text{We get } V_{CE} = V_T \cdot \ln \left( \frac{\alpha_I}{\alpha_N} \right) + V_T \cdot \ln \left( \frac{I_{C0} + \alpha_N I_B - I_C (1 - \alpha_N)}{I_{E0} + I_B + I_C (1 - \alpha_I)} \right) \quad \text{----- (6.44)}$$

(ii) Equation (6.41) may be rewritten as:

$$V_{CE} = V_T \ln \left[ \left( \frac{\left( \frac{I_{C0}}{\alpha_N} + I_B \right) \alpha_N - (1 - \alpha_N) I_C}{I_{E0} + I_B + I_C (1 - \alpha_I)} \right) \left( \frac{I_{E0}}{I_{C0}} \right) \right]$$

Neglecting  $\frac{I_{C0}}{\alpha_N}$  and  $I_{E0}$  as  $I_B \gg I_{E0}$  and  $I_B \gg I_{C0}/\alpha_N$  we get

$$V_{CE} = V_T \ln \left[ \left( \frac{I_B \alpha_N - (1 - \alpha_N) I_C}{I_B + I_C (1 - \alpha_I)} \right) \left( \frac{\alpha_I}{\alpha_N} \right) \right]$$

$$\text{or } V_{CE} = V_T \ln \left[ \frac{\left( 1 - \left\{ \frac{1-\alpha_N}{\alpha_N} \right\} \frac{I_C}{I_B} \right)}{\left( \frac{1}{\alpha_I} + \left\{ \frac{1-\alpha_I}{\alpha_I} \right\} \frac{I_C}{I_B} \right)} \left( \frac{\alpha_I \alpha_N}{\alpha_N \alpha_I} \right) \right]$$

Putting  $\beta_I = \frac{\alpha_I}{1-\alpha_I}$  and  $\beta_N = \frac{\alpha_N}{1-\alpha_N}$  we get:

$$V_{CE} = V_T \cdot \ln \left( \frac{1 - \frac{1}{\beta_N} \cdot \frac{I_C}{I_B}}{\frac{1}{\alpha_I} + \frac{1}{\beta_I} \frac{I_C}{I_B}} \right)$$

**6.11 Maximum Voltage Rating:** The limiting ratings given by the manufacturers for a transistor are maximum current, maximum voltage and maximum power dissipation. The power dissipation in the junctions of a transistor is important since excessive heating can either damage the transistor completely or alter its characteristics considerably. It has been observed that even if the rated dissipation of a transistor is not exceeded, there is an upper limit to the maximum allowable collector junction voltage. Since at high voltage, there is a possibility of voltage break down in the transistor. Two types of breakdowns are possible (i) Avalanche breakdown and (ii) Punch through.

**(i) Avalanche Breakdown:** This is a simple collector diode breakdown, which is due to the avalanche multiplication, similar to one that occurs in a junction diode. It is well known that the collector current increases sharply at a well defined breakdown voltage. For CE configuration, there is a strong influence of carrier multiplication and the breakdown voltage in this case is significantly smaller than CB configuration. Let  $BV_{CBO}$  is the breakdown voltage for CB configuration for the condition  $I_E = 0$  (with emitter is open); and  $BV_{CEO}$  is the breakdown voltage for CE configuration for the condition  $I_B = 0$  (with base is open). Let  $M$  is the factor by which the current entering the collector depletion region is multiplied, to obtain the collector  $I_C$  in each case. The current  $I_C$  is then given by the relation:

$$I_C = -(\alpha \cdot I_E + I_{C0})M \quad \text{----- (6.45)}$$

The factor  $M$  is given by empirical relation as:

$$M \cong \frac{1}{1 - (V_{CB}/BV_{CBO})^n} \quad \text{----- (6.46)}$$

The value of  $n$  is found to be in the range of about 2 to 10 to all the transistors.

From the equation (6.45), it is clear that in case of CB if  $I_E = 0$ , then  $I_C$  is simply  $-MI_{C0}$ , which defines the breakdown of a simple junction. In CE configuration the situation is somewhat complicated. If  $I_B = 0$  then  $I_C$  will be equal to  $I_E$  and thus equation (6.45) becomes:

$$I_c = -\frac{MI_{C_0}}{(1 - M\alpha)} \quad \text{----- (6.47)}$$

It is clear from the equation (6.47) that the collector current increases indefinitely when  $M\alpha$  approaches unity. Since  $\alpha$  is close to unity in most transistors,  $M$  need only be slightly greater than unity. This equation then approaches to breakdown. Avalanche multiplication thus dominates the current in a CE transistor well below the breakdown voltage of the collector junction in CB configuration.

**(ii) Punch through:** The second breakdown that usually takes place in the transistor is known as Punch through or Reach through. This phenomenon occurs because of Early Effect. As per this effect when the reverse bias on the collector junction is increased far enough, it is possible to decrease the effective base width  $W_b$  to the extent that the collector depletion region essentially fills the entire base region (fig. 6.24). That is the effective base width is zero. In this punch through condition holes are swept directly from the emitter region to the collector, and the transistor action is lost. Punch through is a breakdown effect which is generally avoided in the circuit design.

The punch through is controlled by the basic transistor design parameters such as base conductivity and base width and not by the circuit configuration so it takes place at a fixed collector base voltage. However, the avalanche multiplication not only depends on the collector voltage but also upon the circuit in which it is used. In a particular transistor, the maximum allowable voltage limit is determined by punch through or the avalanche breakdown, whichever occurs earlier.

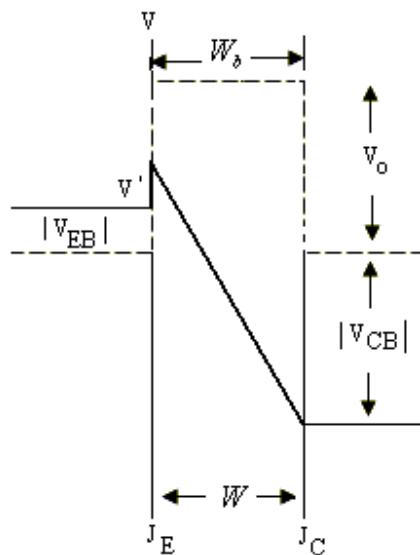
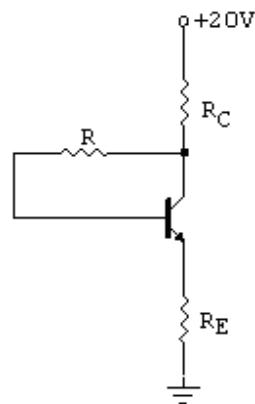


Fig. 6.24

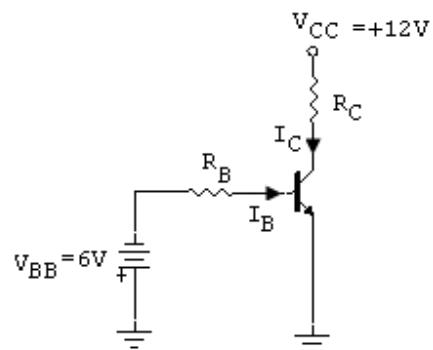
**Problems:**

1. Explain Base – width modulation (The Early Effect) with the aid of plot of potential and minority carrier concentration in the base region.
2. Sketch the output static characteristic curves of a PNP transistor in CB configuration. Explain the shapes of these curves qualitatively in active, cut-off and saturation region.
3. Sketch the input static characteristic curves of a PNP transistor in CB configuration. Explain the shapes of these curves qualitatively.
4. Draw the output static characteristic curves of a PNP transistor in CE configuration. Explain the shapes of the curves qualitatively in active, cut-off and saturation region.
5. Draw the input static characteristic curves of a PNP transistor in CE configuration. Explain the shapes of these curves qualitatively.
6. Discuss the Early Effect with its three consequences.
7. For a PNP transistor biased in the active region, plot the variations in potential and minority carrier concentration in each emitter, base and collector region. Explain the shapes of these plots.
8. Write the Ebers and Moll equations. Draw the circuit model which satisfies these equations.
9. Draw the Ebers and Moll model of a transistor. Explain a transistor can not be represented by two diodes connected back to back.
10. Discuss two possible sources of break down in a transistor as the collector to emitter voltage is increased.
11. Discuss maximum voltage ratings of a transistor.
12. Prove that the transistor can be used as an amplifier.
13. Discuss qualitatively different current components in a PNP transistor. Deduce the equation  $I_C = -\alpha I_E + I_{C0} \left( 1 - e^{\frac{V_C}{V_T}} \right)$ , where symbols have their usual meanings.
14. Define the current gain  $\alpha$  and  $\beta$ . Derive the relation between them.
15. Discuss the phenomenon of punch trough and reach through in a transistor.
16. Define the following regions in a transistor (a) active (b) saturation and (c) cut-off.
17. Discuss the variations in potential and minority carrier concentrations in each section of open circuited symmetrical PNP transistor.
18. Discuss the different current components in a PNP transistor. Deduce an expression for the collector current  $I_C$ . Define each symbol in this equation. Finally deduce the generalized expression for  $I_C$  so that it is valid even if the transistor is not operating in its active region.
19. Define the three current gain  $\beta$ ,  $\beta_{d.c.}$  ( $h_{FE}$ ), and  $\beta'$  ( $h_{fe}$ ) in CE transistor. Derive the relation between  $h_{FE}$  and  $h_{fe}$ .
20. Find the value of resistance  $R$  in the circuit given below in which Si transistor with  $\beta = 49$  is used.  $V_{CC} = 20$  V,  $V_{CE} = 5.8$  V,  $R_E = 0.2$  K $\Omega$ ,  $R_C = 8.2$  K $\Omega$ . Neglect reverse saturation current. (Ans. 159.4 K $\Omega$ )



21. Find the values of  $R_B$  and  $R_C$  in the circuit given below, so that collector current of 12mA flows in the Si transistor with  $\beta = 80$ .  $V_{CE} = 4$  V. Neglect reverse saturation current.

(Ans.  $667\Omega$ ,  $35K\Omega$ )



# 7

## The Transistors at Low Frequencies

In the preceding chapter the static characteristics of a transistor have been discussed. The use of transistor as amplifier will be discussed in this chapter. Transistor can be used in large signal or small signal operation. The graphical approach may be studied for the large signal behaviour. However, for small signal, the transistor is operated in the active region. Thus small signal linear model of the transistor will be derived in the active region for the analysis of the transistor behaviour. The  $h$  – parameter model of the transistor is generally used to characterise a transistor which can further be used easily to explain the amplifier characteristics in CE, CB and CC configuration.

**7.1 Low Frequency  $h$  – Parameter Model of a Transistor:** There are three modes of transistor namely CE, CB and CC configurations. In all three configurations one terminal is assumed as common between input and output terminals. One pair of terminal is used as the input port and other pair of terminals as output port. So any transistor configuration can be represented by a two port network. In CE configuration base and emitter terminals are treated as input port and collector & emitter terminals as the output port. In common base configuration emitter & base are known as the input port and collector & base are known as the output port. In common collector configuration input port consists of base and collector; and output port is emitter and collector.

We consider the common emitter configuration since it is most commonly used amplifier. In figure (7.1a) the transistor in common emitter configuration is shown with their terminal variables. We choose  $i_b$  and  $v_{ce}$  as independent variables and  $v_{be}$  and  $i_c$  as the dependent variables. We may write the  $h$  – parameter equations as discussed in section 2.3.

$$v_{be} = h_{11} i_b + h_{12} v_{ce} \quad \text{----- (7.1)}$$

$$i_c = h_{21} i_b + h_{22} v_{ce} \quad \text{----- (7.2)}$$

We define:

$h_{11} = (v_{be}/i_b) \Big|_{v_{ce}=0}$  as the input resistance with output shorted, it is represented by  $h_{ie}$

$h_{12} = (v_{be}/v_{ce}) \Big|_{i_b=0}$  as the reverse transfer voltage ratio with input open, it is represented by  $h_{re}$ .

$h_{21} = (i_c/i_b) \Big|_{v_{ce}=0}$  as the forward transfer current ratio with output shorted, it is represented by  $h_{fe}$ .

$h_{22} = (i_c/v_{ce}) \Big|_{i_b=0}$  as the output conductance with input open, it is represented by  $h_{oe}$ .

In all these parameters the subscript  $e$  is used for common emitter configuration. For common base or common collector configuration the subscript  $e$  will be replaced with  $b$  or  $c$  respectively.

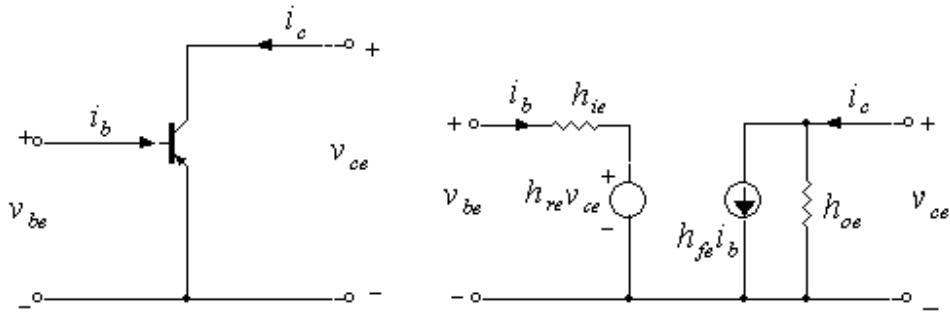


Fig. 7.1a

Fig. 7.1b

Thus the common emitter  $h$  – parameter equations in the form of the traditional symbols are given as:

$$v_{be} = h_{ie} i_b + h_{re} v_{ce} \quad \text{----- (7.3)}$$

$$i_c = h_{fe} i_b + h_{oe} v_{ce} \quad \text{----- (7.4)}$$

The equivalent circuit for these two equations may be drawn as shown in figure (7.1b), which can be verified by applying KVL to the input circuit and KCL to the output circuit. Thus the circuit of figure (7.1b) forms the model of the transistor which is known as  $h$  – Parameter Model (or hybrid model) of a Transistor in common emitter configuration.

The  $h$  – parameter model of a transistor in CB configuration is shown in figure (7.2). The terminal variables are chosen properly and  $h$  – parameters have the suffix  $b$  in place of  $e$ . The  $h$  – parameter equations in this configuration may be written as:

$$v_{eb} = h_{ib} i_e + h_{rb} v_{cb} \quad \text{----- (7.5)}$$

$$i_c = h_{fb} i_e + h_{ob} v_{cb} \quad \text{----- (7.6)}$$

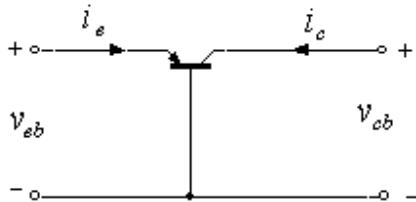


Fig. 7.2a

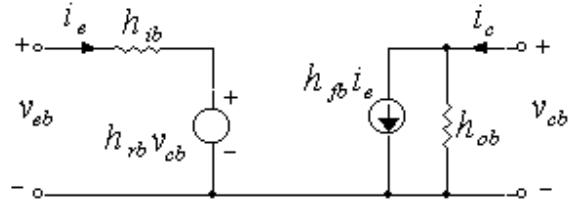


Fig. 7.2b

Similarly, h – parameter equations in CC configuration may be given below and its equivalent model is shown in figure (7.3)

$$v_{bc} = h_{ic} i_b + h_{rc} v_{ec} \quad \text{----- (7.7)}$$

$$i_e = h_{fc} i_b + h_{oc} v_{ec} \quad \text{----- (7.8)}$$

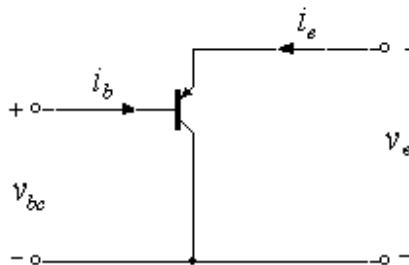


Fig. 7.3a

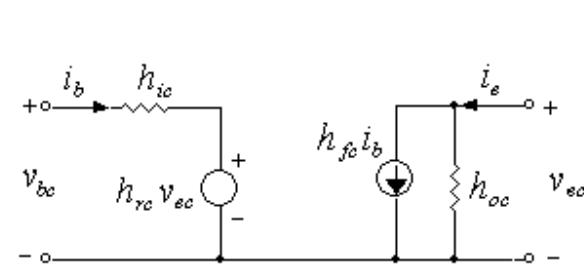


Fig. 7.3b

The Hybrid models and the equations discussed above are valid for NPN as well as for PNP transistors.

**7.2 Determination of h – parameters:** Although the  $h$  – parameters are directly measured in practice with suitable circuit arrangement, but these parameters can also be estimated from the static characteristics of the transistor in any configuration. Figures (7.4a) & (7.4b) show the output and input characteristics respectively of an NPN transistor in CE configuration. In the output characteristic we choose the operating point Q for an ideal current bias flowing in the base and ideal collector to emitter voltage. The point P in the input characteristic corresponds to the values of base current and  $V_{BE}$  for a particular  $V_{CE}$ . Considering two points  $P_1$  and  $P_2$  lying in the horizontal line (base current is constant), we find the difference  $\Delta V_{BE}$  as ( $V_{BE}$ , at  $P_2$  –  $V_{BE}$ , at  $P_1$ ) and the difference  $\Delta V_{CE}$  corresponding to these two points in the input characteristics. The ratio of  $\Delta V_{BE}$  and  $\Delta V_{CE}$  will be the estimate of  $h_{re}$ . On the curve of given  $V_{CE}$  (the curve on which the

point  $P$  lies) the two more points A and B are chosen, the ratio of  $\Delta V_{BE}$  and  $\Delta I_B$  at these two points gives  $h_{ie}$ . On the output characteristics of figure (7.4a) two points  $Q_1$  and  $Q_2$  are chosen for the fixed value of  $V_{CE}$ . The ratio of  $\Delta I_C$  and  $\Delta I_B$ , corresponding to these two points gives  $h_{fe}$ . The ratio of  $\Delta I_C$  and  $\Delta V_{CE}$  on the curve of fixed  $I_B$  (the curve on which the point Q lies) will give the estimate of  $h_{oe}$ .

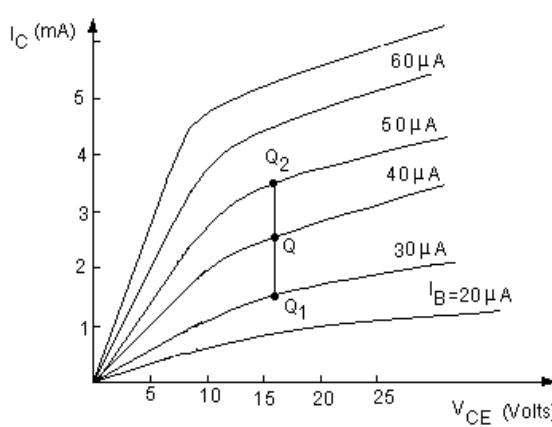


Fig. 7.4(a)

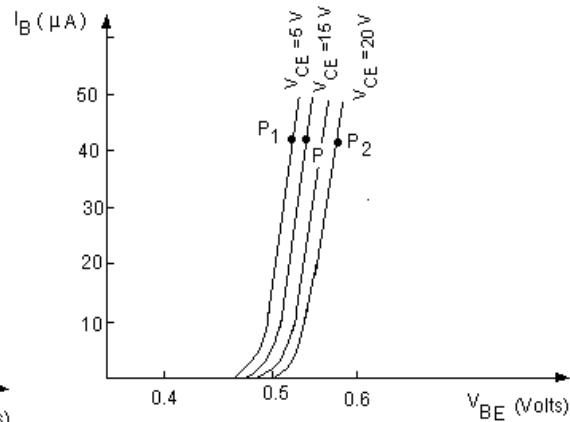


Fig. 7.4(b)

The method described above for the determination of  $h$  – parameters in CE configuration may also be used for evaluating these parameters in CB and CC configuration using their corresponding static characteristics.

**7.3 Conversion of  $h$  – Parameters in Three Configurations:** Sometimes  $h$  – parameters in one configuration is given and we are required to use the transistor in other configuration, so it becomes necessary to have the parameters in other configuration. For this one has to transform the parameters from one configuration to other configuration. Procedure for conversion of  $h$  – parameters from one configuration to other configuration is given as follows:

- Step 1: Write the set of  $h$  – parameter equations in the given configuration.
- Step 2: Draw the circuit model in the given configuration.
- Step 3: Write the set of  $h$  – parameter equations in the required configuration.
- Step 4: Redraw the circuit model in the required configuration.
- Step 5: Using the circuit model obtained in step 4, we write some possible equations. By doing some manipulation in these equations, a set of two equations in the formats of required configuration is obtained.
- Step 6: Comparing the equations (in step 5) with the  $h$  – parameter equations in the required configuration (in step 3), the required  $h$  – parameters are obtained in terms of the parameters of given configuration.

**Examples 7.1** Convert the CB  $h$  – parameters in to CC  $h$  – parameters.

Solution: We write  $h$  – parameter equations in CB configuration as:

$$v_{eb} = h_{ib} i_e + h_{rb} v_{cb} \quad \text{----- (7.9)}$$

$$i_c = h_{fb} i_e + h_{ob} v_{cb} \quad \text{----- (7.10)}$$

We draw the  $h$  – parameter model in CB configuration (Fig. 7.5):

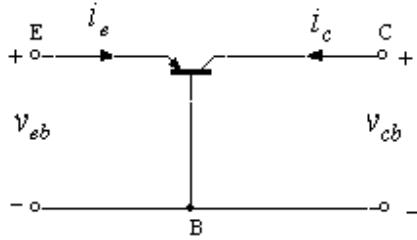


Fig. 7.5a

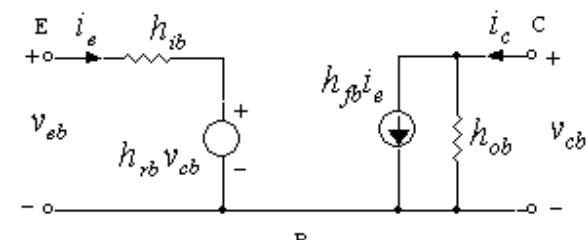


Fig. 7.5b

We write  $h$  – parameter equations in CC configuration as:

$$v_{bc} = h_{ic} i_b + h_{rc} v_{ec} \quad \text{----- (7.11)}$$

$$i_e = h_{fc} i_b + h_{oc} v_{ec} \quad \text{----- (7.12)}$$

We redraw circuit model of fig. 7.5 in the CC configuration as (Fig. 7.6):

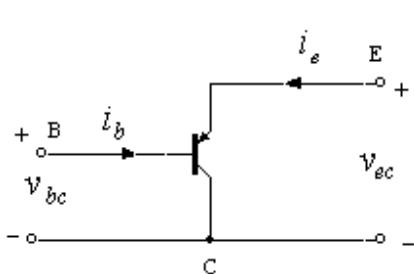


Fig. 7.6a

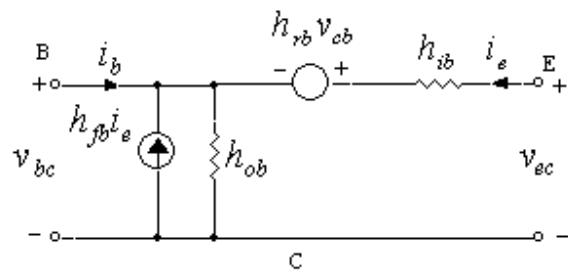


Fig. 7.6b

From the figures (7.6 b) we get the following equations:

$$i_b + h_{fb} i_e + i_e - h_{ob} v_{bc} = 0$$

$$\text{or} \quad i_b + (1 + h_{fb}) i_e - h_{ob} v_{bc} = 0 \quad \text{----- (7.13)}$$

$$v_{ec} = h_{ib} i_e + h_{rb} v_{cb} + v_{bc}$$

$$\text{or} \quad v_{ec} = h_{ib} i_e + (1 - h_{rb}) v_{bc} \quad \text{----- (7.14)}$$

From equation (7.13) we get the value of  $i_e$  as:

$$i_e = \frac{h_{ob} v_{bc}}{(1 + h_{fb})} - \frac{i_b}{(1 + h_{fb})} \quad \text{----- (7.15)}$$

From equations (7.14) & (7.15) we get:

$$\begin{aligned} v_{ec} &= v_{bc} (1 - h_{rb}) + h_{ib} \left( \frac{h_{ob} v_{bc}}{(1 + h_{fb})} - \frac{i_b}{(1 + h_{fb})} \right) \\ \text{or } v_{bc} &= \frac{h_{ib}}{[h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})]} i_b + \frac{(1 + h_{fb})}{[h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})]} v_{ec} \end{aligned} \quad \text{----- (7.17)}$$

Putting the value of  $v_{bc}$  from equation (7.17) in equation (7.15) and doing some manipulation we get:

$$i_e = \frac{-(1 - h_{rb})}{[h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})]} i_b + \frac{h_{ob}}{[h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})]} v_{ec} \quad \text{----- (7.18)}$$

These are the two equations in the required configuration, the parameters in this configuration may be obtained by comparing these two equations with equations (7.11 & 7.12) we get:

$$h_{ic} = \frac{h_{ib}}{[h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})]} \quad h_{rc} = \frac{(1 + h_{fb})}{[h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})]}$$

$$h_{fc} = \frac{-(1 - h_{rb})}{[h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})]} \quad h_{oc} = \frac{h_{ob}}{[h_{ib} h_{ob} + (1 - h_{rb})(1 + h_{fb})]}$$

**Example 7.2** Find the CC  $h$  – parameters in terms of CE  $h$  – parameters.

Solution: We write  $h$  – parameter equations in CE configuration as:

$$v_{be} = h_{ie} i_b + h_{re} v_{ce} \quad \text{----- (7.19)}$$

$$i_c = h_{fe} i_b + h_{oe} v_{ce} \quad \text{----- (7.20)}$$

We draw the  $h$  – parameter model in CE configuration:

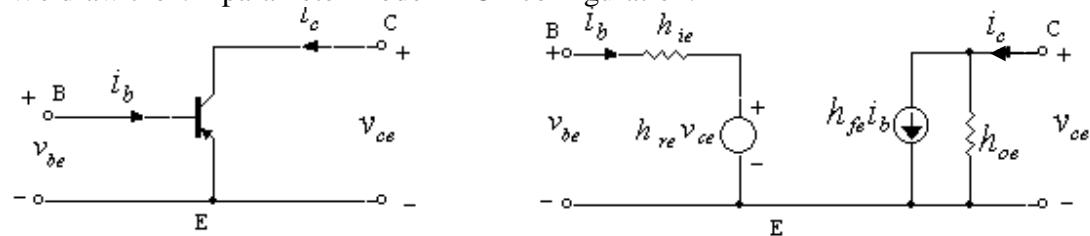


Fig. 7.7a

Fig. 7.7b

We write  $h$  – parameter equations in CC configuration as:

$$v_{bc} = h_{ic} i_b + h_{rc} v_{ec} \quad \text{----- (7.21)}$$

$$i_e = h_{fc} i_b + h_{oc} v_{ec} \quad \text{----- (7.22)}$$

We redraw circuit model of fig. 7.7 in the CC configuration as:

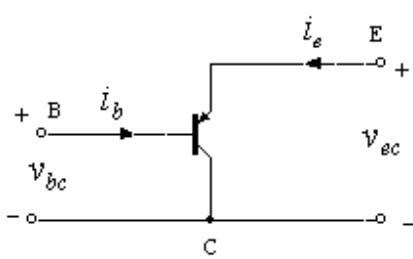


Fig. 7.8a

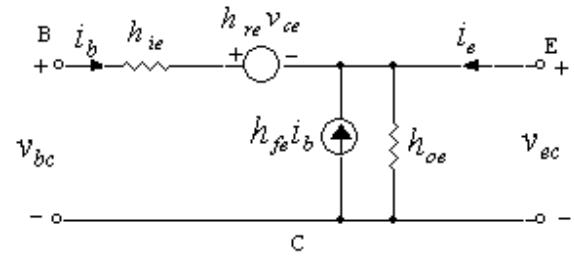


Fig. 7.8b

From the figures (7.8 b) we get the following equations:

$$v_{bc} = h_{ie} i_b + h_{re} v_{ce} + v_{ec}$$

or  $v_{bc} = h_{ie} i_b + v_{ec} (1 - h_{re}) \quad \text{----- (7.23)}$

$$i_b + h_{fe} i_b + i_e - h_{oe} v_{ec} = 0$$

or  $(1 + h_{fe}) i_b + i_e - h_{oe} v_{ec} = 0 \quad \text{----- (7.24)}$

Comparing the equations (7.23) & (7.24) with equations (7.21) & (7.22) respectively, we get CC  $h$  – parameters in CE parameters.

$$h_{ic} = h_{ie}$$

$$h_{rc} = (1 - h_{re})$$

$$h_{fc} = -(1 + h_{fe})$$

$$h_{oc} = h_{oe}$$

**Examples 7.3** Convert the CC  $h$  – parameters in to CB  $h$  – parameters.

Solution: We write  $h$  – parameter equations in CC configuration as:

$$v_{bc} = h_{ic} i_b + h_{rc} v_{ec} \quad \text{----- (7.25)}$$

$$i_e = h_{fc} i_b + h_{oc} v_{ec} \quad \text{----- (7.26)}$$

We draw the  $h$  – parameter model in CC configuration:

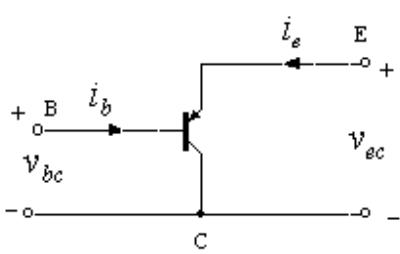


Fig. 7.9a

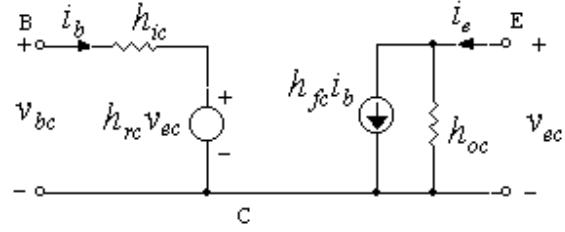


Fig. 7.9b

We write  $h$ -parameter equations in CB configuration as:

$$v_{eb} = h_{ib} i_e + h_{rb} v_{cb} \quad \text{----- (7.27)}$$

$$i_c = h_{fb} i_e + h_{ob} v_{cb} \quad \text{----- (7.28)}$$

We redraw circuit model of fig. 7.9 in the CB configuration as:

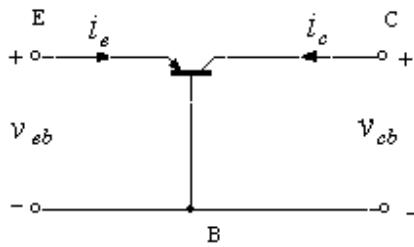


Fig. 7.10a

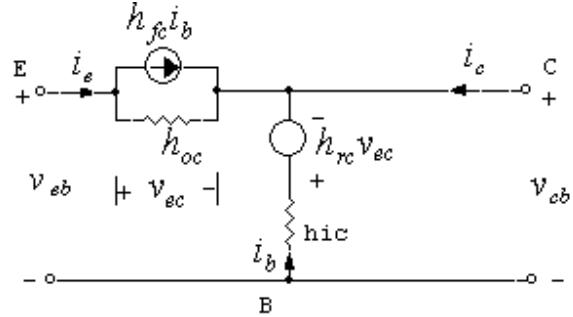


Fig. 7.10b

From the figures (7.10 b) we get the following equations:

$$v_{eb} = v_{ec} - h_{rc} v_{ec} - h_{ic} i_b$$

$$\text{or } v_{eb} = v_{ec} (1 - h_{rc}) - h_{ic} i_b \quad \text{----- (7.29)}$$

$$i_e = h_{fc} i_b + h_{oc} v_{ec} \quad \text{----- (7.30)}$$

$$v_{eb} = v_{ec} + v_{cb} \quad \text{----- (7.31)}$$

$$i_e + i_b + i_c = 0 \quad \text{----- (7.32)}$$

Eliminate the values of  $i_b$  and  $v_{ec}$  from equation (7.29) using equations (7.30) & (7.31) we get:

$$v_{eb} = \frac{h_{ic}}{[h_{ic} h_{oc} - h_{rc} h_{fc}]} i_e + \frac{(1 - h_{rc}) h_{fc} + h_{ic} h_{oc}}{[h_{ic} h_{oc} - h_{rc} h_{fc}]} v_{cb} \quad \text{----- (7.33)}$$

Using the equations (7.30) to (7.33) and doing some manipulations we get:

$$i_c = \frac{h_{rc} (1 + h_{fc}) - h_{ic} h_{oc}}{[h_{ic} h_{oc} - h_{rc} h_{fc}]} i_e + \frac{h_{oc}}{[h_{ic} h_{oc} - h_{rc} h_{fc}]} v_{cb} \quad \text{----- (7.34)}$$

Comparing the equations (7.33) & (7.34) with equations (7.27) & (7.28) respectively, we get CB  $h$  – parameters in CC parameters.

$$h_{ib} = \frac{h_{ic}}{[h_{ic}h_{oc} - h_{rc}h_{fc}]} \quad h_{rb} = \frac{(1 - h_{rc})h_{fc} + h_{ic}h_{oc}}{[h_{ic}h_{oc} - h_{rc}h_{fc}]} \\ h_{fb} = \frac{h_{rc}(1 + h_{fe}) - h_{ic}h_{oc}}{[h_{ic}h_{oc} - h_{rc}h_{fc}]} \quad h_{ob} = \frac{h_{oc}}{[h_{ic}h_{oc} - h_{rc}h_{fc}]}$$

Conversions for  $h$  – parameters in three configurations are given in table 7.1.

Table 7.1

CB $h$ – parameters	
In terms of CE parameters	In terms of CC parameters
$h_{ib} = \frac{h_{ie}}{(1 + h_{fe})(1 - h_{re}) + h_{ie}h_{oe}}$ $h_{rb} = \frac{h_{ie}h_{oe} - h_{re}(1 + h_{fe})}{(1 + h_{fe})(1 - h_{re}) + h_{ie}h_{oe}}$ $h_{fb} = \frac{-h_{fe}(1 - h_{re}) - h_{ie}h_{oe}}{(1 + h_{fe})(1 - h_{re}) + h_{ie}h_{oe}}$ $h_{ob} = \frac{h_{oe}}{(1 + h_{fe})(1 - h_{re}) + h_{ie}h_{oe}}$	$h_{ib} = \frac{h_{ic}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$ $h_{rb} = \frac{h_{fc}(1 - h_{rc}) + h_{ic}h_{oc}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$ $h_{fb} = \frac{h_{rc}(1 + h_{fe}) - h_{ic}h_{oc}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$ $h_{ob} = \frac{h_{oc}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$
CE $h$ – parameters	
In terms of CB parameters	In terms of CC parameters
$h_{ie} = \frac{h_{ib}}{(1 + h_{fb})(1 - h_{rb}) + h_{ib}h_{ob}}$ $h_{re} = \frac{h_{ib}h_{ob} - h_{rb}(1 + h_{fb})}{(1 + h_{fb})(1 - h_{rb}) + h_{ib}h_{ob}}$ $h_{fe} = \frac{-h_{fb}(1 - h_{rb}) - h_{ib}h_{ob}}{(1 + h_{fb})(1 - h_{rb}) + h_{ib}h_{ob}}$ $h_{oe} = \frac{h_{ob}}{(1 + h_{fb})(1 - h_{rb}) + h_{ib}h_{ob}}$	$h_{ie} = h_{ic}$ $h_{re} = (1 - h_{rc})$ $h_{fe} = -(1 + h_{fc})$ $h_{oe} = h_{oc}$
CC $h$ – parameters	
In terms of CB parameters	In terms of CE parameters
$h_{ic} = \frac{h_{ib}}{(1 + h_{fb})(1 - h_{rb}) + h_{ib}h_{ob}}$	$h_{ic} = h_{ie}$

$h_{rc} = \frac{1 + h_{fb}}{(1 + h_{fb})(1 - h_{rb}) + h_{ib}h_{ob}}$ $h_{fc} = \frac{-(1 - h_{rb})}{(1 + h_{fb})(1 - h_{rb}) + h_{ib}h_{ob}}$ $h_{oc} = \frac{h_{ob}}{(1 + h_{fb})(1 - h_{rb}) + h_{ib}h_{ob}}$	$h_{rc} = (1 - h_{re})$ $h_{fc} = -(1 + h_{fe})$ $h_{oc} = h_{oe}$
--	--

The  $h$  – parameters of actual transistors are such that some approximation will greatly simplify the conversion formulas with reasonable accuracy. Generally following approximations are made.

$$h_i h_o \ll 1 \quad h_{rc} \approx 1 \quad h_{rb} \ll 1 \quad \text{and} \quad h_{re} \ll 1$$

Approximate formulas for the three configurations are given in table 7.2.

Table 7.2

CB $h$ – parameters	
In terms of CE parameters	In terms of CC parameters
$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$ $h_{rb} = \frac{h_{ie}h_{oe}}{1 + h_{fe}} - h_{re}$ $h_{fb} = \frac{-h_{fe}}{1 + h_{fe}}$ $h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$	$h_{ib} = -\frac{h_{ic}}{h_{fc}}$ $h_{rb} = h_{rc} - \frac{h_{ic}h_{oc}}{h_{fc}} - 1$ $h_{fb} = -\frac{1 + h_{fc}}{h_{fc}}$ $h_{ob} = -\frac{h_{oc}}{h_{fc}}$
CE $h$ – parameters	
In terms of CB parameters	In terms of CC parameters
$h_{ie} = \frac{h_{ib}}{1 + h_{fb}}$ $h_{re} = \frac{h_{ib}h_{ob}}{1 + h_{fb}} - h_{ib}$ $h_{fe} = \frac{-h_{fb}}{1 + h_{fb}}$ $h_{oe} = \frac{h_{ob}}{1 + h_{fb}}$	$h_{ie} = h_{ic}$ $h_{re} = (1 - h_{rc})$ $h_{fe} = -(1 + h_{fc})$ $h_{oe} = h_{oc}$
CC $h$ – parameters	
In terms of CB parameters	In terms of CE parameters

$h_{ic} = \frac{h_{ib}}{1 + h_{fb}}$ $h_{rc} = 1$ $h_{fc} = \frac{-1}{1 + h_{fb}}$ $h_{oc} = \frac{h_{ob}}{1 + h_{fb}}$	$h_{ie} = h_{ic}$ $h_{rc} = 1$ $h_{fc} = -(1 + h_{fe})$ $h_{oc} = h_{oe}$
---	---

**7.4 An Analysis of Transistor Amplifier:** To analyse the transistor amplifier, we consider a transistor in any of the three configurations. To the input of the amplifier, a signal source  $V_s$  having  $R_s$  as the source resistance is applied, and a load impedance  $Z_L$  is connected to its output. The transistor is however biased properly. The amplifier is replaced by a two port network (active) as shown in figure (7.11) without bothering about in which mode the transistor is used. The quantities of our interest, regarding the transistor amplifier are current gain  $A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$ , voltage gain  $A_V = \frac{V_2}{V_1}$ , input impedance  $Z_I = \frac{V_1}{I_1}$  and output impedance  $Z_O = \frac{V_2}{I_2}$ . To find these quantities we represent the transistor into its equivalent small signal hybrid model as shown in figure (7.12). Here we are considering the general case of the amplifier, so no second suffix to

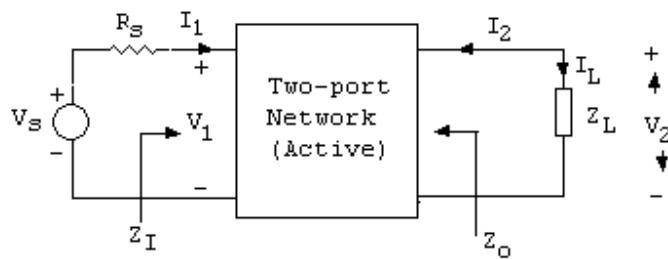


Fig. 7.11

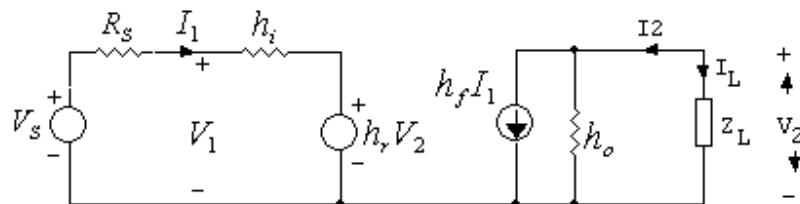


Fig. 7.12

the  $h$  – parameters are introduced. Later on, we will introduce the suffix e, b, or c for CE, CB and CC configurations respectively, as the case may be. We shall now calculate these quantities as given below.

**(i) Current Gain  $A_I$ :** The current gain  $A_I$  is defined as the ratio of output current to the input current as  $A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$

From the circuit of figure (7.12), we have :

$$I_2 = h_f I_1 + h_o V_2 \quad \text{----- (7.35)}$$

Putting  $V_2 = I_L Z_L = -I_2 Z_L$  in the above equation we get:

$$I_2 = h_f I_1 - h_o I_2 Z_L$$

or

$$I_2 (1 + h_o Z_L) = h_f I_1$$

or

$$A_I = \frac{-I_2}{I_1} = \frac{-h_f}{(1 + h_o Z_L)} \quad \text{----- (7.36)}$$

Note that the current gain of the amplifier depends on the  $h$  – parameters of the transistor as well as on the load impedance  $Z_L$ . The maximum current gain of the amplifier is  $|h_f|$  which is obtained when  $h_o Z_L \rightarrow 0$ .

**(ii) Input Impedance  $Z_I$ :** The impedance looking into the input terminals of the amplifier is known as input impedance  $Z_I = \frac{V_1}{I_1}$ .

From the input circuit of figure (7.12), we have

$$V_1 = h_i I_1 + h_r V_2$$

$$\text{or} \quad Z_I = \frac{V_1}{I_1} = \frac{(h_i I_1 + h_r V_2)}{I_1} = h_i + \frac{h_r V_2}{I_1}$$

Putting  $V_2 = -I_2 Z_L$  in the above equation we get:

$$Z_I = h_i - \frac{h_r I_2 Z_L}{I_1} = h_i + h_r A_I Z_L$$

Substituting the value of  $A_I$  from equation (7.36), we have

$$Z_I = h_i - \frac{h_r h_f Z_L}{(1 + h_o Z_L)} = h_i - \frac{h_f h_r}{(Y_L + h_o)} \quad \text{----- (7.37)}$$

Where  $Y_L = (1/Z_L)$ , is the load admittance. It is clear from the above equation that the input impedance is not only a function of  $h$  – parameters of the transistor but also depends on the load impedance.

**(iii) Voltage Gain  $A_V$ :** The voltage gain  $A_V$  is defined as  $A_V = \frac{V_2}{V_1}$  which is given by:

$$A_V = \frac{-I_2 Z_L}{V_1} = \frac{A_I Z_L}{Z_I} \quad \text{----- (7.38)}$$

**(iv) Output Impedance  $Z_o$ :** By definition the output impedance is  $Z_o = \frac{V_2}{I_2}$ , with source replaced by its internal resistance  $R_s$  and  $Z_L = \infty$ . From equation (7.17) we have the output admittance  $Y_o$

$$Y_o = \frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o \quad \text{----- (7.39)}$$

From figure (7.12), with  $V_s = 0$  we have

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$\text{or} \quad \frac{I_1}{V_2} = -\frac{h_r}{h_i + R_s} \quad \text{----- (7.40)}$$

Putting the value of  $\frac{I_1}{V_2}$  from equation (7.40) to equation (7.39), we get

$$Y_o = h_o - \frac{h_f h_r}{(h_i + R_s)} \quad \text{----- (7.41)}$$

Note that output impedance is a function of the source resistance in addition to the h – parameters of the transistor. Further if source resistance is resistive than the output admittance will be real (conductance). If the output impedance of the amplifier  $Z_L$  is included than output impedance will be parallel combination of  $Z_L$  and  $Z_o$ .

In addition to the formulas derived above, it is important to find the overall voltage gain and overall current gain also.

**(v) Overall Voltage Gain  $A_{vs}$ :** The overall voltage gain  $A_{vs}$ , taking into account the resistance  $R_s$  of the source is given by:

$$A_{vs} = \frac{V_2}{V_s} = \frac{V_2}{V_1} \cdot \frac{V_1}{V_s} = A_V \cdot \frac{V_1}{V_s}$$

From figure (7.12),

$$V_1 = \frac{V_s}{R_s + Z_I} \cdot Z_I$$

$$\text{Then} \quad A_{vs} = \frac{A_V}{R_s + Z_I} \cdot Z_I = \frac{A_I Z_L}{R_s + Z_I} \quad \text{----- (7.42)}$$

Note that if  $R_s = 0$ , then  $A_{vs} = A_V$ .

**(vi) Overall Current Gain  $A_{IS}$ :** If the input source is a current source  $I_S$  in parallel with the source resistance  $R_S$  (i.e. Norton's equivalent of the voltage source), then the overall current gain  $A_{IS}$  is given by:

$$A_{IS} = -\frac{I_2}{I_S} = \frac{-I_2}{I_1} \cdot \frac{I_1}{I_S} = A_I \frac{I_1}{I_S}$$

Using the Norton's equivalent of the voltage source  $V_S$  in the figure (7.12), we get:

$$I_1 = \frac{R_S}{R_S + Z_I} I_S$$

Then  $A_{IS} = \frac{A_I R_S}{R_S + Z_I}$

Note that if  $R_S = 0$ , then  $A_{IS} = A_I$ . Also we have

$$A_{VS} = \frac{A_{IS} Z_L}{R_S}$$

The formulas derived above are summarised in table 7.3.

Table 7.3

$A_I = \frac{-h_f}{(1+h_o Z_L)}$	$Y_o = h_o - \frac{h_f h_r}{(h_i + R_s)} = \frac{1}{Z_0}$
$Z_I = h_i + h_r A_I Z_L$	$A_{VS} = \frac{A_V}{R_S + Z_I} \cdot Z_I = \frac{A_I Z_L}{R_S + Z_I}$
$A_V = \frac{A_I Z_L}{Z_I}$	$A_{IS} = \frac{A_I R_S}{R_S + Z_I}$

Example 7.4 Prove for any single transistor amplifier

$$Z_I = \frac{h_i}{1 - h_r A_V}$$

Solution: We know  $Z_I = h_i + h_r A_I Z_L$  ----- (7.43)

and

$$A_V = \frac{A_I Z_L}{Z_I} \quad \text{----- (7.44)}$$

From the equations (7.43) & (7.44) we have:

$$Z_I = h_i + h_r A_V Z_I$$

$$Z_I (1 - A_V) = h_i$$

or

$$Z_I = \frac{h_i}{1 - h_r A_V} \quad \text{Proved}$$

**Example 7.5** Prove that the output admittance of the transistor may be given in the following form:

$$Y_o = h_o \left( \frac{R_s + Z_{I\infty}}{R_s + Z_{I0}} \right)$$

where  $Z_{I\infty} = Z_I$  for  $Z_L = \infty$  and  $Z_{I0} = Z_I$  for  $Z_L = 0$ .

**Solution:** We know that

$$Y_o = h_o - \frac{h_f h_r}{(h_i + R_s)} \quad \text{----- (7.45)}$$

$$Z_I = h_i + h_r A_I Z_L \quad \text{----- (7.46)}$$

$$A_I = \frac{-h_f}{(1 + h_o Z_L)} \quad \text{----- (7.47)}$$

From equations (7.46) & (7.47) have:

$$Z_I = h_i - \frac{h_f h_r Z_L}{(1 + h_o Z_L)} = h_i - \frac{h_f h_r}{(h_o + \frac{1}{Z_L})}$$

For  $Z_L = 0$   $Z_I = Z_{I0}$  so  $Z_I = h_i$

For  $Z_L = \infty$   $Z_I = Z_{I\infty}$  so  $Z_{I\infty} = h_i - \frac{h_f h_r}{h_o}$

$$\text{Now from eq. (7.45)} \quad Y_o = \frac{h_o(h_i + R_s) - h_f h_r}{(h_i + R_s)}$$

$$\text{or} \quad Y_o = \frac{h_o \left[ h_i + R_s - \frac{h_f h_r}{h_o} \right]}{(h_i + R_s)}$$

or

$$Y_o = h_o \left( \frac{R_s + Z_{I\infty}}{R_s + Z_{I0}} \right) \quad \text{proved}$$

Example 7.6 For the circuit shown in figure (7.13), verify that the modified  $h$  – parameters (indicated by  $\dot{h}$ ) are given by:

$$(i) \quad \dot{h}_{ie} \approx h_{ie} + \frac{(1 + h_{fe})R_e}{(1 + h_{oe}R_e)} \quad (ii) \quad \dot{h}_{re} = \frac{h_{re} + h_{oe}R_e}{(1 + h_{oe}R_e)}$$

$$(iii) \quad \dot{h}_{fe} = \frac{h_{fe} - h_{oe}R_e}{(1 + h_{oe}R_e)} \quad (iv) \quad \dot{h}_{oe} = \frac{h_{oe}}{(1 + h_{oe}R_e)}$$

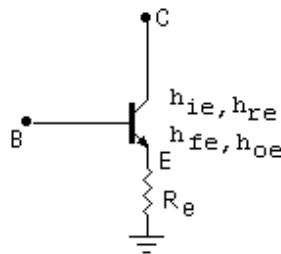


Fig. 7.13

Solution: The  $h$  – parameter model of the circuit is shown in figure (7.14)

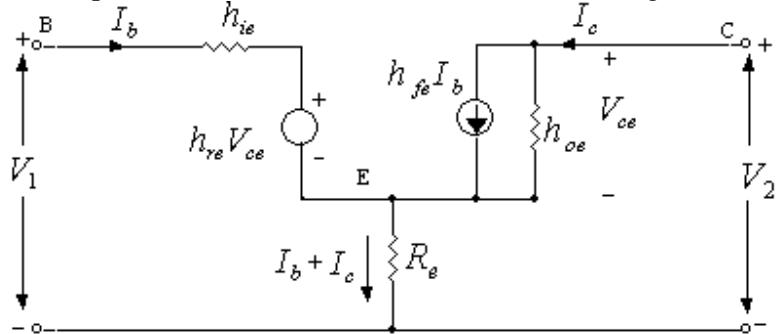


Fig. 7.14

The  $h$  – parameter equations of this network is given as :

$$V_1 = \dot{h}_{ie} I_b + \dot{h}_{re} V_2$$

$$I_C = \dot{h}_{fe} I_b + \dot{h}_{oe} V_2$$

where

$$\dot{h}_{ie} = \left. \frac{V_1}{I_b} \right|_{V_2=0} \quad \dot{h}_{re} = \left. \frac{V_1}{V_2} \right|_{I_b=0}$$

$$\dot{h}_{fe} = \left. \frac{I_c}{I_b} \right|_{V_2=0} \quad \dot{h}_{oe} = \left. \frac{I_c}{V_2} \right|_{I_b=0}$$

For  $\dot{h}_{fe} = \frac{I_c}{I_b} \Big|_{V_2=0}$

Applying the KVL & KCL to the input and output circuits we get:

$$V_1 = h_{ie} I_b + h_{re} V_{ce} + I_b R_e + I_c R_e \quad \text{----- (7.48)}$$

$$V_2 = V_{ce} + R_e (I_b + I_c) \quad \text{----- (7.49)}$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \quad \text{----- (7.50)}$$

From Eq. (7.50)  $V_{ce} = \frac{I_c - h_{fe} I_b}{h_{oe}}$  ----- (7.51)

Since  $V_2 = 0$

So eq. (7.49) reduces to

$$V_{ce} = -R_e (I_b + I_c) \quad \text{or} \quad I_c = -\frac{V_{ce} + R_e I_b}{R_e} \quad \text{----- (7.52)}$$

From eqs. (7.51) & (7.52) we have

$$\begin{aligned} \frac{I_c - h_{fe} I_b}{h_{oe}} &= -(I_b + I_c) R_e \\ \text{or} \quad I_c \left( \frac{1}{h_{oe}} + R_e \right) &= -I_b R_e + \frac{h_{fe} I_b}{h_{oe}} \\ \text{or} \quad \frac{I_c}{I_b} &= \frac{h_{fe} - R_e h_{oe}}{(1 + R_e h_{oe})} \\ \text{or} \quad \dot{h}_{fe} &= \frac{I_c}{I_b} = \frac{h_{fe} - R_e h_{oe}}{(1 + R_e h_{oe})} \end{aligned} \quad \text{----- (7.53)}$$

Note that part (iii) is proved.

For  $\dot{h}_{ie} = \frac{V_1}{I_b} \Big|_{V_2=0}$

From equations (7.48) & (7.53) we have:

$$\begin{aligned} V_1 &= h_{ie} I_b + h_{re} V_{ce} + I_b R_e + R_e \left( \frac{h_{fe} - R_e h_{oe}}{1 + R_e h_{oe}} \right) I_b \\ \text{or} \quad V_1 &= I_b \left( h_{ie} + R_e \left\{ \frac{1 + R_e h_{oe} + h_{fe} - R_e h_{oe}}{(1 + R_e h_{oe})} \right\} \right) + h_{re} V_{ce} \\ \text{or} \quad V_1 &= I_b \left( h_{ie} + R_e \left\{ \frac{1 + h_{fe}}{(1 + R_e h_{oe})} \right\} \right) + h_{re} V_{ce} \end{aligned}$$

Neglecting  $V_{ce}h_{re}$ , we have

$$V_1 \approx I_b \left( h_{ie} + R_e \left\{ \frac{1+h_{fe}}{(1+R_e h_{oe})} \right\} \right)$$

or  $\dot{h}_{ie} = \frac{V_1}{I_b} \approx \left( h_{ie} + R_e \left\{ \frac{1+h_{fe}}{(1+R_e h_{oe})} \right\} \right)$  ----- (7.54)

Note that part (i) is proved.

For  $\dot{h}_{re} = \frac{V_1}{V_2} \Big|_{I_b=0}$

Putting  $I_b = 0$  in Equations (7.48) to (7.50) we have:

$$V_1 = h_{re} V_{ce} + I_c R_e \quad \text{----- (7.55)}$$

$$V_2 = V_{ce} + R_e I_c \quad \text{----- (7.56)}$$

$$I_c = h_{oe} V_{ce} \quad \text{----- (7.57)}$$

From eqs. (7.55) to (7.57)

$$V_1 = h_{re} V_{ce} + R_e h_{oe} V_{ce}$$

$$V_1 = (h_{re} + R_e h_{oe}) V_{ce}$$

and  $V_2 = V_{ce} (1 + R_e h_{oe}) \quad \text{----- (7.58)}$

or  $\dot{h}_{re} = \frac{V_1}{V_2} = \frac{h_{re} + h_{oe} R_e}{(1 + h_{oe} R_e)} \quad \text{----- (7.59)}$

Note that part (ii) is proved.

For  $\dot{h}_{oe} = \frac{I_c}{V_2} \Big|_{I_b=0}$

From eqs. (7.57) & (7.55)

$$\dot{h}_{oe} = \frac{I_c}{V_2} = \frac{h_{oe}}{(1 + h_{oe} R_e)} \quad \text{----- (7.60)}$$

Part (iv) is proved.

**7.5 Comparison of Transistor Amplifier Configurations:** Typical values of  $h$ -parameters of a transistor in the three configurations are given in the Table 7.4. Using these values of  $h$ -parameters in the formulas given in table 7.4, the current gain, voltage gain, input impedances were calculated as functions of load impedances; and output impedance as the function of source resistance for the three configurations. The variations of current gain, voltage gain, input impedance and output impedance as functions of load impedance and source resistance are shown in figure 7.15.

Table 7.4

Parameter	Common Emitter CE	Common Base CB	Common Collector CC
$h_i$	$h_{ie} = 2600 \Omega$	$h_{ib} = 25.8 \Omega$	$h_{ic} = 2600 \Omega$
$h_f$	$h_{fe} = 100$	$h_{fb} = -0.99$	$h_{fc} = -101$
$h_r$	$h_{re} = 0.62 \times 10^{-4}$	$h_{rb} = 0.67 \times 10^{-4}$	$h_{rc} = 1$
$h_o$	$h_{oe} = 5 \mu\text{-mhos}$	$h_{ob} = 0.05 \mu\text{-mhos}$	$h_{oc} = 5 \mu\text{-mhos}$

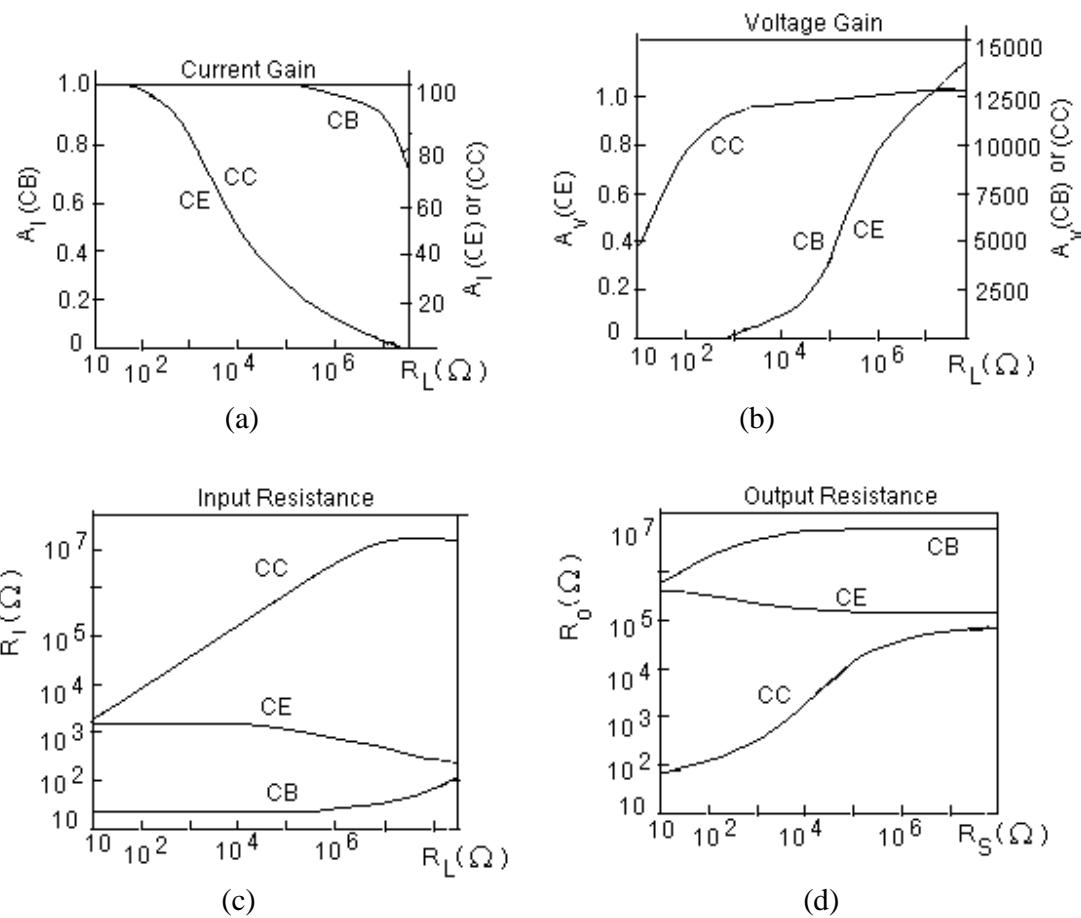


Fig. 7.15

On the careful study of these curves, the characteristics of the three configurations may be summarised as shown in table 7.5.

Table 7.5

Quantity	CB	CE	CC
Current gain ( $A_I$ )	$\approx 1$	High	High
Voltage gain ( $A_V$ )	High	High	$\approx 1$

Input impedance ( $Z_i$ )	Low	Medium	High
Output impedance ( $Z_o$ )	High	Medium	Low

From this table, we get the following inferences regarding the three transistor configurations.

1. In case of CE amplifier both voltage gain and current gain are high. Generally speaking, we get high power gain also. The input and output impedance are of medium range, so the CE amplifier may be called a general purpose amplifier. The middle stages of a multistage amplifier are usually designed using this configuration.
2. The CC configuration has the high input impedance and low output impedance; its voltage gain is nearly equal to unity. So such an amplifier is used as a buffer amplifier between a source of high source resistance (poor source) and a low impedance load. Generally a source of high source resistance does not deliver much current to the load impedance as load impedance loads the source. The common collector configuration overcomes this difficulty as high input impedance of this configuration may properly be matched with the source resistance; thus it gives the output signal of almost the same magnitude as the input having the low output impedance. The low output impedance of CC amplifier will be properly matched with the low impedance load. The common collector configuration thus transforms the source of high output impedance to a source of low output impedance having the signal of almost same magnitude.
3. The common base configuration has the current gain of nearly unity, its input impedance is low and output impedance is high. So CB configuration may be used as buffer amplifier between a current source of low source resistance and high load impedance. It therefore transforms the source of low output impedance to a source of high output impedance having the current of almost same magnitude.

**7.6 Miller's Theorem:** This theorem states that an impedance  $Z$  shunting an active network having a known voltage gain  $A_V$  may be eliminated by connecting impedance

$$Z_1 = \frac{Z}{(1 - A_V)}$$
 and another impedance  $Z_2 = \frac{ZA_V}{(A_V - 1)}$  across the input and the output terminals respectively. This is illustrated in figure (7.16).

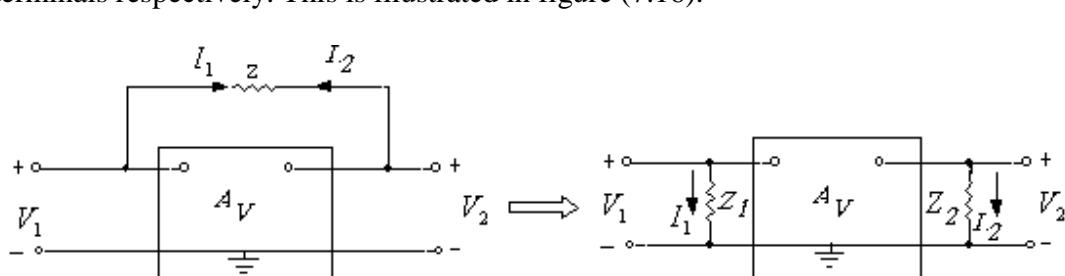


Fig. 7.16(a)

Fig. 7.16(b)

This can be proved by considering fig.(7.16a). The current  $I_1$  from this figure is given by:

$$I_1 = \frac{V_1 - V_2}{Z} \quad \text{----- (7.61)}$$

and the voltage  $V_2$  is given by:  $V_2 = A_V \cdot V_1$  ----- (7.62)

From equations (7.61) & (7.62) we have:

$$I_1 = \frac{V_1 - A_V V_1}{Z} = \frac{V_1(1 - A_V)}{Z} \quad \text{----- (7.63)}$$

From figure (7.16 b) the current  $I_1$  is given by  $I_1 = \frac{V_1}{Z_1}$  ----- (7.64)

From the equations (7.63) and (7.64), it is clear that the two networks given in figures (7.16a) & (7.16b) will be identical when  $Z_1 = \frac{Z}{(1 - A_V)}$

Similarly, from fig.(7.16a):

$$\begin{aligned} I_2 &= \frac{V_2 - V_1}{Z} \quad \text{and} \quad V_1 = \frac{V_2}{A_V} \\ \text{or} \quad I_2 &= \frac{V_2 - \frac{V_2}{A_V}}{Z} = \frac{V_2(1 - \frac{1}{A_V})}{Z} \end{aligned} \quad \text{----- (7.65)}$$

From fig. (7.16b)  $I_2 = \frac{V_2}{Z_2}$  ----- (7.66)

From the equations (7.65) and (7.66), it is clear that the two networks given in figures (7.16a) & (7.16b) will be identical when  $Z_2 = \frac{ZA_V}{(A_V - 1)}$

Hence the theorem is proved.

**7.7 Dual of Miller's Theorem:** It states that an impedance  $Z$ , in series with both the input and the output terminals of an active network having a known current source  $A_I$  may be eliminated by adding impedance  $Z_1 = Z(1 - A_I)$  and another impedance  $Z_2 = \frac{Z(A_I - 1)}{A_I}$  in series with the input and the output terminals respectively of the active network. This may be illustrated in figure (7.17).

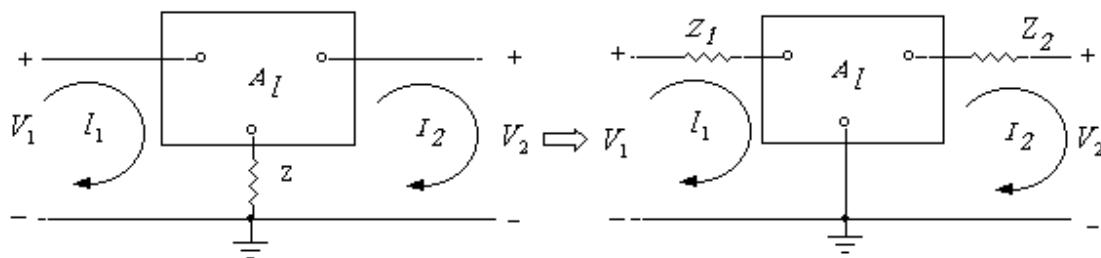


Fig. 7.17(a)

Fig. 7.17(b)

From figure (7.17a) the voltage across impedance  $Z$  is

$$Z(I_1 + I_2) = Z(I_1 - A_I I_1) = ZI_1(1 - A_I) \quad \text{----- (7.67)}$$

$$\text{where } A_I = -\frac{I_2}{I_1}$$

From figure (7.17b) the voltage across impedance  $Z_1$  is  $Z_1 I_1$

These two voltages will be equal when  $Z_1 = Z(1 - A_I)$

$$\text{In the similar fashion it can be proved that } Z_2 = \frac{Z(A_I - 1)}{A_I}$$

**7.8 The Emitter Follower:** As discussed above that the common collector amplifier has very high input impedance and very low output impedance and its voltage gain is almost unity. So this amplifier is used for impedance transformation. The practical circuit of the common collector amplifier is shown in figure (7.18), in which the collector is

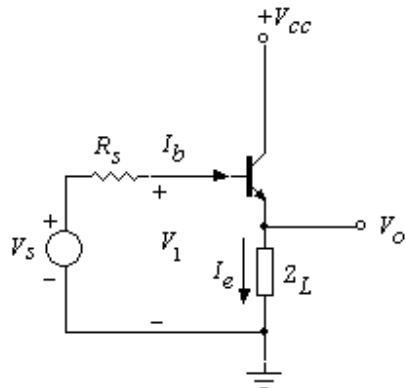


Fig. 7.18

directly connected to the supply voltage and a load impedance  $Z_L$  is connected to the emitter, and the output is taken across the load impedance. This circuit seems more as the common emitter amplifier than the common collector amplifier, but this is the common collector amplifier. In fact when the a.c. analysis of a network is made the d.c. source is assumed to be short circuited, this leads the collector to be shorted to the ground. Hence it is a common collector amplifier. The common collector amplifier is also known as the emitter follower, because its voltage gain is almost unity, any change in the base voltage will appear across the load impedance. The emitter (output) follows the input signal and hence the name emitter follower.

The expressions for current gain  $A_I$ , input impedance  $Z_I$ , voltage gain  $A_V$  and the output impedance  $Z_o$  are to be calculated. While calculating these expressions the common collector parameters of the transistor are to be used, but sometimes the common emitter  $h$  – parameters are given. So conversions of CE  $h$  – parameters to CC  $h$  parameters are to be made as shown in table 7.1. These expressions are therefore given below in terms of both common collector and common emitter  $h$  – parameters.

Current Gain       $A_I = \frac{-I_e}{I_b} = \frac{-h_{fe}}{1 + h_{oe}Z_L} = \frac{1 + h_{fe}}{1 + h_{oe}Z_L}$

Input Impedance       $Z_I = \frac{V_1}{I_b} = h_{ic} + h_{rc}A_I Z_L = h_{ie} + A_I Z_L$

Voltage Gain       $A_V = \frac{V_o}{V_1} = \frac{A_I Z_L}{Z_I} = 1 - \frac{h_{ie}}{Z_I}$

The voltage gain is slightly less than one and no phase reversal between input and output signal.

Output Admittance       $Y_o = h_{oc} - \frac{h_{rc}h_{fe}}{h_{ic} + R_s} = h_{oe} + \frac{1 + h_{fe}}{h_{ie} + R_s}$

**Example 7.7** A CE transistor amplifier is driven by a signal source of source resistance  $500 \Omega$ . The load impedance is  $2 K\Omega$ . The h –parameters values are given in the table 7.4. Calculate the current gain, input impedance, voltage gain and output impedance of the amplifier. Find the overall voltage gain and current gain also.

Solution:       $A_I = \frac{-h_{fe}}{(1 + h_{oe}Z_L)} = \frac{-100}{(1 + 5 \times 10^{-6} \times 2 \times 10^3)} = \frac{-100}{1.01} = -99$

$$Z_I = h_{ie} + h_{re}A_I Z_L = 2600 + 0.62 \times 10^{-4} \times (-99)(2 \times 10^3)$$

$$= 2600 - 12.276 = 2587.7 \Omega = 2.59 K\Omega$$

$$A_V = A_I \frac{Z_L}{Z_I} = (-99) \frac{2 K\Omega}{2.59 K\Omega} = -76.45$$

$$Y_o = h_{oe} - \frac{h_{fe}h_{re}}{(h_{ie} + R_s)} = 5 \times 10^{-6} - \frac{(100)(0.62 \times 10^{-4})}{(2600 + 500)}$$

$$= 5 \times 10^{-6} - 2 \times 10^{-6} = 3 \times 10^{-6} mhos$$

$$Z_o = \frac{1}{Y_o} = \frac{1}{3 \times 10^{-6}} = 333.33 K\Omega$$

$$A_{VS} = \frac{A_I Z_L}{R_s + Z_I} = \frac{(-99)(2 \times 10^3)}{(500 + 2587.7)} = -64.125$$

$$A_{IS} = \frac{A_I R_s}{R_s + Z_I} = \frac{(-99)(500)}{(500 + 2587.7)} = -16.03$$

**Example 7.8** A CB transistor amplifier is driven by a signal source of source resistance  $500 \Omega$ . The load impedance is  $2 K\Omega$ . The h –parameters values are given in the table 7.4. Calculate the current gain, input impedance, voltage gain and output impedance of the amplifier. Find the overall voltage gain and current gain also.

Solution:       $A_I = \frac{-h_{fb}}{(1 + h_{ob}Z_L)} = \frac{-(-.99)}{(1 + 0.05 \times 10^{-6} \times 2 \times 10^3)} \approx 0.99$

$$Z_I = h_{ib} + h_{rb}A_I Z_L = 25.8 + 0.67 \times 10^{-4} \times (0.99)(2 \times 10^3)$$

$$\begin{aligned}
&= 25.8 - 0.66 = 25.73\Omega \\
A_V &= A_I \frac{Z_L}{Z_I} = (0.99) \frac{2K\Omega}{25.73\Omega} = 76.95 \\
Y_o &= h_{ob} - \frac{h_{fb} h_{rb}}{(h_{ib} + R_s)} = 0.05 \times 10^{-6} - \frac{(-0.99)(0.67 \times 10^{-4})}{(25.8 + 500)} \\
&= 0.05 \times 10^{-6} + 0.126 \times 10^{-6} = 0.176 \times 10^{-6} \text{ mhos} \\
Z_o &= \frac{1}{Y_o} = \frac{1}{0.176 \times 10^{-6}} = 5.68M\Omega \\
A_{VS} &= \frac{A_I Z_L}{R_s + Z_I} = \frac{(0.99)(2 \times 10^3)}{(500 + 25.73)} = 3.77 \\
A_{IS} &= \frac{A_I R_s}{R_s + Z_I} = \frac{(0.99)(500)}{(500 + 25.73)} = 0.942
\end{aligned}$$

**Example 7.9** Design a single stage buffer amplifier which is to be used with a transducer having a source resistance of 12 KΩ. The amplifier should have input impedance greater than 100 KΩ when connected to the load impedance of 1 KΩ. The h – parameters of the transistor used are given in the table 7.4. Calculate the current gain, overall current gain, input impedance, voltage gain, overall voltage gain and output impedance of the amplifier thus designed.

**Solution:** From the above problem it is clear that the amplifier to be designed should have high input impedance (greater than 100 KΩ) and low output impedance (lower than 1 KΩ). The CC amplifier has such properties, so we are to design the CC amplifier. Now we calculate the various gain and input and output impedance as follows:

$$\begin{aligned}
A_I &= \frac{-h_{fc}}{(1 + h_{oc} Z_L)} = \frac{-(-101)}{(1 + 5 \times 10^{-6} \times 1 \times 10^3)} = \frac{101}{1.005} = 100.5 \\
Z_I &= h_{ic} + h_{rc} A_I Z_L = 2600 + 1 \times (100.5)(1 \times 10^3) \\
&= 2600 + 2587.7\Omega = 103.1K\Omega, \text{ which is greater than } 100 \text{ K}\Omega. \\
A_V &= A_I \frac{Z_L}{Z_I} = 100.5 \frac{1K\Omega}{103.1K\Omega} = 0.975 \\
Y_o &= h_{oc} - \frac{h_{fe} h_{rc}}{(h_{ic} + R_s)} = 5 \times 10^{-6} - \frac{(-101) \times 1}{(2600 + 12000)} \\
&= 5 \times 10^{-6} + 0.0069 = 6.9 \times 10^{-3} \text{ mhos} \\
Z_o &= \frac{1}{Y_o} = \frac{1}{6.9 \times 10^{-3}} = 144.9\Omega, \text{ which is less than } 1 \text{ K}\Omega \\
A_{VS} &= \frac{A_I Z_L}{R_s + Z_I} = \frac{(100.5)(1 \times 10^3)}{(12K + 103.1K)} = 0.87 \\
A_{IS} &= \frac{A_I R_s}{R_s + Z_I} = \frac{(100.5)(12K)}{(12K + 103.1K)} = 10.48
\end{aligned}$$

**7.9 Cascaded Transistor Amplifier:** We have studied that the three modes of the transistor are used to design the single stage amplifiers. But sometimes single stage amplifier does not provide the amplification up to the desired level or the input/ output impedances do not properly match. In such cases it becomes necessary to cascade the transistor amplifiers. The cascading we mean that the output of the first stage is connected to the input of the second stage. More than two stages may be connected as per our requirement. Several types of cascaded stages may be used for different purposes. A few of them are being discussed here.

**CE – CC Cascaded Amplifier:** Figure (7.19) shows the CE –CC cascaded amplifier, in which first stage is the common emitter stage and the second stage is the common

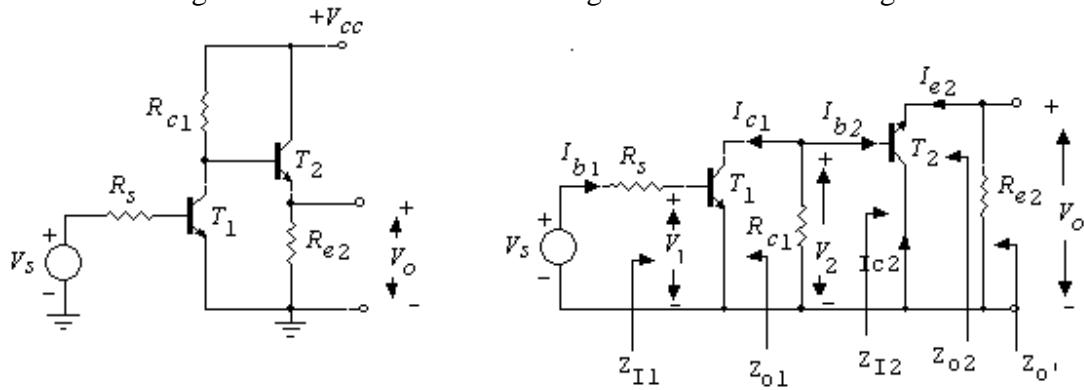


Fig. 7.19 a

Fig. 7.19 b

collector stage. We will find the expressions of various gains and input & output impedances of the cascaded amplifier. The current gain, input impedance and voltage gain of the second stage are calculated first and subsequently of first stage, since load resistance is required in the calculations of these quantities. However, the output impedance of the first stage is calculated first followed by the output impedance of the second stage.

**Analysis of the second stage:** The current gain of the second stage which is the common collector stage is given by (ref. table 7.3):

$$A_{I2} = -\frac{I_{c2}}{I_{b2}} = \frac{-h_{fc}}{1 + h_{oc} R_{c2}}$$

The input impedance is  $Z_{I2} = h_{ic} + h_{rc} A_{I2} R_{c2}$

The voltage gain of this stage is given by:

$$A_{V2} = \frac{V_o}{V_2} = A_{I2} \frac{R_{c2}}{Z_{I2}}$$

**Analysis of first stage:** For the first stage the effective load resistance will be the parallel combination of  $R_{c1}$  and  $Z_{I2}$  given by

$$R_{L1} = \frac{R_{c1} Z_{I2}}{R_{c1} + Z_{I2}}$$

The current gain of this stage is

$$A_{I1} = -\frac{I_{c1}}{I_{b1}} = \frac{-h_{fe}}{1 + h_{oe} R_{L1}}$$

The input impedance of the first stage which is also the input impedance of the cascaded amplifier is given by:

$$Z_{I1} = h_{ie} + h_{re} A_{I1} R_{L1}$$

The voltage gain of this stage is

$$A_{V1} = \frac{V_2}{V_1} = A_{I1} \frac{R_{L1}}{Z_{I1}}$$

The output admittance  $Y_o = (1/Z_{o1})$  of the first stage is given by

$$Y_{o1} = \left( h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s} \right)$$

The output impedance of this stage, taking into account the resistance  $R_{c1}$ , will be the parallel combination of  $Z_{o1}$  and  $R_{c1}$ .

$$\text{i.e. } Z'_{o1} = Z_{o1} \| R_{c1}$$

The output admittance of the second stage can be calculated by considering the effective source resistance  $R_{s2}$  as the parallel combination of  $Z_{o1}$  and  $R_{c1}$ .

$$Y_{o2} = \left( h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic} + R_{s2}} \right)$$

The output impedance of the cascaded amplifier will be the parallel combination of  $Z_{o2}$  and  $R_{c2}$

$$\text{i.e. } Z_0 = Z_{o2} \| R_{c2}$$

Now the total (overall) current gain of both stages is

$$A_I = -\frac{I_{c2}}{I_{b1}} = -\frac{I_{c2}}{I_{b2}} \frac{I_{b2}}{I_{c1}} \frac{I_{c1}}{I_{b1}} = -A_{I2} \cdot A_{I1} \frac{I_{b2}}{I_{c1}}$$

From figure (7.19) we have

$$\begin{aligned} I_{b2} &= (-I_{c1}) \left( \frac{R_{c1} Z_{I2}}{Z_{I2} + R_{c1}} \right) \left( \frac{1}{Z_{I2}} \right) \\ \text{or } \frac{I_{b2}}{I_{c1}} &= - \left( \frac{R_{c1}}{Z_{I2} + R_{c1}} \right) \end{aligned}$$

$$\text{Hence } A_I = A_{I2} \cdot A_{I1} \left( \frac{R_{c1}}{Z_{I2} + R_{c1}} \right)$$

The voltage gain of the cascaded amplifier is

$$A_V = \frac{V_o}{V_1} = \frac{V_o}{V_2} \frac{V_2}{V_1} = A_{V2} A_{V1}$$

The overall voltage gain of the cascaded amplifier by considering the source resistance also, is given by:

$$A_{Vs} = \frac{V_o}{V_s} = A_V \frac{Z_{I1}}{Z_{I1} + R_s}$$

**7.10 Simplified Common – Emitter Hybrid Model:** In the preceding sections the exact hybrid models of the transistors were used for getting the expressions of various gains and input & output impedances of different transistor amplifiers. However, in most cases the approximate hybrid model of the transistor will give acceptable results within the specified limits, thus tedious and lengthy calculations may be avoided. The CE amplifier is most frequently used amplifier, so we shall get the simplified h – parameter model in this configuration which will further be used in CB and CC configuration circuits.

The exact model in CE configuration is redrawn in figure (7.20).

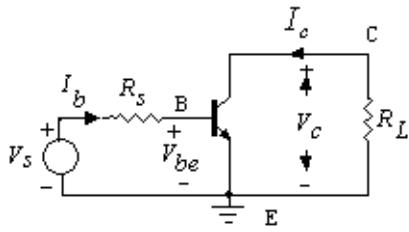


Fig. 7.20 a

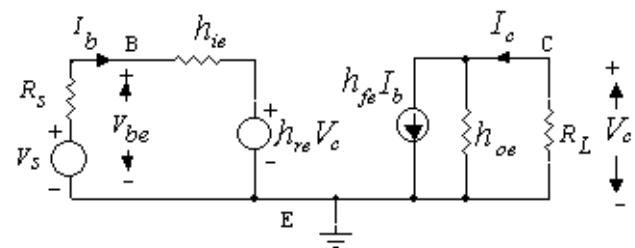


Fig. 7.20 b

Out of four  $h$  – parameters only two parameters  $h_{ie}$  and  $h_{fe}$  are sufficient to use in the simplified model in CE configuration and other two parameters may be neglected provided the load resistance  $R_L$  is small enough in comparison with  $(1/h_{oe})$ , so that the parallel combination  $R_L$  and  $1/h_{oe}$  is approximately equal to  $R_L$ . We may, therefore, omit  $h_{oe}$  from the exact model shown in figure (7.20 b). In this condition the collector current will be approximately equal to  $h_{fe}I_b$ . The magnitude of the voltage source  $(h_{re}V_c)$  in the emitter circuit will be equal to  $h_{re}h_{fe}I_bR_L$  since  $V_c = -h_{fe}I_bR_L$ . In most of the transistor parameters  $h_{re}h_{fe} \approx 0.01$ , so the voltage  $h_{re}V_c$  may be neglected in comparison with the voltage drop  $(h_{ie}I_b)$  across  $h_{ie}$  provided  $R_L$  is small enough. The simplified model may therefore be given in figure (7.21). It has been observed that the errors in using this simplified model will not be more than 10% if  $h_{oe}R_L < 0.1$ .

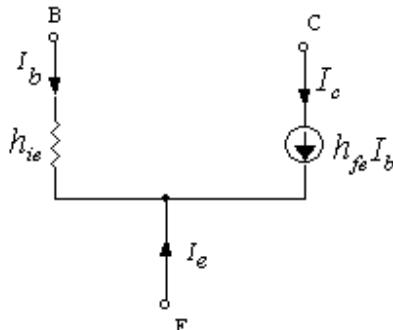


Fig. 7.21

We shall now calculate various gains and input and output impedances in all the three configurations using this simplified model.

**7.10.1 Simplified Calculation for the Common Emitter Configuration:** The simplified model in CE configuration is shown in figure (7.22).

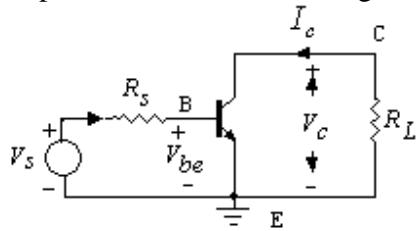


Fig. 7.22 a

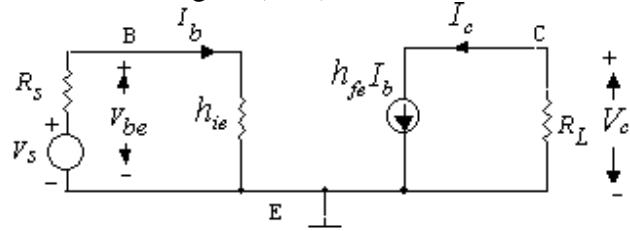


Fig. 7.22 b

(i) **Current Gain:** From the figure (7.22 b) we have

$$A_I = \frac{-I_c}{I_b} \cong -\frac{h_{fe}I_b}{I_b} = -h_{fe} \quad \text{----- (7.68)}$$

(ii) **Input impedance:** The input impedance  $Z_I$  is given by:

$$Z_I = h_{ie} + h_{re}A_I R_L$$

which may be put in the form

$$Z_I = h_{ie} \left[ 1 - \frac{h_{re}h_{fe}}{h_{ie}h_{oe}} \frac{|A_I|}{h_{fe}} h_{oe} R_L \right] \quad \text{----- (7.69)}$$

The value of the quantity  $\left[ \frac{h_{re}h_{fe}}{h_{ie}h_{oe}} \right]$  is approximately 0.5 for the typical  $h$ -parameter values of the transistor.

Thus, if  $h_{oe} R_L < 0.1$  then  $Z_I \cong h_{ie}$ .

(iii) **Voltage Gain:**

$$A_V = \frac{A_I R_L}{Z_I} \cong -\frac{h_{fe} R_L}{h_{ie}} \quad \text{----- (7.70)}$$

**(iv) Output Impedance:** From Fig. 7.22 b, if  $V_c$  is the applied voltage at the output, we

$$\text{get } Z_o = \frac{V_c}{I_c} \text{ with } V_s = 0.$$

Since  $h_{fe}I_b$  reduces to zero then  $Z_o = \infty$ . The true value of  $Z_o$  depends upon the source resistance and lies between 40 to 80 KΩ.

Output impedance  $Z_o$  taking into account the load resistance  $R_L$  will be approximately equal to  $R_L$  as it is the parallel combination of output resistance ( $Z_o = \infty$ ) and  $R_L$ .

**7.10..2 Simplified Calculation for the Common Base Configuration:** The simplified model of CE configuration can be used to get approximate model in CB configuration as shown in figure (7.23) in which base is grounded and the collector is connected to the ground through the load resistance  $R_L$ .

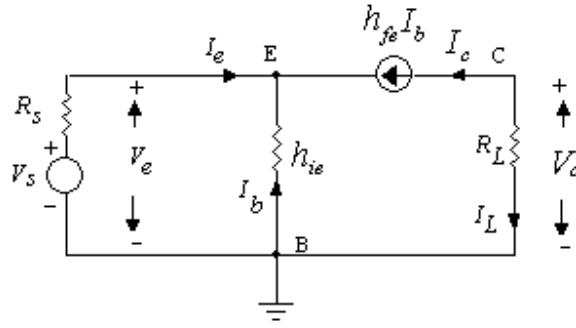


Fig. 7.23

**(i) Current Gain:** From the figure (7.23) we have

$$A_I = \frac{I_L}{I_e} = \frac{-I_c}{I_b}$$

$$\approx \frac{-h_{fe}I_b}{-I_b(1+h_{fe})} = \frac{h_{fe}}{1+h_{fe}}$$

**(ii) Input impedance:**  $Z_I = \frac{V_e}{I_e} \approx \frac{-h_{ie}I_b}{-(1+h_{fe})I_b} = \frac{h_{ie}}{1+h_{fe}}$

**(iii) Voltage Gain:**  $A_v = A_I \frac{R_L}{Z_I} \approx \frac{h_{fe}}{1+h_{fe}} \frac{(1+h_{fe})}{h_{ie}} R_L$

$$= \frac{h_{fe}}{h_{ie}} R_L$$

**(iv) Output Impedance:**  $Z_o = \frac{V_c}{I_c} = \infty \text{ as } V_s = 0$

The output resistance taking into account  $R_L$  will be equal to  $R_L$ .

**7.10.3 Simplified Calculation for the Common Collector Configuration:** The simplified model of CE configuration can be used to get approximate model in CC

configuration as shown in figure (7.24) in which collector is grounded and the load resistance  $R_L$  is connected between emitter and the ground.

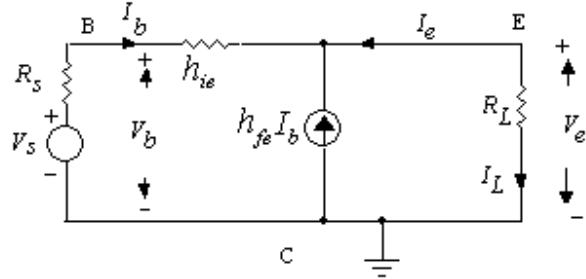


Fig. 7.24

(i) **Current Gain:** From the figure (7.24) we have

$$A_I = \frac{I_L}{I_b} = \frac{-I_e}{I_b}$$

$$\cong \frac{(1+h_{fe})I_b}{I_b} = 1 + h_{fe}$$

(ii) **Input impedance:**

$$Z_I = \frac{V_b}{I_b} \cong \frac{h_{ie}I_b + (1+h_{fe})I_bR_L}{I_b}$$

$$= h_{ie} + (1+h_{fe})R_L$$

(iii) **Voltage Gain:**

$$A_v = A_I \frac{R_L}{Z_I} \cong \frac{(1+h_{fe})R_L}{h_{ie} + (1+h_{fe})R_L}$$

$$= \frac{h_{ie} + (1+h_{fe})R_L - h_{ie}}{h_{ie} + (1+h_{fe})R_L} = 1 - \frac{h_{ie}}{Z_I}$$

(iv) **Output Impedance:** From the figure (7.24), the open circuit output voltage is  $V_s$  while the short circuit output current is

$$I = (1+h_{fe})I_b = \frac{(1+h_{fe})V_s}{R_s + h_{ie}}.$$

So the output impedance is given by:

$$Z_o = \frac{V_s}{I} = \frac{R_s + h_{ie}}{1+h_{fe}}$$

The output resistance taking into account  $R_L$  will be equal to the parallel combination of  $R_L$  and  $Z_o$  calculated above.

The approximate formulas for different quantities obtained using the simplified model of the transistor are given in table 7.6 for the three configurations.

**Table 7.6**

Quantity	CE	CB	CC
$A_I$	$-h_{fe}$	$\frac{h_{fe}}{1+h_{ie}}$	$1+h_{fe}$
$Z_I$	$h_{ie}$	$\frac{h_{ie}}{1+h_{fe}}$	$h_{ie} + (1+h_{fe})R_L$
$A_v$	$-\frac{h_{fe}R_L}{h_{ie}}$	$\frac{h_{fe}}{h_{ie}}R_L$	$1 - \frac{h_{ie}}{Z_I}$
$Z_o$	$\infty$	$\infty$	$\frac{R_s + h_{ie}}{1+h_{fe}}$
$Z'_o$	$R_L$	$R_L$	$Z_o \parallel R_L$

**7.11 CC – CC Cascaded Amplifier (Darlington pair):** As is well known that the common collector amplifier is used where we need input impedance to be large enough and output impedance to be very small. Some times one stage of such an amplifier does not provide much degree of buffering (ratio of  $Z_I / Z_o$ ), it becomes necessary to cascade two transistors, each in CC configuration as shown in figure (7.25). A pair of transistors connected like this is known as a Darlington pair. Analysis of this circuit will be done as in the previous case of cascaded amplifier.

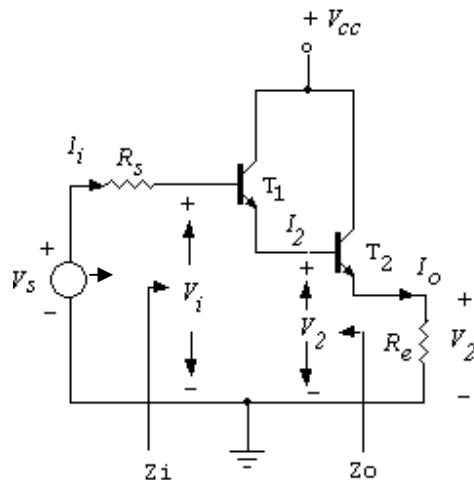


Fig. 7.25

The current gain of the transistor  $T_2$  is calculated first, assuming  $h_{oe}R_e \leq 0.1$  and  $h_{fe}R_e \gg h_{ie}$ . The relations given in table 7.6 may be used for calculating the current gain and input impedance of the second stage.

$$A_{I2} = \frac{I_o}{I_2} \approx 1 + h_{fe} \quad \text{and} \quad Z_{I2} \approx (1 + h_{fe})R_e$$

We shall find the current gain of the first stage by considering the exact formula of the current gain as  $h_{oe}Z_{I2} \leq 0.1$  requirement is not met out since  $Z_{I2}$  is the effective load resistance for the transistor  $T_1$ .

$$\begin{aligned} \text{Thus } A_{I1} &= \frac{I_2}{I_i} = \frac{1+h_{fe}}{1+h_{oe}Z_{I2}} \\ &= \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe})R_e} \\ &\approx \frac{1+h_{fe}}{1+h_{oe}h_{fe}R_e} \quad \text{as } h_{oe}R_e \leq 0.1. \end{aligned}$$

The overall current gain of the Darlington pair is given by:

$$\begin{aligned} A_I &= \frac{I_o}{I_i} = \frac{I_o}{I_2} \frac{I_2}{I_i} = A_{I2}A_{I1} \\ \text{or } A_I &= \frac{(1+h_{fe})^2}{1+h_{oe}h_{fe}R_e} \end{aligned}$$

The input impedance of  $T_1$ , which will be the overall input impedance of the cascaded circuit, is given by:

$$Z_{I1} = h_{ie} + A_{I1}R_{i2} \approx \frac{(1+h_{fe})^2 R_e}{1+h_{oe}h_{fe}R_e}$$

The voltage gain of the first stage is given by the expression,

$$A_{V1} = 1 - \frac{h_{ie}}{Z_{I1}}$$

$$\text{and } A_{V2} \approx 1 - \frac{h_{ie}}{A_{I1}Z_{I2}}$$

The overall voltage gain of the Darlington emitter follower is

$$\begin{aligned} A_V &= A_{V1}A_{V2} = \left(1 - \frac{h_{ie}}{Z_{I2}}\right) \left(1 - \frac{h_{ie}}{A_{I1}Z_{I2}}\right) \\ &\approx 1 - \frac{h_{ie}}{A_{I1}Z_{I2}} - \frac{h_{ie}}{Z_{I2}} \end{aligned}$$

$$\text{But } A_{I1}Z_{I2} \gg h_{ie}, \quad \text{hence } A_V \approx \left(1 - \frac{h_{ie}}{Z_{I2}}\right)$$

It is clear from this equation that the voltage gain of the Darlington emitter follower is approximately the same as that of the conventional emitter follower of transistor  $T_2$  and is very close to unity.

The output impedance  $Z_{o1}$  of the first stage is given by:

$$Z_{o1} = \frac{R_s + h_{ie}}{1+h_{fe}}$$

This output impedance works as the source resistance for the second stage of the circuit. Hence the output impedance of the second stage, which will be the overall output impedance of the circuit given by:

$$Z_{o2} \approx \frac{\frac{R_s + h_{ie}}{1 + h_{fe}} + h_{ie}}{1 + h_{fe}} \approx \frac{R_s + h_{ie}}{(1 + h_{fe})^2} + \frac{h_{ie}}{1 + h_{fe}}$$

Thus the output impedance of this Darlington pair circuit is smaller than that of single stage emitter follower.

From the above calculations of the Darlington emitter follower circuit, it is concluded that:

- (i) Its overall current gain is high.
- (ii) Its input impedance is higher than that of the single stage emitter follower.
- (iii) Its voltage gain close to unity and approximately the same as that of the single stage emitter follower.
- (iv) Its output impedance is smaller than that of the single stage.

The major drawback of this Darlington pair of transistors is that the leakage current of the first stage of the amplifier is amplified by the second stage. Hence the overall leakage current is high and is not suitable to use more than three transistors in cascade in emitter follower mode.

**Example 7.10** Show that the overall h parameters of the two – stage cascaded amplifier shown in figure (7.26)are

$$\begin{array}{ll} \text{(i)} \quad h_{11} = h_{11}' - \frac{h_{12}' h_{21}'}{1 + h_{22}' h_{11}''} h_{11}'' & \text{(ii)} \quad h_{12} = \frac{h_{12}' h_{12}''}{1 + h_{22}' h_{11}''} \\ \text{(iii)} \quad h_{21} = -\frac{h_{21}' h_{21}''}{1 + h_{22}' h_{11}''} & \text{(iv)} \quad h_{22} = h_{22}'' - \frac{h_{12}'' h_{21}''}{1 + h_{22}'' h_{11}'} h_{22}' \end{array}$$

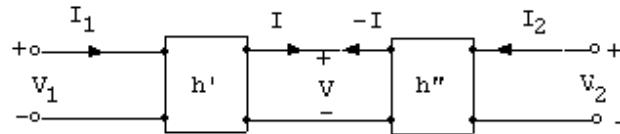


Fig. 7.26

**Solution:** For the two individual networks shown in figure (7.26 h – parameter equations are given

$$V_1 = h_{11}' I_1 + h_{12}' V \quad \dots \dots \quad (7.71)$$

$$I = h_{21}' I_1 + h_{22}' V \quad \dots \dots \quad (7.72)$$

$$\text{and} \quad V = -h_{11}'' I + h_{12}'' V_2 \quad \dots \dots \quad (7.73)$$

$$I_2 = -h_{21}'' I + h_{22}'' V_2 \quad \dots \dots \quad (7.74)$$

The h - parameter equations of the cascaded network in the required form are given

$$V_1 = h_{11}I_1 + h_{12}V_2 \quad \dots \dots \dots (7.75)$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \quad \dots \dots \dots (7.76)$$

Using the equations (7.71) to (7.74), we get the two equations of the form given in equations (7.75) & (7.76).

Putting the value of  $I$  from equation (7.72) in equations (7.73) & (7.74) we have

$$\begin{aligned} V &= -h_{11}''(h_{21}'I_1 + h_{22}'V) + h_{12}''V_2 \\ \text{or } V(1 + h_{11}''h_{22}') &= -h_{11}''h_{21}'I_1 + h_{12}''V_2 \\ \text{or } V &= -\frac{h_{11}''h_{21}'}{(1 + h_{11}''h_{22}')}I_1 + \frac{h_{12}''}{(1 + h_{11}''h_{22}')}V_2 \quad \dots \dots \dots (7.77) \\ \text{and } I_2 &= -h_{21}''(h_{21}'I_1 + h_{22}'V) + h_{22}''V_2 \\ \text{or } I_2 &= -h_{21}''h_{21}'I_1 - h_{21}''h_{22}'V + h_{22}''V_2 \quad \dots \dots \dots (7.78) \end{aligned}$$

Put the value of  $V$  from equation (7.77) in equations (7.71) & (7.78) we have

$$\begin{aligned} V_1 &= h_{11}'I_1 + h_{12}'\left(-\frac{h_{11}''h_{21}'}{(1 + h_{11}''h_{22}')}I_1 + \frac{h_{12}''}{(1 + h_{11}''h_{22}')}V_2\right) \\ \text{or } V_1 &= \left(h_{11}' - \frac{h_{12}'h_{11}''h_{21}'}{(1 + h_{11}''h_{22}')}I_1 + \frac{h_{12}'h_{12}''}{(1 + h_{11}''h_{22}')}V_2\right) \\ \text{or } V_1 &= \left(\frac{h_{11}' + h_{11}''h_{11}'h_{22}' - h_{12}'h_{11}''h_{21}'}{(1 + h_{11}''h_{22}')}I_1 + \frac{h_{12}'h_{12}''}{(1 + h_{11}''h_{22}')}V_2\right) \\ \text{or } V_1 &= \left(h_{11}' - \frac{h_{12}'h_{21}'}{(1 + h_{11}''h_{22}')}h_{11}''\right)I_1 + \frac{h_{12}'h_{12}''}{(1 + h_{11}''h_{22}')}V_2 \quad \dots \dots \dots (7.79) \\ \text{and } I_2 &= -h_{21}''h_{21}'I_1 - h_{21}''h_{22}'\left(-\frac{h_{11}''h_{21}'}{(1 + h_{11}''h_{22}')}I_1 + \frac{h_{12}''}{(1 + h_{11}''h_{22}')}V_2\right) + h_{22}''V_2 \\ \text{or } I_2 &= \left(-h_{21}''h_{21}' + \frac{h_{21}''h_{22}'h_{11}''h_{21}'}{(1 + h_{11}''h_{22}')}I_1 + \left(h_{22}'' - \frac{h_{21}''h_{22}'h_{12}''}{(1 + h_{11}''h_{22}')}V_2\right)\right) \\ \text{or } I_2 &= \left(\frac{-h_{21}''h_{21}' - h_{21}''h_{21}'h_{11}''h_{22}' + h_{21}''h_{22}'h_{11}''h_{21}'}{(1 + h_{11}''h_{22}')}I_1 + \left(\frac{h_{22}'' + h_{11}''h_{22}'h_{22}'' - h_{21}''h_{22}'h_{12}''}{(1 + h_{11}''h_{22}')}V_2\right)\right) \\ \text{or } I_2 &= \left(\frac{-h_{21}''h_{21}'}{(1 + h_{11}''h_{22}')}I_1 + \left(h_{22}'' - \frac{h_{21}''h_{12}''}{(1 + h_{11}''h_{22}')}h_{22}'\right)V_2\right) \quad \dots \dots \dots (7.80) \end{aligned}$$

Comparing the equations (7.79) & (7.80) with equations (7.75) & (7.76), we get the required result.

$$\begin{array}{ll}
 \text{(i)} & h_{11} = h_{11}^{\prime} - \frac{h_{12}^{\prime} h_{21}^{\prime}}{1 + h_{22}^{\prime} h_{11}^{\prime\prime}} h_{11}^{\prime\prime} \\
 & \text{(ii)} \quad h_{12} = \frac{h_{12}^{\prime} h_{12}^{\prime\prime}}{1 + h_{22}^{\prime} h_{11}^{\prime\prime}} \\
 \text{(iii)} & h_{21} = -\frac{h_{21}^{\prime} h_{21}^{\prime\prime}}{1 + h_{22}^{\prime} h_{11}^{\prime\prime}} \\
 & \text{(iv)} \quad h_{22} = h_{22}^{\prime\prime} - \frac{h_{12}^{\prime\prime} h_{21}^{\prime\prime}}{1 + h_{22}^{\prime} h_{11}^{\prime\prime}} h_{22}^{\prime}
 \end{array}$$

**Example 7.11** Show that the overall  $h$  – parameters for the composite transistors illustrated in figure (7.27), are:

$$\begin{array}{ll}
 \text{(i)} & h_{ie} = h_{ie1} + \frac{(1 - h_{re1})(1 + h_{fe1})h_{ie2}}{1 + h_{oe1}h_{ie2}} \\
 \text{(ii)} & h_{fe} = h_{fe1} + \frac{(h_{fe2} - h_{oe1}h_{ie2})(1 + h_{fe1})}{1 + h_{oe1}h_{ie2}} \\
 \text{(iii)} & h_{oe} = h_{oe2} + \frac{(1 + h_{fe2})(1 - h_{re2})h_{oe1}}{1 + h_{oe1}h_{ie2}} \\
 \text{(iv)} & h_{re} = h_{re2} + \frac{(h_{ie2}h_{oe1} + h_{re1})(1 - h_{re2})}{1 + h_{oe1}h_{ie2}}
 \end{array}$$

- (v) Obtain the numerical values for the  $h$  – parameters of the composite transistor by assuming transistors  $T_1$  and  $T_2$  as identical and using  $h_{ie} = 1100\Omega$ ,  $h_{re} = 2.5 \times 10^{-4}$ ,  $h_{fe} = 50$  and  $h_{oe} = 24\mu A/volts$ .

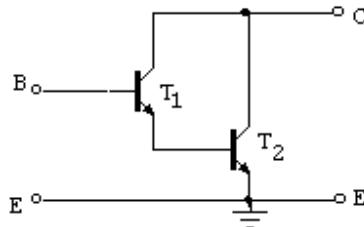


Fig. 7.27

**Solution:** The transistor  $T_1$  is in CC configuration and  $T_2$  is in CE configuration. The  $h$  – parameters of the composite configuration may be obtained using the results of example 7.10.

$$\text{(i)} \quad h_{ie} = h_{ic1} - \frac{h_{rc1}h_{fc1}}{1 + h_{oc1}h_{ie2}} h_{ie2}$$

Put CC  $h$  – parameters in the form of CE  $h$  – parameters as

$$h_{ic1} = h_{ie1} \quad h_{fc1} = -(1 + h_{fe1})$$

$$\begin{aligned}
h_{rc1} &= (1 - h_{re1}) & h_{oc1} &= h_{oe1} \\
h_{ie} &= h_{ie1} - \frac{(1 - h_{re1})(1 + h_{fe1})}{1 + h_{oe1}h_{ie2}} h_{ie2} & \text{part (i) proved.} \\
\text{(ii)} \quad h_{fe} &= -\frac{h_{fc1}h_{fe2}}{1 + h_{oc1}h_{ie2}} = \frac{(1 + h_{fe1})h_{fe2}}{1 + h_{oe1}h_{ie2}} \\
&= \frac{h_{fe2} + h_{fe1}h_{fe2} - h_{oe1}h_{ie2}h_{fe1} + h_{oe1}h_{ie2} - h_{oe1}h_{ie2} + h_{oe1}h_{ie2}h_{fe1}}{1 + h_{oe1}h_{ie2}} \\
&= h_{fe1} + \frac{(1 + h_{fe1})h_{fe2} - h_{oe1}h_{ie2}(1 + h_{fe1})}{1 + h_{oe1}h_{ie2}} \\
\text{(iii)} \quad h_{re} &= \frac{h_{rc1}h_{re2}}{1 + h_{oc1}h_{ie2}} = \frac{(1 - h_{re1})h_{re2}}{1 + h_{oe1}h_{ie2}}
\end{aligned}$$

### Problems:

1. Define  $h$  – parameters of a transistor. Draw the  $h$  – parameter model of a transistor.
2. Discuss how are  $h$  – parameters deduced from the input output characteristics curves of the transistor.
3. Discuss the method of converting  $h$  – parameters from one configuration to other configuration.
4. Draw the circuit of transistor in common emitter configuration and give its  $h$  – parameter model.
5. Draw the circuit of transistor in common base configuration and give its  $h$  – parameter model.
6. Draw the circuit of transistor in common collector configuration and give its  $h$  – parameter model.
7. Find CE  $h$  – parameters in terms of CC configuration.
8. Find CC  $h$  – parameters in terms of CE configuration.
9. Find CE  $h$  – parameters in terms of CB configuration.
10. Find CB  $h$  – parameters in terms of CE configuration.
11. Find CB  $h$  – parameters in terms of CC configuration.
12. Find CC  $h$  – parameters in terms of CB configuration.
13. Discuss the method of converting  $h$  – parameter from one configuration to other configuration.
14. Explain how to obtain  $h_{fe}$  and  $h_{re}$  from the output characteristics of the transistor.
15. Prove that  $h_{ic} = h_{ie}$ ,  $h_{rc} = (1 - h_{re})$ ,  $h_{fc} = -(1 + h_{fe})$ ,  $h_{oc} = h_{oe}$ .
16. Prove that  $h_{ie} = h_{ic}$ ,  $h_{re} = (1 - h_{rc})$ ,  $h_{fe} = -(1 + h_{fc})$ ,  $h_{oe} = h_{oc}$ .
17. Prove the following expressions:

$$h_{ic} = \frac{h_{ib}}{[h_{ib}h_{ob} + (1-h_{rb})(1+h_{fb})]} \quad h_{rc} = \frac{(1+h_{fb})}{[h_{ib}h_{ob} + (1-h_{rb})(1+h_{fb})]}$$

18. Prove the following expressions:

$$h_{fc} = \frac{-(1-h_{rb})}{[h_{ib}h_{ob} + (1-h_{rb})(1+h_{fb})]} \quad h_{oc} = \frac{h_{ob}}{[h_{ib}h_{ob} + (1-h_{rb})(1+h_{fb})]}$$

19. (i) Prove the following expressions

$$h_{ib} = \frac{h_{ie}}{(1+h_{fe})(1-h_{re}) + h_{ie}h_{oe}} \quad h_{rb} = \frac{h_{ie}h_{oe} - h_{re}(1+h_{fe})}{(1+h_{fe})(1-h_{re}) + h_{ie}h_{oe}}$$

(ii) From these exact formulas deduce the approximate formulas given below:

$$h_{ib} = \frac{h_{ie}}{1+h_{fe}} \quad h_{rb} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$$

20. (i) Prove the following expressions

$$h_{fe} = \frac{-h_{fb}(1-h_{rb}) - h_{ib}h_{ob}}{(1+h_{fb})(1-h_{rb}) + h_{ib}h_{ob}} \quad h_{oe} = \frac{h_{ob}}{(1+h_{fb})(1-h_{rb}) + h_{ib}h_{ob}}$$

(ii) From these exact formulas prove the following expressions

$$h_{fe} = \frac{-h_{fb}}{1+h_{fb}} \quad h_{oe} = \frac{h_{ob}}{1+h_{fb}}$$

21. By drawing the variations of voltage gain, current gain and input impedance with load impedance and output impedance with source resistance for the three configuration of the transistor, find the characteristics of the transistor amplifier in the three configurations.
22. Discuss the comparative study of the transistor amplifier in the three configurations.
23. Draw the circuit model of a transistor amplifier (general amplifier configuration). Using this model find the expressions of various gains, input and output impedances.
24. Drive the expressions of  $A_I$  and  $Z_I$  of a transistor amplifier in terms of load impedance.
25. State and prove Miller theorem and its dual.
26. Using the approximate model  $h$  – parameter model, obtain the expression for a CE circuit for  $A_I$ ,  $Z_I$ ,  $A_V$ , and  $Z_o$ .
27. Using the approximate model  $h$  – parameter model, obtain the expression for the emitter follower circuit for  $A_I$ ,  $Z_I$ ,  $A_V$ , and  $Z_o$ . What are the advantages of the emitter follower circuit?
28. Using the simplified model of the CE configuration obtain the expressions of various gain and input output impedances of the CB configuration.
29. Using the simplified model of the CE configuration obtain the expressions of various gain and input output impedances of the CC configuration.
30. Using the simplified model of the CE configuration obtain the expressions of various gain and input output impedances of this configuration.
31. What do you understand by the cascading of the transistor amplifiers? Why cascading is done? Draw the circuit of CE – CC cascaded amplifiers. Find the

expressions of the overall voltage gain, current gain and input / output impedances of this cascaded amplifier.

32. Draw a Darlington emitter follower circuit and find the expressions of the overall voltage gain, current gain and input / output impedances of this Darlington emitter follower circuit.
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# 8

## Transistor Biasing and Thermal Stabilization

In this chapter we shall discuss the different biasing methods of transistor, to operate the transistor in the linear operating region of the characteristics. The operating point shifts with temperature as the transistor parameters are dependent on temperature. The temperature compensated techniques will also be discussed in this chapter in addition to the study of the stability factor of different biasing methods.

**8.1 The Operating Point:** It is well known that the CE amplifier is most commonly used amplifier and whenever the general amplification of the signal is needed this amplifier configuration is used. So we shall discuss the operating point and other factor by considering the CE amplifier. Figure 8.1(a) shows a simple circuit of CE

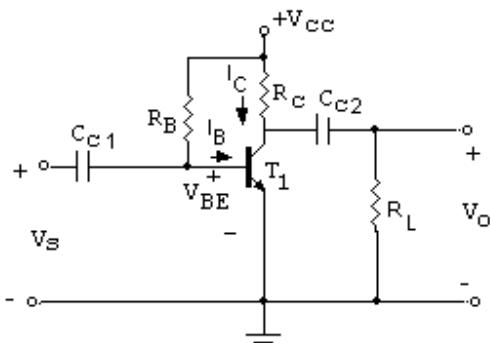


Fig. 8.1(a)

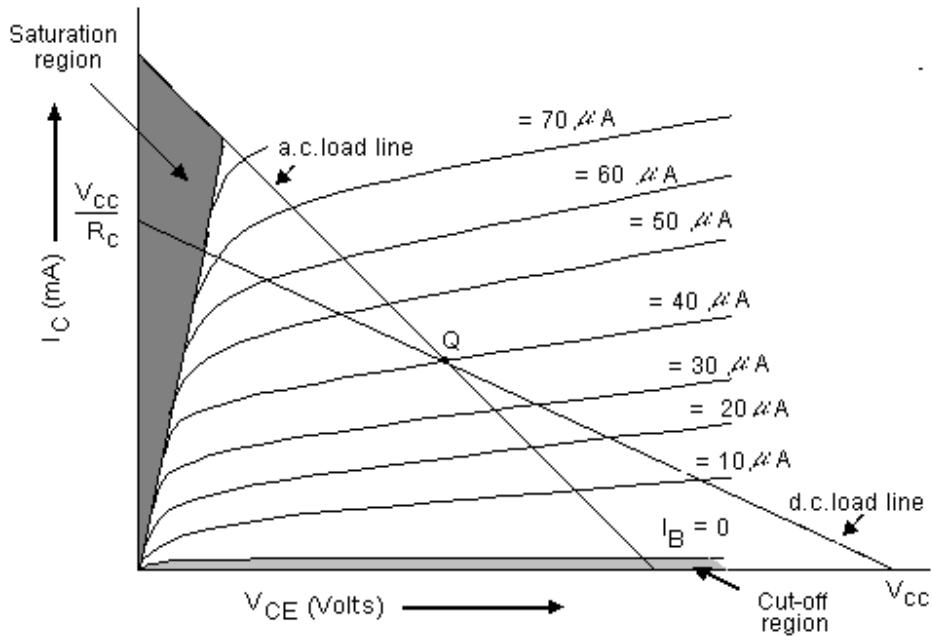


Fig. 8.1(b)

amplifier. In this circuit  $V_{CC}$  and  $R_C$  are fixed. The values of collector current  $I_C$  and collector to emitter voltage  $V_{CE}$  are dependent on the values of  $R_B$ . The signal to be amplified from the source  $V_s$  is applied to the base of the transistor through the coupling capacitor  $C_{CI}$  and the output is taken from the collector through the other coupling capacitor  $C_{C2}$ . These two coupling capacitors offer low reactances to the signal frequency thus the signal is passed through them and d.c. voltage is blocked. Figure 8.1(b) shows a set of output characteristics of a transistor.

Applying KVL to the collector circuit (fig. 8.1a) under d.c. condition the coupling capacitor  $C_{C2}$  will act as an open circuit and  $R_L = \infty$ , it is obtained

$$V_{CC} = R_C I_C + V_{CE}$$

$$\text{or } I_C = \left(-\frac{1}{R_C}\right).V_{CC} + \frac{V_{CC}}{R_C}$$

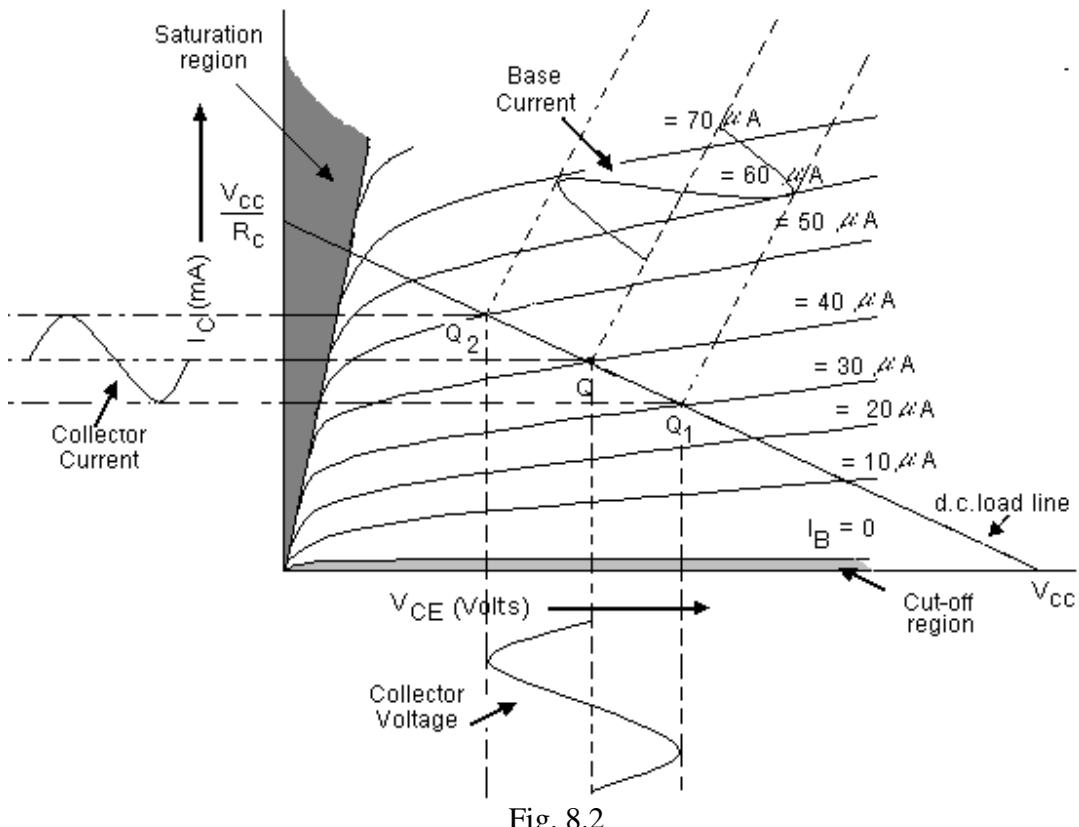
The above equation is a straight line equation of the form  $y = mx + C$ , having the slope  $\left(-\frac{1}{R_C}\right)$  and intercept on y-axis as  $\frac{V_{CC}}{R_C}$ .

A straight line drawn between  $\frac{V_{CC}}{R_C}$  and  $V_{CC}$  on the characteristic curves of the transistor will have the slope  $\left(-\frac{1}{R_C}\right)$  as shown in figure 8.1(b). This straight on the characteristic curves of the transistor is known as the d.c or static load line.

The point of intersection of the load line and characteristic curve of the particular base current is known as quiescent operating point or simply the operating point. The operating point may be chosen anywhere on the load line, which will be decided by the base current. For the proper amplification of the signal the transistor should be operated in the centre of the load line.

If on the other hand  $R_L \neq \infty$ , an a.c. or dynamic load line is to be drawn. At the signal frequency  $C_{C2}$  will act as short circuit, the effective load resistance at the collector will be the parallel combination of  $R_L$  and  $R_C$ . The a.c. load line must be drawn through the operating point Q and the slope should correspond to the effective load resistance at the collector (figure 8.1b).

Figure 8.2 illustrates that the operating point Q is chosen in the middle of the load line. It gives the variation of the sinusoidal collector current and collector voltage corresponding to the input signal (base current). It is clear from this figure that the output signal is without distortion. If the operating shifts nearer to  $Q_2$  the output voltage and current get clipped at the positive peaks. If on the other hand the operating point shifts nearer to  $Q_1$  the clipping will at the negative peaks of the output voltage and the current. This results the distortion in the output signal which is undesirable. Thus the maximum signal that can be handled by an amplifier will be decided by the choice of the operating point. In other words we may say that the variation of the base current (signal current) should be such that operating point will not go either to the saturation region or to the cutoff region. The collector current will therefore, flow in the outer circuit for the whole of the input cycle.



**8.2 Operating Point Stability:** The operating point selected in the middle of load line should remain fixed in the amplifier circuit. But the operating point shift due to following two reasons.

- (i) **Unit to unit variation:** When a transistor is replaced by another transistor of the same type (or number), the current amplification  $\beta$  of transistor may be three times larger or smaller than the other; and if the biasing current is not capable of balancing this, the collector current as a result the collector voltage of the circuit will become different causing shift in the operating point.
- (ii) **Thermal variation:** Another important factor is the temperature variation which leads the operating point instability in the circuit. When the device temperature changes there is a variation in reverse saturation collector current  $I_{CO}$ , base to emitter voltage ( $V_{BE}$ ) and  $\beta$ . As a result of which collector current will change affecting the operating point stability. It has been observed that  $I_{CO}$  doubles for every  $10^{\circ}\text{C}$  rise in temperature,  $V_{BE}$  decreases at a rate of about  $2.5\text{ mV/deg. C}$  for both Si and Ge and also there is an increase in  $\beta$  with the increase in temperature.

There are two techniques for maintaining the operating point stability in the transistor circuits. One is called as the Bias Stabilization and the other is known as the Compensation technique. Both these techniques will be discussed in detail in following sections. The resistive biasing circuits will be used in the bias stabilization techniques that will maintain the collector current stable in spite of variation in  $I_{CO}$ ,  $\beta$  and  $V_{BE}$  with temperature or unit to unit variation. However, in the Compensation technique, the temperature sensitive devices such as diodes, transistors, thermistors etc. are used for the operating point stability.

**8.3 The Stability Factors:** Since the collector current  $I_C$  is a function of  $I_{CO}$ ,  $\beta$  and  $V_{BE}$ , so we define the three partial derivatives of  $I_C$  with respect to these variables. These derivatives are called the stability factors  $S$ ,  $S'$ ,  $S''$  and are defined as:

The stability  $S$  is defined as the rate of change of collector current with respect to the reverse saturation current, keeping  $\beta$  and  $V_{BE}$  constant.

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}$$

Here the smaller the value of  $S$  better is the stability against  $I_{CO}$ .

The stability  $S'$  is defined as the rate of change of collector current with respect to base to emitter voltage  $V_{BE}$ , keeping  $I_{CO}$  and  $\beta$  constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}$$

Similarly the variation of  $I_C$  with respect to  $\beta$  is known as stability factor

$$S'' \text{ given by } S'' = \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta}.$$

We shall now discuss the different biasing circuit and study the stability factor of each case.

**8.4 Fixed Base Bias:** The circuit diagram for the fixed base bias is shown in figure (8.4). The required voltage at the base is obtained from  $V_{CC}$  by having an excess voltage drop across  $R_B$ .

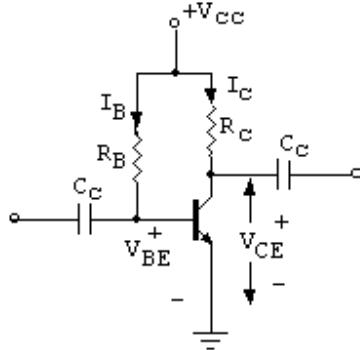


Fig. 8.4

For a CE configuration, we have the collector current as:

$$I_C = (1 + \beta)I_{CO} + \beta I_B \quad \text{----- (8.1)}$$

Applying the KVL to the input circuit, we have:

$$V_{CC} = I_B R_B + V_{BE} \quad \text{----- (8.2)}$$

or  $I_B = \frac{V_{CC} - V_{BE}}{R_B} \approx \frac{V_{CC}}{R_B} \quad \text{----- (8.3)}$

Since  $V_{CC} \gg V_{BE}$  and the change in  $V_{BE}$  will have little effect on base bias  $I_B$ . For this reason it is called as fixed base bias.

From the equations (8.1) and (8.2) we have:

$$I_C = \frac{V_{CC}}{R_B} \beta + (1 + \beta)I_{CO} \quad \text{----- (8.4)}$$

Differentiating this equation with respect to  $I_{CO}$  we get:

$$S = \frac{\partial I_C}{\partial I_{CO}} = (1 + \beta) \quad \text{----- (8.5)}$$

As  $\beta$  is always sufficiently a larger quantity, the circuit has thus a poor thermal stability. In other words it may be discussed that the fixed bias circuit is very simple to design as it has only a few components and the operating point may be fixed at the desired place just by varying the value of  $R_B$ . But with the rise of temperature the collector current increases which further rises the temperature of the device. A cumulative action takes place and the collector current goes on increasing which leads the thermal instability. The circuit provides no check on the increase in the collector current.

Further this circuit does not provide the stability against unit to unit variation. Since  $I_C = \beta I_B$ , the base current is fixed by  $R_B$  so the collector current depends only on  $\beta$ . This biasing method is thus not of practical use.

**8.5 Collector to Base Bias:** An improvement in operating point stability is possible by connecting resistance  $R_B$  between collector and base as shown in figure (8.5). This method of biasing is known as collector to base bias.

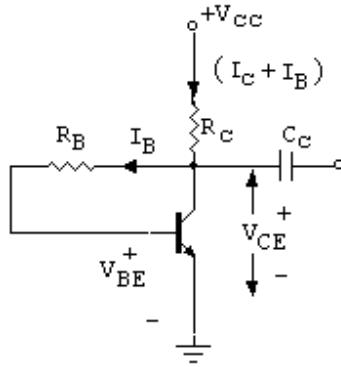


Fig. 8.5

Here, as  $I_C$  increases because of  $\beta$  or temperature,  $V_{CE}$  decreases as there is a larger drop across  $R_C$ . Hence  $I_B$  decreases which leads a decrease in  $I_C$ . Thus it gives the stability in the operating point. Let us calculate the stability factor in this case.

$$\text{We have } I_C = \beta I_B + (1+\beta) I_{CO}$$

$$\text{or } I_B = \frac{[I_C - (1+\beta) I_{CO}]}{\beta} \quad \text{----- (8.6)}$$

Applying the KVL to the input circuit, we get

$$V_{CC} = R_C (I_C + I_B) + I_B R_B + V_{BE} \quad \text{----- (8.7)}$$

From equations (8.6) and (8.7) we have

$$V_{CC} - V_{BE} = I_C R_C + \frac{(R_B + R_C)}{\beta} [I_C - (1+\beta) I_{CO}] \quad \text{----- (8.8)}$$

Differentiating this equation with respect to  $I_{CO}$ , we have

$$\frac{\partial I_C}{\partial I_{CO}} R_C + \left[ \frac{R_B + R_C}{\beta} \right] \left[ \frac{\partial I_C}{\partial I_{CO}} - (1+\beta) \right] = 0$$

$$\frac{\partial I_C}{\partial I_{CO}} \left[ R_C + \frac{(R_B + R_C)}{\beta} \right] - (1+\beta) \left[ \frac{R_B + R_C}{\beta} \right] = 0$$

$$\text{or } S = \frac{\partial I_C}{\partial I_{CO}} = \frac{[(1+\beta)(R_B + R_C)]/\beta}{[(1+\beta)R_C + R_B]/\beta}$$

$$S = \frac{[(1+\beta)(R_B + R_C)]}{[(1+\beta)R_C + R_B]} \quad \text{----- (8.9)}$$

$$\text{or } S = \frac{(1+\beta)}{\left[1 + \frac{\beta R_C}{R_B + R_C}\right]} \quad \text{----- (8.10)}$$

The stability factor  $S$  is smaller than its value for fixed base bias circuit. The improvement in operating point stability in this circuit is due to the fact that a part of the signal output is coupled back to the base through  $R_B$ , reducing thereby the voltage gain of the amplifier. The operating point stability is obtained in this case at the cost of the voltage gain.

Differentiating the equation (8.8) with respect to  $V_{BE}$ , we get the expression for stability factor  $S'$  as

$$-1 = \left[ \frac{R_B + (1+\beta)R_C}{\beta} \right] \frac{\partial I_C}{\partial V_{BE}}$$

$$\text{or } S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{[R_B + (1+\beta)R_C]}$$

This equation may further be manipulated as

$$S' = \frac{-\beta(1+\beta)(R_B + R_C)}{[R_B + (1+\beta)R_C]x(1+\beta)(R_B + R_C)}$$

$$\text{or } S' = \frac{-\beta \cdot S}{(1+\beta)(R_B + R_C)} \quad \text{----- (8.11)}$$

$$\text{where } \frac{[(1+\beta)(R_B + R_C)]}{[(1+\beta)R_C + R_B]} = S.$$

Further differentiating the equation (8.8) with respect to  $\beta$ , we may obtain the expression for stability factor  $S''$ . Rewriting the equation (8.8) we have:

$$\left[ \frac{R_B + (1+\beta)R_C}{\beta} \right] I_C = \frac{(V_{CC} - V_{BE})\beta + (R_C + R_B)(1+\beta)I_{CO}}{\beta}$$

If  $(1 + \beta)I_{CO} \approx \beta I_{CO}$  then

$$I_C = \frac{[V_{CC} - V_{BE} + (R_C + R_B)I_{CO}]\beta}{[R_B + (1+\beta)R_C]} \quad \text{----- (8.12)}$$

Now differentiating equation (8.12) with respect to  $\beta$  we may have:

$$\begin{aligned}
S'' &= \frac{\partial I_C}{\partial \beta} = \frac{[R_B + (1+\beta)R_C][V_{CC} - V_{BE} + (R_C + R_B)I_{CO}] - [V_{CC} - V_{BE} + (R_C + R_B)I_{CO}]\beta R_C}{[R_B + (1+\beta)R_C]^2} \\
&= \frac{[V_{CC} - V_{BE} + (R_C + R_B)I_{CO}][R_B + R_C + \beta R_C - \beta R_C]}{[R_B + (1+\beta)R_C]^2} \\
&= \frac{[V_{CC} - V_{BE} + (R_C + R_B)I_{CO}][R_B + R_C]}{[R_B + (1+\beta)R_C]^2} \quad \text{----- (8.13)}
\end{aligned}$$

Using the equations (8.12) and (8.13) we get:

$$S'' = \frac{I_C[R_B + R_C]}{[R_B + (1+\beta)R_C]\beta} x \frac{(1+\beta)}{(1+\beta)} \quad \text{----- (8.14)}$$

By using the equations (8.13) and (8.9) we may get the expression of  $S''$  in terms of  $S$  as:

$$S'' = \frac{I_C}{\beta} \cdot \frac{S}{(1+\beta)}$$

**8.6 Self Bias or Emitter Bias:** Another circuit that is very commonly employed is the Self bias or Emitter bias. This arrangement is shown in figure (8.6), which comprises of resistance  $R_E$  in series with the emitter across which a voltage equal to  $R_E I_E$  is dropped,

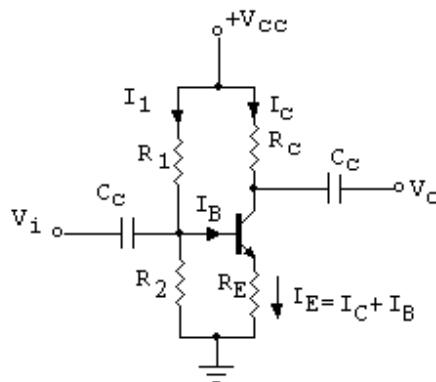


Fig. 8.6

and a potential divider consisting of  $R_1$  &  $R_2$ . The improvement in the stability of the operating point in this circuit may be explained as given below.

As the temperature is increased,  $I_{CO}$  as well  $I_C$  increases. The increase in  $I_C$  will in turn increases the voltage drop across  $R_E$ , reducing thereby the base current and hence reduction in the collector current.

The circuit may be analyzed to find the stability factors  $S$ ,  $S'$ ,  $S''$  as follows:

In the self biasing circuit, the values of resistances  $R_1$  and  $R_2$  are so chosen so that the current  $I_1$  flowing through the resistance  $R_1$  is large enough compared with  $I_B$ . The current flowing through the resistance  $R_2$  will therefore be equal to  $I_1$ . The potential drop  $V_{BB}$  across  $R_2$  will be given by:

$$V_{BB} = \frac{V_{CC} \cdot R_C}{R_1 + R_2} \quad \text{----- (8.15)}$$

The circuit can be redrawn by its Thevenin's equivalent as shown in figure (8.7).

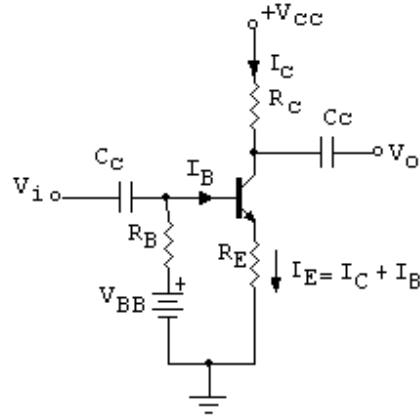


Fig. 8.7

Thevenin's resistance  $R_B$  may be obtained by shorting the supply voltage  $V_{CC}$  to ground. This resistance is given by:

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \quad \text{----- (8.16)}$$

Applying the KVL to the input circuit we get:

$$\begin{aligned} V_{BB} &= I_B R_B + V_{BE} + (I_B + I_C) R_E \\ \text{or} \quad V_{BB} - V_{BE} &= (R_B + R_E) I_B + I_C R_E \end{aligned} \quad \text{----- (8.17)}$$

The collector current is given by:

$$\begin{aligned} I_C &= \beta I_B + (1 + \beta) I_{CO} \\ \text{or} \quad I_B &= \frac{[I_C - (1 + \beta) I_{CO}]}{\beta} \end{aligned} \quad \text{----- (8.18)}$$

Using the equations (8.17) & (8.18) we get:

$$V_{BB} - V_{BE} = (R_B + R_E) \left[ \frac{I_C - (1 + \beta) I_{CO}}{\beta} \right] + I_C R_E \quad \text{----- (8.19)}$$

Differentiating the equation (8.19) with respect to  $I_{CO}$ , we may obtain the expression for the stability factor  $S$ .

$$\left[ \frac{R_B + R_E}{\beta} \right] \left[ \frac{\partial I_C}{\partial I_{CO}} - (1 + \beta) \right] + \frac{\partial I_C}{\partial I_{CO}} R_E = 0$$

or

$$\left[ \frac{R_B + R_E}{\beta} + R_E \right] \frac{\partial I_C}{\partial I_{CO}} = (1 + \beta) \frac{R_B + R_E}{\beta}$$

or

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{[(1 + \beta)(R_B + R_E)] / \beta}{[(1 + \beta)R_E + R_B] / \beta}$$

$$S = \frac{[(1 + \beta)(R_B + R_E)]}{[(1 + \beta)R_E + R_B]} \quad \text{----- (8.20)}$$

or

$$S = \frac{(1 + \beta) \left[ 1 + \frac{R_B}{R_E} \right]}{\left[ 1 + \beta + \frac{R_B}{R_E} \right]} \quad \text{----- (8.21)}$$

From this equation it is clear that the stability factor S will be equal to unity if  $\frac{R_B}{R_E}$  is small and it will be equal to  $(1 + \beta)$  if  $\frac{R_B}{R_E}$  is  $\infty$ . So smaller the value of  $R_B$ , better will be the stabilization. But if the operating is fixed for low values of  $R_B$ , the current drawn from the d.c. source  $V_{CC}$  will be large enough. That means power dissipation of the source will be larger. If  $R_E$  is increased keeping  $R_B$  constant,  $V_{CC}$  has to be increased to maintain the same value of quiescent current otherwise there will be loss of gain due to the negative feedback. So there must be compromise between the good stability and low loss of power. The resistance may also be by-passed by a large capacitance to reduce the negative feedback and to improve the stability.

Differentiating the equation (8.19) with respect to  $V_{BE}$ , we may obtain the expression for the stability factor  $S'$ .

$$-1 = \left[ \frac{R_B + (1 + \beta)R_E}{\beta} \right] \frac{\partial I_C}{\partial V_{BE}}$$

or

$$S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{[R_B + (1 + \beta)R_E]}$$

This equation may further be manipulated as

$$S' = \frac{-\beta(1 + \beta)(R_B + R_E)}{[R_B + (1 + \beta)R_E]x(1 + \beta)(R_B + R_E)}$$

or

$$S' = \frac{-\beta S}{(1 + \beta)(R_B + R_E)} \quad \text{----- (8.22)}$$

where  $\frac{[(1 + \beta)(R_B + R_E)]}{[(1 + \beta)R_C + R_B]} = S$ .

From this equation it is clear that as S is reduced,  $S'$  also reduces.

Further differentiating the equation (8.19) with respect to  $\beta$ , we may obtain the expression for stability factor  $S''$ . Rewriting the equation (8.19) we have:

$$\left[ \frac{R_B + (1+\beta)R_E}{\beta} \right] I_C = \frac{(V_{BB} - V_{BE})\beta + (R_E + R_B)(1+\beta)I_{CO}}{\beta}$$

If  $(1+\beta)I_{CO} \approx \beta I_{CO}$  then

$$I_C = \frac{[V_{BB} - V_{BE} + (R_E + R_B)I_{CO}]\beta}{[R_B + (1+\beta)R_E]} \quad \text{----- (8.23)}$$

Now differentiating equation (8.23) with respect to  $\beta$  we may have:

$$\begin{aligned} S'' &= \frac{\partial I_C}{\partial \beta} = \frac{[R_B + (1+\beta)R_E][V_{BB} - V_{BE} + (R_E + R_B)I_{CO}] - [V_{BB} - V_{BE} + (R_E + R_B)I_{CO}]\beta R_E}{[R_B + (1+\beta)R_E]^2} \\ &= \frac{[V_{BB} - V_{BE} + (R_E + R_B)I_{CO}][R_B + R_E + \beta R_E - \beta R_E]}{[R_B + (1+\beta)R_E]^2} \\ &= \frac{[V_{BB} - V_{BE} + (R_E + R_B)I_{CO}][R_B + R_E]}{[R_B + (1+\beta)R_E]^2} \end{aligned} \quad \text{----- (8.24)}$$

Using the equations (8.23) and (8.24) we get:

$$S'' = \frac{I_C[R_B + R_E]}{[R_B + (1+\beta)R_E]\beta} \times \frac{(1+\beta)}{(1+\beta)}$$

By using the equations (8.24) and (8.20), we may get the expression of  $S''$  in terms of  $S$  as:

$$S'' = \frac{I_C}{\beta} \cdot \frac{S}{(1+\beta)} \quad \text{----- (8.25)}$$

One can observe from this equation that the stability  $S''$  is a function of  $\beta$ . So if there is change in  $\beta$  due to some reason then what value of  $\beta$  should be taken in to account while calculating the stability factor  $S''$ , the initial value, final value or the average value of  $\beta$ . This type of problem does not occur in  $S$  or  $S'$ . To sort out this problem, let us calculate the change in collector current  $I_C$  due to change in  $\beta$  given by:

$$\Delta I_C = S'' \cdot \Delta \beta = \frac{S \cdot I_C}{\beta(1+\beta)} \Delta \beta$$

Now we calculate  $S''$ , by taking the ratio of the difference of  $I_C$  and the difference of  $\beta$  as:

$$S'' = \frac{I_{C2} - I_{C1}}{\beta_2 - \beta_1} = \frac{\Delta I_C}{\Delta \beta}$$

From equation (8.23), we have

$$\begin{aligned}
 \frac{I_{C2}}{I_{C1}} &= \left( \frac{\beta_2}{\beta_1} \right) \left( \frac{R_B + (1 + \beta_1)R_E}{R_B + (1 + \beta_2)R_E} \right) \\
 \text{or } \frac{I_{C2}}{I_{C1}} - 1 &= \left( \frac{\beta_2}{\beta_1} \right) \left( \frac{R_B + (1 + \beta_1)R_E}{R_B + (1 + \beta_2)R_E} \right) - 1 \\
 \text{or } \frac{I_{C2} - I_{C1}}{I_{C1}} &= \left( \frac{\beta_2 - \beta_1}{\beta_1} \right) \left( \frac{R_B + R_E}{R_B + (1 + \beta_2)R_E} \right) \\
 \text{or } S' &= \frac{\Delta I_C}{\Delta \beta} = \left( \frac{I_{C1}}{\beta_1} \right) \left( \frac{R_B + R_E}{R_B + (1 + \beta_2)R_E} \right) \\
 \text{or } S' &= \left( \frac{I_{C1}}{\beta_1} \right) \left( \frac{S_2}{(1 + \beta_2)} \right)
 \end{aligned} \tag{8.26}$$

Where  $S_2$  is the value of  $S$  for  $\beta = \beta_2$  given by  $S_2 = \frac{[(1 + \beta)(R_B + R_E)]}{[(1 + \beta)R_E + R_B]}$

If  $\Delta\beta \rightarrow 0$  so that  $I_{C1} \approx I_{C2}$ , then equation (8.26) reduces to

$$S' = \frac{I_C}{\beta} \cdot \frac{S}{(1 + \beta)}, \text{ which is the same as equation (8.25).}$$

Equation (8.26) signifies that the maximum value of  $S_2$  can be determined, for a given span of  $\beta$  and a given value of  $I_{C1}$ . The variation in  $\beta$  may be due to the temperature variation or unit to unit variation of the transistor.

**Example 8.1:** Show that  $S$  for self biasing circuit may be put in the form

$$S = \frac{G_E + G_1 + G_2}{\left[ \frac{G_E}{(1 + \beta)} + G_1 + G_2 \right]} \quad \text{where the } G's \text{ are conductances}$$

corresponding to the  $R$ 's used in self biasing circuit.

**Solution:** The stability factor  $S$  for self biasing circuit is given by equation (8.20), which is rewritten here.

$$S = \frac{[(1 + \beta)(R_B + R_E)]}{[(1 + \beta)R_E + R_B]} \tag{8.27}$$

$$\text{where } R_B = \frac{R_1 R_2}{R_1 + R_2} \quad \text{or} \quad \frac{1}{R_B} = \frac{1}{R_1} + \frac{1}{R_2} = G_1 + G_2 \tag{8.28}$$

$$\text{and } G_E = \frac{1}{R_E} \tag{8.29}$$

Using the equations (8.27) to (8.29) we have:

$$S = \frac{[(1+\beta)R_B(1+\frac{R_E}{R_B})]}{[(1+\beta)\frac{R_E}{R_B}+1]R_B}$$

$$S = \frac{(1+\beta)[1+\frac{1}{G_E}(G_1+G_2)]}{[1+\frac{(1+\beta)}{G_E}(G_1+G_2)]}$$

or  $= \frac{(1+\beta)[G_E + G_1 + G_2]}{[G_E + (1+\beta)(G_1 + G_2)]}$

or  $S = \frac{G_E + G_1 + G_2}{\left[ \frac{G_E}{(1+\beta)} + G_1 + G_2 \right]}$  Hence proved.

**Example 8.2:** For the two battery transistor circuit shown in figure (8.8), prove that the stabilization factor  $S$  is given by:

$$S = \frac{1+\beta}{1+\beta \frac{R_E}{(R_E + R_B)}}$$

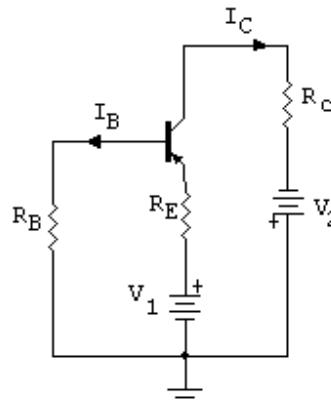


Fig. 8.8

**Solution:** Applying the KVL to the input circuit we get:

$$V_1 - V_{BE} = I_B R_B + I_B R_E + R_E I_C$$

or  $V_1 - V_{BE} = I_B (R_B + R_E) + R_E I_C$  ----- (8.30)

The collector current is given by:

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$\text{or } I_B = \frac{[I_C - (1 + \beta)I_{CO}]}{\beta} \quad \text{----- (8.31)}$$

From equations (8.30) & (8.31), we have

$$V_1 - V_{BE} = \left[ \frac{I_C - (1 + \beta)I_{CO}}{\beta} \right] (R_B + R_E) + R_E I_C \quad \text{----- (8.32)}$$

Differentiating the equation (8.32) with respect to  $I_{CO}$ , we may obtain the expression for the stability factor  $S$ .

$$\frac{\partial I_C}{\partial I_{CO}} R_E - \frac{(R_E + R_B)(1 + \beta)}{\beta} + \frac{(R_B + R_E)}{\beta} \frac{\partial I_C}{\partial I_{CO}} = 0$$

$$\frac{(1 + \beta)R_E + R_B}{\beta} S = \frac{(1 + \beta)(R_E + R_B)}{\beta}$$

$$\text{or } S = \frac{(1 + \beta)(R_E + R_B)}{[R_B + R_E + \beta R_E]}$$

$$\text{or } S = \frac{1 + \beta}{1 + \beta \frac{R_E}{(R_E + R_B)}} \quad \text{Hence proved.}$$

**Example 8.3:** In the transformer coupled amplifier shown in figure (8.9),

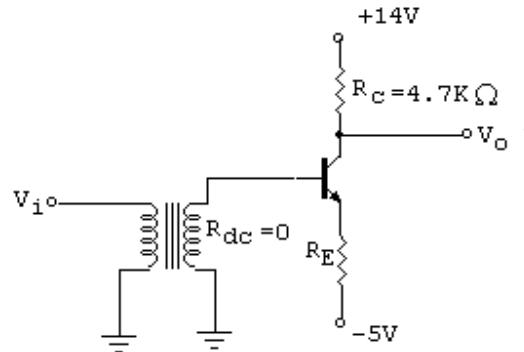


Fig. 8.9

$V_{BE} = 0.7$  volt,  $\beta = 45$  and  $V_{CE} = 4$  volts. Determine  $R_E$  and stability factor  $S$ .

**Solution:** Applying the KVL to the output circuit we get:

$$14 + 5 \approx 4.7K \cdot I_C + 4 + R_E \cdot I_C$$

$$\text{or } (4.7K + R_E)I_C = 15V$$

Applying KVL to the input circuit we get:

$$V_{BE} + R_E I_C - 5V = 0$$

or  $0.7 + I_C R_E = 5V$

or  $I_C R_E = 4.3V$

Solving for  $R_E$  and  $I_C$ , we have  $I_C = 2.28 \text{ mA}$  and  $R_E = 1.9 \text{ K}\Omega$ .

The given circuit is the Thevenin's equivalent of the self biasing circuit with  $R_B = 0$ .

The stability factor S is given by:

$$S = \frac{1 + \beta}{\frac{R_E}{1 + \beta \frac{R_E}{(R_E + R_B)}}}$$

Putting the value of  $R_B = 0$ , we get  $S = 1$ .

**Example 8.4:** Assume that a Silicon transistor with  $\beta = 45$ ,  $V_{BE} = 0.7 \text{ V}$ ,  $V_{CC} = 24 \text{ V}$  and  $R_C = 5 \text{ K}\Omega$  is used in self biasing CE amplifier. It is desired to establish a Q point at  $V_{CE} = 14 \text{ V}$  and  $I_C = 1.7 \text{ mA}$  and stability factor  $S \leq 4$ . Find the values of  $R_E$ ,  $R_L$  and  $R_2$ .

Solution: The current in  $R_E$  is  $I_E \approx I_C = 1.7 \text{ mA}$

Applying the KVL to the output circuit we have,

$$24V = (5K + R_E)1.7mA + 14V$$

or  $5K + R_E = \frac{10}{1.7} \text{ K}\Omega = 5.88 \text{ K}\Omega$

or  $R_E = 0.88 \text{ K}\Omega$

The stability factor S is given by:

$$S = \frac{(1 + \beta) \left[ 1 + \frac{R_B}{R_E} \right]}{\left[ 1 + \beta + \frac{R_B}{R_E} \right]}$$

$$4 = 46 \frac{1 + \frac{R_B}{R_E}}{46 + \frac{R_B}{R_E}}$$

or  $4 \times 46 + 4 \frac{R_B}{R_E} = 46 + 46 \frac{R_B}{R_E}$

or  $\frac{R_B}{R_E} = 3.29$

$$\text{or } R_B = 3.29 \times 0.88 K\Omega = 2.9 K\Omega$$

Applying the KVL to the input circuit, we get

$$V_{BB} = R_B I_B + V_{BE} + R_E I_C$$

$$I_B = \frac{I_C}{\beta} = \frac{1.7mA}{45} = 37.8\mu A$$

$$\begin{aligned} \text{or } V_{BB} &= 2.9 \times 10^3 \times 37.8 \times 10^{-6} + 0.7 + 0.88 \times 10^3 \times 1.7 \times 10^{-3} \\ &= 2.31V \end{aligned}$$

$$\begin{aligned} \text{Further } V_{BB} &= \frac{V_{CC}xR_2}{R_1 + R_2} \quad \text{and} \quad R_B = \frac{R_1xR_2}{R_1 + R_2} \\ 2.31 &= \frac{14xR_2}{R_1 + R_2} \quad \text{or} \quad \frac{R_2}{R_1 + R_2} = \frac{2.31}{14} = 0.165 \\ R_1 &= \frac{2.9K}{0.165} = 17.6K\Omega \quad \text{and} \quad R_2 = 3.48K\Omega \end{aligned}$$

**Variation of Operating Point Stability with Simultaneous Variation of  $I_{CO}$ ,  $V_{BE}$  and  $\beta$ :** We have defined the stability factors  $S$ ,  $S'$ , and  $S''$  as the partial derivatives of  $I_C$  with  $I_{CO}$ ,  $V_{BE}$  and  $\beta$  respectively. Each partial derivatives is calculated when all other parameters are held constant. The collector current is a function of  $I_{CO}$ ,  $V_{BE}$  and  $\beta$  as

$$I_C = f(I_{CO}, V_{BE}, \beta)$$

The total change in collector current due to the simultaneous variation in  $I_{CO}$ ,  $V_{BE}$  and  $\beta$  may be given as

$$\begin{aligned} \Delta I_C &= \frac{\partial I_C}{\partial I_{CO}} \cdot \Delta I_{CO} + \frac{\partial I_C}{\partial V_{BE}} \cdot \Delta V_{BE} + \frac{\partial I_C}{\partial \beta} \cdot \Delta \beta \\ &= S \cdot \Delta I_{CO} + S' \cdot \Delta V_{BE} + S'' \cdot \Delta \beta \end{aligned} \quad \text{----- (8.33)}$$

The stability factor  $S$ ,  $S'$ , and  $S''$  may be expressed in terms of parameter  $M$  defined by

$$M = \frac{1}{1 + \frac{R_B}{[R_E(1+\beta)]}}$$

$$S = \frac{[(1+\beta)(R_B + R_E)]}{[(1+\beta)R_E + R_B]} = \frac{(1+\beta)R_E(1 + \frac{R_B}{R_E})}{(1+\beta)R_E[1 + \frac{R_B}{R_E(1+\beta)}]} = (1 + \frac{R_B}{R_E})M \quad \text{----- (8.34)}$$

$$S' = \frac{-\beta \cdot S}{(1+\beta)(R_B + R_E)} = \frac{-\beta M (R_B + R_E)}{(1 + \beta)(R_B + R_E)R_E} = \frac{-M}{R_E} \quad \text{----- (8.35)}$$

(Provided  $\beta \gg 1$ )

$$\text{and } S'' = \left( \frac{I_{C1}}{\beta_1} \right) \left( \frac{S_2}{(1 + \beta_2)} \right) = \frac{I_{C1}}{\beta_1} \frac{M_2 (1 + \frac{R_B}{R_E})}{(1 + \beta_2)} \approx (1 + \frac{R_B}{R_E}) \frac{I_{C1} M_2}{\beta_1 \beta_2} \quad \dots \quad (8.36)$$

(Provided  $\beta \gg 1$  and  $M_2$  is the value of  $M$  for  $\beta = \beta_2$ )

Putting the values of  $S$ ,  $S'$ , and  $S''$  from equations (8.34) to (8.35) in equation (8.33), we get the fractional change in collector current as:

$$\frac{\Delta I_C}{I_{C1}} = \left( 1 + \frac{R_B}{R_E} \right) \frac{M_1 \Delta I_{CO}}{I_{C1}} - \frac{M_1 \Delta V_{BE}}{I_{C1} R_E} + \left( 1 + \frac{R_B}{R_E} \right) \frac{M_2 \Delta \beta}{\beta_1 \beta_2} \quad \dots \quad (8.37)$$

Once  $\Delta I_C$  is known,  $\Delta V_{CE}$  is obtained from the d.c. load line.

The range of temperature over which a transistor is operated is normally  $-65^0\text{C}$  to  $+75^0\text{C}$  for Germanium transistor and  $-65^0\text{C}$  to  $+175^0\text{C}$  for Silicon transistor. Table 8.1 illustrates the typical parameters for both Silicon and Germanium transistors for their respective temperature range of operation. It is of significance to study the order of  $\Delta I_C$  due to the change in  $I_{CO}$ ,  $V_{BE}$  and  $\beta$  over the temperature range of operation.

Table : 8.1

Parameters	Silicon Transistor			Germanium Transistor		
	$-65^0\text{C}$	$+25^0\text{C}$	$+175^0\text{C}$	$-65^0\text{C}$	$+25^0\text{C}$	$+75^0\text{C}$
$I_{CO}$	$1.95 \times 10^{-3} \text{nA}$	$1.0 \text{nA}$	$33000 \text{nA}$	$1.95 \times 10^{-3} \mu\text{A}$	$1.0 \mu\text{A}$	$32 \mu\text{A}$
$\beta$	25	55	100	20	55	90
$V_{BE}(\text{volts})$	0.78	0.6	0.225	0.38	0.2	0.1

It may clearly be seen from this table that at room temperature ( $25^0\text{C}$ ) both Si and Ge transistors have the same value of  $\beta$ . For Si  $I_{CO}$  is much smaller than Ge. However,  $I_{CO}$  approximately doubles for every  $10^0\text{C}$  and  $V_{BE}$  decreases by approximately  $2.5 \text{ mV}/{}^0\text{C}$  rise in temperature.

Making use of the parameters given in table (8.1) and equation (8.37), one can easily find that the change in collector current for both Si and Ge transistors for their respective range of temperature. The study reveals that the collector current variation for  $240^0\text{C}$  change of temperature for Si transistor is approximately same for  $140^0\text{C}$  change of temperature for Ge transistor. This means that the variation of collector current due to temperature is more for Ge transistor than that of Si. Hence the Si transistor is superior. However, for Si the influence of  $V_{BE}$  is more significant than that of  $I_{CO}$  on collector current.

**Example 8.5 :** For the self bias CE transistor (Ge) amplifier has the following values  $R_E = 4.5 \text{ K}\Omega$ ,  $R_1 = 90 \text{ K}\Omega$ ,  $R_2 = 10 \text{ K}\Omega$ . The collector supply voltage and collector resistance  $R_C$  are adjusted so as to give the collector current of  $1.5 \text{ mA}$  at  $25^\circ\text{C}$ . Determine the variation of collector current in the temperature range  $+25^\circ\text{C}$  to  $+75^\circ\text{C}$ , when the Ge transistor of table 8.1 is used.

Solution: The resistance  $R_B$  is given by:  $R_B = \frac{R_1 \times R_2}{R_1 + R_2} = \frac{90 \times 10}{100} = 9 \text{ K}\Omega$

The ratio  $\frac{R_B}{R_E} = \frac{9 \text{ K}\Omega}{4.5 \text{ K}\Omega} = 2$

At room temperature  $M_1 = \frac{1}{1 + \frac{R_B}{[R_E(1 + \beta)]}} = \frac{1}{1 + \frac{2}{56}} \approx 1$

The stability factor  $S$  at room temperature ( $+25^\circ\text{C}$ ) is given by:

$$S (\text{at } +25^\circ\text{C}) = \left(1 + \frac{R_B}{R_E}\right) M_1 = 3$$

The stability factor  $S'$  is given by:

$$S' (\text{at } +25^\circ\text{C}) = \frac{-M}{R_E} = -\frac{1}{4.5} \text{ mA/V} = -0.22 \text{ mA/V}$$

The stability factor  $S''$  is given by

$$S'' (\text{at } +75^\circ\text{C}) = \left(1 + \frac{R_B}{R_E}\right) \frac{I_{C1} M_2}{\beta_1 \beta_2} = \frac{(1+2) \times 1.5 \times 10^{-3} \times 1}{55 \times 90} = 0.91 \times 10^{-6} \text{ mA}$$

where  $M_2$  is also approximately equal to unity.

The change in  $I_C$  in the temperature range from  $(+25^\circ\text{C}$  to  $+75^\circ\text{C})$  is obtained as:

$$\begin{aligned} \Delta I_C &= S \cdot \Delta I_{CO} + S' \cdot \Delta V_{BE} + S'' \Delta \beta \\ &= 3 \times 31 \times 10^{-6} + (-0.22 \times 10^{-3})(-0.1) + (0.91 \times 10^{-6})(35) \\ &= 0.147 \text{ mA} \end{aligned} \quad (35)$$

**8.8 Bias Compensation:** For the proper use of transistor as amplifier it has earlier been discussed that it is to be biased in the active region. The operating point should be made stable against the variation of temperature. The resistive biasing circuits have been used for stabilization techniques that maintain the collector current stable in spite of variation in  $I_{CO}$ ,  $\beta$  and  $V_{BE}$  with temperature or unit to unit variation. However, in the Compensation technique, the temperature sensitive devices such as diodes, transistors, thermistors etc. are introduced that compensate the change of  $V_{BE}$  or  $I_{CO}$  in the circuits.

**8.8.1 Diode Compensation for  $V_{BE}$ :** Figure (8.10) illustrates the self biasing circuit having the diode  $D$  connected in the emitter circuit as the compensating element. This diode  $D$  is biased in the forward direction by a voltage source  $V_{DD}$  through a resistance  $r_d$ .

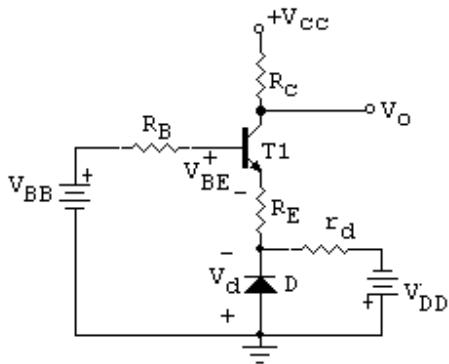


Fig.8.10

Further it is assumed that the diode  $D$  and the transistor  $T_1$  are made up of the same material and same type. The voltage drop across the diode  $V_d$  and the voltage across the emitter base junction  $V_{BE}$  will therefore have the same temperature coefficient.

Applying the KVL to the input circuit, we have:

$$-V_{BB} + R_B I_B + V_{BE} + R_E (I_C + I_B) - V_d = 0$$

$$\text{or } (V_{BB} - V_{BE} + V_d) = R_E I_C + (R_B + R_E) I_B \quad \dots\dots (8.38)$$

$$\text{But } I_C = \beta I_B + (1 + \beta) I_{CO}$$

$$\text{or } I_B = \frac{I_C - (1 + \beta) I_{CO}}{\beta} \quad \dots\dots (8.39)$$

Substituting the value of  $I_B$  from equation (8.38) in equation (8.39), we get

$$(V_{BB} - V_{BE} + V_d) = R_E I_C + (R_B + R_E) \left[ \frac{I_C - (1 + \beta) I_{CO}}{\beta} \right]$$

$$\beta [V_{BB} - (V_{BE} - V_d)] + I_{CO} (R_B + R_E) (1 + \beta) = I_C [R_B + R_E + \beta R_E]$$

$$\text{or } I_C = \frac{\beta [V_{BB} - (V_{BE} - V_d)] + I_{CO} (R_B + R_E) (1 + \beta)}{R_B + R_E (1 + \beta)} \quad \dots\dots (8.40)$$

From the equation (8.40), it is clear that since the variation in  $V_{BE}$  and  $V_d$  is the same as both are made of the same material and type, the factor  $(V_{BE} - V_d)$  will remain to be constant. That is the change in  $V_{BE}$  is compensated by the change in  $V_d$  by almost the same amount. Hence  $I_C$  will be insensitive to the variations in  $V_{BE}$ . Although this compensation is not perfect but it is sufficiently effective to take care the transistor drift due to the variations in  $V_{BE}$ . This compensation technique is generally used in Silicon transistors as the change of  $V_{BE}$  has dominating effect in the variation of  $I_C$ .

**8.8.2 Diode Compensation for  $I_{CO}$ :** The diode compensation for  $I_{CO}$  is useful for stabilizing the Germanium transistors as the variation of  $I_{CO}$  with temperature is quite large in these transistors. Figure (8.11) illustrates the circuit of Germanium transistor

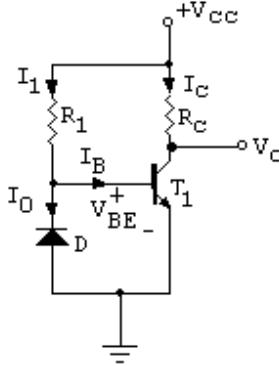


Fig. 8.11

amplifier in which a diode D is connected between emitter and the base of the transistor. If the diode and the transistor are made up of the same material and the type, the reverse saturation current  $I_0$  of the diode will increase with temperature at the same rate as the transistor collector saturation current  $I_{CO}$ .

From the figure (8.11), we get

$$I_1 = \frac{V_{CC} - V_{BE}}{R_1}$$

Since the diode is reverse biased by an amount  $V_{BE} \approx 0.2$  volt for Germanium devices, so

$$I_1 \approx \frac{V_{CC}}{R_1} = \text{Constant}$$

The base current is given by:

$$I_B = I_1 - I_0 \quad \text{----- (8.41)}$$

But we have the collector current  $I_C$  as:

$$I_C = \beta I_B + (1 + \beta) I_{CO} \quad \text{----- (8.42)}$$

Substituting the value of  $I_B$  from equation (8.41) in equation (8.42) we have:

$$I_C = \beta I_1 - \beta I_0 + (1 + \beta) I_{CO}$$

If  $\beta \gg 1$ , then

$$I_C \approx \beta I_1 - \beta I_0 + \beta I_{CO}$$

From this equation it is clear that if the diode and the transistor T1 are made up of same material and type, the variation of  $I_0$  and  $I_{CO}$  will be nullified and the collector current will remain to be essentially constant over the entire range of temperature.

**Example 8.6:** For the biasing arrangement shown in figure (8.11) and assuming that the reverse saturation currents of the diode and transistor are equal, prove that

$$S = 1$$

$$S' = -\frac{\beta}{R_1}$$

$$S'' = \frac{\Delta(I_C - I_{CO})}{\Delta\beta} = \frac{I_{C1} - I_{CO1}}{\beta_1}$$

Solution: We have

$$I_1 = \frac{V_{CC} - V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1} = \text{constant}$$

$$\text{and } I_C = \beta I_B + (1 + \beta) I_{CO}$$

$$I_B = I_1 - I_0$$

where  $I_0$  is the reverse saturation current of the diode.

$$\begin{aligned} \text{or } I_C &= \beta I_1 - \beta I_0 + (1 + \beta) I_{CO} \\ &= \beta I_1 - \beta I_0 + I_{CO} + \beta I_{CO} \end{aligned}$$

Since  $I_{CO} = I_0$  so we have

$$I_C = \beta I_1 + I_{CO} \quad \text{----- (8.43)}$$

Differentiating this equation with respect to  $I_{CO}$ , we get

$$\frac{\partial I_C}{\partial I_{CO}} = 0 + 1$$

$$\text{or } S = \frac{\partial I_C}{\partial I_{CO}} = 1 \quad \text{Proved part I}$$

Equation (8.43) may be rewritten:

$$I_C = \frac{\beta}{R_1} (V_{CC} - V_{BE}) + I_{CO}$$

Differentiating this equation with respect to  $V_{BE}$ , we get

$$\frac{\partial I_C}{\partial V_{BE}} = -\frac{\beta}{R_1}$$

$$\text{or } S' = \frac{\partial I_C}{\partial V_{BE}} = -\frac{\beta}{R_1} \quad \text{Proved part II}$$

Equation (8.43) may be rewritten as

$$I_C - I_{CO} = \beta I_1$$

$$\begin{aligned}
 \text{or} \quad & I_{C2} - I_{CO2} = \beta_2 I_1 \\
 \text{and} \quad & I_{C1} - I_{CO1} = \beta_1 I_1 \\
 \text{or} \quad & \frac{I_{C2} - I_{CO2}}{I_{C1} - I_{CO1}} - 1 = \frac{\beta_2}{\beta_1} - 1 \\
 \text{or} \quad & \frac{\Delta I_C - \Delta I_{CO}}{I_{C1} - I_{CO1}} = \frac{\beta_2 - \beta_1}{\beta_1} \\
 \text{or} \quad & \frac{\Delta(I_C - I_{CO})}{\Delta\beta} = \frac{I_{C1} - I_{CO1}}{\beta_1} \\
 S'' = & \frac{\Delta(I_C - I_{CO})}{\Delta\beta} = \frac{I_{C1} - I_{CO1}}{\beta_1} \quad \text{Proved part III}
 \end{aligned}$$

**8.9 Thermistor and Sensistor Compensation:** In this compensation technique, the temperature sensitive element such as a thermistor or a sensistor is used rather than diode.

**8.9.1 Thermistor Compensation:** Figure (8.12) shows the self-bias CE transistor amplifier with thermistor compensation. Thermistor has a negative temperature

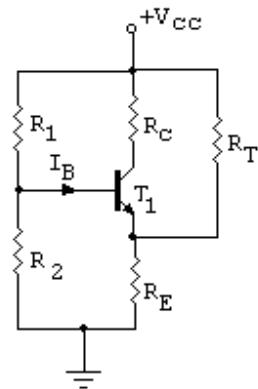


Fig. 8.12

coefficient of resistance i.e. its resistance decreases with the increase of temperature. Thermistor  $R_T$  connected between emitter and the positive supply compensate the variation of  $I_C$  with  $I_{CO}$ ,  $V_{BE}$  or  $\beta$  caused due to the variation in temperature. As the temperature increases the resistance of  $R_T$  decreases, the current flowing through  $R_T$  in to  $R_E$  increases. Since voltage across  $R_E$  is in the direction to reverse bias the emitter base junction of the transistor, the increase in temperature will reduce the net forward bias of the emitter junction and as a result the collector current will remain fairly constant.

An alternative configuration using thermistor compensation is shown in Figure (8.13), in which the thermistor  $R_T$  is placed in parallel with  $R_2$ . As the temperature

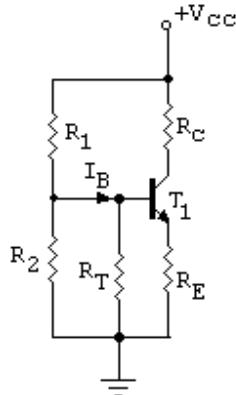


Fig. 8.13

increases,  $R_T$  decreases also the drop across  $R_T$  decreases. This results the decrease in collector current. This reduced  $I_C$  tends to compensate for the increased collector current caused by the rise in temperature.

**8.9.2 Sensistor Compensation:** For the operating point stability of the transistor, sensistor which has the positive temperature coefficient of resistance may be used as the compensating element instead of thermistor. The sensistor is placed either in parallel with  $R_1$  or in parallel with  $R_E$  or in place of  $R_E$  in the self bias circuit. This may be explained that the net voltage drop across  $R_2$  increases reducing thereby the collector current.

**8.10 Thermal Runaway:** In transistor amplifier, one must control the biasing of the transistor in such a way as to keep the average dissipation of the device below its maximum value. The amplifier design leads the operating point to shift with temperature in such a way as to burn out the transistor. The biasing problem is aggravated by an effect known as Thermal Runaway, which may be explained as follows. The collector-base junction of the transistor, where all of the dissipation occurs, is not in perfect contact with the transistor case. That is, there is some thermal resistance between the junction and the case, and between the case and ambient. Thus the power dissipated in the transistor will heat the junction to a temperature considerably above the ambient. The internal increase in temperature will cause a change in the transistor characteristics which in turn increases the power dissipation and the internal temperature. This cyclic chain of events will cause the rapid rise in transistor temperature and finally result the destruction of the transistor, known as thermal runaway. The power dissipation can be controlled and hence the thermal runaway be prevented, if the biasing arrangement is designed to keep the operating point approximately fixed in the  $V_{CE}$  –  $I_C$  plane.

**8.10.1 Thermal Resistance:** Let  $T_J$  is the temperature of the collector base junction and  $T_A$  is the ambient temperature of the transistor. Here  $T_J > T_A$  due to heating within the transistor. It has been observed that:

$$(T_J - T_A) \propto P_D$$

Where  $P_D$  is the power dissipated in the transistor.

$$\text{or } (T_J - T_A) = \Theta P_D \quad \text{----- (8.44)}$$

$\Theta$  is the proportionality constant and is called as thermal resistance given in  $^{\circ}\text{C}/\text{watt}$ .

$$\text{or } T_J = T_A + \Theta P_D$$

The collector junction temperature  $T_J$  is higher than the ambient temperature  $T_A$  by an amount equal to the product of thermal resistance  $\Theta$  and power dissipation  $P_D$  in the transistor.

The value of the thermal resistance  $\Theta$  depends upon

1. the size of the transistor,
2. convection and radiation,
3. on the nature of the cooling like forced air colling, and
4. the thermal connection of the device to the metal chassis or a heat sink.

Typical values for various transistor designs vary from  $0.2 \ ^{\circ}\text{C}/\text{watt}$  for high power transistor fitted with a suitable heat sink to  $100 \ ^{\circ}\text{C}/\text{watt}$  for a low power transistor which has no cooling arrangement.

The maximum collector power  $P_C$  permitted for a transistor for safe operation at  $25 \ ^{\circ}\text{C}$  (room temperature) is specified by the manufacturer. For ambient temperatures above this value, the maximum permissible value reduces. The  $P_C$  reduces to zero at the temperature at which the transistor may operate, that is this value is  $100 \ ^{\circ}\text{C}$  for Ge transistor and  $225 \ ^{\circ}\text{C}$  for Si transistor as shown in figure (8.14).

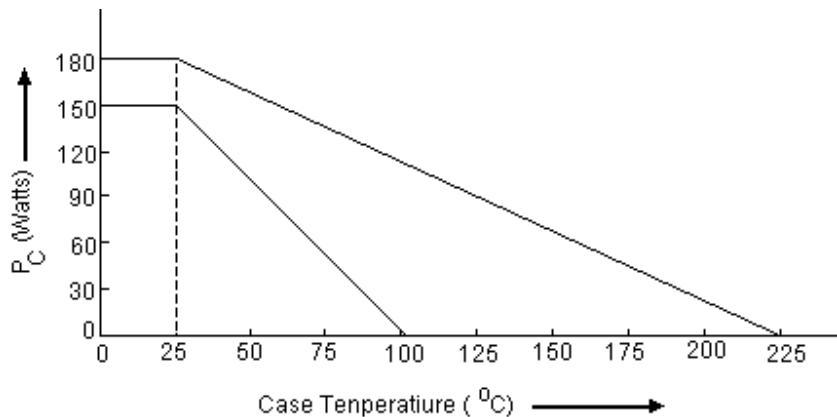


Fig. 8.14

**8.10.2 Condition to Prevent Thermal Runaway:** The condition to avoid the thermal runaway is that the rate at which heat is released at the collector junction must not exceed the rate at which heat can be dissipated i.e.

$$\frac{\partial P_C}{\partial T_J} < \frac{\partial P_D}{\partial T_J} \quad \text{----- (8.45)}$$

Differentiating equation (8.44) with respect to  $T_J$ , we have

$$1 = \Theta \frac{\partial P_D}{\partial T_J}$$

or  $\frac{\partial P_D}{\partial T_J} = \frac{1}{\Theta}$  ----- (8.46)

From equations (8.45) and (8.46), we get

$$\frac{\partial P_C}{\partial T_J} < \frac{1}{\Theta} \quad \text{----- (8.47)}$$

To prevent the thermal runaway in the transistor this condition must be satisfied.

**8.10.3 Thermal Stability:** It is well known that the transistor is to be biased in the active region for the transistor to work as an amplifier. The power generated at the collector junction with no signal is given by:

$$P_C = I_C V_{CE} \approx I_C V_{CE} \quad \text{----- (8.48)}$$

If we assume that the quiescent collector current almost equals the emitter current, then equation (8.48) can be written as:

$$\begin{aligned} P_C &= I_C [V_{CC} - I_C (R_E + R_C)] \\ &= I_C V_{CC} - I_C^2 (R_E + R_C) \end{aligned} \quad \text{----- (8.49)}$$

The condition (equation 8.47) to prevent the thermal runaway is rewritten as:

$$\frac{\partial P_C}{\partial I_C} \cdot \frac{\partial I_C}{\partial T_J} < \frac{1}{\Theta} \quad \text{----- (8.50)}$$

Here  $\Theta$  and  $\frac{\partial I_C}{\partial T_J}$  are positive, hence equation (8.50) is always satisfied when  $\frac{\partial P_C}{\partial I_C}$  is negative. Differentiating equation (8.49) with respect to  $I_C$  we get,

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C (R_E + R_C) \quad \text{----- (8.51)}$$

Hence to prevent the thermal runaway the right hand side of the equation (8.51) should be negative. That is

$$I_C > \frac{V_{CC}}{2(R_E + R_C)} \quad \text{----- (8.52)}$$

$$\text{But } V_{CE} = V_{CC} - I_C(R_E + R_C)$$

So the equation (8.52) implies that

$$V_{CE} < \frac{V_{CC}}{2} \quad \text{----- (8.53)}$$

If  $I_C$  is not greater than  $\frac{V_{CC}}{2(R_E + R_C)}$  and  $V_{CE} > \frac{V_{CC}}{2}$  then  $\frac{\partial P_C}{\partial I_C}$  is positive; and thus the thermal runaway is not prevented. To ensure that the thermal runaway does not occur, the equation (8.50) should be satisfied.

It is well known that  $I_C$  depends on the variation of  $I_{CO}$ ,  $V_{BE}$  and  $\beta$  due to the junction temperature  $T_J$ .

Hence

$$\begin{aligned} \Delta I_C &= \frac{\partial I_C}{\partial I_{CO}} \Delta I_{CO} + \frac{\partial I_C}{\partial V_{BE}} \Delta V_{BE} + \frac{\partial I_C}{\partial \beta} \Delta \beta \\ \frac{\partial I_C}{\partial T_J} &= \frac{\partial I_C}{\partial I_{CO}} \cdot \frac{\partial I_{CO}}{\partial T_J} + \frac{\partial I_C}{\partial V_{BE}} \cdot \frac{\partial V_{BE}}{\partial T_J} + \frac{\partial I_C}{\partial \beta} \cdot \frac{\partial \beta}{\partial T_J} \\ \frac{\partial I_C}{\partial T_J} &= S \cdot \frac{\partial I_{CO}}{\partial T_J} + S' \cdot \frac{\partial V_{BE}}{\partial T_J} + S'' \cdot \frac{\partial \beta}{\partial T_J} \end{aligned} \quad \text{----- (8.54)}$$

For a given transistor,  $\frac{\partial I_{CO}}{\partial T_J}$ ,  $\frac{\partial V_{BE}}{\partial T_J}$  and  $\frac{\partial \beta}{\partial T_J}$  are known and thus by selecting the values of  $S$ ,  $S'$  and  $S''$  equation (8.50) may be satisfied.

In some practical problems the effect of  $I_{CO}$  dominates, the term  $\frac{\partial I_{CO}}{\partial T_J}$  in equation (8.54) also dominates and the problem of thermal runaway may be analyzed as follows. From the equations (8.50) and (8.54) we have:

$$\frac{\partial P_C}{\partial I_C} \left[ S \frac{\partial I_{CO}}{\partial T_J} \right] < \frac{1}{\Theta} \quad \text{----- (8.55)}$$

Here we neglected all the terms on right hand side of equation (8.54) except first.

It is well known that for both Ge and Si transistors the reverse saturation current  $I_{CO}$  increases by 7 percent/°C i.e.,

$$\frac{\partial I_{CO}}{\partial T_J} = 0.07 I_{CO} \quad \text{----- (8.56)}$$

Putting the value of  $\frac{\partial P_C}{\partial I_C}$  from (8.51) and the value of  $\frac{\partial I_{CO}}{\partial T_J}$  from equation (8.56) in equation (8.55) we have:

$$[V_{CC} - 2I_C(R_E + R_C)][S(0.07I_{CO})] < \frac{1}{\Theta} \quad \text{----- (8.57)}$$

This equation gives the necessary condition for avoiding thermal runaway and is valid for any NPN transistor. It can also be valid for any PNP transistor if  $I_C$  and  $I_{CO}$  are used to represent the magnitudes of the current.

Equation (8.57) shows that amplifiers operated at low currents and used for stability factor  $S < 10$  are almost free from thermal runaway. On the other hand, power amplifiers operating at high power levels use  $R_E$  of low value, resulting high value of stability factor  $S$ . Thus in power amplifiers, thermal runaway is the common problem and care must be taken in the design of power amplifiers to prevent the thermal runaway.

**Example 8.7:** What will be the temperature of the junction if the transistor dissipates 2.5 watt of power? Given for a transistor  $\Theta = 12 \text{ }^{\circ}\text{C}/\text{watt}$  and working in an ambient temperature of  $25 \text{ }^{\circ}\text{C}$ .

Solution: We have

$$\begin{aligned} T_J &= T_A + \Theta P_D \\ &= 25 + 12 \times 2.5 = 55 \text{ }^{\circ}\text{C} \end{aligned}$$

**Example 8.8 :** Find the maximum permissible value of thermal resistance  $\Theta$  required for a transistor so that the circuit is thermally stable. Given that  $V_{CC} = 24$  volts,  $V_{CE} = 15$  volts  $R_C = 5 \text{ K}\Omega$ ,  $R_E = 1.5 \text{ K}\Omega$ ,  $I_C = 1.5 \text{ mA}$  and stability factor  $S = 8$ . Assume  $I_{CO} = 2.0 \text{ nA}$  at  $25 \text{ }^{\circ}\text{C}$ .

Solution:  $\frac{V_{CC}}{2} = \frac{24}{2} = 12 \text{ volts}$

and  $V_{CE} = 15 \text{ volts}$

Since  $V_{CE} > (V_{CC} / 2)$ , the circuit is not stable. The condition to prevent thermal runaway is

$$[V_{CC} - 2I_C(R_E + R_C)][S(0.07I_{CO})] < \frac{1}{\Theta}$$

$$\text{or } [24 - 2 \times 1.5 \text{ mA} (1.5 + 5) \text{ K}\Omega][8(0.07 \times 2 \times 10^{-9})] < \frac{1}{\Theta}$$

$$\text{or } 4.5 \times 1.12 \times 10^{-9} < \frac{1}{\Theta}$$

$$\text{or } \Theta < \frac{10}{5.04} \times 10^8$$

$$\text{or } \Theta < 1.98 \times 10^8 \text{ }^{\circ}\text{C/Watt}$$

**Example 8.9:** Figure (8.15) shows a power amplifier using a PNP

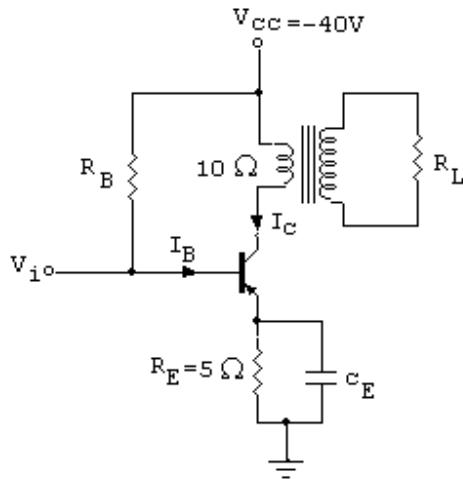


Fig. 8.15

Ge transistor with  $\beta = 120$  and  $I_{CO} = -6 \text{ mA}$ . The quiescent collector current  $I_C = -1 \text{ A}$ . Find

- (i) the value of  $R_B$
- (ii) the largest value of  $\Theta$  that can result the thermal stable circuit. Assume that the effect of  $I_{CO}$  dominates.

Solution: (i) The collector current is given by:

$$I_C = \beta I_B + (1 + \beta) I_{CO} \approx \beta (I_B + I_{CO})$$

$$\text{or } I_B = \frac{I_C - \beta I_{CO}}{\beta} = -\frac{1 - 120 \times 6 \times 10^{-3}}{120} \text{ A} = -2.8 \text{ mA}$$

Neglecting  $V_{BE}$ , we get

$$R_B = \frac{V_{CC} - V_E}{I_B} = \frac{40 - 5}{2.8} k\Omega = 12.5 k\Omega$$

$$(ii) |V_{CE}| = 40 - (10 + 5)1A = 25$$

$$\text{and } \frac{V_{CC}}{2} = \frac{40}{2} = 20V$$

Since  $V_{CE} > V_{CC}/2$ , so the circuit is not inherently stable. The stability factor is given by:

$$S = \frac{(1+\beta) \left[ 1 + \frac{R_B}{R_E} \right]}{\left[ 1 + \beta + \frac{R_B}{R_E} \right]} = 121x \frac{1 + \frac{12500}{5}}{121 + \frac{12500}{5}} = 115.5$$

The condition to prevent thermal runaway is

$$[V_{CC} - 2I_C(R_E + R_C)][S(0.07I_{CO})] < \frac{1}{\Theta}$$

$$\text{or } [40 - 2x1(5 + 10)][115.5(0.07x6x10^{-3})] < \frac{1}{\Theta}$$

$$\text{or } 10x115.5x0.42x10^{-3} < \frac{1}{\Theta}$$

$$\text{or } \Theta < 2.06 \text{ } ^0\text{C/Watt}$$

### Problems:

1. What do you understand by transistor biasing? Why it is needed?
2. What do you mean by the stabilization of operating point? Define the Stability factor. Derive the expression for the stability factor for fixed base bias.
3. Draw the self bias circuit. Find the expression for the stability factor for the self bias circuit. Explain qualitatively why such a circuit is an improvement on the fixed bias circuit.
4. List the three sources of instability of collector current. Define the three stability factor.
5. Show that the stability factor for the collector to base bias is  $S = \frac{(1+\beta)}{\left[ 1 + \frac{\beta R_C}{R_B + R_C} \right]}$ ,

the symbols have their meaning.

6. Find the expression for the stability factor  $S'$  for self bias circuit.
7. Find the expression for the stability factor  $S''$  for self bias circuit.
8. Define Stabilization and Compensation techniques.

9. Show that the stability factor for the self bias is  $S = \frac{(1+\beta) \left[ 1 + \frac{R_B}{R_E} \right]}{\left[ 1 + \beta + \frac{R_B}{R_E} \right]}$ , the symbols have their meaning.

10. Prove that the stability factor  $S'$  for self bias circuit is  $S' = \frac{-\beta \cdot S}{(1 + \beta)(R_B + R_E)}$ . The symbols have their usual meaning.
11. Prove that the stability factor  $S''$  for self bias circuit is  $S'' = \frac{I_C}{\beta} \cdot \frac{S}{(1 + \beta)}$ . The symbols have their usual meaning.
12. Prove that the stability factor  $S''$  for self bias circuit is  $S'' = \left( \frac{I_{C1}}{\beta_1} \right) \left( \frac{S_2}{(1 + \beta_2)} \right)$   
 Where  $S_2$  is the value of  $S$  for  $\beta = \beta_2$  given by  $S_2 = \frac{[(1 + \beta)(R_B + R_E)]}{[(1 + \beta)R_E + R_B]}$ . The other symbols have their usual meaning.
13. Prove that the stability factor  $S'$  for collector to base bias circuit is  $S' = \frac{-\beta \cdot S}{(1 + \beta)(R_B + R_C)}$ . The symbols have their usual meaning.
14. Prove that the stability factor  $S''$  for the collector to base bias circuit is  $S'' = \frac{I_C}{\beta} \cdot \frac{S}{(1 + \beta)}$ . Where  $S$  is the stability factor for this circuit and other symbols have their meaning.
15. Draw and explain the circuit for diode compensation for the changes in  $V_{BE}$ .
16. Draw and explain the circuit for diode compensation for the changes in  $I_{CO}$ .
17. Draw and explain the circuit employing thermistor compensation and sesistor compensation.
18. Discuss thermal runaway.
19. Define thermal resistance. What is the condition for thermal stability? Explain.
20. Show that the thermal runaway cannot take place if  $V_{CE} < \frac{V_{CC}}{2}$ .
21. Determine the operating point for a silicon transistor with  $\beta = 50$  used in the self biasing circuit. The circuit components are  $V_{CC} = 20$  V,  $R_C = 2$  K $\Omega$ ,  $R_E = 100$   $\Omega$ ,  $R_I = 100$  K $\Omega$  and  $R_2 = 5$  K $\Omega$ . Find also the stability factor for this circuit.
22. Determine the operating point for a Germanium transistor with  $\beta = 50$  used in the self biasing circuit. The circuit components are  $V_{CC} = 20$  V,  $R_C = 2$  K $\Omega$ ,  $R_E = 100$   $\Omega$ ,  $R_I = 100$  K $\Omega$  and  $R_2 = 5$  K $\Omega$ . Find also the stability factor for this circuit.
23. In self bias  $CE$  transistor (NPN) amplifier circuit  $R_I = 90$  K $\Omega$ ,  $R_2 = 10$  K $\Omega$  and  $\alpha = 0.98$ . Find the value of  $S$  when emitter resistance is :  
 (i) 1 K $\Omega$  and (ii) 2 K $\Omega$ . (Ans. 8.46, 5.0)

24. An NPN transistor with  $\beta = 100$  is used in  $CE$  circuit with  $V_{CC} = 15$  V,  $R_C = 4.7$   $K\Omega$ . Bias is obtained by connecting a  $220$   $K\Omega$  resistance from collector to base (collector to base bias). Find Q – point and the stability factor  $S$ .

(Ans.  $I_B = 21\mu A$ ,  $I_C = 2.1$  mA,  $V_{CE} = 5.13$  V &  $S = 32.7$ )

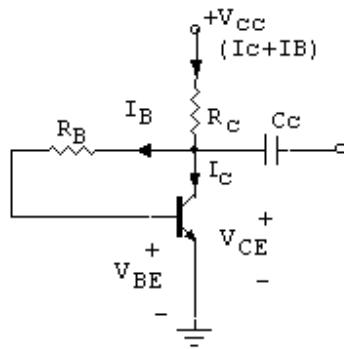
25. A Si NPN transistor is used in self bias  $CE$  amplifier, with  $V_{CC} = 24$  V,  $R_C = 5$   $K\Omega$ ,  $R_E = 1$   $K\Omega$ ,  $R_I = 81$   $K\Omega$  and  $R_2 = 9$   $K\Omega$ . The transistor has  $\beta = 60$ . Find the Q – point and the value of stability factor  $S$ .

(Ans.  $I_B = 25\mu A$ ,  $I_C = 1.5$  mA,  $V_{CE} = 15$  V &  $S = 8.03$ )

26. A Si NPN transistor is used in the self bias  $CE$  amplifier, having  $\beta = 50$  at room temperature. The circuit has  $R_I = 90$   $K\Omega$  and  $R_2 = 10$   $K\Omega$  and  $R_E = 1.5$   $K\Omega$ . The values of other components are adjusted to have the collector current  $I_C$  equal to 2 mA. Calculate the values of  $S$ ,  $S'$ ,  $S''$ .

(Ans.  $S = 6.3$ ,  $S' = -5.85 \times 10^{-4}$  amp/volt,  $S'' = 4.9 \times 10^{-6}$  amp.)

27. For the circuit given below



- (i) Calculate the values of  $I_B$ ,  $I_C$  &  $V_{CE}$  if Si transistor with  $\beta = 45$  is used.  
Provided  $V_{CC} = 12$  V,  $R_C = 2.7$   $K\Omega$ ,  $R_B = 120$   $K\Omega$  and  $V_{BE} = 0.7$  V

- (ii) Find the value of  $R_B$  so that  $V_{CE} = 8$  Volts.

(Ans. (i)  $I_B = 46.3$   $\mu A$ ,  $I_C = 2.08$  mA  $V_{CE} = 6.23$  V (ii)  $R_B = 207$   $K\Omega$ )

28. For the self bias  $CE$  transistor (Si) amplifier has the following values  $R_E = 4.5$   $K\Omega$ ,  $R_I = 90$   $K\Omega$ ,  $R_2 = 10$   $K\Omega$ . The collector supply voltage and collector resistance  $R_C$  are adjusted so as to give the collector current of 1.5 mA at  $25^{\circ}\text{C}$ . Determine the variation of collector current in the temperature range  $+25^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$ , when the Si transistor of table 8.1 is used.

(Ans. 0.21mA)



# 9

## Field Effect Transistors

The field effect transistor (FET) is a three terminal semiconductor device in which the current is controlled by an electric field and used for variety of applications in electronics. Unlike the usual transistor, its operation depends upon the flow of majority carriers and the minority charge carriers play no significant role in the operation of the device. It is, therefore, known as a unipolar device. In usual transistors the current flow due to both types of charge carriers (electrons and holes) hence known as bipolar junction transistors (BJT). In the present chapter classification, operation and characteristics of the field effect transistors will be discussed. In addition the biasing and applications of the field effect transistors will also be illustrated.

**9.1 Field Effect Transistors:** The field effect transistors may broadly be classified in to the following two categories:

- (1) Junction Field Effect Transistors (JFET)
- (2) Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

It is also called Insulated Gate Field Effect Transistors (IGFET)

MOSFET's are further subdivided in two categories:

- (i) Enhancement type MOSFET
- (ii) Depletion type MOSFET

Each of the above categories may be either N – channel or P - channel.

The field effect transistors differ from the bipolar junction transistors in the following important characteristics:

FET'S	BJT'S
<ol style="list-style-type: none"> <li>1. Its operation depends upon the flow of majority charge carriers only. It is therefore a Unipolar device.</li> <li>2. It exhibits very high input resistance, typically many megohms.</li> <li>3. It is voltage controlled device i.e. the output (drain) current is controlled by the input (gate) voltage.</li> <li>4. Less noisy.</li> <li>5. Thermal stability is good.</li> <li>6. Immune to radiations.</li> <li>7. It is simpler to fabricate and occupies less space in the integrated form.</li> <li>8. It exhibits no offset voltage at zero drain current, and hence makes an excellent signal chopper.</li> <li>9. It has small band width product. (This is the only drawback).</li> </ol>	<p>Its operation depends upon the flow of both the two types of charge carriers i.e. electrons and holes hence it is named as Bipolar device.</p> <p>It exhibits low input resistance. It ranges from <math>10^2</math> to <math>10^6</math> ohms.</p> <p>It is current controlled device i.e. the output current is controlled by the input current.</p> <p>More noisy.</p> <p>Thermal stability is poor.</p> <p>Sensitive to radiations.</p> <p>It occupies more space in the integrated form.</p> <p>It has offset voltage at zero collector current, hence not used for signal chopper.</p> <p>It has high band width product.</p>

**9.2 Junction Field Effect Transistor:** Figure 9.1(a) shows the structure of N – channel junction field effect transistor. It consists of an  $N$  – type substrate (bar or channel) in which two  $P^+$  – regions (heavily doped  $P$  – regions) are diffused. One end of the  $N$  – type substrate is called source and other end is called drain. The two heavily doped  $P$  – regions are connected to a third terminal called gate. The detailed sketch of the  $N$  – channel JFET is shown in figure 9.1(b).

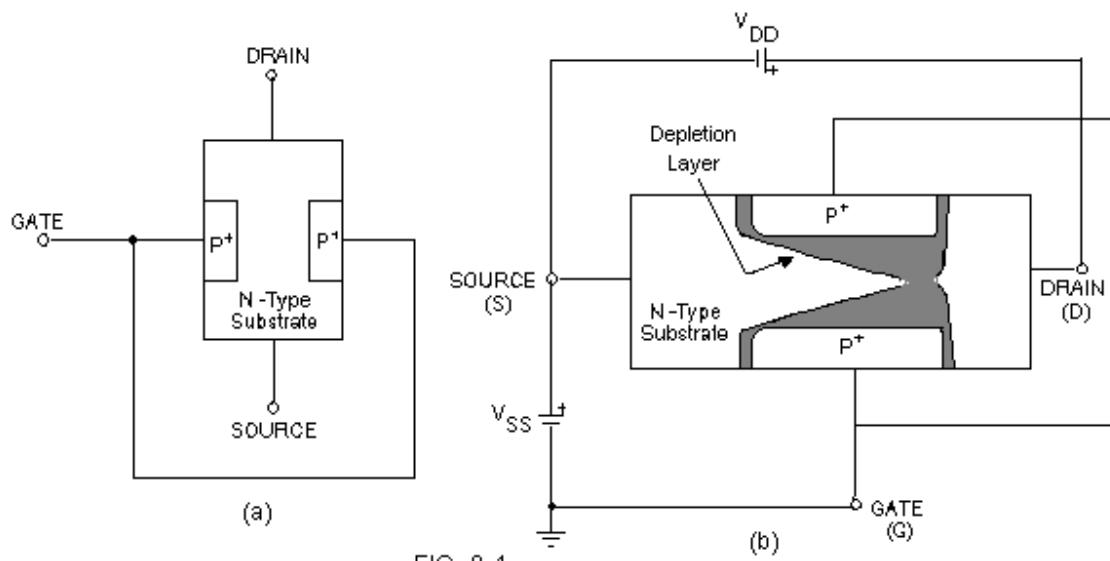


FIG. 9.1

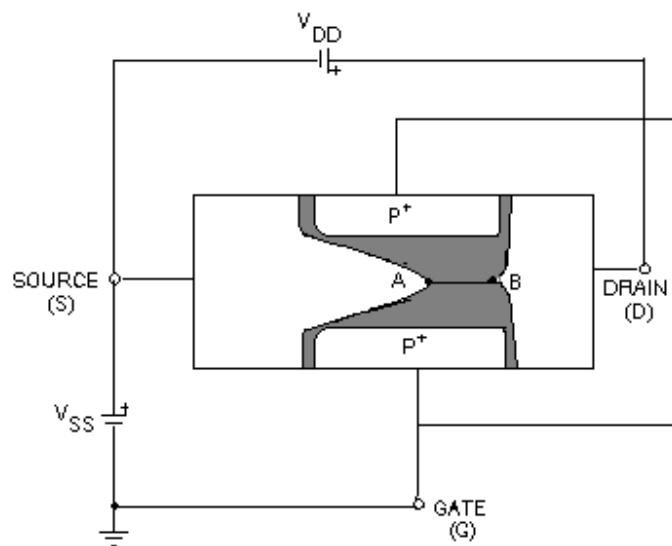
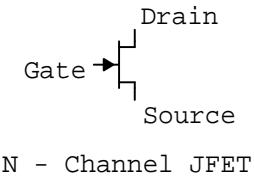


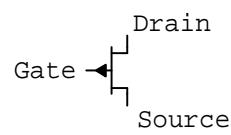
Fig. 9.1(c)

In the normal operation of JFET, the gate is kept at a negative potential with respect to the source. The two  $P - N$  junctions are in reverse bias. The drain is operated at a positive potential with respect to the source. There exist space charge region (depletion region) on either side of junction leaving uncovered positive ions on the  $N$  side and uncovered negative ions on the  $P$  side. The electric field extends from the positive ions on one side to the negative ions on the other side. As the magnitude of the reverse bias across the junction increases, the thickness of the uncovered region also increases. The conductivity of the uncovered region is zero since there are no current carriers. Since the two  $P$  regions are heavily doped compared to the  $N$  region (bar), the bulk of the depletion region may assume to be in the  $N$  channel. It is well known that the width of the depletion region increases with increasing reverse bias. So when we move from the source end to the drain end the reverse bias across the  $P - N$  junction increases. The width of the depletion region will also increase from the source end to the drain end. The width of depletion region in the  $N$  – channel is, therefore, like wedge shaped as shown by dark shadow in figure 9.1(b)and (c). Thus for a fixed drain to source voltage, it becomes possible to control the drain current by varying the reverse bias voltage across the gate junction. The field effect transistor is named so because the current control is the effect of the extension of the field associated with depletion region as caused by the increasing reverse bias.

**9.2.1 Static characteristics of JFET:** The symbols used for  $N$  – channel JFET and  $P$  – channel JFET are shown in Figure (9.2). The direction of



$N$  – Channel JFET



$P$ – Channel JFET

Figure 9.2

arrow at the gate of the JFET indicates the direction in which the gate current would flow if the gate junction were forward biased. Figure 9.3 shows the circuit diagram, to plot the

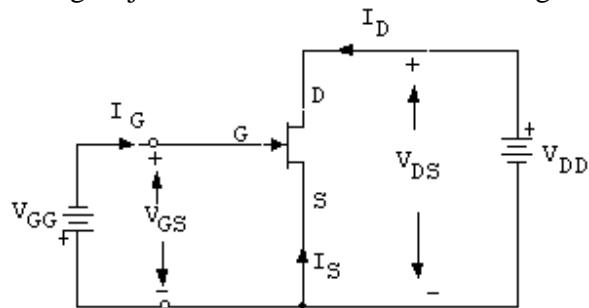


Figure 9.3

characteristic curves of  $JFET$  in common source mode. Figure (9.4) shows the characteristic curves of the  $FET$ , where the drain current  $I_D$  is plotted against  $V_{DS}$  (drain

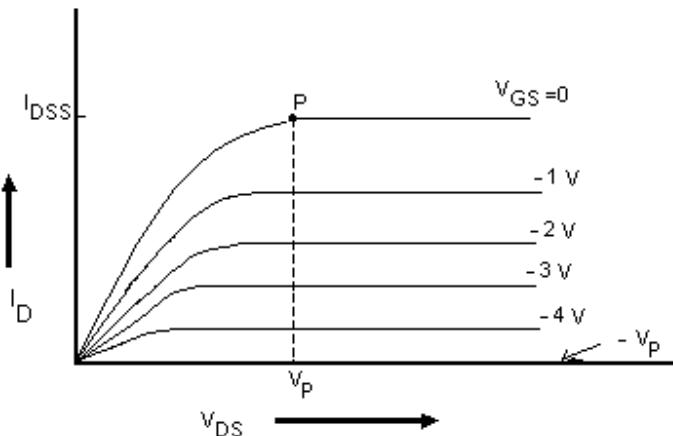


Figure 9.4

to source voltage) with  $V_{GS}$  (gate to source voltage) as the parameter. To understand the nature of these characteristic curves, let us set  $V_{GS}$  equal to zero. As we increase  $V_{DS}$  the drain current  $I_D$  increases until  $V_{DS}$  equals  $V_P$ . At the voltage  $V_P$  the two depletion regions meet at a point in the channel and we say channel is pinched off. Thus, if we increase the  $V_{DS}$  beyond  $V_P$ , the drain current  $I_D$  saturates and becomes a constant value denoted by

$I_{DSS}$ . In fact when  $V_{DS}$  is increased beyond  $V_P$ , the potential at two points A and B (ref. 9.1c) is responsible for the drain current to flow. The electric field so generated helps in sweeping the carriers from the source end to drain end. The increase of  $V_{DS}$  (beyond  $V_P$ ) corresponds to the proportional increase in the distance AB. This in turn gives the constant electric field  $\frac{V_{DS}}{AB}$ . The constant electric field does not allow the drain current to increase further. The saturated drain current ( $I_{DSS}$ ) is thus obtained.

If now the magnitude of the gate potential is increased in the direction to provide the additional reverse bias, pinch off will take place at a lower voltage. Further increase in  $V_{DS}$  does not result in any increase in  $I_D$  and the current saturates at a lower value than  $I_{DSS}$ . Curves corresponding to different negative values of  $V_{GS}$  are shown in figure (9.4). If  $V_{DS}$  is increased beyond a certain limit, the JFET enters in the breakdown region where the drain current increases drastically. This happens because the reverse biased P – N junctions undergo avalanche breakdown when small changes in  $V_{DS}$  produce very large change in drain current.

It is worthwhile to mention that the characteristic curves beyond the pinch off voltage are parallel to each other (having the saturated values) and the saturated drain currents for this region are denoted by  $I_{DS}$ . In amplifier applications the FET is always used in this region. The value of  $I_{DS}$  with gate shorted to the source ( $V_{GS} = 0$ ) is denoted by  $I_{DSS}$ .

The transfer characteristic of the JFET ( $I_D$  versus  $V_{GS}$  with  $V_{DS}$  kept constant at a value greater than  $|V_P|$ ), is shown in figure (9.5). Note that for  $V_{GS} = 0$ ,  $I_{DS} = I_{DSS}$

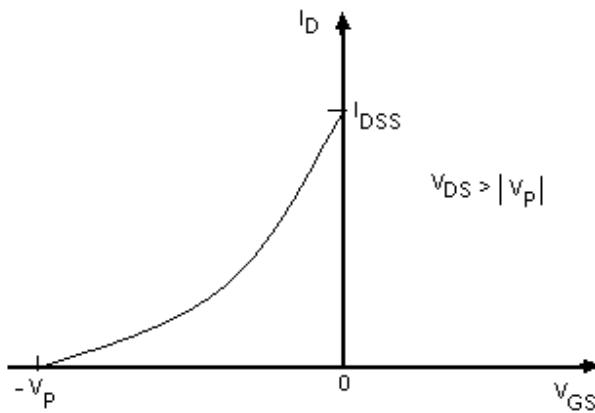


Fig. 9.5

and for  $V_{GS} = -V_p$ ,  $I_{DS} = 0$ . The dependence of  $I_{DS}$  on  $V_{GS}$  can be approximated by the parabola given by:

$$I_{DS} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2 \quad \text{----- (9.1)}$$

This simple parabolic approximation gives an excellent fit, with the experimentally determined transfer characteristics for FET's made by diffusion process.

**9.3 Metal Oxide Semiconductor (MOS) FET:** There are two types of Metal Oxide Semiconductor field Effect Transistors. One is called as Enhancement type MOSFET, while the other is called as Depletion type MOSFET. Both the two types of MOSFET's will be discussed below.

**9.3.1 Enhance type MOSFET:** Figure (9.6) shows the  $P$  – channel enhancement type MOSFET which consists of a lightly doped N – type substrate into which two heavily doped  $P^+$  regions are diffused. These two  $P^+$  regions act as the source and the drain. The source and drain are 10 to 20  $\mu\text{m}$  apart. Then a thin layer of insulating silicon dioxide ( $\text{SiO}_2$ ) is grown over the entire surface of the structure. Holes are cut in the  $\text{SiO}_2$  layer above the  $P^+$  regions (source and drain). The metal film is evaporated between the source and the drain and also through the cut in the  $\text{SiO}_2$  layer. The metallic layer between the source and the drain forms the gate. The contacts to the source and the drain are also taken through the metallic layers in the cuts over the two  $P^+$  regions.

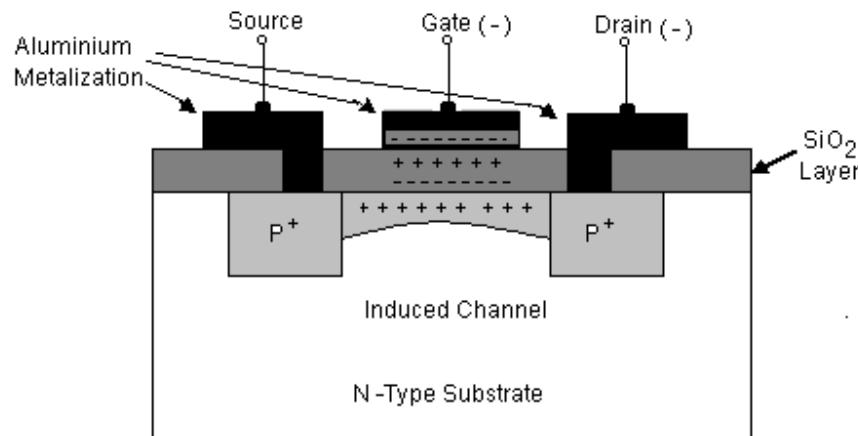


Fig. 9.6

The metal area of the gate, in addition with the insulating dielectric oxide layer and the semiconductor channel, form a parallel plate capacitor. The insulating layer of silicon dioxide is the reason why this device is called the insulated gate field effect transistor.

When a negative voltage is applied at the gate, it induces positive charges in insulating layer and correspondingly positive charges in semiconductor. The positive charge region in semiconductor increases as the negative voltage at the gate increases. When the drain is kept at the negative potential with respect to source, the positive charges in the semiconductor help in conducting between source and the drain. In this way the drain current is enhanced by the negative gate voltage. Figure 9.7 (a) and 9.7(b)

show the drain characteristics and transfer characteristics of P – channel enhancement type MOSFET.

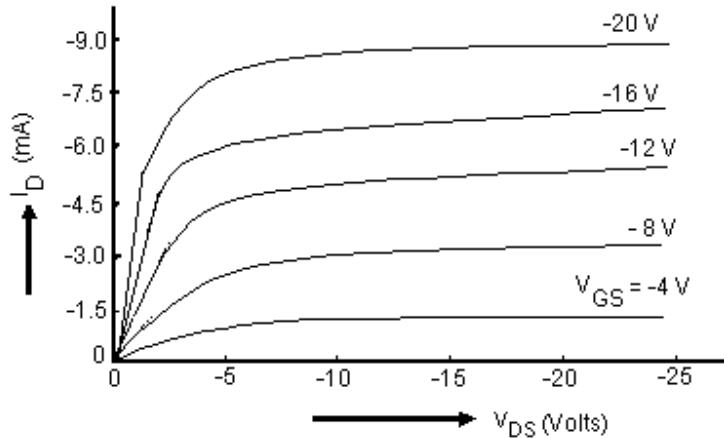


Fig. 9.7(a)

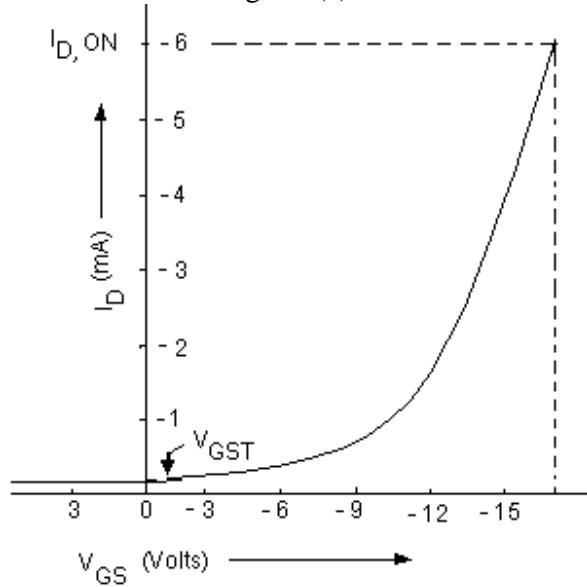


Fig. 9.7(b)

It may be noted from figure 9.7(a), that the drain current for  $V_{GS}$  greater than zero is very small and as  $V_{GS}$  is made more negative the current increases slowly at first and then increases drastically. The manufacturer often indicates the gate source threshold voltage  $V_{GST}$  or  $V_T$  at which the drain current  $|I_D|$  attains some defined small value say about  $10 \mu\text{A}$ . The current  $I_{D,ON}$ , the maximum permissible current on the drain characteristics, is also specified by the manufacturer.

**9.3.2 Depletion type MOSFET:** The basic structure of  $N$  – channel depletion type MOSFET is shown in figure 9.8(a). It consists of a lightly doped  $P$  – type substrate into which two heavily doped  $N^+$  regions are diffused. These two  $N^+$  regions act as the source and the drain. In depletion type MOSFET a lightly doped  $N$  – channel is diffused between

the source and the drain. Then a thin layer of insulating silicon dioxide ( $\text{SiO}_2$ ) is grown over the entire surface of the structure. Holes are cut in the  $\text{SiO}_2$  layer above the  $N^+$  regions (source and drain). The metal film is evaporated between the source and the drain and also through the cut in the  $\text{SiO}_2$  layer. The metallic layer between the source and the drain forms the gate.

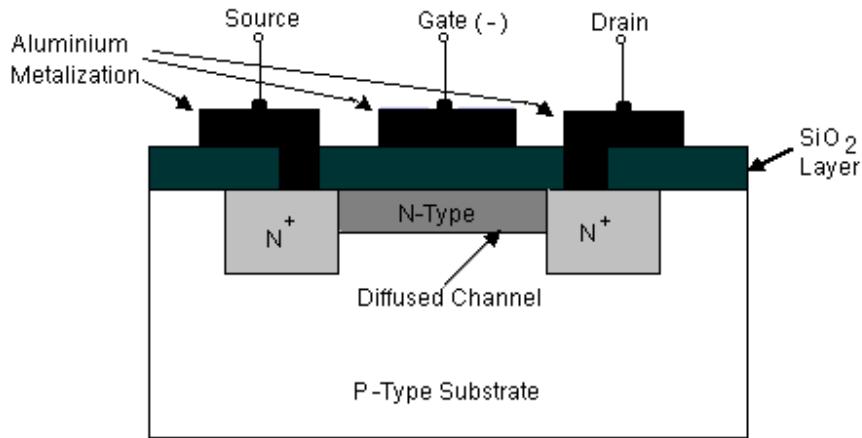


Fig. 9.8(a)

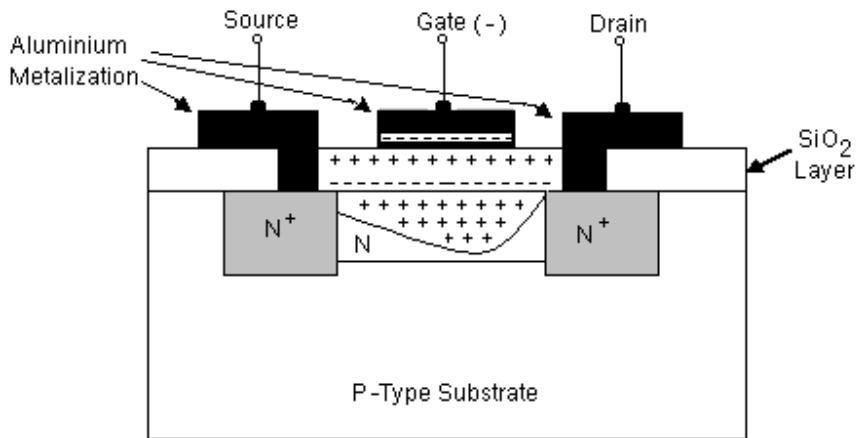


Fig 9.8(b)

When negative voltage is applied at the gate, positive charges are induced in the  $N^-$  channel through the insulating layer of  $\text{SiO}_2$ , as shown in figure 9.8(b). Since the conduction of current through the channel is by means of majority carriers (electrons in  $N^-$  channel), the conductivity of the channel reduces as the gate voltage is made more negative. It is so because the channel is depleted of majority carriers due to induction of positive charge in it by application of negative gate voltage. The drain current  $I_D$  is decreased as the gate voltage  $V_{GS}$  is made more negative. This phenomenon is analogous

to that of pinch off occurring in the JFET at the drain end of the channel. Figures 9.9(a) and 9.9(b) show the drain and transfer characteristics of the depletion type MOSFET. The drain characteristics of a depletion type MOSFET are similar to that of a JFET.

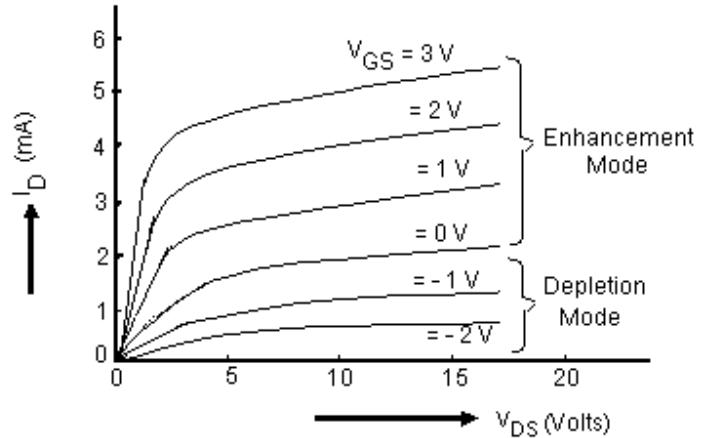


Fig. 9.9(a)

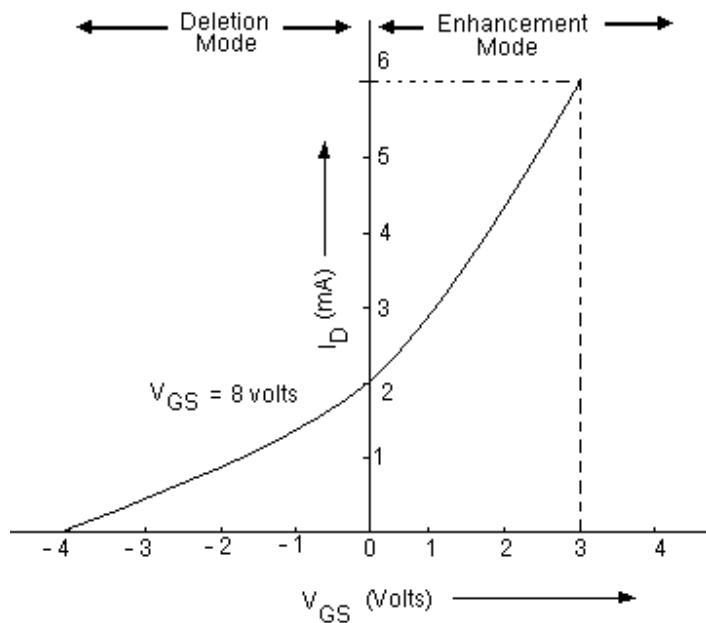
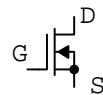


Fig. 9.9(b)

A depletion MOSFET may also be used in enhancement mode, by applying positive voltage at the gate. In this case the negative charges are induced in the channel and its conductivity increases. The drain current  $I_D$  thus increases or enhances as more positive potential is applied. Figures 9.9(a) and 9.9(b) also show the drain and transfer characteristics of the MOSFET operated in both depletion and enhancement mode.

**9.3.3 Circuit Symbols:** The graphical symbols for an N – channel and P – channel depletion type MOSFET's are shown in figure 9.10(a) and 9.10(b) respectively. Two

N – channel



P – channel

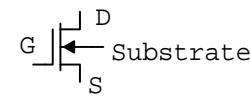


Figure 9.10(a)

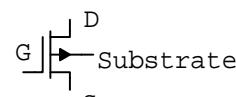
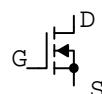


Figure 9.10(b)

symbols are provided for each type of channel. Similarly the symbols for N – channel and P – channel enhancement type MOSFET's are shown in figure 9.11(a) and 9.11(b) respectively.

N – channel



P – channel

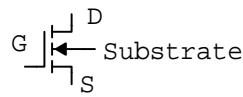


Figure 9.11(a)

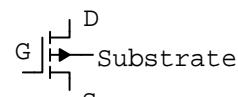


Figure 9.11(b)

**9.4 Parameters of FET:** The linear small signal model for the field effect transistor can be obtained in the same fashion as for bipolar junction transistor. As is well known that the drain current  $i_D$  may be expressed as a function of gate voltage  $v_{GS}$  and  $v_{DS}$  as given below:

$$i_D = f(v_{GS}, v_{DS}) \quad \text{----- (9.2)}$$

The three parameters namely the drain resistance  $r_d$ , transconductance  $g_m$  and amplification factor  $\mu$  may be defined as follows:

**9.4.1 Drain Resistance  $r_d$ :** The parameter  $r_d$  known as dynamic drain resistance or the output resistance is defined as the ratio of the change in the drain to source voltage to the change in drain current at a constant gate to source voltage  $v_{GS}$ .

$$r_d = \left. \frac{\partial v_{DS}}{\partial i_D} \right|_{v_{GS}} \approx \left. \frac{\Delta v_{DS}}{\Delta i_D} \right|_{v_{GS}} \quad \text{----- (9.3)}$$

The reciprocal of the drain resistance is known as the drain conductance  $g_d$ .

**9.4.2 Transconductance  $g_m$ :** The mutual conductance or transconductance  $g_m$  is defined as the ratio of the change in the drain current to the change in gate to source voltage at a constant drain to source voltage.

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{DS}} \approx \left. \frac{\Delta i_D}{\Delta v_{GS}} \right|_{v_{DS}} \quad \text{----- (9.4)}$$

**9.4.3 Amplification Factor  $\mu$ :** Third important parameter of the FET is the amplification factor  $\mu$  defined as the ratio of the change in drain to source voltage to the change in gate to source voltage when the drain current is kept constant.

$$\mu = - \left. \frac{\partial v_{DS}}{\partial v_{GS}} \right|_{i_D} \approx - \left. \frac{\Delta v_{DS}}{\Delta v_{GS}} \right|_{i_D} \quad \text{----- (9.5)}$$

The negative sign in this expression represents that when the drain to source voltage is increased; the drain current increases now to keep the drain current constant the gate to voltage has to be decreased. In other words to the keep the drain current constant the drain to source voltage and the gate to source voltage should of opposite sign.

The amplification factor  $\mu$  can also be written in the following form

$$|\mu| = \frac{\partial v_{DS}}{\partial i_D} \cdot \frac{\partial i_D}{\partial v_{GS}} = r_d \cdot g_m \quad \text{----- (9.6)}$$

**9.4.4 Relation between Transconductance  $g_m$  and Drain Current  $I_{DS}$  of the FET:** We have the drain current given by equation (9.1) which is reproduced here:

$$I_{DS} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \quad \text{----- (9.7)}$$

Differentiating this equation with respect to  $v_{GS}$  we get:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = 2I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right) x \left( -\frac{1}{V_P} \right)$$

$$\begin{aligned}
&= -\frac{2 \cdot I_{DSS}}{V_P} \left( 1 - \frac{V_{GS}}{V_P} \right) \\
&= g_{m0} \left( 1 - \frac{V_{GS}}{V_P} \right)
\end{aligned} \quad \text{----- (9.8)}$$

Where  $g_{m0}$  is the value of gm for  $V_{GS} = 0$  and given by:

$$g_{m0} = -\frac{2I_{DSS}}{V_P}$$

Combining the equations (9.7) and (9.8), we get:

$$g_m = -\frac{2}{V_P} \sqrt{I_{DSS} \cdot I_{DS}} \quad \text{----- (9.9)}$$

From the equation (9.9) it is clear that the transconductance gm varies as the square root of the drain current.

**9.5 Small Signal Model of Field Effect Transistor:** The drain current  $i_D$  may be expressed as a function of gate voltage  $v_{GS}$  and  $v_{DS}$  as given below:

$$i_D = f(v_{GS}, v_{DS})$$

The incremental change in the drain current  $i_D$  may be given by the Taylor series expansion as:

$$\Delta i_D = \frac{\partial i_D}{\partial v_{GS}} \cdot \Delta v_{GS} + \frac{\partial i_D}{\partial v_{DS}} \cdot \Delta v_{DS} \quad \text{----- (9.10)}$$

In the small signal notation,  $\Delta i_D = i_d$ ,  $\Delta v_{GS} = v_{gs}$  and  $\Delta v_{DS} = v_{ds}$ , the equation (9.10) may be written in the form:

$$i_d = g_m \cdot v_{gs} + \frac{1}{r_d} \cdot v_{ds} \quad \text{----- (9.11)}$$

A circuit satisfying the equation (9.11) may be drawn as shown in the figure (9.12).

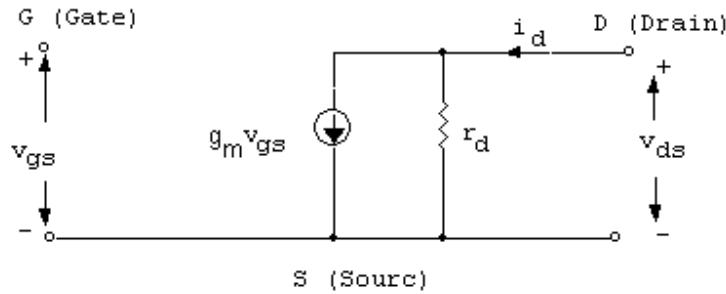


Fig. 9.12

This circuit is known as the small signal model of the field effect transistor. This small signal model has a Norton's output (current source) whose current is proportional to the gate to source voltage. The proportionality factor is the transconductance  $g_m$ . The input resistance between gate and source is infinite since reverse biased gate current is assumed to be zero. Similarly the resistance between the gate and the drain is infinite. The output resistance is drain resistance  $r_d$ , whose value is infinitely large when FET is operated in the linear region where the characteristic curves are parallel and equidistant from each other. In that case the output will behave like a constant current source whose value will depend upon the input voltage  $v_{gs}$ . Hence the FET is known as the voltage operated device or Voltage Controlled Current Source (VCCS).

The small signal model discussed above is suitable for low frequency signal only. The capacitances between the terminals of the field effect transistors may get added at high frequencies as these will produce finite reactance at the frequency. So the small signal model at the high frequencies will be as given in figure (9.13).

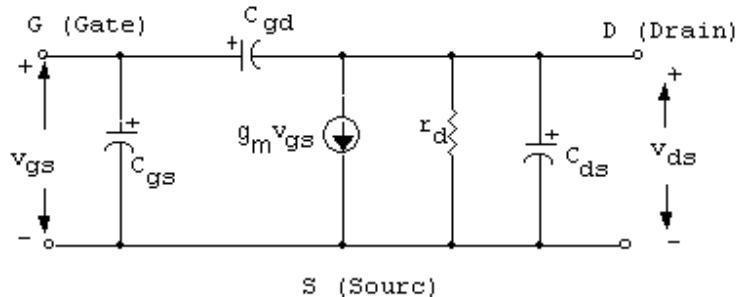


Fig. 9.13

In this circuit the capacitance  $C_{gs}$  is the barrier capacitance between the gate and the source,  $C_{gd}$  is the barrier capacitance between the gate and the drain and the capacitance  $C_{ds}$  is similarly the drain to source capacitance of the channel. These capacitances produce the feedback from the output to the input and the voltage gain drops rapidly as the frequency increases.

**Example 9.1** Show that for small values of  $V_{GS}$  compared with  $V_P$ , the drain current is approximately given by:

$$I_D \cong I_{DSS} + g_{m0}V_{GS}$$

Solution: We have

$$g_m = g_{m0} \left( 1 - \frac{V_{GS}}{V_P} \right)$$

We also have the expression for the drain current as:

$$I_D = g_m \cdot V_{GS} + \frac{1}{r_d} \cdot V_{DS}$$

Putting the value of gm in this expression we get:

$$I_D = g_{m0} \left( 1 - \frac{V_{GS}}{V_P} \right) + \frac{1}{r_d} \cdot V_{DS}$$

$$\text{or } I_D = g_{m0}V_{GS} - g_{m0} \frac{V_{GS}}{V_P} V_{GS} + \frac{1}{r_d} \cdot V_{DS}$$

If  $V_{GS}$  is smaller than the magnitude of  $V_P$  then we have

$$I_D \cong g_{m0}V_{GS} + \frac{1}{r_d} \cdot V_{DS}$$

$$\text{If } V_{GS} = 0 \text{ then } I_D = I_{DSS} = \frac{V_{DS}}{r_d}, \text{ so}$$

$$I_D \cong I_{DSS} + g_{m0}V_{GS} \quad \text{Proved.}$$

Example 9.2 If the two FETs (which are not identical) are connected in parallel then prove that the effective transconductance and drain resistance of this combination are:

$$g_m = g_{m1} + g_{m2}$$

$$\text{and } \frac{1}{r_d} = \frac{1}{r_{d1}} + \frac{1}{r_{d2}} \text{ respectively.}$$

The amplification factor of the combination is given by:

$$\mu = \frac{\mu_1 r_{d2} + \mu_2 r_{d1}}{r_{d1} + r_{d2}}$$

Solution: Let two FETs, whose drain resistances are  $r_{d1}$  and  $r_{d2}$  and their transconductance are  $g_{m1}$  and  $g_{m2}$ , are connected in parallel as shown in figure 9.14. The combination of these FETs behaves like a single FET.

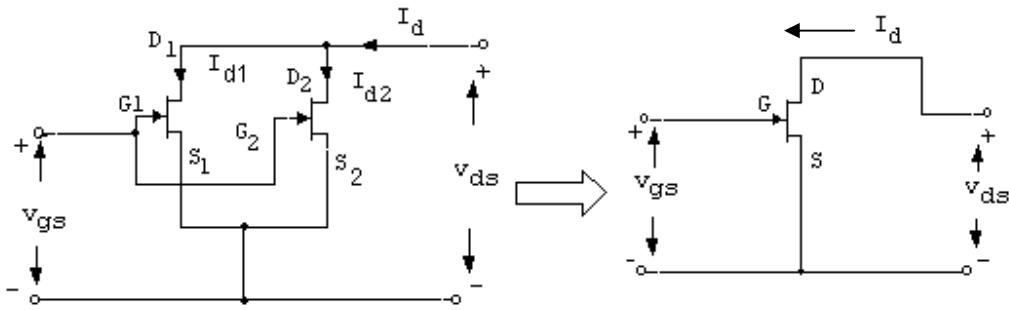


Fig. 9.14

Let  $I_{d1}$  and  $I_{d2}$  are the two drain currents of the individual FET given by:

$$I_{d1} = g_{m1} \cdot V_{GS} + \frac{1}{r_{d1}} V_{DS}$$

$$I_{d2} = g_{m2} \cdot V_{GS} + \frac{1}{r_{d2}} V_{DS}$$

and

$$I_d = I_{d1} + I_{d2}$$

or

$$I_d = (g_{m1} + g_{m2}) V_{GS} + \left( \frac{1}{r_{d1}} + \frac{1}{r_{d2}} \right) V_{DS}$$

This implies

$$g_m = g_{m1} + g_{m2}$$

and

$$\frac{1}{r_d} = \frac{1}{r_{d1}} + \frac{1}{r_{d2}}$$

Amplification factor  $\mu$  is given by:

$$\mu = r_d \cdot g_m = \left( \frac{r_{d1} \cdot r_{d2}}{r_{d1} + r_{d2}} \right) \cdot (g_{m1} + g_{m2})$$

or

$$= \frac{g_{m1} \cdot r_{d1} \cdot r_{d2} + g_{m2} \cdot r_{d1} \cdot r_{d2}}{r_{d1} + r_{d2}}$$

$$= \frac{\mu_1 \cdot r_{d2} + \mu_2 \cdot r_{d1}}{r_{d1} + r_{d2}} \quad \text{Proved.}$$

**9.6 Low Frequency FET Amplifiers:** As is well known that the bipolar transistors can be used in three amplifiers configurations CE, CB and CC. The field effect transistors can also be used in three amplifier configurations namely common source (CS), common gate (CG) and common drain (CD). The common source amplifier is

analogous to the common emitter amplifier of the bipolar transistor. The common drain (CD) amplifier is analogous to the common collector amplifier. The common drain amplifier is also called source follower as the common collector amplifier is known as emitter follower. We shall analyze these amplifiers in detail.

**9.6.1 Common Source Amplifier:** The basic circuit diagram of common source amplifier is shown in figure 9.15, in which the source is common between input and output circuit. The input signal  $V_i$  to be amplified is applied to the gate terminal of the FET. The output is taken at the drain and across the load resistance  $R_L$ . We shall analyze the circuit by calculating the voltage gain and output resistance of the amplifier.

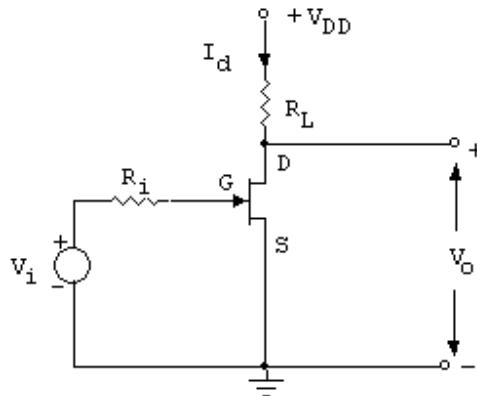


Fig. 9.15

The small signal model for the purpose the above mentioned quantities of this circuit may be drawn as given in figure 9.16.

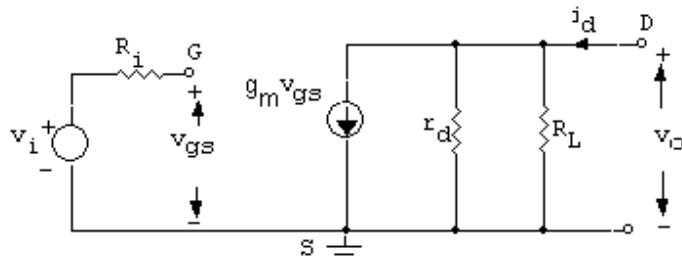


Fig. 9.16

The Thevenin's equivalent model of this circuit may also be drawn as shown in figure 9.17.

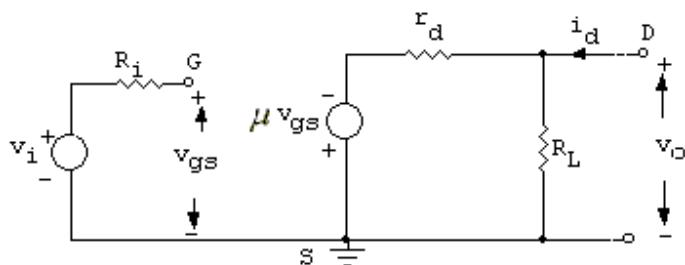


Fig. 9.17

Voltage Gain: The voltage gain  $A_v = \frac{V_o}{V_i}$  of the amplifier can be calculated from the figure 9.17, as:

$$A_v = \frac{V_o}{V_i} = \frac{-\mu}{r_d + R_L} x R_L \quad \text{----- (9.12)}$$

$$= \frac{-\left(\frac{\mu}{r_d}\right)}{\left(1 + \frac{R_L}{r_d}\right)} x R_L = \frac{-g_m}{\left(1 + \frac{R_L}{r_d}\right)} x R_L$$

If  $r_d \gg R_L$ , then the voltage gain of the amplifier is given as:

$$A_v = -g_m \cdot R_L \quad \text{----- (9.13)}$$

The negative sign in this expression indicates that there is a phase reversal of 180° between input and output signal.

From the equivalent circuit the output resistance is:

$$R_o = r_d \quad \text{----- (9.14)}$$

**9.6.2 Common Drain Amplifier:** The basic circuit of a common drain amplifier using field effect transistor is shown in figure (9.18).

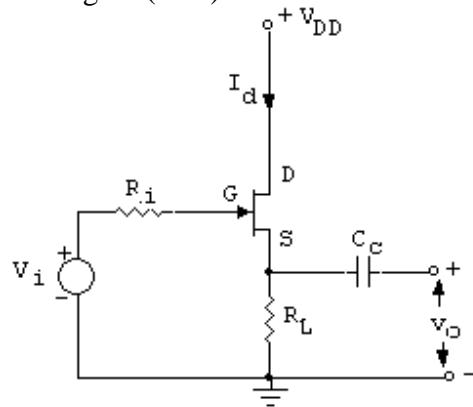


Fig. 9.18

In this circuit the drain is connected to the d.c. supply and for the a.c. signal analysis the d.c. supply is shorted to ground. Hence the signal applied between the gate and the ground is basically between gate and the drain. The output is being taken between the source and the ground (means drain). Now we shall find the voltage gain and output resistance of this circuit. The equivalent circuit is therefore, drawn as shown in figure (9.19).

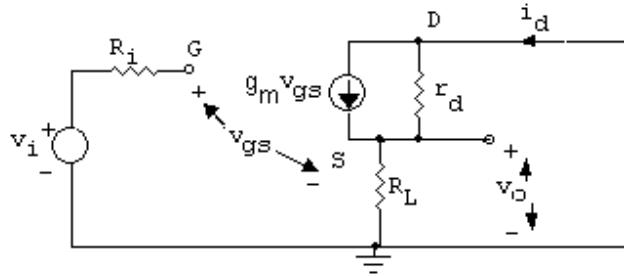


Fig. 9.19

Applying the KVL to the output circuit, we get:

$$i_d \cdot R_L + (i_d - g_m \cdot V_{GS})r_d = 0 \quad \dots\dots (9.15)$$

and

$$V_{GS} = V_i - i_d \cdot R_L \quad \dots\dots (9.16)$$

or

$$i_d \cdot (R_L + r_d) - g_m \cdot r_d (V_i - i_d \cdot R_L) = 0$$

or

$$i_d = \frac{g_m \cdot r_d \cdot V_i}{[R_L(1+\mu) + r_d]} = \frac{\mu \cdot V_i}{[r_d + (1+\mu)R_L]} \quad \dots\dots (9.17)$$

The output voltage is given by:

$$V_o = i_d \cdot R_L = \frac{\mu \cdot V_i \cdot R_L}{[r_d + (1+\mu)R_L]} \quad \dots\dots (9.18)$$

The voltage gain of the amplifier can be obtained as

$$A_v = \frac{V_o}{V_i} = \frac{\mu \cdot R_L}{[r_d + (1+\mu)R_L]} \quad \dots\dots (9.19)$$

$$\text{If } (\mu+1)R_L \gg r_d \text{ then } A_v \approx \frac{\mu}{(1+\mu)}$$

Generally  $\mu \gg 1$  for the field effect transistors, so the gain of the amplifier will become almost equal to unity ( $A_v \approx 1$ ).

The voltage of unity means that the output (Source) follows the input (gate) signal. Hence the Common Drain configuration may be called as the Source Follower circuit, similar to the emitter follower of bipolar transistor amplifiers.

The equation (9.18) may be rewritten of the following form:

$$V_o = \frac{\frac{\mu \cdot V_i}{(1+\mu)} \cdot R_L}{\left[ \frac{r_d}{(1+\mu)} + R_L \right]} \quad \dots\dots (9.20)$$

Thevenin equivalent circuit, for the amplifier whose output voltage  $V_O$  is given by equation (9.20), is shown in figure (9.20).

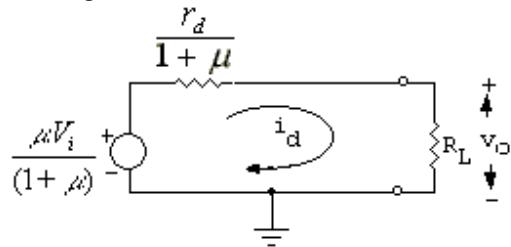


Fig. 9.20

The output resistance  $R_0$  of the source follower circuit is obtained from the figure (9.19) as:

$$R_0 = \frac{r_d}{1 + \mu} \approx \frac{r_d}{\mu} \approx \frac{1}{g_m} \quad \text{----- (9.21)}$$

Provided  $\mu \gg 1$ .

**9.6.3 Common Gate Amplifier:** The circuit in figure (9.21) is the common gate amplifier using field effect transistor. In this circuit the gate is common between input and output terminals. The input signal is applied at source terminal with respect to gate and output is taken across the drain and the gate.

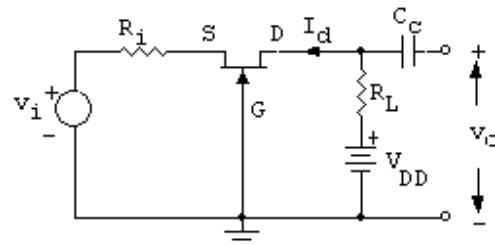


Fig. 9.21

The voltage gain and output resistance of this circuit may be obtained by drawing its equivalent circuit as shown in figure (9.22).

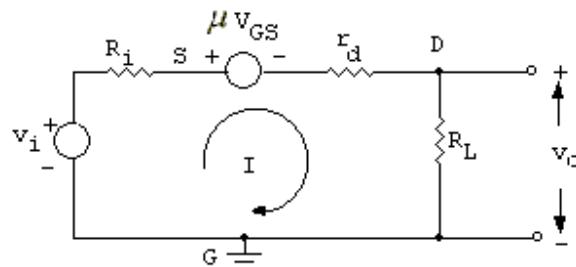


Fig. 9.22

Applying the KVL to this circuit:

$$R_i \cdot I + \mu V_{GS} + (r_d + R_L)I - V_i = 0$$

or

$$I(R_i + r_d + R_L) = V_i - \mu V_{GS}$$

or

$$I = \frac{V_i - \mu V_{GS}}{(R_i + R_L + r_d)} = \frac{V_i - \mu(-V_i + R_i I)}{(R_i + R_L + r_d)}$$

or

$$I \left[ 1 + \frac{\mu \cdot R_i}{R_i + r_d + R_L} \right] = \frac{(1 + \mu)V_i}{(R_i + r_d + R_L)}$$

or

$$I = \frac{(1 + \mu)V_i}{[(1 + \mu)R_i + r_d + R_L]} \quad \text{----- (9.22)}$$

the output voltage  $V_O$  is therefore calculated as:

$$V_O = R_L I = \frac{(1 + \mu)V_i \cdot R_L}{[(1 + \mu)R_i + r_d + R_L]} \quad \text{----- (9.23)}$$

The voltage gain of the common gate amplifier is given by:

$$A_V = \frac{V_O}{V_i} = \frac{(1 + \mu)R_L}{[(1 + \mu)R_i + r_d + R_L]} \quad \text{----- (9.24)}$$

The output resistance of the common gate amplifier can be obtained by drawing the Thevenin's equivalent circuit for the equation (9.23) as shown in figure (9.23).

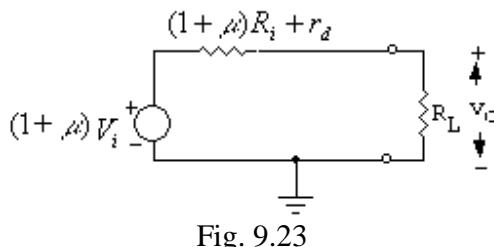


Fig. 9.23

The output resistance from this figure is therefore given by:

$$R_O = (1 + \mu)R_i + r_d \quad \text{----- (9.25)}$$

Example 9.3: The figure (9.24) shows the circuit diagram for common source amplifier with unbypassed source resistance. Prove that

- (i) the expression for the voltage gain  $A_v = \frac{V_O}{V_i} = \frac{-\mu}{r_d + R_L + (1 + \mu)R_s} x R_L$ , and
- (ii) the expression for output resistance  $R_O = r_d + (1 + \mu)R_s$ .

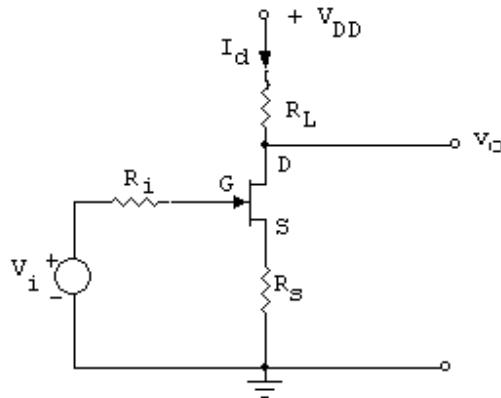


Fig. 9.24

Solution: To find the voltage gain and the output resistance of the circuit we draw small signal model of the given circuit as shown in figure (9.25).

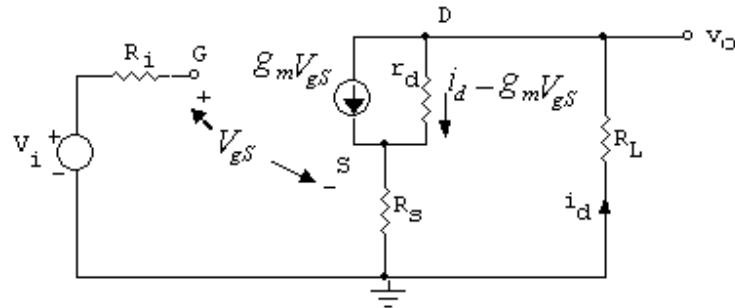


Fig. 9.25

Applying the KVL to the output circuit, we get:

$$i_d \cdot R_L + (i_d - g_m \cdot V_{gs})r_d + R_s \cdot i_d = 0 \quad \text{----- (9.26)}$$

$$\text{and} \quad V_{gs} = V_i - i_d \cdot R_s \quad \text{----- (9.27)}$$

$$\text{or} \quad i_d \cdot (R_L + R_s + r_d) - g_m \cdot r_d (V_i - i_d \cdot R_s) = 0$$

$$\text{or} \quad i_d = \frac{g_m \cdot r_d \cdot V_i}{[R_s(1+\mu) + r_d + R_L]} = \frac{\mu \cdot V_i}{[r_d + (\mu+1)R_s + R_L]}$$

The output voltage is given by:

$$V_o = -i_d \cdot R_L = \frac{-\mu \cdot V_i \cdot R_L}{[r_d + (1+\mu)R_s + R_L]} \quad \text{----- (9.28)}$$

The voltage gain of the amplifier can be obtained as

$$A_v = \frac{V_o}{V_i} = \frac{-\mu}{r_d + R_L + (1+\mu)R_s} x R_L \quad \text{----- (9.29)}$$

Thevenin's equivalent of the equation (9.29) is given by (fig. 9.26):

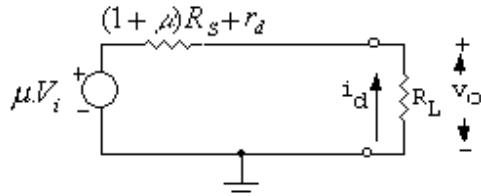


Fig. 9.26

The output resistance  $R_O$  is therefore given by:

$$R_O = r_d + (1+\mu)R_s$$

**Example 9.4:** In Common Source amplifier, a FET has  $r_d = 200 \text{ K}\Omega$  and  $\mu = 18$ . The load resistance  $R_L = 120 \text{ K}\Omega$ . Compute the voltage gain and output resistance of this amplifier.

**Solution:** We know that the voltage gain of the Common Source amplifier is given by:

$$\begin{aligned} A_v &= \frac{-\mu}{r_d + R_L} x R_L \\ &= -\frac{18 \times 10 \text{ K}\Omega}{(200 + 120) \text{ K}\Omega} = -\frac{18}{32} = -6.7 \end{aligned}$$

The output resistance is given by:

$$R_O = r_d = 200 \text{ K}\Omega$$

**Example 9.5:** A Common Source FET amplifier uses load resistance  $R_L = 100 \text{ k}\Omega$  and an unbypassed resistance  $R_s = 10 \text{ K}\Omega$  connected between the source and the ground. The drain resistance of the FET is  $300 \text{ K}\Omega$  and  $\mu = 15$ . Compute the voltage gain and the output resistance of the amplifier.

**Solution:** The voltage gain of the common source amplifier with a source resistance  $R_s$  connected between source and the ground is given by:

$$\begin{aligned} A_v &= \frac{-\mu}{r_d + R_L + (1+\mu)R_s} x R_L \\ &= \frac{-15 \times 100 \text{ K}\Omega}{(300 + 100 + 15 \times 10) \text{ K}\Omega} = \frac{-150}{56} = -2.67 \end{aligned}$$

The output resistance of the amplifier is given by :

$$R_o = r_d + (1 + \mu)R_s = (300 + 16 \times 10)K\Omega = 460K\Omega$$

**9.7 Biasing the FET:** The amplifiers using FET have so far been discussed without showing the biasing arrangement as the d.c. biasing does not produce any significant role for the a.c. signal analysis. However, for the practical point of view the biasing of the FET's is very necessary. Like the bipolar transistors, the FET's have also to be biased properly. The consideration must be given to operate the field effect transistor in the linear region of its characteristic curves. Following are the biasing arrangements generally used in field effect transistors.

**9.7.1 Source Self Bias:** Figure (9.27) shows the self biasing arrangement for the field effect transistor. This type of biasing is generally used in JFET or depletion type MOS

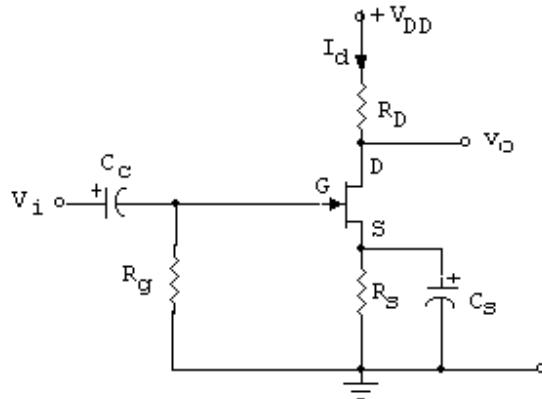


Fig. 9.27

FET's. In this circuit a resistance  $R_g$  is connected between the gate and the ground to bias the gate source junction in the reverse bias. The gate is supposed to be at ground potential as the voltage drop across  $R_g$  is negligibly small due to the very small gate current. To keep the gate at the negative potential with respect to the source, a resistance  $R_s$  is connected between the source and the ground. The voltage drop across  $R_s$  will be equal to  $I_d \cdot R_s$  i.e. the source is at the positive potential ( $I_d \cdot R_s$ ) with respect to ground. The gate is, therefore, at the negative potential with respect to the source since the gate is at the ground potential and source is at the positive potential. However the resistance  $R_s$  will produce a degenerative feedback for the a.c. signal to be applied to the input terminals. To avoid this problem a capacitance  $C_E$  is connected in parallel with the resistance  $R_s$ . The capacitance  $C_E$  bypasses the signal available at the source. Source is therefore called at the signal ground.

**9.7.2 Voltage Divider Biasing:** The voltage divider biasing arrangement can also be applied to the FET amplifiers as shown in figure (9.28).

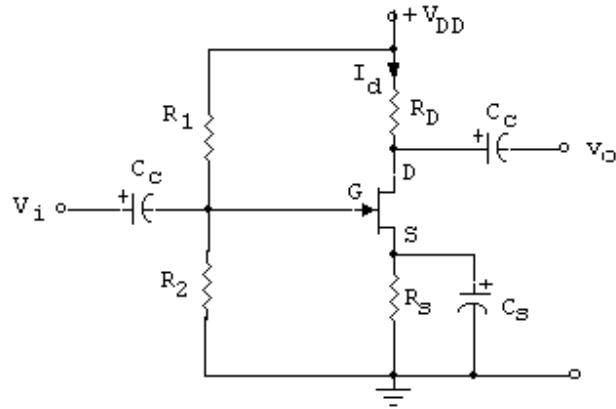


Fig. 9.28

In this case the gate to source voltage  $V_{GS}$  is given by:

$$V_{GS} = V_{GG} - I_d \cdot R_s$$

where  $V_{GG}$  is the voltage between gate and the ground given by:

$$V_{GG} = \frac{V_{DD} \cdot R_2}{R_1 + R_2}$$

**9.8 Common Source Amplifier at High Frequencies:** The common source amplifier at low frequencies has been discussed in the earlier section of this chapter. At high frequencies the inter electrode capacitance will influence the amplifier. So we shall discuss the common source amplifier at high frequencies taking into account the effect of inter electrode capacitances. Figure (9.29) shows the CS amplifier without biasing.

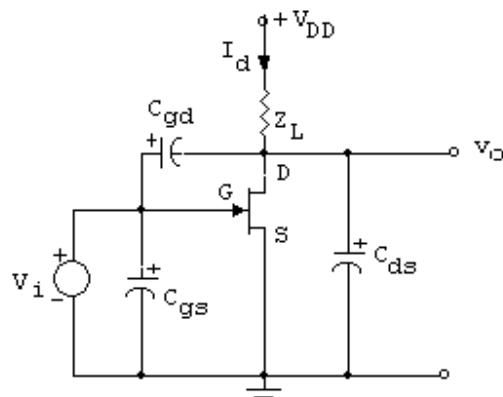


Fig. 9.29

In this circuit the capacitance  $C_{gs}$  is the barrier capacitance between the gate and the source,  $C_{gd}$  is the barrier capacitance between the gate and the drain and the capacitance  $C_{ds}$  is similarly the drain to source capacitance of the channel. The magnitude of these capacitances being very low produces finite reactance at high frequencies. We shall calculate voltage gain, input and output admittances and input capacitance, by

drawing the equivalent circuit of the CS amplifier. Such an equivalent circuit is shown in figure (9.30).

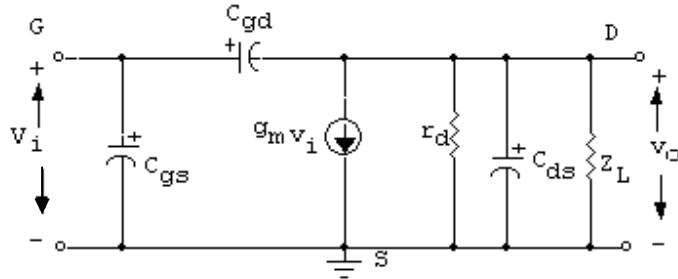


Fig. 9.30

**Voltage Gain:** The output voltage of the circuit shown in figure (9.30) can easily be obtained by applying Norton's theorem. The output voltage  $V_o$  at the drain source terminals is given by:  $V_o = IZ$ , where  $I$  is the short circuit current at the output terminals and the impedance  $Z$  is impedance at the output terminals when all the sources are replaced by their equivalent internal impedances (i.e. the voltage sources are shorted and current sources are open circuited).

So to find the impedance  $Z$ , we short circuit the independent source  $V_i$  (i.e.  $V_i = 0$ ) and open circuit the dependent current source  $g_m V_i$  (i.e. the current source  $g_m V_i$  is removed). So the impedance  $Z$  will be the parallel combination of impedances corresponding to  $Z_L$ ,  $C_{ds}$ ,  $r_d$  and  $C_{gd}$ . Hence

$$\frac{1}{Z} = \frac{1}{Z_L} + \frac{1}{r_d} + \frac{1}{(1/j\omega C_{ds})} + \frac{1}{(j\omega C_{gd})}$$

$$\text{or } Y = \frac{1}{Z} = Y_L + g_d + Y_{ds} + Y_{gd} \quad \text{----- (9.30)}$$

Where  $Y_L = 1/Z_L$  = admittance corresponding to  $Z_L$ .

$g_d = 1/r_d$  = admittance corresponding to  $r_d$ .

$Y_{ds} = 1/C_{ds}$  = admittance corresponding to  $C_{ds}$ .

$Y_{gd} = 1/C_{gd}$  = admittance corresponding to  $C_{gd}$ .

The short circuit current  $I$  is obtained by short circuiting the drain to source terminals as:

$$I = -g_m V_i + V_i (1/j\omega C_{ds}) = (-g_m + Y_{ds}) V_i \quad \text{----- (9.31)}$$

The voltage gain is therefore given by:

$$\begin{aligned}
A_V &= \frac{V_o}{V_i} = \frac{Z \cdot I}{V_i} = \frac{I}{V_i \cdot Y} \\
&= \frac{(-g_m + Y_{ds})V_i}{(Y_L + g_d + Y_{ds} + Y_{gd})V_i} \\
A_V &= \frac{-g_m + Y_{ds}}{Y_L + g_d + Y_{ds} + Y_{gd}}
\end{aligned} \quad \text{----- (9.32)}$$

**Input Admittance :** To obtain the input admittance of the figure (9.30), we can apply the Miller's theorem as a capacitance  $C_{gd}$  is connected between the gate and the drain.

This capacitance can be replaced by impedance  $Z_1 = \frac{1}{j\omega C_{gd} \cdot (1 - A_V)}$  connected

between the gate and the source and another impedance  $Z_2 = \frac{A_V}{j\omega C_{gd} \cdot (A_V - 1)}$  connected between the drain and the source. Hence the input admittance is given by :

$$\begin{aligned}
Y_i &= Y_{gs} + \frac{1}{Z_1} = Y_{gs} + j\omega C_{gd} \cdot (1 - A_V) \\
\text{or} \quad Y_i &= Y_{gs} + Y_{gd} \cdot (1 - A_V)
\end{aligned} \quad \text{----- (9.33)}$$

**Input Capacitance:** Input capacitance is important to find since it is needed in cascaded amplifiers. In such an amplifier the output of one stage is used as the input of the second stage. The input of the second stage acts as shunt across the output of the first stage. So the input capacitance  $C_i$  of the second stage is shunted by the output load resistance of the first stage.

Let the drain circuit impedance  $Z_L$  be a pure resistance and for the low frequency, the gain of the amplifier is given by:

$$A_v = \frac{-\mu}{r_d + Z_L} x Z_L = -gm \cdot Z_L'$$

$$\text{where } Z_L' = \frac{r_d \cdot Z_L}{r_d + Z_L}$$

In this case the equation (9.33) becomes:

$$\frac{Y_i}{j\omega} \equiv C_i = C_{gs} + (1 + g_m \cdot Z_L') C_{gd} \quad \text{----- (9.34)}$$

From this equation it is clear that there is an increase in the input capacitance  $C_i$  due to the inter electrode capacitance between the gate and the drain. This increase in the input capacitance of the amplifier is called as the Miller effect.

**Output Admittance :** The output admittance is obtained by looking back from output terminals into drain with  $V_i$  is kept zero. If the input source is shorted, then  $r_d$ ,  $C_{dS}$  and  $C_{gd}$  will seem to be in parallel. Thus the output admittance will be given by:

$$Y_O = Y_{dS} + Y_{gd} \quad \text{----- (9.35)}$$

**9.9 Common Drain Amplifier (Source Follower) at High Frequencies:** Figure (9.31) shows the CD amplifier without biasing and having the inter electrode capacitances.

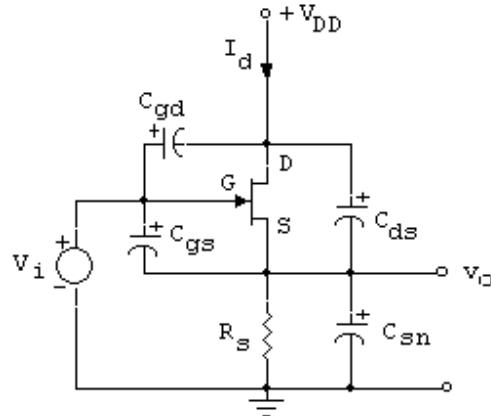


Fig. 9.31

Now we shall calculate voltage gain, input and output admittances and input capacitance, by drawing the equivalent circuit of the CS amplifier. Such an equivalent circuit is shown in figure (9.32).

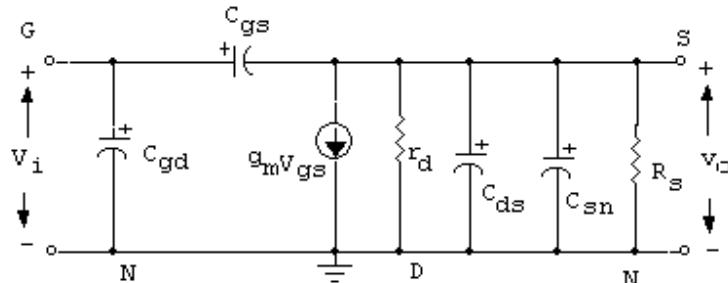


Fig. 9.32

**Voltage Gain:** In this circuit  $C_{sn}$  is the capacitance between the source and the ground terminal. The output voltage can be obtained as:

$$V_o = Z \cdot I \quad \text{----- (9.36)}$$

where  $I$  is the short circuit current across the terminals S and N; and  $Z$  is the impedance at the output terminals (S and N) when all the source have been replaced by their internal impedances (Norton's resistance).

The short circuit current is given by:

$$I = g_m \cdot V_{gS} + V_i \cdot (1/j\omega C_{gS}) = g_m \cdot V_{gS} + V_i \cdot Y_{gS}$$

But  $V_{gS} = V_i - V_o = V_i - Z \cdot I$

or  $I(1 + g_m \cdot Z) = g_m \cdot V_i + V_i \cdot Y_{gS}$

or  $I = \frac{(g_m + Y_{gS}) \cdot V_i}{(1 + g_m \cdot Z)}$

or  $V_o = I \cdot Z = \frac{(g_m + Y_{gS}) \cdot V_i}{(Y + g_m)} \quad \text{----- (9.37)}$

The value of admittance  $Y$  is given by:

$$Y = \frac{1}{Z} = \frac{1}{R_s} + g_d + Y_{sn} + Y_{ds} + Y_{gS} \quad \text{----- (9.38)}$$

From equations (9.37) & (9.38) we have:

$$A_V = \frac{V_o}{V_i} = \frac{(g_m + Y_{gS}) R_s}{1 + (g_m + g_d + Y_{sn} + Y_{ds} + Y_{gS}) R_s} \quad \text{----- (9.39)}$$

**Input Admittance :** The input admittance can be obtained by applying the Miller's theorem to the capacitance  $C_{gS}$ . Thus the input admittance is given by:

$$Y_i = j\omega C_{gd} + j\omega C_{gS}(1 - A_V) \approx j\omega C_{gd} \quad \text{----- (9.40)}$$

as  $A_V \approx 1$  for source follower.

**Input Capacitance:** The input capacitance  $C_i$  is given by:

$$C_i = C_{gd} + (1 - A_V) C_{gS} \quad \text{----- (9.41)}$$

**Output Admittance:** The output admittance without considering the load resistance  $R_s$  is given by:

$$Y_o = g_m + g_d + Y_{ds} + Y_{gS} + Y_{sn} \quad \text{----- (9.42)}$$

**Example 9.6:** Using the high frequency model of the field effect transistor, show that for common gate amplifier with  $R_s = 0$  and  $C_{ds} = 0$ .

(i) Voltage gain  $A_V = \frac{(g_m + g_d) R_L}{1 + R_L(g_d + j\omega C_{gS})}$

(ii) Input admittance  $Y_i = g_m + g_d(1 - A_V) + j\omega C_{gS}$

**Solution:** To find the voltage gain and input admittance of the common gate amplifier we draw the circuit of CG amplifier with its high frequency model as shown in figure (9.33).

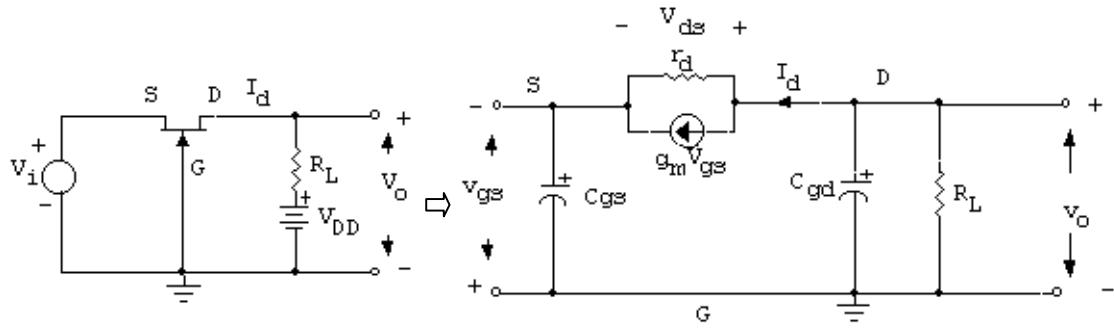


Fig. 9.33

(i) From this circuit, the drain current  $I_d$  is given by:

$$I_d = g_m \cdot V_{gs} + \frac{V_{ds}}{r_d} = g_m \cdot V_{gs} + g_d (V_{ds} + V_{gs})$$

Since  $V_{ds} = V_{dg} + V_{gs}$

$$\text{or} \quad I_d = (g_m + g_d) \cdot V_{gs} + g_d \cdot V_{dg} \quad \dots \dots \quad (9.43)$$

The output voltage is given by:

$$V_{dg} = -I_d \left( \frac{R_L \cdot (1/j\omega C_{gd})}{R_L + (1/j\omega C_{gd})} \right)$$

$$\text{or} \quad I_d = \frac{-V_{dg} (1 + j\omega C_{gd} \cdot R_L)}{R_L} \quad \dots \dots \quad (9.44)$$

From equations (9.43) & (9.44), we have:

$$(g_m + g_d) \cdot V_{gs} + g_d \cdot V_{dg} = \frac{-V_{dg} (1 + j\omega C_{gd} \cdot R_L)}{R_L}$$

$$\text{or} \quad (g_m + g_d) \cdot R_L \cdot V_{gs} = -V_{dg} (1 + j\omega C_{gd} \cdot R_L + g_d \cdot R_L)$$

$$\text{or} \quad A_V = \frac{V_{ds}}{-V_{gs}} = \frac{(g_m + g_d) \cdot R_L}{1 + (g_d + j\omega C_{gd}) R_L}$$

(ii) Input admittance will be obtained by applying Miller's theorem to the resistance  $r_d$ . In this case a resistance  $r_d/(1-A_V)$  will be in parallel with  $C_{gs}$ .

So

$$Y_i = g_m + \frac{1}{[r_d/(1 - A_V)]} + \frac{1}{1/j\omega C_{gs}}$$

or

$$Y_i = g_m + g_d(1 - A_V) + j\omega C_{gs}$$

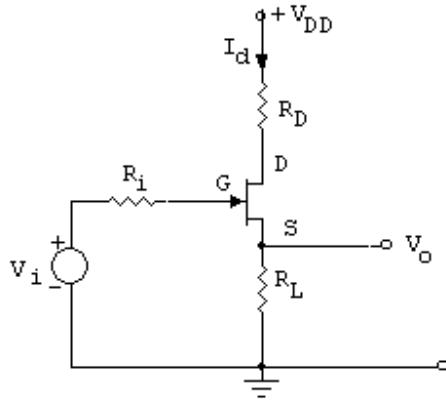
### Problems:

1. What are the advantages of the FET over the conventional transistors? What do the terms Unipolar and Bipolar refer to?
2. Define transconductance  $g_m$ , drain resistance  $r_d$  and amplification factor  $\mu$  of a FET. What is the relation between these three constants?
3. Draw the drain characteristics of an N – channel JFET. Explain the shape of these curves qualitatively.
4. Sketch the basic structure of N – channel Junction Field Effect Transistor and explain its working. Give its circuit symbol also.
5. Give the cross section of a P – channel enhancement MOSFET and explain its working. Give the two circuit symbols of this MOSFET.
6. Sketch the basic structure of N – channel depletion type MOSFET and explain its working. Give its two circuit symbols also.
7. Draw and explain the drain and transfer characteristics of a P – channel enhancement MOSFET.
8. Draw and explain the drain and transfer characteristics of an N – channel depletion MOSFET.
9. Draw the small signal model of a field effect transistor.
10. Draw the circuit of common source amplifier and find the expression for the voltage gain and output resistance of this amplifier.
11. Draw the circuit of common drain amplifier and find the expression for the voltage gain and output resistance of this amplifier.
12. Draw the circuit of common gate amplifier and find the expression for the voltage gain and output resistance of this amplifier.
13. What is source follower circuit? Draw the circuit of source follower and show that its voltage gain is almost unity. Find also the expression for the output resistance of the source follower.
14. If the two identical FETs are connected in parallel then prove that the effective transconductance is doubled and drain resistance is halved. The amplification factor remains unchanged.

15. Draw the small signal model of a FET and show that the FET behaves as a voltage controlled current source (VCCS).
16. The figure given below shows the circuit diagram for common drain amplifier with unbypassed drain resistance  $R_d$ . Prove that

(i) the expression for the voltage gain

$$A_v = \frac{V_o}{V_i} = \frac{\mu V_i}{r_d + R_D + (1 + \mu)R_L} \times R_L, \text{ and (ii) the expression for output resistance } R_o = \frac{r_d + R_D}{\mu + 1}.$$



17. A Common Source amplifier uses FET having drain resistance  $r_d = 10 K\Omega$  and  $\mu = 16$ . Calculate the voltage and the output resistance of the amplifier for load resistance equal to (i)  $100 K\Omega$  (ii)  $200 K\Omega$  and (iii)  $1 M\Omega$ .

Ans.: (i) -8,  $100 K\Omega$  (ii) – 10.67,  $100 K\Omega$  (iii)- 14.5,  $100 K\Omega$ .

18. A Common Source FET amplifier uses load resistance  $R_L = 100 k\Omega$  and an unbypassed resistance  $R_S$  connected between the source and the ground. The drain resistance of the FET is  $200 K\Omega$  and transconductance  $g_m = 0.1$  millimhos. Compute the voltage gain and the output resistance of the amplifier for  $R_S$  equal to :

(i)  $2 K\Omega$  (ii)  $10 K\Omega$  and (iii)  $20 K\Omega$ .

Ans.: (i) – 5.85,  $242 K\Omega$ , (ii) – 3.9,  $410 K\Omega$  (iii) – 2.78,  $620 K\Omega$

19. A source follower amplifier uses FET having  $r_d = 200 K\Omega$  and  $\mu = 20$ . The load resistance connected between the source and the ground is  $120 K\Omega$ . Calculate the voltage gain and output resistance of the amplifier.

(Ans.: 0.88,  $9.5 K\Omega$ )

# 10

## Multistage Amplifiers

In many applications of electronic circuits, the gain of the single stage transistor amplifier is not sufficient to the desired level, so more stages of amplification are generally used. In such cases the output of one stage is connected to the second stage of the amplifier through some coupling network. In this chapter different types of coupling in addition to the classification of amplifiers will be discussed. High frequency amplifiers, power amplifiers as well as distortion in amplifiers will also be discussed.

**10.1 Classification of amplifiers:** Amplifiers may be classified into the following ways:

- (i) According to frequency range
- (ii) According to the method of operation
- (iii) According to their applications
- (iv) According to the method of inter stage coupling

**(i) According to frequency range :** The amplifiers are further classified according to frequency range as follows:

- (a) **D.C. amplifiers:** These amplifiers are capable of amplifying even zero frequency signals, i.e. D.C. signals.
- (b) **Audio frequency amplifiers:** The amplifiers capable of amplifying the signal of frequency range 20 Hz to 20 KHz are known as Audio frequency amplifiers.
- (c) **Video amplifiers:** These amplifiers amplify the signal of frequency up to a few megahertz.
- (d) **Radio frequency amplifiers:** Its frequency range operation is a few kilohertz to hundreds of megahertz.
- (e) **Ultrahigh – frequency amplifiers:** The frequency range of operation of these amplifiers is up to hundreds or thousands of megahertz.

**(ii) According to the method of operation:** The method of operation means the position of the operating point. The amplifiers are thus classified according to the method of operation as follows:

- (a) **Class A amplifiers:** In class A amplifiers the operating point is chosen in the middle of the load line such that the output current follows for the entire input signal.
- (b) **Class B amplifiers:** In class B amplifiers the operating point is fixed at an extreme end of the characteristics, so that quiescent power is very small. In this case the output current flows only for half of the input sinusoidal signal.
- (c) **Class AB amplifiers:** The operating point, in this class AB amplifier, is fixed between the two extremes defined for class A and class B amplifiers. Hence in this class of amplifiers the output current is zero for a small part but less than half of the input sinusoidal signal.
- (d) **Class C amplifiers:** The operating point in this class of amplifiers is fixed such that the output current flows only for less than half of the input sinusoidal.

**(iii) According to their applications:** The classification according to use includes voltage, power, current or general purpose amplifiers.

**(iv) According to the method of inter - stage coupling:** The amplifiers according to the method of inter stage coupling may be classified as follows:

- (a) **Resistance – capacitance coupling :** When the coupling network, comprising resistance and capacitance is used to couple the output of one stage to the input of second stage then the amplifiers of this type are called as R – C coupled amplifiers.
- (b) **Transformer coupling:** Amplifiers using this coupling are known as transformer coupled amplifiers. In these amplifiers transformers are used for inter stage coupling. The transformer coupled amplifiers saves the power dissipation.
- (c) **Direct coupling:** For applications where the signal frequency is very low (may be below 10 Hz), the coupling networks discussed above are not used. In such cases output of the one stage is directly coupled to the input of the succeeding stages. The amplifiers using direct coupling are known as direct coupled amplifiers.

**10.2 R – C Coupled Amplifier :** The circuit diagram of two stage R – C coupled amplifier is shown in figure (10.1). In this circuit two single stage common emitter amplifiers are coupled through  $R_{C1}$  and  $C_C$  network.

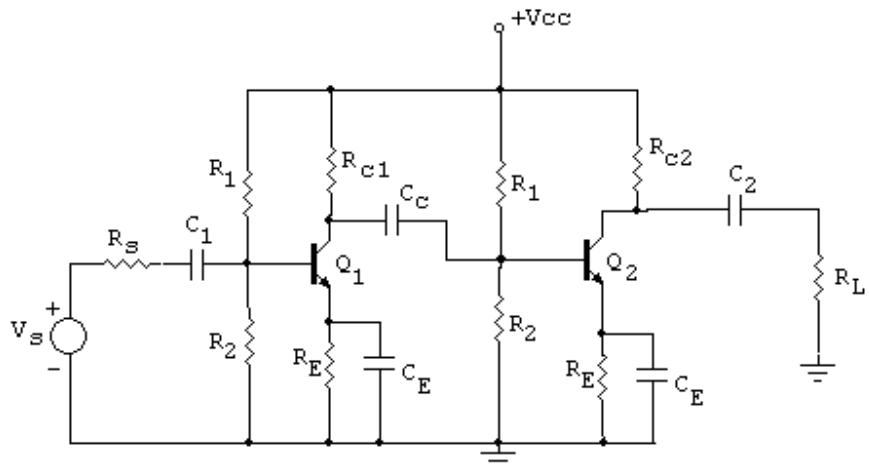
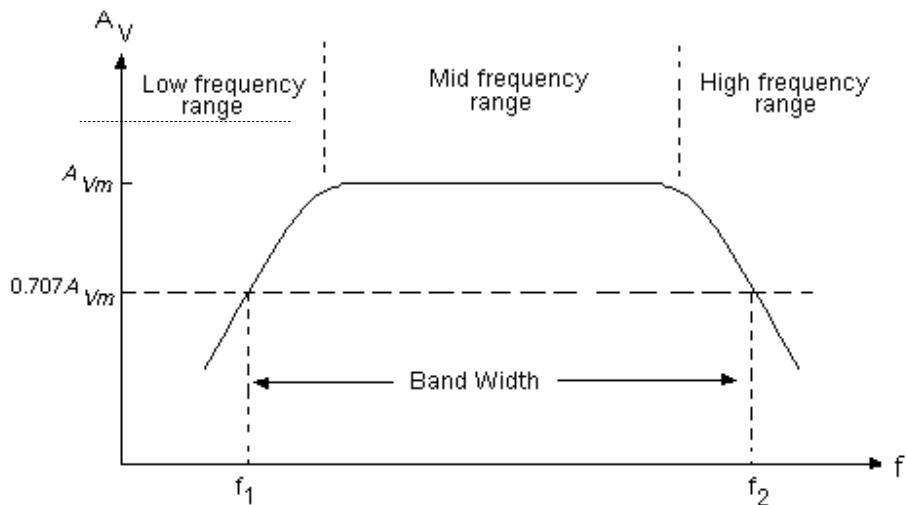


Fig. 10.1

In this circuit the resistances  $R_1$ ,  $R_2$ ,  $R_{C1}$ ,  $R_{C2}$  and  $R_E$  are used to provide the self biasing and bias stabilization to the two transistors  $Q_1$  and  $Q_2$ . The coupling capacitor  $C_C$  blocks the quiescent d.c. current and prevents it from appearing at the input of the second stage. However,  $C_C$  is so chosen that it offers negligible reactance for signal frequencies. Thus it couples the signal effectively to the second stage.

As is well known, the emitter resistance  $R_E$  is used to provide good stabilization to the transistor circuits; and larger the value of this resistance better will be biasing stability. But the larger value of  $R_E$  introduces larger amount of negative feedback in the circuit which on the contrary reduces the gain of the amplifier. To overcome this difficulty a by-pass capacitor  $C_E$  is connected in parallel with the emitter resistance  $R_E$ . The choice of a larger value for  $C_E$  makes the emitter at the signal ground.

**10.2.1 Frequency Response:** The curve representing the variation of gain of the amplifier with frequency is known as frequency response curve. It is shown for RC coupled amplifier in figure (10.2). The frequency response of

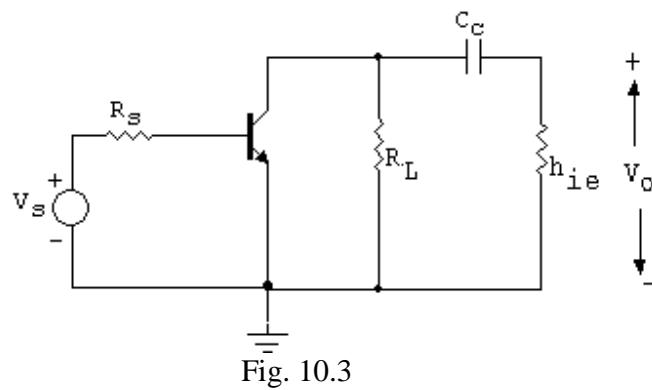


the *RC* coupled amplifier will be studied over a band of frequencies. The entire frequency range is divided into three regions namely low frequency region, mid frequency region and high frequency region. The coupling and the emitter bye pass capacitances are assumed to be large in the mid and high frequency region so that at the signal frequency these can be considered as short circuited. But at lower frequencies, their reactances will not be negligible. Thus the gain of an *RC* coupled amplifier will fall off at lower frequencies. Generally the frequency response of this amplifier will be governed by the two time constants.

- (i) The coupling capacitor  $C_C$  together with the input impedance of the second stage of the amplifier will form the simple *RC* high pass filter. The effect of this time constant will be that the gain of the amplifier will reduce at lower frequencies.
- (ii) The second time constant is due to the emitter bye pass capacitor  $C_E$ . The parallel combination of  $R_E$  and  $C_E$  offers the finite impedance in the emitter circuit at lower frequencies. As a result of which the gain of the amplifier decreases at lower frequencies.

Now the effect of these two time constants on the frequency response of this amplifier will be discussed.

**10.2.2 Effect of coupling capacitor:** To study the effect of time constant due to the coupling capacitor  $C_C$  together with input impedance of second stage of the amplifier, the effect of second time constant due to  $R_E$  and  $C_E$  is assumed to be negligible .As a result the emitter is assumed to be shorted to ground. Also the parallel combination of resistances  $R_1$  and  $R_2$  is assumed to be much larger than  $R_i$ . So the biasing resistances are not taking into account in the equivalent circuit. The a.c. equivalent circuit and the approximate *h* – parameter model of the amplifier are shown in figures (10.3) and (10.4) respectively. In the approximate *h* – parameter model, only the parameters  $h_{ie}$  and  $h_{fe}$  are considered and  $h_{oe}$  and  $h_{re}$  are neglected.



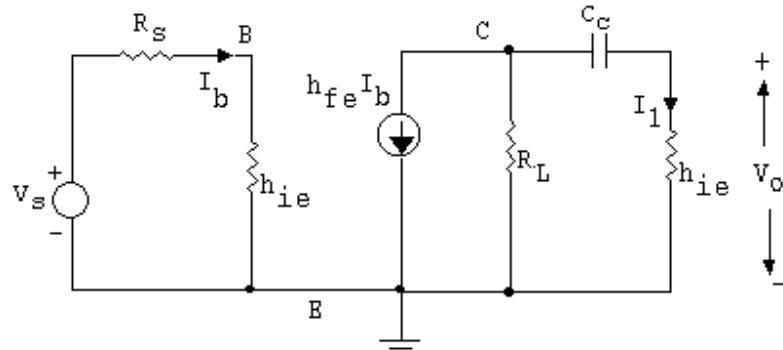


Fig. 10.4

Considering the figure (10.4), the effective load impedance  $Z_L$  at the collector of the first stage of the amplifier is the parallel combination of  $R_L$  and  $(h_{ie} + \frac{1}{j\omega C_c})$ .

$$Z_L = \frac{R_L(h_{ie} + \frac{1}{j\omega C_c})}{R_L + h_{ie} + \frac{1}{j\omega C_c}} \quad \text{----- (10.1)}$$

From the figure (10.4), we have:

$$\begin{aligned} I_1(h_{ie} + \frac{1}{j\omega C_c}) &= h_{fe} I_b Z_L \\ \text{or} \quad I_1 &= \frac{h_{fe} I_b Z_L}{(h_{ie} + \frac{1}{j\omega C_c})} \end{aligned} \quad \text{----- (10.2)}$$

The output voltage  $V_o$  is given by:

$$\begin{aligned} V_o &= -I_1 h_{ie} \\ \text{or} \quad V_o &= -\frac{h_{fe} h_{ie} I_b Z_L}{(h_{ie} + \frac{1}{j\omega C_c})} \end{aligned} \quad \text{----- (10.3)}$$

The input voltage  $V_s$  is given by:

$$V_s = (R_s + h_{ie}) I_b \quad \text{----- (10.4)}$$

Using the equations (10.3) & (10.4), the voltage gain  $A_{VLI}$  is given as :

$$A_{VLI} = \frac{V_o}{V_s} = \frac{-h_{fe} h_{ie} I_b Z_L}{(h_{ie} + \frac{1}{j\omega C_c}) I_b (R_s + h_{ie})}$$

$$\text{or} \quad = \frac{-h_{fe} \cdot h_{ie} \cdot Z_L}{(h_{ie} + \frac{1}{j\omega C_C}) \cdot (R_S + h_{ie})}$$

Putting the value of  $Z_L$  from equation (10.1),  $A_{VL1}$  is given as:

$$A_{VL1} = \frac{-h_{fe} \cdot h_{ie} \cdot R_L (h_{ie} + \frac{1}{j\omega C_C})}{(h_{ie} + \frac{1}{j\omega C_C}) \cdot (R_S + h_{ie}) \cdot (R_L + h_{ie} + \frac{1}{j\omega C_C})}$$

$$= \frac{-h_{fe} \cdot h_{ie} \cdot R_L}{(R_S + h_{ie}) \cdot (R_L + h_{ie} + \frac{1}{j\omega C_C})} \quad \text{----- (10.5)}$$

$$\text{or} \quad A_{VL1} = \frac{-h_{fe} \cdot h_{ie} \cdot R_L}{(R_S + h_{ie}) \cdot (R_L + h_{ie}) \cdot (1 + \frac{1}{j\omega \cdot (R_L + h_{ie}) \cdot C_C})} \quad \text{----- (10.6)}$$

This is the low frequency gain when only the effect of coupling capacitor is considered. The mid frequency gain of the amplifier is obtained by neglecting the effect of  $C_C$ . So by putting the factor  $(\frac{1}{j\omega C_C})$  equal to zero in equation (10.5), the mid frequency gain of the amplifier may be obtained as:

$$A_{Vm} = \frac{-h_{fe} \cdot h_{ie} \cdot R_L}{(R_S + h_{ie}) \cdot (R_L + h_{ie})} \quad \text{----- (10.7)}$$

From equations (10.6) & (10.7), we have:

$$A_{VL1} = \frac{A_{Vm}}{\left(1 + \frac{1}{j\omega \cdot (R_L + h_{ie}) \cdot C_C}\right)}$$

$$\text{or} \quad |A_{VL1}| = \frac{|A_{Vm}|}{\sqrt{1 + \left[\frac{1}{\omega \cdot (R_L + h_{ie}) \cdot C_C}\right]^2}} \quad \text{----- (10.8)}$$

At  $\omega = \frac{1}{(R_L + h_{ie}) \cdot C_C}$ , the voltage gain of the amplifier reduces to  $\frac{1}{\sqrt{2}}$  (or -3 db) of the mid frequency gain of the amplifier, i.e.,

$$|A_{VL1}| = \frac{|A_{Vm}|}{\sqrt{2}}$$

This frequency is known as the lower cutoff frequency,

$$\omega_{L1} = \frac{1}{(R_L + h_{ie}).C_C}$$

or

$$f_{L1} = \frac{1}{2\pi(R_L + h_{ie}).C_C}$$

And the low frequency gain is reduced to

$$|A_{VL1}| = \frac{|A_{Vm}|}{\sqrt{1 + \left[ \frac{f_{L1}}{f} \right]^2}}$$

**10.2.3 Effect of Emitter Bye - pass Capacitor:** The effect of second time constant due to  $R_E$  and  $C_E$  will be studied and the coupling capacitor  $C_C$  is assumed to be large enough so that its reactance is negligibly small and it has no effect on the response. The biasing resistances are also not being taken into account in the equivalent circuit. The a.c. equivalent circuit and the approximate  $h$  – parameter model of the amplifier are shown in figures (10.5) and (10.6) respectively. In the approximate  $h$  – parameter model only the parameters  $h_{ie}$  and  $h_{fe}$  are considered and  $h_{oe}$  and  $h_{re}$  are neglected.

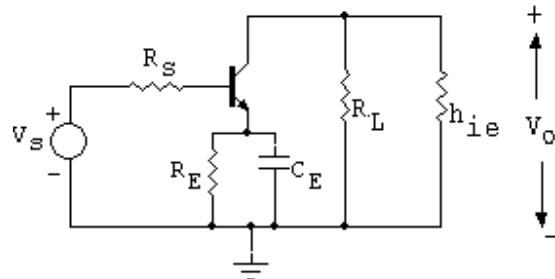


Fig. 10.5

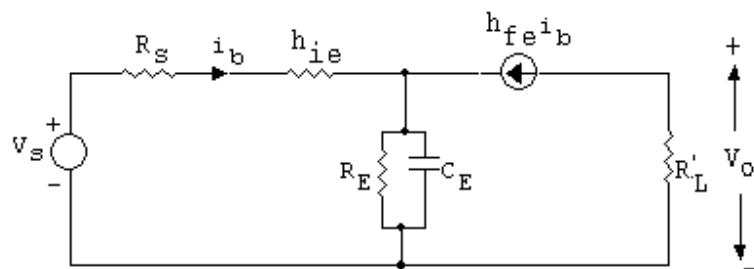


Fig. 10.6

With reference to the figure (10.6) the output voltage  $V_o$  is given by:

$$V_o = -h_{fe} i_b \cdot R_L' \quad \text{----- (10.9)}$$

where  $R_L'$  is the parallel combination of  $R_L$  and  $h_{ie}$ .

Applying the KVL to the input circuit we get:

$$V_S = (R_S + h_{ie}) i_b + Z_E (1 + h_{fe}) i_b \quad \text{----- (10.10)}$$

$$\text{or } i_b = \frac{V_S}{R_S + h_{ie} + (1 + h_{fe}) Z_E} \quad \text{----- (10.11)}$$

where  $Z_E$  is the parallel combination of  $R_E$  and  $C_E$  given by:

$$Z_E = \frac{(R_E) \left( \frac{1}{j\omega C_E} \right)}{\left( R_E + \frac{1}{j\omega C_E} \right)} = \frac{R_E}{1 + j\omega R_E C_E} \quad \text{----- (10.12)}$$

From equations (10.9) and (10.11),  $V_o$  is given by:

$$V_o = \frac{-V_S \cdot h_{fe} \cdot R_L'}{R_S + h_{ie} + (1 + h_{fe}) Z_E}$$

The voltage gain at low frequency is given by:

$$A_{VL.2} = \frac{V_o}{V_S} = \frac{-h_{fe} \cdot R_L'}{R_S + h_{ie} + (1 + h_{fe}) Z_E} \quad \text{----- (10.13)}$$

Note that when  $\omega$  is large (in the mid frequency region), the voltage gain known as mid band gain is given by:

$$A_{VM} = \frac{-h_{fe} \cdot R_L'}{R_S + h_{ie}} \quad \text{----- (10.14)}$$

Since  $Z_E$  will behave as short circuit at the mid and high frequency region.

Put the value of  $Z_E$  from equation (10.12) into equation (10.13) we have:

$$A_{VL.2} = \frac{-h_{fe} \cdot R_L'}{R_S + h_{ie} + \frac{(1 + h_{fe}) R_E}{1 + j\omega R_E C_E}}$$

$$\text{or } = \frac{-h_{fe} \cdot R_L' \cdot (1 + j\omega R_E C_E)}{(R_S + h_{ie})(1 + j\omega R_E C_E) + (1 + h_{fe}) \cdot R_E}$$

$$\begin{aligned}
\text{or} \quad &= \frac{-h_{fe} \cdot R_L \cdot (1 + j\omega R_E C_E)}{\{R_S + h_{ie} + (1 + h_{fe}) \cdot R_E\} + \{j\omega R_E C_E (R_S + h_{ie})\}} \\
&= \left( \frac{-h_{fe} \cdot R_L}{R_S + h_{ie} + (1 + h_{fe}) \cdot R_E} \right) \left( \frac{1 + j\omega R_E C_E}{1 + j\omega \left( \frac{R_E C_E (R_S + h_{ie})}{R_S + h_{ie} + (1 + h_{fe}) R_E} \right)} \right) \\
&= \left( \frac{-h_{fe} \cdot R_L}{R_S + h_{ie} + (1 + h_{fe}) \cdot R_E} \right) \left( \frac{1 + j\omega \tau_1}{1 + j\omega \tau_2} \right)
\end{aligned}$$

where  $\tau_1 = R_E C_E$

$$\text{and } \tau_2 = \frac{R_E C_E (R_S + h_{ie})}{R_S + h_{ie} + (1 + h_{fe}) R_E}$$

Generally  $(1 + h_{fe}) R_E \gg (R_S + h_{ie})$ , so  $\tau_2 \ll \tau_1$ .

The voltage gain at  $\omega = \frac{1}{\tau_2}$  is, therefore, given by:

$$A_{VL.2} = \left( \frac{-h_{fe} \cdot R_L}{R_S + h_{ie} + (1 + h_{fe}) \cdot R_E} \right) \left( \frac{1 + j \cdot \left( \frac{\tau_1}{\tau_2} \right)}{1 + j} \right) \quad \text{----- (10.15)}$$

For  $\tau_2 \ll \tau_1$ , the voltage gain is approximated as:

$$\begin{aligned}
A_{VL.2} &= \left( \frac{-h_{fe} \cdot R_L}{R_S + h_{ie} + (1 + h_{fe}) \cdot R_E} \right) \left( \frac{j \cdot \left( \frac{\tau_1}{\tau_2} \right)}{1 + j} \right) \\
\text{or } |A_{VL.2}| &= \frac{1}{\sqrt{2}} \left( \frac{h_{fe} \cdot R_L \left( \frac{\tau_1}{\tau_2} \right)}{R_S + h_{ie} + (1 + h_{fe}) \cdot R_E} \right)
\end{aligned}$$

Putting the values of  $\tau_1$  and  $\tau_2$ , in the above equation the voltage gain is given by:

$$\text{or } |A_{VL.2}| = \frac{1}{\sqrt{2}} \left| h_{fe} \cdot R_L \left( \frac{\frac{R_E \cdot C_E}{R_E \cdot C_E (R_S + h_{ie})}}{R_S + h_{ie} + (1 + h_{fe}) R_E} \right) \right|$$

$$|A_{VL.2}| = \frac{1}{\sqrt{2}} \left( \frac{h_{fe} \cdot R_L}{R_S + h_{ie}} \right) \quad \text{----- (10.16)}$$

$$\text{or } \left| \frac{A_{VL.2}}{A_{VM}} \right| = \frac{1}{\sqrt{2}} \quad \text{----- (10.17)}$$

$$\text{From equation (10.14)} \quad |A_{VM}| = \frac{h_{fe} \cdot R_L}{R_S + h_{ie}} \quad \text{----- (10.18)}$$

Further it is clear from the equation (10.17) that the voltage gain of the amplifier has dropped by 3 db from the gain at the mid frequency region. In other words, at  $\omega = \frac{1}{\tau_2}$  the magnitude of the gain is  $\frac{1}{\sqrt{2}}$  times the mid frequency gain. This frequency is called the lower cut off frequency, which may be given by:

$$\omega_{L2} = \frac{1}{\tau_2} = \frac{R_S + h_{ie} + (1 + h_{fe}) R_E}{R_E \cdot C_E (R_S + h_{ie})}$$

If  $(1 + h_{fe}) R_E \gg (R_S + h_{ie})$  then the lower cut off frequency is given by:

$$\omega_{L2} = \frac{(1 + h_{fe})}{C_E (R_S + h_{ie})} \quad \text{----- (10.19)}$$

$$\text{or } f_{L2} = \frac{1 + h_{fe}}{2\pi \cdot (R_S + h_{ie}) \cdot C_E} \quad \text{----- (10.20)}$$

Note that the expression for the lower cut off frequency  $f_{L2}$  does not contain the emitter resistance, so the lower 3 db frequency is dependent on the transistor parameters and the source resistance.

**10.2.4 High Frequency Response :** The variation of voltage gain of the RC coupled amplifier in the high frequency region will now be studied. In this region the coupling capacitor and emitter bye pass capacitor will offer negligibly low reactance and these

capacitances will behave as short circuited. However, in this range of frequencies, effective shunt capacitance  $C_o$  due to the input and output capacitances of the devices along with the associated stray wiring capacitance plays important role in the variation of the voltage gain of the amplifier. The detailed discussion of these capacitances will be illustrated in the following section using the high frequency  $\pi$  model of the transistor. The values of these capacitances are very low, so at high frequencies its reactance will considerably be low. The effective load impedance at the collector of the first stage will be the parallel combination of the  $R_L$ ,  $h_{ie}$  and the reactance of  $C_o$ . As a result the gain of the amplifier will decrease with the increase in frequency.

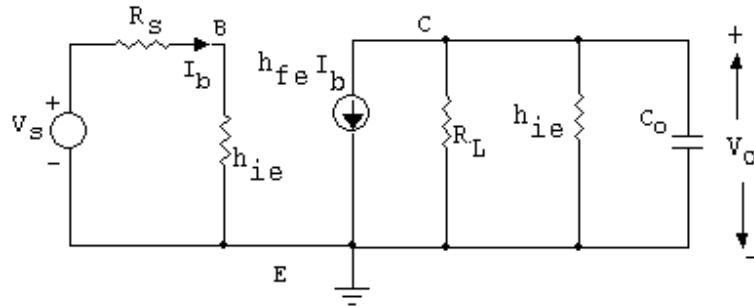


Fig. 10.7

Considering the figure (10.7), the effective load impedance  $Z_L$  is given by:

$$\frac{1}{Z_L} = \frac{1}{R_L} + \frac{1}{h_{ie}} + j\omega C_o$$

$$Z_L = \frac{R_L h_{ie}}{R_L + h_{ie} + j\omega C_o h_{ie} R_L} \quad \text{----- (10.21)}$$

The output voltage  $V_o$  is given by:

$$V_o = -h_{fe} I_b Z_L$$

The input voltage  $V_s$  is given by:

$$V_s = (R_s + h_{ie}) I_b \quad \text{----- (10.22)}$$

Using the equations (10.21) & (10.22), the voltage gain  $A_{VH}$  is given as :

$$A_{VH} = \frac{V_o}{V_s} = \frac{-h_{fe} I_b Z_L}{I_b (R_s + h_{ie})} = \frac{-h_{fe} Z_L}{R_s + h_{ie}}$$

Putting the value of  $Z_L$  from equation (10.21),  $A_{VH}$  is given as:

$$A_{VH} = \frac{-h_{fe} h_{ie} R_L}{(R_s + h_{ie})(R_L + h_{ie} + j\omega C_o h_{ie} R_L)} \quad \text{----- (10.23)}$$

The mid frequency gain of the amplifier is obtained by neglecting the effect of  $C_o$ . So the mid frequency gain of the amplifier may be obtained as:

$$A_{Vm} = \frac{-h_{fe} \cdot h_{ie} \cdot R_L}{(R_S + h_{ie})(R_L + h_{ie})} \quad \text{----- (10.24)}$$

From equations (10.23) & (10.24), we have:

$$\begin{aligned} A_{VH} &= \frac{A_{Vm}}{\left(1 + \frac{j\omega C_o h_{ie} R_L}{R_L + h_{ie}}\right)} \\ \text{or } |A_{VH}| &= \frac{|A_{Vm}|}{\sqrt{1 + \left[\frac{\omega C_o h_{ie} R_L}{(R_L + h_{ie})}\right]^2}} \quad \text{----- (10.25)} \end{aligned}$$

At  $\omega = \frac{R_L + h_{ie}}{R_L h_{ie} \cdot C_o}$ , the voltage gain of the amplifier reduces to  $\frac{1}{\sqrt{2}}$  (or -3 db)

of the mid frequency gain of the amplifier, i.e.,

$$|A_{VH}| = \frac{|A_{Vm}|}{\sqrt{2}}$$

This frequency is known as the higher cutoff frequency,

$$\begin{aligned} \omega_H &= \frac{R_L + h_{ie}}{R_L h_{ie} \cdot C_o} \\ f_H &= \frac{R_L + h_{ie}}{2\pi R_L h_{ie} \cdot C_o} \end{aligned}$$

And the gain at high frequencies is reduced to

$$|A_{VL1}| = \frac{|A_{Vm}|}{\sqrt{1 + \left[\frac{f}{f_H}\right]^2}}$$

**Example 10.1** The individual voltage gains of the three stages amplifier are 50, 60, 70. Calculate the overall gain in db of this three stage amplifier.

Solution:      Overall gain =  $50 \times 60 \times 70$   
 $= 210000$   
 Gain in db =  $20 \log (210000) = 106.4 \text{ db}$

**Example 10.2** The mid frequency gain of RC coupled amplifier is 100. If the gain falls by 3 db at the lower cut off frequency, calculate the gain at the cutoff frequency in db.

Solution:      Mid frequency gain = 100  
 Mid frequency gain in db =  $20 \log (100) = 40 \text{ db}$

$$\text{Gain at cut off frequency} = 40 - 3 = 37 \text{ db}$$

**Example 10.3** The mid frequency gain of a RC coupled amplifier is 100. The values of lower and higher cut off frequencies are 100 Hz and 100 KHz. Find the frequency at which the gain reduces to 90.

Solition: The gain at lower frequency region is given by:

$$|A_{VL}| = \frac{|A_{Vm}|}{\sqrt{1 + \left[ \frac{f_L}{f} \right]^2}}$$

$$\text{According to the problem } A_{Vm} = 100 \quad A_{VL} = 90 \quad f_L = 100 \text{ Hz}$$

So the frequency  $f$  at which the gain reduces to 90 is given by:

$$\sqrt{1 + \left[ \frac{100}{f} \right]^2} = \frac{100}{90}$$

$$\text{or} \quad f = \frac{100}{\sqrt{\left[ \frac{100}{81} - 1 \right]}} = 206 \text{ Hz}$$

The gain at higher frequency region is given by:

$$|A_{VH}| = \frac{|A_{Vm}|}{\sqrt{1 + \left[ \frac{f'}{f_H} \right]^2}}$$

$$\text{According to the problem } A_{Vm} = 100 \quad A_{VH} = 90 \quad f_H = 100 \text{ KHz}$$

So the frequency  $f'$  at which the gain reduces to 90 is given by:

$$\sqrt{1 + \left[ \frac{f'}{100} \right]^2} = \frac{100}{90}$$

$$\text{or} \quad \frac{f'}{100} = \sqrt{\frac{100}{81} - 1} = 0.484$$

$$\text{or} \quad f' = 0.484 \times 100 = 48.4 \text{ KHz}$$

**Example 10.4** The  $h$  parameters of the transistors used in two stage RC coupled amplifier are  $h_{fe} = 600$ ,  $h_{ie} = 10 \text{ K}\Omega$ . If the shunt capacitance at high frequency is 400 pF, coupling capacitance is 0.5  $\mu\text{F}$  and  $R_L = 10 \text{ K}\Omega$ , calculate the lower and higher cutoff frequencies of the amplifier. The source may assume to be negligibly small.

Solution: The lower cut off frequency is given by:

$$\begin{aligned}
 f_L &= \frac{1}{2\pi(R_L + h_{ie}).C_C} \\
 &= \frac{1}{2 \times 3.14 \times (10 + 10) \times 10^3 \times 0.5 \times 10^{-6}} \\
 &= \frac{1000}{62.8} = 15.9 \text{ Hz}
 \end{aligned}$$

The higher cut off frequency is given by:

$$\begin{aligned}
 f_H &= \frac{R_L + h_{ie}}{2\pi R_L h_{ie} C_o} \\
 &= \frac{(10 + 10) \times 10^3}{2 \times 3.14 \times 10^4 \times 10^4 \times 400 \times 10^{-12}} \\
 &= \frac{10^6}{12.56} = 79.6 \text{ KHz}
 \end{aligned}$$

**10.3 Hybrid  $\pi$  - model For the CE Transistor Amplifier:** Hybrid  $\pi$  model of the transistor will be considered to discuss the performance of a transistor amplifier at high frequencies. The capacitive effect of the PN junctions of the transistor is taken into account. This model helps in determining the common emitter short circuit current gain and its dependence on frequency. The hybrid  $\pi$  model also known as the Giacoletto model of the transistor is shown in figure 10.8.

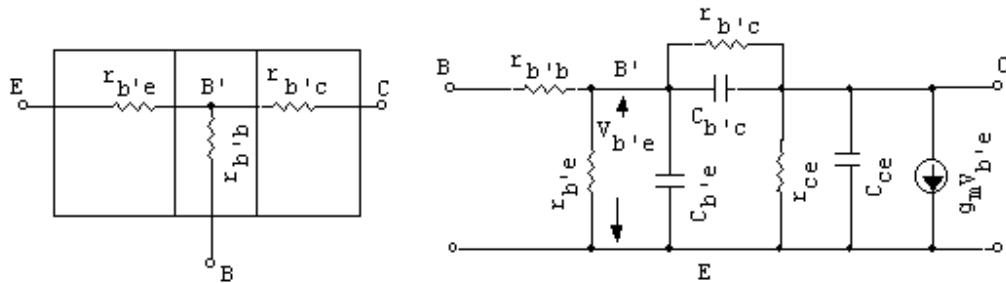


Fig. 10.8

In a transistor forward bias, emitter base junction has a capacitance associated with it. This arises from the diffusion across the base emitter junction. This is represented by  $C_{b'e}$ . The node  $B'$  is an imaginary node within the base of the transistor. The resistance  $r_{b'b}$  is the bulk resistance of the base region through which current has to flow from base lead  $B$ . The resistance  $r_{b'c}$  is the incremental resistance;  $C_{b'c}$  is the transition capacitance of the reverse biased collector base junction. The resistance and capacitance between the output terminals (collector and emitter) are  $r_{ce}$  and  $C_{ce}$ .

$V_{b'e}$  is the voltage across the emitter base junction. For small changes in  $V_{b'e}$  across the emitter junction, the extra minority carrier concentration injected into the base

region is proportional to  $V_{b'e}$ . Now the small signal collector current with collector shorted to emitter will be proportional to the voltage  $V_{b'e}$ . It will act as the constant current source across the collector and emitter having the magnitude equal to  $g_m V_{b'e}$ .

The common emitter short circuit current gain may be calculated using this hybrid  $\pi$  model. The following assumptions are made while calculating the short circuit current gain of the common emitter amplifier.

- (i) In the equivalent circuit,  $r_{b'c}$  is neglected as  $r_{b'c} \gg r_{b'e}$ .
- (ii) The resistance  $r_{ce}$  disappears as output is short circuited.
- (iii) The load resistance  $R_L = R_C = 0$ .

The equivalent circuit of the common emitter amplifier will be as shown in figure 10.9.

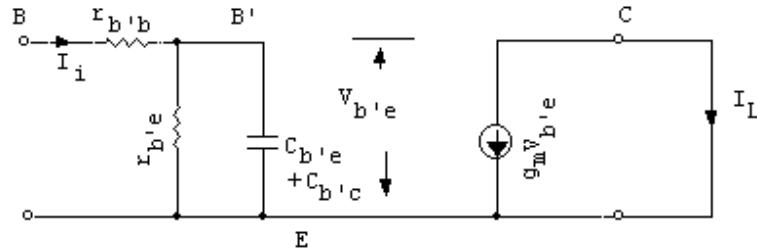


Fig. 10.9

From this equivalent circuit the short circuit current  $I_L$  is given by:

$$I_L = -g_m V_{b'e} \quad \text{----- (10.26)}$$

The voltage  $V_{b'e}$  is given by:

$$V_{b'e} = I_i Z_{eq} \quad \text{----- (10.27)}$$

where  $Z_{eq}$  is the parallel combination of the resistance  $r_{b'e}$  and the capacitive reactance  $j\omega(C_{b'e} + C_{b'c})$  given by:

$$\begin{aligned} Z_{eq} &= \frac{1}{\frac{r_{b'e}}{r_{b'e} + j\omega(C_{b'e} + C_{b'c})}} \\ &= \frac{1}{\frac{1}{r_{b'e}} + j\omega(C_{b'e} + C_{b'c})} \quad \text{----- (10.28)} \end{aligned}$$

Using the equations (10.26) to (10.28), the short circuit current gain is given as:

$$I_L = \frac{-g_m I_i}{\frac{1}{r_{b'e}} + j\omega(C_{b'e} + C_{b'c})}$$

The short circuit current gain  $A_I$  is obtained as:

$$A_I = \frac{I_L}{I_i} = \frac{-g_m}{\frac{1}{r_{b'e}} + j\omega(C_{b'e} + C_{b'c})} \quad \text{----- (10.29)}$$

Put  $r_{b'e} = \frac{h_{fe}}{g_m}$  in equation (10.24) we have:

$$\begin{aligned} A_I &= \frac{-g_m h_{fe}}{g_m + j\omega h_{fe} \cdot (C_{b'e} + C_{b'c})} \\ &= \frac{-h_{fe}}{1 + j\omega r_{b'e} \cdot (C_{b'e} + C_{b'c})} \\ &= \frac{-h_{fe}}{1 + j \left( \frac{f}{f_h} \right)} \quad \text{----- (10.30)} \end{aligned}$$

where  $f_h = \frac{1}{2\pi r_{b'e} (C_{b'e} + C_{b'c})}$ , is the cutoff frequency.

When  $f = 0$ ,  $A_I = -h_{fe}$  (low frequency current gain with output short circuited).

At  $f = f_H$ ,  $A_I = \frac{-h_{fe}}{\sqrt{2}}$  i.e. the current gain falls by  $\frac{1}{\sqrt{2}}$  times the low frequency gain (or -3db fall of gain). The gain variation is shown in figure (10.10).

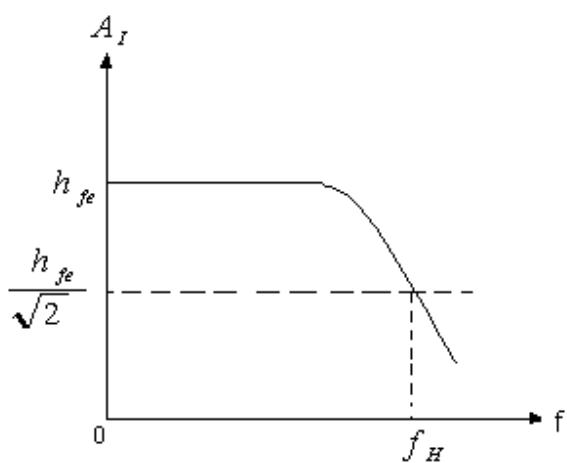


Fig. 10.10

**10.4 Class A power Amplifier:** The power amplifier also called large signal amplifier is used to obtain large power at the output of the amplifier. To have the signal up to the desired level, before the signal is applied to the power amplifier the signal is to be amplified by the multistage amplifiers. In many electronic systems, such as public address system, audio amplifier of the television receiver or transistor receiver, power amplifiers are used. The power amplifier provides a large voltage swing and also large current swing, so as to deliver the maximum power to the load with minimum distortion. Figure 10.11 shows the class A power amplifier in the common emitter configuration. Here the load resistance  $R_L$  is directly coupled to the amplifier.

The theoretical efficiency of such an amplifier will be calculated which is defined as the ratio of the output power delivered to the load to the d.c. input power from the power supply.

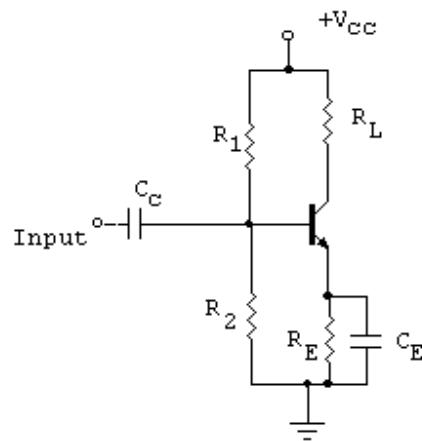


Fig. 10.11

To calculate the efficiency of this transistor amplifier circuit, it is assumed that the emitter is at the signal ground and the  $V_{CE,sat}$  is equal to zero, so that the signal swing from 0 to  $V_{CC}$ . The quiescent voltage  $V_{CQ}$  will be equal to peak swing  $V_m = \frac{V_{CC}}{2}$ . The maximum collector current is  $I_m = \frac{V_{CC}}{2 R_L}$ .

$$\begin{aligned}
 \text{The output power } P_o &= V_{rms} \cdot I_{rms} \\
 &= \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}} = \frac{V_m \cdot I_m}{2} \\
 &= \frac{1}{2} \cdot \frac{V_{CC}}{2} \cdot \frac{V_{CC}}{2 R_L} \\
 &= \frac{V_{CC}^2}{8 R_L}
 \end{aligned}$$

The input power from the supply is given by:

$$P_{d.c.} = V_{CC} \cdot I_{CQ}$$

where  $I_{CQ}$  is the average current from the supply which is equal to the maximum collector current  $I_m$ . So the input power from the supply is given by:

$$P_{d.c.} = \frac{(V_{CC})^2}{2R_L}$$

The maximum efficiency is given by:

$$\begin{aligned}\eta &= \frac{P_o}{P_{d.c.}} = \frac{\{V_{CC}^2 / 8R_L\}}{\{V_{CC}^2 / 2R_L\}} \\ &= \frac{1}{4} = 25 \%\end{aligned}$$

This is the maximum theoretical efficiency; however, the efficiency of the practical amplifier will always be less than this efficiency, because the bias resistances also consume some power which has not been considered in the above calculations.

**10.5 Transformer Coupled Amplifier:** The load for the power amplifier is generally in the form of the voice coil of the loudspeaker having low output impedance. However, the ordinary class A amplifier has the high impedance in the collector circuit. So the maximum power will not be transferred from the output of the power amplifier to the voice coil of the loudspeaker. In order to transfer the maximum power to the load impedance, the transistor collector circuit should be coupled by means of a transformer. The circuit of a transformer coupled amplifier is shown in figure (10.12).

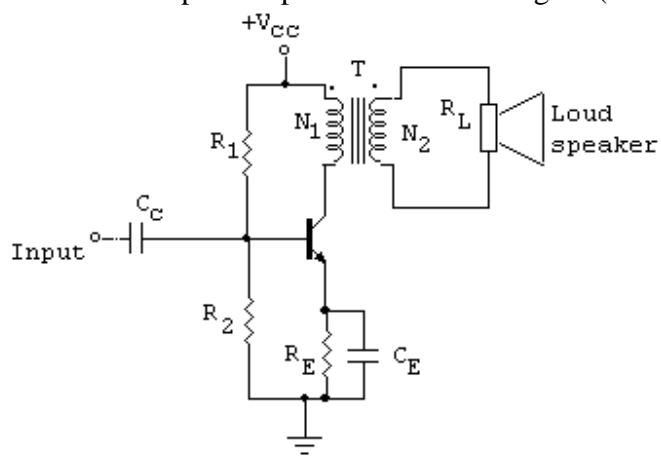


Fig. 10.12

In this circuit there is no coupling capacitor, the d.c. isolation is provided by the transformer itself. There exist no d.c. path between the primary and the secondary windings of a transformer. The a.c. signal across the primary winding is transformed to

the secondary windings. The function of the resistance  $R_1$  and  $R_2$  are used to bias the transistor in class A mode. The emitter resistance  $R_E$  provides the bias stabilization and the bye pass capacitor  $C_E$  is used to prevent the amplified signal to appear at the input.

From the figure 10.12, it is clear that the effective resistance in the collector circuit is approximately equal to d.c. resistance of the primary of the transformer which is negligibly small. The d.c. load line will, therefore, be vertical straight line passing through the operating point as shown in figure 10.13.

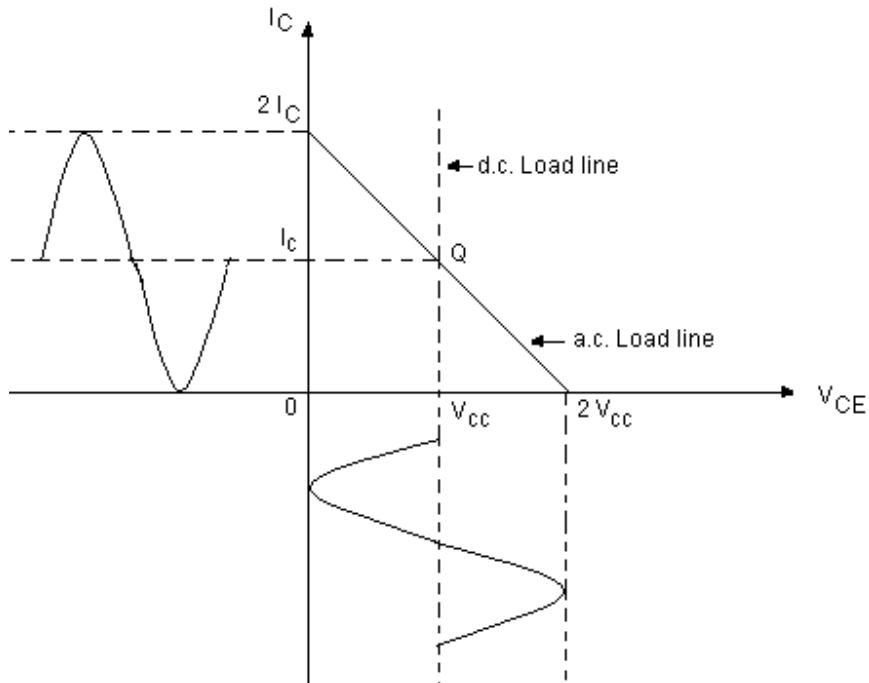


Fig. 10.13

When a.c. signal is applied to the input of the amplifier, the resistance in the collector circuit is formed by the reflected resistance of the load. Thus the effective load  $R'_L$  as seen by the collector of the amplifier is given by:

$$\begin{aligned} \frac{R'_L}{R_L} &= \frac{V_1/I_1}{V_2/I_2} = \frac{V_1}{V_2} \frac{I_2}{I_1} \\ &= \frac{N_1}{N_2} \frac{N_1}{N_2} = \left( \frac{N_1}{N_2} \right)^2 \end{aligned}$$

Where  $V_1$  and  $V_2$  are the voltages across the primary and the secondary windings of a transformer respectively and  $I_1$  and  $I_2$  are the corresponding current in the primary and the secondary windings of the transformer.

or 
$$R'_L = n^2 \cdot R_L$$
  
where  $n = \left( \frac{N_1}{N_2} \right)$  is the turn ratio.

The operating point moves along the a.c. load line whose slope is  $\left(-\frac{1}{R_L}\right)$ , after the application of the large signal to the input of the amplifier. During the peak of the positive half cycle of the signal, the collector current is  $2I_C$  and  $V_{CE} = 0$ . However during the negative half cycle, the collector current is zero and  $V_{CE} = 2V_{CC}$ .

Thus peak to peak collector emitter voltage is given by:

$$v_c = 2V_{CC}$$

The r.m.s. value of the collector voltage is  $V_{rms} = \frac{1}{2} \frac{v_c}{\sqrt{2}} = \frac{V_{CC}}{\sqrt{2}}$

The peak to peak collector current is given by:

$$i_c = \frac{v_c}{R_L} = \frac{2V_{CC}}{R_L}$$

The r.m.s. value of the collector current is :

$$I_{rms} = \frac{1}{2} \frac{i_c}{\sqrt{2}} = \frac{V_{CC}}{\sqrt{2} R_L}$$

$$\begin{aligned} \text{The output power } P_o &= V_{rms} \cdot I_{rms} \\ &= \frac{V_{CC}}{\sqrt{2}} \cdot \frac{V_{CC}}{\sqrt{2} R_L} \\ &= \frac{V_{CC}^2}{2 R_L} \end{aligned}$$

The d.c. input power from the supply is

$$P_{d.c.} = V_{CC} \cdot I_C = \frac{V_{CC}^2}{R_L}$$

The maximum efficiency is given by:

$$\begin{aligned} \eta &= \frac{P_o}{P_{d.c.}} = \frac{\{V_{CC}^2/2R_L\}}{\{V_{CC}^2/R_L\}} \\ &= \frac{1}{2} = 50\% \end{aligned}$$

The transformer coupled transistor amplifier has the advantage that its theoretical efficiency is 50% which is twice the power available in the RC coupled amplifier. Secondly the transformer provides the proper impedance matching to the output impedance of the collector circuit with the load resistance of the few ohms (resistance of the voice coil of the loud speaker). However, this amplifier has the disadvantage that the output transformer saturates (because of the core saturation), when the large d.c. current flows through the primary of the transformer. This leads the distortion at the extreme points of the output signal.

**Example 10.5:** A 12 volt battery is connected to a power transistor used in class A mode. If the maximum change in collector current is 120 mA, find the power transferred to the load, when a loudspeaker of  $8\ \Omega$  is:

- (i) connected directly in the collector circuit.
- (ii) transformer coupled.

Solution: (i) Voltage across the loudspeaker when directly connected to the collector circuit  $V_C$  is given by:

$$V_C = \Delta I_C x R_L \\ = 120 \times 8 = 960 \text{ mV} = 0.96 \text{ Volt}$$

Required power transferred to the loudspeaker is given by:

$$P_L = V_C x I_C \\ = 0.96 \text{ V} \times 120 \text{ mA} = 115.2 \text{ mW}$$

(ii) The output impedance looking at the primary of the transformer is equal to the output impedance at the collector is given by:

$$R_L' = \frac{V_{CC}}{\Delta I_C} = \frac{12V}{120 \text{ mA}} = 100 \Omega$$

$$\begin{aligned} \text{Now } R_L' &= n^2 \cdot R_L \\ 100 &= n^2 \times 8 \\ \text{or } n &= \sqrt{12.5} = 3.54 \end{aligned}$$

This is the turn ratio of the transformer.

$$\text{Voltage at the secondary of the transformer} = \frac{12V}{3.54} = 3.39V$$

$$\text{Now the load current } I_L = \frac{3.39V}{8\Omega} = 0.424 \text{ A}$$

The power delivered to the loudspeaker

$$\begin{aligned} &= I_L^2 \cdot R_L = (0.424)^2 \times 8 \\ &= 1.44 \text{ Watt} \end{aligned}$$

**Example 10.6** If the load connected to the secondary of the transformer in a transformer coupled power amplifier is  $15\ \Omega$  and zero signal current is 120 mA. Find the maximum power output, if the turn ratio of the transformer is 10.

Solution: The effective load resistance at the collector of the transistor is:

$$\begin{aligned} R_L' &= n^2 R_L \\ &= (10)^2 \times 15 = 1500 \Omega \end{aligned}$$

$$\text{Power output } P_O = I_{rms}^2 \cdot R_L'$$

$$\text{And } I_{rms} = \frac{I_C}{\sqrt{2}}$$

$$\text{So } P_O = \frac{I_C^2}{2} \cdot R_L' = \frac{(120)^2 \times 1500}{2} \mu W$$

$$= 10.8W$$

**10.6 Class B Push – Pull Amplifier:** The most frequently used power amplifier in the output stage of electronic circuits is the push pull amplifier. The push pull amplifier consists of two transistors and each transistor conducts in class *B* operation i.e. transistors are biased in the cutoff region so that the current flows only for half cycle in each transistor. In push pull amplifiers the transistors can also be used in class *A* mode but in this case the amplifier efficiency is not more than 50% and distortion is high. However the class *B* push pull amplifier provides low distortion and has the efficiency about 78.5%. The class *B* push pull amplifier is, therefore, used in the practical circuits. Figure 10.14 shows the circuit diagram of this class *B* push pull amplifier.

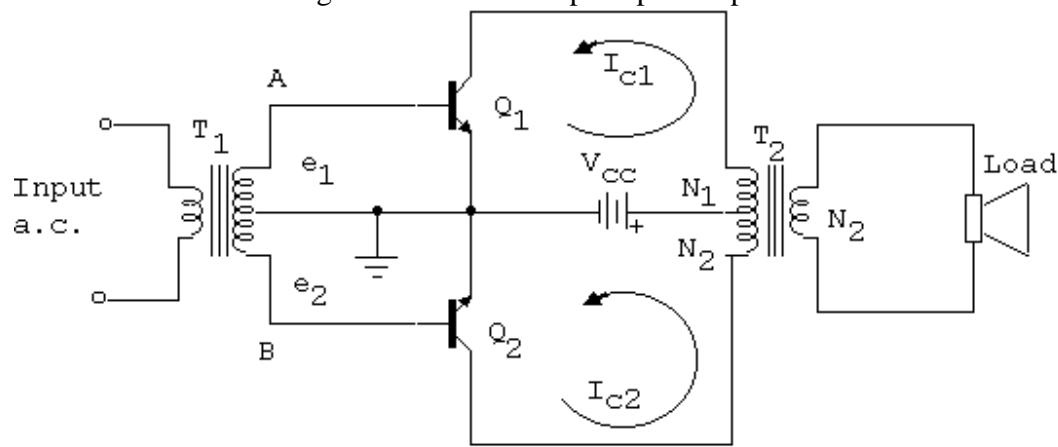


Fig. 10.14

This circuit consists of two transistors  $Q_1$  and  $Q_2$  whose emitters are coupled together and two centre tapped transformers  $T_1$  and  $T_2$ . The two transistors are biased in the cutoff region so that the collector current flows only for half of the input cycle. The input transformer  $T_1$  converts the input signal into two waves  $e_1$  and  $e_2$  which are  $180^\circ$  out of phase. When the point  $A$  is positive with respect to ground, point  $B$  will be negative with respect to ground and vice versa.

During the positive half of the input signal, the point  $A$  is positive and point  $B$  is negative with respect to the common point. The transistor  $Q_1$  will conduct and the collector current  $I_{c1}$  will flow in the collector circuit of the transistor  $Q_1$ . The transistor  $Q_2$  will, of course, be in the cutoff stage and the collector current  $I_{c2}$  in the collector circuit of transistor  $T_2$  will not flow. During the next cycle of the input signal the case is reversed that the collector current  $I_{c2}$  in transistor  $Q_2$  will be flowing and the collector current  $I_{c1}$  in the transistor  $Q_1$  will be zero. These two currents flow in opposite directions in the two halves of the primary windings of the output transformer  $T_2$ . The centre tapped primary of this transformer  $T_2$  combines two collector currents to form a sine wave output at the secondary. The effective load as seen by the amplifier is given by:

$$R'_L = n^2 \cdot R_L$$

Where  $R_L$  is load resistance at the secondary of the transformer  $T_2$  and  $n$  is the turn ratio of this transformer which is given by:

$$n = \left( \frac{2N_1}{N_2} \right).$$

It is worth to mention that in the first half cycle of the input signal the transistor  $Q_1$  is pushed up for conduction and  $Q_2$  is pulled down.; and in second cycle the case is reversed. Hence it is named as push pull amplifier.

**Analysis:** Let the base currents of the two transistors are sinusoidal in nature which are given as :

$$\begin{aligned} I_{B1} &= I_B \sin \omega.t \\ \text{and} \quad I_{B2} &= I_B \sin(\omega.t + \pi) \end{aligned}$$

Where  $\omega$  is frequency of the input signal in radians and  $\pi$  is phase difference which occurs in the two signals at the base of the two transistors due to secondary windings of the input transformer.

Due to the nonlinear characteristics of the transistors the collector currents will not be the function of frequency  $\omega$  of their signals at the base but will have the higher harmonics of this frequency  $\omega$  in addition to the d.c. currents. The collector current  $I_{c1}$  and  $I_{c2}$  are given as:

$$\begin{aligned} I_{c1} &= I_0 + I_1 \sin \omega.t + I_2 \sin 2\omega.t + I_3 \sin 3\omega.t + \dots \\ I_{c2} &= I_0 + I_1 \sin(\omega.t + \pi) + I_2 \sin 2(\omega.t + \pi) + I_3 \sin 3(\omega.t + \pi) + \dots \\ &= I_0 - I_1 \sin \omega.t + I_2 \sin 2\omega.t - I_3 \sin 3\omega.t + \dots \end{aligned}$$

The coefficients of harmonic terms in the two equations are same since the transistors are assumed to be identical. The matched pairs of transistors for push pull amplifiers are available in the market.

The voltage induces in the secondary of the output transformer  $T_2$  which is proportional to the difference of collector currents ( $I_{c1} \sim I_{c2}$ ), which is given by:

$$\begin{aligned} V_0 &= k(I_{c1} - I_{c2}) \\ &= 2k(I_1 \sin \omega.t + I_3 \sin 3\omega.t + I_5 \sin 5\omega.t + \dots) \end{aligned}$$

where  $k$  is the proportionality constant.

It is important to note from the above equation that the d.c. components (which causes the saturation in the core of the output transformer) and all even harmonic terms are eliminated leaving the third harmonic term as the only source of distortion. Fifth and other odd harmonic terms will have negligible magnitude since in the power amplifiers all harmonic terms have the magnitudes in the decreasing order not equal. So the net distortion in the output of the push pull amplifier is very less than that of the single ended amplifier.

**Theoretical Efficiency:** The current drawn in the load is the sum of currents  $I_{c1}$  and  $I_{c2}$  and will have the full wave rectified output as shown in figure 10.15.

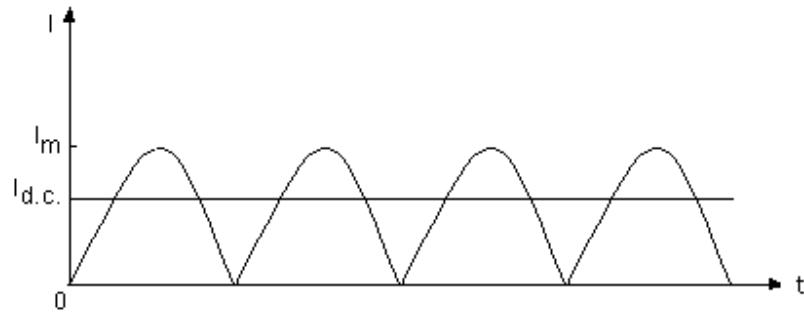


Fig. 10.15

The average value of this full wave rectified current is given by:

$$I_{dc} = \frac{2I_m}{\pi}$$

$I_m$  is the peak value of current given by:

$$I_m = \frac{V_{CC}}{R_L}$$

$$\text{so } I_{dc} = \frac{2.V_{CC}}{\pi.R_L}$$

$$P_{dc} = V_{CC} \cdot I_{dc} = \frac{2.V_{CC}^2}{\pi.R_L}$$

The maximum a.c. power in the load is given by:

$$\begin{aligned} P_o &= V_{rms} \cdot I_{rms} \\ &= \frac{V_{CC}}{\sqrt{2}} \cdot \frac{V_{CC}}{\sqrt{2} R_L} \\ &= \frac{V_{CC}^2}{2 R_L} \end{aligned}$$

Thus the maximum efficiency is

$$\begin{aligned} \eta &= \frac{P_o}{P_{d.c.}} = \frac{\{V_{CC}^2 / 2R_L\}}{\{2V_{CC}^2 / \pi.R_L\}} \\ &= \frac{\pi}{4} = 78.5\% \end{aligned}$$

### **Advantages of Push Pull Amplifier:**

1. The magnetic saturation of the core of the output transformer by the d.c. current does not occur, as it opposes each other in the transformer. Small size transformers can, therefore, be used in the push pull amplifier which will reduce its cost.
2. The harmonic distortion in the output is very less due to the cancellation of all the even harmonic components.
3. The maximum theoretical efficiency of this amplifier is 78.5% which is much larger than that of the single ended amplifier.
4. The ripple content in the d.c. power supply does not affect the output because these components get cancelled, as the ripple currents flow in the opposite direction in the two halves of the primary windings of the output transformer.

### **Disadvantages of Push Pull Amplifier:**

1. Two identical transistors must be used in this circuit otherwise harmonic terms or harmonic distortion will not be reduced.
2. The push pull amplifier becomes very bulky because of the use of two centre tapped transformers.
3. The frequency response of this amplifier becomes poor because of the stray inter-winding capacitances.

**10.7 More About Properties of Amplifiers:** One must study the following properties about the amplifiers.

**10.7.1 Distortion:** When a sinusoidal signal is applied to the input of an amplifier, the output should be the exact replica of the input wave shape with, of course, having power gain. But due to some reasons, output wave form differs from the input signal wave shape, this change in output wave form is known as distortion. There are generally of the following three types of distortions present individually or simultaneously in the amplifiers.

1. Non – linear distortion
2. Frequency distortion
3. Phase – shift distortion

**1. Non – linear distortion:** Due to the non – linearity of the dynamic transfer characteristics of the active device in the operating range, the wave form of the output voltage differs from that of the input signal. Such a distortion is called non – linear or amplitude distortion. Further it is observed that the output signal does not only contain the input signal frequency but also the new frequencies which are higher harmonics of the frequency of the input signal. This type of distortion is called as harmonic distortion. Quantitatively harmonic distortion is defined as the ratio of the total power in all the harmonics to the power contained in the fundamental frequency at the output.

Consider a sinusoidal signal  $v_i = v_o \sin \omega t$  is applied to the input of the power amplifier, and then the output current wave form may be expressed as:

$$i_0 = I_0 + I_1 \sin \omega.t + I_2 \sin 2\omega.t + I_3 \sin 3\omega.t + \dots$$

where  $I_0$  is the d.c. component,  $I_1$  the peak value of fundamental frequency (original frequency or first harmonic),  $I_2$  the peak value of the second harmonic and so on.

The harmonic distortion for the second harmonic known as second harmonic distortion is given by:

$$D_2 = \frac{I_2}{I_1}$$

$$\text{Similarly, third harmonic distortion } D_3 = \frac{I_3}{I_1}$$

and so on.

When distortion is present that power delivered to the fundamental frequency is :

$$P_1 = \frac{I_1^2 R_L}{2}$$

The total power delivered to all the harmonic components is given by:

$$\begin{aligned} P_T &= [I_1^2 + I_2^2 + I_3^2 + \dots] \frac{R_L}{2} \\ &= \frac{I_1^2 R_L}{2} \left[ 1 + \left( \frac{I_2}{I_1} \right)^2 + \left( \frac{I_3}{I_1} \right)^2 + \dots \right] \\ &= P_1 [1 + D_2^2 + D_3^2 + \dots] \\ &= P_1 [1 + D^2] \end{aligned}$$

where  $D$  is called as the total distortion or distortion factor given by:

$$D = \sqrt{D_2^2 + D_3^2 + \dots}$$

**Example 10.7** When a sinusoidal signal of fundamental frequency of 500 radians/sec. is fed to a transistor amplifier, the resulting output collector current is of the form:

$$I_C = 12. \sin 500t + 1.1. \sin 1000t + \sin 1500t + 0.6. \sin 2000t + \dots$$

Calculate (i) Second, third and fourth harmonic distortions.

(ii) Percentage increase in power due to harmonic distortion.

Solution: (i) Second harmonic distortion:

$$D_2 = \frac{I_2}{I_1} = \frac{1.1}{12} = 0.0917 = 9.17\%$$

Third Second harmonic distortion:

$$D_3 = \frac{I_3}{I_1} = \frac{1.0}{12} = 0.083 = 8.33\%$$

Fourth harmonic distortion:

$$D_4 = \frac{I_4}{I_1} = \frac{.6}{12} = 0.05 = 5\%$$

(ii) Distortion Factor

$$\begin{aligned} D &= \sqrt{D_2^2 + D_3^2 + D_4^2} \\ &= \sqrt{(0.0917)^2 + (0.083)^2 + (0.05)^2} = 0.133 = 13.3\% \end{aligned}$$

Power delivered to all the harmonic components:

$$\begin{aligned} &= P_1(1 + D^2) = P_1(1 + (.133)^2) \\ &= 1.0177 P_1 \end{aligned}$$

Percentage increase in power due to distortion:

$$\frac{(1.0177 - 1)P_1}{P_1} \times 100 = 1.77\%$$

**2. Frequency Distortion:** When the signals of different frequencies are amplified by an amplifier than the amplification will be different at different frequencies. The frequency distortion is, therefore, said to exist. At different frequencies the different behavior of the amplifier is due to coupling network or due to the device inter-capacitances. The graph plotted between the gains of the amplifier versus the frequency of the input signal is called as amplitude frequency response characteristic. When the frequency response characteristic is not horizontal over the range of frequencies under consideration, the frequency distortion is said to exist.

**3. Phase – Shift Distortion:** It has been observed that all amplifiers behave as low pass filter at high frequencies. In the region of frequency response curve where the gain falls, the signals of different frequencies suffer unequal phase shift. The phase shift distortion is, therefore, said to exist. The plot of the phase shift as a function of frequency is called phase response. There will be no phase shift distortion if there is linear increase in phase shift with frequency. The phase shift distortion has no consequence in audio amplifiers since human ear is not sensitive to the phase relationship between the Fourier signal components. Video amplifiers used in television system suffer problem due to phase shift distortion, and highly distorted pictures will be observed. Video amplifiers are thus designed to have linear phase – shift characteristics.

**10.7.2 Noise in Amplifiers:** It has been observed that even when no signal is applied to the input of an amplifier, some voltage variation of appreciable magnitude is available at its output. This voltage variation is referred to as noise. Sometimes it is impossible to distinguish between the signal and the background noise. The background hiss in a radio receiver is an example of noise. Snow like appearance on the television screen is due to the noise in the video amplifier of the television system. Noise in the amplifiers is caused by random movement of charge carriers in transistors and resistors used in amplifiers. Various sources of noise in an amplifier are being discussed.

**10.7.3 Thermal Noise or Johnson Noise:** The random movement of electrons in a conductor is due to the thermal energy possessed by the electrons. If there is a small fluctuation in the energy, it will produce small noise potential in the conductor. This type

of noise is known as thermal noise or Johnson noise. The mean square value of the thermally varying voltage in a resistor  $R$  at  $T^0 K$  is given by:

$$E_n^2 = 4RKT(BW)$$

where  $k$  is the Boltzmann's constant (Joules/ $^0 K$ ),

$T$  is the absolute temperature of the resistor, and

$BW$  is the bandwidth (Hz).

This thermal voltage available across the resistance will be amplified and appear as the noise at the output terminals, when the resistance is connected across the input terminals of the amplifier. This noise is also called the white noise since it gives almost the same noise per unit band width over a wide frequency spectrum.

**10.7.4 Shot Noise:** The current in a transistor or field effect transistor is normally assumed to be constant under d.c. conditions. But in practice there are fluctuations in these currents due to the random movements of charge carriers in the semiconductor. In other words the d.c. current is the average value of this current. Microscopically one can say that the random component of the current known as shot noise is superimposed on the average value.

The mean square value of the shot noise current is proportional to the d.c. current  $I_{dc}$  given by:

$$I_N^2 = 2qI_{dc}(BW)$$

where  $q$  is the magnitude of the electronic charge.

If  $R_L$  is the value of load resistance than the noise voltage  $I_N R_L$  will appear across the load resistance.

**10.7.5 Noise Figure:** To know quantitatively how noisy a device is, a term known as noise figure has been introduced. Before discussing the noise figure one more quantity known as signal to noise power ratio, which is defined as the ratio of the input signal power to the noise power at the input signal. The signal noise power ratio may be defined for both the input as well as for the output. Thus the input signal to noise power ratio ( $SNPI$ ) and output signal to noise power ratio ( $SNPO$ ) are given by:

$$SNPI = \frac{S_{Pi}}{N_{Pi}}$$

$$SNPO = \frac{S_{Po}}{N_{Po}}$$

where  $S_{Pi}$  = signal power input

$N_{Pi}$  = Noise power input due to source resistance

$S_{Po}$  = signal power output

$N_{Po}$  = noise power output

The ratio of the input signal to noise power ratio (SNPI) and output signal to noise power ratio (SNPO) is called as the noise figure given as:

$$NF = \frac{S_{Pi}/N_{Pi}}{S_{Po}/N_{Po}} = \frac{S_{Pi} \cdot N_{Po}}{S_{Po} \cdot N_{Pi}}$$

Noise figure is often expressed in decibels as :

$$\begin{aligned} NF(db) &= 10 \log \left( \frac{S_{Pi} \cdot N_{Po}}{S_{Po} \cdot N_{Pi}} \right) \\ &= 10 \log \left( \frac{S_{Pi}}{N_{Pi}} \right) - 10 \log \left( \frac{S_{Po}}{N_{Po}} \right) \end{aligned}$$

Noise figure in decibels is given by the input signal to noise power ratio in decibels minus output signal to noise power ratio in decibels.

The noise figure in decibels can also be given in form of signal to noise voltage ratio as:

$$\begin{aligned} NF(db) &= 20 \log \left( \frac{S_{Vi} \cdot N_{Vo}}{S_{Vo} \cdot N_{Vi}} \right) \\ &= 20 \log \left( \frac{S_{Vi}}{N_{Vi}} \right) - 20 \log \left( \frac{S_{Vo}}{N_{Vo}} \right) \end{aligned}$$

where  $(S_{Vi}/N_{Vi})$  is called input signal to noise voltage ratio, and

$(S_{Vo}/N_{Vo})$  is called output signal to noise voltage ratio.

**Example 10. 8** The signal input to a small signal amplifier consists of  $60 \mu W$  of signal power and  $0.8 \mu W$  of noise power. The amplifier generates an internal noise of power of  $50 \mu W$  and has power of  $20 db$ . Compute for this amplifier:

- (i) Signal to Noise power input (SNPI)
- (ii) Signal to Noise power output (SNPO)
- (iii) Noise Figure and its value in  $db$  also.

Solution: (i) Signal to Noise power input

$$SNPI = \frac{S_{Pi}}{N_{Pi}} = \frac{60 \mu W}{0.8 \mu W} = 75$$

- (ii) Power gain is given as  $20 db$
- i.e.  $20 = 10 \log_{10}(power.gain)$
- So power gain = 100
- Input signal power =  $60 \mu W$

$$\begin{aligned}\text{Output signal power } (S_{Po}) &= (\text{input signal power}) \times (\text{power gain}) \\ &= 60 \times 100 = 6000 \mu W\end{aligned}$$

Noise power output ( $N_{Po}$ ) =

$$\begin{aligned}&\text{(power gain). (noise power input) + internal noise of the amplifier} \\ &= 100 \times 0.8 \mu W + 50 \mu W = 130 \mu W\end{aligned}$$

$$\text{Signal to noise power output } SNPO = \frac{S_{Po}}{N_{Po}} = \frac{6000}{130} = 46.2$$

$$\text{Noise Figure } NF = \frac{SNPI}{SPNO} = \frac{75}{46.2} = 1.63$$

$$\text{Noise figure (db)} = 10 \log_{10}(1.63) = 2.12 \text{ db}$$

**Example 10. 9** A  $1 \text{ M}\Omega$  resistance is connected between the base and the ground in CE transistor amplifier whose input impedance is infinitely large. The amplifier has a voltage gain of 100 and band width 100 KHz. Find the amount of noise voltage at the output of amplifier at room temperature ( $300 \text{ }^{\circ}\text{K}$ ) when no source is connected to the amplifier. The amplifier itself does not provide any noise.

Solution: (i) The noise voltage will be developed across  $1 \text{ M}\Omega$  input resistance whose root mean square value is given by:

$$\begin{aligned}E_n &= \sqrt{4RKT(BW)} \\ &= \sqrt{4(10^6)(1.38 \times 10^{-23})(300)(100 \times 10^3)} \\ &= 40.7 \mu V\end{aligned}$$

The noise voltage at the output is given by:

$$\begin{aligned}E_{no} &= E_n \times (\text{gain of the amplifier}) \\ &= 100 \times 40.7 = 4.7 mV\end{aligned}$$

## Problems:

1. Discuss the classifications of amplifiers.
2. Draw the circuit diagram of R – C coupled transistor amplifier. Discuss the working of this circuit explaining the function of each component used in the circuit.
3. Explain the frequency response curve of R – C coupled amplifier for the low and mid frequency region.
4. Drive the expression for the lower cutoff frequency of the R – C coupled transistor amplifier due to emitter bypass capacitance alone and assume other capacitances to have zero impedance.

5. Discuss hybrid  $\pi$ -model of transistor. Find the expression for higher cut off frequency and show that the current gain falls by  $\frac{1}{\sqrt{2}}$  times the low frequency gain (or -3db fall of gain).
6. What is power amplifier? Draw the circuit diagram of a Class A power Amplifier and show that its maximum theoretical efficiency is only 25%.
7. Draw the circuit diagram of a single ended transformer coupled class A power amplifier. Explain the working of this amplifier. What are its advantages and disadvantages?
8. Draw the circuit diagram of a single ended transformer coupled class A power amplifier and show that its maximum theoretical efficiency is about 50%.
9. Draw the circuit diagram of class B push - pull amplifier and explain its working. Give the advantages and disadvantages of this amplifier.
10. Explain the circuit diagram of class B push – pull amplifier. Show that its maximum theoretical efficiency is about 78.5%.
11. Draw the circuit diagram of class B push - pull amplifier and explain the harmonic distortion in class B push – pull amplifier.
12. Discuss various types of distortions in transistor amplifiers.
13. Discuss various types of noise in transistor amplifiers.
14. Define following modes of operation of an amplifier (i) Class A, (ii) Class B, (iii) Class AB and (iv) Class C.
15. Draw the circuit diagram of two stage R – C coupled CE transistor amplifier. By drawing the low frequency model of the first stage of the amplifier, find the expression of lower cutoff frequency of the amplifier assuming only the emitter bypass capacitance.
16. What is meant by amplifier noise? Define Johnson noise and shot noise.
17. Define noise figure and signal to noise ratio. Drive the expression for the noise figure in terms of the input and output signal to noise ratio.
18. Discuss the following types of distortion (i) non-linear distortion (ii) frequency distortion and (iii) phase-shift distortion.
19. Show that the maximum theoretical efficiency of a single ended class A power amplifier is 25%. Also show that if the output is transformer coupled, then by proper matching, efficiency can be increased to 50%.
20. In a transformer coupled class A power amplifier, the turn ratio of the transformer is 10 and load resistance connected to the secondary is  $50\Omega$ . The zero signal collector current is  $80\text{ mA}$ .  
(Ans. 16 W)
21. The individual gains of the three stage amplifier are 30, 40, 50. Calculate the overall gain of the amplifier and express it in db also.  
(Ans. 60000, 95.6 db)

22. The voltage gain of an RC coupled amplifier in the mid frequency range is 90. If the gain falls by 3 db at the lower cut off frequency, calculate the gain at the cutoff frequency in db.  
(Ans. 36.08 db)
23. The mid frequency gain of a RC coupled amplifier is 120. The values of lower and higher cut off frequencies are 50 Hz and 75 KHz. Find the frequency at which the gain reduces to 100.  
(Ans. 75.4 Hz, 49.75 KHz)
24. The  $h$  parameters of the transistors used in two stage RC coupled amplifier are  $h_{fe} = 400$ ,  $h_{ie} = 8 K\Omega$ . If the shunt capacitance at high frequency is 500 pf, coupling capacitance is 0.5  $\mu F$  and  $R_L = 15 K\Omega$ , calculate the lower and higher cutoff frequencies of the amplifier. The source may assume to be negligibly small.  
(Ans. 13.85Hz, 61KHz)
25. A 10 volt battery is connected to a power transistor used in class A mode. If the maximum change in collector current is 100 mA, find the power transferred to the load, when a loudspeaker of  $16 \Omega$  is:  
(i) connected directly in the collector circuit.  
(ii) transformer coupled.  
(Ans. 160 mW, 1W)
26. If the load connected to the secondary of the transformer in a transformer coupled power amplifier is  $10 \Omega$  and zero signal current is 100 mA. Find the maximum power output, if the turn ratio of the transformer is 12.  
(Ans. 7.2 W)
27. When a sinusoidal signal of fundamental frequency of 300 radians/ sec. is fed to a transistor amplifier, the resulting output collector current is of the form:  
$$I_C = 10.Sin 300t + 1.1.Sin 600t + 0.9 Sin 900t + 0.6.Sin 1200t + ....$$
Calculate (i) Second, third and fourth harmonic distortions.  
(ii) Percentage increase in power due to harmonic distortion.  
(Ans. (i) 11%, 9%, 6% : (ii) 2.38%)

# 11

## Electronic Instruments

With the advent of Nanotechnology, now a days very sophisticated, modern and sensitive electronic instrument are available for the use of human beings in every walks of life. In this chapter only the very basic electronic instruments for the use in laboratories will be discussed. The purpose of this chapter is to acquaint the students with the basic principle, working and applications of these instruments. The most commonly used instruments in laboratories are Multimeters, Cathode Ray Oscilloscope, Digital Frequency Meter and Function Generators etc.

**11.1 Multimeters:** While working with the electronic circuits, it is sometimes necessary to measure the basic electronic quantities namely current, voltage (for both a.c. and d.c.), and also the resistances. With the use of an important electronic instrument known as multimeter, these quantities can easily be measured. Multimeter is a very versatile, rugged and general purpose instrument for use in laboratories. It is also known as AVO meter (Ampere Volt Ohm meter). The multimeters are basically of two types namely Analog multimeters and digital multimeters.

**11.1.1 Analog Multimeters:** In analog multimeters, the reading of the measuring quantity is given by the deflection of the needle on the indicating meter. The heart of this

meter is a pivoted type moving coil galvanometer having a coil on jeweled bearings between the poles of a permanent magnet. The indicating needle is fastened to the coil. The zero is marked on the extreme left of the galvanometer and not in the middle as is normally marked in the galvanometer. The needle is, therefore, rests on the zero of the meter. With this galvanometer, the arrangements are made so that it can measure the voltage, current and resistances.

**Measurement of Voltage:** To use the multimeter for the measurement of voltage, a high resistance  $R$  is connected in series with the galvanometer of the multimeter as shown in figure (11.1). Let  $I_g$  is the current sensitivity for the full scale deflection of the galvanometer and  $G$  is the galvanometer resistance. The maximum voltage that can be measured by this meter will be  $I_g \cdot G$ , which is known as the voltage rating of the

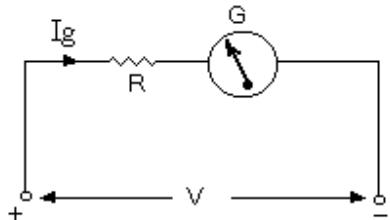


Fig. 11.1

instrument. The high resistance  $R$  connected in series with the galvanometer will increase the voltage ratings of the instrument. The value of the series resistance  $R$  for the measurement of voltage from 0 to  $V$  volt is given by:

$$V = I_g (R + G)$$

or

$$R = \frac{V}{I_g} - G \quad \text{----- (11.1)}$$

From this equation it is clear that to have the larger voltage range, larger series resistance is required.

A multi - range voltmeter can, therefore, be constructed by providing a number of high resistance in series with the galvanometer and a rotary switch for the selection of the proper voltage range as shown in figure (11.2).

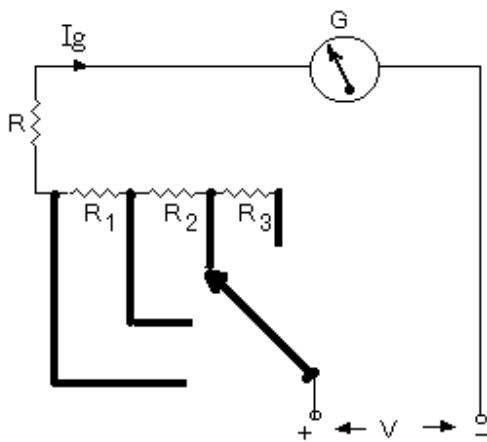


Fig. 11.2

The a.c. voltage can also be measured in the similar fashion, simply by connecting the bridge rectifier with the galvanometer as shown in figure (11.3).

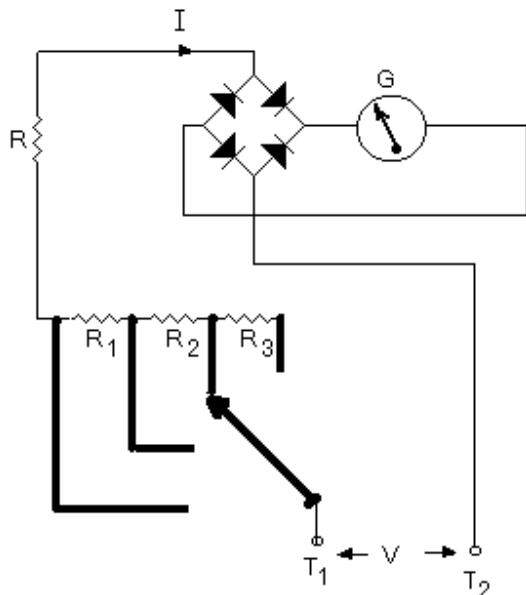


Fig. 11.3

**Measurement of Current:** For the measurement of current, using the analog multimeter, a low resistance  $R$  is connected in shunt (parallel) with the galvanometer as shown in figure (11.4). Let  $I_g$  is the sensitivity of the galvanometer and  $G$  is the resistance of the

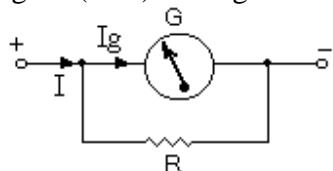


Fig. 11.4

galvanometer. The current  $I$  flowing through the terminals of the galvanometer is given by:

$$\frac{R \cdot G}{(R + G)} \cdot I = G \cdot I_g$$

or

$$\frac{R \cdot I}{(R + G)} = I_g$$

or

$$R = \frac{G \cdot I_g}{(I - I_g)} \quad \text{----- (11.2)}$$

From this equation, it is clear that for the different current ranges, the different values of shunt resistances are required. A multi-range current meter, is therefore, constructed by providing a number of shunt resistances and a rotary switch for the selection of proper current range as shown in figure (11.5).

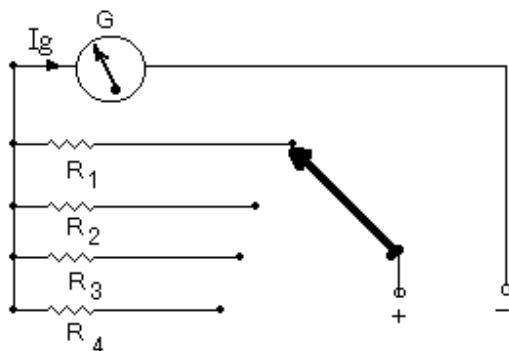


Fig.11.5

**Measurement of Resistance:** The measurement of resistance is possible with the help of multimeter if its galvanometer is connected with a battery and a current limiting resistance  $R_S$  as shown in figure (11.6).

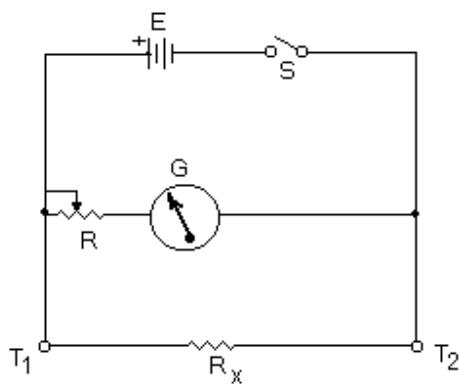


Fig. 11.6

The resistor whose resistance is to be measured is connected across the output terminal of the arrangement shown in figure (11.6). In this case the amount of current flowing through the meter will depend on the value of the measuring resistance. So the scale of the meter can be calibrated in ohms. When the leads of the multimeter are shorted together, the variable resistance  $R$  should be adjusted such that the galvanometer show the full scale deflection to the right side of the galvanometer where zero for the ohm scale is marked.

The galvanometer current is given by:

$$\frac{E}{R + G} = I_g$$

When the leads are open, the resistance between the leads is infinite and needle rests to the left side of the scale where infinite for the resistance is marked. It is worth mentioning that the scale for the ohmmeter is not linear. The value of the resistances at the left side of the meter is crowded. The different ranges of resistances may also be provided with the help of selector switch and by using the different values of resistance  $R$ . The block diagram of a basic analog multimeter is shown in figure 11.7.

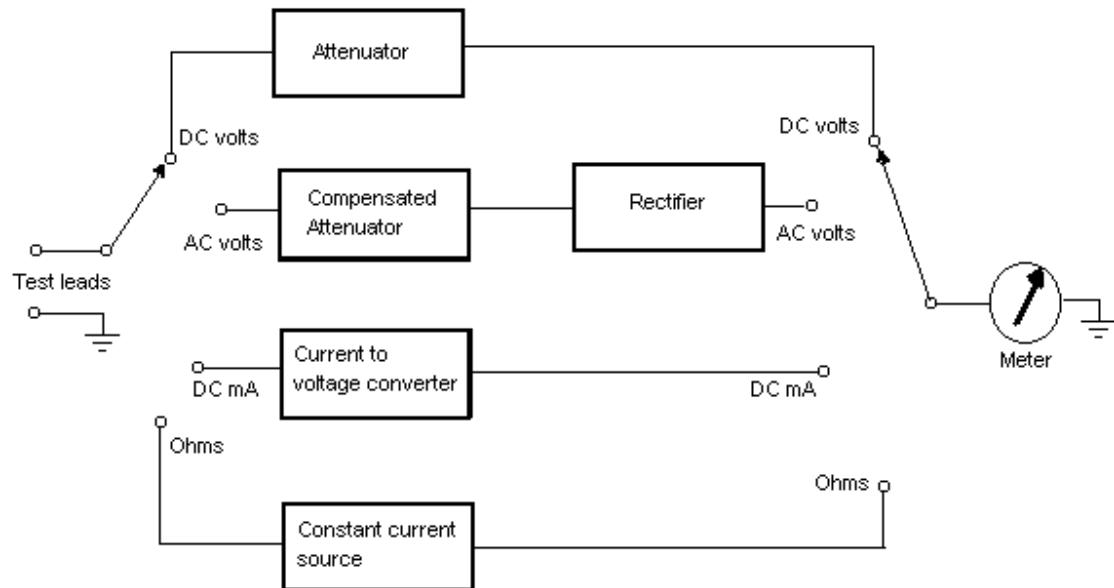


Fig. 11.7

Commercially available Analog multimeters is shown in figure 11.8.



Fig. 11.8

**11.1.2 Electronic Voltmeter:** The simple multimeter discussed above have the input impedance in the range of  $10\text{ K}\Omega$  to  $20\text{ K}\Omega/\text{volt}$ . These are, therefore, low impedance voltmeter especially when the voltage in the range of milli - volts or micro - volts is measured. Further, these multimeters have poor sensitivity and low bandwidth. Thus these multimeters are not suitable for the measurement of low voltage from high impedance source. In such cases the electronic voltmeter is used.

The electronic voltmeter has very high input impedance, good sensitivity and larger bandwidth. The electronic voltmeter consists of amplifier, rectifier and other circuit so as to give the current proportional to the voltage to be measured. This current is then passed through a conventional analog voltmeter. The block diagram of such an electronic voltmeter is shown in figure (11.9). These voltmeters have the input impedance in the range of  $1\text{ M}\Omega$  to  $10\text{ M}\Omega$  and bandwidth of several hundred megahertz and the sensitivity lies in the range of milli-volts.

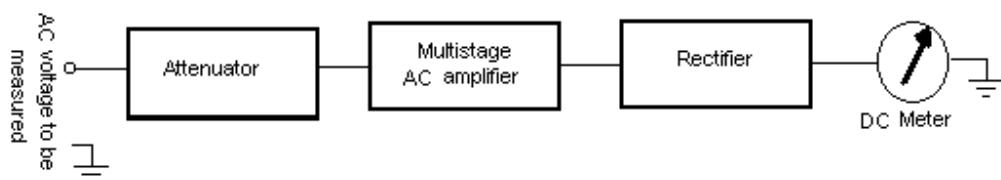


Fig. 11.9

**11.1.3 Digital Multimeters:** In digital multimeters, the reading of the measuring quantity is given in the form of digital readout on the panel of the meter; and not by the deflection of the needle on the indicating meter as is done in the analog multimeters. The digital multimeters are also used to measure voltage, current and resistance. The measuring quantities are first converted to d.c. voltage by some device, which is measured and displayed on the digital panel meter. For the measurement of a.c. voltage, the input voltage is converted to d.c. voltage by means of a rectifier. For the measurement of current, it is passed through a precision resistor in the meter and voltage across that resistor will be processed to have its digital readout on the panel meter. Similarly, for the resistance measurement a constant current supplied by a constant current source is passed through the measuring resistance and voltage drop across it is measured and displayed in ohms on the panel meter. The functional block diagram of the digital multimeter is shown in the figure (11.10).

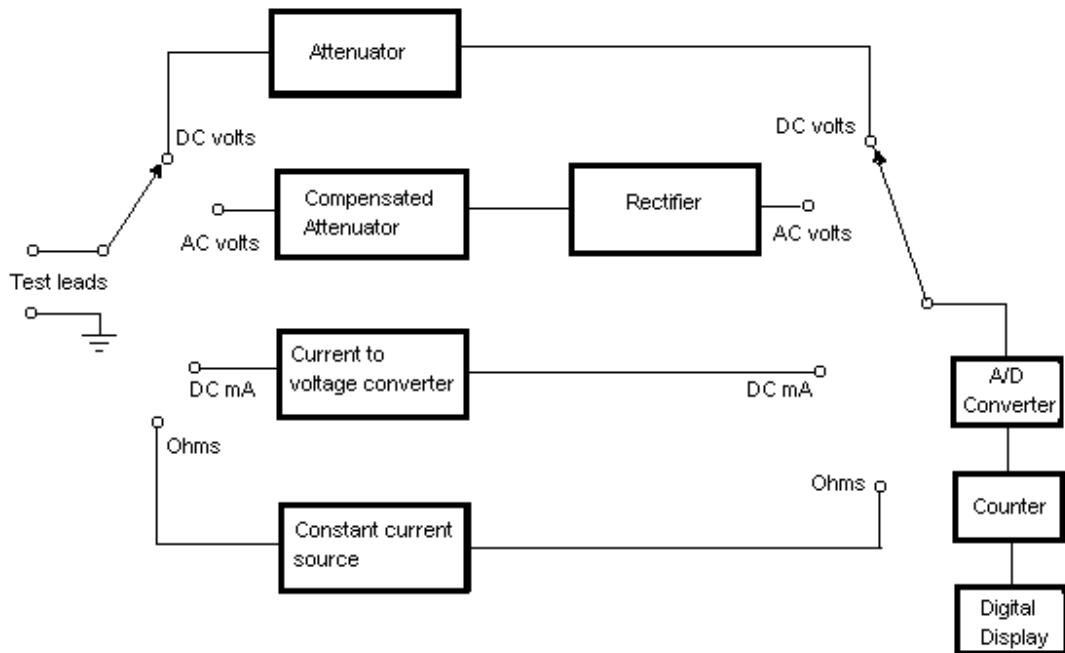


Fig. 11.10

Commercially available digital multimeter is shown in figure 11.11.



Fig. 11.11

Advantages of the Digital multimeters:

- (1) The digital multimeters provide better resolution than the conventional analog multimeters. A typical resolution of 1 part in  $10^6$  is easily observed.
- (2) The digital multimeters are more accurate than the analog multimeters.
- (3) Input impedance on both a.c. and d.c. is much larger than the analog multimeters.
- (4) These are operated on low voltage cells which are kept inside the multimeters.
- (5) Since the result of the measuring quantity is displayed on the pen meter in the form of digits so it avoids errors due to reading, interpolation and parallax.

**11.2 Cathode Ray Oscilloscope:** The cathode ray oscilloscope (CRO) is another measuring electronic instrument used in laboratories. It is capable of displaying the signal wave shapes on the screen of the CRO, so it is widely used for the trouble shooting in the electronic circuits in the laboratories. It is very versatile instrument and can also be used to measure the voltage, frequency and the phase shift. The heart of the cathode ray oscilloscope is the cathode ray tube (CRT).

**11.2.1 Cathode Ray tube:** The schematic diagram of a cathode ray tube (CRT) is shown in figure (11.12). It has the following four major parts.

1. Electron gun – an arrangement for producing and focusing the electron beam.

2. Deflecting system – a system for deflecting the electron beam librated from the electron gun.
3. Fluorescent screen – for producing bright spot.
4. Evacuated glass enclosure – all assemblies fitted in evacuated glass enclosure.

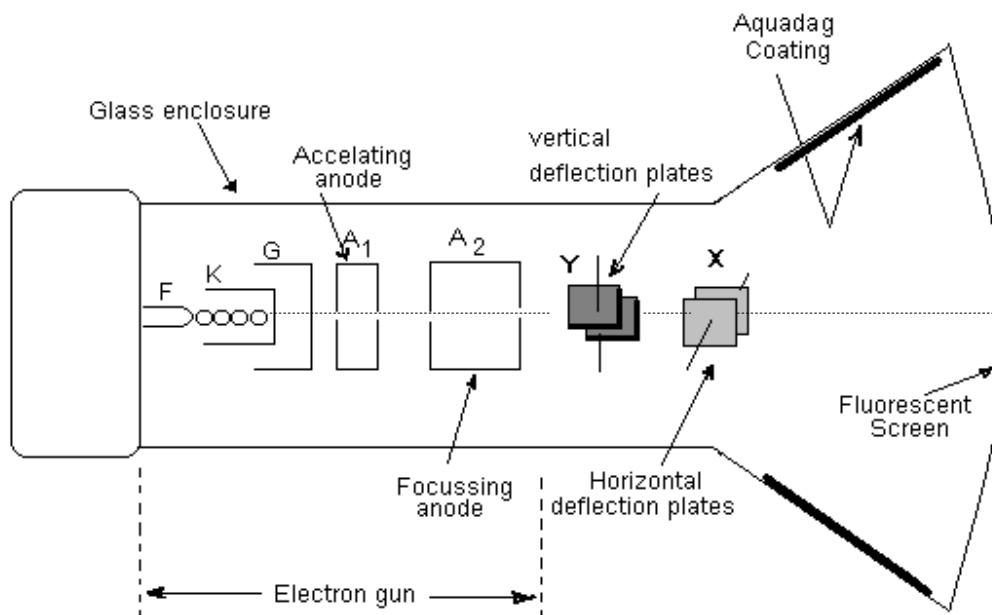


Fig. 11.12

**1. Electron gun:** The arrangement of electrodes that produces a focused beam of electrons is known as electron gun. It consists of an indirectly heated cathode K, a control grid G, a focusing anode A<sub>1</sub> and accelerating anode A<sub>2</sub>. The control grid is held at a negative potential with respect to cathode and focusing and accelerating grids are maintained at successively higher potential with respect to cathode.

The cathode consists of a nickel cylinder coated with oxides of barium and strontium for liberation plenty of electrons. The control grid enclosing the cathode consists of metallic cylinder with very small aperture. This small opening helps to keep the electron beam of very small in size. By controlling the positive potential of the focusing anode A<sub>1</sub>, the electron beam is focused in to a sharp pin – dot. The accelerating anode A<sub>2</sub> which is at higher potential than the focusing anode accelerates the electron beam to a very high velocity. The electron gun thus librates a narrow, accelerated beam of electrons which produces a sharp spot of light when strikes on the fluorescent screen.

**2. Deflecting system:** For deflecting the narrow accelerated electron beam librated from the electron gun are deflected in the vertical and horizontal directions by the two sets of deflecting plates. One set marked as Y is known vertical deflecting plates and the other set marked as X is known as horizontal deflecting plates. By the application of proper

potential to the two sets plates, the electron beam deflects in the vertical and horizontal direction. If no potential is applied to the two sets of plates, the electron beam without deflection strikes the screen at the centre producing a bright spot. If on the other hand, a positive potential is applied to the upper vertical deflecting plate with respect to the lower vertical plate, the electron beam deflect upwards. The height of the deflecting beam will be proportional to the applied potential. If an alternating voltage is applied to the set of Y plates, the spot will be moving continuously upward and downward thereby producing a luminous trace in the vertical direction on the fluorescent screen due to the persistence of vision. The beam will be deflecting in the horizontal direction if the similar potential is applied to the set of horizontal plates.

**3. Fluorescent Screen:** The inside face of the tube is coated with some fluorescent material such as Zinc orthosilicate, Zinc oxide etc which works as fluorescent screen. It makes the visible. Various kinds of phosphors or their combinations are used to obtain spots of variety of colors. The green spot is produced if Zinc orthosilicate is used as the fluorescent material.

**4. Evacuated glass enclosure:** The all parts discussed above are enclosed inside a funnel shaped evacuated glass envelope. The vacuum created inside the tube helps the electron beam to transverse the tube easily without any collision. The flared part of the tube is coated from inside with a conducting graphite layer called aquadag. This coating is kept at a positive potential with respect to the cathode and collects the primary as well as secondary electrons returned from the screen.

**11.2.2 Construction:** The simplified block diagram of a cathode ray oscilloscope is shown in figure 11.13. The filament of the electron gun is heated with help of the a.c. supply. The electrons are therefore, emitted. The intensity of the beam is controlled by the control grid supply. The electron beam after the control of the control grid is influenced by the focusing and the accelerating grid. These two electrodes are maintained at high positive potential with respect to cathode. The electrostatic field that exists between the anodes provides the necessary focusing of the electron beam and the system of electrodes is known as electron lens. The focusing of the beam that strikes on the fluorescent screen can be corrected by varying voltage on the two electrodes. The focus control is provided on the front panel of the oscilloscope.

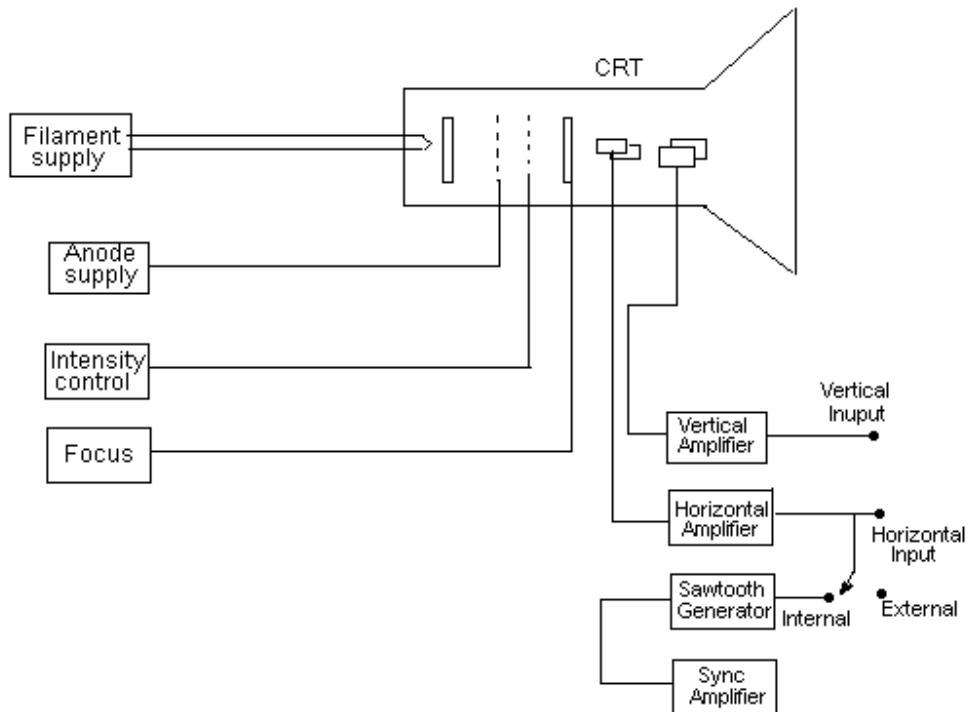


Fig. 11.13

Now after the electron beam leaves the accelerating anode, it comes under the influence of vertical and horizontal plates. If no voltage is applied to the deflection plates, the electron beam will produce spot of light at the centre of the screen (point P). The electron beam will be deflected upwards (point Q), if certain voltage is applied to the vertical plates (figure 11.14). The height of the deflection will be proportional to the applied voltage to the vertical plates. The electron beam will be deflected downwards (point R) if the polarity of the voltage on the vertical plates is reversed. Similarly, the spot can be moved in the horizontal direction if the proper voltage is applied across the horizontal plates. If the sinusoidal voltage is applied to the vertical plates, the spot will

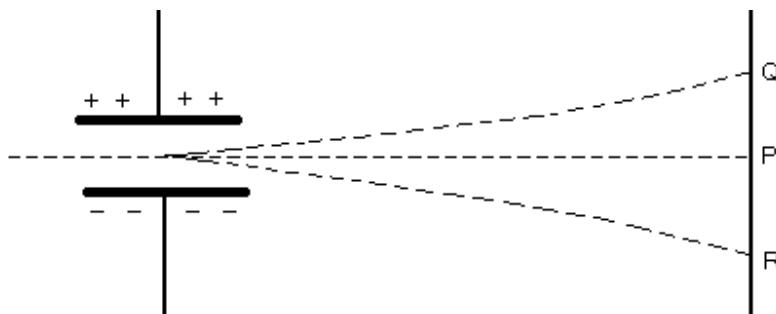


Fig. 11.14

deflect upward and downward direction continuously and due to the persistence of vision a vertical line will be observed on the fluorescent screen. However, to see the variation of the sinusoidal signal with time on the CRO screen, the spot is simultaneously to be moved in the horizontal direction uniform speed. This is possible if suitable waveform (saw tooth) is applied to the horizontal plates. So a saw tooth is generated internally in the CRO with the help of saw tooth generator or linear time base generator. During the trace path of the saw tooth wave (fig. 11.15) the complete cycle is traced on the screen, while during the fly back or retrace path of the saw tooth wave the spot is blanked out and not visible on the screen. The fly back time of the wave is kept very small.

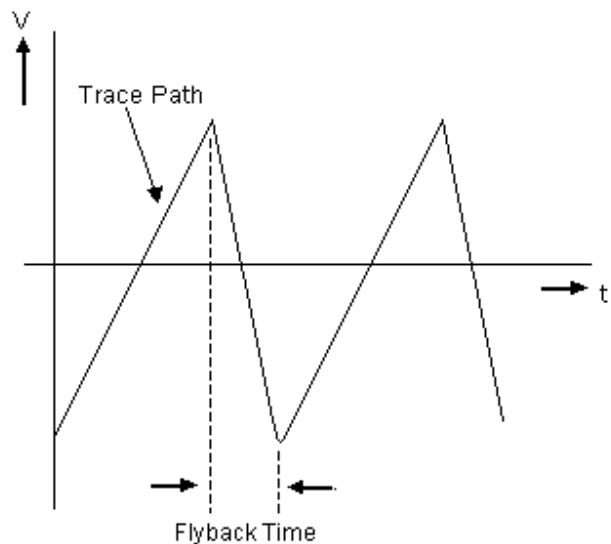


Fig. 11.15

Figure 11.16 clearly illustrates the synchronization between the input sinusoidal wave applied across the vertical plates of the CR tube and saw tooth wave applied internally across the horizontal plates of the tube.

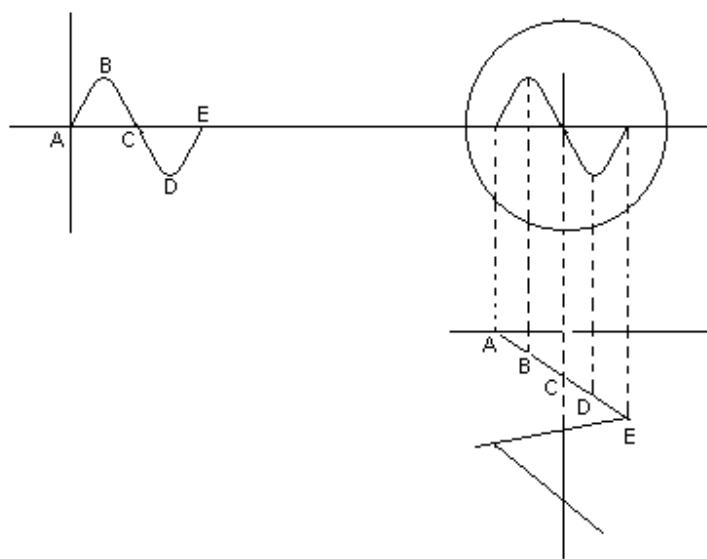


Fig. 11.16

On the screen of the CRO scale (equidistant horizontal and vertical lines as in graph sheet) is provided as shown in figure 11.17. The size of the input wave can be seen on this scale.

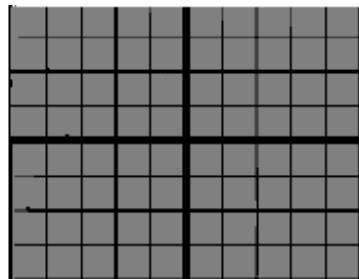


Fig. 11.17

Commercially available cathode ray oscilloscope for use in electronics laboratory is shown in figure 11.18.

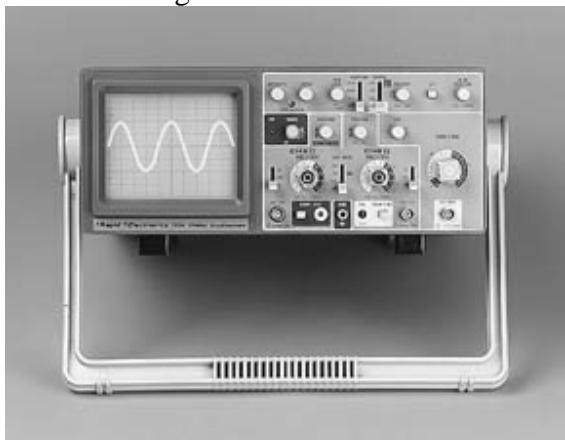


Fig. 11.18

**11.3 Application of CRO:** The CRO finds many applications in electronics laboratory. Here some very common and important applications of CRO will be discussed.

**11.3.1 Measurement of Voltage and Time Period:** For the measurement of voltage the signal whose voltage is to be measured, is applied to the Y – axis and internal time base is used. The scale is determined by the Y – amplifier (volts/cm) control provided on the front panel of the oscilloscope. The height of the wave observed on the screen of CRO is adjusted with the help of Y – amplifier such that it fits on the screen of the CRO. Further the wave is deflected so that it coincides with the scale of the screen as shown in figure 11.19. From this figure it is clear that the length of the trace (in cm) measured on the scale will give the peak to peak voltage of the a.c. signal applied on the vertical input of CRO. The peak to peak voltage of the signal is calculated by multiplying the length of the

trace with the deflection sensitivity of the vertical amplifier. The rms value of this signal is obtained by dividing the peak to peak value by  $2\sqrt{2}$ .

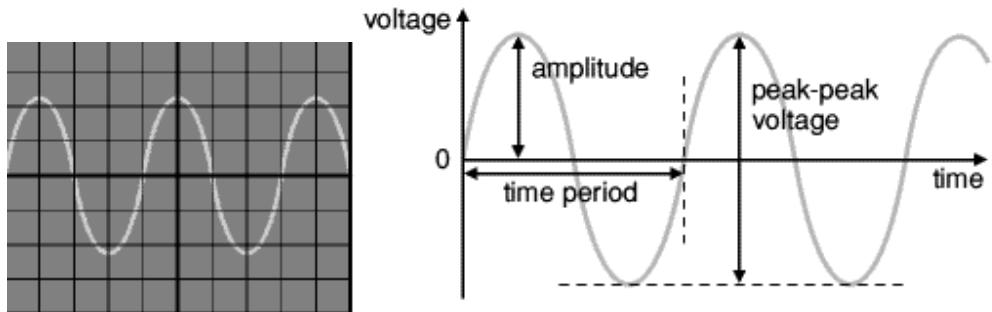


Fig. 11.19

To measure the d.c. voltage on the CRO, the position of the zero volt (normally halfway up the screen) is first checked. The AC/DC/GND switch is kept to GND (0V) and Y – shift is used to adjust the position of the trace to middle line on the CRO screen. The AC/DC/GND switch is thrown to the DC position and d.c. voltage is applied to the Y – input. The vertical displacement (in cm) of the horizontal line is multiplied by the deflection sensitivity of the vertical amplifier. This results the magnitude of the d.c. voltage.

The time period of the signal can also be measured with help of CRO. The time period is the time for one cycle of the signal. The frequency of the signal is the number of cycles per second i.e.

$$\text{Frequency} = \frac{1}{\text{time period}}$$

The horizontal distance (in cm) of the complete one cycle of the wave (fig. 11.19) is obtained from the CRO screen. This distance when multiplied by the scale of the time base control (Time/cm) gives the time period of the wave. The time period may be converted to frequency from the above formula.

**11.3.2 Measurement of Phase Difference:** The cathode ray oscilloscope can be used for the measurement of phase difference between two sinusoidal signals of the same frequency. One signal is applied to the Y – input of the CRO and other signal is applied to the X – input of CRO. The time base of the oscilloscope is in the external mode. On the screen of the CRO, a Lissajous figure (an ellipse) will be formed as shown in figure 11.20. From this figure on the CRO screen the maximum displacement  $y_2$  in the vertical direction and intercept  $y_1$  on the Y – axis are measured. The phase difference  $\theta$  of the two signals is given by the formula:

$$\theta = \sin^{-1} \left( \frac{y_1}{y_2} \right)$$

This phase difference can also be given by the formula:

$$\theta = \sin^{-1}\left(\frac{x_1}{x_2}\right),$$

where  $X_1$  is the intercept on the  $X -$  axis and  $X_2$  is the maximum horizontal displacement.

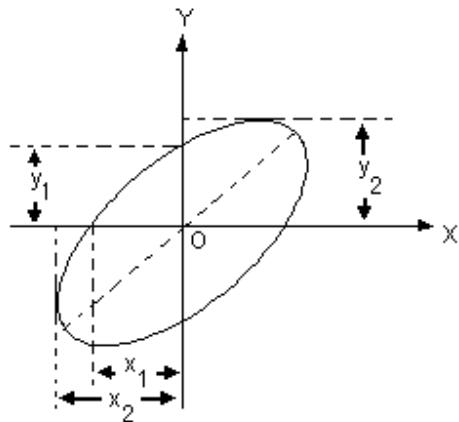


Fig. 11.20

**11.4 Function Generator:** A function generator is an electronic instruments used in laboratories. It provides different wave forms sine, square and triangular of adjustable frequencies and amplitude. The frequency of a wave may be adjusted from a fraction of an Hz to several hundred KHz.

In LC or RC oscillators the frequency is controlled by varying capacitor. However, in the function generators various types of wave shapes are to be generated, so the saw tooth wave is first generated with the help of an integrator. In the integrator circuit a capacitor is charged by the constant current source. The frequency of the saw tooth will depend upon the magnitude of the constant current source. The saw tooth wave is smoothed by the resistance and diode shaping circuit to get the sinusoidal wave. Further, square or triangular wave is obtained by simultaneously connecting the saw tooth wave to a comparator circuit. The comparator circuit limits the height of the square wave and time of integration.

Figure 11.21 shows the block diagram of such a function generator. It consists of two constant current sources namely positive and negative current source, the magnitude of these current sources is controlled by the frequency controlled network. Its control is done by a variable resistance provided on the front panel of the function generator. The outputs of these current sources are applied to an integrator circuit through a switching circuit. The switching circuit allows the positive constant current source to charge the capacitor of the integrated circuit. The output voltage of the integrator increases linearly with time by the relation given as:

$$V_o = -\frac{1}{C} \int_0^t I \cdot dt$$

where  $I$  is the magnitude of the constant current source.

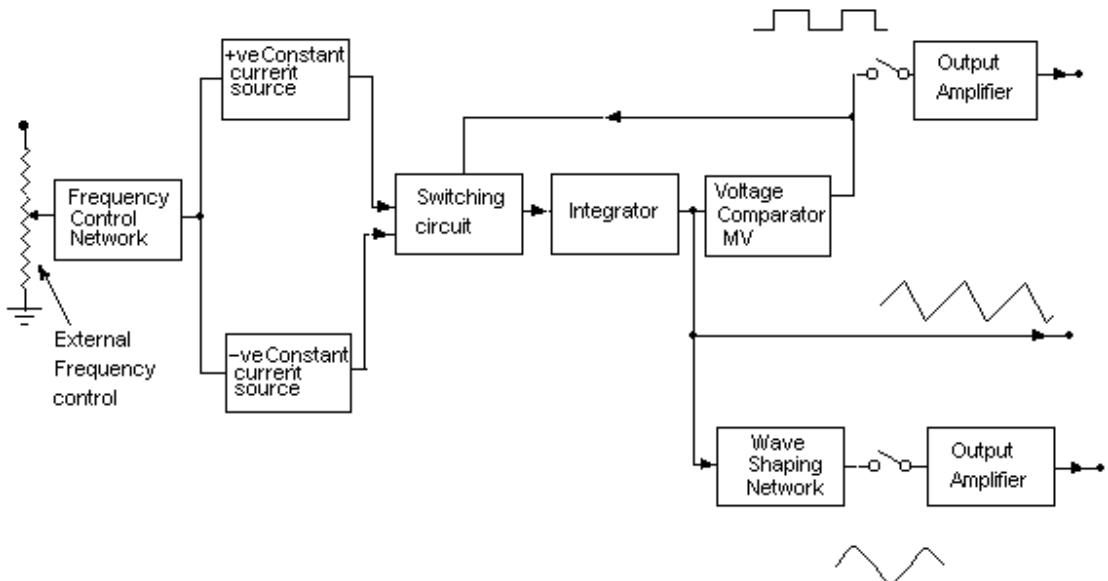


Fig. 11.21

Rising slope of the integrator output will depend upon the magnitude of the current source. As soon as the output voltage of the integrator reaches a predetermined level, the voltage comparator multivibrator changes its state and the switching circuit connects the input of the integrator to the negative constant current source.

The negative constant current source supplies the reverse current to the capacitor C. Thus the output voltage of the integrator decreases linearly with time. Further, as the voltage decreases to a predetermined level, the voltage comparator multivibrator changes its state. The switching circuit again connects back the positive constant current source to the integrator. The triangular wave form is therefore obtained at the output of the integrator, whose frequency is determined by the magnitude of the current supplied by the constant current source. The output of the comparator is the square wave; its frequency is the same as that of the triangular waves. The resistance and diode shaping network connected to the triangular wave, gives the sinusoidal wave. The output amplifiers are used to get the waves.

**11.5 Digital Frequency Meter:** The digital frequency meter is an electronic instrument used to measure the frequency of a periodic waveform. The basic principle for the precise determination of frequency of an unknown signal is illustrated in figure 11.22. The unknown signal is applied to amplifier/attenuator, where the signal is amplified if it is a weak signal and attenuated if the signal of high amplitude. The amplified signal is then connected to a Schmitt trigger circuit where the signal is converted to a square wave. The square is differentiated to get the narrow pulse train. The number of pulses in the pulse train is equal to the frequency of the input unknown signal. This narrow pulse train is then applied to one input of a two input AND gate. The second input of this AND gate is connected another standard sample pulse of constant width. The sample pulse controls

for how long the pulse train is allowed to pass through the AND gate to the digital counter. If the width of this sample pulse is kept as 1 second, then the AND gate will allow the pulse train to go to the input of the counter for 1 second. The counter will display the counts on the display devices (in digital form) counted by it for 1 second. The number displayed on the display devices will show the frequency of the input signal directly in Hz, since the number of pulses in the pulse train is equal to the frequency of the input unknown signal. The digital counter basically contains BCD counter, decoder and display unit (seven segment display).

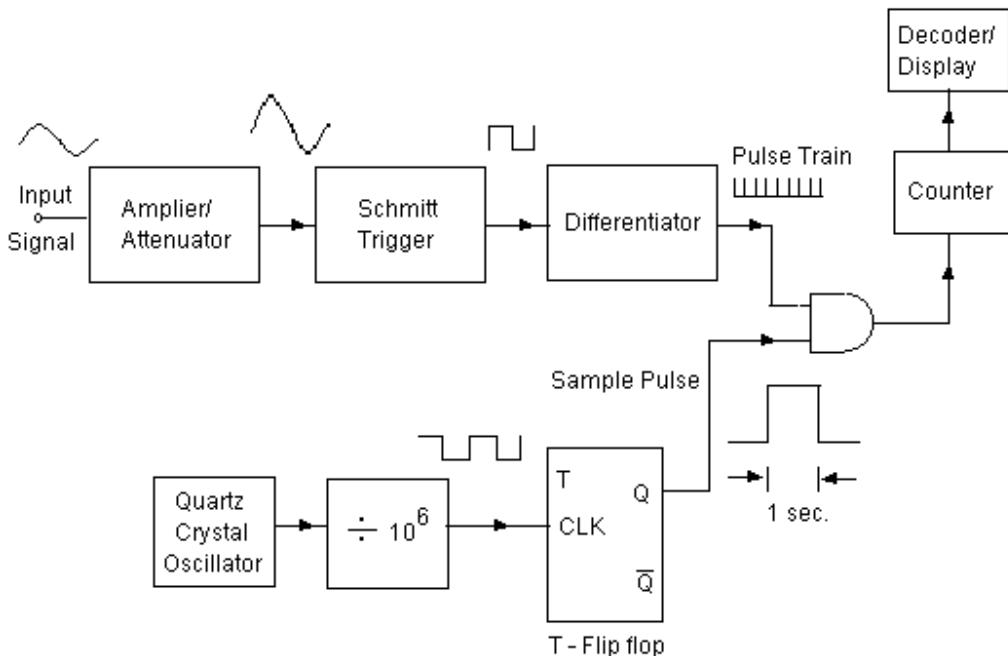


Fig. 11.22

The accuracy of the counter will depend on the accuracy of the width of the sample pulse. The sample pulse of standard time period is therefore, obtained from a high frequency quartz crystal oscillator, say, 1 MHz. The frequency of this crystal oscillator is divided by a factor of  $10^6$  using frequency divider circuit, which gives a square wave of 1 Hz frequency. Finally the 1 Hz frequency is divided a factor of 2, to obtain a square whose pulse width is 1 second. If the width of the sample pulse is taken as 1 msec, then the counter will display the frequency directly in KHz, if it is taken as 1  $\mu$ sec, the counter will display the frequency in MHz.

### Problem:

1. Draw the functional block diagram of the function generator. Explain the working of each block.
2. Discuss the principle and working of a digital frequency meter.
3. Draw the block diagram of a cathode ray tube and explain its main components.

4. Draw the basic block diagram of a cathode ray oscilloscope and explain the function of each block.
  5. Explain the use of CRO for the measurement of frequency of a signal.
  6. How the voltage of a signal is measured with the help of CRO?
  7. Explain how the phase difference of two signals is measured with the help of CRO.
  8. What is the need for time base generator in CRO?
  9. Draw the functional block diagram of an electronic multimeter. Explain the function of each block. What are its advantages over the conventional multimeter.
  10. Draw and explain the functional block diagram of a digital multimeter. What are the advantages of digital multimeter.
  11. What is an analog multimeter? Discuss the principle of measuring a.c./d.c. voltage with an analog multimeter.
  12. Discuss the principle of measuring the current with an analog multimeter.
  13. Discuss the principle of measuring resistance with an analog multimeter.
-

## Appendix - I

### Decibel:

To discuss the term decibel, consider an amplifier whose output power is  $P_2$  and input power is  $P_1$ . The ratio  $\frac{P_2}{P_1}$  is known as the power gain of the amplifier. This ratio may be more than unity or less than unity. If this ratio is more than unity the amplifier is said to have been gained, and if,  $\frac{P_2}{P_1}$  is less than unity, there is attenuation in the power of the amplifier.

When a number of power amplifiers are connected in tandem, then the overall power gain of such a cascaded amplifier is the product of power gains of the individual amplifier. It is, therefore, customary to define the power ratio on the logarithmic scale since it is an established fact that the power (or audio level) is related on the logarithmic basis. The overall gain will easily be obtained by adding the logarithmic units rather than multiplying.

The power gain in logarithmic scale is defined as :

$$\text{Power gain} = \log_{10} \left( \frac{P_2}{P_1} \right) \text{ bel}$$

The unit *bel* was found to be quite larger unit for practical purposes, a smaller unit known as *decibel (db)* is defined which is one - tenth of a *bel*.

$$1 \text{ bel} = 10 \text{ db}$$

So power gain in *db* is defined as:

$$\text{Power gain (in db)} = 10 \log_{10} \left( \frac{P_2}{P_1} \right) \text{ db}$$

It is interesting to note that there is a power gain of 0 *db* if output power is equal to the input power ( $P_2 = P_1$ ). If  $P_2 = 2P_1$  i.e. output power is twice the input power then there is a gain of 3*db* as:

$$\begin{aligned} \text{Power gain (in db)} &= 10 \log_{10} \left( \frac{P_2}{P_1} \right) = 10 \log_{10} \frac{2P_1}{P_1} \text{ db} \\ &= 10 \log_{10}(2) = 10 \times 0.3010 = 3 \text{ db} \end{aligned}$$

If on the other hand the power of the amplifier is attenuated by a factor of two i.e.  $P_2 = \frac{P_1}{2}$ , there is the loss of power (reduced half); however, in *db* it will be denoted by – 3db (negative quantity) as:

$$\begin{aligned}\text{Power gain (in } db\text{)} &= 10 \log_{10} \left( \frac{P_2}{P_1} \right) = 10 \log_{10} \frac{P_1}{2P_1} db \\ &= 10 \log_{10} \left( \frac{1}{2} \right) = -10 \log_{10}(2) = -10 \times 0.3010 = -3db\end{aligned}$$

Further, if  $V_1$  and  $I_1$  are the voltage and current of the input of the amplifier; and  $V_2$  and  $I_2$  are the voltage and current of the output of the amplifier, the ratio  $\frac{P_2}{P_1}$  is given as:

$$\frac{P_2}{P_1} = \frac{V_2^2/R_2}{V_1^2/R_1} = \frac{I_2^2 R_2}{I_1^2 R_1}$$

If  $R_1 = R_2$ , then

$$\frac{P_2}{P_1} = \frac{V_2^2}{V_1^2} = \frac{I_2^2}{I_1^2}$$

Thus power gain in *db*

$$= 10 \log_{10} \left( \frac{P_2}{P_1} \right) = 20 \log_{10} \left( \frac{V_2}{V_1} \right) = 20 \log_{10} \left( \frac{I_2}{I_1} \right)$$

Generally, the input and output impedances are not equal, so if the effect of different impedances is ignored, the voltage gain or the current gain of the amplifier can conveniently be expressed in *decibels* as:

$$\text{Voltage gain in } db = 20 \log_{10} \left( \frac{V_2}{V_1} \right) db = 20 \log_{10} (A_V) db$$

$$\text{Current gain in } db = 20 \log_{10} \left( \frac{I_2}{I_1} \right) db = 20 \log_{10} (A_I) db$$

## Appendix – II

### Switches

Switch is a device used for opening and closing a circuit. Switches are designed in variety of sizes, types and shapes. Some most commonly available switches are being discussed.

**(1) Single Pole Single Throw (SPST) Switches:** The SPST switch also called toggle switch, has one switch contact set and one conducting position. It can connect or disconnect of a single wire or line. It is in fact a simple on – off switch. This type of switch can be used to switch the power supply to a circuit. Figure 1(a) shows the symbolic representation of SPST switch and figure 1(b) shows the commercially available switch.



Fig. 1(a)



Fig. 1(b)

**(2) Push – to – On Momentary SPST Switch:** Figure 2(a) shows the symbolic representation of this switch and its physical appearance is shown in figure 2(b). This switch returns to its normally open (OFF) position, when the push button is released. It momentarily makes the connection. It is like the door bell switch.

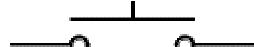


Fig. 2(a)



Fig. 2(b)

**(3) Push – to – Off Momentary SPST switch:** This type of switch is shown in figure 3. It performs the reverse function of push to on momentary switch, that is, the switch returns to its normally close (ON) position, when the push button is released. It momentarily breaks the circuit.



Fig. 3(b)



Fig. 3(a)

**(4) Single Pole Double Throw Switch (SPDT):** Such a switch has two ON positions. It has three terminals, when the switching position is in the centre the two circuits will be in the off positions. When the switch is thrown to either of the two positions it closes the corresponding one circuit. Figure 4 shows its physical appearance and schematic diagram.



Fig. 4(a)

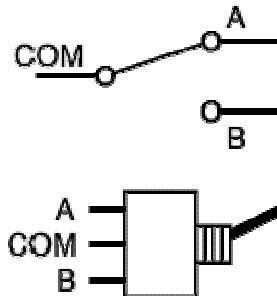


Fig. 4(b)

**(5) Double Pole Double Throw (DPDT) Switch:** It has a pair of On – Off switches which operate together as shown by dotted lines of its schematic diagram (fig. 5a). Figure 5(b) shows its physical appearance.

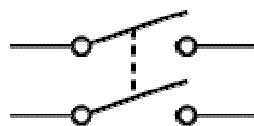


Fig. 5(a)



Fig. 5(b)

**(6) Push – Push Switch:** Physical appearance of this type of switch is shown in figure 6. It looks like a momentary action push switch but it is standard on – off switch. It is switched to on when pushed once and it is pushed off when pushed again. This is called a latching action.



Fig. 6

**(7) Reed Switch:** The reed switches have a glass body inside which micro switches usually SPST are there. It is shown in figure 7. Its contacts are closed when a small magnet is brought near the switch. Such switches may be used in security circuits.



Fig. 7

**(8) DIP (Dual – in – line parallel) Switch:** This switch is a set of miniature SPST on – off switches is a dual in line integrated circuit package. Figure 8 shows such switch containing 8 miniature switches.



Fig. 8

**(9) Rotary Switch:** Rotary switches have 3 or more conduction positions, by rotating the shaft connections to different poles may be made. Figure 9 shows the schematic and physical appearance of such switch.

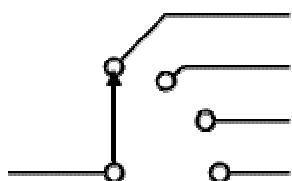


Fig. 9(a)



Fig. 9(b)

## **Appendix – III**

### **Resistances**

Resistances are the passive elements used in electronics. They are measured in ohms ( $\Omega$ ). The resistances are available in different variety. While using the resistance one should know the following specifications of the resistances.

<u>Specifications</u>	<u>Remarks</u>
1. Nominal Value                      in ohms	Value indicated on the resistor usually by color code.
2. Tolerance                        in $\pm X\%$	Real value will be with in $\pm X\%$ of the nominal value.
3. Wattage                          in watts	Maximum power that can be dissipated in a resistor.
4. Temperature coefficient ppm/ $^{\circ}\text{C}$	Variation of resistance with temperature.
5. Stability                        in %	Variation of resistance with ageing and ambient conditions.

The most widely used resistances are carbon composition, carbon film, metal film and wire wound. The carbon composition resistors are inexpensive and therefore, generally used in entertainment purposes. They are not very stable and their tolerances are also not very good. Metal films resistances are, however, very stable and its tolerances are also very good. They are costly. Such resistances are used in the circuits in which accuracy is the important factor. The wire wound resistances are available in high wattages; the size of such resistors increases as the wattage is increased. Such resistances are never used in high frequency circuits.

The nominal value and the tolerance of the resistances are obtained from the color bands indicated on the resistances. Each resistance has four color bands and each color band represents a number shown in table 1.

**Table 1**

The Resistor Color Code	
Color	Number
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

- The first band gives the first digit.
- The second band gives the second digit.
- The third band indicates the number of zeros.
- The fourth band is used to shows the tolerance (precision) of the resistor, usually fourth band is silver or gold. If the fourth band is silver then it tolerance is 10%, and for gold its tolerance is 5%.

Figure 1 shows the color code of one resistance. This resistor has red (2), violet (7), yellow (4 zeros) and gold bands 5%. So its value is  $270000 \Omega \pm 5\% = 270 \text{ K} \Omega \pm 5\%$ .

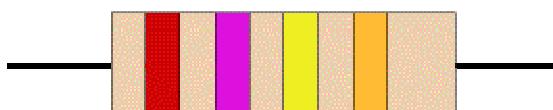


Fig. 1

**Small value resistors (less than 10 ohm):** The standard color code cannot show values of less than  $10 \Omega$ . To show these small values two special colors are used for the third band: gold which means  $\times 0.1$  and silver which means  $\times 0.01$ . The first and second bands represent the digits as normal.

For example: The color code of  $2.7 \Omega$  resistance is red, violet and gold.

**Variable resistances:** Variable resistors consist of a resistance track with connections at both ends and a wiper which moves along the track as the spindle is turned. The track may be made from carbon or a coil of wire (for low resistances). Figure 2 shows the physical appearance of this type of variable resistance also called potentiometer.



Fig. 2

The potentiometers are available in linear and logarithmic tracks. The linear track means that the resistance changes at a constant rate as the wiper is moved. In most of the electronic circuits LIN potentiometers are used. However, in log potentiometers, the resistance changes slowly at one end of the track and changes rapidly at the other end, so halfway along the track is not half the total resistance. These types of potentiometers are used for volume controls in audio equipments.

**Preset potentiometers:** Preset pots are used where precise variation of resistances is required. Preset pots are available in single turn and multi-turn pot. The screw is provided in multi-turn pots. The screw moves the slider from one end of the track to the other end giving the very fine control. Figure 3 shows such presets.

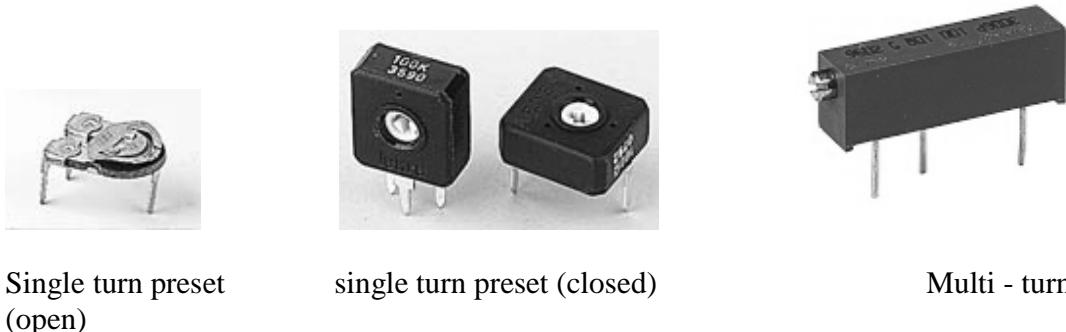


Fig. 3

## Appendix – IV

### Capacitors

Capacitors store electric charge. The capacitors are also used in filter circuits because it easily pass AC (changing) signals but they block DC (constant) signals. The capacity of a capacitor is its ability to store charge. A large capacitance means that more charge can be stored. Capacitance is measured in farads, and its symbol is F. However 1 F is very large, so prefixes are used to show the smaller values.

Three prefixes (multipliers) used with Farad F are  $\mu$  (micro), n (nano) and p (pico):

$$1 \mu\text{F} = 10^{-6} \text{ F}$$

$$1 \text{nF} = 10^{-9} \text{ F}$$

$$1 \text{pF} = 10^{-12} \text{ F}$$

All capacitors are generally classified in to two categories, namely:

- (1) Fixed Capacitors and      (2) Variable Capacitors.

**(1) Fixed Capacitors:** The fixed capacitors can be sub-divided into two groups.

**(a) Electrolytic capacitors:** They are large value capacitors (more than  $1 \mu\text{F}$ ). These capacitors use electrolyte (borax or carbon salt) as the negative plate. An Aluminium anode acts as the positive plate, while a thin film of Aluminium oxide on the anodes acts as the dielectric. The electrolytic capacitors are used in circuits where a dc voltage is present, because it requires the dc polarizing voltage. Since Electrolytic capacitors are polarized so they must be connected to the correct polarity. At least one lead of the electrolytic capacitor is marked as + or -. They are not damaged by heat when soldering.

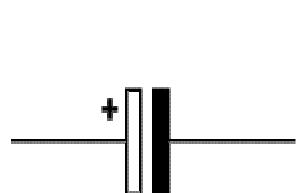


Fig. 1(a)

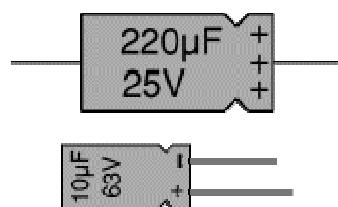


Fig. 1(b)

The value of electrolytic capacitors is printed on the capacitor with their voltage ratings (fig.1). The voltage rating of the capacitors should always be checked while selecting an electrolytic capacitor. In the circuits, one should use the capacitors with a voltage rating greater than the circuit's power supply voltage; otherwise the capacitor may be damaged. The symbolic representation of the electrolytic capacitor is shown in figure 1(a).

**(b) Non electrolytic capacitors:** It includes paper, mica and ceramic capacitors. These capacitors have no polarity requirement, i.e., they can be connected in either direction in the capacitors. They are low value capacitors (less than  $1\mu F$ ) with small size. The circuit symbol and its physical appearance of these capacitors are shown in figure 2.

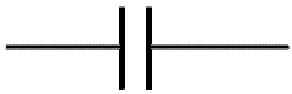


Fig. 2(a)

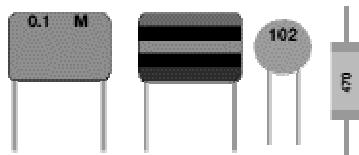


Fig. 2(b)

To find the value of these capacitors a number code is often used on small capacitors where printing is difficult:

- 1st number is the 1st digit,
- 2nd number is the 2nd digit,
- 3rd number is the number of zeros to give the capacitance in pF.
- Ignore any letters - they just indicate tolerance and voltage rating.

For example: **102** means  $1000 \text{ pF} = 1\text{nF}$  (*not  $102\text{pF}$* )

**472J** means  $4700 \text{ pF} = 4.7\text{nF}$  (J means 5% tolerance).

**222** means  $2200 \text{ pF} = 2.2 \text{ nF}$

**(2) Variable Capacitors:** As the name indicates its capacitance can be varied by rotating the small spindle connected with the capacitors. These capacitances are also called gang capacitors. The gang capacitor is shown in figure 3 with its symbol. Variable capacitors are mostly used in radio tuning circuits and they are sometimes called 'tuning capacitors'. They have very small capacitance values, typically between  $100 \text{ pF}$  and  $500 \text{ pF}$ .

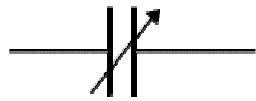


Fig. 3(a)



Fig. 3(b)

**Trimmer capacitors:** Trimmer capacitors (trimmers) are miniature variable capacitors. They are designed to be mounted directly onto the circuit board and adjusted only when the circuit is built. A small screwdriver or similar tool is required to adjust trimmers. The process of adjusting them requires patience because slight variation in the screw driver position will not give the required capacitance in the circuit. Trimmer capacitors are only available with very small capacitances, normally less than 100pF. It is usually specified by their minimum and maximum values, for example 2-10 pF. The Trimmer capacitor is shown in figure 4.



Fig. 4(a)



Fig. 4(b)