ANALOG ELECTRONICS

(CIRCUITS and DEVICES)

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Solution: This circuit is replaced into its Norton's equivalent form. For this find short circuit current by short circuiting the AB terminals as shown in figure (1.45). Short circuit current may be obtained using Superposition theorem.

(i) Consider only current source of 3 *A*, and 30 *V* source is shorted, the short circuit current $I^{'}$ is given by: $I^{'} = \frac{3Ax5}{10} = 1.5A$

(ii) Consider only 30V source, and 3A source is open circuited, we get the short circuit current I" as: $I^{"} = \frac{30V}{10+10} = 1.5A$

Net short circuit current I_0 is given by: $I_0 = I^{'} + I^{"} = 1.5 + 1.5 = 3A$

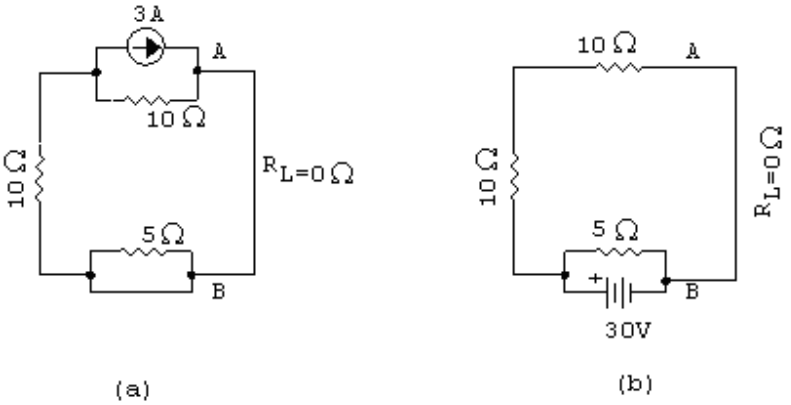


Fig. 1.45

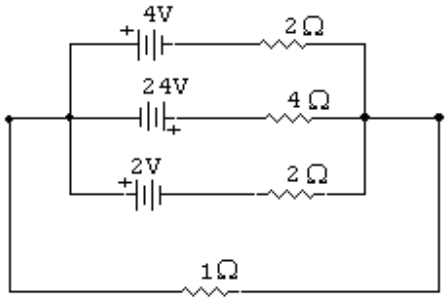
The open circuit resistance R_S (across AB terminals) is obtained by short circuiting the voltage source and open circuiting the current source as:

$$R_S = 10 + 10 = 20\Omega.$$

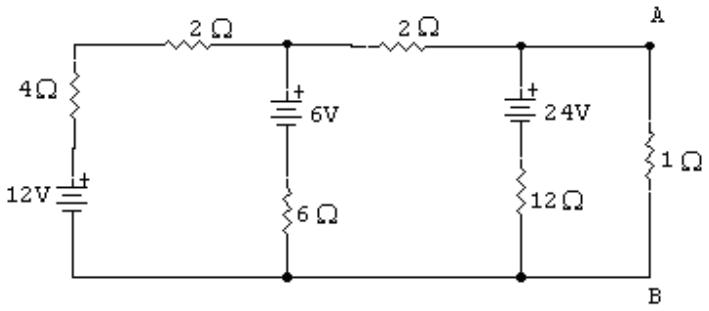
The circuit may be replaced in Noton's and Thevenin's equivalent forms as shown in figure (1.46).

Fig. 1.46

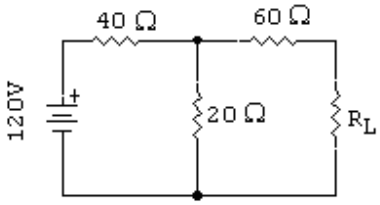
The value of R_L for maximum power transfer should equal to source resistance R_S. So R_L=20 Ω and maximum power $P_{\max} = \frac{V_0^2}{4R_L} = \frac{(60)^2}{4x20} = 45Watt$



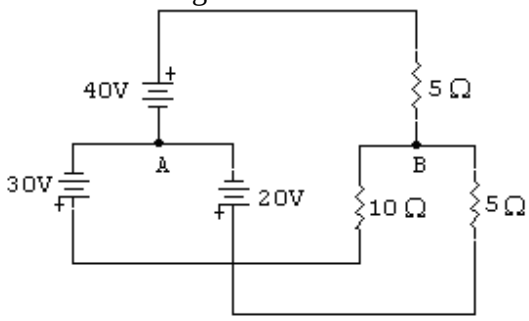
23. Using Norton's theorem, compute current through 1Ω resistance in the given circuit. (Ans. 2.8 A)



24. In the circuit shown below, find the current flowing through the load resistance R_L of 10Ω. For what value of $R_{L,}$ the power delivered to the load is maximum? Also compute the maximum power. (Ans. 0.48A, 73.3Ω, 5.45watt)



25. Using Millman's theorem find the current through a resistance of 25Ω connected between A & B points in the circuit given below. (Ans. 1A)



26. Apply Superposition theorem to find the voltage across AB branch in the given circuit. Verify the result using Loop method also. (Ans. 10 volts)

(iii) $H_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0}$ The corresponding diagram is shown below:

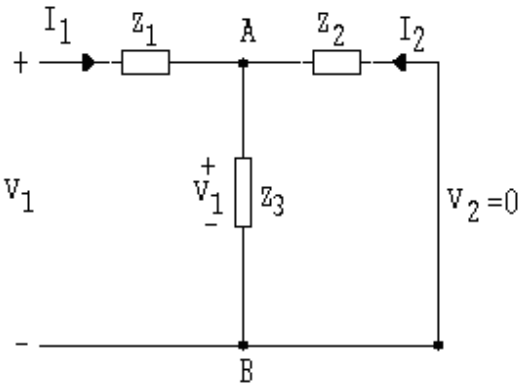


Fig.2.9

Voltage across *AB* points is $V_{AB} = I_1[Z_2 \| Z_3] = \frac{Z_2 Z_3}{Z_2 + Z_3} I_1$

$$I_2 = -\frac{V_{AB}}{Z_2} = -\frac{Z_3 I_1}{(Z_2 + Z_3)}$$

or $$H_{21} = \frac{I_2}{I_1} = -\frac{Z_3}{(Z_2 + Z_3)}$$

(iv) $H_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$ Since I_1=0 (Ref. Fig.2.8)

So $V_2 = I_2 (Z_2+Z_3)$

or $$H_{22} = \frac{I_2}{V_2} = \frac{1}{Z_2 + Z_3}$$

Example. 2.2 Find H' parameters of the given Π - network.

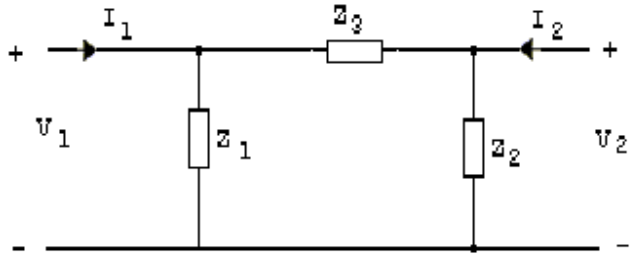


Fig. 2.10

Solution: (i) $H'_{11} = \left.\frac{I_1}{V_1}\right|_{I_2=0}$

The relation between V_1 and I_1 when I_2 = 0, is given by:

$$V_1 = I_1\left[Z_1 \| (Z_2 + Z_3)\right]$$

or $$V_1 = I_1\left[\frac{Z_1(Z_2 + Z_3)}{Z_1 + Z_2 + Z_3}\right]$$

or $$H'_{11} = \frac{I_1}{V_1} = \frac{Z_1 + Z_2 + Z_3}{Z_1Z_2 + Z_1Z_3}$$

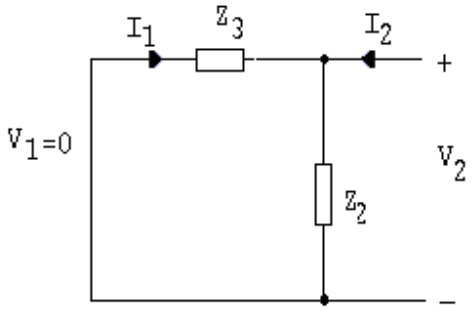


Fig. 2.11

(ii) $$H'_{12} = \left.\frac{I_1}{I_2}\right|_{V_2=0}$$

$$V_2 = I_2\left(\frac{Z_2Z_3}{Z_2 + Z_3}\right) \quad \text{and} \quad I_1 = -\frac{V_2}{Z_3}$$

Combining these two equations, we get

$$I_1 = -\frac{Z_2}{(Z_2 + Z_3)}I_2 \quad \text{or} \quad H'_{12} = \frac{I_1}{I_2} = -\frac{Z_2}{Z_2 + Z_3}$$

(iii) $$H'_{21} = \left.\frac{V_2}{V_1}\right|_{I_2=0}$$ When $I_2 = 0$, the relation between V_1 and V_2 is given by:

$$V_2 = \frac{V_1}{(Z_2 + Z_3)}Z_2 \quad \text{or} \quad H'_{21} = \frac{V_2}{V_1} = \frac{Z_2}{(Z_2 + Z_3)}$$

(iv) $$H'_{22} = \left.\frac{V_2}{I_2}\right|_{V_1=0}$$ The relation between V_2 & I_2 when $V_1 = 0$ is given by (Ref. Fig. 2.11).

$$V_2 = I_2\frac{Z_2Z_3}{Z_2 + Z_3} \quad \text{or} \quad H'_{22} = \frac{V_2}{I_2} = \frac{Z_2Z_3}{Z_2 + Z_3}$$

Example 2.3 Find the transmission Parameters of the network given in figure 2.12. The network is excited by a sinusoidal signal of 10^4 radians /sec.

Solution: The given twin T- network is the parallel combination of the two individual T-networks, which is clear from the given circuit shown the fig. (2.23).

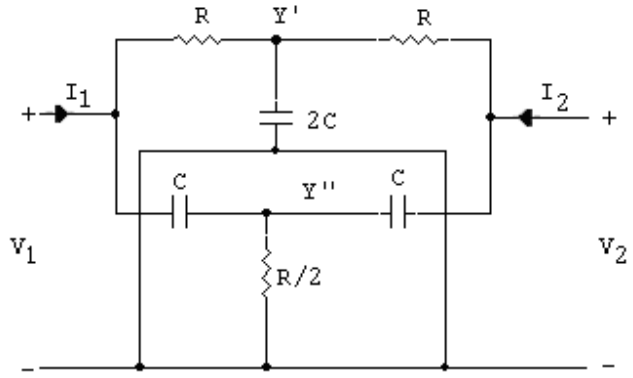


Fig. 2.23

The *Y*-parameters of this *T*- network may be given by:

$$Y_{11} = Y_{11}^{'} + Y_{11}^{''} \qquad Y_{12} = Y_{12}^{'} + Y_{12}^{''}$$
$$Y_{21} = Y_{21}^{'} + Y_{21}^{''} \qquad Y_{22} = Y_{22}^{'} + Y_{22}^{''}$$

Y-parameters of the upper *T*- network may easily be obtained and are given by:

$$Y_{11}^{'} = Y_{22}^{'} = \frac{R + \dfrac{i}{2j\omega C}}{\left[R^2 + \dfrac{R}{2j\omega C} + \dfrac{R}{2j\omega C}\right]} = \frac{(1 + 2j\omega CR)}{2R(1 + i\omega CR)}$$

$$Y_{12}^{'} = Y_{21}^{'} = \frac{-\dfrac{1}{2j\omega C}}{\dfrac{1}{2j\omega C}\left[2R + 2j\omega cR^2\right]} = -\frac{1}{2R(1 + j\omega CR)}$$

Y-parameters of the lower T- network are given by:

$$Y_{11}^{''} = Y_{22}^{''} = \frac{\left[\dfrac{R}{2} + \dfrac{1}{j\omega C}\right]}{\left[-\dfrac{1}{\omega^2 C^2} + \dfrac{R}{2j\omega C} + \dfrac{R}{j\omega C}\right]} = \frac{(2 + j\omega CR)\, j\omega C}{2(1 + j\omega CR)}$$

$$Y_{12}^{''} = Y_{21}^{''} = \frac{-R/2}{\dfrac{2(1 + j\omega CR)}{2j^2\omega^2 C^2}} = \frac{\omega^2 C^2 R^2}{2R(1 + j\omega CR)}$$

The required Y- parameters of the given Twin T- network are given by:

$$V_1 = \frac{7}{2}V_2 - \frac{15}{2}I_2$$

$$I_1 = \frac{3}{2}V_2 - \frac{7}{2}I_2$$

These two equations may be rewritten in the form of *Z*-parameter equations.

$$\frac{3}{2}V_2 = I_1 + \frac{7}{2}I_2 \qquad \text{or} \qquad V_2 = \frac{2}{3}I_1 + \frac{7}{3}I_2$$

$$V_1 = \frac{7}{3}I_1 + \frac{2}{3}I_2$$

Comparing these two equations with *Z*-Parameter equations we get the *Z*-parameters of the given network.

$$Z_{11} = Z_{22} = \frac{7}{3}\Omega \qquad Z_{12} = Z_{21} = \frac{2}{3}\Omega$$

2.9 Dependent sources: So far we have discussed the characteristics of the Passive network having passive elements connected to it. Now the active network having the active elements will be discussed. The active elements used in the network may very likely be transistor, operational amplifiers etc. However, the controlled or dependent Source considered as the basic active element, may be classified as:

(i) Voltage Controlled Voltage Source (VCVS)
(ii) Voltage Controlled Current Source (VCCS)
(iii) Current Controlled Current Source (CCCS)
(iv) Current Controlled Voltage Source (CCVS)

(i) Voltage Controlled Voltage Source (VCVS): It is an ideal voltage source whose voltage is dependent on the input voltage. The network equation may be written by considering following H' or *T*-parameters of the network.

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \mu & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} \Leftrightarrow \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \frac{1}{\mu} & o \\ o & o \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

$I_1 = 0$

& $V_2 = \mu V_1$ Input is open circuited and output is Ideal voltage source, which will depend on the input voltage.

The equivalent network may be drawn as given in Fig. (2.33).

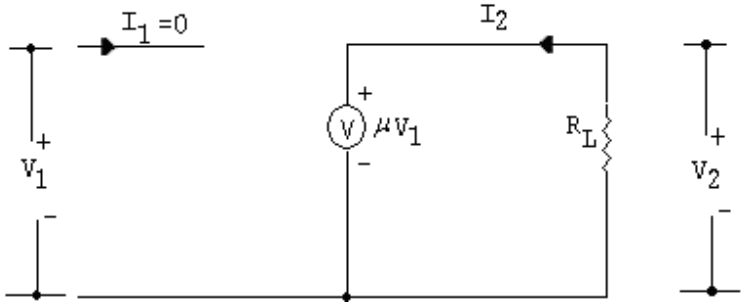


Fig. 2.33

Thus $$\frac{E}{\sqrt{R^2+\left[\omega L-\frac{1}{\omega C}\right]^2}}=\frac{E}{\sqrt{2}R} \qquad \text{------ (3.30)}$$

or $$\sqrt{R^2+\left[\omega L-\frac{1}{\omega C}\right]^2}=\sqrt{2}R \qquad \text{------ (3.31)}$$

or $$R^2+\left[\omega L-\frac{1}{\omega C}\right]^2=2R^2$$

or $$\left[\omega L-\frac{1}{\omega C}\right]^2=R^2$$

or $$\left[\omega L-\frac{1}{\omega C}\right]=\pm R \qquad \text{------ (3.32)}$$

since $\omega_2 > \omega_1$, then $$\left[\omega_1 L-\frac{1}{\omega_1 C}\right]=-R \qquad \text{------ (3.33)}$$

and $$\left[\omega_2 L-\frac{1}{\omega_2 C}\right]=R \qquad \text{------ (3.34)}$$

Adding equations (3.33) & (3.34) we get $$(\omega_1+\omega_2)L-\frac{1}{C}\left(\frac{\omega_1+\omega_2}{\omega_1\omega_2}\right)=0$$

or $$\omega_1\omega_2=\frac{1}{LC}$$

Subtracting equation (3.33) from (3.34), one may get:

$$(\omega_2-\omega_1)L+\frac{1}{C}\left(\frac{\omega_2-\omega_1}{\omega_1\omega_2}\right)=2R$$

or $$(\omega_2-\omega_1)\left(L+\frac{1}{C\omega_1\omega_2}\right)=2R$$

or $$(\omega_2-\omega_1).2L=2R \qquad \text{or} \quad (\omega_2-\omega_1).=\frac{R}{L} \qquad \text{------ (3.35)}$$

$\omega_2-\omega_1$ is known as the Band Width ($\Delta\omega$) and is the band of frequency which lies between two points of either side of resonant frequency where the current falls to $\frac{1}{\sqrt{2}}$ of its resonant value.

The Q-factor of this series circuit is $$Q=\frac{\omega_0 L}{R} \qquad \text{------ (3.36)}$$

From equations (3.35) &(3.36), we have $$Q=\frac{\omega_0}{(\omega_2-\omega_1)}$$

differentiation of the input signal which can be given by:

$$E_0 = RI = RC\left(\frac{dE_I}{dt}\right) \qquad \text{------ (3.58)}$$

This circuit may thus be called as the differentiating circuit. The R – C Differentiating Circuit is identical with the R – C high pass filter.

3.10.2 R – C Integrating Circuit: When a current *I* is passed through a capacitance, then the voltage across the capacitance E_0 is be given by:

$$E_0 = \frac{1}{C}\int Idt \qquad \text{------ (3.59)}$$

This voltage is proportional to the integration of the input current *I*. Now we consider the R – C network as shown in figure (3.26a), a signal *E*

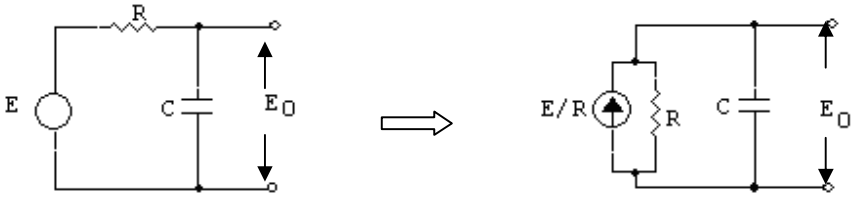


Fig. 3.26(a) (b)

is applied to the input terminals and voltage E_0 is measured across the capacitance *C*. The input signal *E* is converted to the current source *I* (conversion of Thevenin's equivalent to Norton's equivalent). The current *I* is given by: $I = E / R$

So $$E_0 = \frac{1}{C}\int(\frac{E}{R})dt = \frac{1}{RC}\int Edt \qquad \text{------ (3.60)}$$

The equation (3.60) clearly indicates that the output voltage across the capacitance is proportional to the input voltage *E*. Hence this circuit is called as an Integrator. The integrator circuit is identical to the R – C low pass filter.

Problems:

1. Prove that the Fourier Series expansion of the half wave rectified output is given by:

   $$E = \frac{E_m}{\pi} + \frac{E_m}{2}Sin\omega t - \frac{2E_m}{3\pi}Cos2\omega t - \frac{2E_m}{15\pi}Cos4\omega t - \frac{2E_m}{35\pi}Cos6\omega t.....$$

   where $f(t) = E_m Sin\omega t$ when $0 \le t \le T/2$

   $f(t) = 0$ when $(T/2) \le t \le T$
2. Prove that the Fourier Series expansion of the Full wave rectified output is given by:

   $$E = \frac{2E_m}{\pi} - \frac{4E_m}{3\pi}Cos2\omega t - \frac{4E_m}{15\pi}Cos4\omega t - \frac{4E_m}{35\pi}Cos6\omega t.....$$

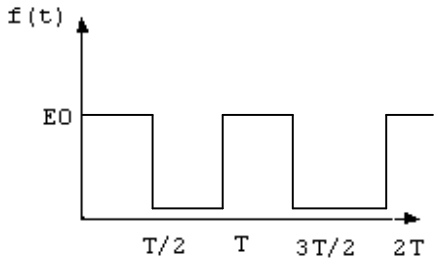
   where $f(t) = E_m Sin\omega t$ when $0 \le t \le T/2$

$$f(t) = -E_m Sin\omega t \quad \text{when} \quad (T/2) \le t \le T$$

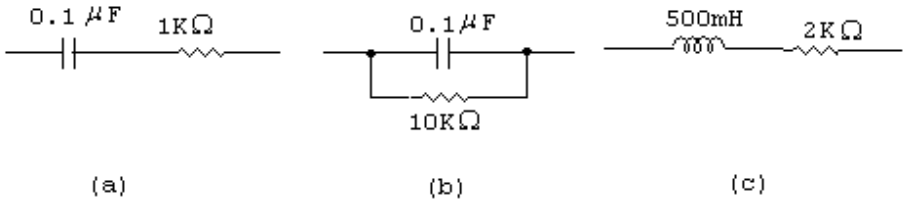
3. Consider a symmetrical triangular wave of peak value E_m and period T. Show that the Fourier Series expansion of the wave is given by:

$$E = \frac{E_m}{2} - \frac{E_m}{\pi} Sin\ \omega t - \frac{E_m}{2\pi} Sin\ 2\omega t - \frac{E_m}{3\pi} Sin\ 3\omega t .....$$

4. Find the Fourier series expansion of the square wave shown in figure given below.



5. Discuss (i) R – L low pass filter, (ii) R – C Low pass filter. Draw the frequency and phase response curves of these filters. Find the expression of cut-off frequency in each case.
6. Discuss (i) R – L High pass filter, (ii) R – C High pass filter. Draw the frequency and phase response curves of these filters. Find the expression of cut-off frequency in each case.
7. Explain the working of R – C integrator circuit.
8. Explain the working of R – C differentiator circuit.
9. Show that the output across the resistance in an R – C circuit is the differential of the input signal.
10. Show that the output across the capacitance in an R – C circuit is the integration of the input signal.
11. Discuss the transient response of an R – C circuit.
12. Discuss the transient response of an R – L circuit.
13. Show that the series R – L – C circuit behaves as a band pass filter. Draw the frequency and phase response curve of this series circuit. Find the expression for the band width also.
14. Show that the parallel R – L – C circuit behaves as a band rejection filter. Draw its frequency and phase response curve. Find the expression for the band width also.
15. Find the impedances of the following network at 1 KHz frequency.



Ans.(a) $1.88K\Omega\angle -57.9^0$, (b) $8.48K\Omega\angle -32.13^0$, (c) $3.72K\Omega\angle 57.5^0$

4.1.1 Intrinsic Semiconductors: Extremely pure form of a semiconductor is known as Intrinsic Semiconductor. The most commonly used semiconductors are Germanium and Silicon, which lies in the IV group of the periodic table. The atomic number of Germanium is 32, so it has 32 electrons, 2 electrons in the first orbit, 8 in the second orbit and 4 in the outer most orbit. Similarly the atomic number of Silicon is 14, and has 14 electrons; 2 electrons are in the first orbit, 8 electrons in the second orbit and 4 electrons in the outer most orbit. Both Germanium and Silicon have the crystalline structure.

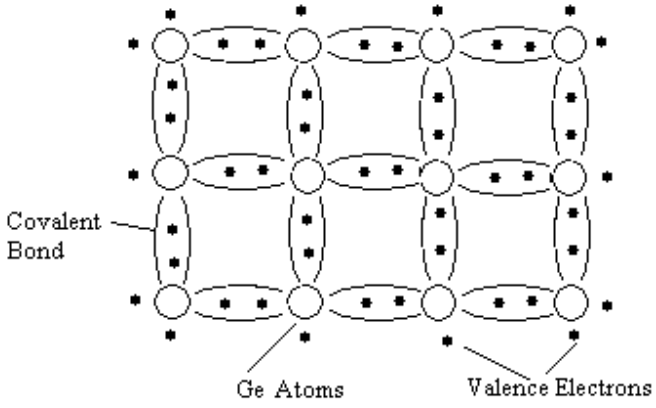


Fig. 4.2

Figure (4.2) shows that germanium (or silicon) atoms are held through covalent bonds. Each of the four electrons in a germanium (or silicon) atoms are shared by the valence electrons of four adjacent germanium (or silicon) atoms. The covalent bonds thus provide the binding force between the neighbouring atoms. The outer most orbits of atoms seem to be complete having 8 (shared) electrons. Consequently, the pure semiconductors (Ge or Si) behave as perfect insulator at 0^0 K. When the temperature is increased, some of the covalent bond is broken, the electrons are released and move to the conduction band. The empty space is left behind in the valence band. This empty space is known as hole and has the charge equal to that of an electron but opposite in sign. Thus each broken bond creates an electron-hole pair. The holes move through the crystal lattice in the random fashion as the free electrons and contribute to the current flow when an electric field is applied. Both these carriers drift in opposite directions giving rise to conventional current in the direction of flow of holes or in the direction opposite to the flow of electrons.

It is worthwhile to mention the following points with regards to the intrinsic semiconductor:

(1) When a covalent bond breaks an electron – hole pair is created. So in an intrinsic semiconductor the number of electrons and number of holes are equal.

(2) In the semiconductors the current flow is due to both the charge carriers unlike in the case of metals in which the current flow is only due electrons.

Table 4.1

Property	Symbols	Units	Ge	Si
Atomic No.	Z		32	14
Atomic Weight	W		72.6	28.1
Density	g	Kg/m^3	$5.32x10^3$	$2.33x10^3$
Atomic Concentration		atoms/ m^3	$4.4x10^{28}$	$5x10^{28}$
Dielectric constant	ε_r		16	12
Band gap at 0^0 K	E_{go}	eV	0.785	1.21
Band gap at 300^0 K	E_g	eV	0.72	1.1
Intrinsic carriers	n_i	$Carriers/m^3$	$2.5x10^{19}$	$1.5x10^{16}$
Intrinsic resistivity	ρ	Ohm-m	0.45	2300
Mobility of electrons	μ_n	m^2/sec-volt	0.38	0.13
Mobility of holes	μ_p	m^2/sec-volt	0.18	0.05
Diff. const. for electrons	D_n	m^2/sec	$9.9x10^{-3}$	$3.4x10^{-3}$
Diff. const. for holes	D_p	m^2/sec	$4.7x10^{-3}$	$1.3x10^{-3}$

It may be mentioned here that the band gap (E_g) of Ge or Si varies with temperature given by:

$Eg(T) = 1.21 - 3.60\ x10^{-4}.T$ for Si

$Eg(T) = 0.785 - 2.23\ x10^{-4}.T$ for Ge

where T is the temperature in *Kelvin.*

Example 4.1 (a) Find the resistivity of the intrinsic germanium crystal at 300^0 K. (b) What will be the resistivity of this germanium crystal if the donor impurity of 1 atom per 10^8 germanium atoms is introduced? Given that n_i = 2.5 $x10^{19}$ atoms/m^3, μ_n = 0.38 m^2/volt-sec, μ_p = 0.18 m^2/volt-sec, Atomic conc. of *Ge* = $4.4x10^{28}$ atoms/m^3 .

Solution: (a) The conductivity of the intrinsic germanium is given by:

$$\sigma_{\text{int}} = qn_i(\mu_n + \mu_p) = 1.6x10^{-19}\,x2.5x10^{19}(0.38+0.18)$$
$$= 1.6x2.5x5.6 = 2.24 \quad \text{mhos/m}$$

The resistivity of the intrinsic germanium is given by:

$$\rho = \frac{1}{\sigma} = \frac{1}{2.24} = 0.45 \quad \Omega\text{-}m$$

(b) $$N_D = \frac{4.4x10^{28}}{10^8} = 4.4x10^{20}$$

$$\sigma_{N-type} = q\mu_n N_D = 1.6\,x10^{19}\,x0.38\,x4.4\,x10^{20}$$
$$= 26.752 \quad mhos/m$$

$$\rho_{N-type} = \frac{1}{\sigma_{N-type}} = \frac{1}{26.752} = 0.037 \quad \Omega\text{-}m$$

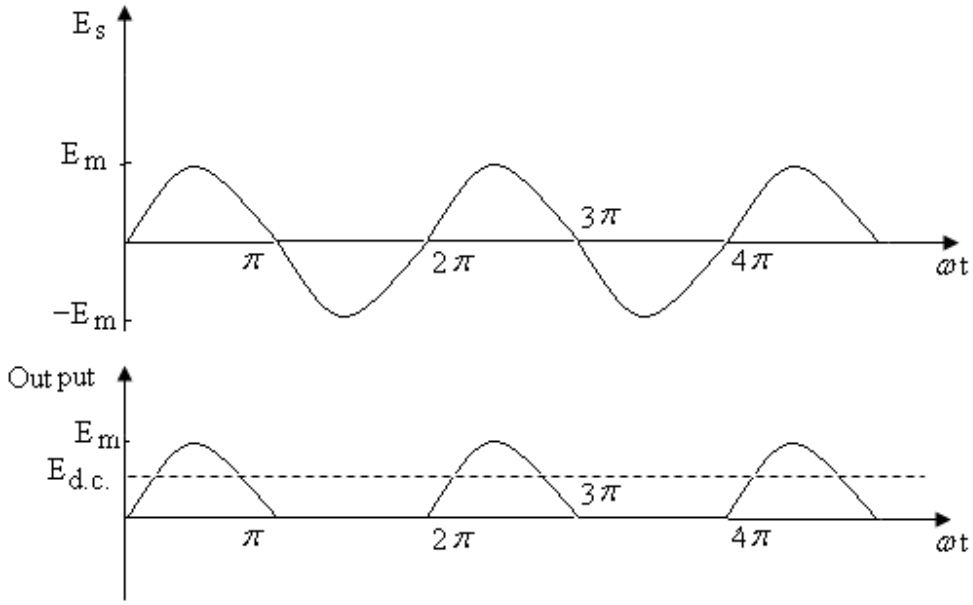


Fig. 5.2

From this figure it is clear that the current in the load resistance flows only during positive half cycle of the input wave and is zero during the negative half cycle, i.e., the current is unidirectional. Hence the circuit is called a half wave rectifier.

Analysis: The input a.c. voltage is given by $E_s = E_m \sin \omega.t$

Since the current in the load resistance is unidirectional, so we take the average value of the voltage across the resistance. It may be given as:

$$E_{d.c.} = \frac{1}{T}\int_0^{T/2} E_m \sin \omega.t.dt \qquad = \frac{E_m}{\pi} \qquad \text{since } T = \frac{2\pi}{\omega}$$

The d.c. current flowing through the load resistance R_L is given by:

$$I_{d.c.} = \frac{E_{d.c.}}{R_L} = \frac{E_m}{\pi R_L}$$

$$= \frac{I_m}{\pi} \qquad \text{(where } I_m = \frac{E_m}{R_L} \text{ is the peak current)}$$

The output voltage across the load resistance may be given by the Fourier analysis as:

$$E_{out} = \frac{E_m}{\pi} + \frac{E_m}{2}\sin \omega t - \frac{2E_m}{3\pi}\cos 2\omega t - \frac{2E_m}{15\pi}\cos 4\omega t - \frac{2Em}{31\pi}\cos 6\omega t - .....$$

------ (5.1)

From equation (5.1), it may be seen that the first term of the equation is the same as $E_{d.c.}$ as calculated above. In addition to this term there are other terms of frequency ω and its higher harmonics. So the output voltage across the load resistance has the required voltage ($E_{d.c}$) and other unwanted components called the ripple.

The root mean square value of the output voltage may be given by:

From these wave shapes, it is clear that the direction of current in the load resistance is same for both the half cycles of the output wave. Hence, the circuit is called as full wave rectifier.

Analysis: In this circuit the centre tapped terminal of the transformer is used as the common terminal of two voltages E_{S1} and E_{S2} which are 180 out of phase.

Let $E_{S1} = -E_{S1} = E_m Sin\,\omega t$

The average value (d.c.) of the voltage across the load resistance for the full wave rectifier is given by:

$$E_{d.c.} = \frac{1}{T}\left[\int_0^{T/2} E_{S1}\,dt + \int_{T/2}^{T} E_{S2}\,dt\right]$$

$$= \frac{1}{T}\left[\int_0^{T/2} E_m \sin\omega t.dt - \int_{T/2}^{T} E_m \sin\omega t.dt\right]$$

which may be simplified as $= \frac{2E_m}{\pi}$.

The r.m.s. value of the voltage across the load resistance is given by:

$$E^2_{r.m.s.} = \frac{1}{T}\left[\int_0^{T/2} E^2_{S1}.dt + \int_{T/2}^{T} E^2_{S2}.dt\right]$$

$$= \frac{1}{T}\left[\int_0^{T/2} E^2_m \sin^2\omega t.dt + \int_{T/2}^{T} E^2_m \sin^2\omega t.dt\right] \quad = \frac{E^2_m}{2}$$

or $E_{r.m.s.} = \frac{E_m}{\sqrt{2}}$

From the Fourier analysis the voltage across the load resistance is given by:

$$E_L = \frac{2E_m}{\pi} - \frac{4E_m}{3\pi}\cos 2\omega.t - \frac{4E_m}{15\pi}\cos 4\omega.t - \frac{4E_m}{31\pi}\cos 6\omega t - \ldots \quad \text{------ (5.5)}$$

It is clear from this equation that first term of the output voltage across the load resistance is the same as that of $E_{d.c.}$, calculated above. Further the lowest frequency term (ripple) in the full wave rectifier circuit is twice the frequency of supply signal.

The ripple factor γ is calculated as:

$$Ed.c. = \frac{16.97}{1 + \frac{1}{2x50x1000x10^{-6}x1000}} = \frac{16.97}{1.1} = 16.8 \text{ Volts}$$

$$I_{d.c.} = \frac{E_{d.c.}}{R_L} = \frac{16.8}{1000} = 16.8mA$$

$$E_R = \frac{I_{d.c.}}{f.C} = \frac{16.8x10^{-3}}{50\ x1000\ \ x10^{-6}} = 0.336 \text{ Volts}$$

$$I_m = \frac{E_m}{R_L} = \frac{16.97}{1000} = 16.97mA$$

If 25% increase in the a.c. signal then peak voltage also increases in the same ratio i.e.

$E_m = 16.97 + 0.25x16.97 = 21.2$ Volts

So the voltage rating of the capacitor should be greater than 21.2 Volts may be taken of 25 Volts or 50 volts.

5.4.2 Full Wave Rectifier with Shunt Capacitor Filter: The circuit diagram of this filter is shown in figure (5.10). The working of this circuit is similar to that of the half wave rectifier with shunt capacitor filter; the only difference between the two is that the circuit works for the half cycles. The input – output wave shaped is given in figure (5.11).

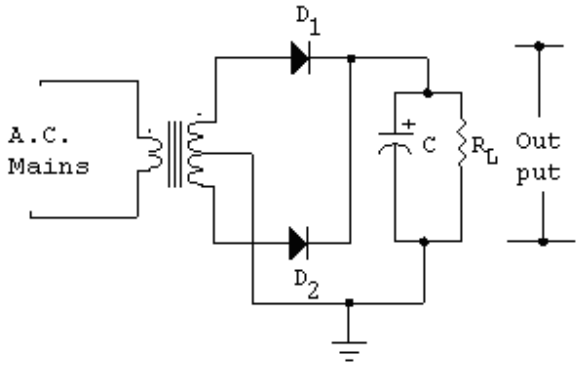


Fig. 5.10

(vi) Overall Current Gain A_{IS} : If the input source is a current source I_S in parallel with the source resistance R_S (i.e. Norton's equivalent of the voltage source), then the overall current gain A_{IS} is given by:

$$A_{IS} = -\frac{I_2}{I_S} = \frac{-I_2}{I_1}.\frac{I_1}{I_S} = A_I \frac{I_1}{I_S}$$

Using the Norton's equivalent of the voltage source V_S in the figure (7.12), we get:

$$I_1 = \frac{R_S}{R_S + Z_I} I_S$$

Then $$A_{IS} = \frac{A_I R_S}{R_S + Z_I}$$

Note that if $R_S = 0$, then $A_{IS} = A_I$. Also we have

$$A_{VS} = \frac{A_{IS} Z_L}{R_S}$$

The formulas derived above are summerised in table 7.3.

Table 7.3

$A_I = \frac{-h_f}{(1+h_o Z_L)}$	$Y_o = h_o - \frac{h_f h_r}{(h_i + R_s)} = \frac{1}{Z_0}$
$Z_I = h_i + h_r A_I Z_L$	$A_{VS} = \frac{A_V}{R_S + Z_I}.Z_I = \frac{A_I Z_L}{R_S + Z_I}$
$A_V = \frac{A_I Z_L}{Z_I}$	$A_{IS} = \frac{A_I R_S}{R_S + Z_I}$

Example 7.4 Prove for any single transistor amplifier

$$Z_I = \frac{h_i}{1 - h_r A_V}$$

Solution: We know $Z_I = h_i + h_r A_I Z_L$ ------- (7.43)

$$S = \frac{[(1+\beta)R_B(1+\frac{R_E}{R_B})]}{[(1+\beta)\frac{R_E}{R_B}+1]R_B}$$

$$S = \frac{(1+\beta)[1+\frac{1}{G_E}(G_1+G_2)]}{[1+\frac{(1+\beta)}{G_E}(G_1+G_2)]}$$

or $$= \frac{(1+\beta)[G_E+G_1+G_2)]}{[G_E+(1+\beta)(G_1+G_2)]}$$

or $$S = \frac{G_E+G_1+G_2}{\left[\frac{G_E}{(1+\beta)}+G_1+G_2\right]}$$ Hence proved.

Example 8.2: For the two battery transistor circuit shown in figure (8.8), prove that the stabilization factor *S* is given by:

$$S = \frac{1+\beta}{1+\beta\frac{R_E}{(R_E+R_B)}}$$

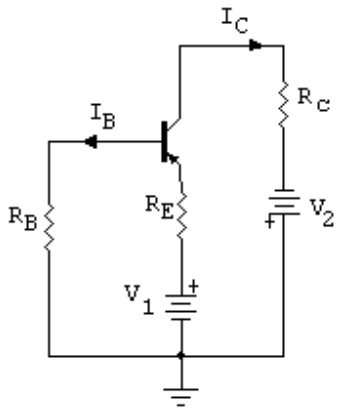


Fig. 8.8

Solution: Applying the KVL to the input circuit we get:

$$V_1 - V_{BE} = I_B R_B + I_B R_E + R_E I_C$$

or $$V_1 - V_{BE} = I_B(R_B+R_E) + R_E I_C$$ ----- (8.30)

The collector current is given by:

$$I_C = \beta I_B + (1+\beta)I_{CO}$$

or $$I_B = \frac{[I_C - (1+\beta)I_{CO}]}{\beta}$$ ------ (8.31)

From equations (8.30) & (8.31), we have

$$V_1 - V_{BE} = \left[\frac{I_C - (1+\beta)I_{CO}}{\beta}\right](R_B + R_E) + R_E I_C \qquad \text{------ (8.32)}$$

Differentiating the equation (8.32) with respect to I_{CO} , we may obtain the expression for the stability factor *S*.

$$\frac{\partial I_C}{\partial I_{CO}} R_E - \frac{(R_E + R_B)(1+\beta)}{\beta} + \frac{(R_B + R_E)}{\beta}\frac{\partial I_C}{\partial I_{CO}} = 0$$

$$\frac{(1+\beta)R_E + R_B}{\beta} S = \frac{(1+\beta)(R_E + R_B)}{\beta}$$

or $$S = \frac{(1+\beta)(R_E + R_B)}{[R_B + R_E + \beta R_E]}$$

or $$S = \frac{1+\beta}{1+\beta\dfrac{R_E}{(R_E + R_B)}}$$ Hence proved.

Example 8.3: In the transformer coupled amplifier shown in figure (8.9),

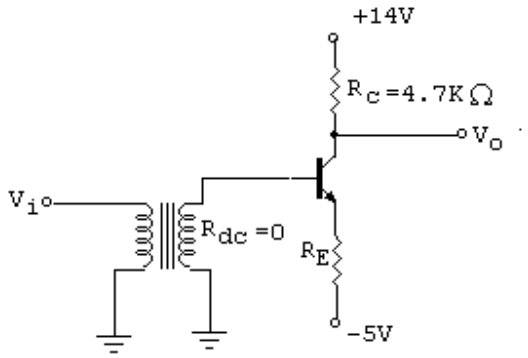


Fig. 8.9

V_{BE} = 0.7 volt, β = 45 and V_{CE} = 4 volts. Determine R_E and stability factor *S*.

Solution: Applying the KVL to the output circuit we get:

$$14 + 5 \approx 4.7K.I_C + 4 + R_E.I_C$$

or $$(4.7K + R_E)I_C = 15V$$

Applying KVL to the input circuit we get:

or $$I_{C2} - I_{CO2} = \beta_2 I_1$$

and $$I_{C1} - I_{CO1} = \beta_1 I_1$$

or $$\frac{I_{C2} - I_{CO2}}{I_{C1} - I_{CO1}} - 1 = \frac{\beta_2}{\beta_1} - 1$$

or $$\frac{\Delta I_C - \Delta I_{CO}}{I_{C1} - I_{CO1}} = \frac{\beta_2 - \beta_1}{\beta_1}$$

or $$\frac{\Delta(I_C - I_{CO})}{\Delta\beta} = \frac{I_{C1} - I_{CO1}}{\beta_1}$$

$$S'' = \frac{\Delta(I_C - I_{CO})}{\Delta\beta} = \frac{I_{C1} - I_{CO1}}{\beta_1}$$ Proved part III

8.9 Thermistor and Sensistor Compensation: In this compensation technique, the temperature sensitive element such as a thermistor or a sensistor is used rather than diode.

8.9.1 Thermistor Compensation: Figure (8.12) shows the self-bias CE transistor amplifier with thermistor compensation. Thermistor has a negative temperature

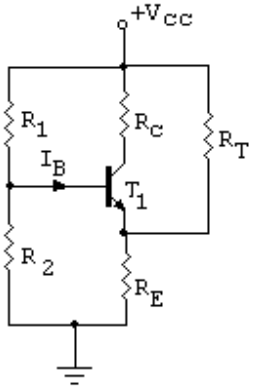


Fig. 8.12

coefficient of resistance i.e. its resistance decreases with the increase of temperature. Thermistor R_T connected between emitter and the positive supply compensate the variation of I_C with I_{CO}, V_{BE} or β caused due to the variation in temperature. As the temperature increases the resistance of R_T decreases, the current flowing through R_T in to R_E increases. Since voltage across R_E is in the direction to reverse bias the emitter base junction of the transistor, the increase in temperature will reduce the net forward bias of the emitter junction and as a result the collector current will remain fairly constant.

An alternative configuration using thermistor compensation is shown in Figure (8.13), in which the thermistor R_T is placed in parallel with R_2. As the temperature

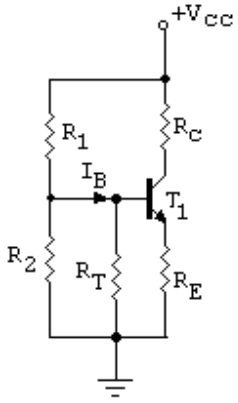


Fig. 8.13

increases, R_T decreases also the drop across R_T decreases. This results the decrease in collector current. This reduced I_C tends to compensate for the increased collector current caused by the rise in temperature.

8.9.2 Sensistor Compensation: For the operating point stability of the transistor, sensistor which has the positive temperature coefficient of resistance may be used as the compensating element instead of thermistor. The sensistor is placed either in parallel with R_1 or in parallel with R_E or in place of R_E in the self bias circuit. This may be explained that the net voltage drop across R_2 increases reducing thereby the collector current.

8.10 Thermal Runaway: In transistor amplifier, one must control the biasing of the transistor in such a way as to keep the average dissipation of the device below its maximum value. The amplifier design leads the operating point to shift with temperature in such a way as to burn out the transistor. The biasing problem is aggravated by an effect known as Thermal Runaway, which may be explained as follows. The collector-base junction of the transistor, where all of the dissipation occurs, is not in perfect contact with the transistor case. That is, there is some thermal resistance between the junction and the case, and between the case and ambient. Thus the power dissipated in the transistor will heat the junction to a temperature considerably above the ambient. The internal increase in temperature will cause a change in the transistor characteristics which in turn increases the power dissipation and the internal temperature. This cyclic chain of events will cause the rapid rise in transistor temperature and finally result the destruction of the transistor, known as thermal runaway. The power dissipation can be controlled and hence the thermal runaway be prevented, if the biasing arrangement is designed to keep the operating point approximately fixed in the $V_{CE} - I_C$ plane.

8.10.1 Thermal Resistance: Let T_J is the temperature of the collector base junction and T_A is the ambient temperature of the transistor. Here $T_J > T_A$ due to heating within the transistor. It has been observed that:

$$(T_J - T_A) \propto P_D$$

9

Field Effect Transistors

The field effect transistor (FET) is a three terminal semiconductor device in which the current is controlled by an electric field and used for variety of applications in electronics. Unlike the usual transistor, its operation depends upon the flow of majority carriers and the minority charge carriers play no significant role in the operation of the device. It is, therefore, known as a unipolar device. In usual transistors the current flow due to both types of charge carriers (electrons and holes) hence known as bipolar junction transistors (BJT). In the present chapter classification, operation and characteristics of the field effect transistors will be discussed. In addition the biasing and applications of the field effect transistors will also be illustrated.

9.1 Field Effect Transistors: The field effect transistors may broadly be classified in to the following two categories:

(1) Junction Field Effect Transistors (JFET)

(2) Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

It is also called Insulated Gate Field Effect Transistors (IGFET)

MOSFET's are further subdivided in two categories:

(i) Enhancement type MOSFET

(ii) Depletion type MOSFET

Each of the above categories may be either N – channel or P - channel.

The field effect transistors differ from the bipolar junction transistors in the following important characteristics:

$$= -\frac{2.I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$$

$$= g_{m0}\left(1-\frac{V_{GS}}{V_P}\right) \qquad \text{------ (9.8)}$$

Where g_{m0} is the value of gm for $V_{GS} = 0$ and given by:

$$g_{m0} = -\frac{2I_{DSS}}{V_P}$$

Combining the equations (9.7) and (9.8), we get:

$$g_m = -\frac{2}{V_P}\sqrt{I_{DSS}.I_{DS}} \qquad \text{------ (9.9)}$$

From the equation (9.9) it is clear that the transconductance gm varies as the square root of the drain current.

9.5 Small Signal Model of Field Effect Transistor: The drain current i_D may be expressed as a function of gate voltage v_{GS} and v_{DS} as given below:

$$i_D = f(v_{GS}, v_{DS})$$

The incremental change in the drain current i_D may be given by the Taylor series expansion as:

$$\Delta i_D = \frac{\partial.i_D}{\partial v_{GS}}.\Delta v_{GS} + \frac{\partial.i_D}{\partial v_{DS}}.\Delta v_{DS} \qquad \text{------ (9.10)}$$

In the small signal notation, $\Delta.i_D = i_d$, $\Delta.v_{GS} = v_{gs}$ and $\Delta.v_{DS} = v_{ds}$, the equation (9.10) may be written in the form:

$$i_D = g_m.v_{gS} + \frac{1}{r_d}.v_{dS} \qquad \text{------ (9.11)}$$

A circuit satisfying the equation (9.11) may be drawn as shown in the figure (9.12).

$$A_v = \frac{V_O}{V_i} = \frac{-\mu}{r_d + R_L + (1+\mu)R_S} xR_L \qquad \text{------ (9.29)}$$

Thevenin's equivalent of the equation (9.29) is given by (fig. 9.26):

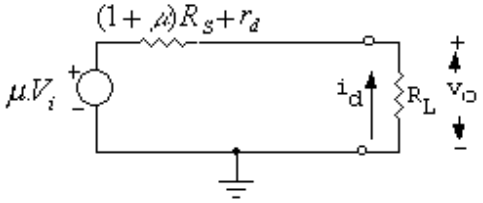


Fig. 9.26

The output resistance R_O is therefore given by:

$$R_O = r_d + (1+\mu)R_S$$

Example 9.4: In Common Source amplifier, a FET has r_d =200 $K\Omega$ and μ= 18. The load resistance R_L = 120 $K\Omega$. Compute the voltage gain and output resistance of this amplifier.

Solution: We know that the voltage gain of the Common Source amplifier is given by:

$$A_v = \frac{-\mu}{r_d + R_L} xR_L$$

$$= -\frac{18x10K\Omega}{(200+120)K\Omega} = -\frac{18}{21} = -6.7$$

The output resistance is given by:

$$R_O = r_d = 200\ K\Omega$$

Example 9.5: A Common Source FET amplifier uses load resistance R_L = 100 kΩ and an unbypassed resistance R_S = 10KΩ connected between the source and the ground. The drain resistance of the FET is 300 KΩ and μ=15. Compute the voltage gain and the output resistance of the amplifier.

Solution: The voltage gain of the common source amplifier with a source resistance R_s connected between source and the ground is given by:

$$A_v = \frac{-\mu}{r_d + R_L + (1+\mu)R_S} xR_L$$

$$= \frac{-15x100K\Omega}{(300+100+16x10)K\Omega} = \frac{-150}{56} = -2.67$$

The output resistance of the amplifier is given by :

$$R_O = r_d + (1+\mu)R_S = (300 + 16x10)K\Omega \quad = 460K\Omega$$

9.7 Biasing the FET: The amplifiers using FET have so far been discussed without showing the biasing arrangement as the d.c. biasing does not produce any significant role for the a.c. signal analysis. However, for the practical point of view the biasing of the FET' is very necessary. Like the bipolar transistors, the FET's have also to be biased properly. The consideration must be given to operate the field effect transistor in the linear region of its characteristic curves. Following are the biasing arrangements generally used in field effect transistors.

9.7.1 Source Self Bias: Figure (9.27) shows the self biasing arrangement for the field effect transistor. This type of biasing is generally used in JFET or depletion type MOS

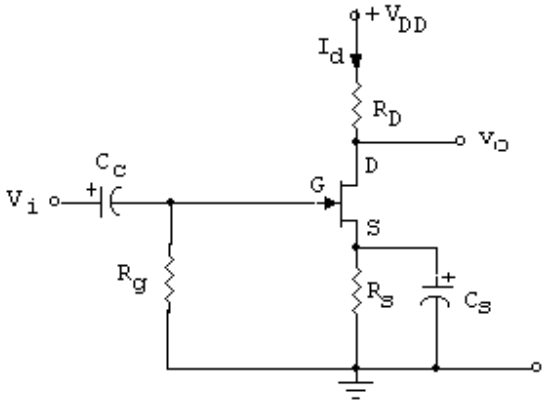


Fig. 9.27

FET's. In this circuit a resistance R_g is connected between the gate and the ground to bias the gate source junction in the reverse bias. The gate is supposed to be at ground potential as the voltage drop across R_g is negligibly small due to the very small gate current. To keep the gate at the negative potential with respect to the source, a resistance R_s is connected between the source and the ground. The voltage drop across Rs will be equal to $I_d.R_s$ i.e. the source is at the positive potential ($I_d.R_s$) with respect to ground. The gate is, therefore, at the negative potential with respect to the source since the gate is at the ground potential and source is at the positive potential. However the resistance R_s will produce a degenerative feedback for the a.c. signal to be applied to the input terminals. To avoid this problem a capacitance C_E is connected in parallel with the resistance R_s. The capacitance C_E bye passes the signal available at the source. Source is therefore called at the signal ground.

9.7.2 Voltage Divider Biasing: The voltage divider biasing arrangement can also be applied to the FET amplifiers as shown in figure (9.28).

(ii) According to the method of operation: The method of operation means the position of the operating point. The amplifiers are thus classified according to the method of operation as follows:

(a) **Class *A* amplifiers:** In class *A* amplifiers the operating point is chosen in the middle of the load line such that the output current follows for the entire input signal.

(b) **Class *B* amplifiers:** In class *B* amplifiers the operating point is fixed at an extreme end of the characteristics, so that quiescent power is very small. In this case the output current flows only for half of the input sinusoidal signal.

(c) **Class *AB* amplifiers:** The operating point, in this class *AB* amplifier, is fixed between the two extremes defined for class *A* and class *B* amplifiers. Hence in this class of amplifiers the output current is zero for a small part but less than half of the input sinusoidal signal.

(d) **Class *C* amplifiers:** The operating point in this class of amplifiers is fixed such that the output current flows only for less than half of the input sinusoidal.

(iii) According to their applications: The classification according to use includes voltage, power, current or general purpose amplifiers.

(iv) According to the method of inter - stage coupling: The amplifiers according to the method of inter stage coupling may be classified as follows:

(a) **Resistance – capacitance coupling** : When the coupling network, comprising resistance and capacitance is used to couple the output of one stage to the input of second stage then the amplifiers of this type are called as R – C coupled amplifiers.

(b) **Transformer coupling**: Amplifiers using this coupling are known as transformer coupled amplifiers. In these amplifiers transformers are used for inter stage coupling. The transformer coupled amplifiers saves the power dissipation.

(c) **Direct coupling**: For applications where the signal frequency is very low (may be below 10 Hz), the coupling networks discussed above are not used. In such cases output of the one stage is directly coupled to the input of the succeeding stages. The amplifiers using direct coupling are known as direct coupled amplifiers.

10.2 R – C Coupled Amplifier :

The circuit diagram of two stage R – C coupled amplifier is shown in figure (10.1). In this circuit two single stage common emitter amplifiers are coupled through R_{C1} and C_C network.

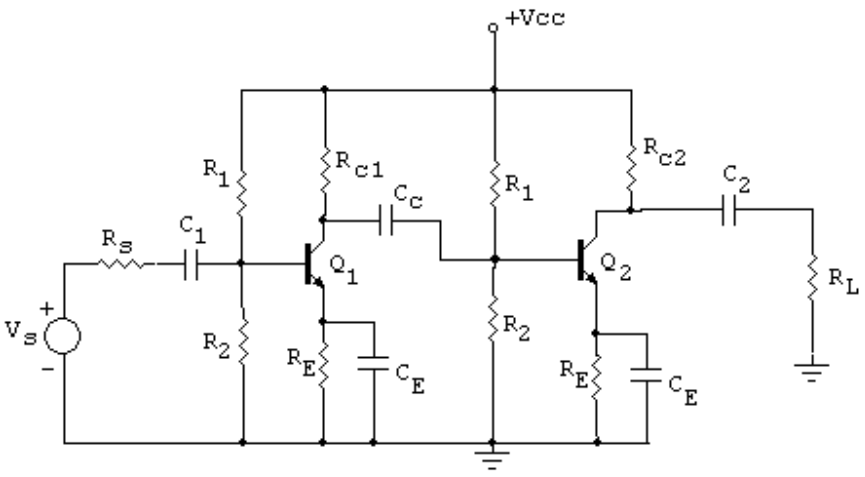
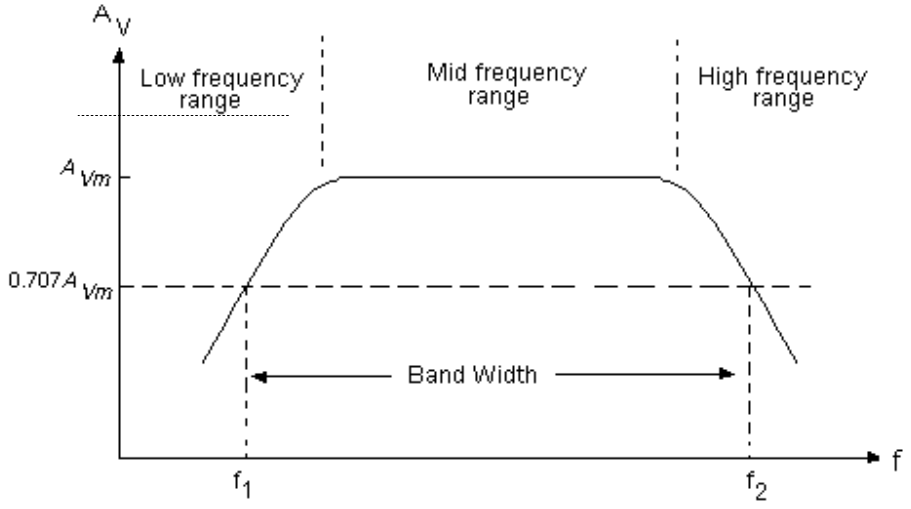


Fig. 10.1

In this circuit the resistances R_1, R_2, R_{C1}, R_{C2} and R_E are used to provide the self biasing and bias stabilization to the two transistors Q_1 and Q_2. The coupling capacitor C_C blocks the quiescent *d.c.* current and prevents it from appearing at the input of the second stage. However, C_C is so chosen that it offers negligible reactance for signal frequencies. Thus it couples the signal effectively to the second stage.

As is well known, the emitter resistance R_E is used to provide good stabilization to the transistor circuits; and larger the value of this resistance better will be biasing stability. But the larger value of R_E introduces larger amount of negative feedback in the circuit which on the contrary reduces the gain of the amplifier. To overcome this difficulty a bye pass capacitor C_E is connected in parallel with the emitter resistance R_E. The choice of a larger value for C_E makes the emitter at the signal ground.

10.2.1 Frequency Response: The curve representing the variation of gain of the amplifier with frequency is known as frequency response curve. It is shown for RC coupled amplifier in figure (10.2). The frequency response of



The short circuit current gain A_I is obtained as:

$$A_I = \frac{I_L}{I_i} = \frac{-g_m}{\frac{1}{r_{b'e}} + j.\omega.(C_{b'e} + C_{b'c})} \qquad \text{------ (10.29)}$$

Put $r_{b'e} = \frac{h_{fe}}{g_m}$ in equation (10.24) we have:

$$A_I = \frac{-g_m h_{fe}}{g_m + j.\omega.h_{fe}.(C_{b'e} + C_{b'c})}$$

$$= \frac{-h_{fe}}{1 + j.\omega.r_{b'e}.(C_{b'e} + C_{b'c})}$$

$$= \frac{-h_{fe}}{1 + j.\left(\frac{f}{f_h}\right)} \qquad \text{------- (10.30)}$$

where $f_h = \frac{1}{2.\pi.r_{b'e}.(C_{b'e} + C_{b'c})}$, is the cutoff frequency.

When $f = 0$, $A_I = -h_{fe}$ (low frequency current gain with output short circuited).

At $f = f_H$, $A_I = \frac{-h_{fe}}{\sqrt{2}}$ i.e. the current gain falls by $\frac{1}{\sqrt{2}}$ times the low frequency gain (or –3db fall of gain). The gain variation is shown in figure (10.10).

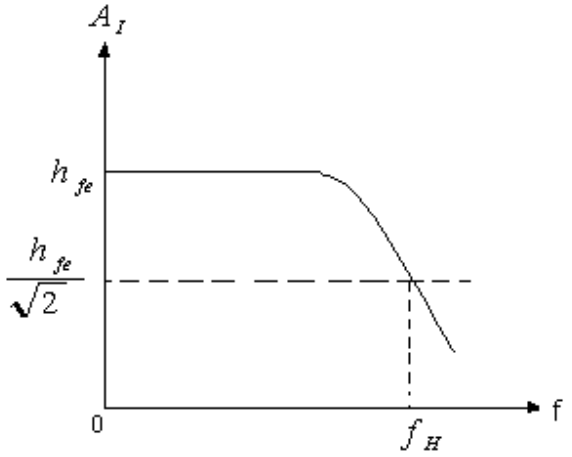


Fig. 10.10

$= 10.8W$

10.6 Class B Push – Pull Amplifier: The most frequently used power amplifier in the output stage of electronic circuits is the push pull amplifier. The push pull amplifier consists of two transistors and each transistor conducts in class *B* operation i.e. transistors are biased in the cutoff region so that the current flows only for half cycle in each transistor. In push pull amplifiers the transistors can also be used in class *A* mode but in this case the amplifier efficiency is not more than 50% and distortion is high. However the class *B* push pull amplifier provides low distortion and has the efficiency about 78.5%. The class *B* push pull amplifier is, therefore, used in the practical circuits. Figure 10.14 shows the circuit diagram of this class *B* push pull amplifier.

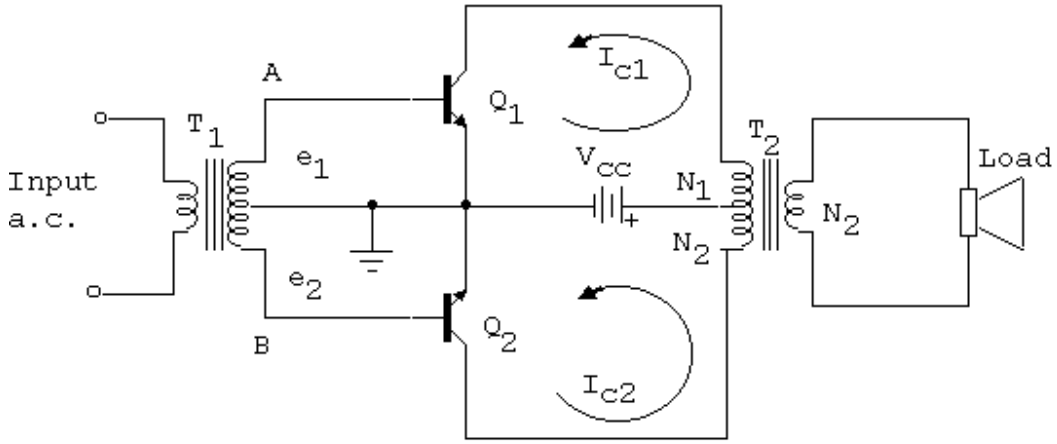


Fig. 10.14

This circuit consists of two transistors *Q1* and *Q2* whose emitters are coupled together and two centre tapped transformers T_1 and T_2. The two transistors are biased in the cutoff region so that the collector current flows only for half of the input cycle. The input transformer T_1 converts the input signal into two waves e_1 and e_2 which are 180^0 out of phase. When the point *A* is positive with respect to ground, point *B* will be negative with respect to ground and vice versa.

During the positive half of the input signal, the point *A* is positive and point *B* is negative with respect to the common point. The transistor Q_1 will conduct and the collector current Ic_1 will flow in the collector circuit of the transistor Q_1. The transistor Q_2 will, of course, be in the cutoff stage and the collector current I_{c2} in the collector circuit of transistor T_2 will not flow. During the next cycle of the input signal the case is reversed that the collector current I_{c2} in transistor Q_2 will be flowing and the collector current I_{c1} in the transistor Q_1 will be zero. These two currents flow in opposite directions in the two halves of the primary windings of the output transformer T_2. The centre tapped primary of this transformer T_2 combines two collector currents to form a sine wave output at the secondary. The effective load as seen by the amplifier is given by:

$$R_L^{'} = n^2.R_L$$

Where R_L is load resistance at the secondary of the transformer T_2 and *n* is the turn ratio of this transformer which is given by:

$$\theta = \sin^{-1}(\frac{x_1}{x_2}),$$

where X_1 is the intercept on the X – axis and X2 is the maximum horizontal displacement.

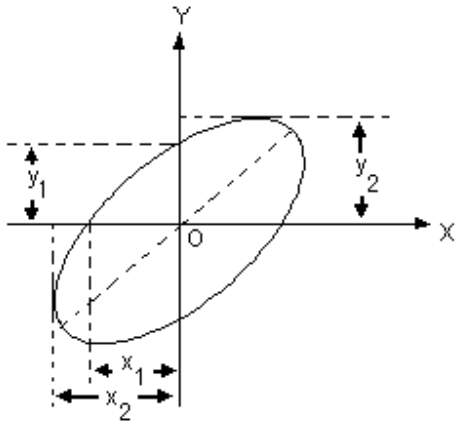


Fig. 11.20

11.4 Function Generator: A function generator is an electronic instruments used in laboratories. It provides different wave forms sine, square and triangular of adjustable frequencies and amplitude. The frequency of a wave may be adjusted from a fraction of an Hz to several hundred KHz.

In LC or RC oscillators the frequency is controlled by varying capacitor. However, in the function generators various types of wave shapes are to be generated, so the saw tooth wave is first generated with the help of an integrator. In the integrator circuit a capacitor is charged by the constant current source. The frequency of the saw tooth will depend upon the magnitude of the constant current source. The saw tooth wave is smoothened by the resistance and diode shaping circuit to get the sinusoidal wave. Further, square or triangular wave is obtained by simultaneously connecting the saw tooth wave to a comparator circuit. The comparator circuit limits the height of the square wave and time of integration.

Figure 11.21 shows the block diagram of such a function generator. It consists of two constant current sources namely positive and negative current source, the magnitude of these current sources is controlled by the frequency controlled network. Its control is done by a variable resistance provided on the front panel of the function generator. The outputs of these current sources are applied to an integrator circuit through a switching circuit. The switching circuit allows the positive constant current source to charge the capacitor of the integrated circuit. The output voltage of the integrator increases linearly with time by the relation given as:

$$V_o = -\frac{1}{C}\int_0^t I.dt$$

where I is the magnitude of the constant current source.