!nrst

*any EOP signal not during EOPchk will send system into ERR state
flush_ERR if it is in the middle of writing to data buffer

IDLE
all en = 0

dedge

START
en8 = 1
shift_en = 1
rx_transfer_active
= 1
flush = 1

SYNCWAIT

bit8

SYNC

byte_data
==
8'b00000001

PIDWAIT

bit8

PID

byte_data[0:4]
==
DATA0,DATA1

DATA_WAIT
w_en = 1

else

D_edge

ERR
RX_error = 1
all en = 0

else

byte_data[0:4]
==
OUT,IN

PACKET_TYPE2
RX_Packet =
OUT,IN
en8 = 0
en7 = 1

bit8

DATA_STORE
store_rx = 1
rx_packet_data
= byte_data

else

bit7

byte_data[0:4]
==
STALL

byte_data[0:4]
==
ACK,NAK

EOP

EOPchk

PACKET_TYPE1
RX_Packet =
ACK/ NACK

tknADDR
en7 = 0
en4 = 1

byte_data != ADDR

CRC_CHECK1
w_en = 0
r_en = 1

fifo_data
== crc1

CRC_CHECK2

byte_data != END

bit4

else

else

fifo_data
== crc2

byte_data[7:3] == CRC

EOP

CRC_CHECK

tknEND
en4 = 0
en5 = 1

else

bit5

FLUSH_ERR
flush = 1
RX_ERR = 1