CSA12 – COMPUTER ARCHITECTURE

INDEX - TUTORIAL

S.NO	TITLE	MARKS	SIGNATURE
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			

CPU PERFORMANCE:

1. Computers A and B implement the same ISA. Computer A has a clock cycle time of 250 ps and an effective CPI of 2.0 for some program and computer B has a clock cycle time of 500 ps and an effective CPI of 1.2 for the same program. Which computer is faster and by how much?

2. Suppose that when Program A is run, the user CPU time is 3 seconds, the elapsed wall clock time is 4 seconds, and the system performance is 10 MFLOP/sec. Assume that there are no other processes taking any significant amount of time, and the computer is either doing calculations in the CPU, or doing I/O, but it can't do both at the same time. We now replace the processor with one that runs six times faster, but doesn't affect the I/O speed. What will the user CPU time, the wall clock time, and the MFLOP/sec performance be now?

3. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. a. Which processor has the highest performance expressed in instructions per second? b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions. c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

ADDRESSING MODES:

4. Find the addressing mode used to indicate the location of the source operands and also calculate the effective address in the following instructions

   i. Sub 8(R3), R0
   ii. Add (R5), R0
   iii. Branch 16(PC)
   iv. Move (R4,R3), R0
   v. Move (C), LOC

INSTRUCTION FORMATS

5. Write a sequence of instructions that will compute the value of $y = x2 + 2x + 3$ for a given x using

a. three-address instructions
b. two-address instructions
c. one-address instructions

INSTRUCTION TYPES:

6. Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, how much amount of memory (in bytes) consumed by the program text?

7. A processor has 16 integer registers (R0, R1, … , R15) and 64 floating point registers (F0, F1, … , F63). It uses a 2 byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type 4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (1F). What is the maximum value of N ?

BOOTH ALGORITHM:

8. Perform the multiplication of (-13) and (-20) using Booth Algorithm.

9. Perform the multiplication of (-7) and (+3) by Binary Multiplication method and Recoding principle of Booth Algorithm.

Integer Restoring & Non Restoring Division

10. Perform Integer Division using Restoration Method for the Dividend (Q) = 11011011 and the Divisor (Q)= 110.

11. Perform the Division using Restoring and Non Restoring Division for the Dividend=1010 and Divisor = 0011

FLOATING POINT OPERATIONS:

12. Add the following two decimal numbers in scientific notation (0.91×10^{-1}) with (9.23×10^{1})

13. Multiply the following two numbers in scientific notation. (1.110×10^{10}) with (9.200×10^{-5})

14. Multiply (1.000×2^{-1}) with (-1.110×2^{-2})

PIPELINING STAGES:

15. Consider a pipeline having 4 phases with duration 30, 40, 80 and 70 ns. Given latch delay is 15 ns. Calculate-

1. Pipeline cycle time
2. Non-pipeline execution time
3. Speed up ratio
4. Pipeline time for 500 tasks
5. Sequential time for 500 tasks
6. Throughput

16. Consider a pipeline having 4 phases with duration 50, 60, 75 and 65 ns. Given latch delay is 20 ns. Calculate-

1. Pipeline cycle time
2. Non-pipeline execution time
3. Speed up ratio
4. Pipeline time for 800 tasks
5. Sequential time for 800 tasks
6. Throughput

17. Consider a non-pipelined processor with a clock rate of 3.0 gigahertz and average cycles per instruction of 3.5. The same processor is upgraded to a pipelined processor with five stages but due to the internal pipeline delay, the clock speed is reduced to 2.5 gigahertz. Assume there are no stalls in the pipeline. Find the speed up achieved in this pipelined processor.

18. Consider a non-pipelined processor with a clock rate of 2.0 gigahertz and average cycles per instruction of 4.1. The same processor is upgraded to a pipelined processor with five stages but due to the internal pipeline delay, the clock speed is reduced to 4.5 gigahertz. Assume there are no stalls in the pipeline. Find the speed up achieved in this pipelined processor.

SUPERSCALAR PROCESSORS:

19. In Super Scalar processor, find the In-order Execution, In-Order 2 way execution and out of order execution.

For the following instructions.

(1) R1= R2 + 5
(2) R3 = R1 / 3
(3) R5 = R3 * 4
(4) R6 = R4 + R5
(5) R7 = R2 + R3

20. In Super Scalar processor, find the In-order Execution, In-Order 2 way execution and out of order execution.
For the following instructions.

(1) R1= R2 - 3
(2) R3 = R1 + 6
(3) R5 = R3 * 5
(4) R6 = R4 - R5
(5) R7 = R2 / R3

CACHE MEMORY:

21. A computer has a 256 KB, 4-way set associative, write back data cache with block size of 32 bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

22. A block-set associative cache memory consists of 128 blocks divided into four block sets . The main memory consists of 16,384 blocks and each block contains 256 eight bit words.

1. How many bits are required for addressing the main memory?
2. How many bits are needed to represent the TAG, SET and WORD fields?

23. A 4-way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. How many number of bits available for the TAG field ?

VIRTUAL MEMORY:

24. A computer with virtual memory has an access time to main memory 50 ns, the time to transfer a block from the virtual into main memory is 10 ms. The probability for the page-fault is 10^{-6} . What is the average access time, if the page-table is in the main memory?

25. Computer with virtual memory has the following features:

- length of the virtual address is 38 bits,
- the page size is 16 KB,
- length of the physical address is 32 bits.

a) How many bits is the length of page descriptor, if in addition to the frame number (FN), additional parameters occupy another 6 bits?

b) What is the maximum size of the page-table in bytes?