Vivado工程1

组合逻辑电路的实现

2019.11.3 17:26

本工程的功能：输入两个逻辑变量，计算它们的与、与非、或、或非、异或、同或： a & b ~(a & b) a | b ~(a | b) a ^ b a ~^ b。

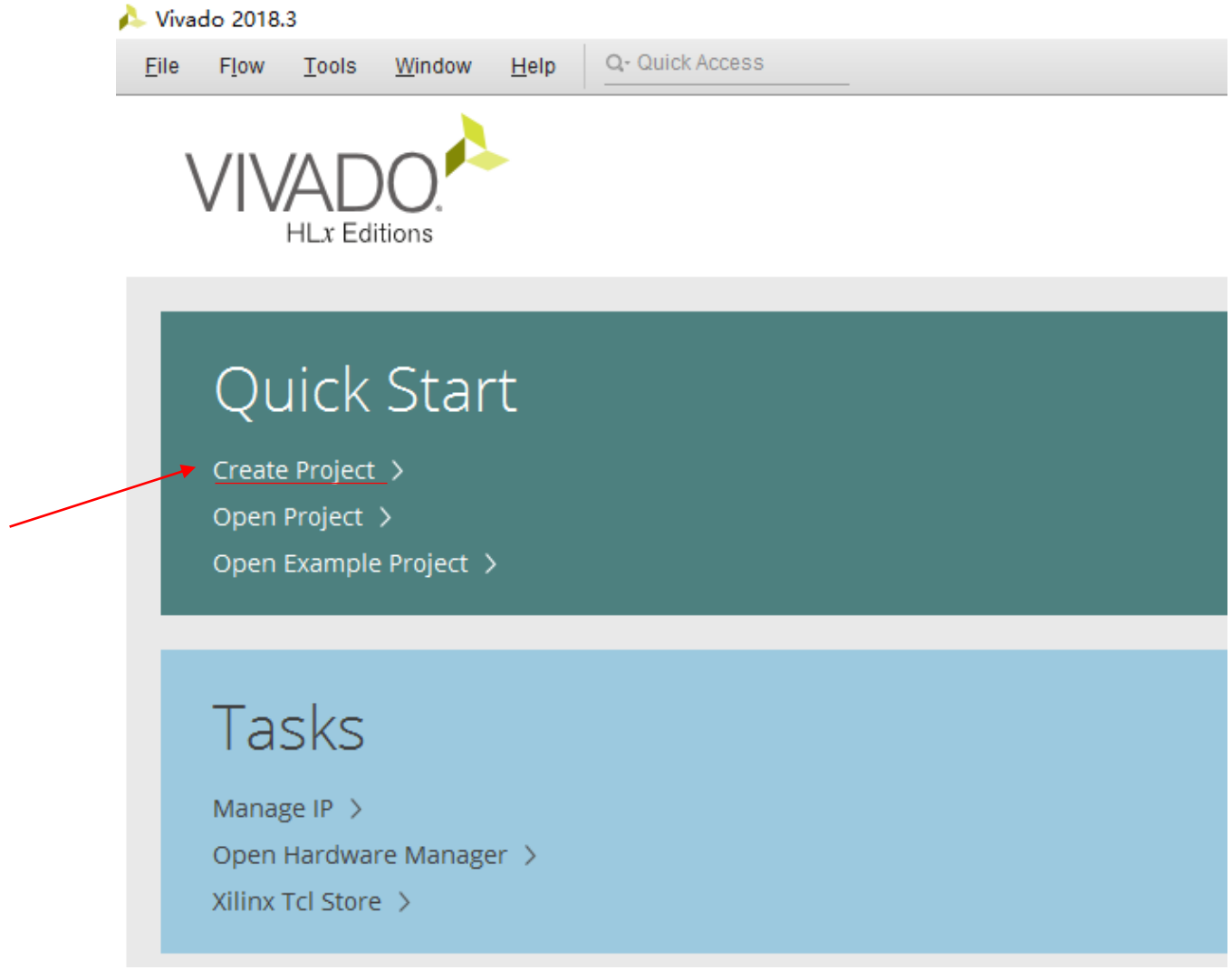
逻辑变量用BASYS-3实验板的两个开关输入，输出采用6个led灯。

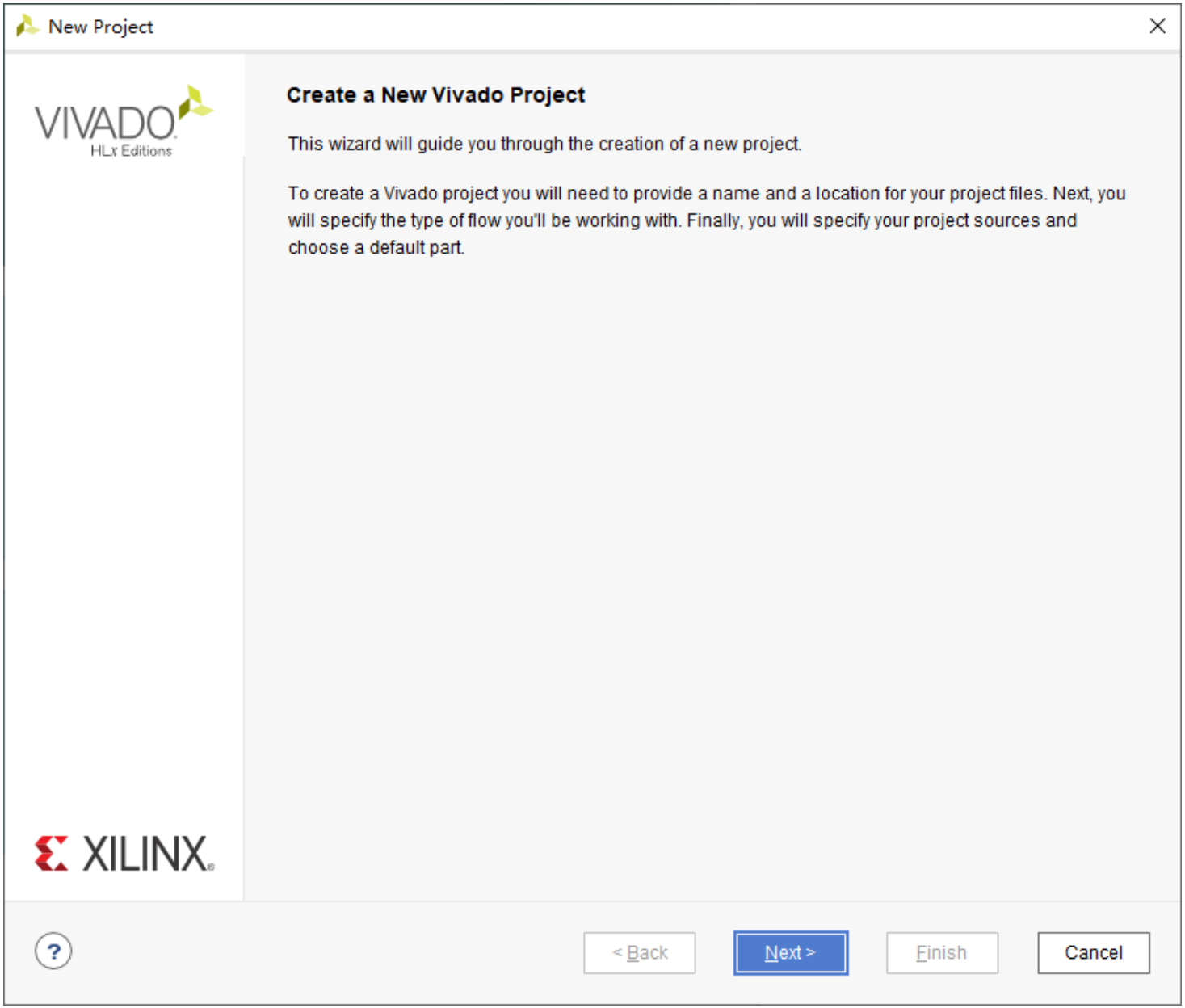
FPGA芯片：xc7a35tcpg236-1

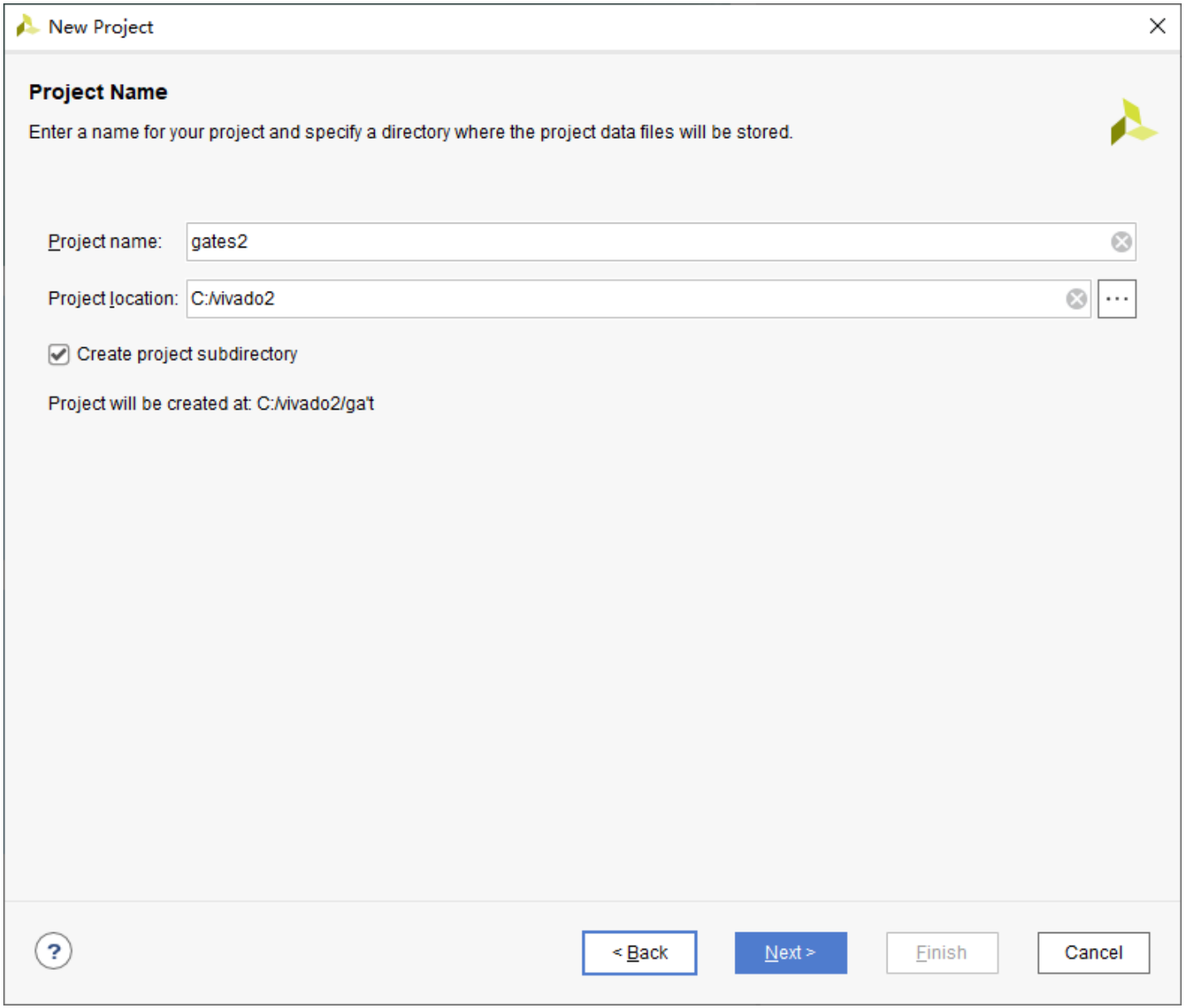
内容

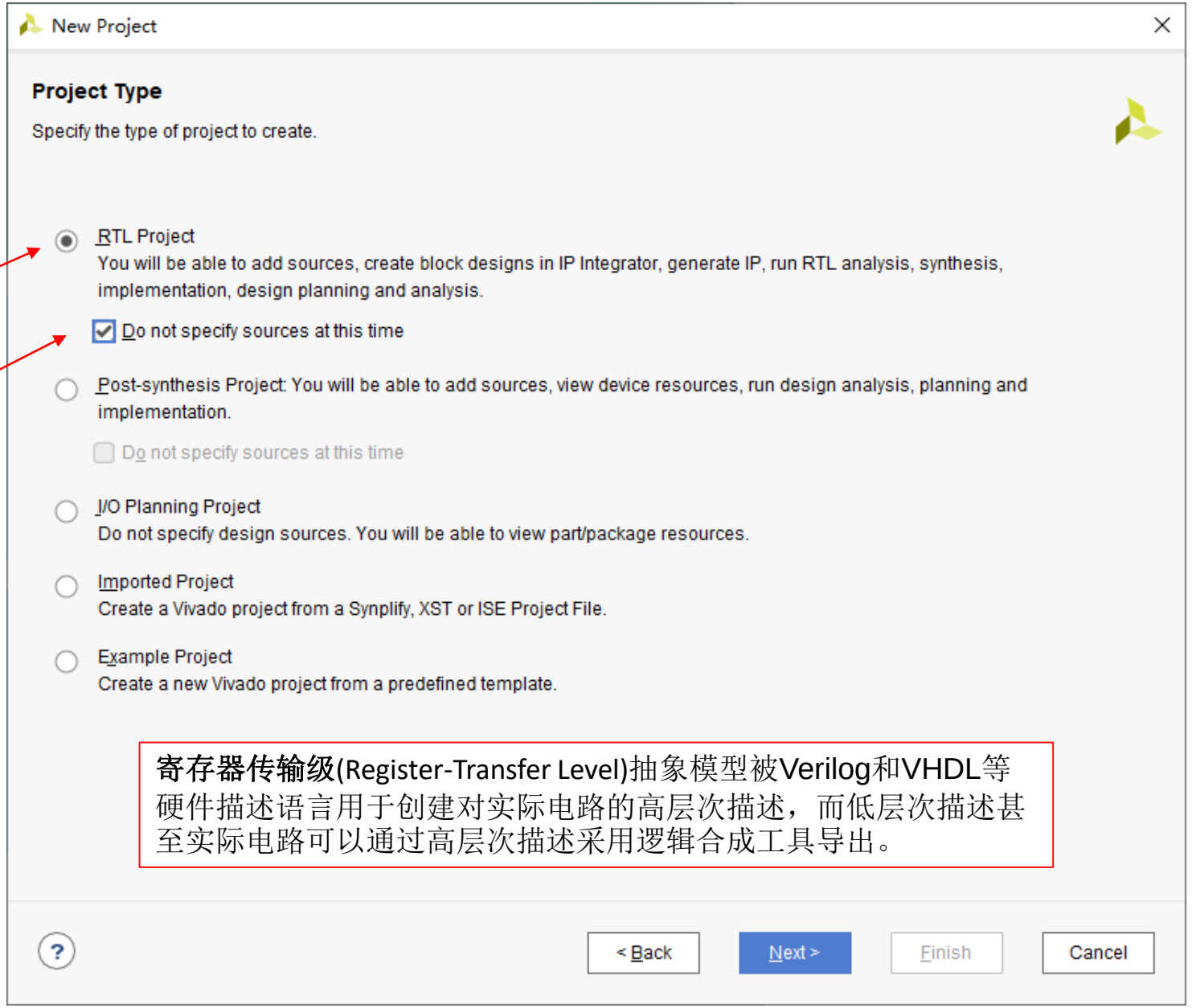
- 创建工程
- 添加设计源程序
- 仿真
- 综合
- 实现
- 约束
- 生成BitStream文件
- 下载
- 添加另一个设计源代码
- 查看FPGA芯片

创建工程

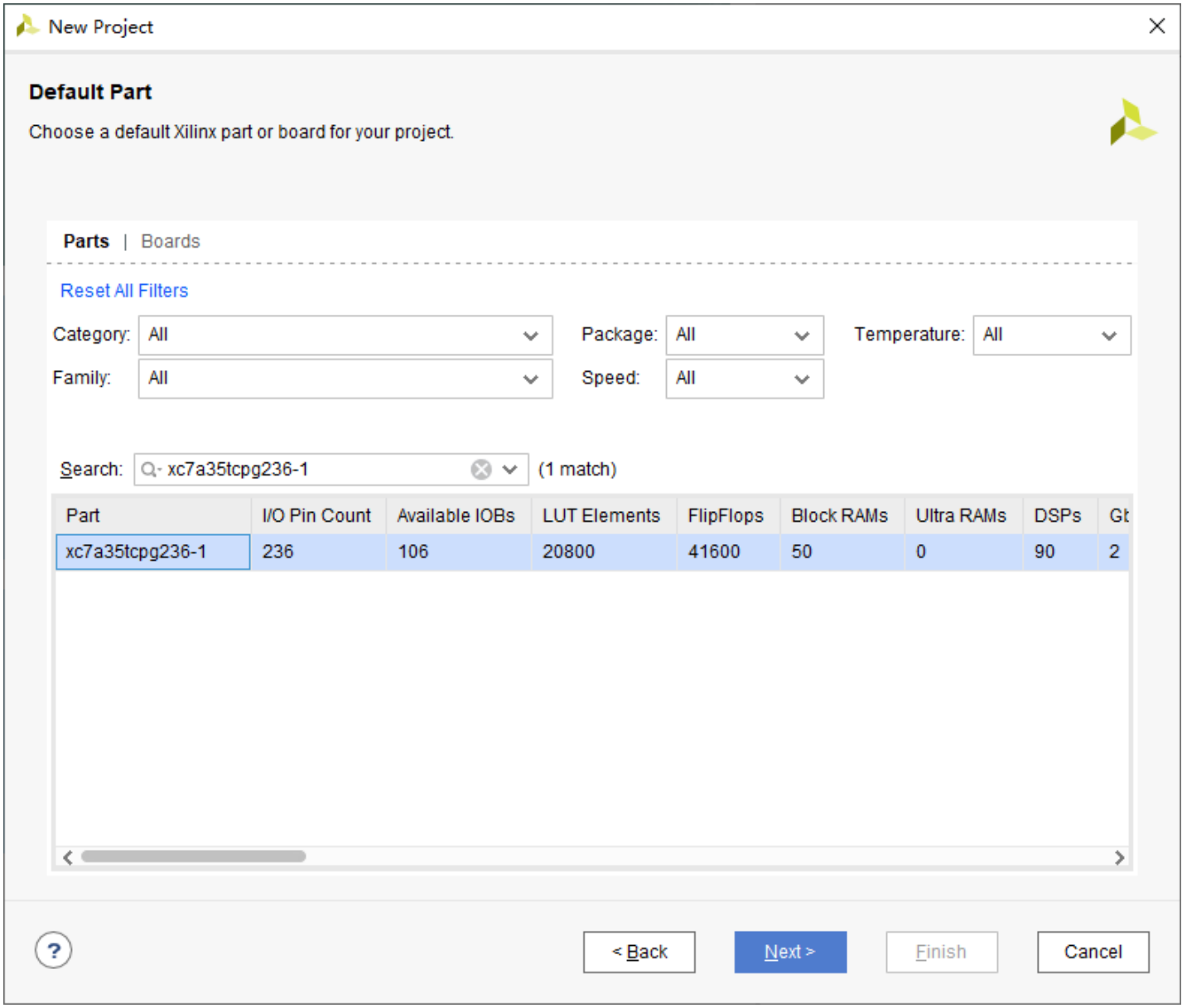

Vivado 2018.3
File
Flow
Tools
Window
Help
Quick Access
VIVADO
HLx Editions
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store

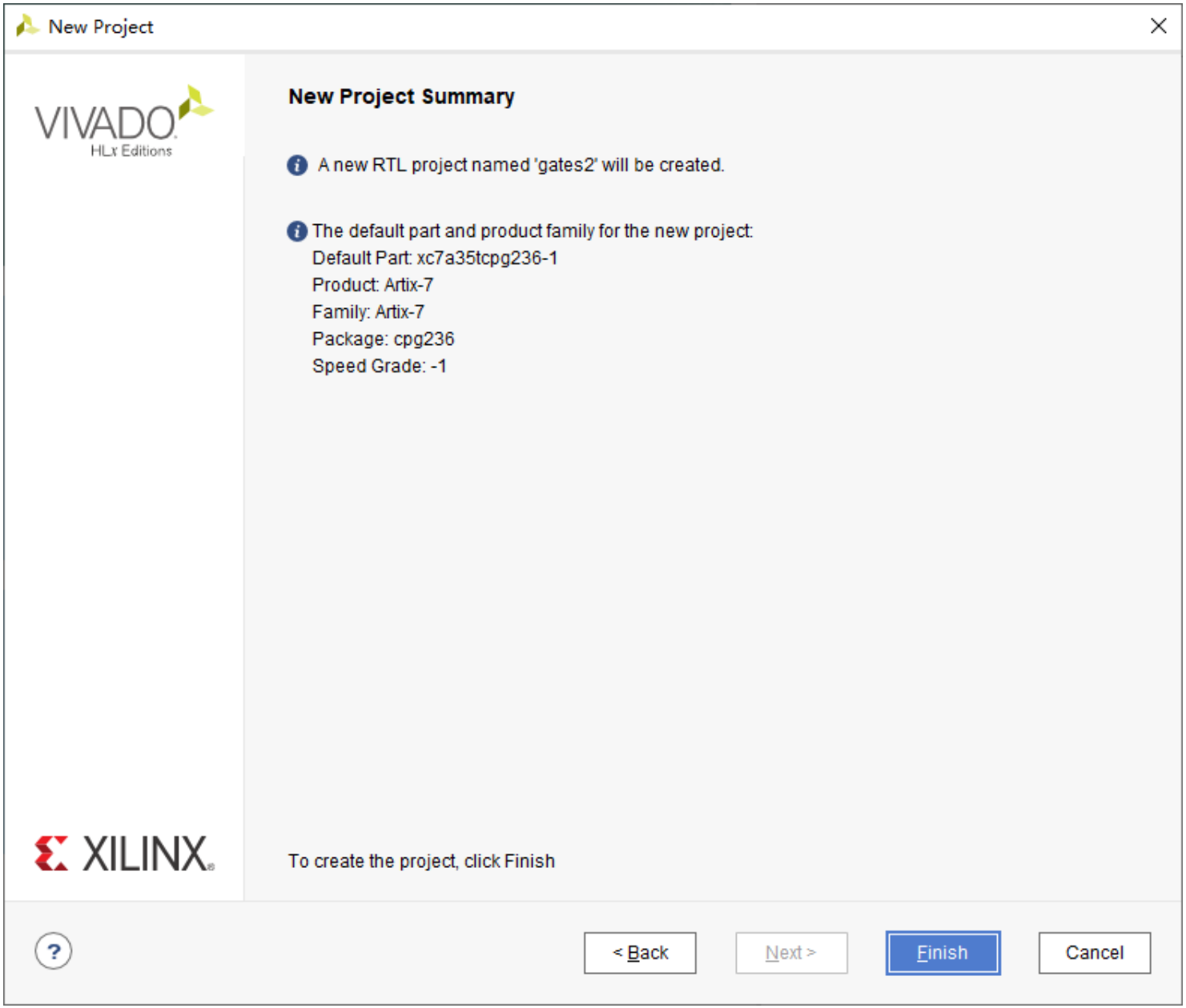

New Project
VIVADO
HLx Editions
Create a New Vivado Project
This wizard will guide you through the creation of a new project.
To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.
XILINX
?
< Back
Next >
Finish
Cancel


New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
gates2
Project location:
C:/vivado2
Create project subdirectory
Project will be created at: C:/vivado2/ga't
< Back
Next >
Finish
Cancel

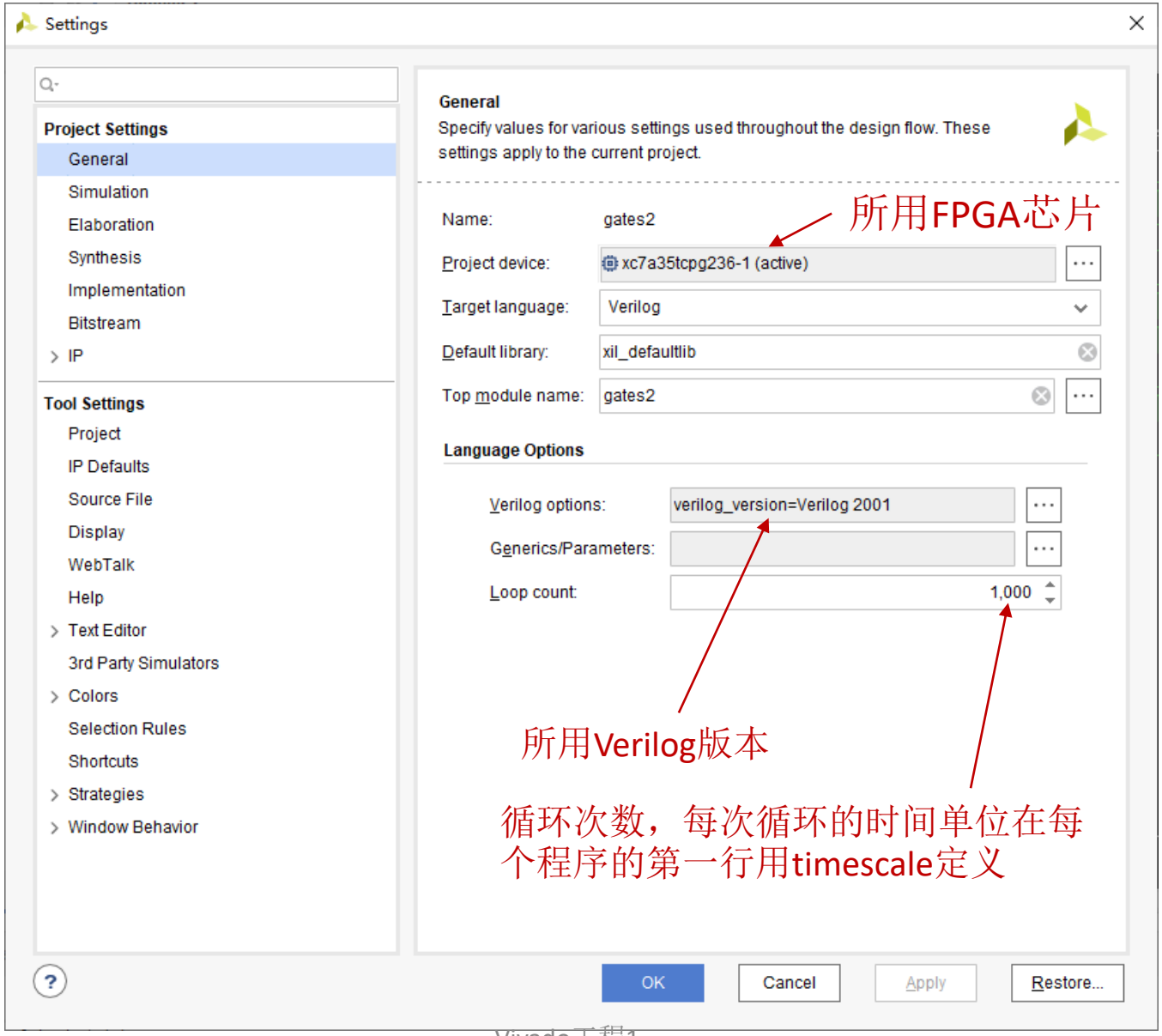

New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
寄存器传输级(Register-Transfer Level)抽象模型被Verilog和VHDL等硬件描述语言用于创建对实际电路的高层次描述，而低层次描述甚至实际电路可以通过高层次描述采用逻辑合成工具导出。
< Back
Next >
Finish
Cancel

选择FPGA芯片：xc7a35tcpg236-1

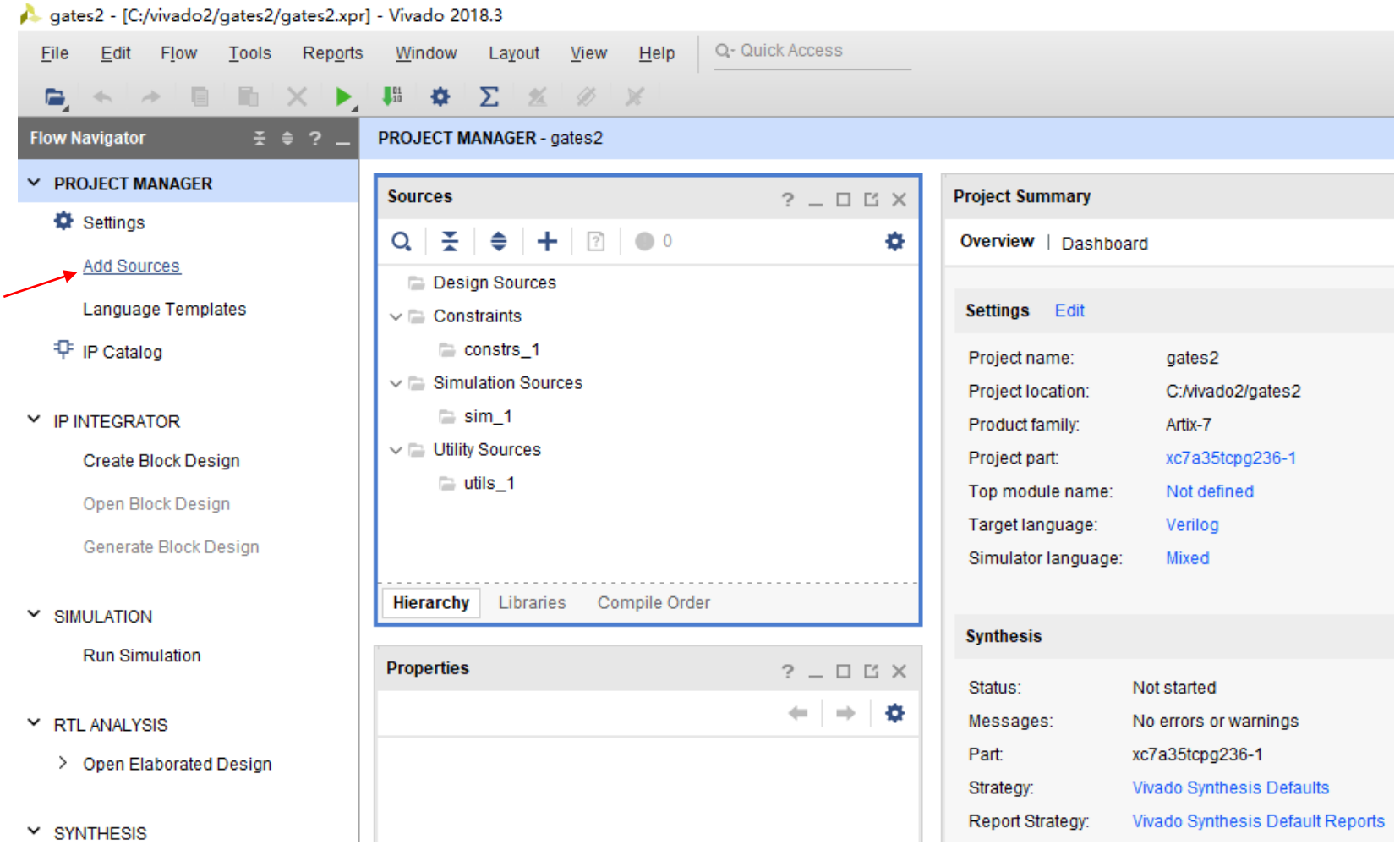


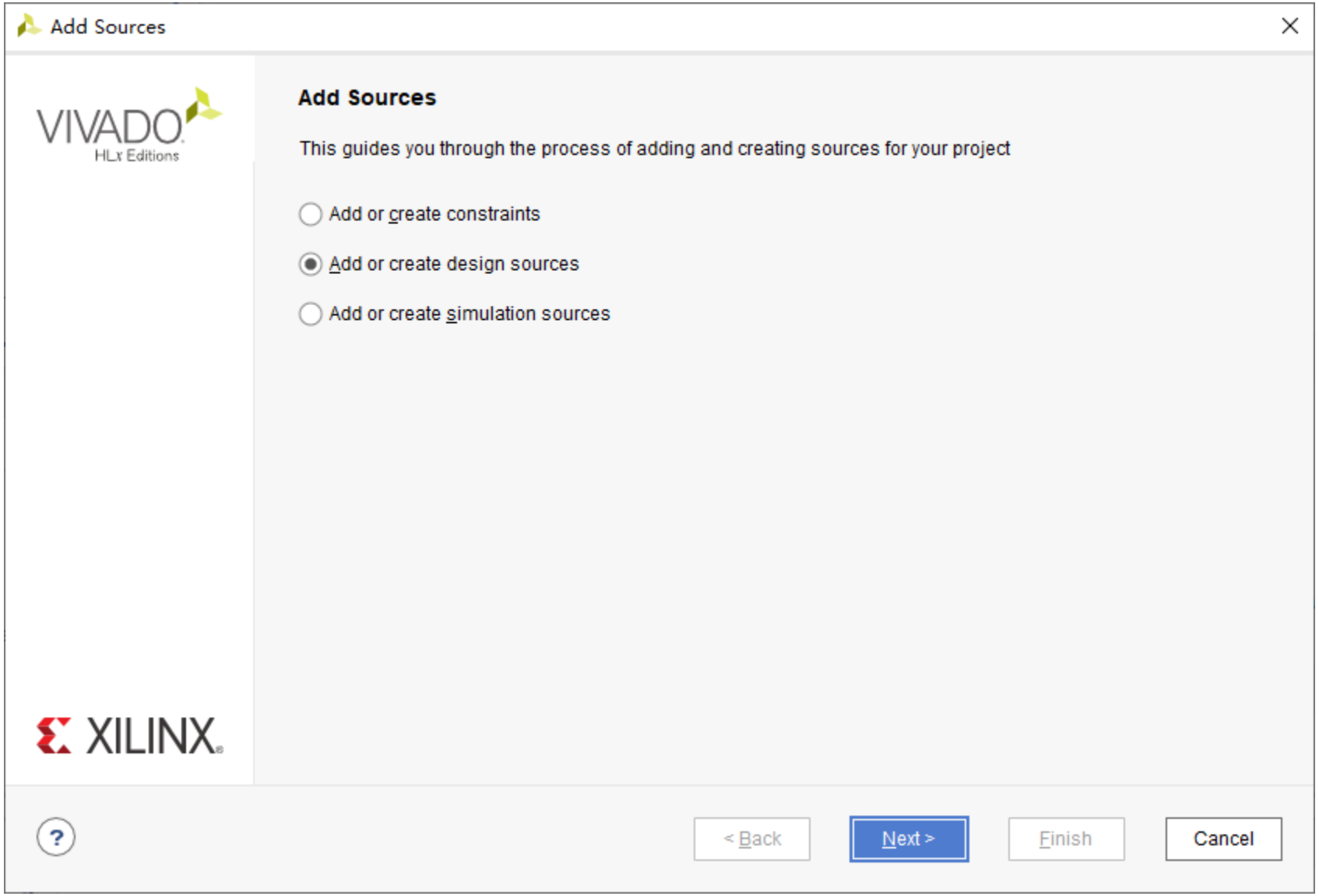

New Project
VIVADO
HLx Editions
New Project Summary
A new RTL project named 'gates2' will be created.
The default part and product family for the new project:
Default Part: xc7a35tcpg236-1
Product: Artix-7
Family: Artix-7
Package: cpg236
Speed Grade: -1
XILINX
To create the project, click Finish
< Back
Next >
Finish
Cancel

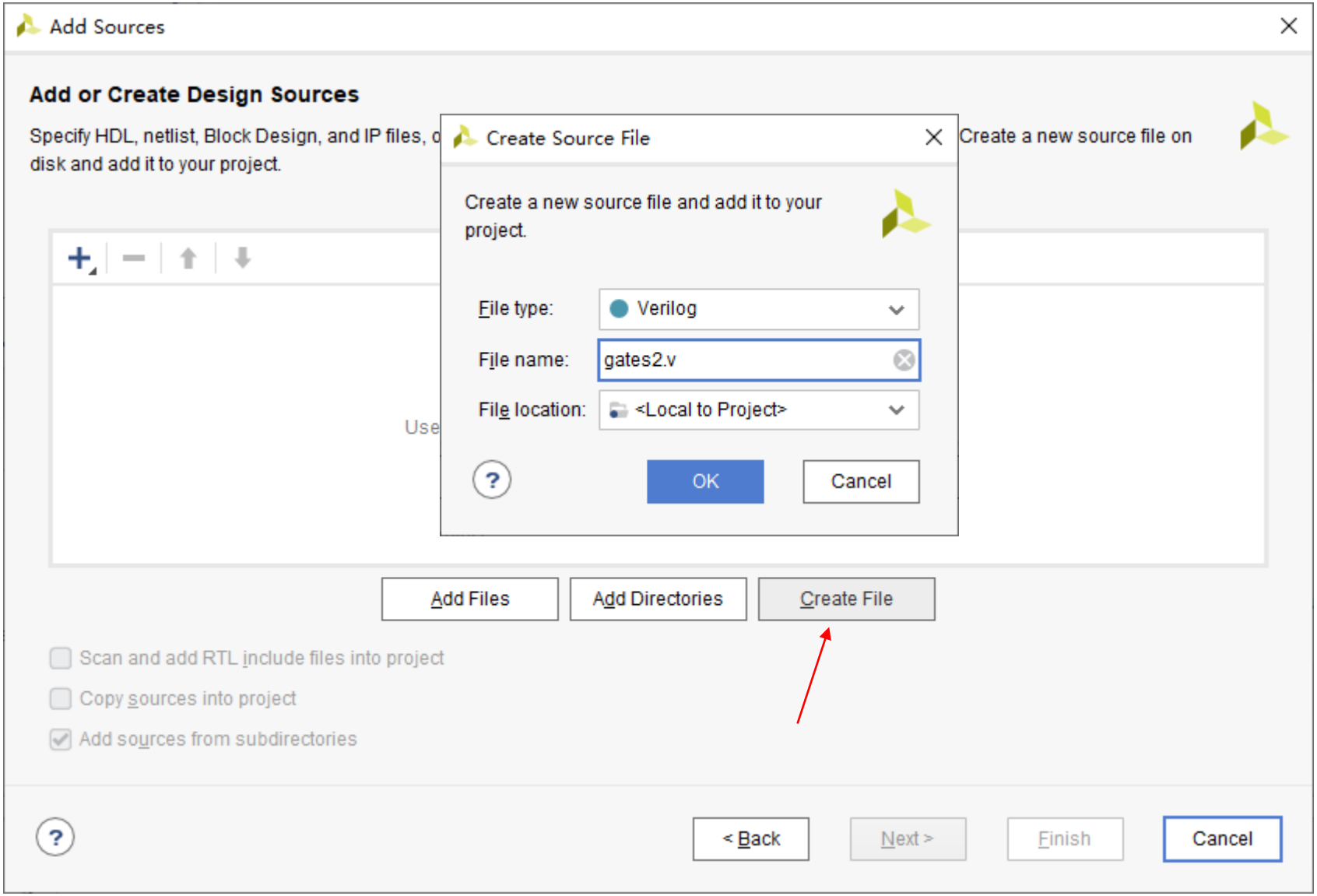
Tools/Settings 查看工程设置

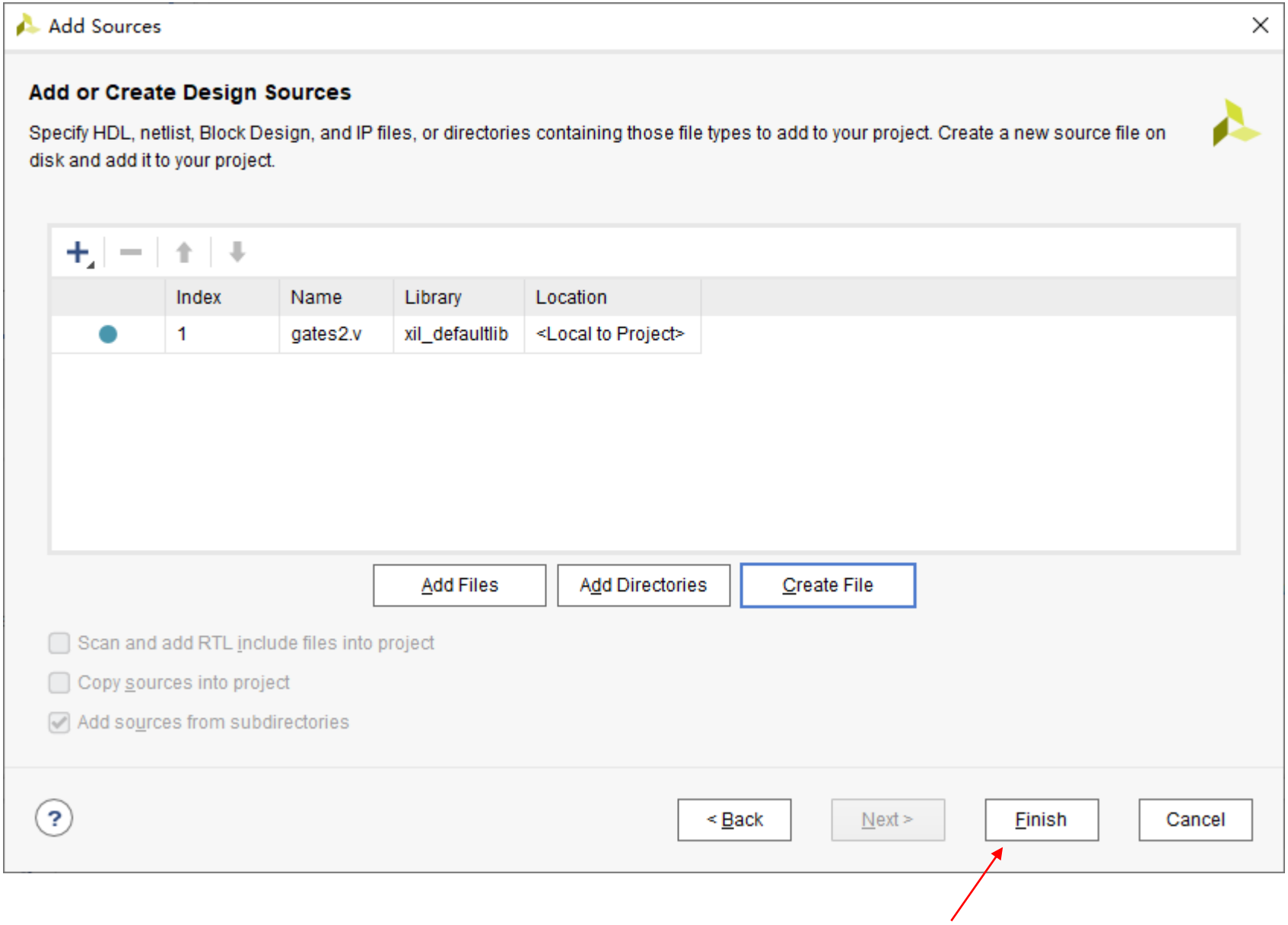


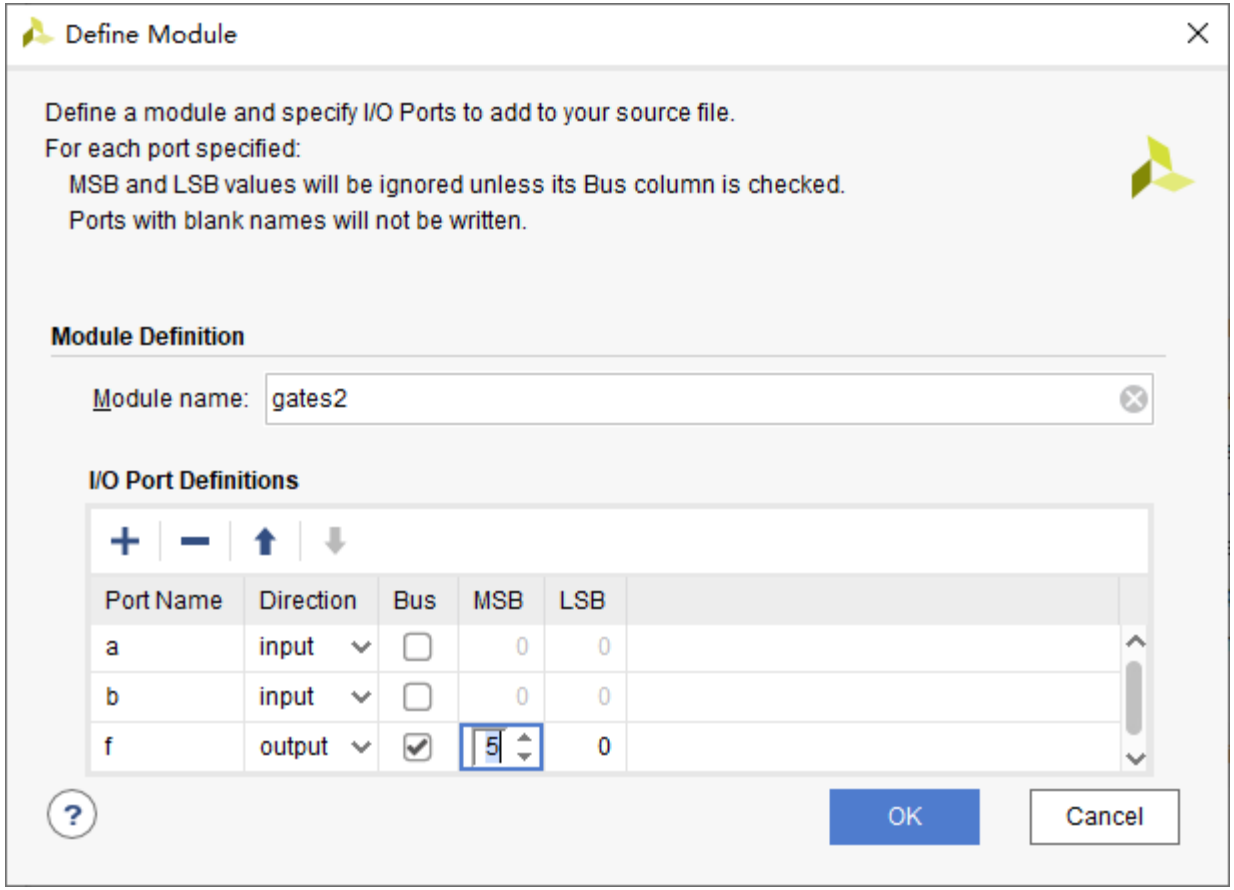
添加设计源代码

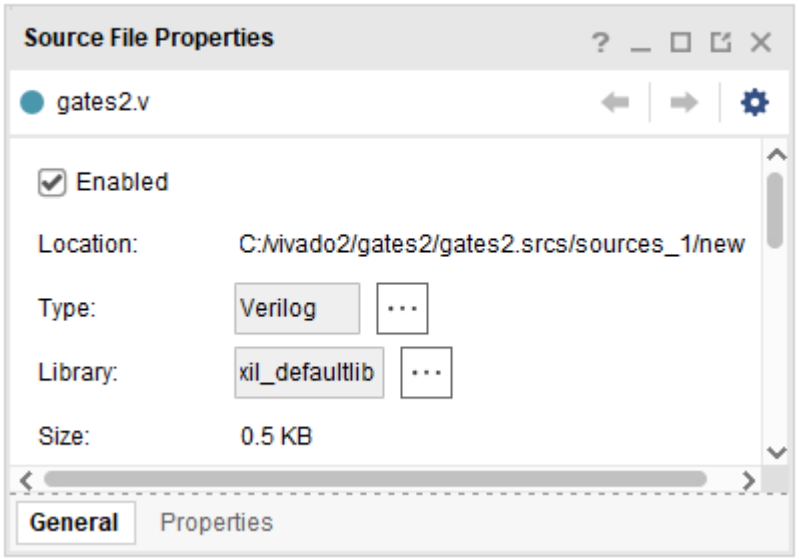

gates2 - [C:/vivado2/gates2/gates2.xpr] - Vivado 2018.3
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
PROJECT MANAGER - gates2
Sources
Design Sources
Constraints
constrs_1
Simulation Sources
sim_1
Utility Sources
utils_1
Hierarchy Libraries Compile Order
Properties
Project Summary
Overview | Dashboard
Settings Edit
Project name: gates2
Project location: C:/vivado2/gates2
Product family: Artix-7
Project part: xc7a35tcpg236-1
Top module name: Not defined
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Not started
Messages: No errors or warnings
Part: xc7a35tcpg236-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports

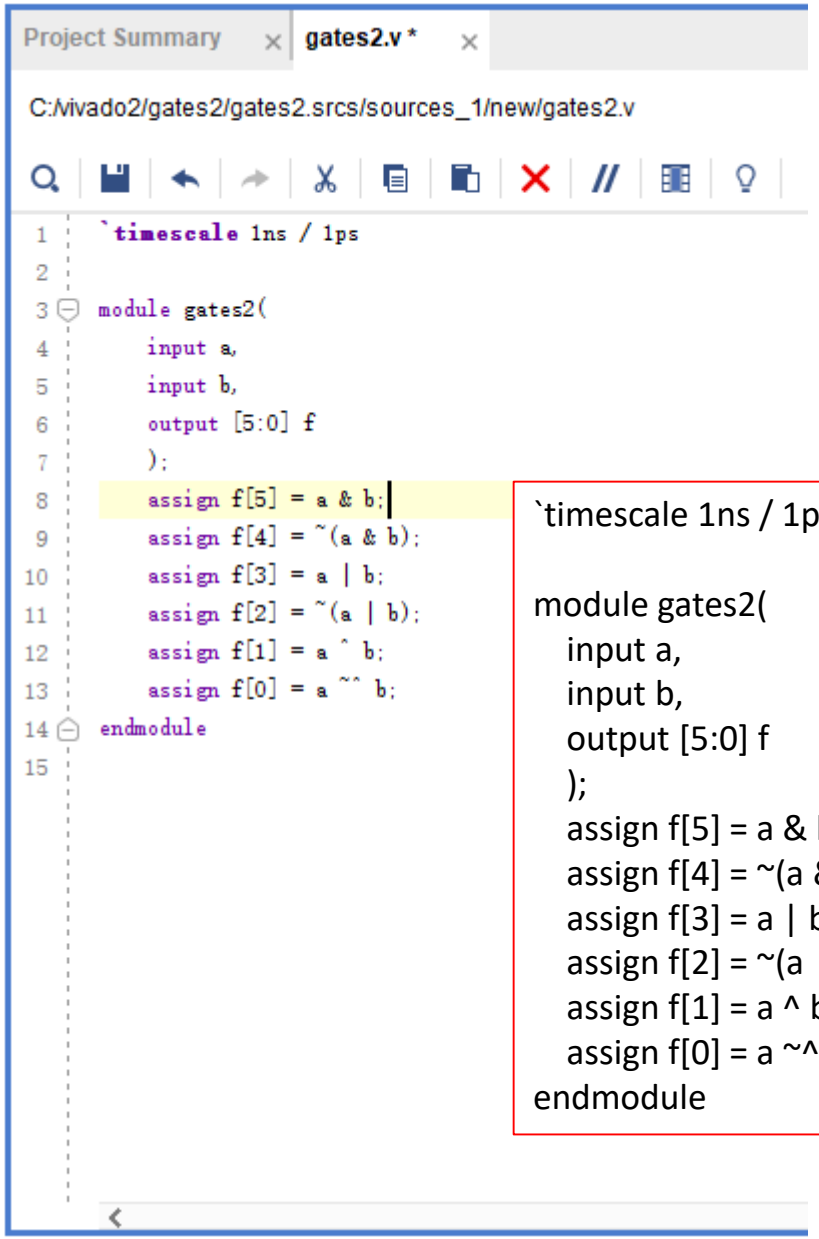

Add Sources
VIVADO
HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, o
disk and add it to your project.
Create a new source file on
Create Source File
Create a new source file and add it to your project.
File type:
Verilog
File name:
gates2.v
File location:
<Local to Project>
OK
Cancel
Use
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Index
Name
Library
Location
1
gates2.v
xil_defaultlib
<Local to Project>
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
< Back
Next >
Finish
Cancel


Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Module name: gates2
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
a
input
0
0
b
input
0
0
f
output
5
0
OK
Cancel





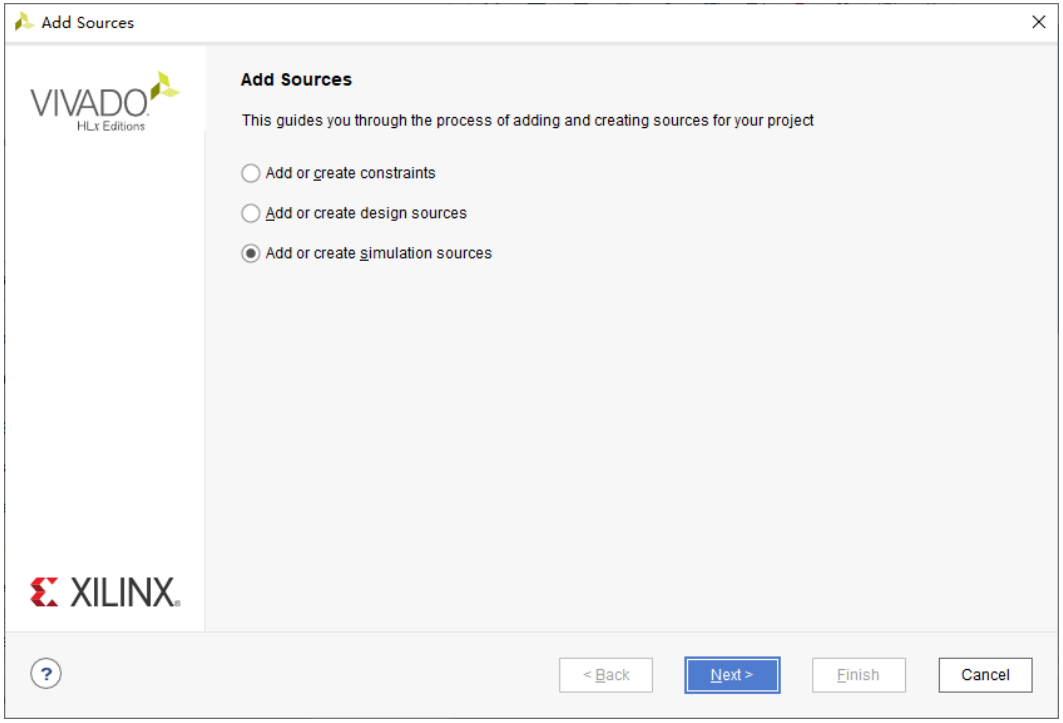

```
`timescale 1ns / 1ps

module gates2(
   input a,
   input b,
   output [5:0] f
   );
   assign f[5] = a & b;
   assign f[4] = ~(a & b);
   assign f[3] = a | b;
   assign f[2] = ~(a | b);
   assign f[1] = a ^ b;
   assign f[0] = a ~^ b;
endmodule
```

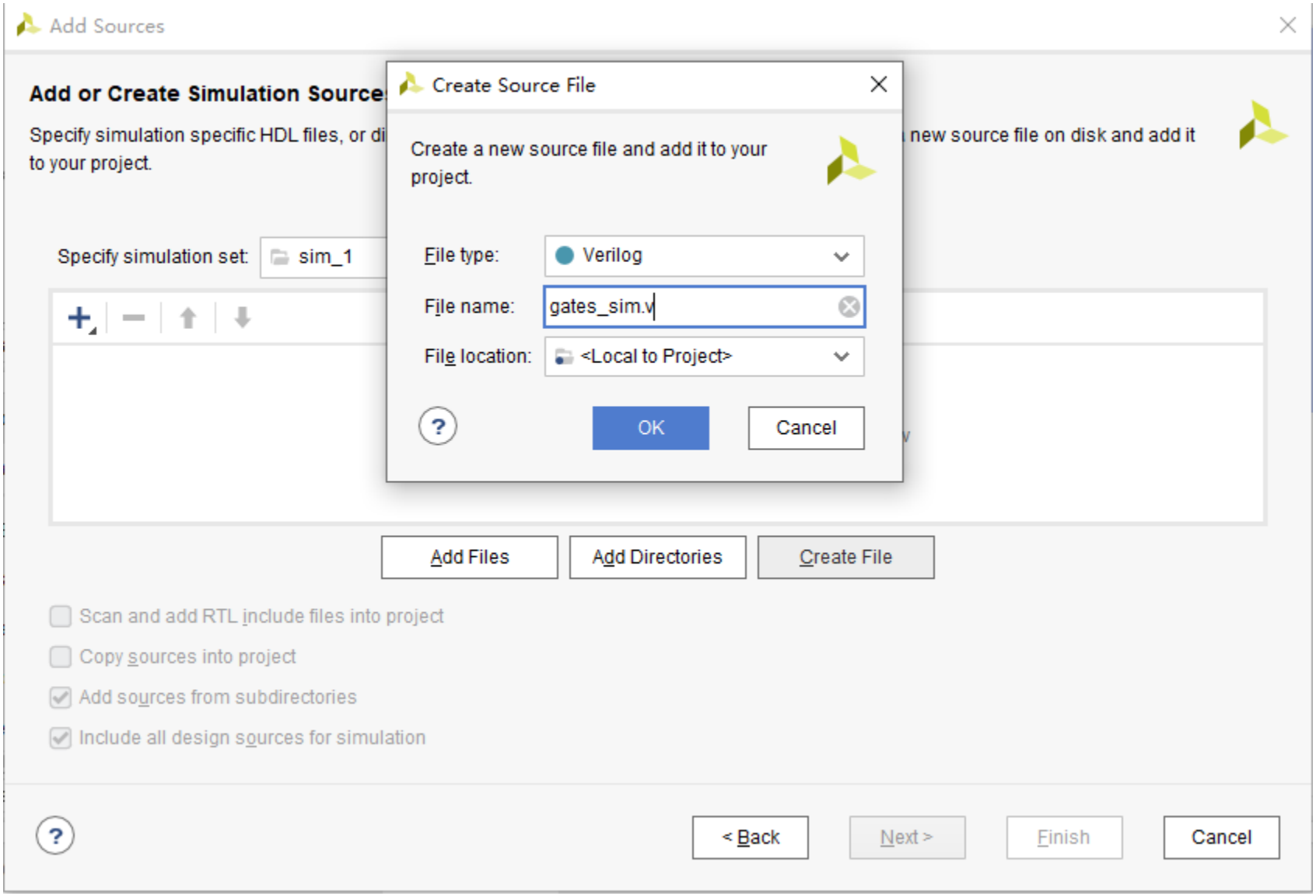
`timescale 1ns / 1ps 时间单位/精度

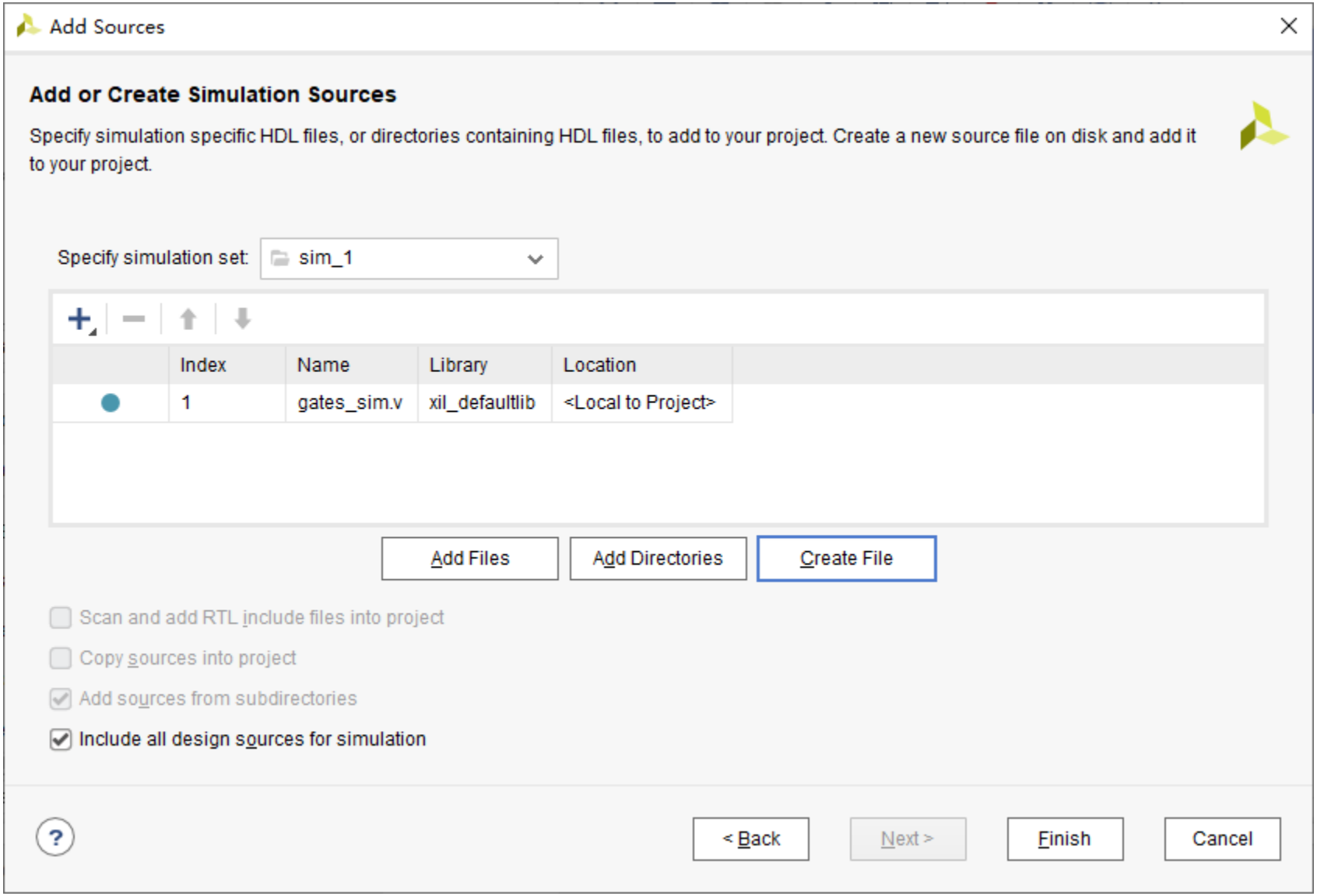
仿真

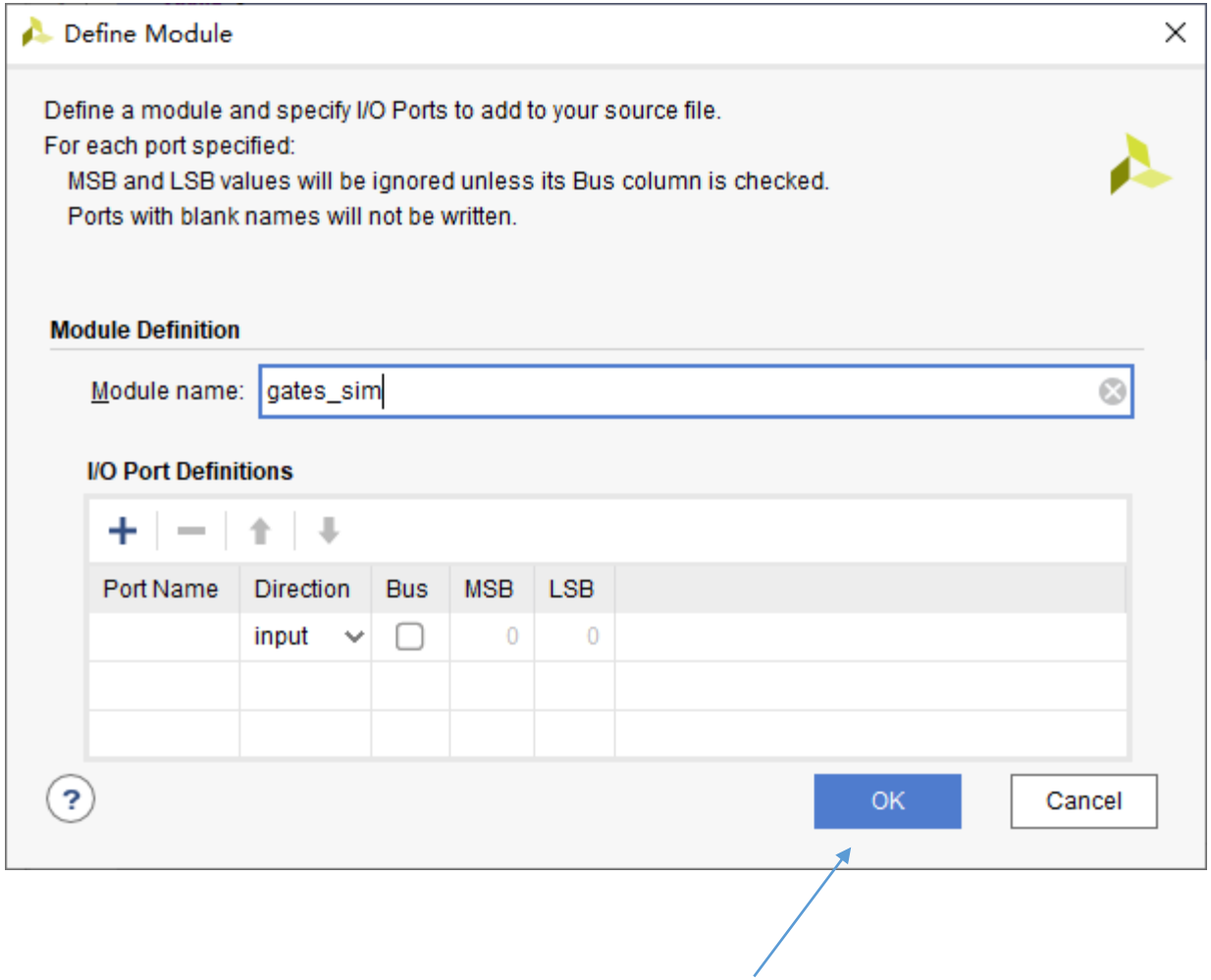
仿真主要用于测试设计模块，在仿真源程序的模块中应该通过调用设计模块来实现功能，当然，如果仿真模块也可以自己独立编程而不调用任何设计模块。仿真的结果图包含仿真模块输入和输出的电平关系。

创建仿真源代码



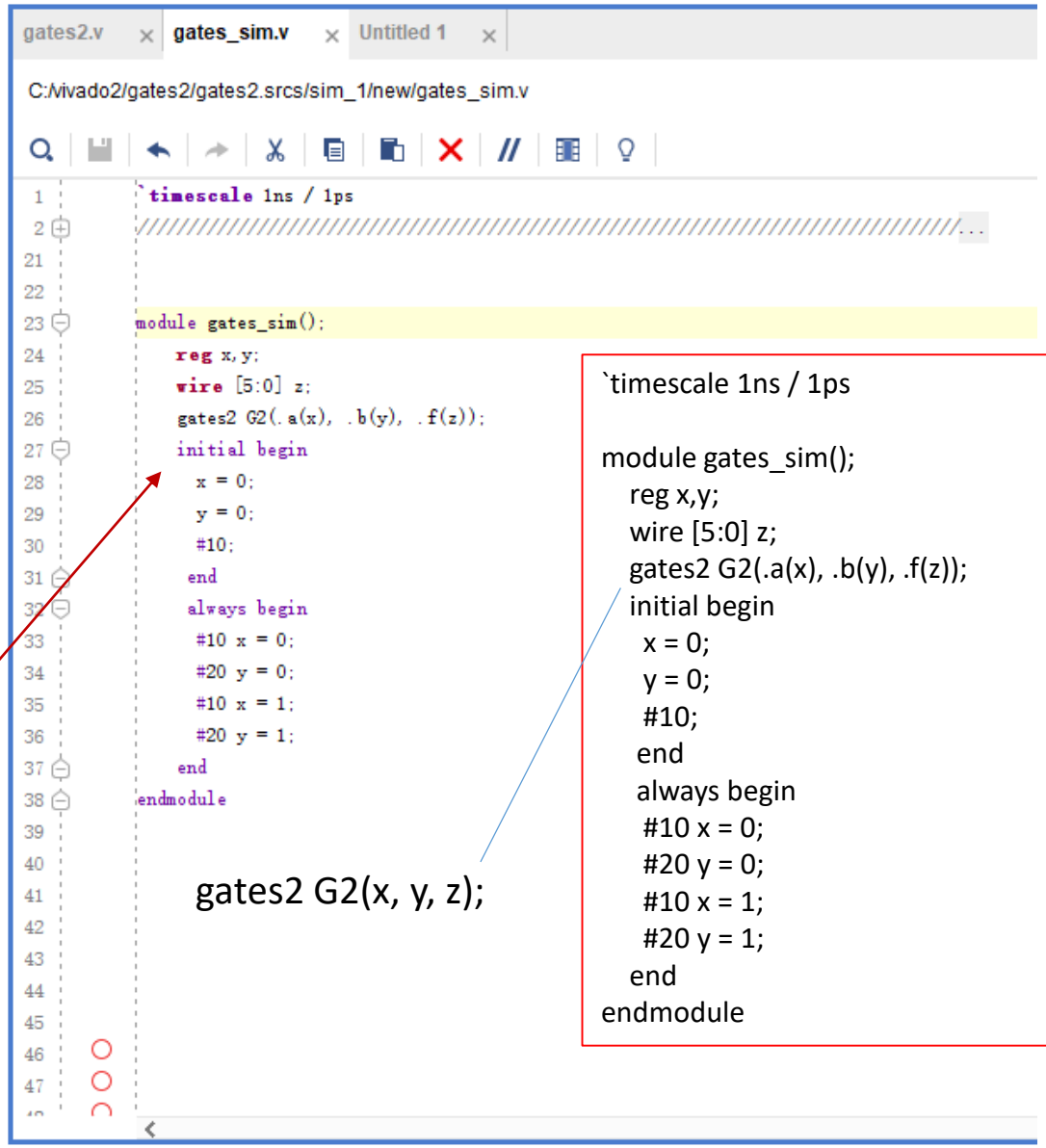

Add Sources
Add or Create Simulation Source
Specify simulation specific HDL files, or di
to your project.
new source file on disk and add it
Specify simulation set:
sim_1
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel
Create Source File
Create a new source file and add it to your project.
File type:
Verilog
File name:
gates_sim.v
File location:
<Local to Project>
OK
Cancel


Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.
Specify simulation set:
sim_1
Index
Name
Library
Location
1
gates_sim.v
xil_defaultlib
<Local to Project>
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel


Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Module name:
gates_sim
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
input
0
0
OK
Cancel

被调用的模块

下拉菜单：Set as Top



先执行initial再执行always

#表示过多少时间单位，再继续往下做

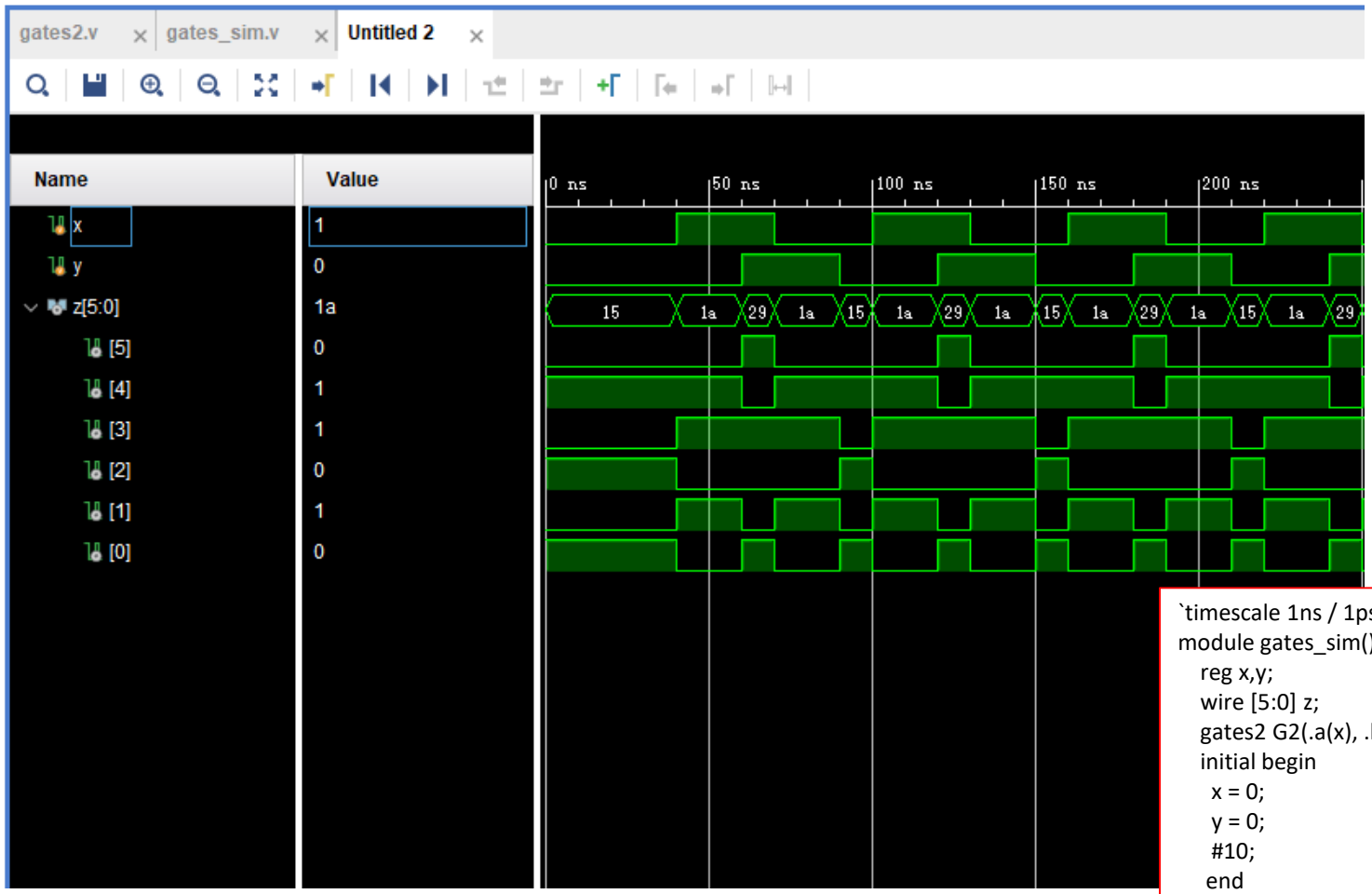
gates2 G2(x, y, z);

```
`timescale 1ns / 1ps

module gates_sim();
   reg x,y;
   wire [5:0] z;
   gates2 G2(.a(x), .b(y), .f(z));
   initial begin
     x = 0;
     y = 0;
     #10;
    end
    always begin
     #10 x = 0;
     #20 y = 0;
     #10 x = 1;
     #20 y = 1;
   end
endmodule
```

`timescale 1ns / 1ps　　时间单位/精度

进行仿真

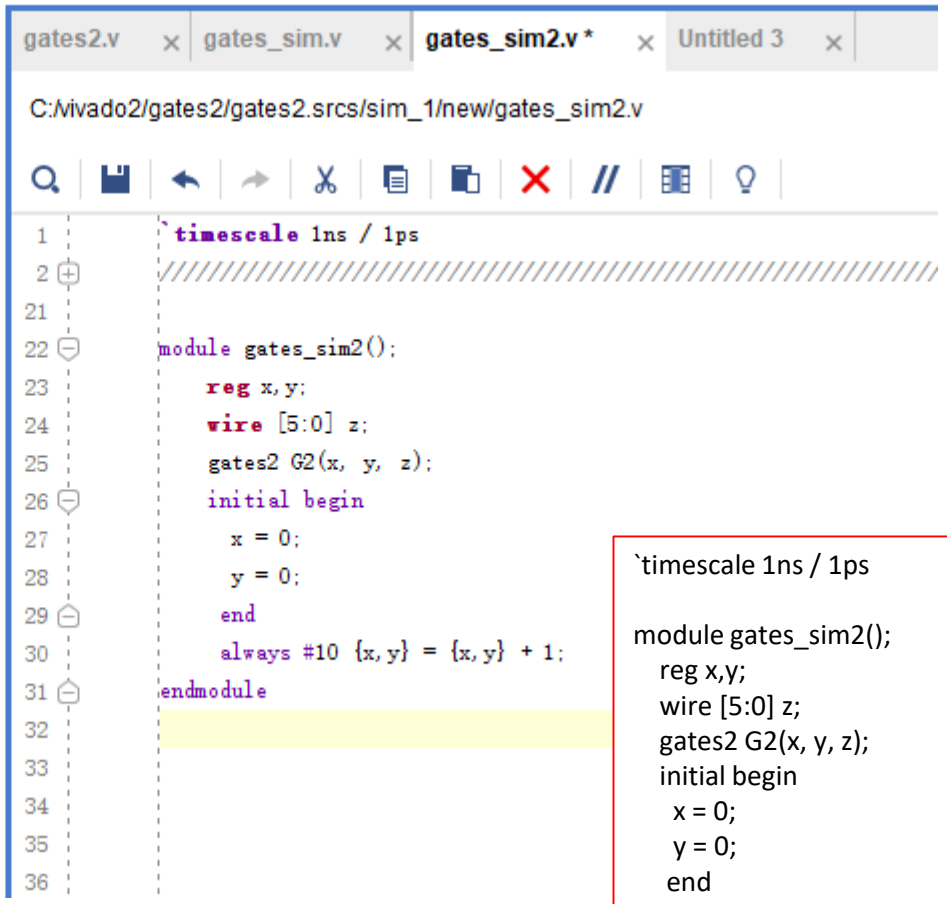
Simulation/Run Simulation/Run Behavioral Simulation：对仿真目录下的顶层模块进行仿真。




```
`timescale 1ns / 1ps
module gates_sim();
   reg x,y;
   wire [5:0] z;
   gates2 G2(.a(x), .b(y), .f(z));
   initial begin
    x = 0;
    y = 0;
    #10;
   end
   always begin
    #10 x = 0;
    #20 y = 0;
    #10 x = 1;
    #20 y = 1;
   end
endmodule
```

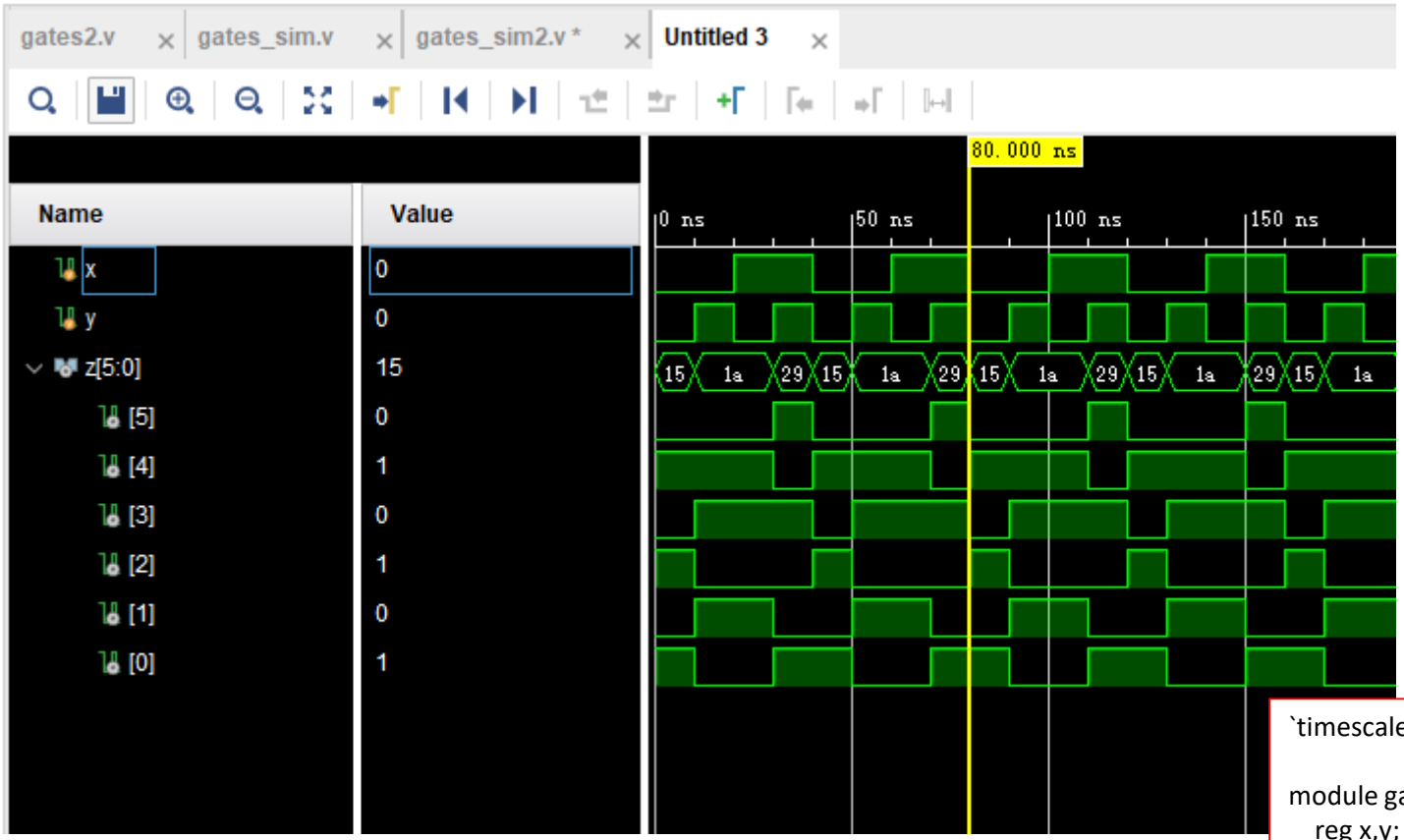
当有多个模拟源代码时，模拟程序会选择模拟目录中设置为Top的源码进行模拟。

创建另一个仿真源程序，要设置为顶层模块




```
`timescale 1ns / 1ps

module gates_sim2();
   reg x,y;
   wire [5:0] z;
   gates2 G2(x, y, z);
   initial begin
    x = 0;
    y = 0;
   end
   always #10 {x,y} = {x,y} + 1;
endmodule
```

仿真：Simulation/Run Simulation/Run Behavioral Simulation



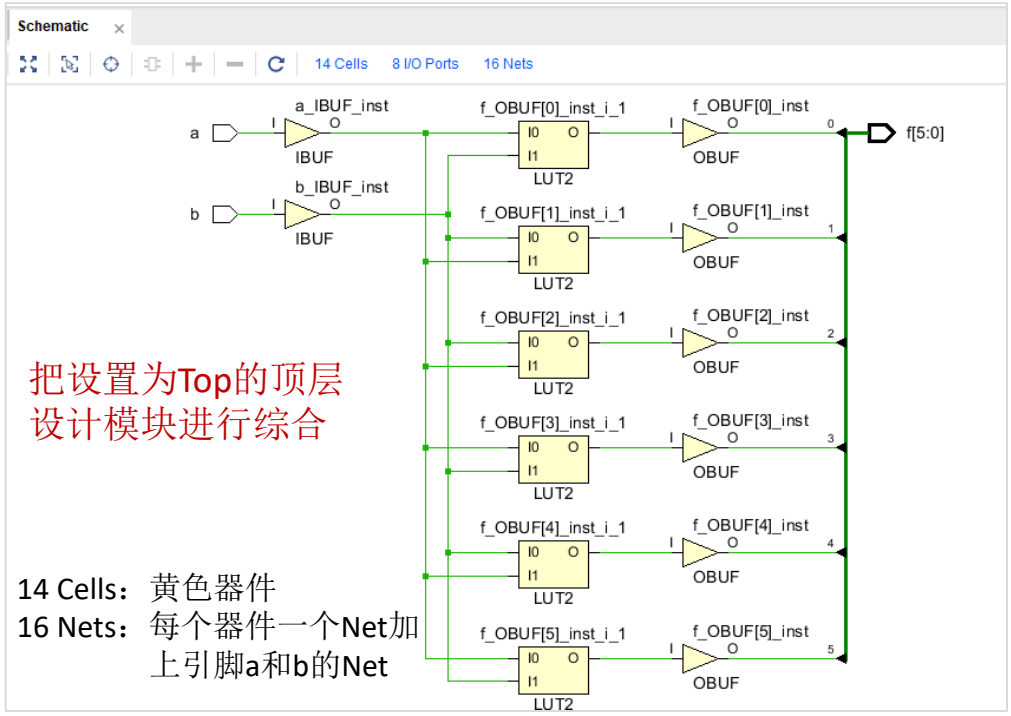

```
`timescale 1ns / 1ps

module gates_sim2();
   reg x,y;
   wire [5:0] z;
   gates2 G2(x, y, z);
   initial begin
     x = 0;
     y = 0;
    end
    always #10 {x,y} = {x,y} + 1;
endmodule
```

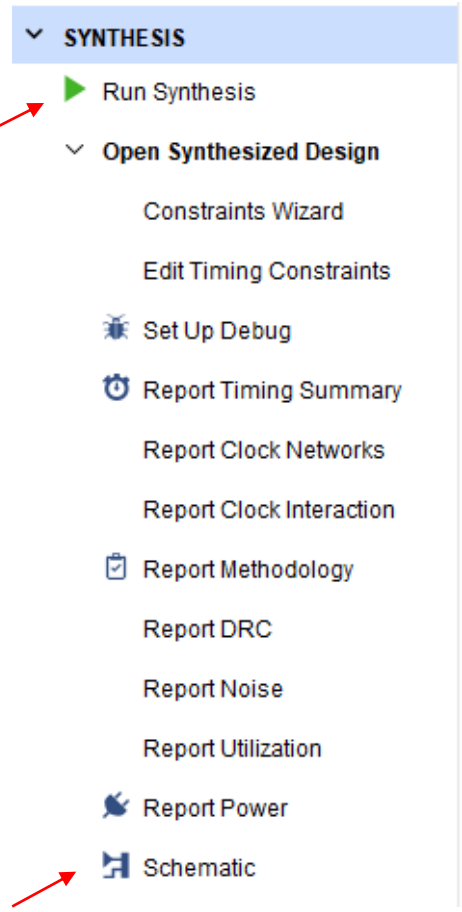
对顶层仿真模块进行仿真

综合(Synthesis)

综合是一个类似编译的过程，把RTL级别的设计描述转化成门级和触发器等基本逻辑单元的互连关系，Vivado会把顶层模块转换成所用FPGA芯片的设计描述。

(1) SYNTHESIS/Run Synthesis
(2) Open Synthesized Design/Schematic

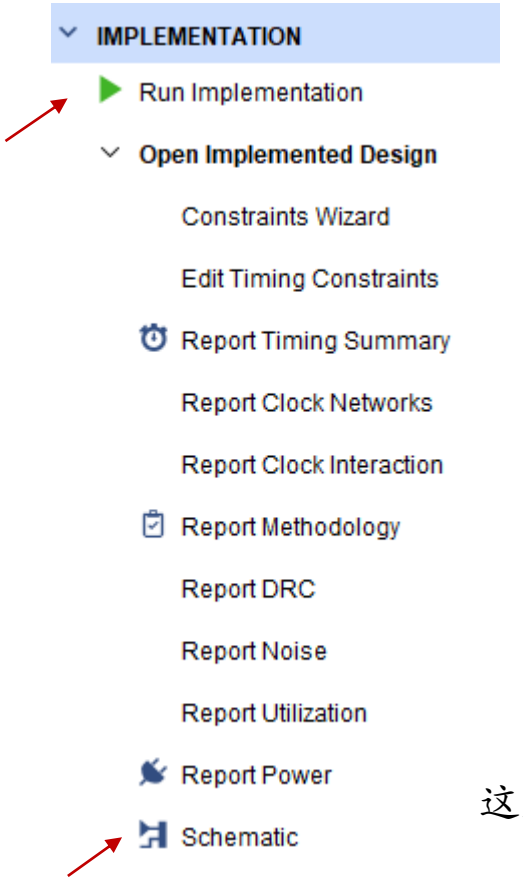




综合时间较长，可以在菜单中选择Window/ Design Runs可查看综合进度

实现(Implementation)

实现把综合后得到芯片内部器件之间的虚拟连接进行实际的布局布线，得到一个具体的设计。

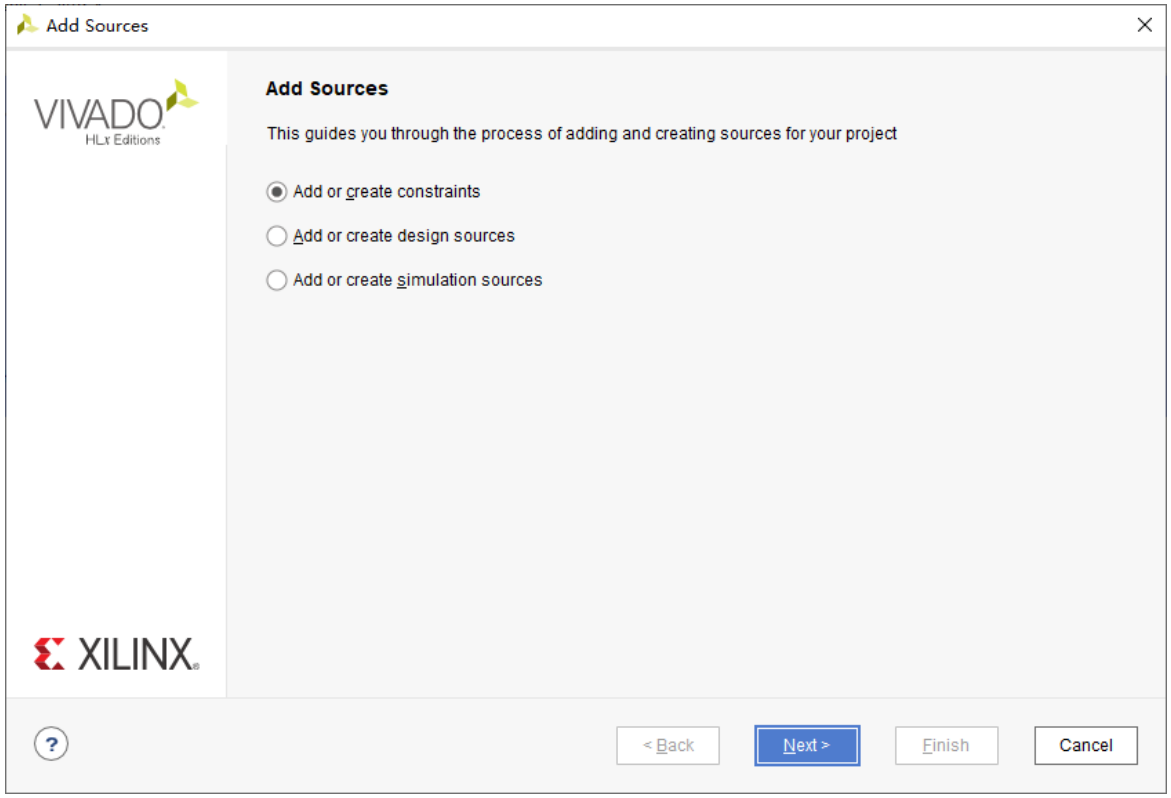


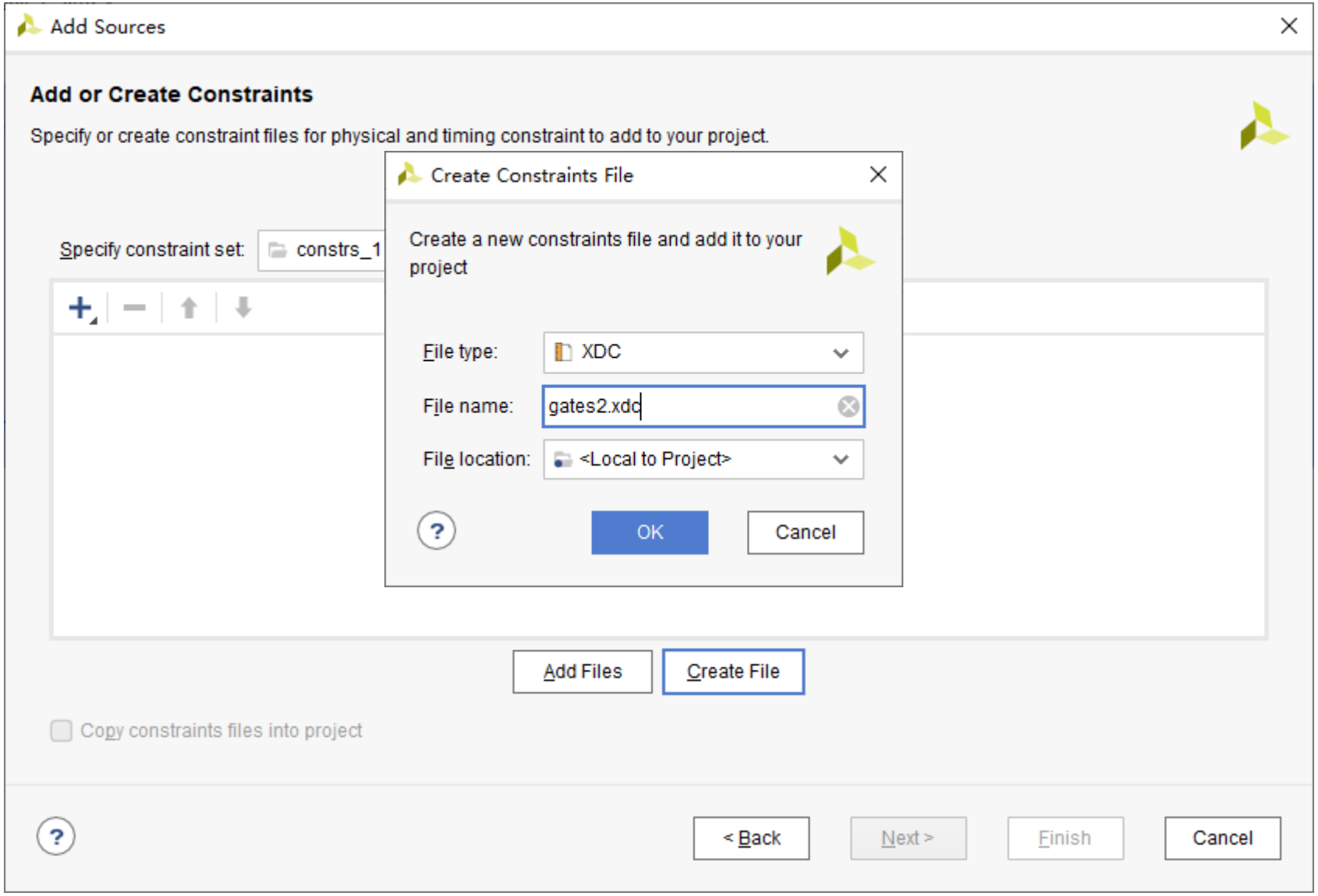
这里的Schematic图与综合的Schematic图相同

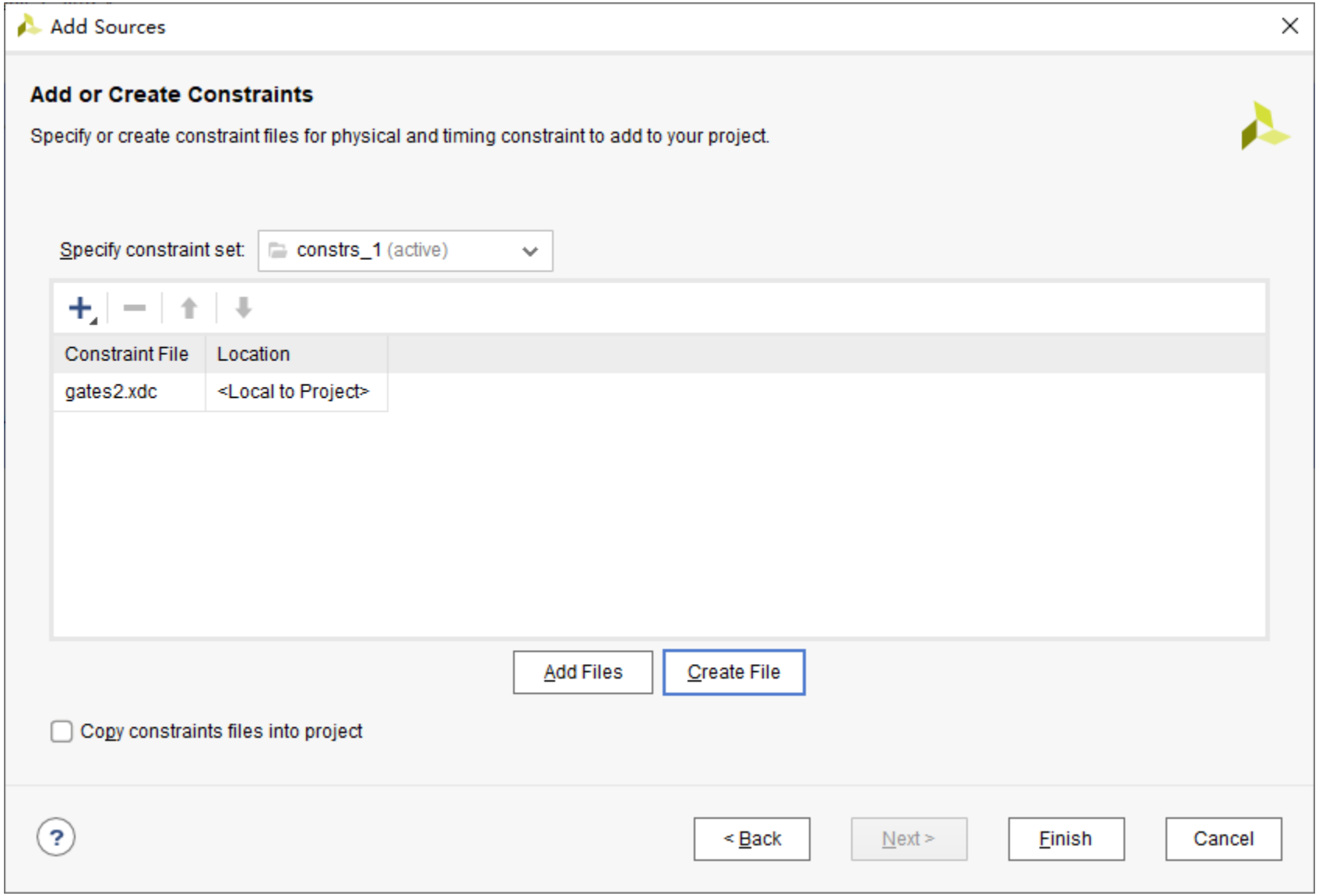
约束(Constraint)

约束用于把模块的输入输出参数映射到FPGA芯片引脚。

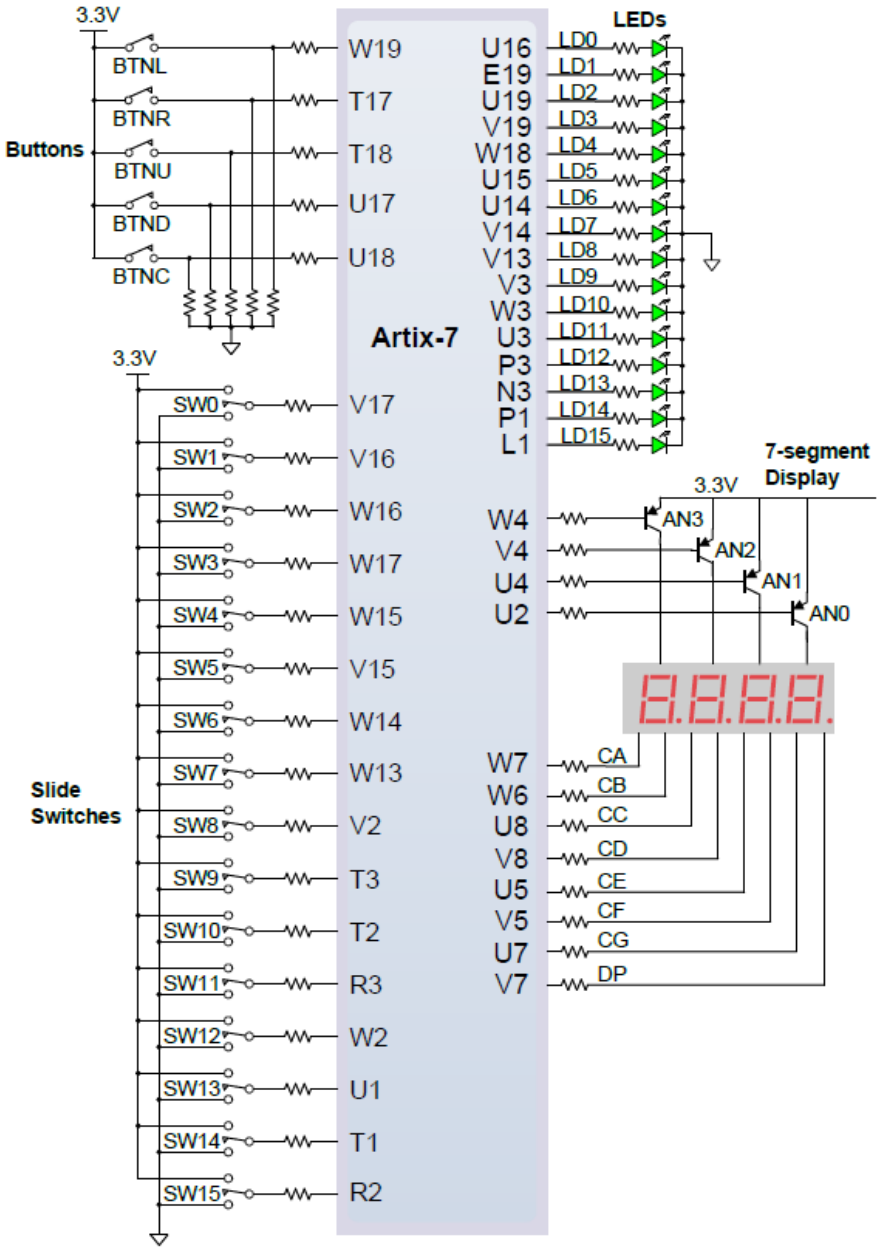
创建约束文件

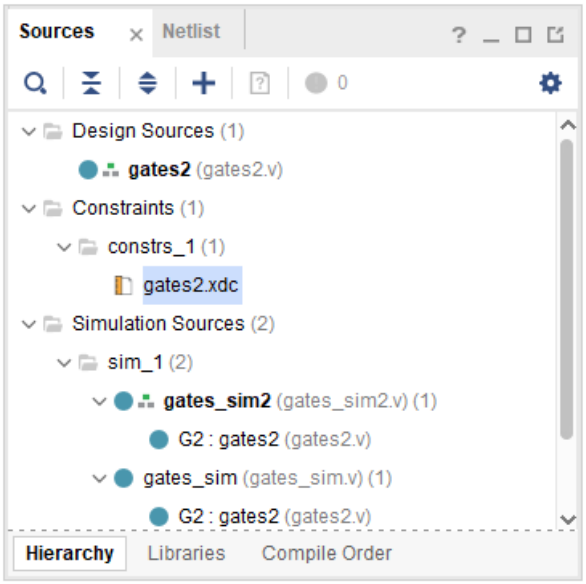


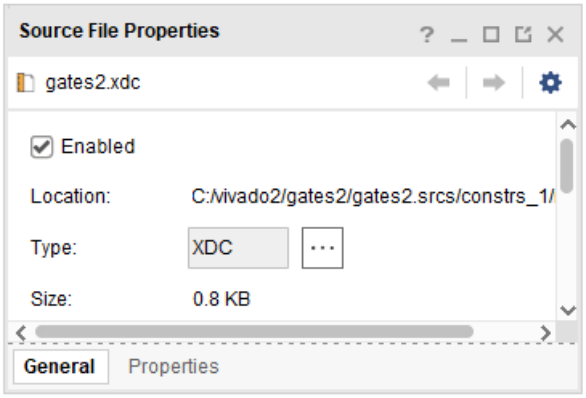

Add Sources
Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1
Create Constraints File
Create a new constraints file and add it to your project
File type:
XDC
File name:
gates2.xdc
File location:
<Local to Project>
OK
Cancel
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

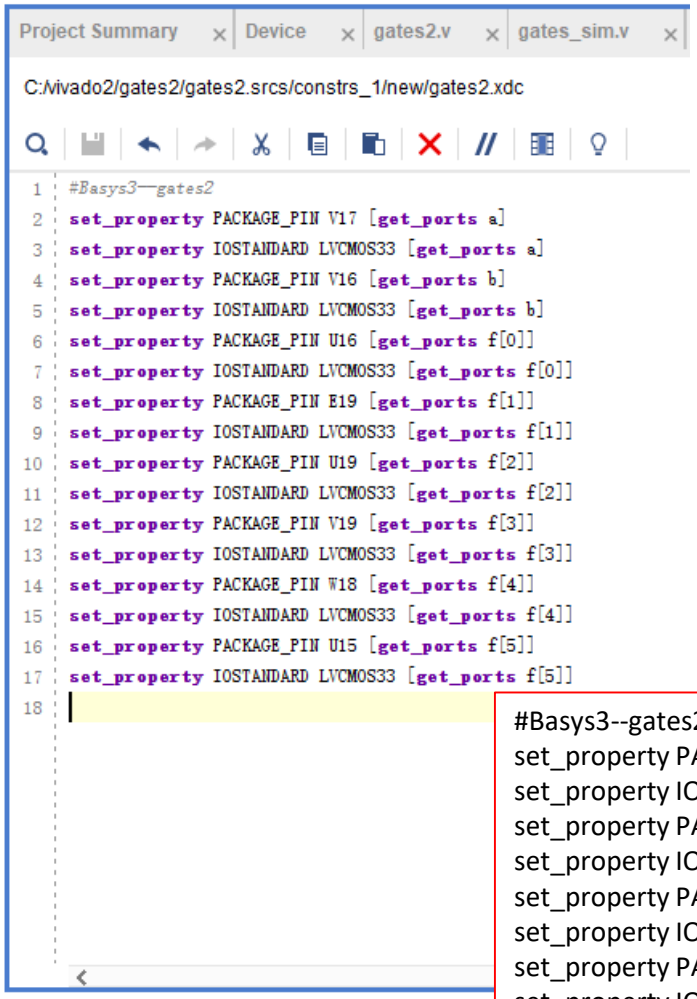

Add Sources
Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1 (active)
Constraint File
Location
gates2.xdc
<Local to Project>
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

FPGA芯片
xc7a35tcpg236-1的引脚





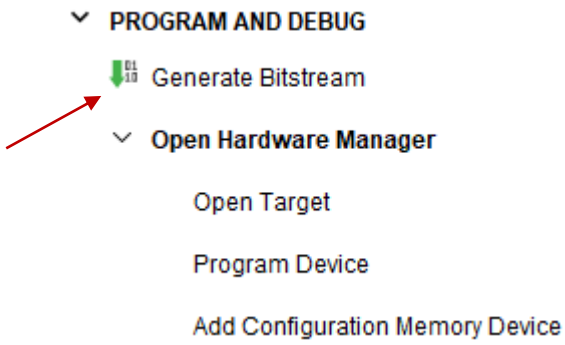





```
#Basys3--gates2
set_property PACKAGE_PIN V17 [get_ports a]
set_property IOSTANDARD LVCMOS33 [get_ports a]
set_property PACKAGE_PIN V16 [get_ports b]
set_property IOSTANDARD LVCMOS33 [get_ports b]
set_property PACKAGE_PIN U16 [get_ports f[0]]
set_property IOSTANDARD LVCMOS33 [get_ports f[0]]
set_property PACKAGE_PIN E19 [get_ports f[1]]
set_property IOSTANDARD LVCMOS33 [get_ports f[1]]
set_property PACKAGE_PIN U19 [get_ports f[2]]
set_property IOSTANDARD LVCMOS33 [get_ports f[2]]
set_property PACKAGE_PIN V19 [get_ports f[3]]
set_property IOSTANDARD LVCMOS33 [get_ports f[3]]
set_property PACKAGE_PIN W18 [get_ports f[4]]
set_property IOSTANDARD LVCMOS33 [get_ports f[4]]
set_property PACKAGE_PIN U15 [get_ports f[5]]
set_property IOSTANDARD LVCMOS33 [get_ports f[5]]
```

生成BitStream文件

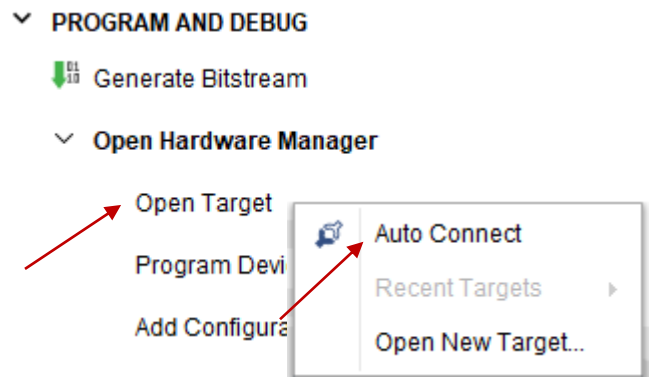
为了把实现的设计下载到实验板上，需要把最近实现的内容转换为二进制文件(.bit)。



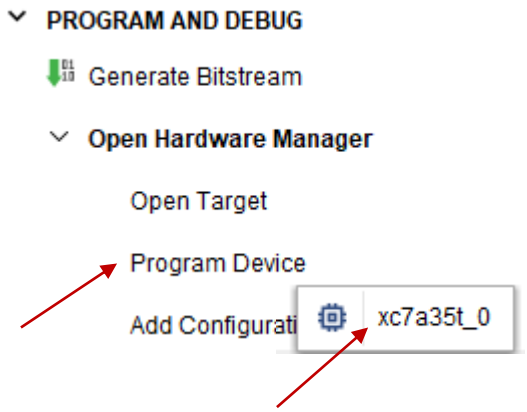
下载(Download)

把BitStream文件下载到实验板。

（1）



（2）

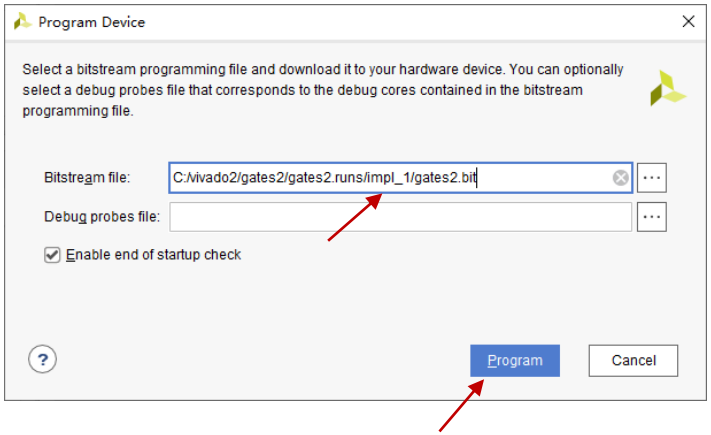


(1) 连接设备:Open Target/Auto Connect
可以同时连接多个设备。

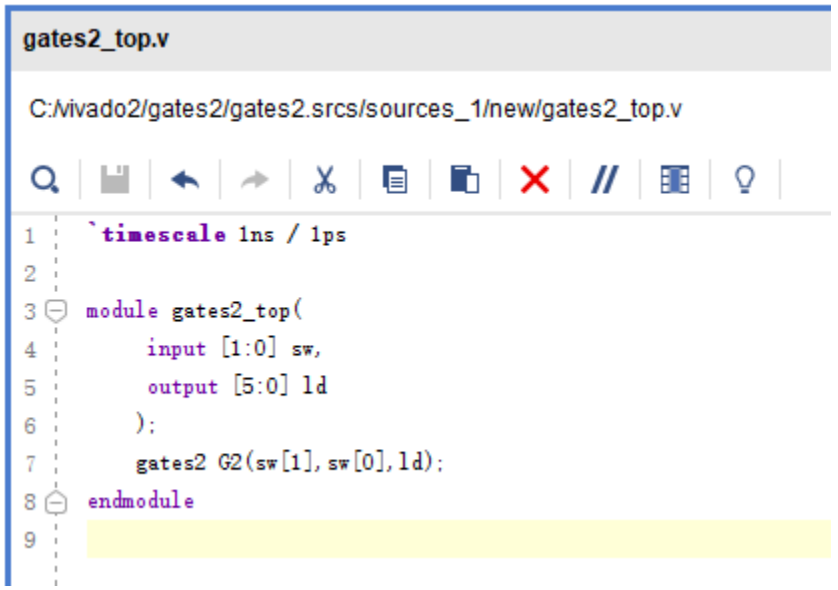
(2) 选择要下载的设备:
Program Device/xc7a35t_0

(3) 选择要下载的BitStream文件，然后下载。

(3)

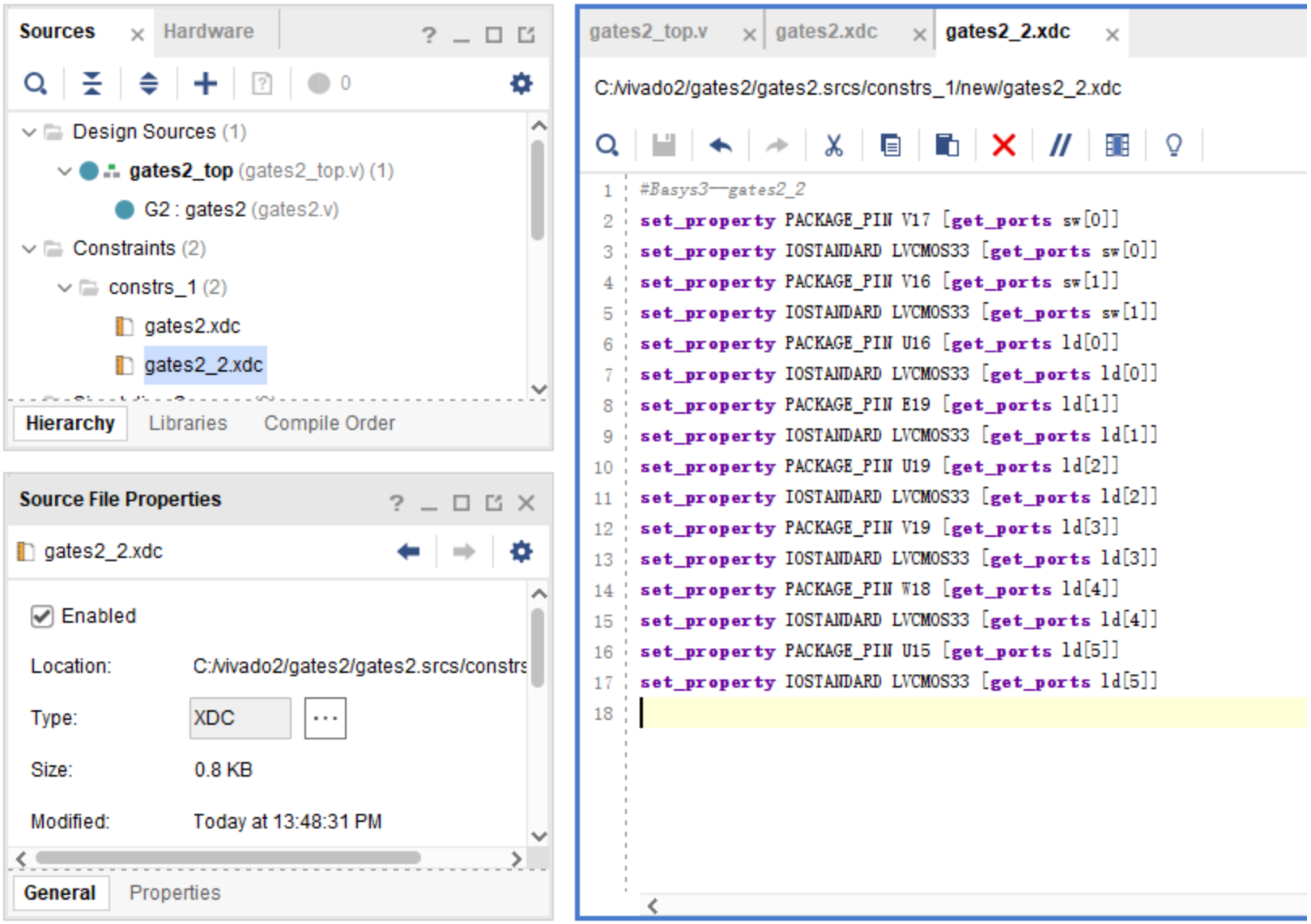


添加另一个设计源代码

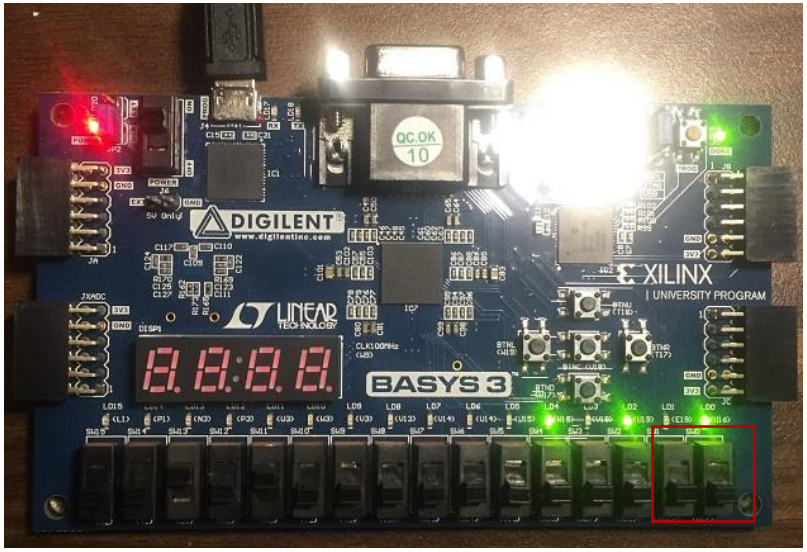


由于gates2_top.v调用了gates2.v，它自然成为了Top模块。可以手动(下拉菜单/Set as Top)把任何一个模块，例如，gates2.v，设置为顶层模块。

增加一个约束文件gates2_2.xdc



生成BitStream会自动选择合用的约束属性，也可以把需要用的约束文件在下拉菜单Disable File。最后在综合、实现、下载之后得到正确的结果。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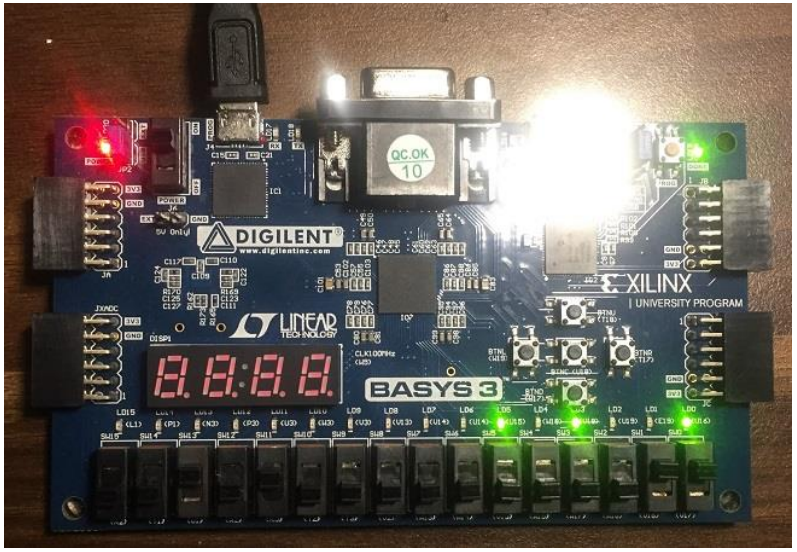
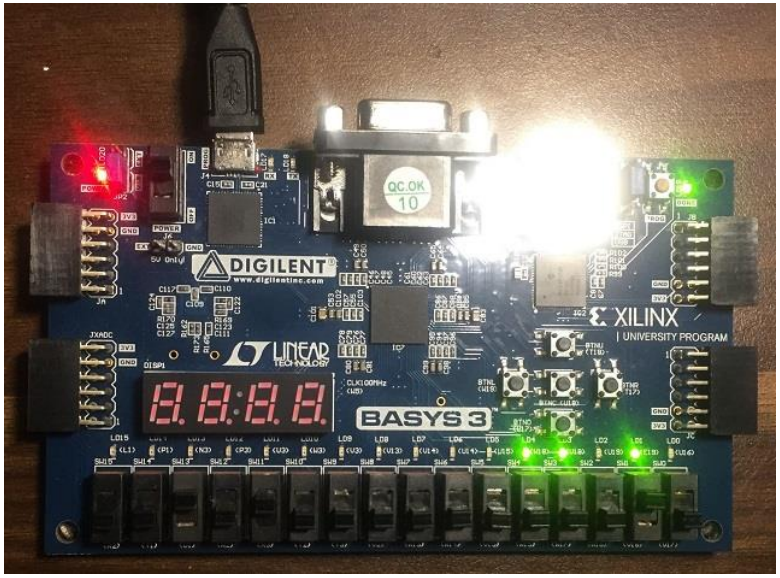
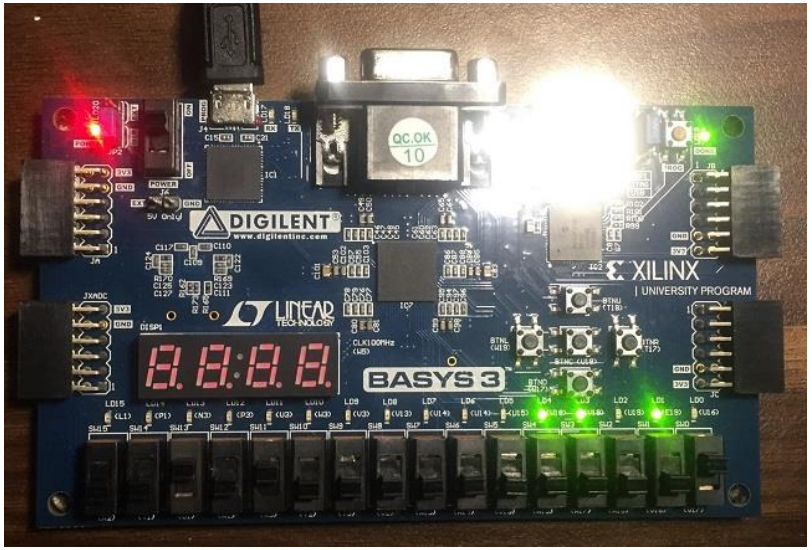
XILINX
UNIVERSITY PROGRAM
BASYS 3


DIGILENT
XILINX
UNIVERSITY PROGRAM
BASYS 3

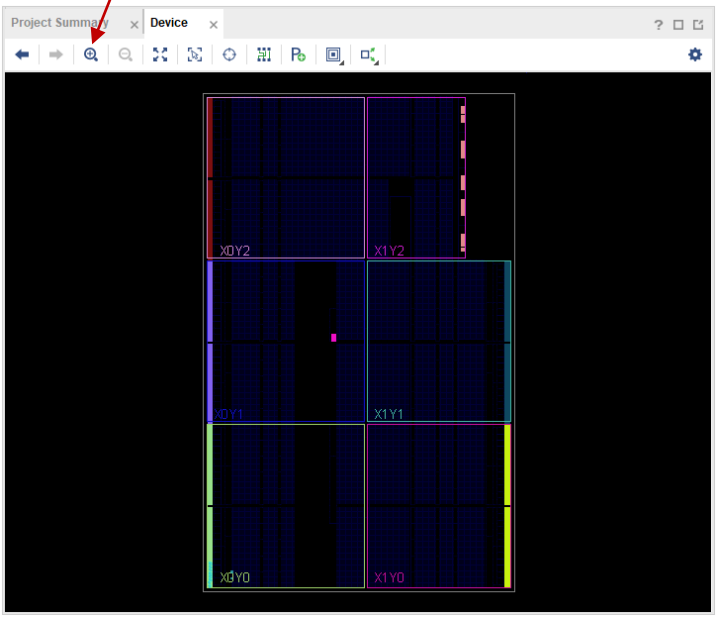

DIGILENT
XILINX
UNIVERSITY PROGRAM
BASYS 3


DIGILENT
XILINX
UNIVERSITY PROGRAM
BASYS 3

查看FPGA芯片

先点击Implematation，然后用Window/Device查看FPGA内部器件图

放大



放大后，可看到其中有些LUT已经被使用