Vivado工程2

用IP核实现多数选择器

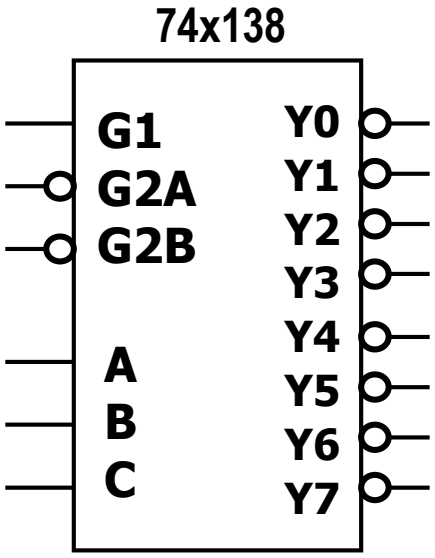
2019.11.17

FPGA芯片：xc7a35tcpg236-1

内容

- 3-8译码器
- 设计
- 仿真
- 约束
- FPGA测试
- 写入flash
- 创建IP核
- 用IP核实现多数表决器

74LS138



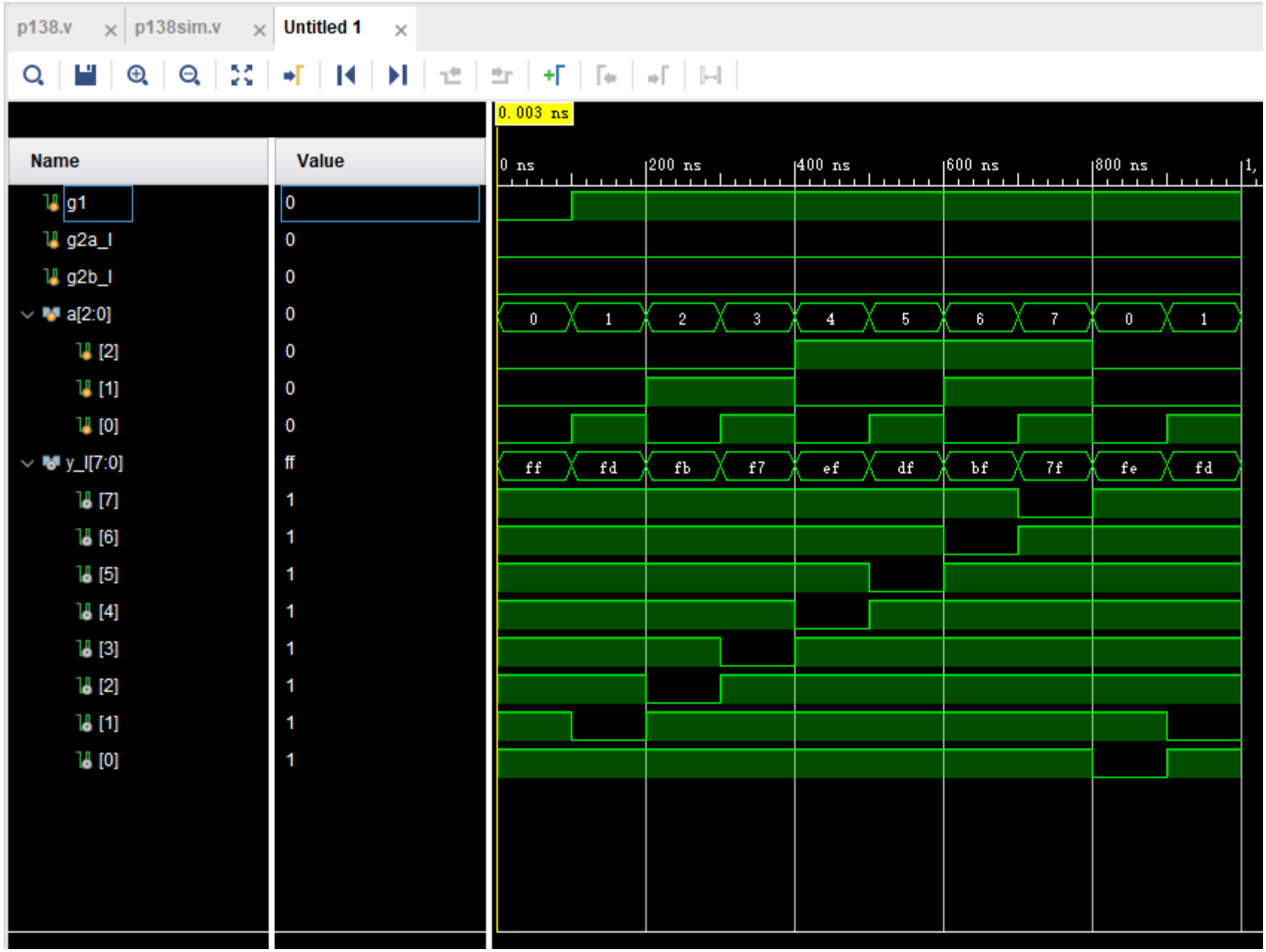
输入						输出							
g1	g2a_L	g2b_L	A_2	A_1	A_0	Y_0_L	Y_1_L	Y_2_L	Y_3_L	Y_4_L	Y_5_L	Y_6_L	Y_7_L
0	Ø	Ø	Ø	Ø	Ø	1	1	1	1	1	1	1	1
Ø	1	Ø	Ø	Ø	Ø	1	1	1	1	1	1	1	1
Ø	Ø	1	Ø	Ø	Ø	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

设计源代码(p138.v)

```
`timescale 1ns / 1ps
module p138(g1,g2a_l,g2b_l,a,y_l);
input g1,g2a_l,g2b_l;
input [2:0] a;
output [7:0] y_l;
reg [7:0] y_l=0;
always @ (g1 or g2a_l or g2b_l or a)
begin
    if (g1 && ~g2a_l && ~g2b_l)
     case (a)
        7:y_l=8'b01111111;
        6:y_l=8'b10111111;
        5:y_l=8'b11011111;
        4:y_l=8'b11101111;
        3:y_l=8'b11110111;
        2:y_l=8'b11111011;
        1:y_l=8'b11111101;
        0:y_l=8'b11111110;
       default:y_l=8'b11111111;
    endcase
  else
     y_l=8'b11111111;
end
endmodule
```

仿真源代码(p138sim.v)

```
`timescale 1ns / 1ps
module p138sim();
  reg g1;
  reg g2a_l;
  reg g2b_l;
  reg[2:0] a;
  wire[7:0] y_l;
  p138 v74x138(g1,g2a_l,g2b_l,a,y_l);
  initial begin
    g1 = 0;
    g2a_l = 0;
    g2b_l = 0;
    a = 0;
    #100;
    g1 = 1;
    g2a_l = 0;
    g2b_l = 0;
  end
  always #100 a = a+ 1;
endmodule
```


p138.v
p138sim.v
Untitled 1
Name
Value
g1
0
g2a_l
0
g2b_l
0
a[2:0]
0
[2]
0
[1]
0
[0]
0
y_l[7:0]
ff
[7]
1
[6]
1
[5]
1
[4]
1
[3]
1
[2]
1
[1]
1
[0]
1
0.003 ns
0 ns
200 ns
400 ns
600 ns
800 ns
0
1
2
3
4
5
6
7
0
1
ff
fd
fb
f7
ef
df
bf
7f
fe
fd

约束源代码(p138.xdc)

```
set_property PACKAGE_PIN W17 [get_ports g1]
set_property IOSTANDARD LVCMOS33 [get_ports g1]
set_property PACKAGE_PIN W15 [get_ports g2a_l]
set_property IOSTANDARD LVCMOS33 [get_ports g2a_l]
set_property PACKAGE_PIN V15 [get_ports g2b_l]
set_property IOSTANDARD LVCMOS33 [get_ports g2b_l]
set_property PACKAGE_PIN W16 [get_ports a[2]]
set_property IOSTANDARD LVCMOS33 [get_ports a[2]]
set_property PACKAGE_PIN V16 [get_ports a[1]]
set_property IOSTANDARD LVCMOS33 [get_ports a[1]]
set_property PACKAGE_PIN V17 [get_ports a[0]]
set_property IOSTANDARD LVCMOS33 [get_ports a[0]]
set_property PACKAGE_PIN U16 [get_ports y_l[0]]
set_property IOSTANDARD LVCMOS33 [get_ports y_l[0]]
set_property PACKAGE_PIN E19 [get_ports y_l[1]]
set_property IOSTANDARD LVCMOS33 [get_ports y_l[1]]
set_property PACKAGE_PIN U19 [get_ports y_l[2]]
set_property IOSTANDARD LVCMOS33 [get_ports y_l[2]]
set_property PACKAGE_PIN V19 [get_ports y_l[3]]
set_property IOSTANDARD LVCMOS33 [get_ports y_l[3]]
set_property PACKAGE_PIN W18 [get_ports y_l[4]]
set_property IOSTANDARD LVCMOS33 [get_ports y_l[4]]
set_property PACKAGE_PIN U15 [get_ports y_l[5]]
set_property IOSTANDARD LVCMOS33 [get_ports y_l[5]]
set_property PACKAGE_PIN U14 [get_ports y_l[6]]
set_property IOSTANDARD LVCMOS33 [get_ports y_l[6]]
set_property PACKAGE_PIN V14 [get_ports y_l[7]]
set_property IOSTANDARD LVCMOS33 [get_ports y_l[7]]
```

FPGA引脚：

sw0: V17 sw1:V16 sw2: W16 sw3: W17 sw4: W15
sw5: V15 sw6: W14 sw7: W13 sw8: V2 sw9: T3
sw10: T2 sw11: R3 sw12: W2 sw13: U1 sw14: T1
sw15: R2

led0: U16 led1: E19 led2: U19 led3: V19 led4: W18
led5:U15 led6: U14 led7: V14 led8: V13 led9: V3
led10: W3 led11: U3 led12: P3 led13: N3 led14: P1
led15: L1

FPGA测试

综合

↓

实现

↓

生成 Bitstream

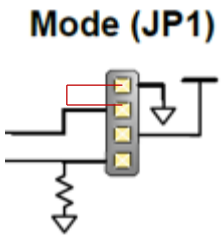
↓

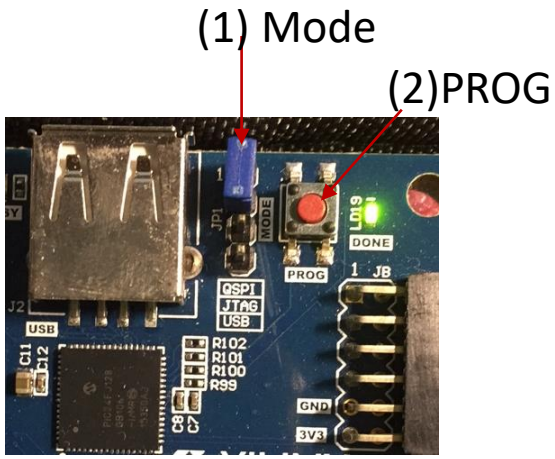
写入FPGA

写入flash

如果希望在掉电时FPGA可以正常工作，就要再Flash中保存Binary程序：

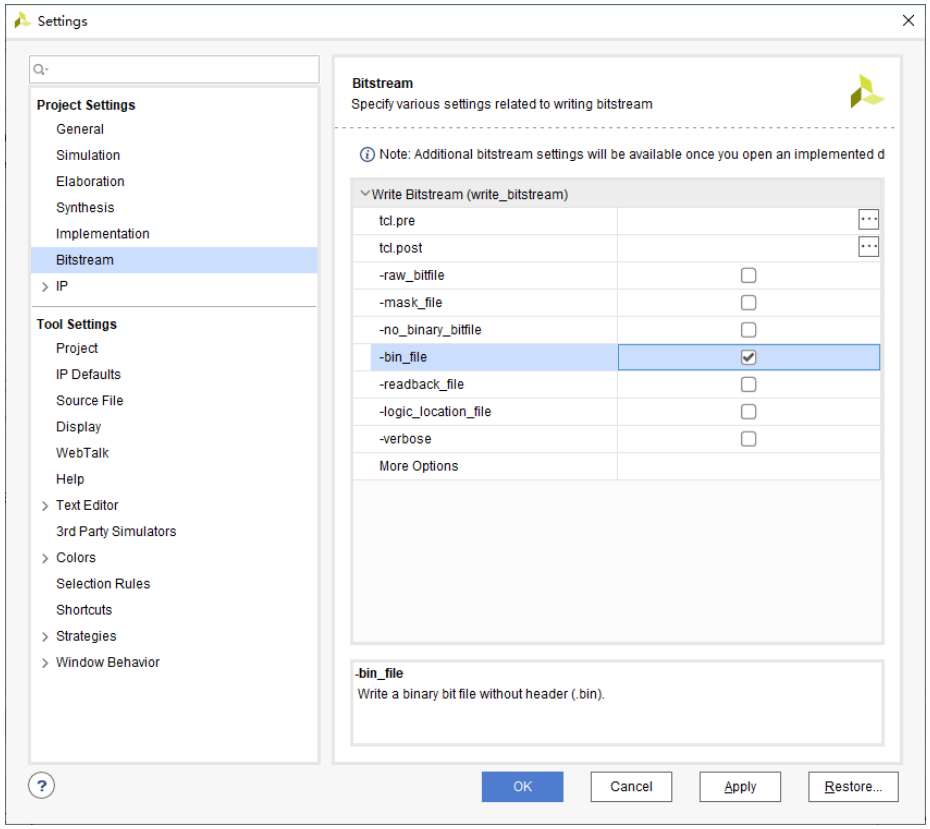
（1）把右上角的MODE的跳线帽连接到最上面两根针，即使用QSPI模式。





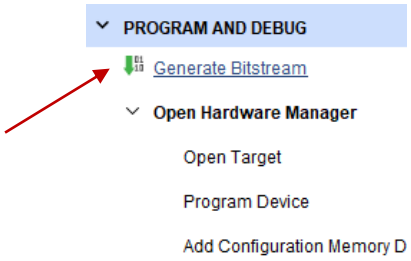
参考 参考

（2）选择和生成Binary文件。

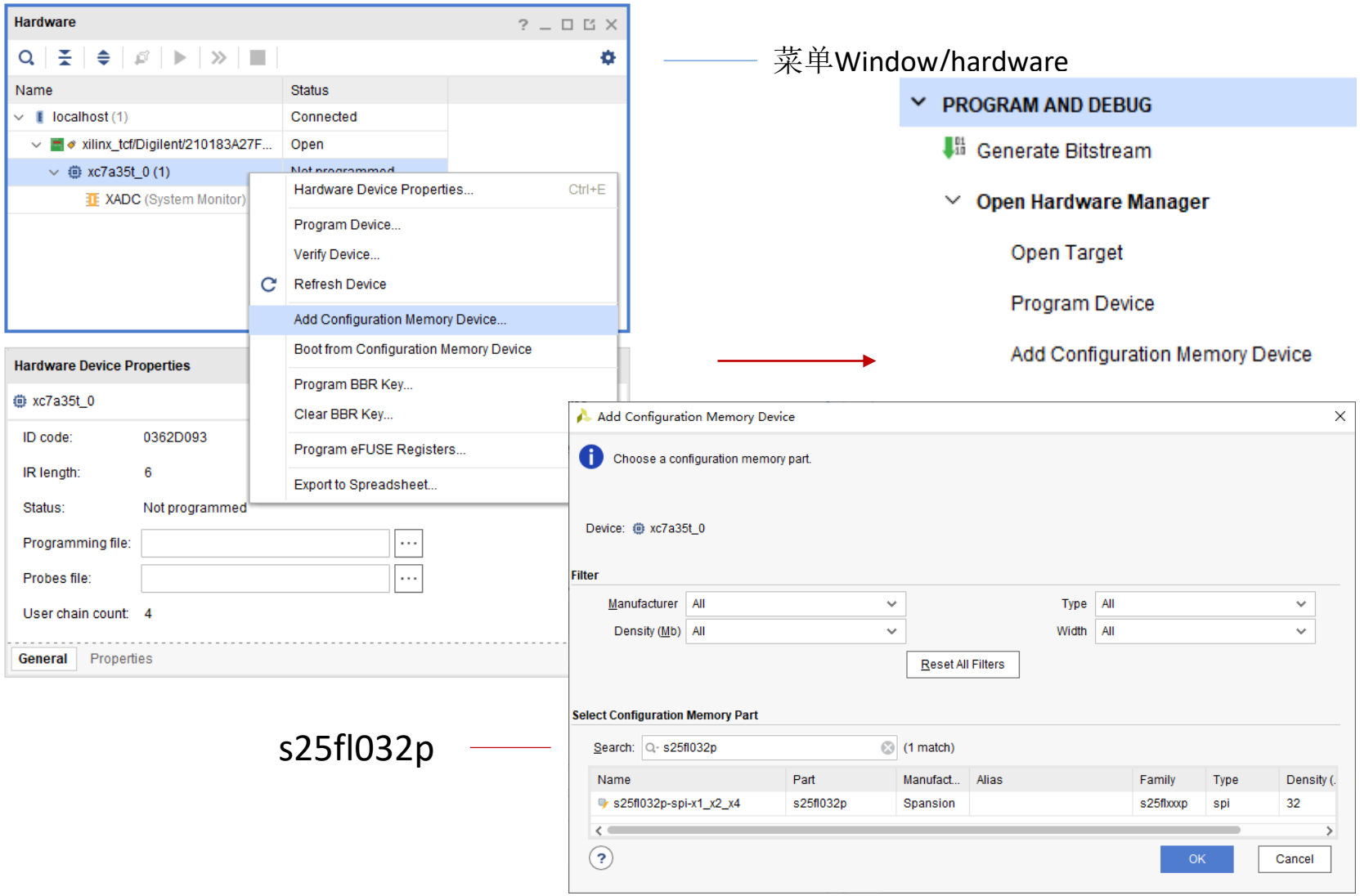


菜单：
Flow/Settings/Bitstream Settings

下拉菜单：
Generate Bitstream/Bitstream Settings

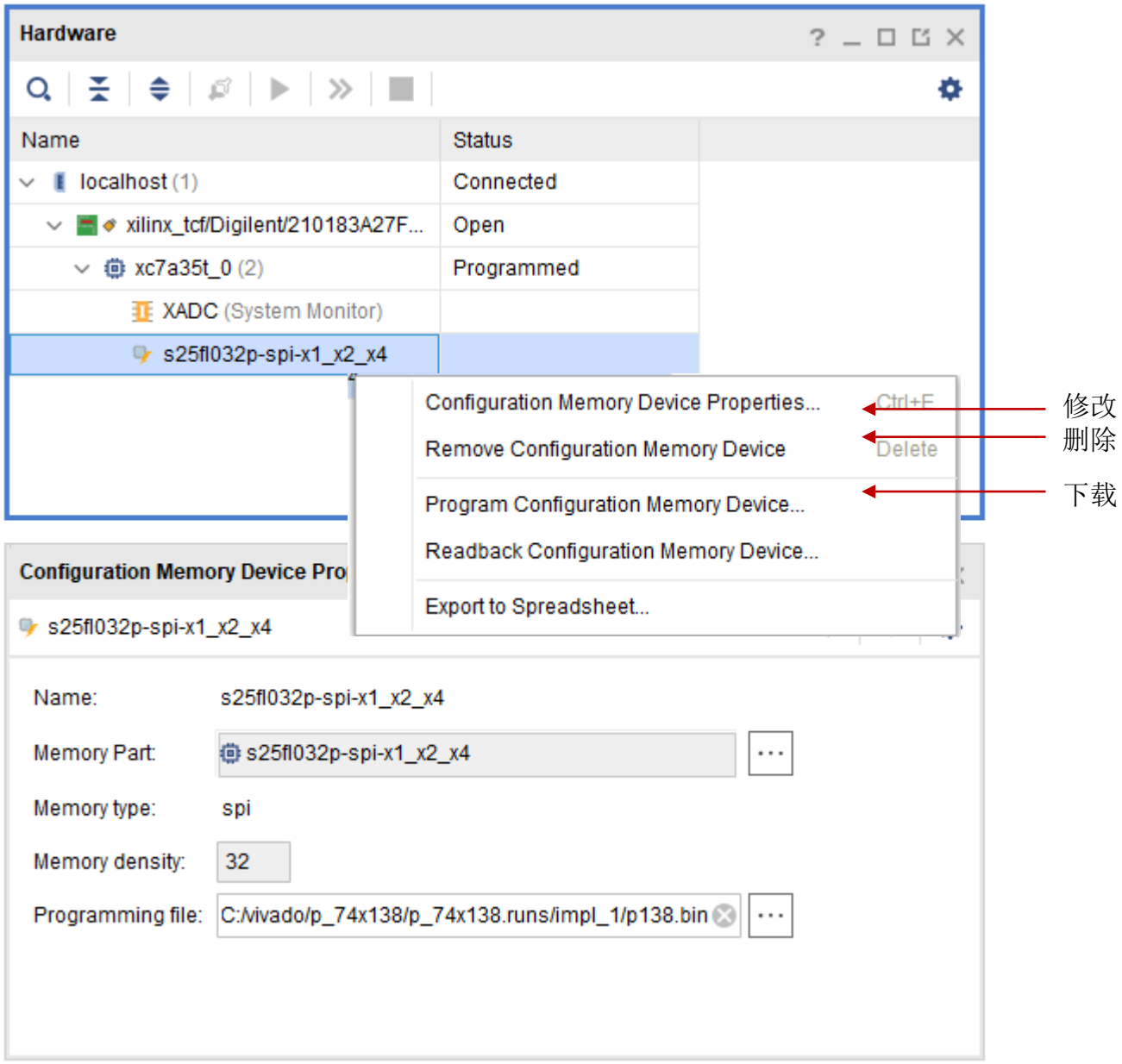


（3）选择配置存储设备

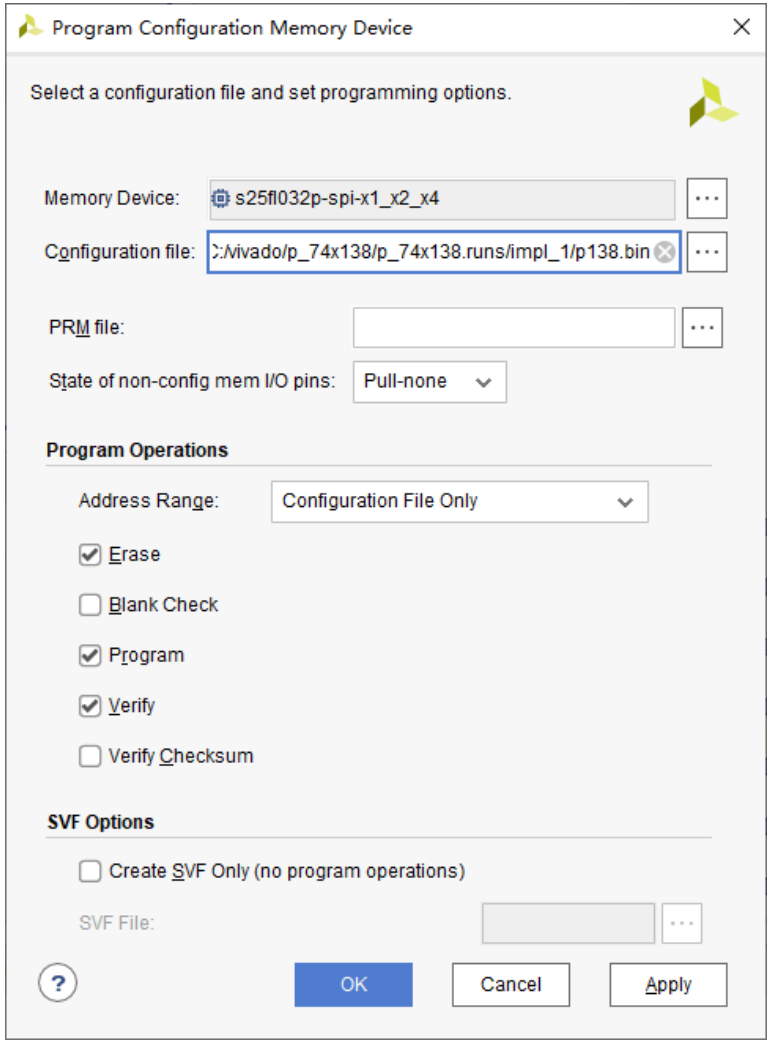


* 选错时，系统会给出应该选择的芯片型号

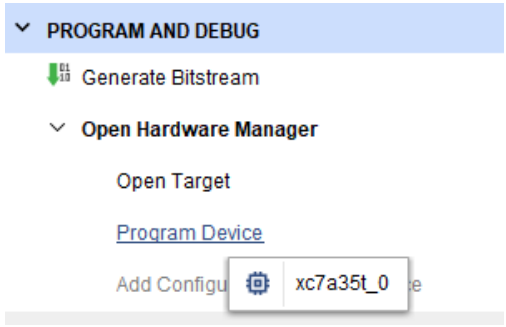
可以修改或删除或下载


Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Digilent/210183A27F...
Open
xc7a35t_0 (2)
Programmed
XADC (System Monitor)
s25fl032p-spi-x1_x2_x4
Configuration Memory Device Properties... Ctrl+E
Remove Configuration Memory Device Delete
Program Configuration Memory Device...
Readback Configuration Memory Device...
Export to Spreadsheet...
修改
删除
下载
Configuration Memory Device Pro
s25fl032p-spi-x1_x2_x4
Name: s25fl032p-spi-x1_x2_x4
Memory Part: s25fl032p-spi-x1_x2_x4
Memory type: spi
Memory density: 32
Programming file: C:/vivado/p_74x138/p_74x138.runs/impl_1/p138.bin

（4）下载 （菜单见上页）



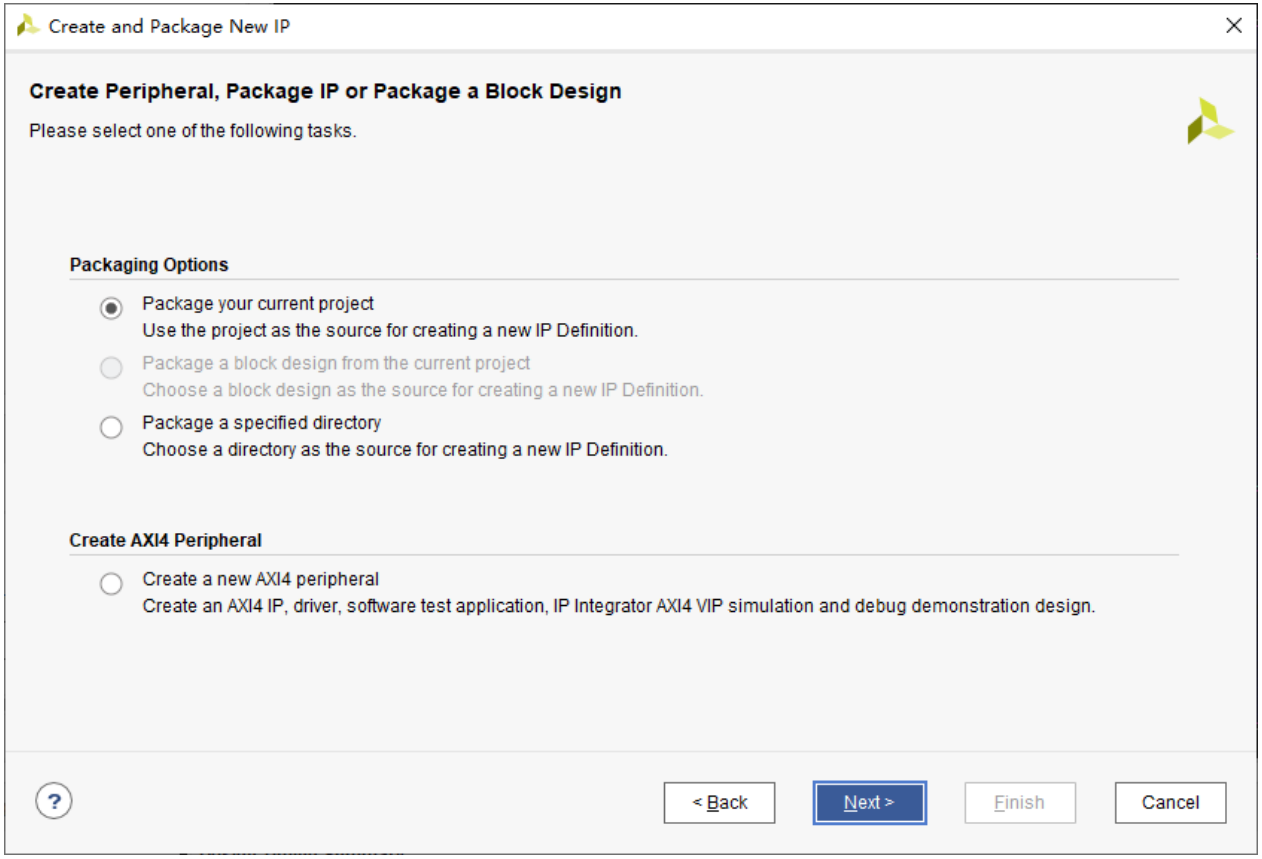
或

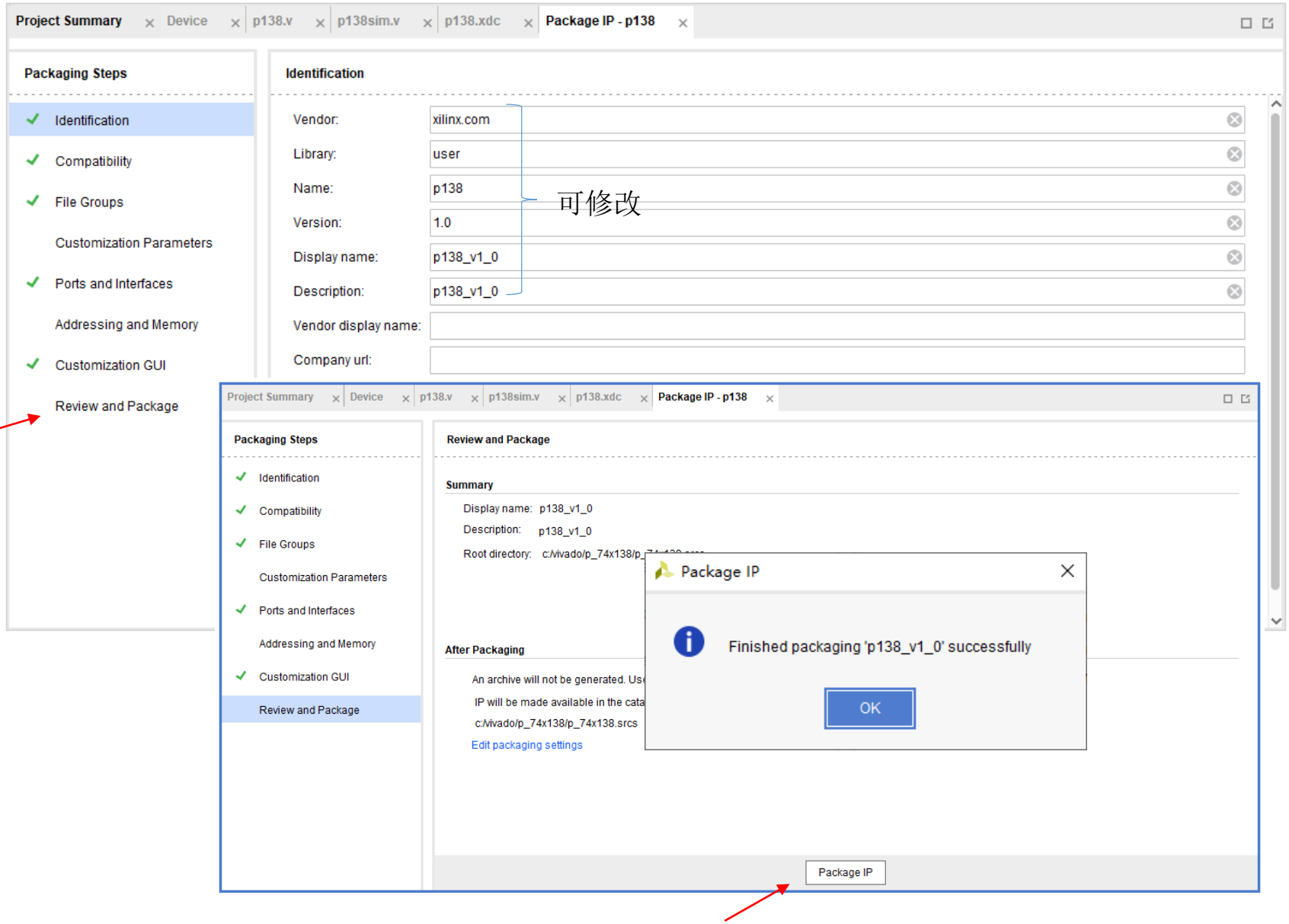


下载并重启后要按右上角的PROG按钮才开始执行flash中指令。

创建IP核

点击Implementation，菜单Tools/Create and Package New IP

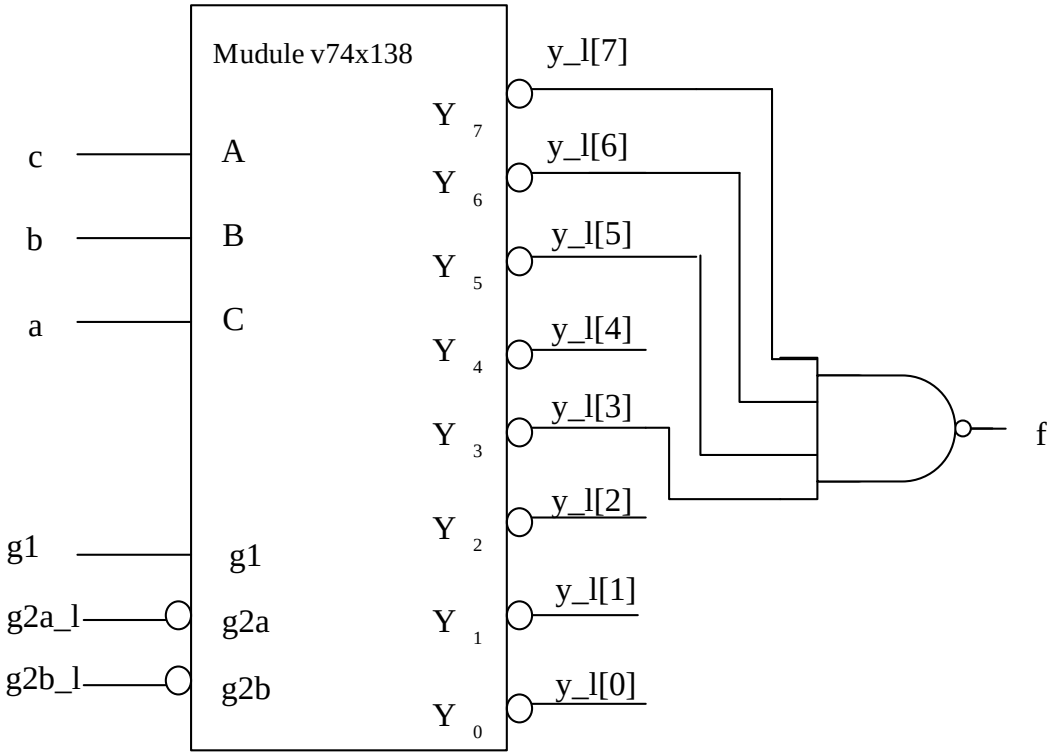



Project Summary
Device
p138.v
p138sim.v
p138.xdc
Package IP - p138
Packaging Steps
Identification
Compatibility
File Groups
Customization Parameters
Ports and Interfaces
Addressing and Memory
Customization GUI
Review and Package
Identification
Vendor:
xilinx.com
Library:
user
Name:
p138
Version:
1.0
Display name:
p138_v1_0
Description:
p138_v1_0
Vendor display name:
Company url:
可修改
Review and Package
Summary
Display name: p138_v1_0
Description: p138_v1_0
Root directory:
After Packaging
An archive will not be generated.
IP will be made available in the cata
c:/vivado/p_74x138/p_74x138.srcs
Edit packaging settings
Package IP
Finished packaging 'p138_v1_0' successfully
OK
Package IP

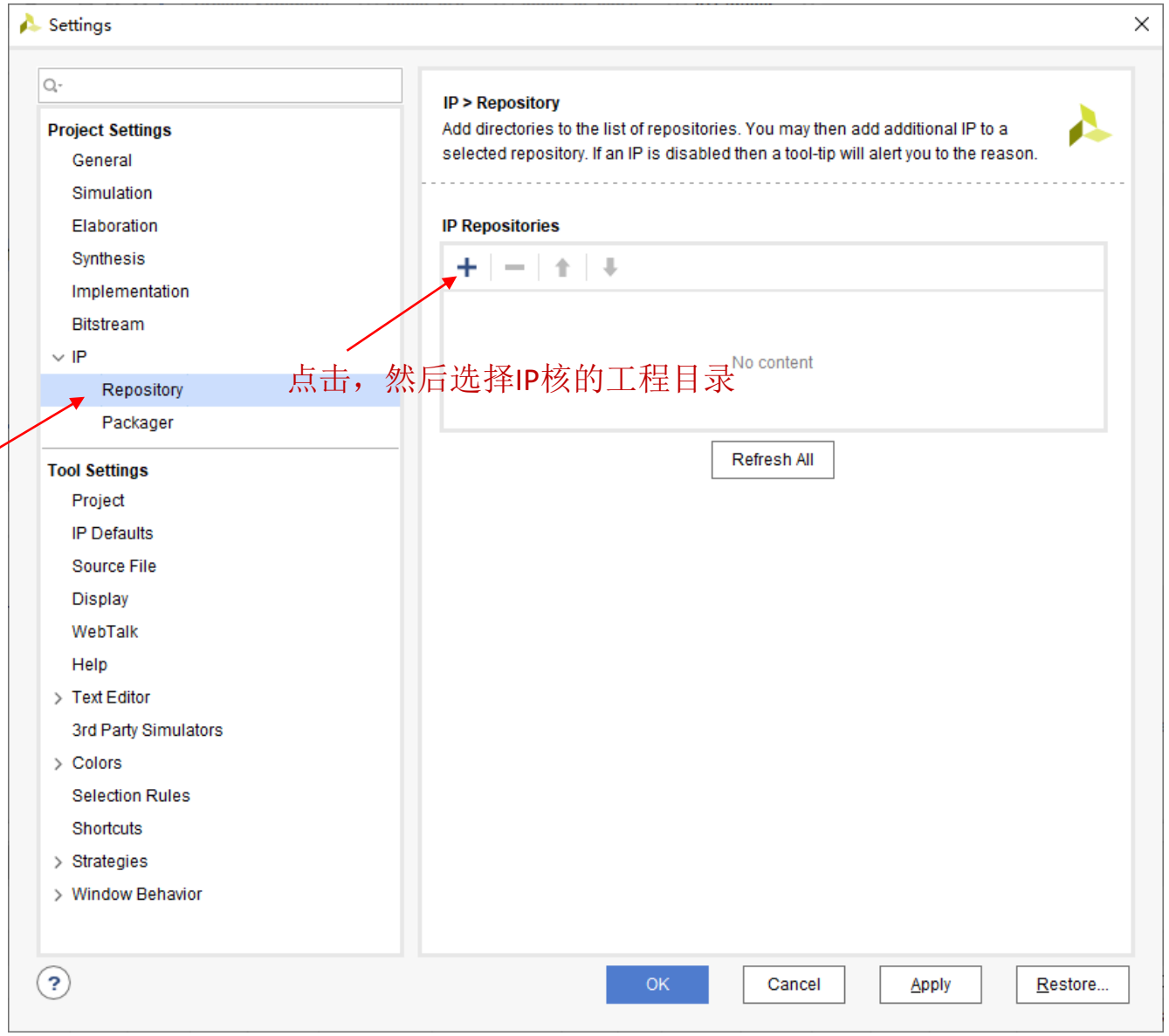
用IP核实现多数表决器

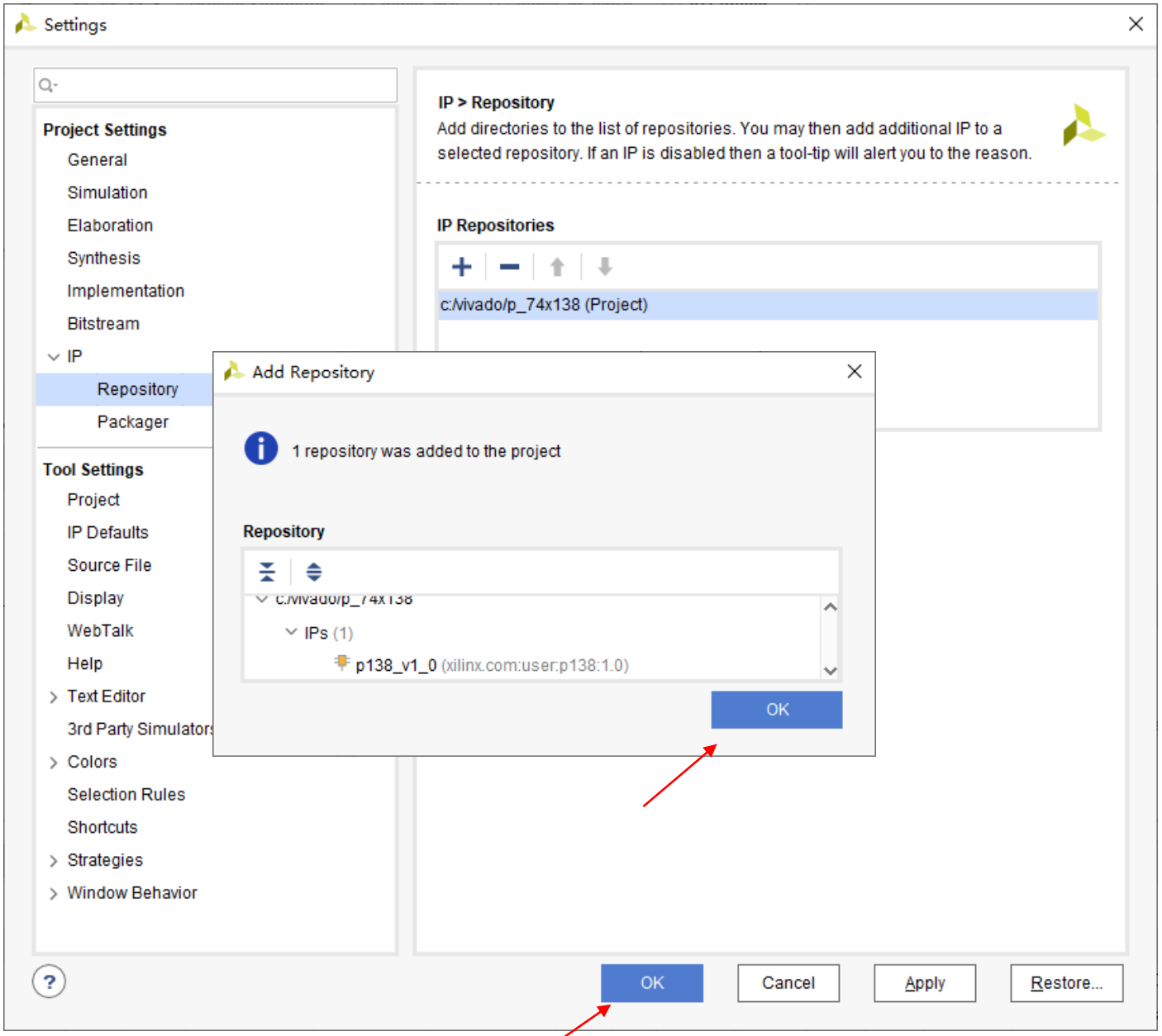
a b c	f
0 0 0	0
0 0 1	0
0 1 0	0
0 1 1	1
1 0 0	0
1 0 1	1
1 1 0	1
1 1 1	1

$f = \sum_{abc}(3,5,6,7)$

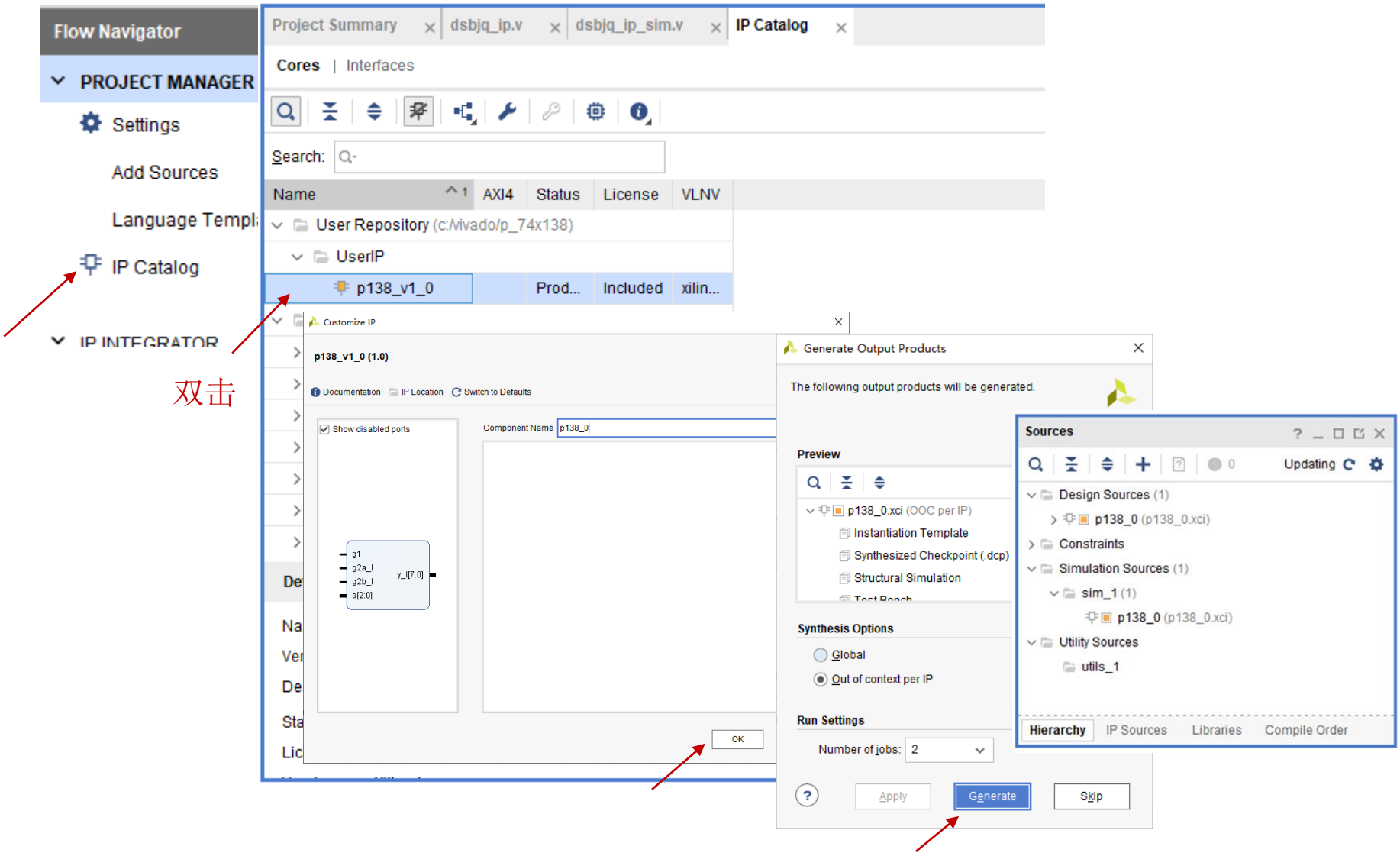


把IP核加入库：Tools/Settings

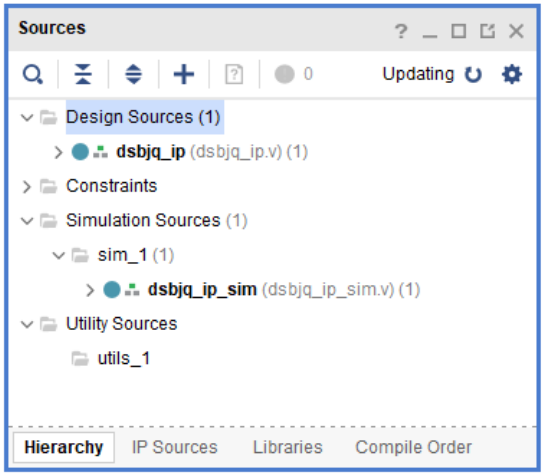



Settings
Project Settings
General
Simulation
Elaboration
Synthesis
Implementation
Bitstream
IP
Repository
Packager
Tool Settings
Project
IP Defaults
Source File
Display
WebTalk
Help
Text Editor
3rd Party Simulators
Colors
Selection Rules
Shortcuts
Strategies
Window Behavior
IP > Repository
Add directories to the list of repositories. You may then add additional IP to a selected repository. If an IP is disabled then a tool-tip will alert you to the reason.
IP Repositories
c:/vivado/p_74x138 (Project)
Add Repository
1 repository was added to the project
Repository
IPs (1)
p138_v1_0 (xilinx.com:user:p138:1.0)
OK
OK
Cancel
Apply
Restore...

把IP核加入项目


Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templ
IP Catalog
IP INTEGRATOR
双击
Project Summary
dsbjq_ip.v
dsbjq_ip_sim.v
IP Catalog
Cores | Interfaces
Search:
Name
AXI4
Status
License
VLNV
User Repository (c:/vivado/p_74x138)
UserIP
p138_v1_0
Prod...
Included
xilin...
Customize IP
p138_v1_0 (1.0)
Documentation
IP Location
Switch to Defaults
Show disabled ports
Component Name
p138_0
OK
Generate Output Products
The following output products will be generated.
Preview
p138_0.xci (OOC per IP)
Instantiation Template
Synthesized Checkpoint (.dcp)
Structural Simulation
Synthesis Options
Global
Out of context per IP
Run Settings
Number of jobs:
2
Apply
Generate
Skip
Sources
Updating
Design Sources (1)
p138_0 (p138_0.xci)
Constraints
Simulation Sources (1)
sim_1 (1)
p138_0 (p138_0.xci)
Utility Sources
utils_1
Hierarchy
IP Sources
Libraries
Compile Order

加入设计源代码和仿真源代码



dsbjq_ip_sim.v

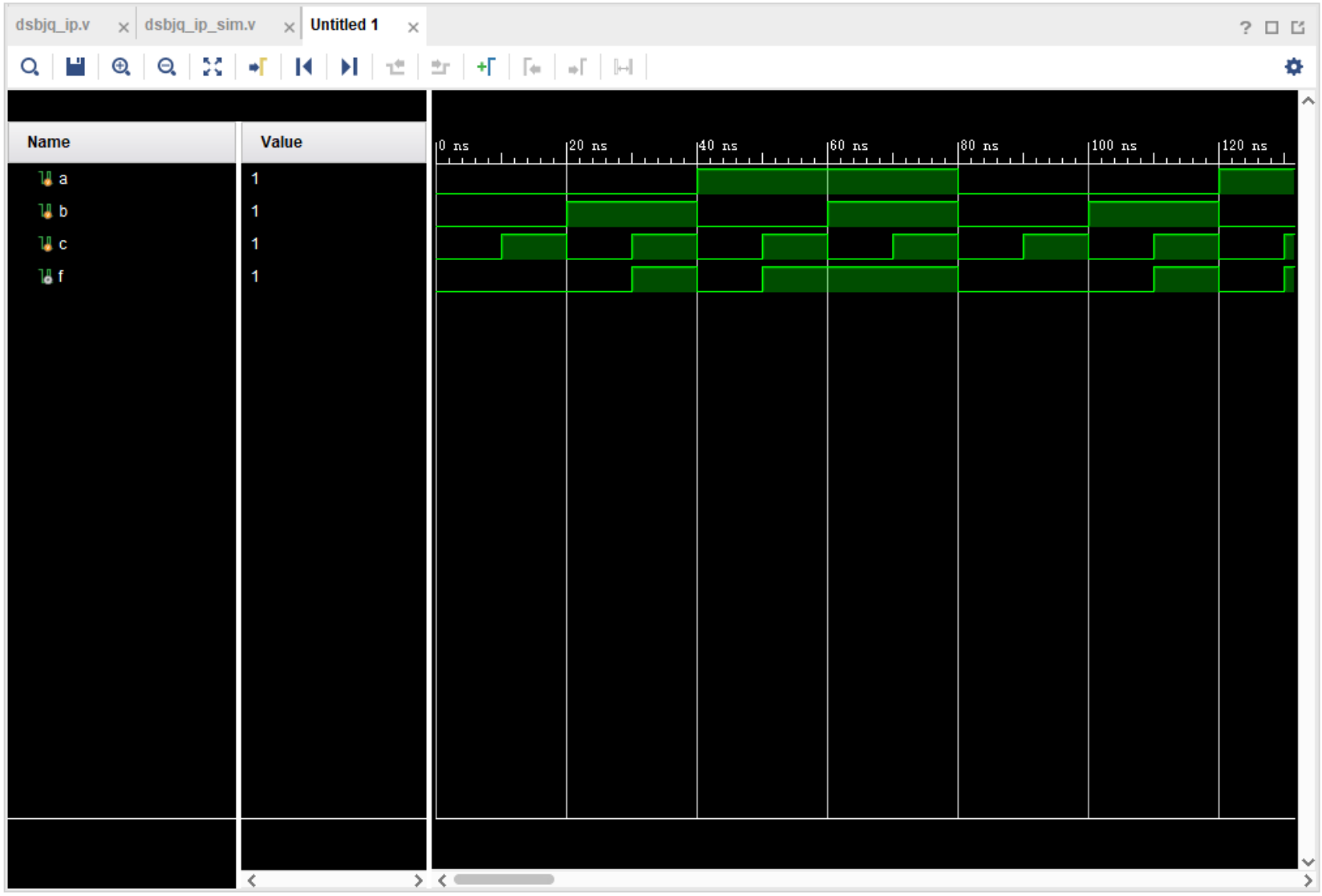
```
`timescale 1ns / 1ps
module dsbjq_ip_sim;
 reg a,b,c;
 wire f;
 dsbjq_ip uut_0(a,b,c,f);
 initial begin
   a=0;
   b=0;
   c=0;
 end
 always #10 {a,b,c}={a,b,c}+1;
endmodule
```

dsbjq_ip.v

```
`timescale 1ns / 1ps

module dsbjq_ip(input a, input b, input c, output f);
wire[7:0] y_l;
assign f = ~(y_l[7] & y_l[6] & y_l[5] & y_l[3]);
p138_0 uut_0(.g1(1),.g2a_l(0),.g2b_l(0),.a({c,b,a}),.y_l(y_l));
endmodule
```

仿真结果


dsbjq_ip.v
dsbjq_ip_sim.v
Untitled 1
Name
Value
a
1
b
1
c
1
f
1
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns

加入约束源代码(dsbjq_ip.xdc)

```
set_property PACKAGE_PIN W16 [get_ports c]
set_property IOSTANDARD LVCMOS33 [get_ports c]
set_property PACKAGE_PIN V16 [get_ports b]
set_property IOSTANDARD LVCMOS33 [get_ports b]
set_property PACKAGE_PIN V17 [get_ports a]
set_property IOSTANDARD LVCMOS33 [get_ports a]
set_property PACKAGE_PIN U16 [get_ports f]
set_property IOSTANDARD LVCMOS33 [get_ports f]
```

sw0: V17 sw1:V16 sw2: W16 sw3: W17 sw4: W15
sw5: V15 sw6: W14 sw7: W13 sw8: V2 sw9: T3
sw10: T2 sw11: R3 sw12: W2 sw13: U1 sw14: T1
sw15: R2

led0: U16 led1: E19 led2: U19 led3: V19 led4: W18
led5:U15 led6: U14 led7: V14 led8: V13 led9: V3
led10: W3 led11: U3 led12: P3 led13: N3 led14: P1
led15: L1

综合、实现和下载：