



电子科技大学  
University of Electronic Science and Technology of China



# 数字设计FPGA应用

第三章 组合逻辑电路与VIVADO进阶

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# 第三章 组合逻辑电路与VIVADO进阶

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3.2.2 译码器IP核生成

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# 第一个工程——多数表决器

有什么样的输入，就有什么样的输出，数字电路的输出只依赖于当前输入值的组合，这样的电路称为**组合逻辑**电路。

例如 **$f=ab+ac$**

第一个工程使用**FPGA**实现一个简单的组合逻辑电路。



题目：假设有三个举重裁判，举重选手完成比赛后，当有多数裁判认定成功，则成功；否则失败。请设计此举重裁决电路。

这个举重裁决电路实际上就是一个三输入的**多数表决器**。



# 第一个工程——多数表决器

假设多数表决器的三个输入分别是**a**、**b**、**c**，输出是**f**。

根据问题的描述，填写真值表

得到最小项表达式 **$f = \sum_{abc}(3,5,6,7)$** 。

填写卡诺图进行化简

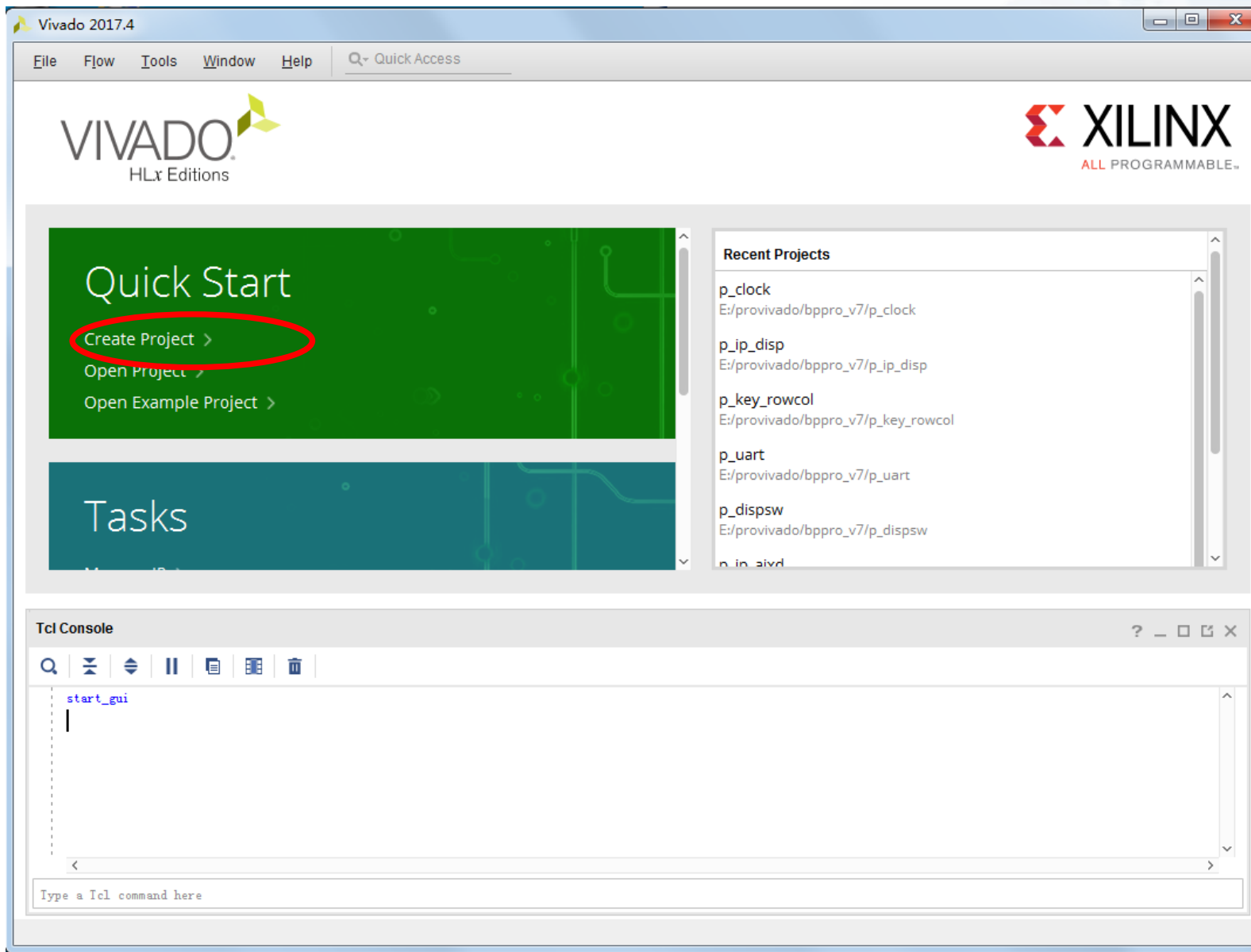
得 **$f=ab+bc+ac$**

a b c	f
0 0 0	0
0 0 1	0
0 1 0	0
0 1 1	1
1 0 0	0
1 0 1	1
1 1 0	1
1 1 1	1

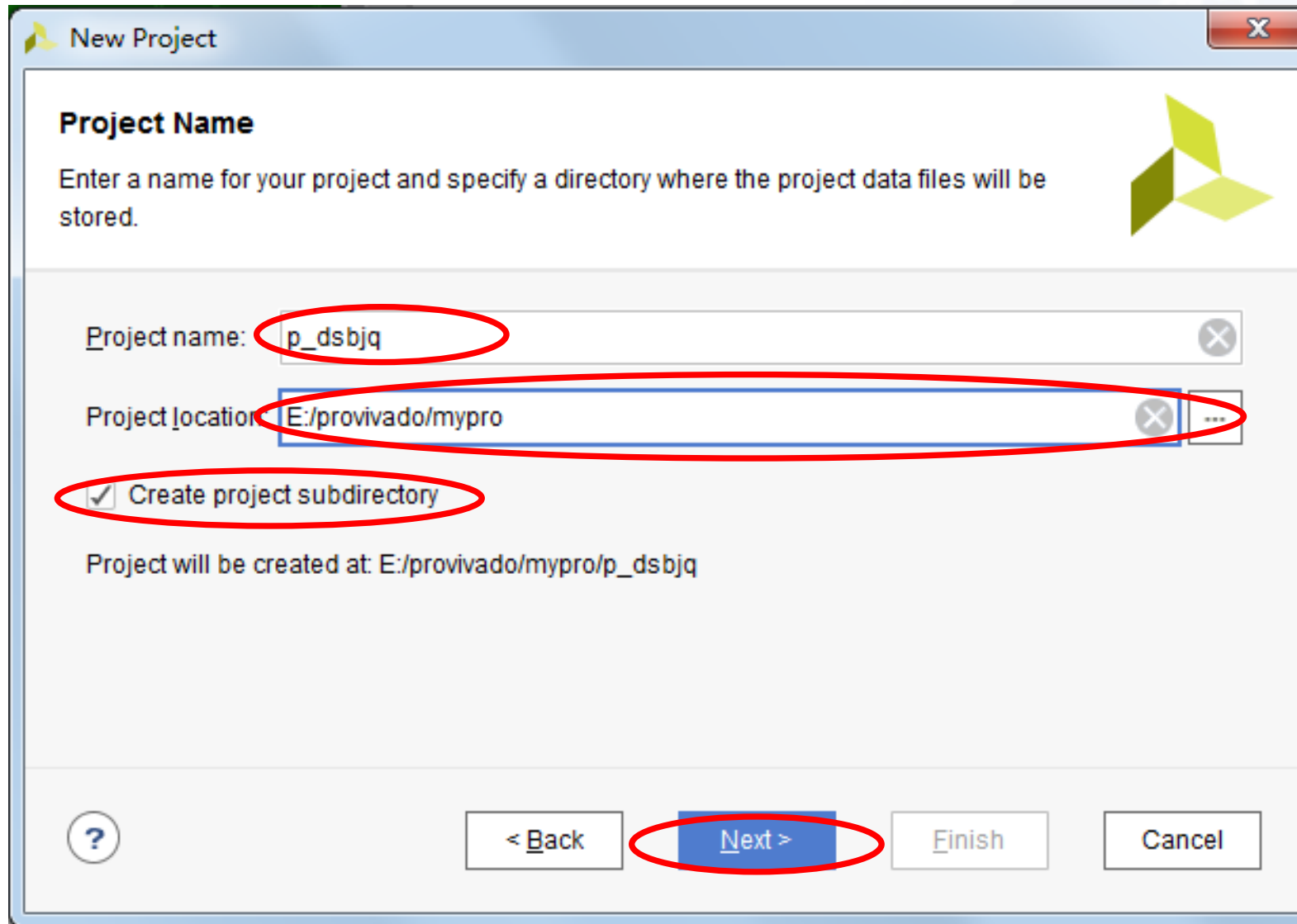
$ab \backslash c$					
		00	01	11	10
0		0	0	1	0
1		0	1	1	1



# 打开VIVADO并新建工程



## 打开VIVADO并新建工程



The image shows the 'New Project' dialog box in Vivado. The dialog has a title bar with the Vivado logo and a close button. The main area is titled 'Project Name' and contains instructions: 'Enter a name for your project and specify a directory where the project data files will be stored.' Below this, there are three input fields: 'Project name:' with the value 'p\_dsbjq', 'Project location:' with the value 'E:/provivado/mypro', and a checkbox labeled 'Create project subdirectory' which is checked. Below these fields, it says 'Project will be created at: E:/provivado/mypro/p\_dsbjq'. At the bottom, there are four buttons: a help button (question mark), '< Back', 'Next >', and 'Cancel'. The 'Next >' button is highlighted in blue. Red circles are drawn around the 'Project name' field, the 'Project location' field, the 'Create project subdirectory' checkbox, and the 'Next >' button.

**New Project**

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name: p\_dsbjq

Project location: E:/provivado/mypro

☒ Create project subdirectory

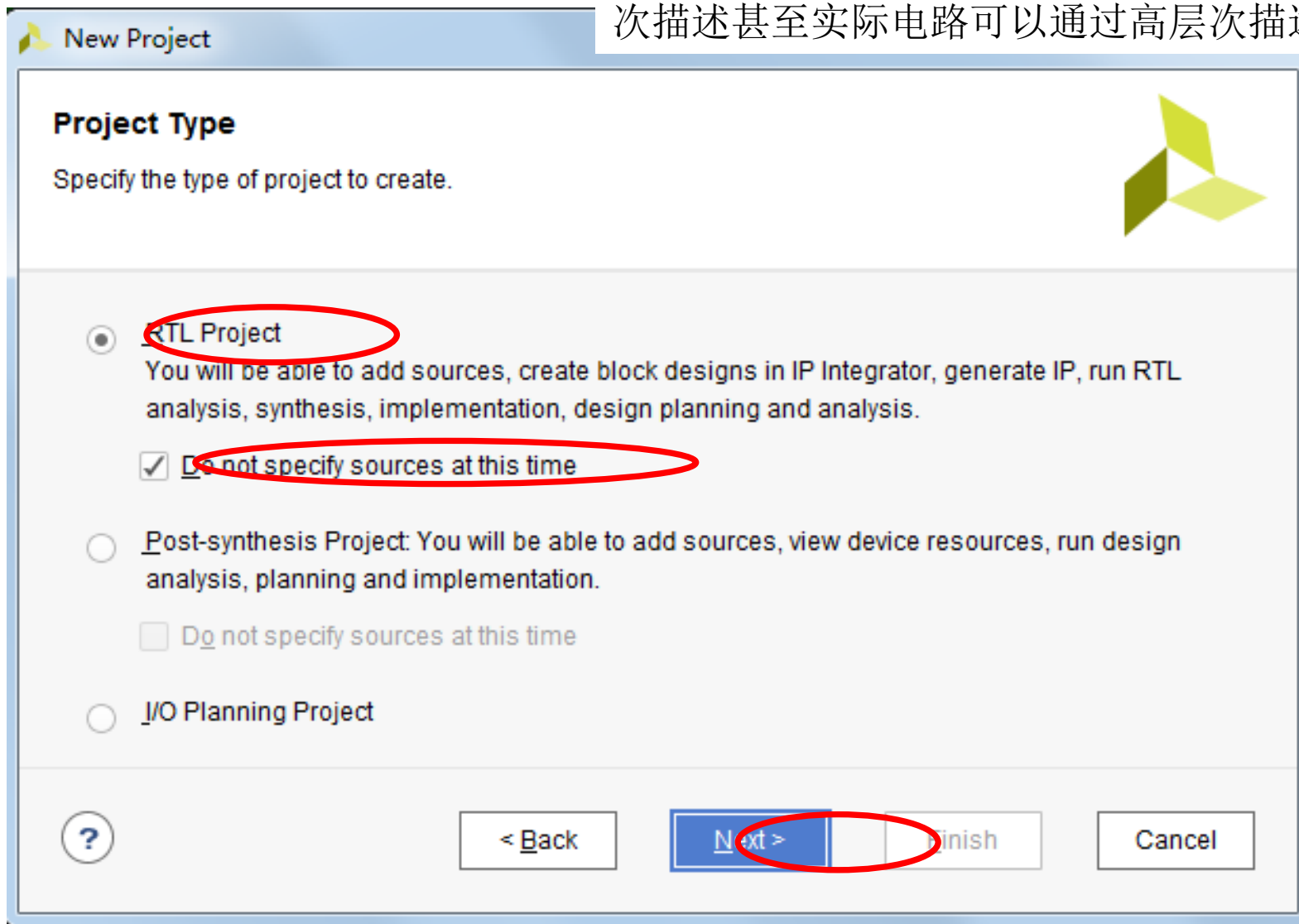
Project will be created at: E:/provivado/mypro/p\_dsbjq

? < Back Next > Finish Cancel



## 工程类型设置

寄存器传输级(Register-Transfer Level, RTL)抽象模型被Verilog和VHDL等硬件描述语言用于创建对实际电路的高层次描述，而低层次描述甚至实际电路可以通过高层次描述采用逻辑合成工具导出。



The image shows a 'New Project' dialog box with the title 'New Project' and a yellow logo. The main section is titled 'Project Type' with the instruction 'Specify the type of project to create.' Below this, there are three radio button options. The first option, 'RTL Project', is selected and circled in red. Below it, the text 'You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.' is displayed. A checkbox labeled 'Do not specify sources at this time' is checked and circled in red. The second option, 'Post-synthesis Project', is unselected and has the text 'You will be able to add sources, view device resources, run design analysis, planning and implementation.' below it. A checkbox labeled 'Do not specify sources at this time' is unselected. The third option, 'I/O Planning Project', is unselected. At the bottom, there is a help icon (question mark in a circle), a '< Back' button, a 'Next >' button (highlighted in blue and circled in red), a 'Finish' button, and a 'Cancel' button.

**New Project**

**Project Type**  
Specify the type of project to create.

☒ **RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
☒ Do not specify sources at this time

☐ **Post-synthesis Project**: You will be able to add sources, view device resources, run design analysis, planning and implementation.  
☐ Do not specify sources at this time

☐ **I/O Planning Project**

? < Back Next > Finish Cancel





# 工程器件选择

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: 

Parts

Boards

Filter

Product category: 

All

Speed grade: 

All

Family: 

All

Temp grade: 

All

Package: 

All

xc7a35tcpg236-1

Reset All Filters

Search: 

xc7a35tfg256

 (4 matches)

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE2 Transceiv
<div>xc7a35tfg256-3</div>	256	170	20800	41600	50	0	90	0	0
<div>xc7a35tfg256-2</div>	256	170	20800	41600	50	0	90	0	0
<div>xc7a35tfg256-2L</div>	256	170	20800	41600	50	0	90	0	0
<div>xc7a35tfg256-1</div>	256	170	20800	41600	50	0	90	0	0

?

< Back

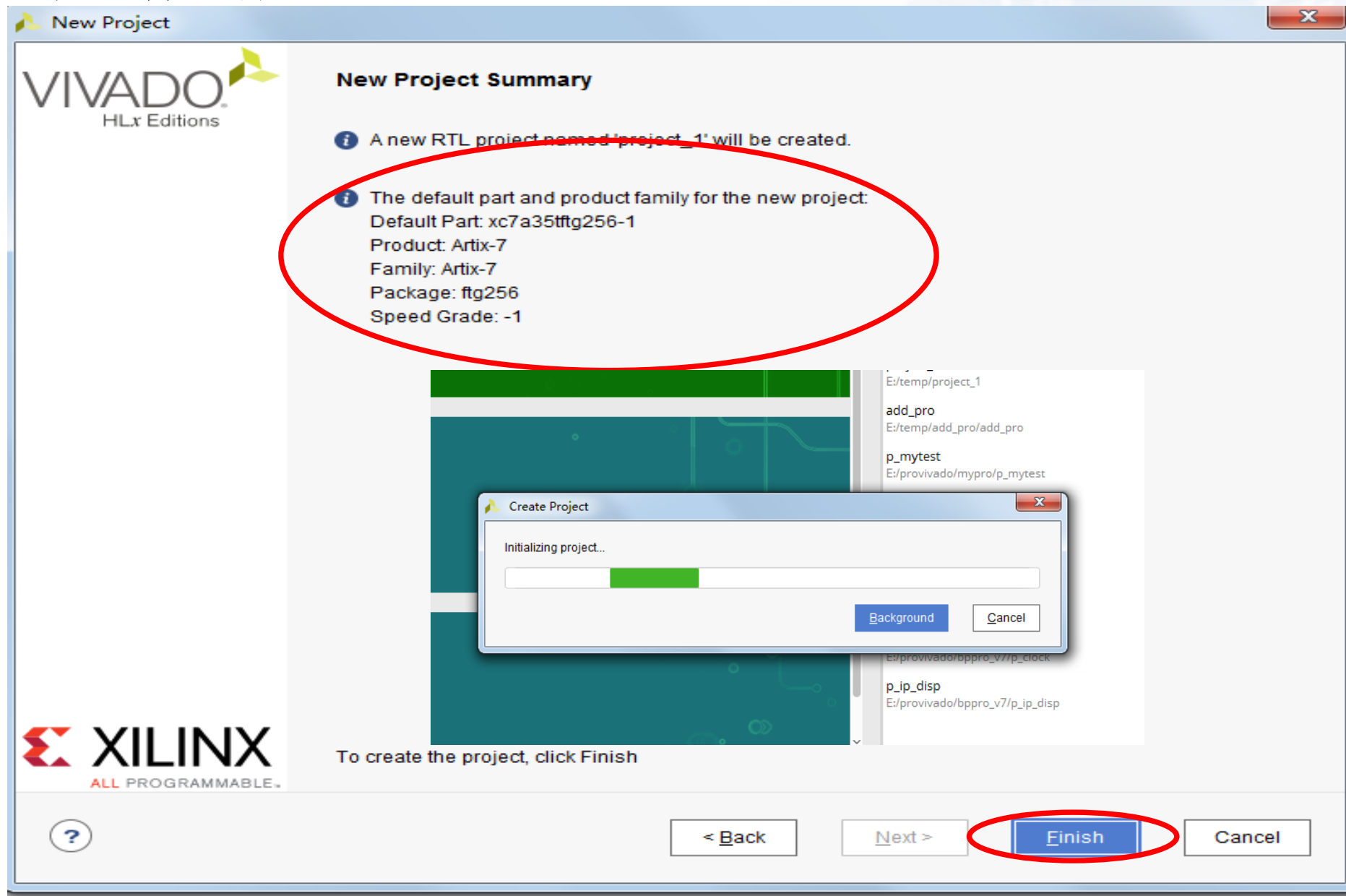
Next >

Finish

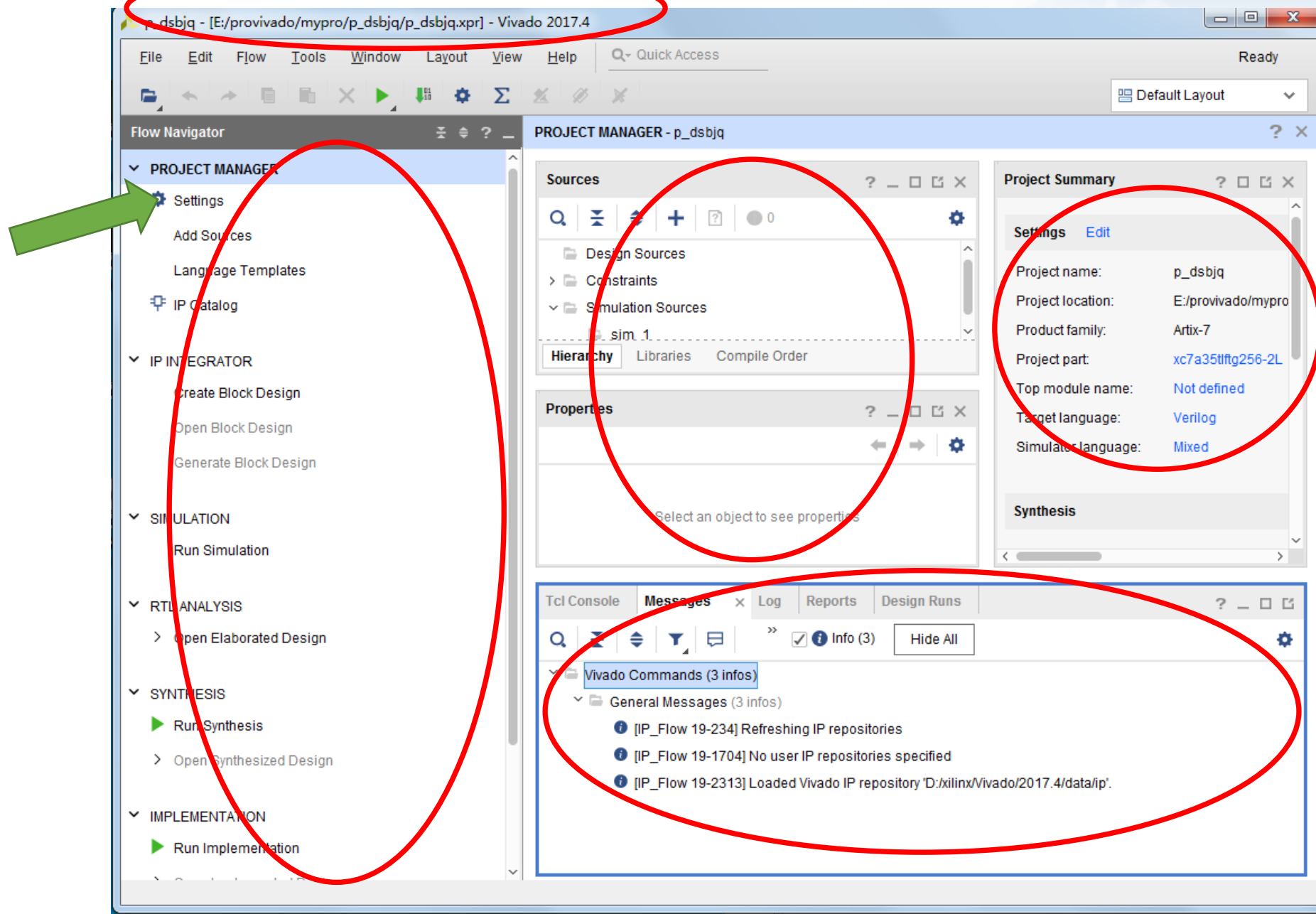
Cancel



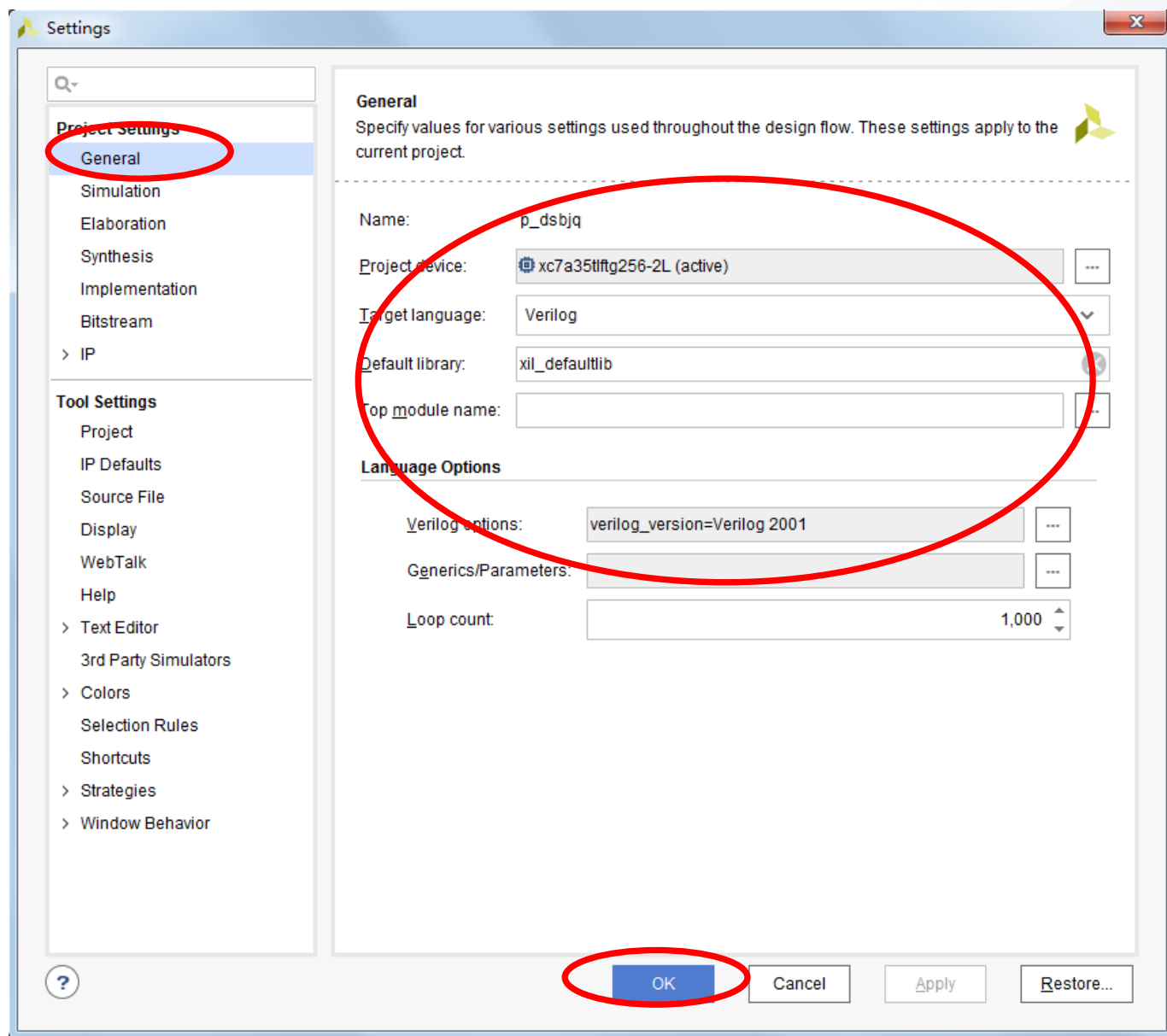
# 工程器件选择



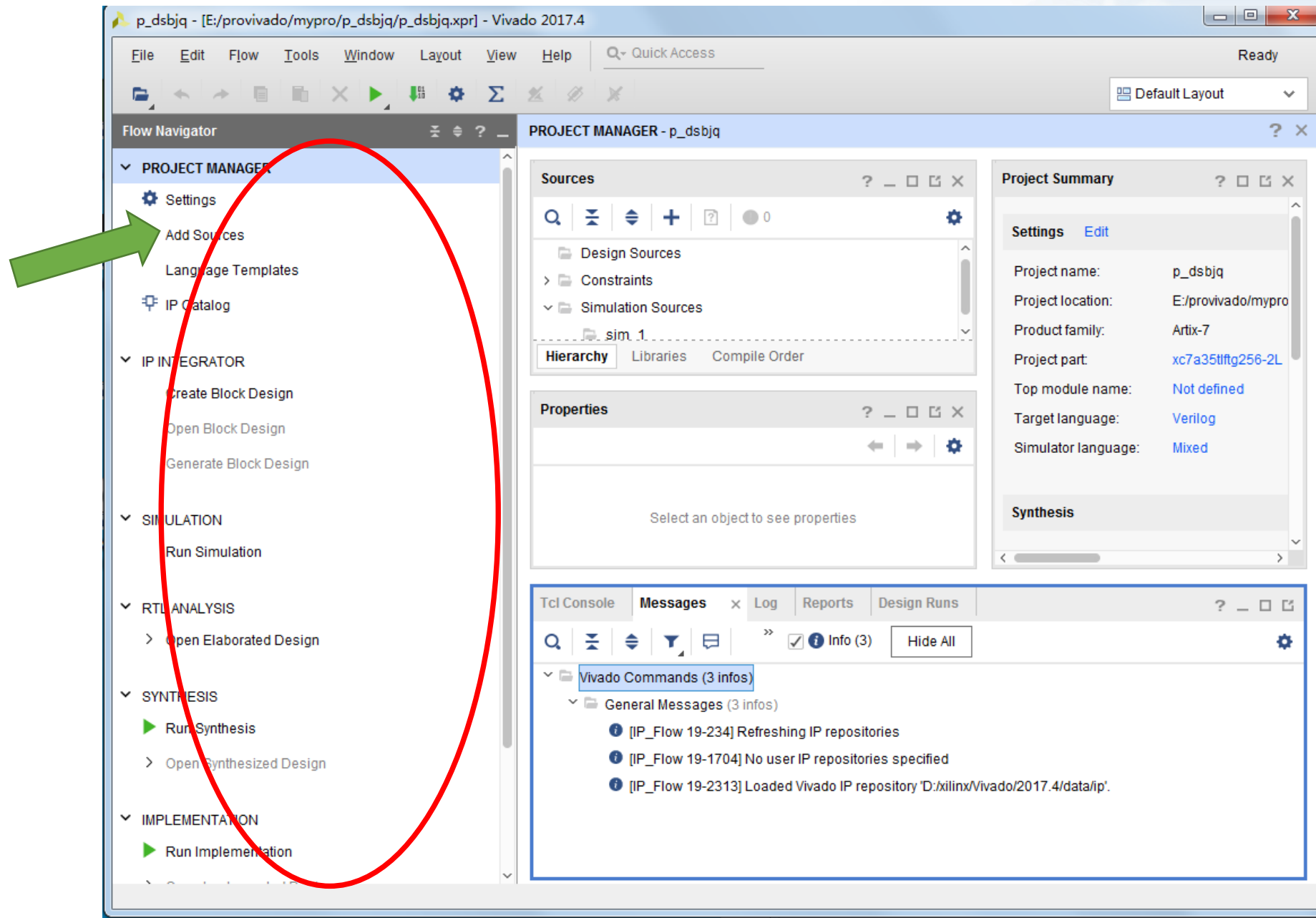
# 创建后的工程



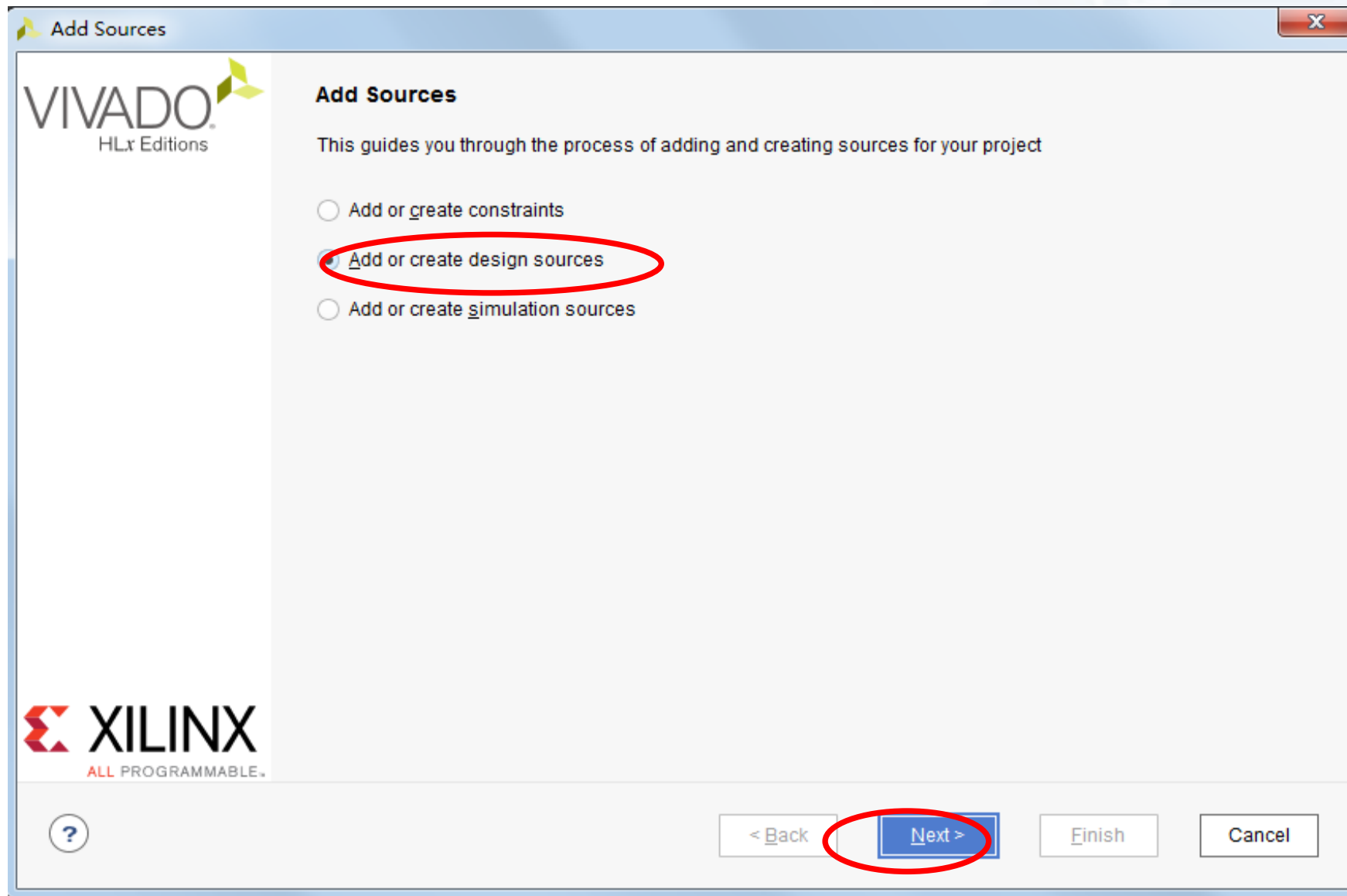
# 工程设置



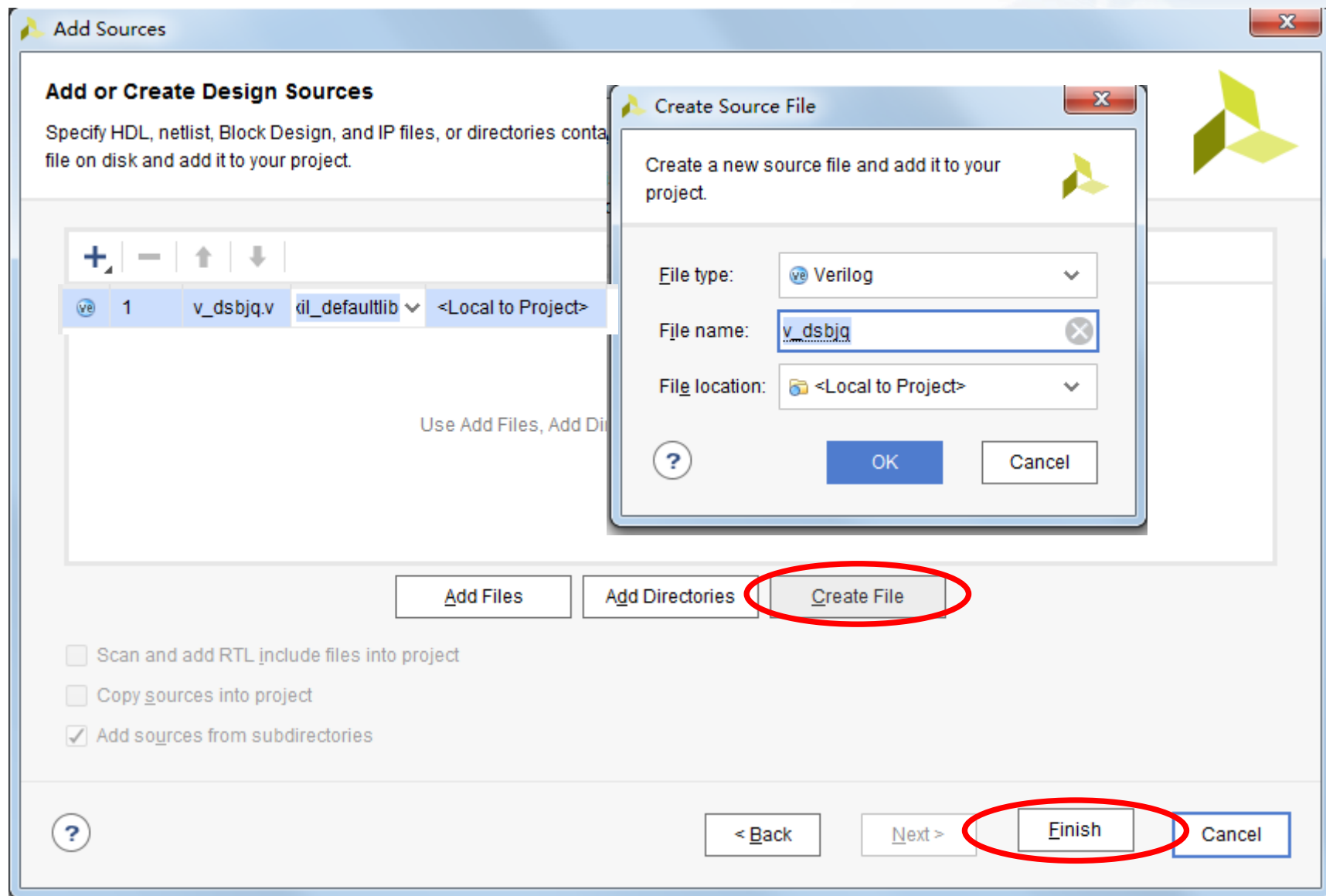
# 添加文件



## 添加文件



# 点击创建文件



## 定义模块

**Define Module**

Define a module and specify I/O Ports to add to your source file.  
For each port specified:  
MSB and LSB values will be ignored unless its Bus column is checked.  
Ports with blank names will not be written.

**Module Definition**

Module name:

**I/O Port Definitions**

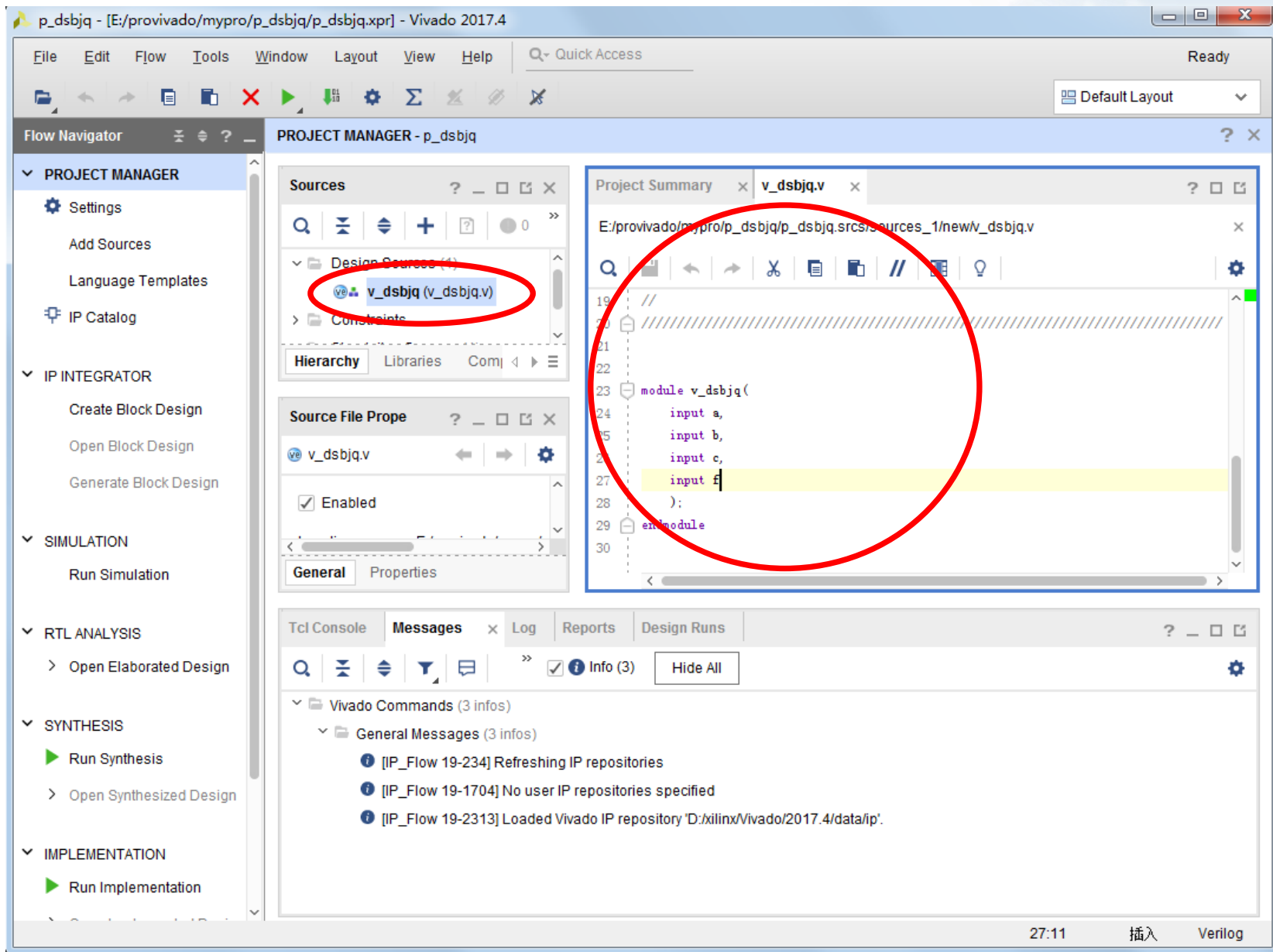
Port Name	Direction	Bus	MSB	LSB
b	input	<input type="checkbox"/>	0	0
c	input	<input type="checkbox"/>	0	0
f	input	<input type="checkbox"/>	0	0

Direction dropdown menu options: input, output, inout

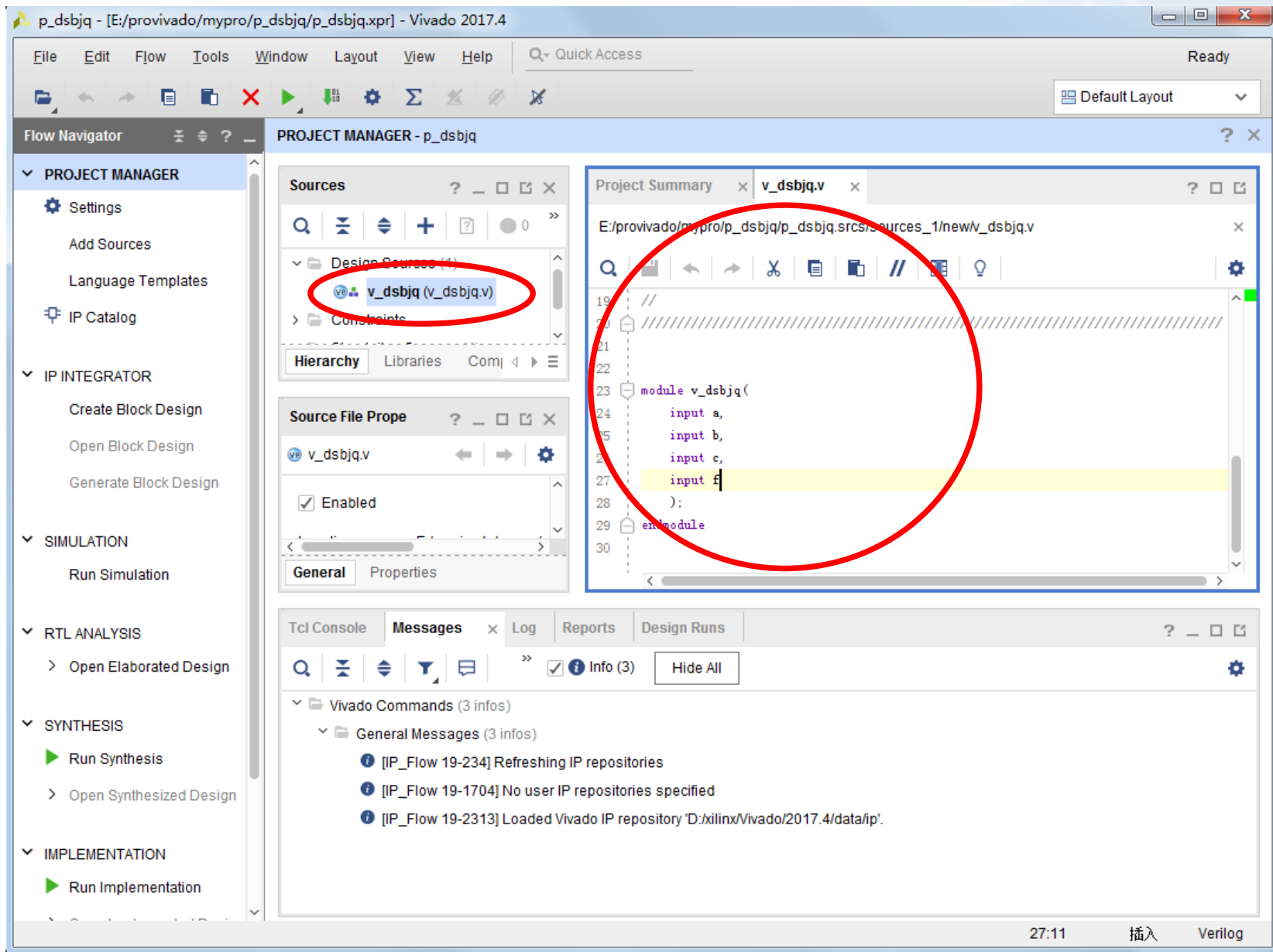
**OK** **Cancel**



# 编辑源文件



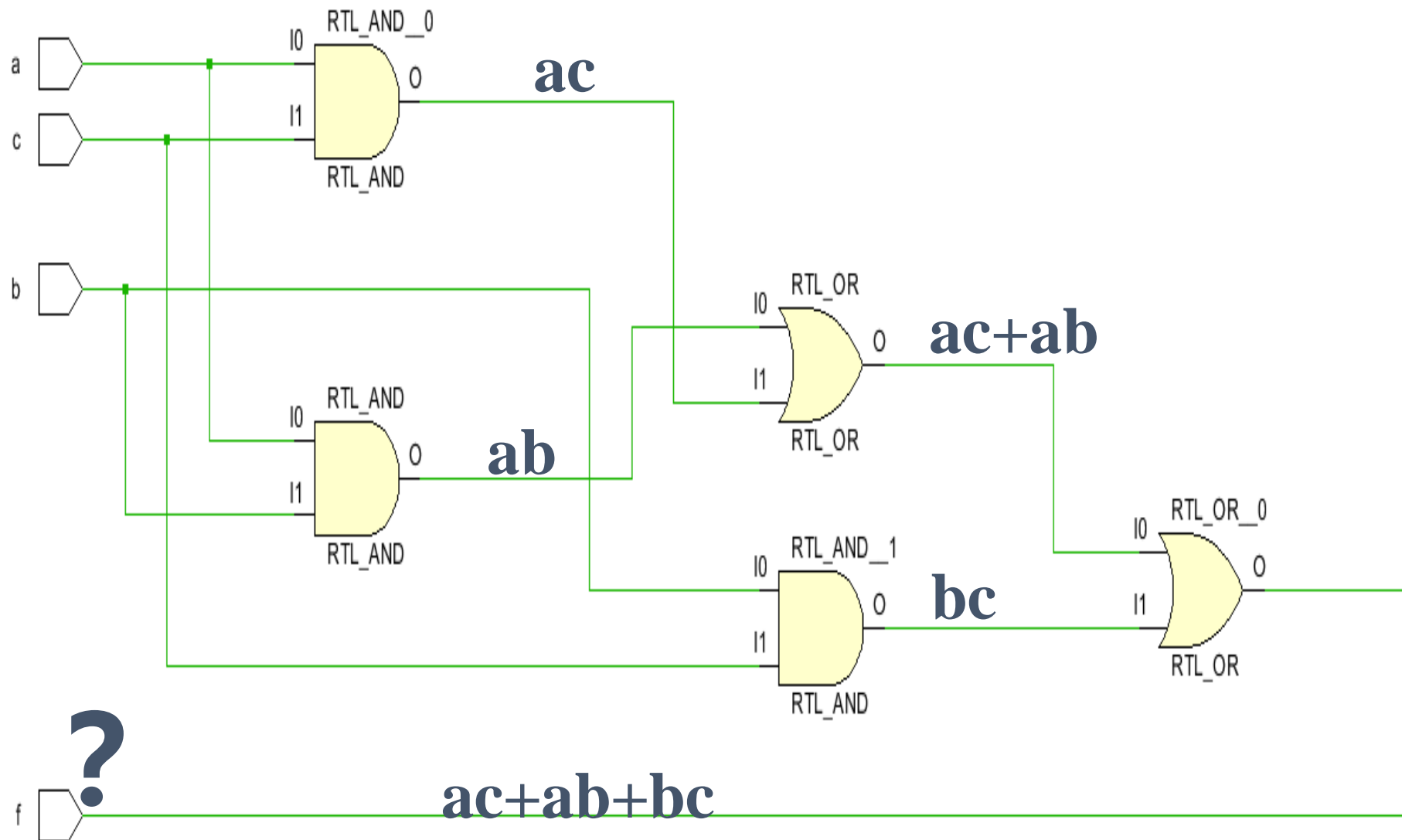
# 编辑源文件



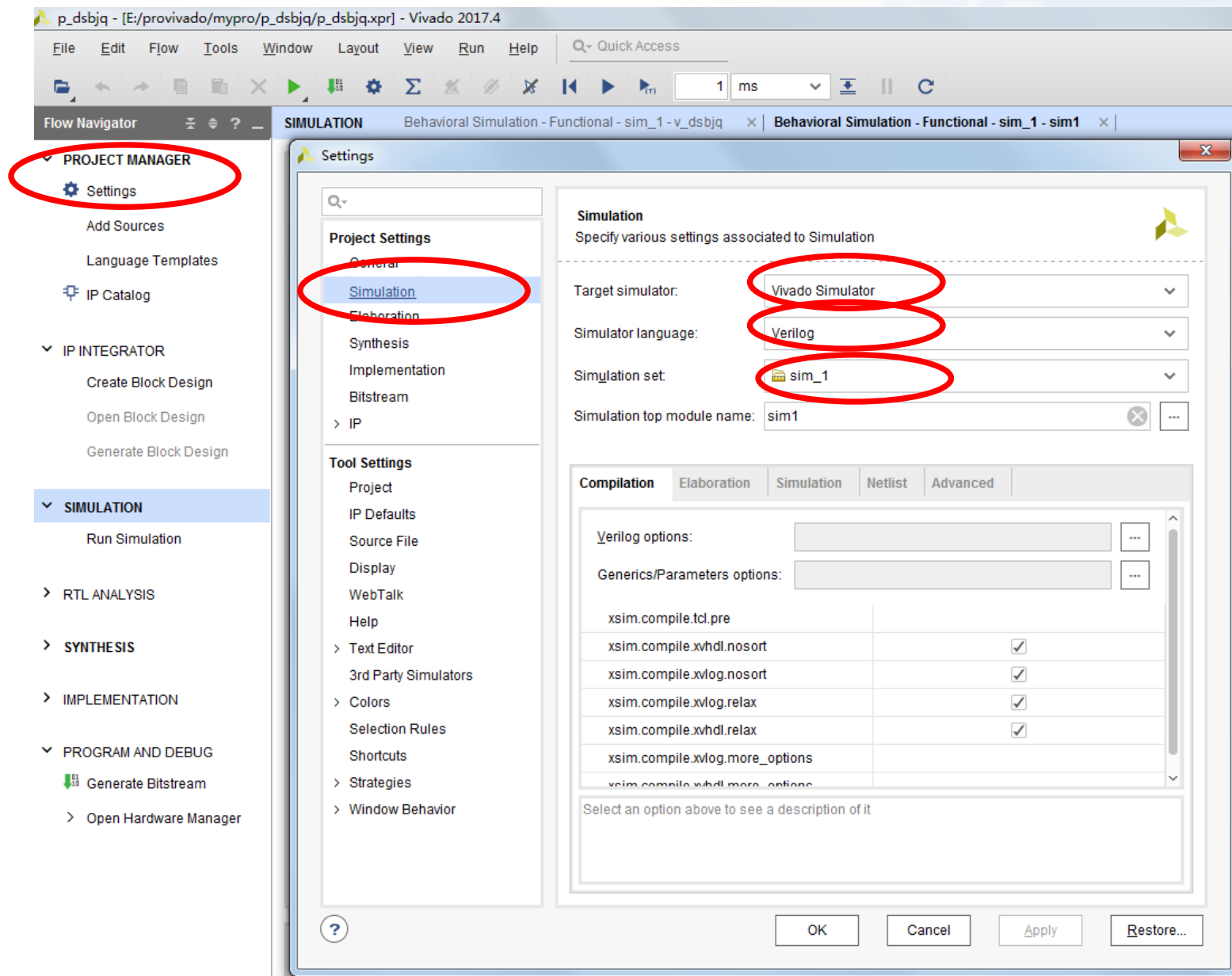
## ■ 编辑源代码

```
■ module v_dsbjq(  
  ■ input a,  
  ■ input b,  
  ■ input c,  
  ■ input f  
  ■ );  
  ■ assign f=a&b | a&c | b&c; //f=ab+ac+bc  
  ■ endmodule
```

# RTL分析



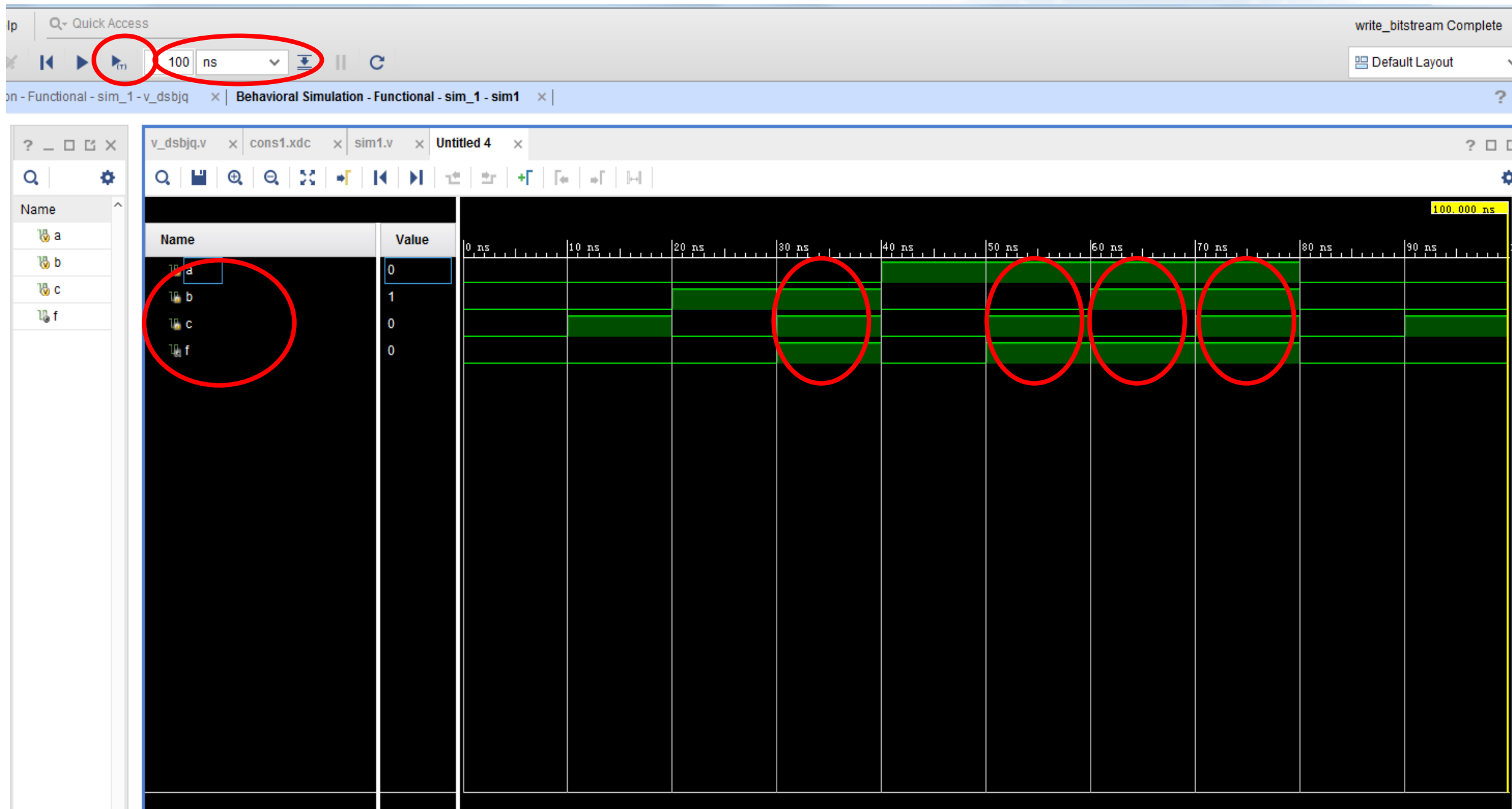
## ■ 设置工程的仿真属性



# 加入仿真文件

```
■ `timescale 1ns / 1ps
■ module sim1;
■   reg a,b,c;
■   wire f;
■   v_dsbjq uut(a,b,c,f );
■   initial begin
■       a=0;b=0;c=0;
■   end
■   always #10 {a,b,c}={a,b,c}+1;
■ endmodule
```

## 运行仿真





## ■ 加入约束文件

■ ## Switches

要改用xc7a35tcpg236-1的引脚! 见下页

■ set\_property PACKAGE\_PIN F3 [get\_ports a]

■ set\_property IOSTANDARD LVCMOS33 [get\_ports a]

■ set\_property PACKAGE\_PIN H4 [get\_ports b]

■ set\_property IOSTANDARD LVCMOS33 [get\_ports b]  
xc7a35tcpg236-1

■ set\_property PACKAGE\_PIN N4 [get\_ports c]

■ set\_property IOSTANDARD LVCMOS33 [get\_ports c]

■

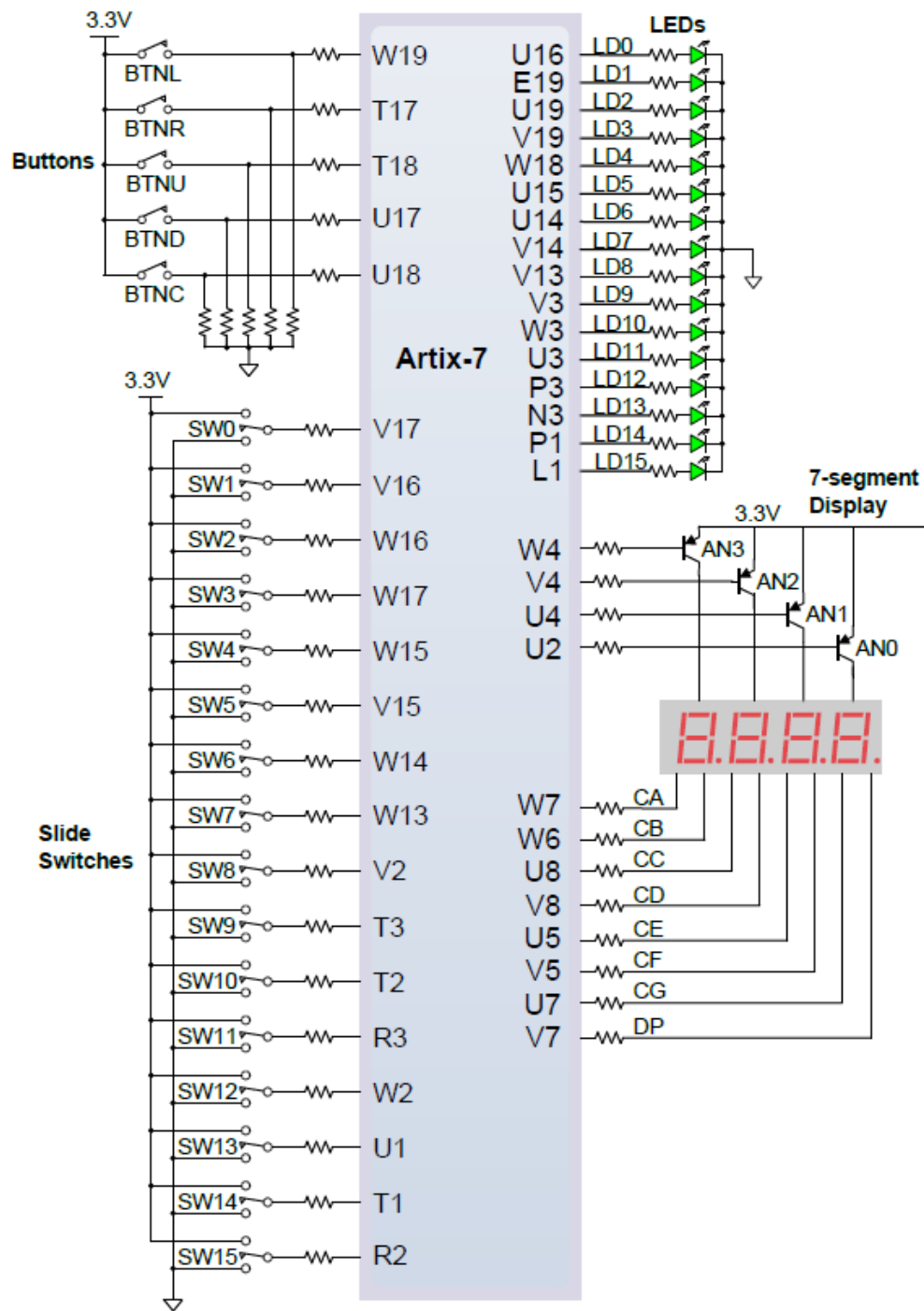
■ ## led

■ set\_property PACKAGE\_PIN E3 [get\_ports f]

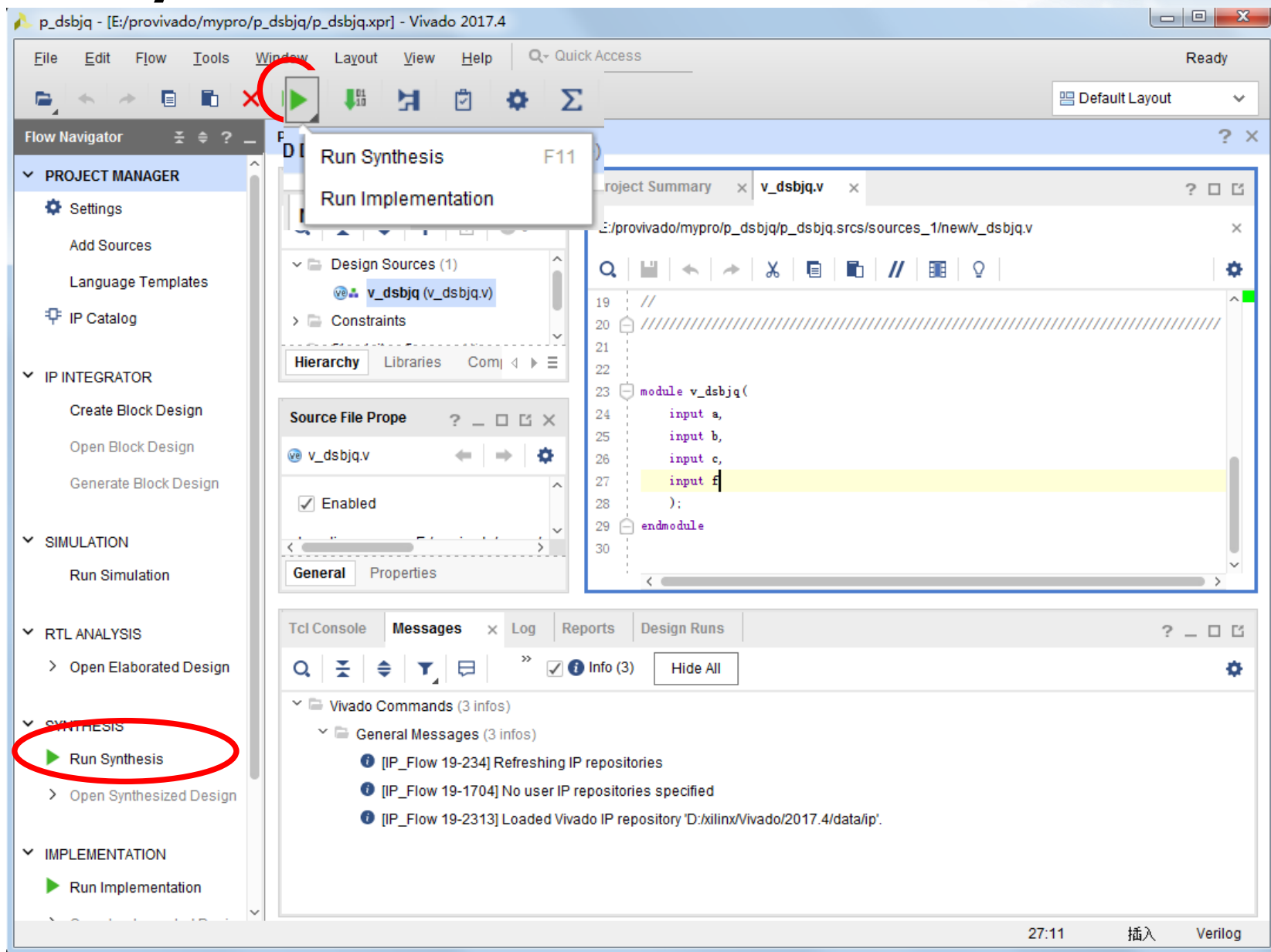
■ set\_property IOSTANDARD LVCMOS33 [get\_ports f]

# 外围设备

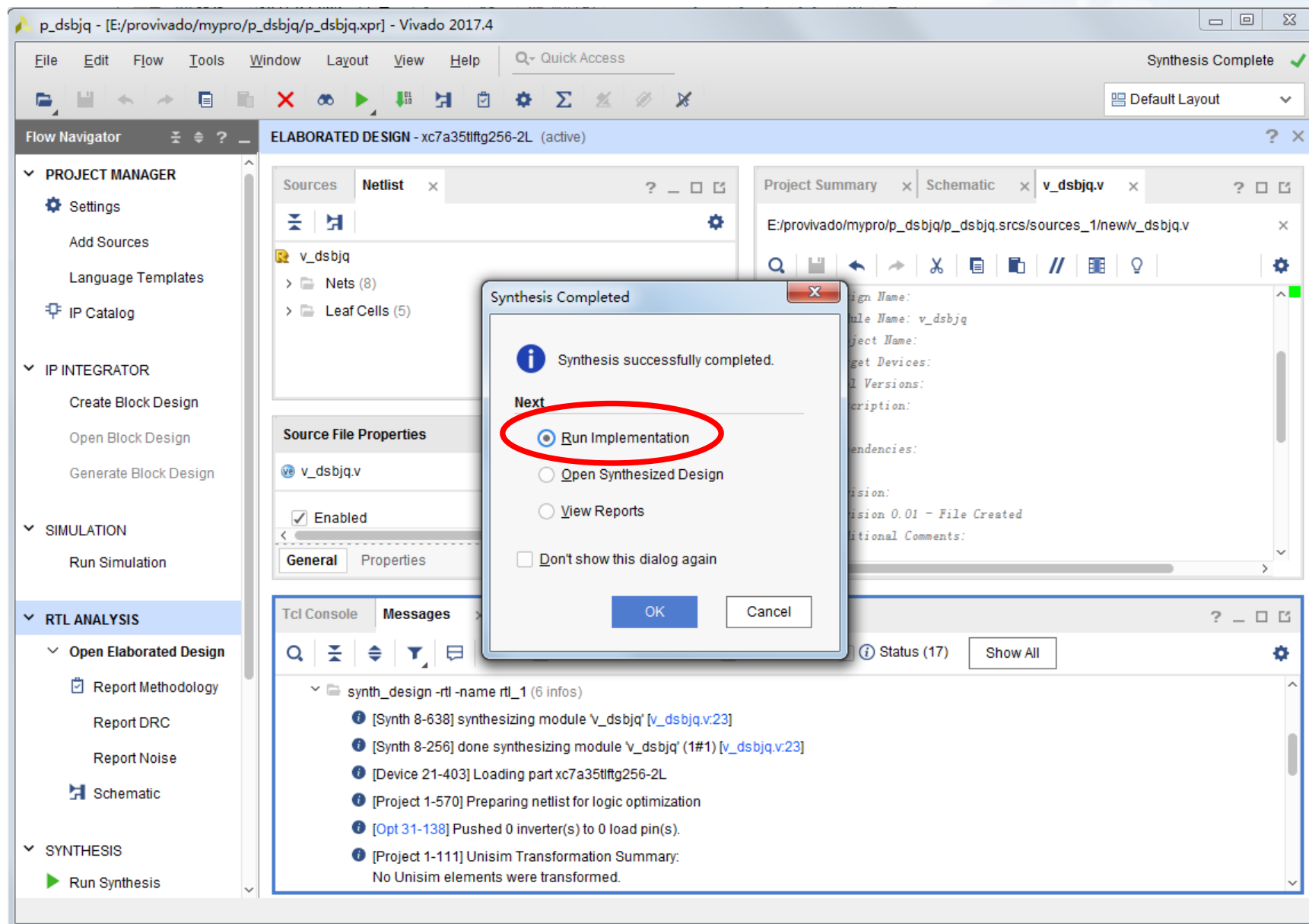
xc7a35tcpg236-1的引脚



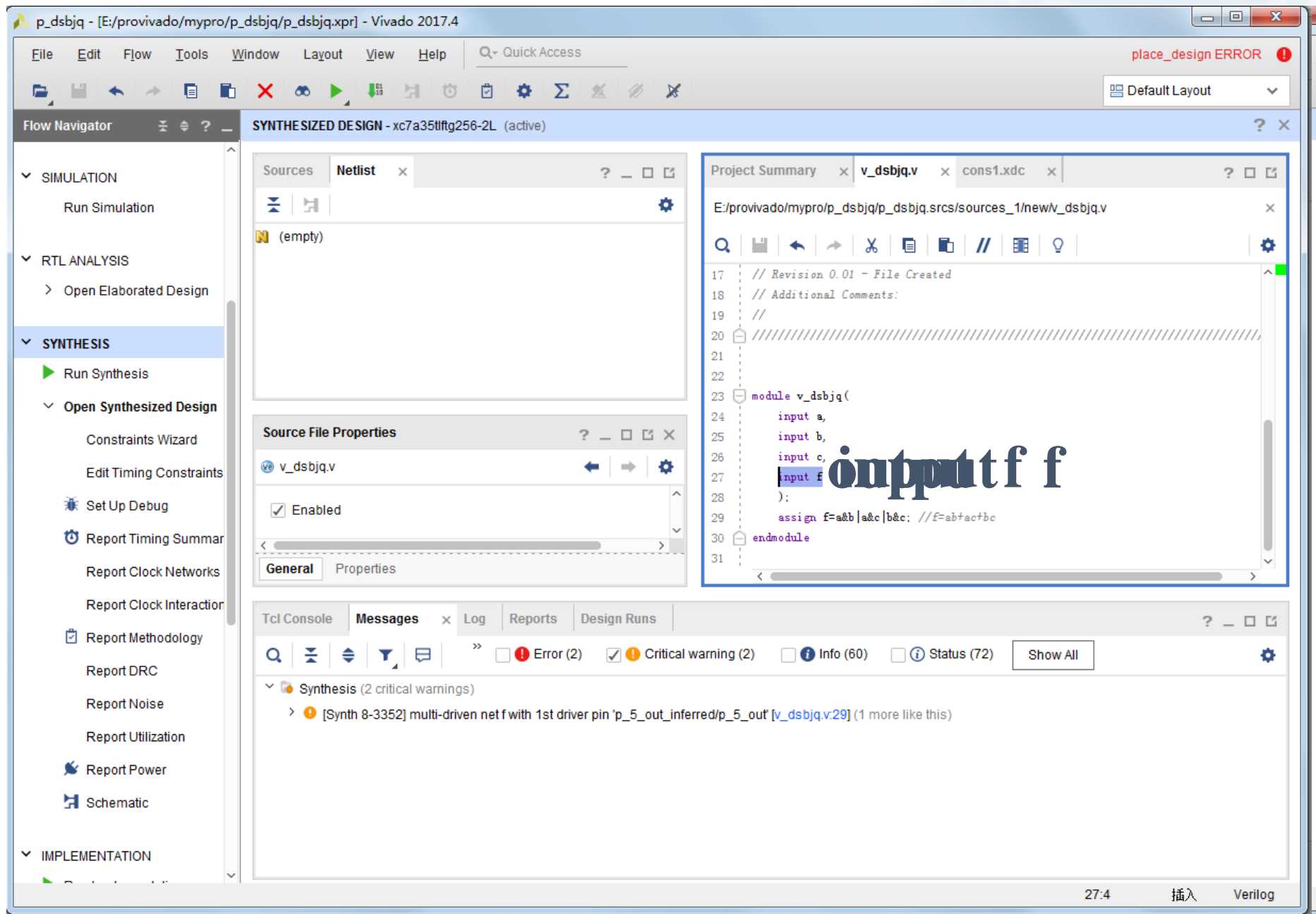
# 综合Synthesis



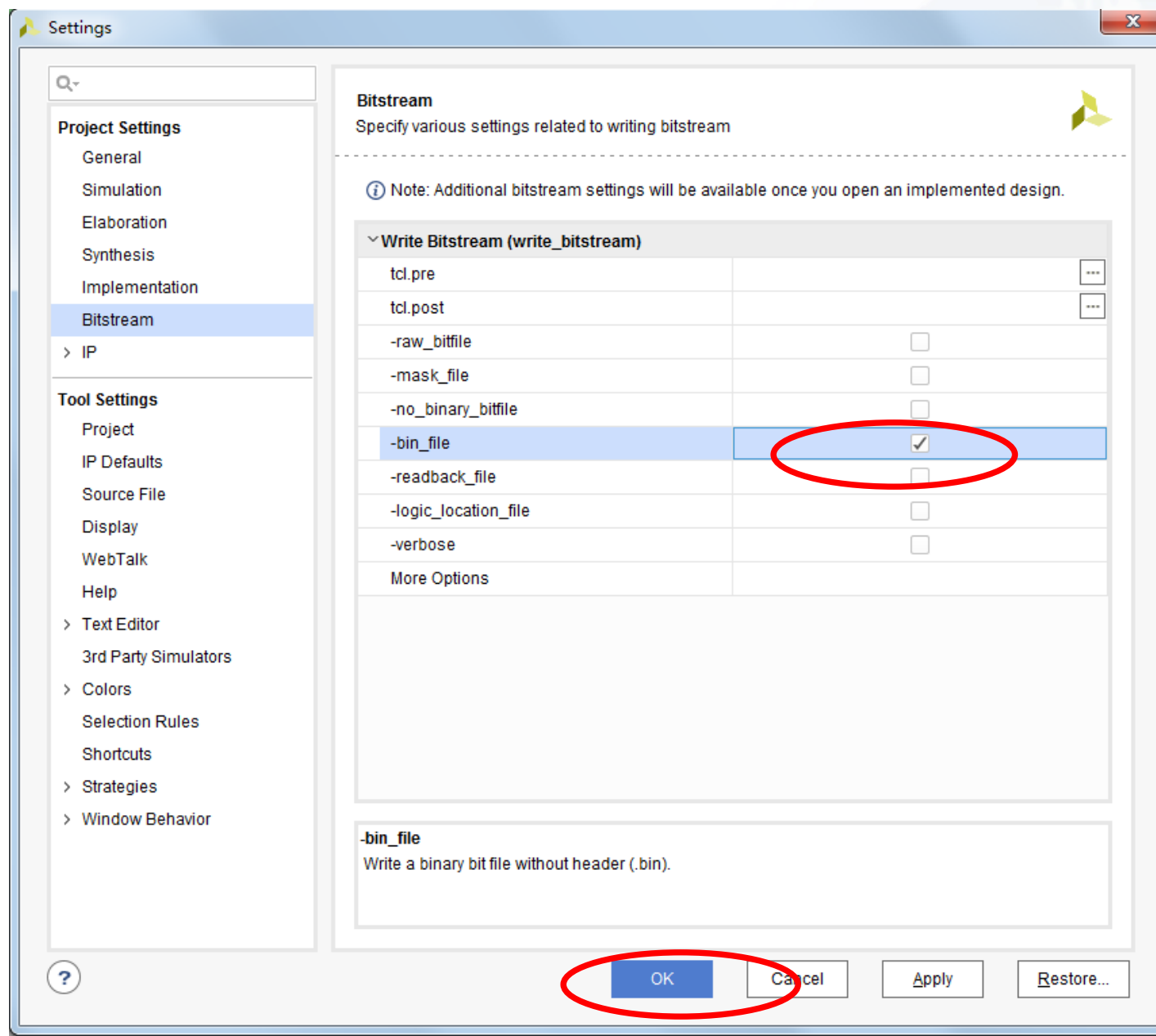
# 实现Implementation



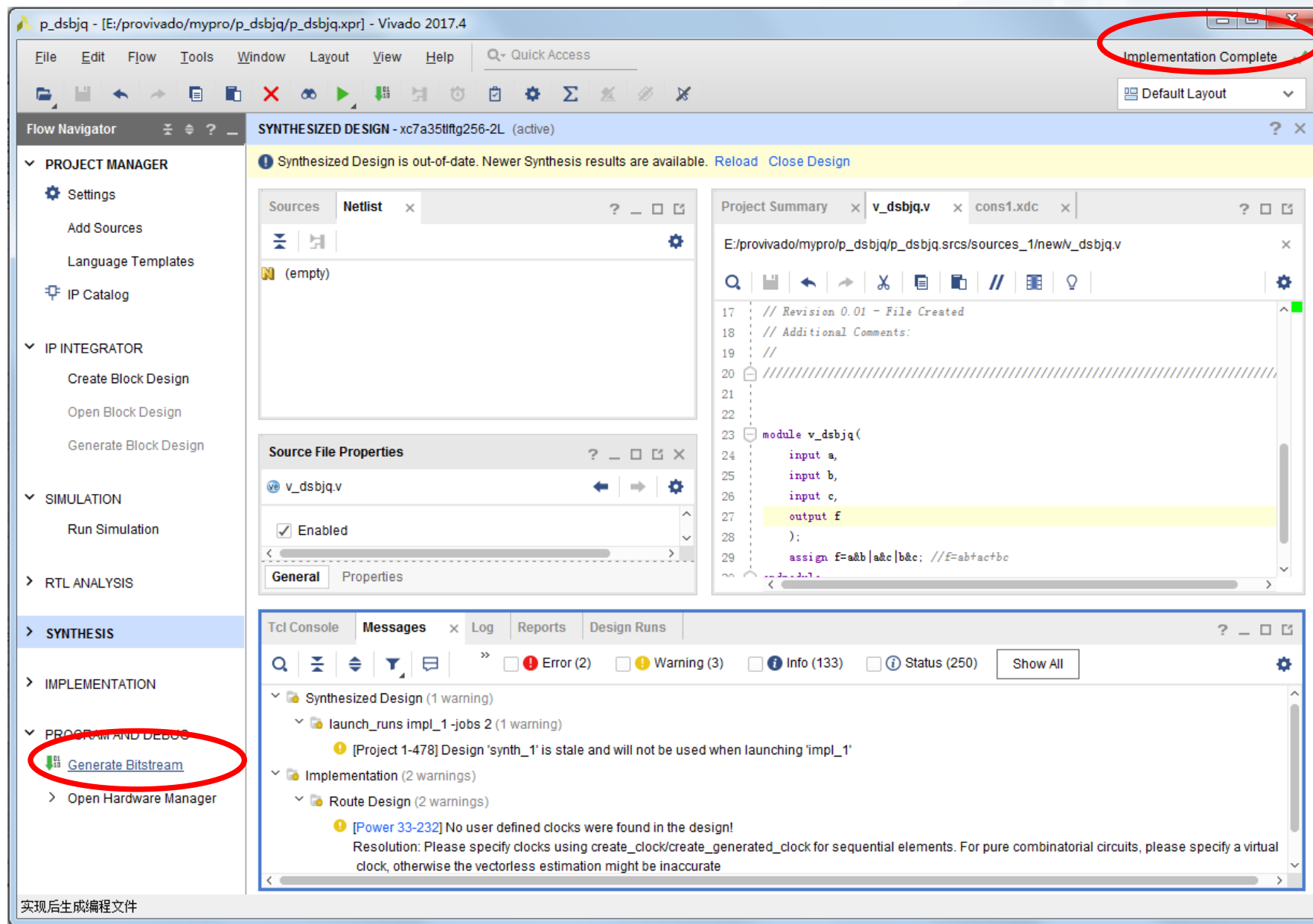
# 实现Implementation



# 生成比特流文件



# 生成比特流文件

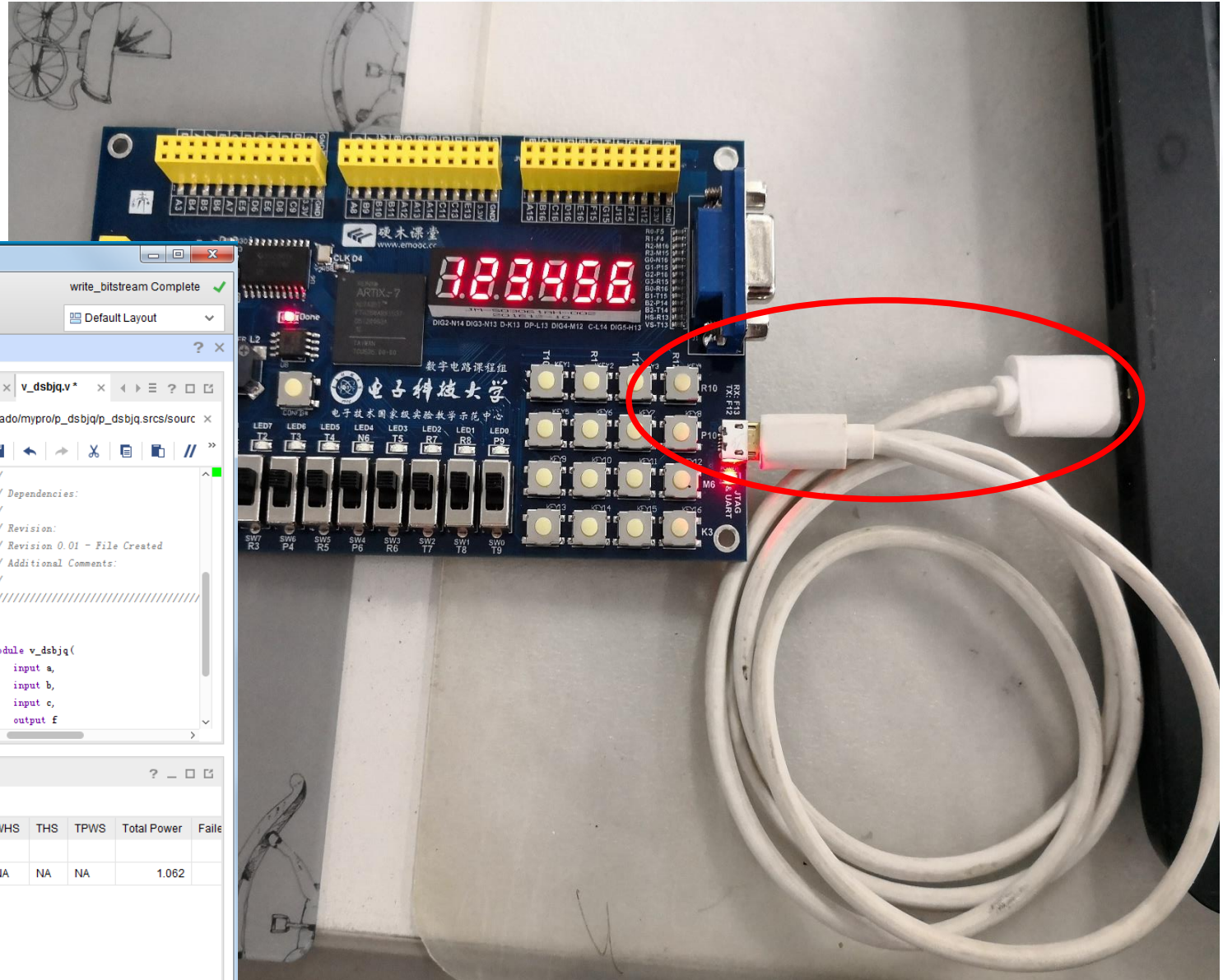
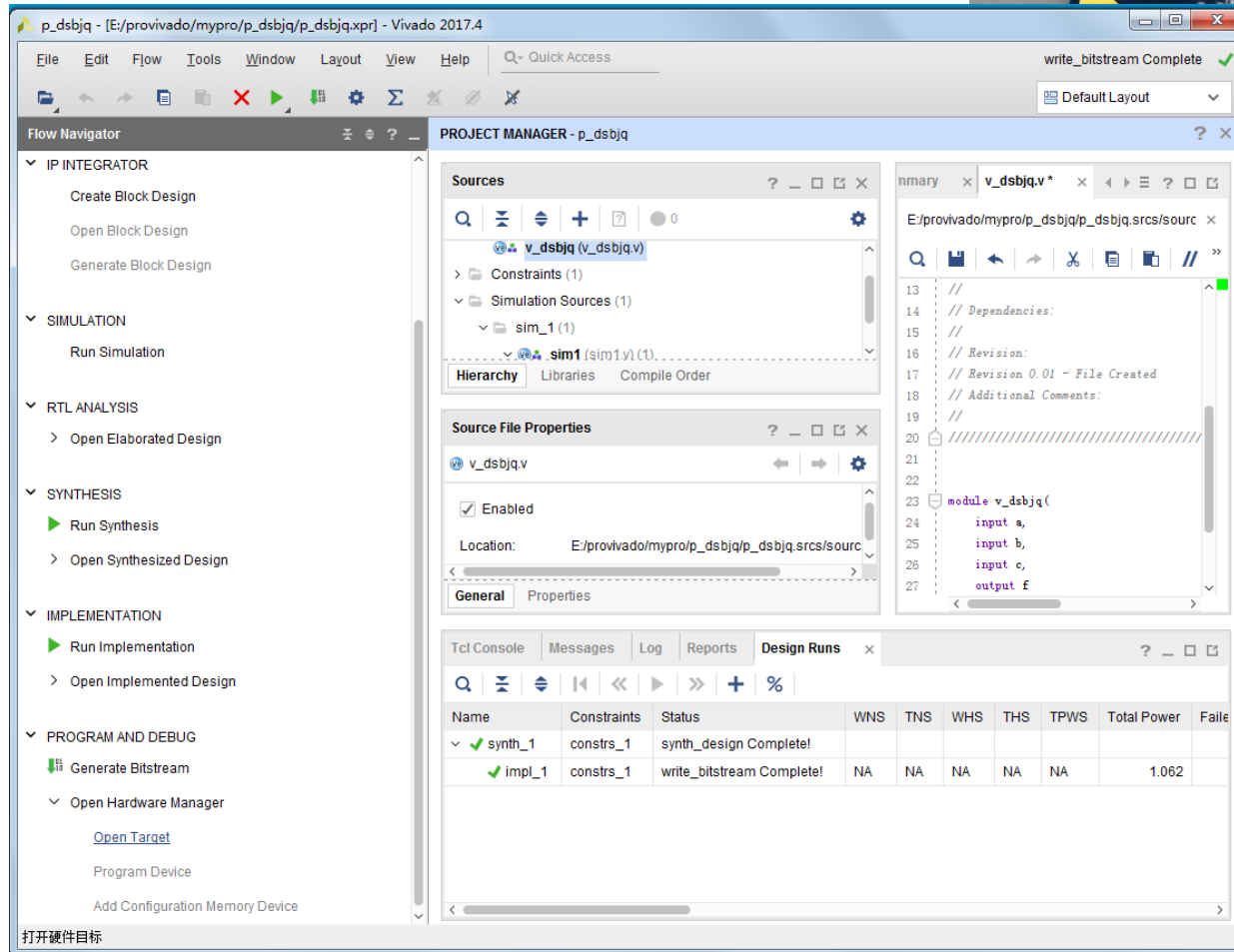




# 连接实验板

连接实验板到计算机。

在**Vivado**下打开硬件管理器。



# 使用硬件管理器连接硬件 open target

p\_dsbjq - [E:/provivado/mypro/p\_dsbjq/p\_dsbjq.xpr] - Vivado 2017.4

File Edit Flow Tools Window Layout View Help Quick Access

write\_bitstream Complete ✓

Default Layout

Flow Navigator

- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG**
  - Generate Bitstream
  - Open Hardware Manager
    - Open Target
    - Program Device
    - Add Configuration Memory Device

PROJECT MANAGER - p\_dsbjq

Sources

- v\_dsbjq (v\_dsbjq.v)
- Constraints (1)
- Simulation Sources (1)
  - sim\_1 (1)
- sim1 (sim1.v) (1)

Hierarchy Libraries Compile Order

Source File Properties

v\_dsbjq.v

Enabled

Location: E:/provivado/mypro/p\_dsbjq/p\_dsbjq.srscs/sourc

General Properties

primary x v\_dsbjq.v\* x

E:/provivado/mypro/p\_dsbjq/p\_dsbjq.srscs/sourc

```
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21
22
23 module v_dsbjq(
24     input a,
25     input b,
26     input c,
27     output f
```

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed
✓ synth_1	constrs_1	synth_design Complete!							
✓ impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	1.062	

打开硬件目标

# 使用硬件管理器连接硬件 auto connect

The screenshot displays the Vivado 2017.4 IDE interface. The **Flow Navigator** on the left has the **PROGRAM AND DEBUG** section expanded, with **Program Device** circled in red. The **HARDWARE MANAGER** window in the center shows a table of hardware components, also circled in red:

Name	Status
localhost (1)	Connected
xilinx_tcf/Xilinx/3455445I A (1)	Open
xc7a35t_0 (1)	Programmed
XADC (System Monitor)	

Below the table is a **Properties** section. The bottom status bar shows tabs for **Synthesis**, **Implementation**, and **Simulation**. The **Tcl Console** at the bottom displays the following log messages:

```
synth_design: Time (s): cpu = 00:00:40 ; elapsed = 00:00:48 . Memory (MB): peak = 758.668 ; gain = 485.031
INFO: [Common 17-1381] The checkpoint 'E:/provivado/mypro/p_dsbjq/p_dsbjq.runs/synth_1/v_dsbjq.dcp' has been gener
INFO: [runtcl-4] Executing : report_utilization -file v_dsbjq_utilization_synth.rpt -pb v_dsbjq_utilization_synth
report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.087 . Memory (MB): peak = 758.668 ; gain = 0.000
INFO: [Common 17-206] Exiting Vivado at Tue Mar 6 16:30:16 2018...
```

# 使用硬件管理器 auto connect

The screenshot shows the Vivado 2017.4 interface. The 'Hardware Manager' window is open, displaying a table of hardware components. A red circle highlights the 'Program Device' button in the bottom left corner of the Hardware Manager window. Another red circle highlights the 'Program device' link in the top status bar of the Hardware Manager window. The table shows the following components:

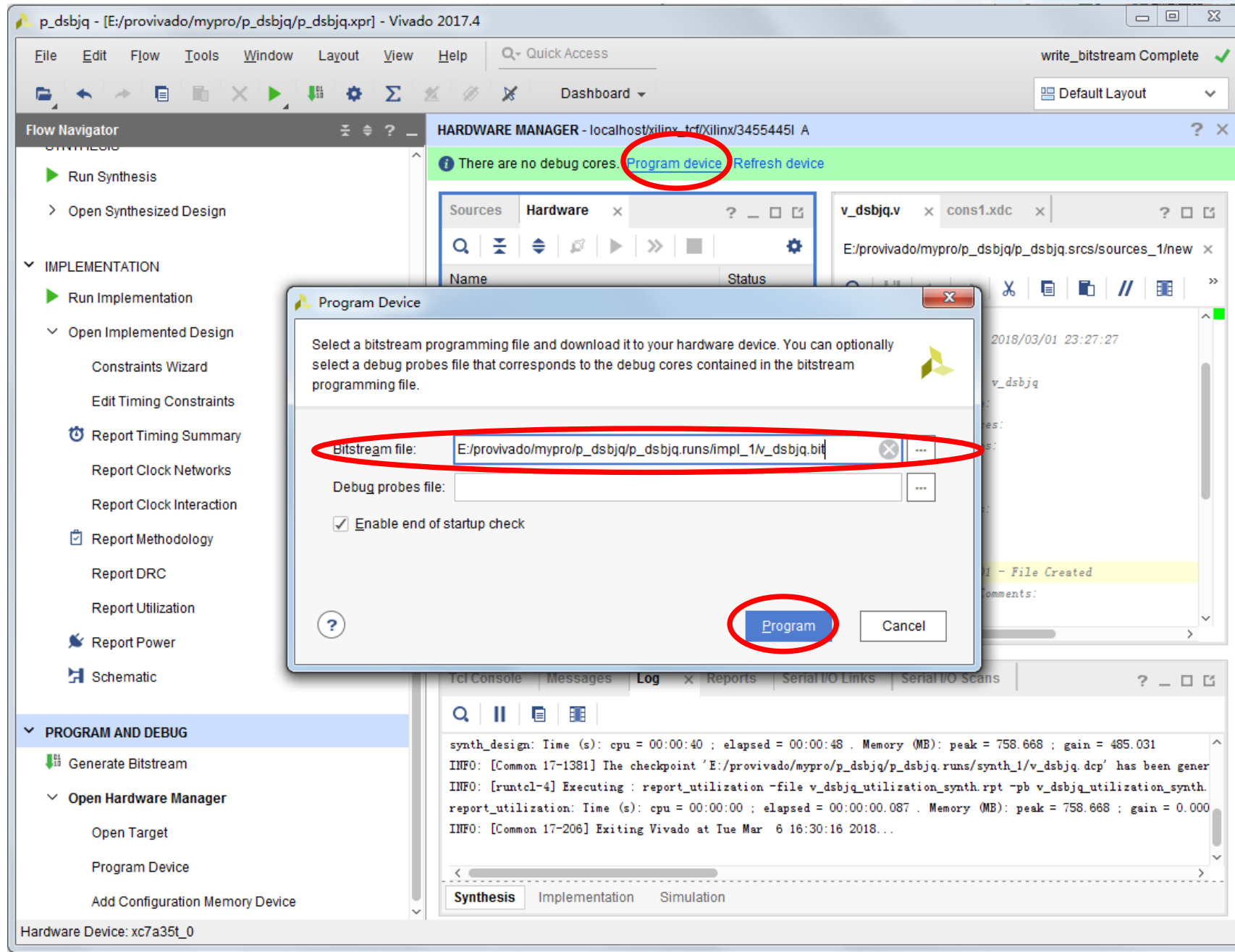
Name	Status
localhost (1)	Connected
xilinx_tcf/Xilinx/3455445I A (1)	Open
xc7a35t_0 (1)	Programmed
XADC (System Monitor)	

The 'Properties' window is open, showing the 'v\_dsbjq.v' file. The 'Tcl Console' window is also open, displaying the following log messages:

```
synth_design: Time (s): cpu = 00:00:40 ; elapsed = 00:00:48 . Memory (MB): peak = 758.668 ; gain = 485.031
INFO: [Common 17-1381] The checkpoint 'E:/provivado/mypro/p_dsbjq/p_dsbjq.runs/synth_1/v_dsbjq.dcp' has been gener
INFO: [runtcl-4] Executing : report_utilization -file v_dsbjq_utilization_synth.rpt -pb v_dsbjq_utilization_synth
report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.087 . Memory (MB): peak = 758.668 ; gain = 0.000
INFO: [Common 17-206] Exiting Vivado at Tue Mar 6 16:30:16 2018...
```



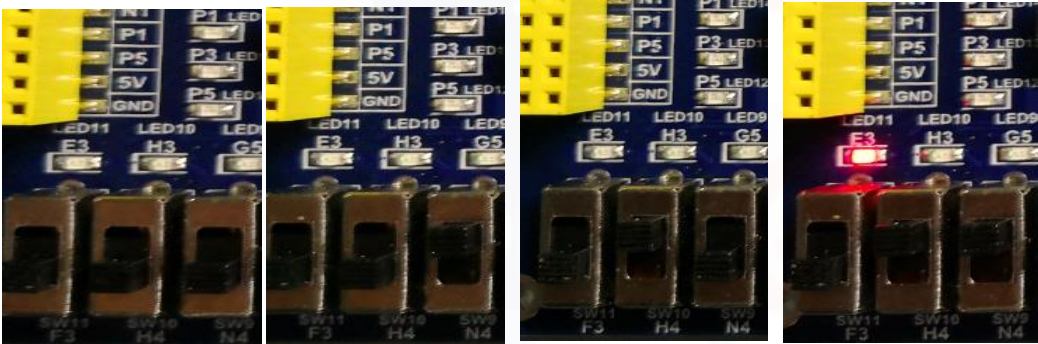
# 使用硬件管理器 Program Device



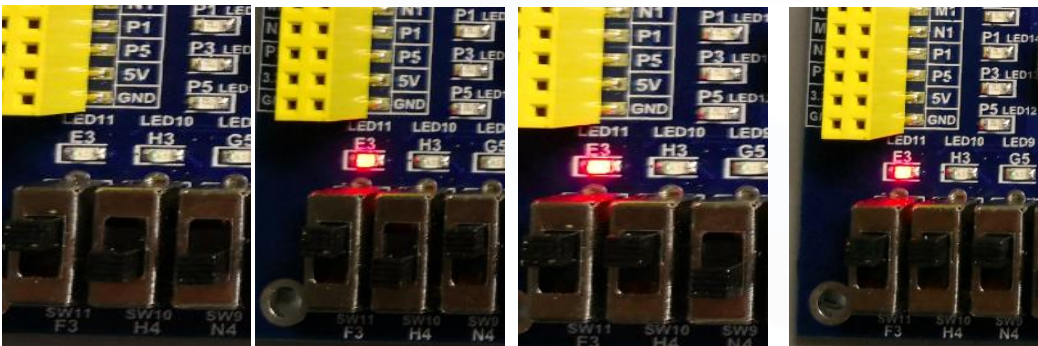
运行效果

a	b	c	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

000 001 010 011



100 101 110 111



# 下载到FLASH

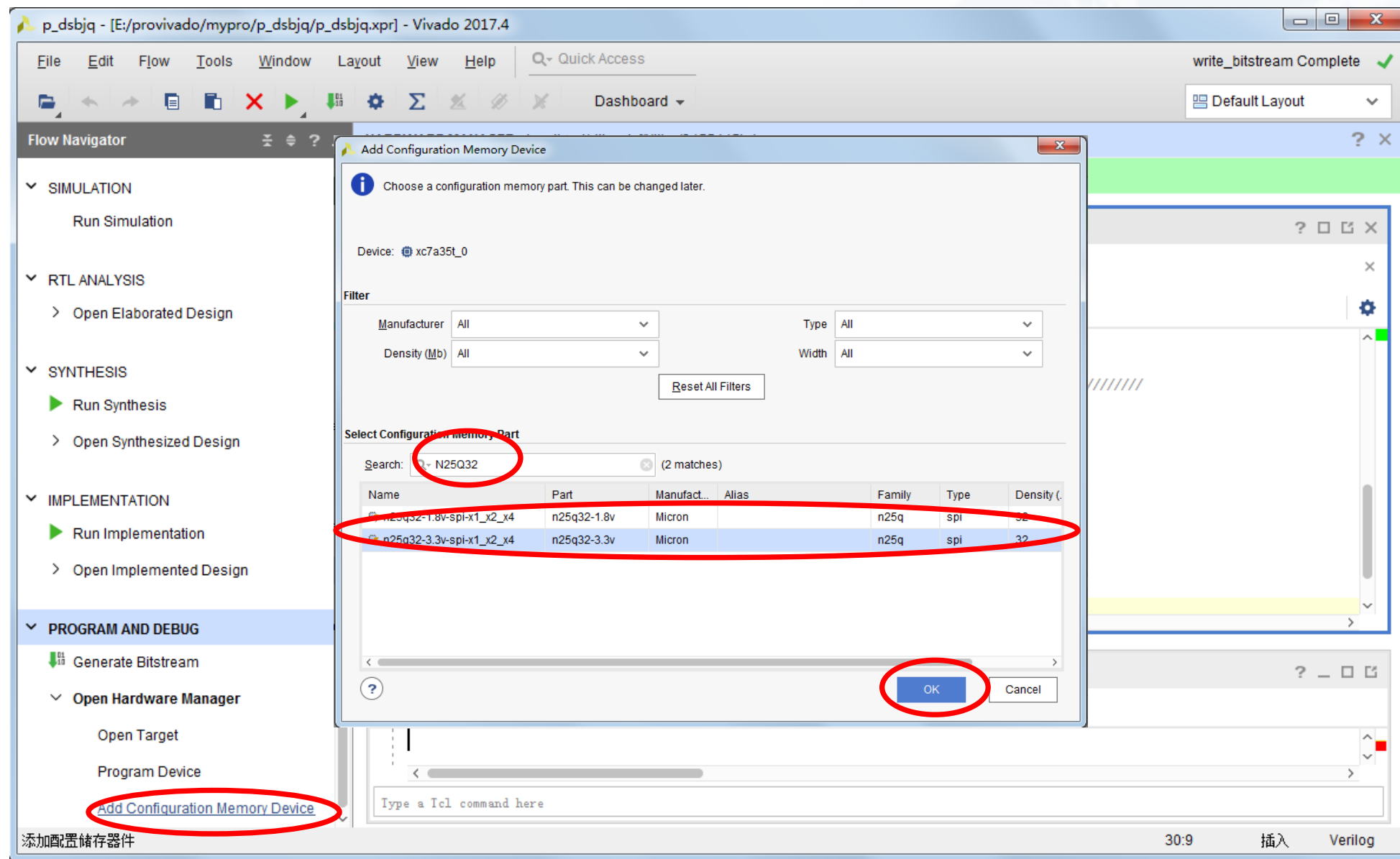
在下载运行后，关闭电路板电源，再打开电源，无论怎么设置拨码开关位置**LED**都不会亮。

这时因为下载采用的是**JTAG**调试模式，只能进行验证，并没有将代码下载到**FLASH**。

要下载到**FLASH**，首先需要加载存储设备。点击流程导航窗口编程和调试 (**Program and Debug**) 项下的增加配置内存设备 (**Add Configuration Memory Device**) 。



# 使用硬件管理器下载到FLASH

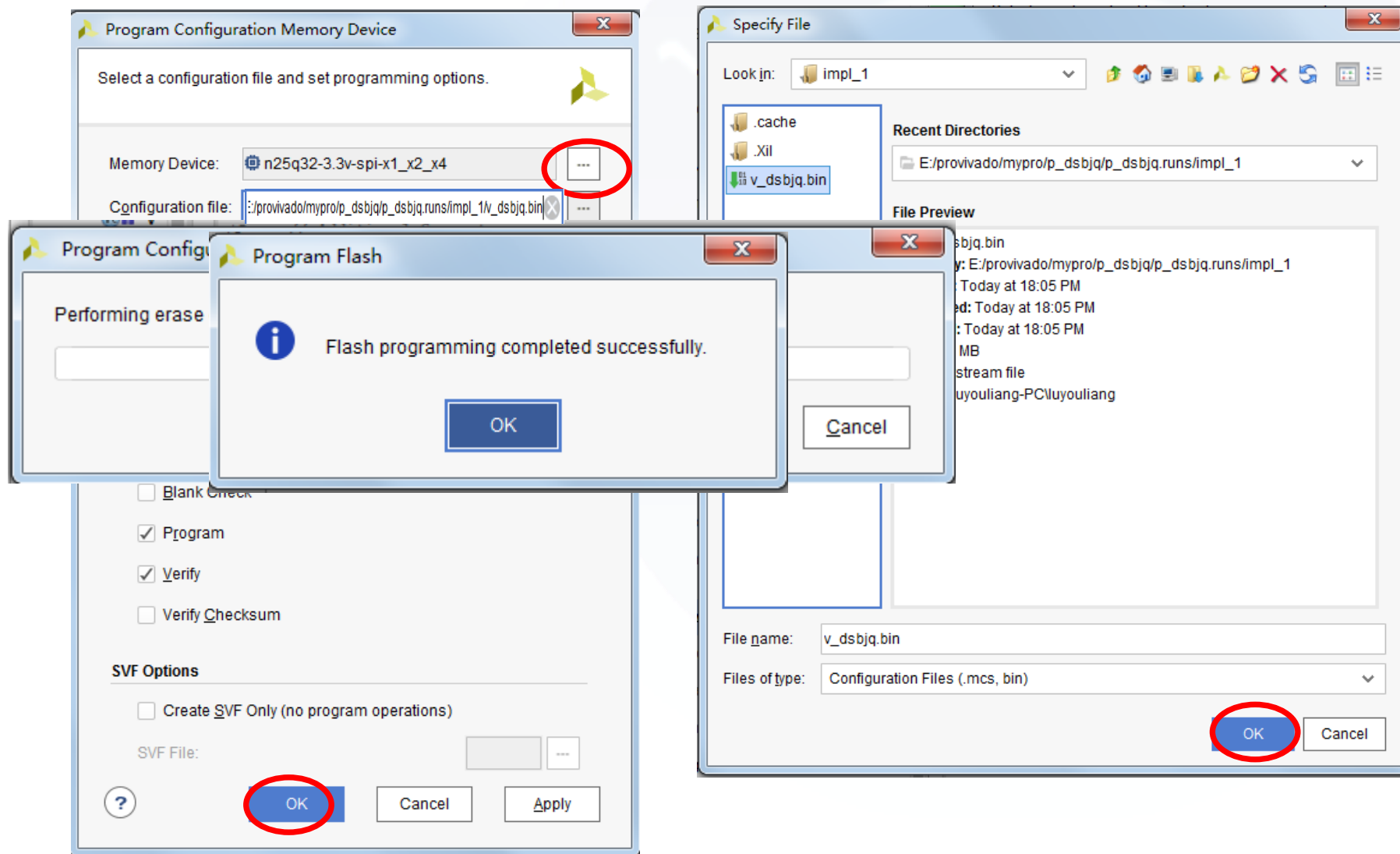


# 下载到FLASH

进入配置存储设备窗口

选择配置文件，注意可以下载到**FLASH**的是**BIN**文件

之后按**OK**进行下载，下载后重启或断电，可以看到芯片已经成功配置。



# 组合逻辑电路与**VIVADO**进阶

- 下一个知识点: 3-8译码器设计和IP核