ICCAD 2014 Contest: Incremental Timing-driven Placement
File formats for Benchmarks and Contest Deliverables
v1.2 – May 14^{th}, 2014

http://cad_contest.ee.ncu.edu.tw/CAD-Contest-at-ICCAD2014/problem_b/default.html

Contents

1 Introduction

The contest will primarily deal with localized set of keywords for each file format, both for input and output. It will also provide a more detailed explanation of the evaluation script.

2 Input Files: Benchmarks

Each benchmark is comprised of a set of five (5) files with the following extensions: (*i*) `.iccad2014`, (*ii*) `.v`, (*iii*) `.lef`, (*iv*) `.def`, and (*v*) `.sdc`.

2.1 .iccad2014 (wrapper)

This file contains the list/location of the other four files needed for benchmark parsing:

```
simple.v simple.lef techlib.def simple.sdc
```

It is used as the only input file when loading the benchmark, e.g., for the evaluation script and for your binary. The order of the file names is not important, e.g.,

```
simple.v simple.sdc techlib.def simple.lef
```

is the same as the above. Each contained filename will have the same directory path location as the `.iccad2014` file. That is, if the call to load the above `.iccad2014` file is

```
%> myPlacer ../simple/simple.iccad2014
```

then the four filenames in `simple.iccad2014` will have the same directory path:

```
../simple/simple.v
../simple/simple.lef
../simple/techlib.def
../simple/simple.sdc
```

2.2 .v (verilog)

The verilog file specifies the top-level hierarchy of the design. For this contest, we will be using a small set of keywords with the verilog language. If you are implementing your own verilog parser, you will be expected to support the set of keywords found within the `simple.v` file (reproduced below for clarity). The design implemented in `simple.v` corresponds to the design found in Figure 1.

```
01.  module simple (
02.  inp1,
03.  inp2,
04.  iccad_clk,
05.  out
06.  );
07.
08.  // Start PIs
09.  input inp1;
10.  input inp2;
11.  input iccad_clk;
12.
13.  // Start POs
14.  output out;
15.
16.  // Start wires
17.  wire n1;
18.  wire n2;
19.  wire n3;
20.  wire n4;
21.  wire inp1;
22.  wire inp2;
23.  wire iccad_clk;
24.  wire out;
25.
26.  // Start cells
27.  NAND2_X1 u1 ( .A1(inp1), .A2(inp2), .ZN(n1) );
28.  DFF_X1 f1 ( .D(n2), .CK(iccad_clk), .Q(n3) );
29.  INV_X1 u2 ( .A(n3), .ZN(n4) );
30.  INV_X1 u3 ( .A(n4), .ZN(out) );
31.  NOR2_X1 u4 ( .A1(n1), .A2(n3), .ZN(n2) );
32.
33.  endmodule
```

Lines 01 and 33 define the start and end of the specified design with the keywords `module` and `endmodule`. Lines 01-06 specify the input and output connection names of the module (note that the direction is not specified here). Lines 09-11 specify the primary inputs (PIs) of the module with the keyword `input`. These names must match the ones stated with `module` (lines 01-06). Line 14 specifies the primary output (PO) of the module with the keyword `output`. This name must match the one stated with `module` (lines 01-06). Lines 17-24 specify the connections or nets within the module with the keyword `wire`. These connections specify both the external PIs and POs as well as the internal connections between gates (explained further

after lines 27-31). Lines 27-31 specify the cells used in the design, as well as how the cells are connected. Each definition's syntax is

cellName instanceName (*.pinName* (*netName*))

where every *cellName* and *.pinName* should be a specified library file (e.g., `simple.def`), and every *netName* should match one of the specified `wire` statements (lines 17-24). For example, on line 27, a `NAND2_X1`-type cell instance of `u1` is specified, its `A1` pin is fed by primary input `inp1`, its `A2` pin is fed by primary input `inp2`, and its `ZN` pin feeds the internal net `n1`. On line 31, `n1` feeds the `A1` pin of the `NOR2_X1`-type cell instance `u4`.

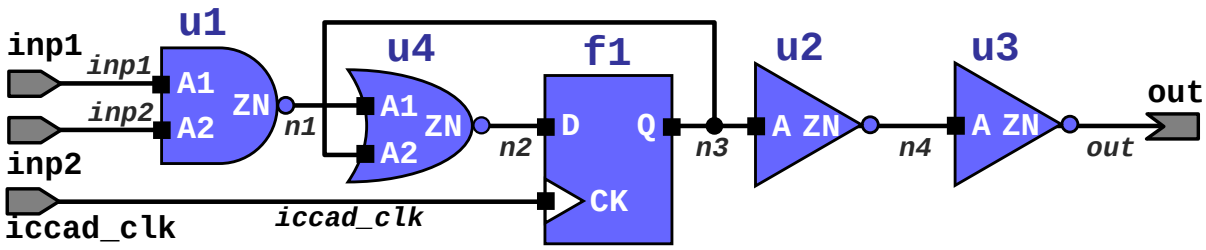

Figure 1: Implementation of `simple.v`.

2.3 .lef (LEF)

The `.lef` file (in Library Exchange Format (LEF) specifies the library definitions of the different cells, metal layers, and placement layout of the design. For this contest, we will be using a very small subset of the keywords in the LEF language. If you are implementing your own parser, you will be expected to support what is defined in `techlib.lef` (in the `simple` benchmark), as well as defined comments beginning with the character '#'. The following explains the general format of the necessary keywords, with snippets of `techlib.lef` reproduced for clarity. The relevant keywords are those listed in the header, as well as **SITE**, **LAYER**, and **MACRO**.

LEF structure. These initial statements are used to set the parsing rules of the LEF file.

```
01.  VERSION 5.5 ;
02.  NAMESCASESENSITIVE ON ;
03.  BUSBITCHARS "[]" ;
04.  DIVIDERCHAR "/" ;
05.
06.  UNITS
07.     DATABASE MICRONS 1000 ;
08.  END UNITS
09.
10.  MANUFACTURINGGRID 0.005 ;
...
99.  END LIBRARY
```

Line 01 specifies the version number of the LEF language used. Line 02 specifies the mode of name parsing. By default, we will assume this to be "ON". Line 03 specifies the special character set used for stating grouped signals e.g., as buses. For instance, `myInputs[31]` specifies that `myInputs` spans 32 bits. For this contest, we will not be defining bus signals (but the keyword may be part of the LEF file). Line 04 specifies the hierarchy divider special character, e.g., `myBox/A` states that pin `A` is contained within the instance `myBox`. Line 06-08 specify the unit conversion from LEF database (distance) units to microns (μm). In this example, every 1000 LEF database units is equivalent to 1 (μm). Line 10 specifies the grid granularity in μm – all shapes' and cells' locations must be snapped to a multiple of that value in the grid. This value must be positive. Line 99 specifies the end of the file.

SITE. Each site defines a placement grouping in the design, i.e., the placement grid for a family of macros and cells. These sites will be used in the keyword **ROW** in the Design Exchange Format (DEF) file (Section 2.4). For this contest, the **SITE** keyword is limited to the following:

```
01.  SITE siteName
02.     CLASS {PAD | CORE} ;
03.     SYMMETRY {X | Y} ;
04.     SIZE width BY height ;
05.  END siteName
```

The following keywords are expected to have the following fields:

- **SITE** (Lines 01 and 05): *siteName* is an alphanumeric string no longer than 64 characters.
- **CLASS** (Line 02): PAD – specifying an I/O pad site – or CORE – specifying a core site.
- **SYMMETRY** (Line 03): X (Y) – specifying the row is symmetric about the X- (Y-)axis. As this contest does not allow cell flipping, this value will not be used.
- **SIZE** (Line 04): *width* and *height* are the dimensions (size) of the site specified in microns.

The following shows an example site (note that the keywords specified within `SITE` can be in any order).

```
01.  SITE core
02.     SIZE 0.20 BY 2.00 ;
03.     CLASS CORE ;
04.     SYMMETRY Y ;
05.  END core
```

Line 01 and line 05 define the site with name `core`. Line 02 defines the dimensions *width* and *height* of the site to be 0.2 μm $\times$ 0.2 μm. Line 03 specifies the site is of type CORE. Line 04 specifies the symmetry of the site to be about the Y-axis.

LAYER. Each metal layer that is available in the design will be specified here. This information is used to specify routing layers and where pins are located. For this contest, we will only use the ROUTING type with a limited set of keywords.

```
01.  LAYER layerName
02.     TYPE ROUTING ;
03.     DIRECTION {HORIZONTAL | VERTICAL} ;
04.     PITCH {distance | xDistance yDistance} ;
05.     WIDTH defaultWidth ;
06.     OFFSET {distance | xDistance yDistance} ;
07.  END layerName
```

The following keywords are expected to have the following fields:

- **LAYER** (Lines 01 and 07): *layerName* is an alphanumeric string no longer than 64 characters.
- **TYPE** (Line 02): ROUTING is currently the only expected option.
- **DIRECTION** (Line 03): the layer either has routing tracks parallel to the X-axis (HORIZONTAL) or the Y-axis (VERTICAL).
- **PITCH** (Line 04): specifies the minimum distance between each routing track in microns (float). If only *distance* is specified, it is for both vertical and horizontal tracks. Otherwise, *xDistance* and *yDistance* specify for the horizontal and vertical tracks, respectively.
- **WIDTH** (Line 05): *defaultWidth* specifies the routing-track width for all (regular) routing tracks in microns.
- **PITCH** (Line 06): specifies the offset distance of the routing grid to align with the standard cell grid in distance units (float). If only *distance* is specified, it is for both x-offset and y-offset. Otherwise, *xDistance* and *yDistance* specify for the x-offset and y-offset, respectively.

The following shows an example definition of a metal layer.

```
01.  LAYER metal1
02.     TYPE ROUTING ;
03.     DIRECTION HORIZONTAL ;
04.     PITCH 0.200 ;
05.     OFFSET 0.000 ;
06.     WIDTH 0.100 ;
07.  END metal1
```

Lines 01 and 07 specify the definition of the layer with name `metal1`. Line 02 specifies the layer type to be ROUTING. Line 03 specifies the routing tracks on this layer are HORIZONTAL. Line 04 specifies the minimum spacing between routing tracks is 0.2 μm. Line 05 specifies no offset with the routing grid and the standard-cell boundaries. Line 06 specifies the track width to be 0.1 μm.

MACRO. Each definition specifies the definition of a cell type, which can be instantiated in other files, e.g., `simple.v`. For this contest, we will be using a limited set of keywords associated with **MACRO**.

```
01.  MACRO macroName
02.     CLASS {PAD | CORE} ;
03.     ORIGIN point ;
04.     SIZE width BY height ;
05.     SITE siteName ;
06.     PIN pinName DIRECTION {INPUT | OUTPUT}
07.        PORT
08.        LAYER layerName ;
09.        RECT point point ;
10.        END
11.     END pinName
12.  END macroName
```

The following keywords are expected to have the following fields:

- **MACRO** (Lines 01 and 12): *layerName* is an alphanumeric string no longer than 64 characters.
- **CLASS** (Line 02): Specifies either an I/O pad (PAD) or standard-cell area (CORE).
- **ORIGIN** (Line 03): Specifies a point (x,y) where to align the origin of the macro to the DEF **COMPONENTS** placement point (see Section 2.4). The macro is shifted by (x,y) before alignment. For example, if *point* is (0,$-$1), then all macro objects at (0,1) are shifted to (0,0).
- **SIZE** (Line 04): Specifies the dimensions (size) *width* and *height* of the macro in microns.
- **SITE** (Line 05): Specifies the macro's associated *siteName* (defined as using **SITE**).
- **PIN** (Lines 06 and 11): Specifies a input (INPUT) or output (OUTPUT) pin with name *pinName*. Lines 07-10 are associated with this keyword.
- **PORT** (Lines 07 and 10): Required (no following variable input).
- **LAYER** (Line 08): Specifies the macro pin's associated *layerName* (defined with **LAYER**).
- **RECT** (Line 09): Specifies two points (x_1,y_1) and (x_2,y_2) that define the locations of two opposite corners of the macro pins. The points are specified in microns.

The following is an example definition of a macro.

```
01.  MACRO INV_X1
02.     CLASS CORE ;
03.     ORIGIN 0 0 ;
04.     SIZE 0.8 BY 2.0 ;
05.
06.     SITE core ;
07.     PIN ZN DIRECTION OUTPUT ;
08.        PORT
09.        LAYER metal1 ;
10.        RECT 0.05 0.500 0.15 1.500 ;
11.        END
12.     END ZN
13.     PIN A DIRECTION INPUT ;
14.        PORT
15.        LAYER metal1 ;
16.        RECT 0.45 0.500 0.55 1.500 ;
17.        END
18.     END A
19.  END INV_X1
```

Lines 01 and 19 specify the definition of the macro `INV_X1`. Line 02 specifies the macro type to be CORE. Line 03 specifies the origin of `INV_X1` to be at (0,0). Line 04 specifies the size of the macro to be 0.8 μm $\times$ 2.0 μm. Line 06 specifies that this macro belongs to the site `core`. Lines 07-12 specify an output pin `ZN`, located on layer `metal1` with lower-left and upper-right coordinates being (0.05 μm, 0.5 μm) and (0.15 μm, 1.5 μm), respectively. Lines 13-18 specify an input pin `A`, located on layer `metal1`, with lower-left and upper-right coordinates being (0.45 μm, 0.5 μm) and (0.55 μm, 1.5 μm), respectively.

2.4 .def (DEF)

The `.def` file (in Design Exchange Format (LEF) specifies the different cells and connectivity of the design. For this contest, we will be using a very small subset of the keywords in the DEF language. If you are implementing your own parser, you will be expected to support what is defined in `simple.def`, as well as defined comments beginning with the character '#'. The following explains the general format of the necessary keywords, with snippets of `simple.def` reproduced for clarity. The relevant keywords are those listed in the header, as well as **ROW**, **COMPONENTS**, **PINS**, and **NETS**.

DEF structure. These initial statements are used to set the parsing rules of the DEF file.

```
01. VERSION 5.7 ;
02. DIVIDERCHAR "/" ;
03. BUSBITCHARS "[]" ;
04. DESIGN c17 ;
05. UNITS DISTANCE MICRONS 1000 ;
06.
07. DIEAREA ( 0 0 ) ( 8000 8000 ) ;
...
99. END DESIGN
```

Line 01 specifies the DEF language version used. Line 02 specifies the hierarchy delimiter character. For instance, `myBox/A` defines the `A` to be within the instance `myBox`. Line 03 specifies the character set used to specify groups of signals, e.g., bus signals. For instance, `myInputs[31]` specify a signal that spans 32 bits. For this contest, we will not be defining bus signals (but the keyword may be part of the DEF file). Line 04 specifies the design name. Line 05 specifies the unit conversion between DEF database units to microns (μm). In this example, every 1000 DEF units is equivalent to 1 μm. Line 07 specifies the lower-left and upper-right coordinates of the total layout area in DEF database units (integers). Line 99 specifies the end of the DEF file.

ROW. Each row specifies a region where standard cells are placed. It has the following syntax:

ROW *rowName siteName origX origY siteOrient* DO *numX* BY *numY* STEP *stepX stepY*

Here, *rowName* defines the row name, *siteName* defines the associated site name (as defined by **SITE**, (*origX*, *origY*) defines the origin (lower-left) of the row in DEF database units (integers), and *siteOrient* defines site orientation (up to two characters). The DO *numX* BY *numY* segment specifies the number of sites in **ROW**. At least one of *numX* and *numY* must equal 1; if $numX = 1$, then the row is vertical, and if $numY = 1$, then the row is horizontal. If both $numX = numY = 1$, then the row is a single site. The STEP *stepX stepY* segment specifies the spacing between sites in the horizontal (*stepX*) or vertical (*stepY*) row in DEF database units. The following shows an example definition of a row with name `core_SITE_ROW_2` in the site `core` at (0,4000) with 'N' orientation. The row is horizontal with 40 sites and 200 DEF database units between each site.

ROW `core_SITE_ROW_2 core 0 4000 N DO 40 BY 1 STEP 200 0 ;`

COMPONENTS. All cell instances are defined here with DEF database units.

```
01.  COMPONENTS numComponents ;
02.     - instanceName cellName
03.        + {PLACED | FIXED} ( xLoc yLoc ) orientation ;
04.  END COMPONENTS
```

In line 01, *numComponents* specifies the total number of components or cell instances there are in the design. Line 02 specifies the instance *instanceName* and cell-type *cellName* names of the component, e.g., those defined in the verilog file. Line 03 specifies if the cell instance is movable (PLACED) or not movable (FIXED), along with the lower-left coordinate of the cell (*xLoc*,*yLoc*) in DEF database units and its orientation. Line 04 specifies the end of the **COMPONENTS** keyword. The following shows an example definition of components:

```
01.  COMPONENTS 5 ;
02.     - u1 NAND2_X1
03.        + PLACED ( 2000 6000 ) N ;
04.     - f1 DFF_X1
05.        + FIXED ( 400 0 ) N ;
06.     - u2 INV_X1
07.        + PLACED ( 4000 2000 ) N ;
08.     - u3 INV_X1
09.        + PLACED ( 9000 4000 ) N ;
10.     - u4 NOR2_X1
11.        + PLACED ( 2000 2000 ) N ;
12.  END COMPONENTS
```

Lines 01 and 12 specify 5 cell instances in the components definition. Lines 02-03 define a movable instance of `u1` of cell-type `NAND2_X1` at location (2000,6000) with orientation 'N'. Lines 04-05 define a non-movable instance of `f1` of cell-type `DFF_X1` at location (400,0) with orientation 'N'. Lines 06-07 define a movable instance of `u2` of cell-type `INV_X1` at location (4000,2000) with orientation 'N'. Lines 08-09 define a movable instance of `u3` of cell-type `INV_X1` at location (9000,4000) with orientation 'N'. Lines 08-09 define a movable instance of `u4` of cell-type `NOR_X1` at location (2000,4000) with orientation 'N'.

PINS. In the DEF file, only the primary input and outputs pins of the design are specified.

```
01.  PINS numPins ;
02.     - pinName + NET netName
03.        + DIRECTION {INPUT | OUTPUT}
04.        + {PLACED | FIXED} point orientation
04.        + LAYER layerName ( point ) ( point ) ;
05.  END PINS
```

Line 01 specifies the number of primary input and output pins in the design (*numPins*). Line 02 specifies the individual pin name (*pinName*) and its connected net (*netName*). These names should match the ones specified in the other files, e.g., verilog. Line 03 specifies the pin as either a primary input (INPUT) or primary output (OUTPUT). Line 04 specifies if the pin is movable (PLACED) or non-movable (FIXED), along with the lower-left coordinate of the pin (x,y) in DEF database units and the orientation. Line 05 specifies the layer (*layerName*) the pin is located on, as well as its geometry, defined in DEF database units, as the two opposite corners. Note that the semi-colon (;) character denotes the end of the pin read – if lines 03 and 05 were in reverse order, the semi-colon would be after {`INPUT | OUTPUT`}. Line 06 specifies the end of the **PINS** keyword. The following is example pins definition:

```
01.  PINS 4 ;
02.     - out + NET out
03.        + DIRECTION OUTPUT
04.        + FIXED ( 8000 6000 ) N
05.        + LAYER metal3 ( 0 0 ) ( 100 100 ) ;
06.     - inp1 + NET inp1
07.        + DIRECTION INPUT
08.        + FIXED ( 2000 8000 ) N
09.        + LAYER metal3 ( 0 0 ) ( 100 100 ) ;
10.     - inp2 + NET inp2
11.        + DIRECTION INPUT
12.        + FIXED ( 4000 8000 ) N
13.        + LAYER metal3 ( 0 0 ) ( 100 100 ) ;
14.     - iccad_clk + NET iccad_clk
15.        + DIRECTION INPUT
16.        + FIXED ( 0 2000 ) N
17.        + LAYER metal3 ( 0 0 ) ( 100 100 ) ;
18.  END PINS
```

Lines 01 and 18 asserts four (4) primary inputs and outputs in the design. Lines 02-05 define the primary output `out` pin connected to net `out` with fixed location (8000,6000) and orientation 'N' on `metal3` with size 100 × 100. Lines 06-09 define the primary input `inp1` pin connected to net `inp1` with fixed location (2000,8000) and orientation 'N' on `metal3` with size 100 × 100. Lines 10-13 define the primary input `inp2` pin connected to net `inp2` with fixed location (4000,8000) and orientation 'N' on `metal3` with size 100 × 100. Lines 14-17 define the primary input `iccad_clk` pin connected to net `iccad_clk` with fixed location (0,2000) and orientation 'N' on `metal3` with size 100 × 100.

NETS. All internal and external connections are specified as nets. Its syntax is:

```
01.  NETS numNets ;
02.     - netName ({PIN | instanceName} pinName) [...] ;
03.  END NETS
```

Lines 01 and 03 specify the nets definition with *numNets* total connections. Line 02 specifies the name of the net (e.g., *netName*) as well as its the pins it connects. If the pin is part of a cell instance, then the syntax is (*instanceName pinName*); if the pin is a primary input or output, its syntax is (PIN *pinName*). These nets should match the definitions in the verilog file. The following shows an example nets definition.

```
01.  NETS 8 ;
02.     - n1 ( u1 ZN ) ( u4 A1 ) ;
03.     - n2 ( u4 ZN ) ( f1 D ) ;
04.     - n3 ( f1 Q ) ( u2 A ) ( u4 A2 ) ;
05.     - n4 ( u2 ZN ) ( u3 A ) ;
06.     - out ( u3 ZN ) ( PIN out ) ;
07.     - inp1 ( PIN inp1 ) ( u1 A1 ) ;
08.     - inp2 ( PIN inp2 ) ( u1 A2 ) ;
09.     - iccad_clk ( PIN iccad_clk ) ( f1 CK ) ;
10.  END NETS
```

Lines 01 and 10 specify the 8 nets as part of the design. Line 02 defines a net `n1` that connects pins `u1/ZN` and `u4/A1`. Line 03 defines a net `n2` that connects pins `u4/ZN` and `f1/D`. Line 04 defines a net `n3` that connects pins `f1/Q`, `u2/A` and `u4/A2`. Line 05 defines a net `n4` that connects pins `u2/ZN` and `u3/A`. Line 06 defines a net `out` that connects pin `u3/ZN` and primary output pin `out`. Line 07 defines a net `inp1` that connects primary input pin `inp1` and pin `u1/A1`. Line 08 defines a net `inp1` that connects primary input pin `inp2` and pin `u1/A2`. Line 09 defines a net `iccad_clk` that connects primary input pin `iccad_clk` and pin `f1/CK`.

2.5 .sdc (Constraints)

The Synopsys Design Constraints (SDC) file specifies the set of assertions or constraints used as initial timing conditions for the design. For this contest, we will be using a very limited set of commands. If you are writing your own parser, you are expected to support the commands and keywords specified in *simple.sdc*, as well as the comments starting with '#'. All time values are specified in picoseconds (ps). We expect to be using the following five commands and their associated options in a restricted manner:

- `get_ports` {*pinName pinName* ...}:
  returns a set of pins specified by the list of *pinNames*, which are enclosed in {}. A single *pinName* does not require {}, but can have them.

- `create_clock -name` *`clockName`* `-period` *`val`* `[get_ports ...]`:
  creates a clock signal *clockName* with a corresponding period of *val*, and associates it with the primary input (clock) pin returned from `get_ports`.
- `set_input_delay` *`val`* `-clock` *`clockName`* `[get_ports ...]`:
  sets the arrival time of the primary input pins with *val* time with respect to *clockName*.
- `set_driving_cell -lib_cell` *`cellName`* `-pin` *`pinName`*
  `-input_transition_fall` *`val`* `input_transition_rise` *`val`* `[get_ports ...]`:
  sets the cell type (*cellName*) and pin name (*pinName*) with associated input slews for rise and fall.
- `set_output_delay -clock` *`clockName`* *`val`* `[get_ports ...]`:
  sets the required arrival time of the primary output signals with respect to *clockName*.
- `set_load` *`val`* `[get_ports ...]`:
  asserts the capacitance (specified in fF) at the output pin.

This is similar to that shown in Figure 2. The following shows an example set of assertions.

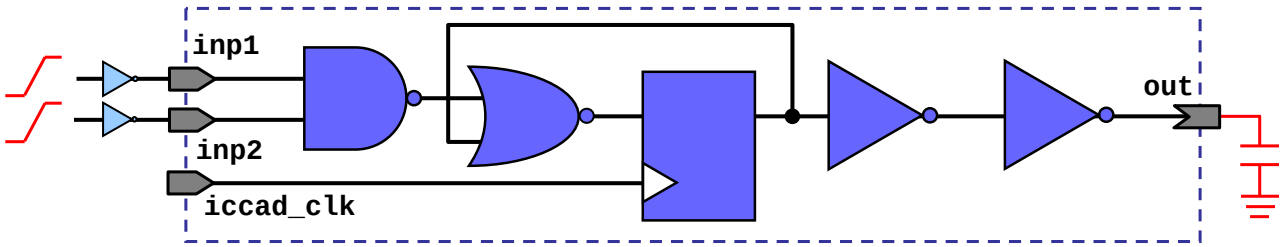

Figure 2: Circuit in `simple.v` with assertions.

```
01.  create_clock -name mclk -period 50.0 [get_ports iccad_clk]
02.  set_input_delay 0.0 [get_ports {inp1}] -clock mclk
03.  set_input_delay 0.0 [get_ports {inp2}] -clock mclk
04.  set_driving_cell -lib_cell INV_X8 -pin ZN [get_ports {inp1}]
      -input_transition_fall 80.0 -input_transition_rise 80.0
05.  set_driving_cell -lib_cell INV_X8 -pin ZN [get_ports {inp2}]
      -input_transition_fall 80.0 -input_transition_rise 80.0
06.  set_output_delay 0.0 [get_ports {out}] -clock mclk
07.  set_load -pin_load 4.0 [get_ports {out}]
```

Line 01 creates a clock signal `mclk` with a period of 50 ps, and assigns it to the primary input `iccad_clk`. Line 02 (03) sets the arrival time of `inp1` (`inp2`) to 0, with respect to the `mclk` signal. Line 04 (05) sets the input slew of 80 ps at the driving cell `INV_X8` feeding `inp1` (`inp2`) for both rise and fall. Line 06 sets the required time at `out` to 0, with respect to the `mclk` signal. Line 07 sets the output capacitance attached to `out` to 4 fF.

3 Output File

The expected output file (that is generated by your placer) is a simplified DEF file (.def) that reports the placement locations in DEF database units of all cell instances in the design. For a full explanation of DEF, please see Section 2.4.

In this DEF output file, you should include all cells, i.e., those with either the `FIXED` or `PLACED` property. The expected keywords are (along with any comments): `VERSION`, `DESIGN`, and `COMPONENTS`. For details regarding the syntax of these keywords, please refer to Section 2.4. Below shows an example output DEF file:

```
01.  VERSION 5.7 ;
02.  DESIGN simple ;
03.
04.  COMPONENTS 5 ;
05.  - u1 NAND2_X1
06.     + PLACED ( 2000 4000 ) N ;
07.  - f1 DFF_X1
08.     + FIXED ( 400 0 ) N ;
09.  - u2 INV_X1
10.     + PLACED ( 4000 2000 ) N ;
11.  - u3 INV_X1
12.     + PLACED ( 7000 4000 ) N ;
13.  - u4 NOR2_X1
14.     + PLACED ( 2000 2000 ) N ;
15.  END COMPONENTS
16.
17.  END DESIGN
```

Line 01 documents the DEF language version. Line 02 states the design name. Lines 04 and 15 state the set of five (5) components or cells in the design. Lines 05-06 state the cell instance `u1` is at (2000,4000). Lines 07-08 state the cell instance `f1` is at (400,0). Lines 09-10 state the cell instance `u2` is at (4000,2000). Lines 11-12 state the cell instance `u3` is at (7000,2000). Lines 13-14 state the cell instance `u4` is at (2000,2000).

4 Updates

- 05/14/14 [v1.2]: clarified that the benchmarks will not use the bus characters (Sections 2.4 and 2.3).
- 05/13/14 [v1.1]: added Updates section, minor formatting changes.
- 05/12/14 [v1.0]: initial version.