CS & IT ENGINEERING

Digital Logic

Logic Gate

DPP 0 2

Discussion **Notes**

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01 Questions

02 Discussion

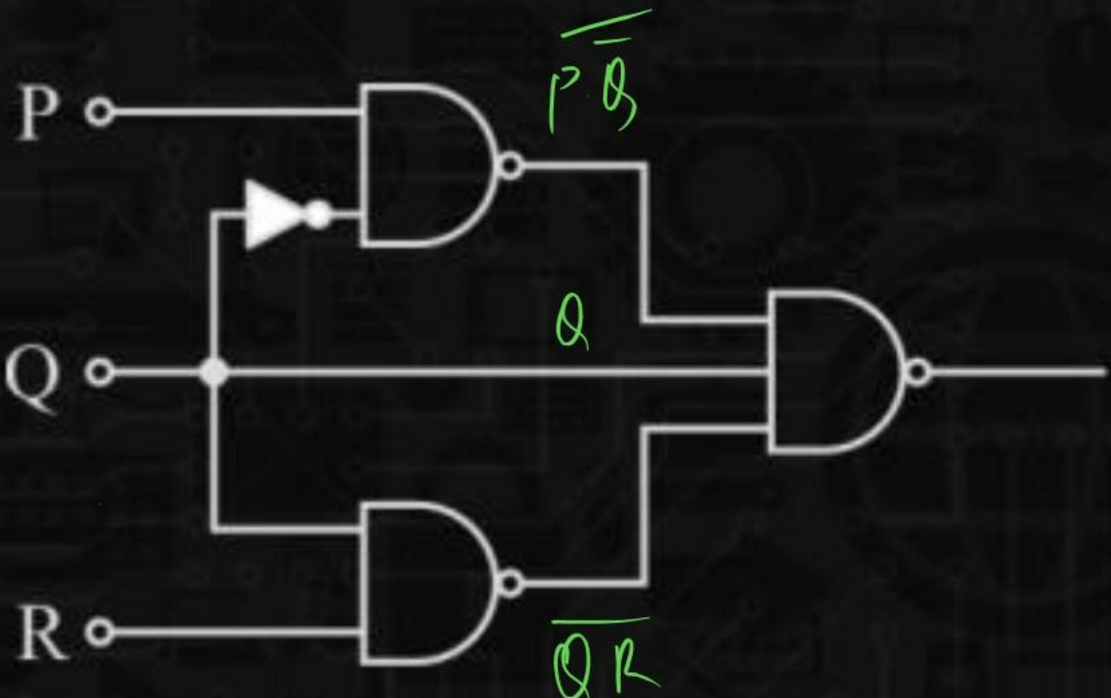
Q.1 For a 3-input logic circuit shown below, the output Z can be expressed as

A. $Q+\bar{R}$

B. $P\bar{Q}+R$

C. $\bar{Q}+R$

D. $P+\bar{Q}+R$



$Z = \overline{P\bar{Q} \cdot Q \cdot \overline{QR}}$

$= P\bar{Q} + \bar{Q} + QR$

$= \bar{Q}(P+1) + QR$

$= \bar{Q} + QR$

$= (\bar{Q}+Q)(\bar{Q}+R)$

$= \bar{Q}+R$

Q.2

The complete set of only those Logic Gates designated as Universal Gates is

A. NOT, OR and AND Gates

B. XNOR, NOR and NAND Gates

C. NOR and NAND Gates

D. XOR, NOR and NAND Gates

Q.3

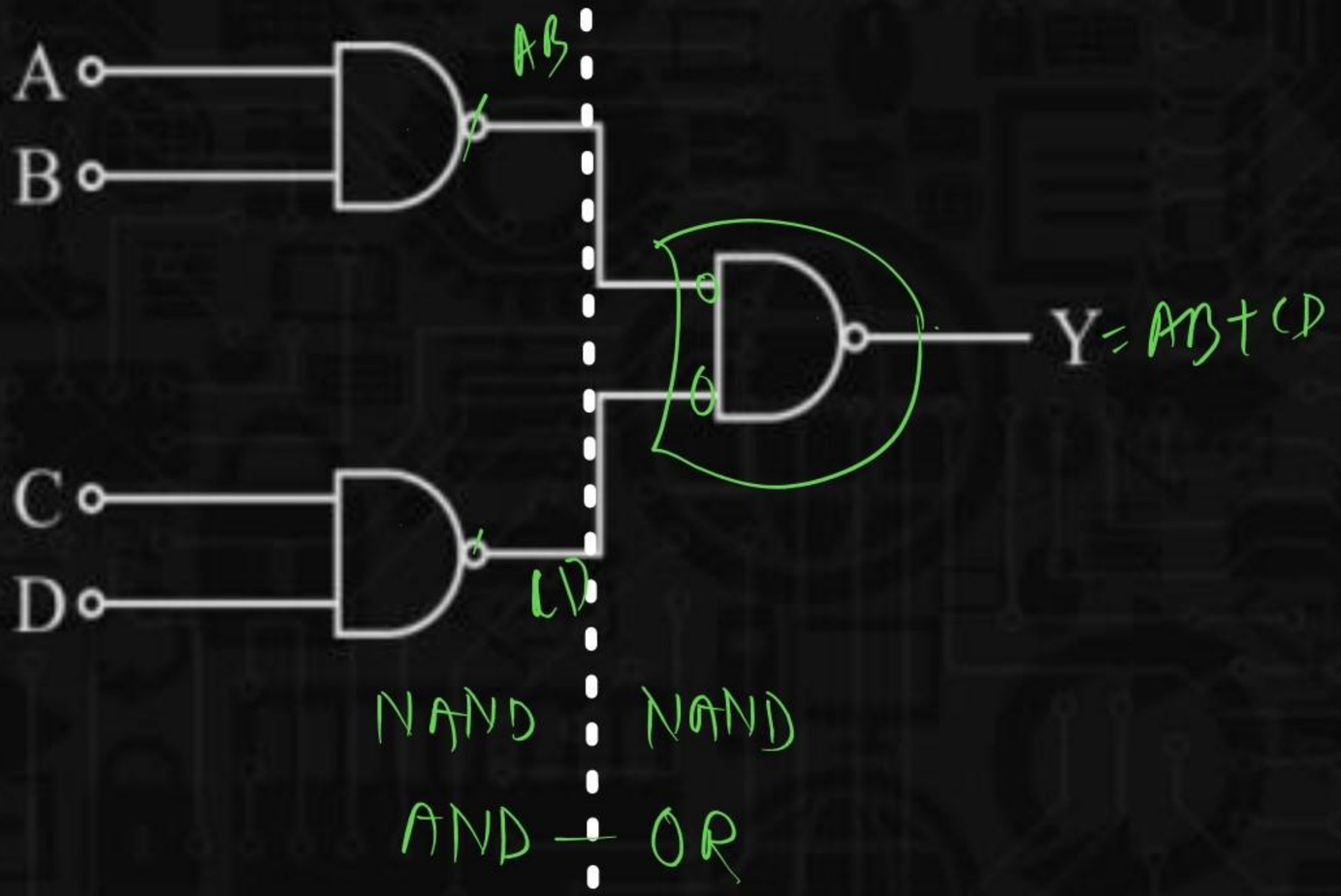
In the logic circuit shown in the figure, Y is given by

A. $Y = ABCD$

B. $Y = (A+B)(C+D)$

C. $Y = A+B+C+D$

D. $Y = AB+CD$



Q.4 $F = AB + CD + E$ will be implemented with how many minimum number NAND gates?

A. Three

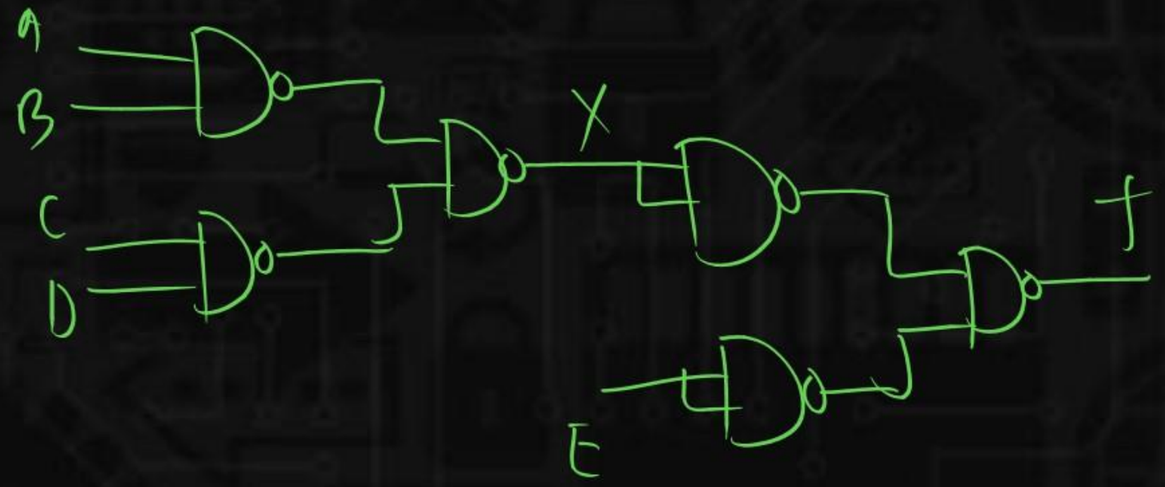
B. Four

C. Five

D. Six

$AB + CD = X$ — 3

$F = X + E$ — 3



Q.5 The minimum number of NAND gates required to reduce the expression ((A + B) C) D is

A. 6

B. 5

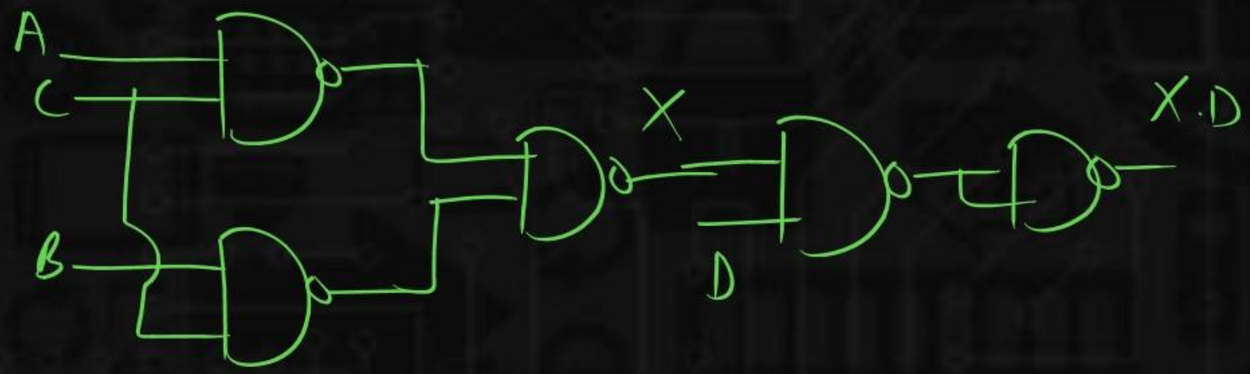
C. 8

D. 4

$f = [AC + BC] \cdot D$

$X = AC + BC \rightarrow (3)$

$f = X \cdot D \rightarrow (2)$



Q.6

In a two-input NAND gate, if both inputs are shorted, it will behave like a _____ gate.

A. Buffer

B. AND

C. NOT

D. EX-OR

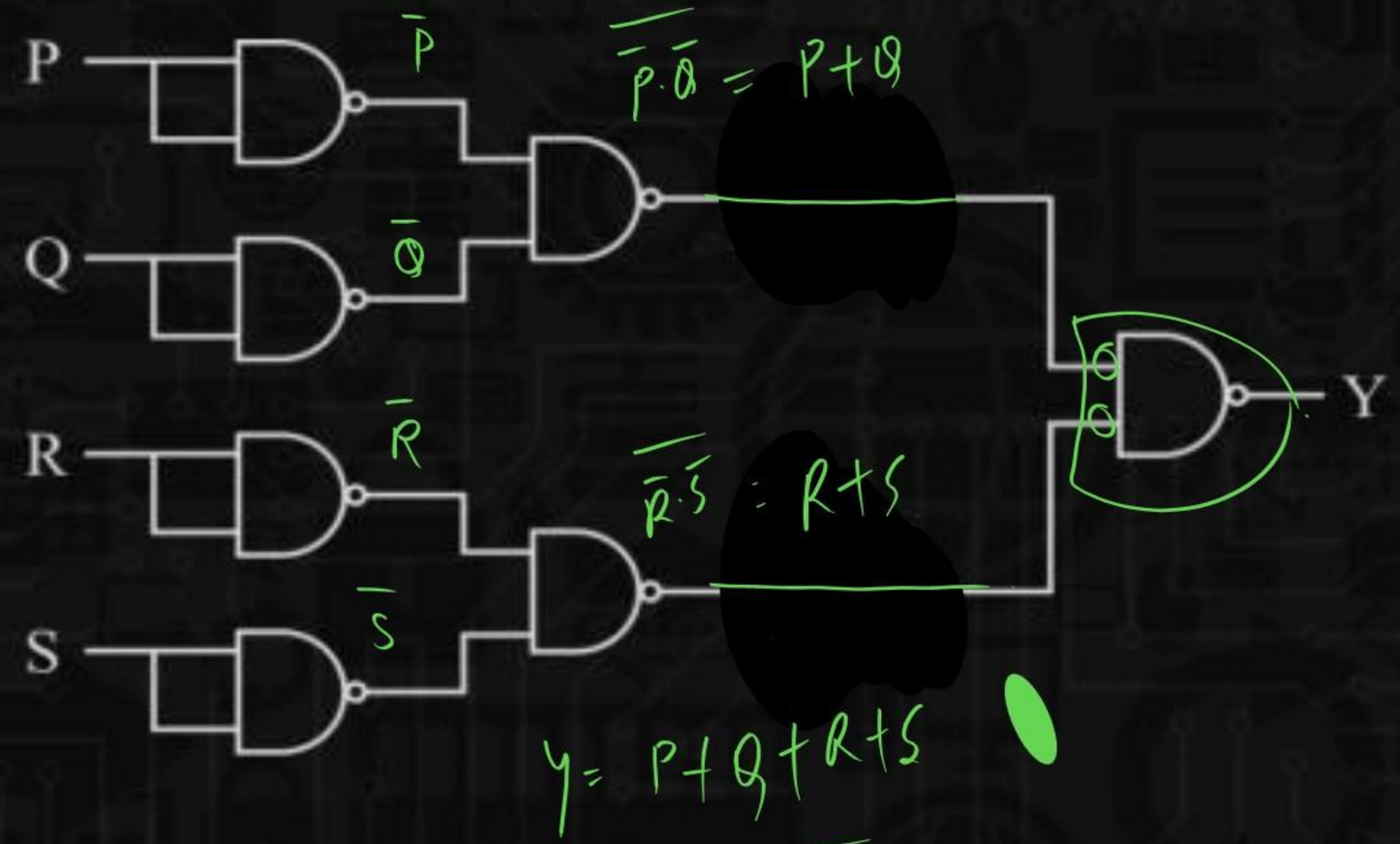
Q.7 For the circuit shown in figure the Boolean expression for the output Y in terms of inputs P, Q, R and S is

A. $\bar{P}+\bar{Q}+\bar{R}+\bar{S}$

B. $P+Q+R+S$

C. $(\bar{P}+\bar{Q})+(\bar{R}+\bar{S})$

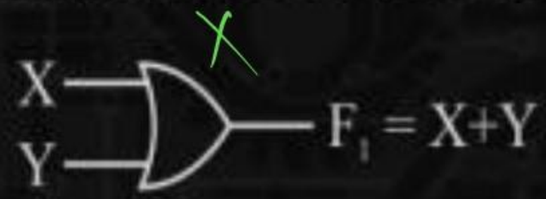
D. $(P+Q)(R+S)$



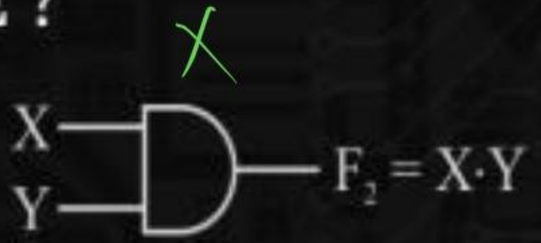
Q.8 A universal logic gate can implement any Boolean function by connecting sufficient number of them appropriately. Three gates are shown:

Which one of the following statements is TRUE ?

A. Gate 1 is a universal gate.



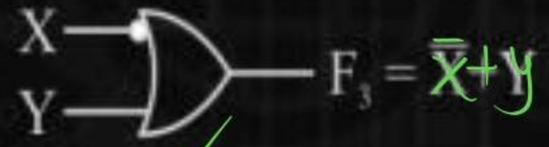
Gate 1



Gate 2

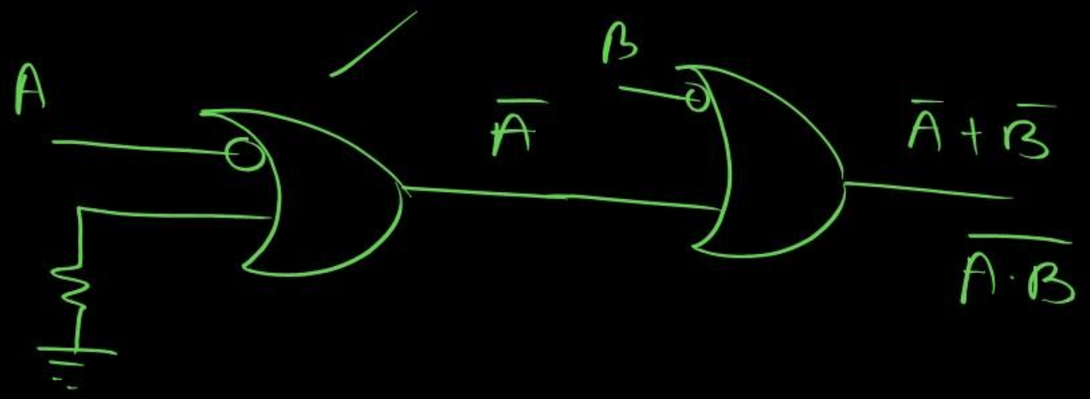
B. Gate 2 is a universal gate.

C. Gate 3 is a universal gate



Gate 3

D. None of the shown is a universal gate.



NAND

Q.9

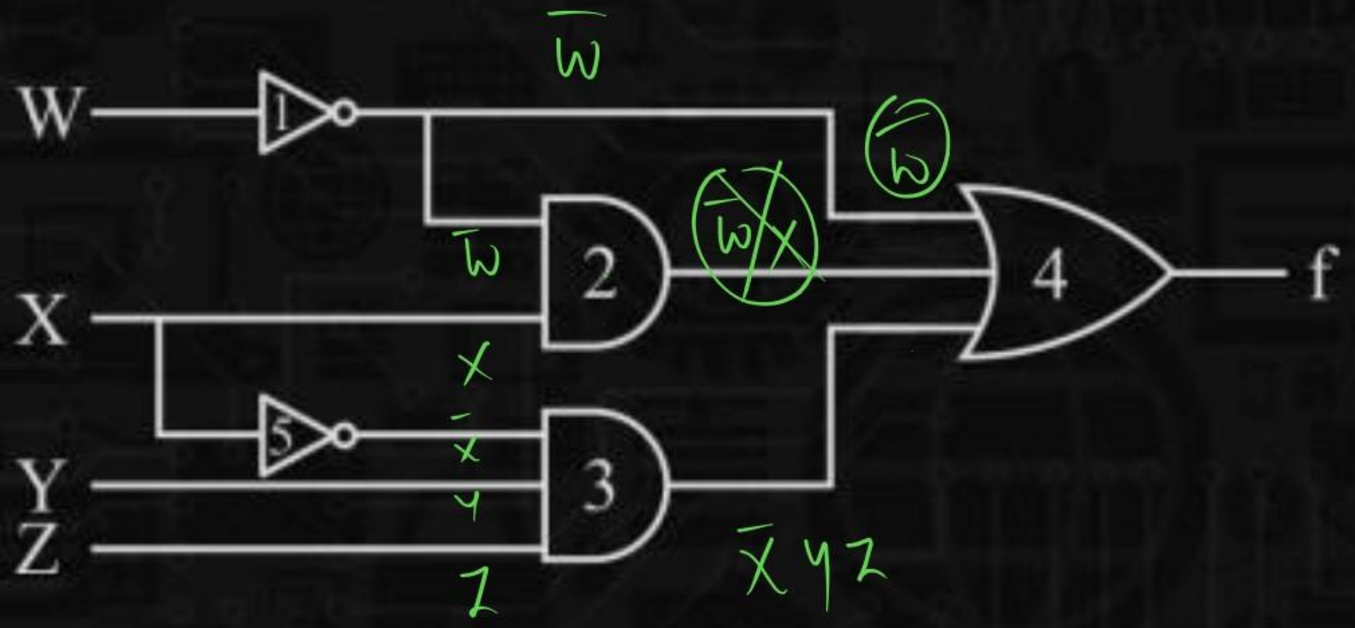
Consider the following gate network:
Which one of the following gates is redundant?

A. Gate No. 1

B. Gate No. 2

C. Gate No. 3

D. Gate No. 4



$f = \bar{w} + \bar{w}x + \bar{x}yz$

$= \bar{w}(1+x) + \bar{x}yz$

$= \bar{w} + xyz$

Q.10 The minimum of NAND gates required to implement A + A B C is equal to

A. 0

B. 1

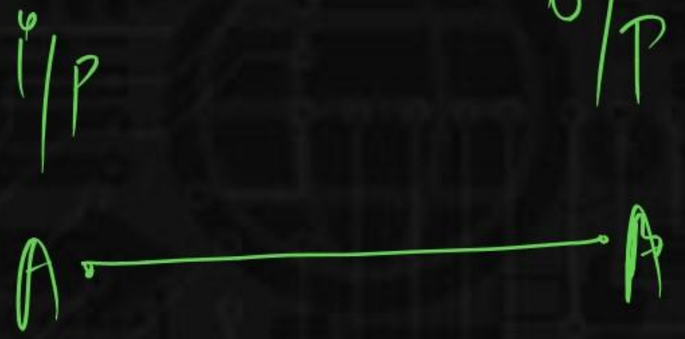
C. 4

D. 7

$A + ABC$

$A(1 + BC)$

A




THANK YOU GW
SOLDIERS !