CS & IT ENGINEERING

DIGITAL LOGIC

Sequential Circuit

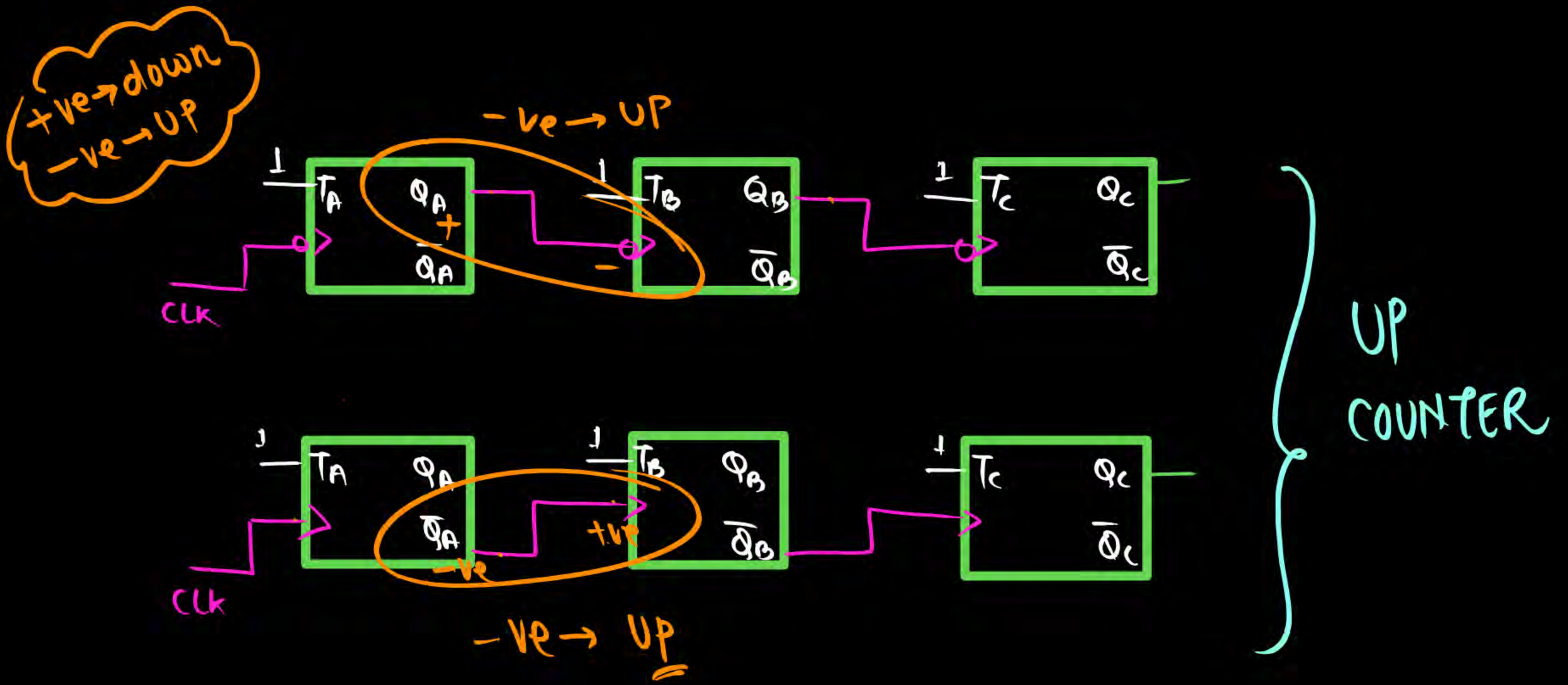
Lecture No. 08

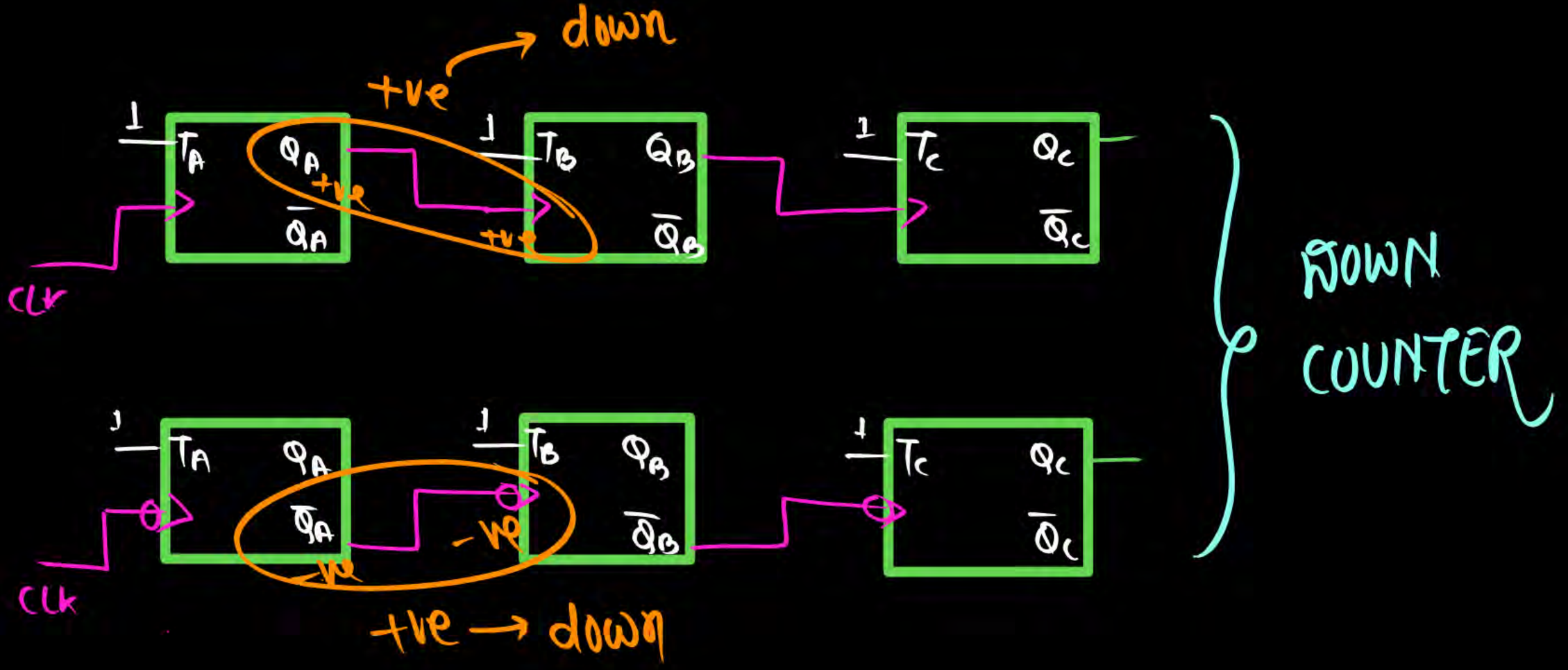
By- CHANDAN SIR

01 ASYNCHRONOUS COUNTER

02 PRACTICE

03 DISCUSSION

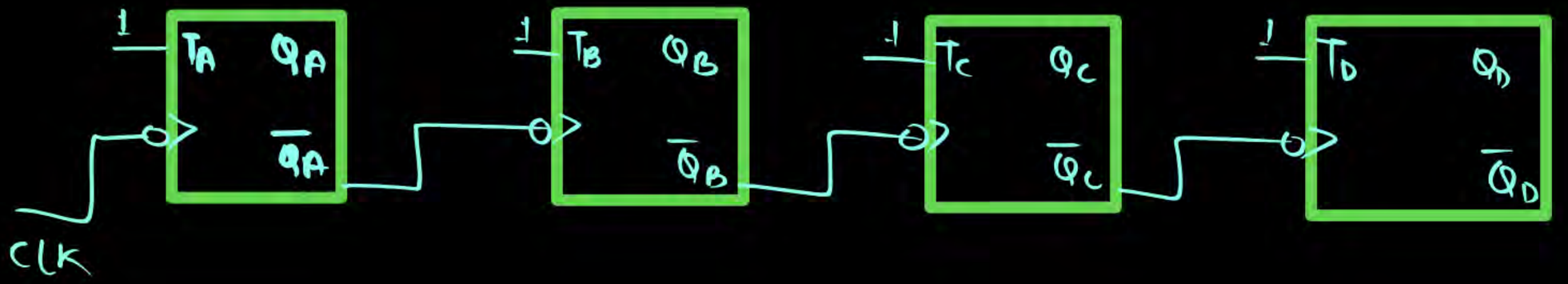

+ve → down
−ve → up
−ve → UP
1
T_A
Q_A
$\overline{Q}_A$
1
T_B
Q_B
$\overline{Q}_B$
1
T_C
Q_C
$\overline{Q}_C$
CLK
UP COUNTER
1
T_A
Q_A
$\overline{Q}_A$
1
T_B
Q_B
$\overline{Q}_B$
1
T_C
Q_C
$\overline{Q}_C$
CLK
+ve
−ve
−ve → UP


down
+ve
1
T_A
Q_A
$\overline{Q}_A$
+ve
1
T_B
Q_B
$\overline{Q}_B$
+ve
1
T_C
Q_C
$\overline{Q}_C$
CLK
DOWN COUNTER
1
T_A
Q_A
$\overline{Q}_A$
-ve
1
T_B
Q_B
$\overline{Q}_B$
1
T_C
Q_C
$\overline{Q}_C$
CLK
-ve
+ve → down

Full Mode counter ⇒ when all the states are used by the counter.

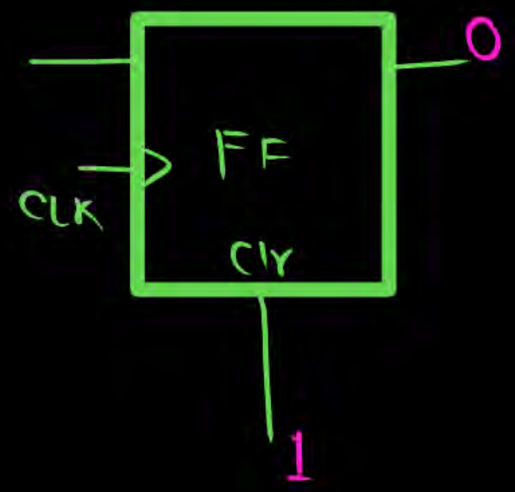
n = 3	MOD = 8
n = 4	MOD = 16
n = 5	MOD = 32

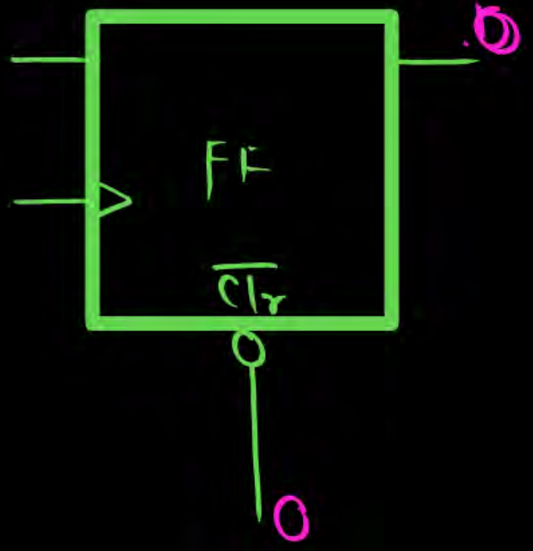
Q Design a MOD 16 down counter in which $\bar{Q}$ is taken as clock?.



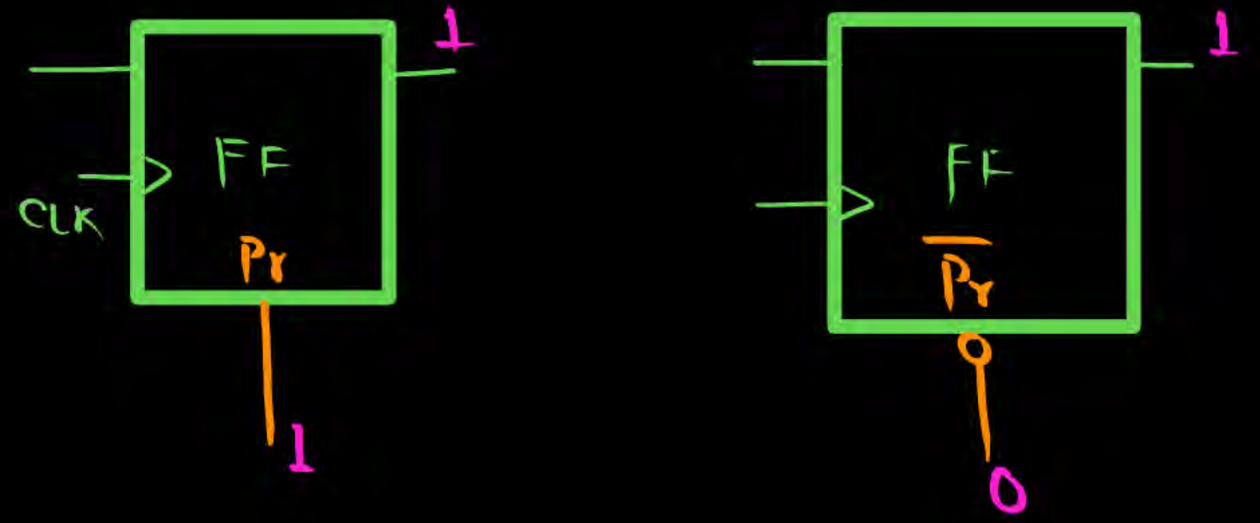
$\Rightarrow$ Feedback Reduces the number of states.

RESET clear





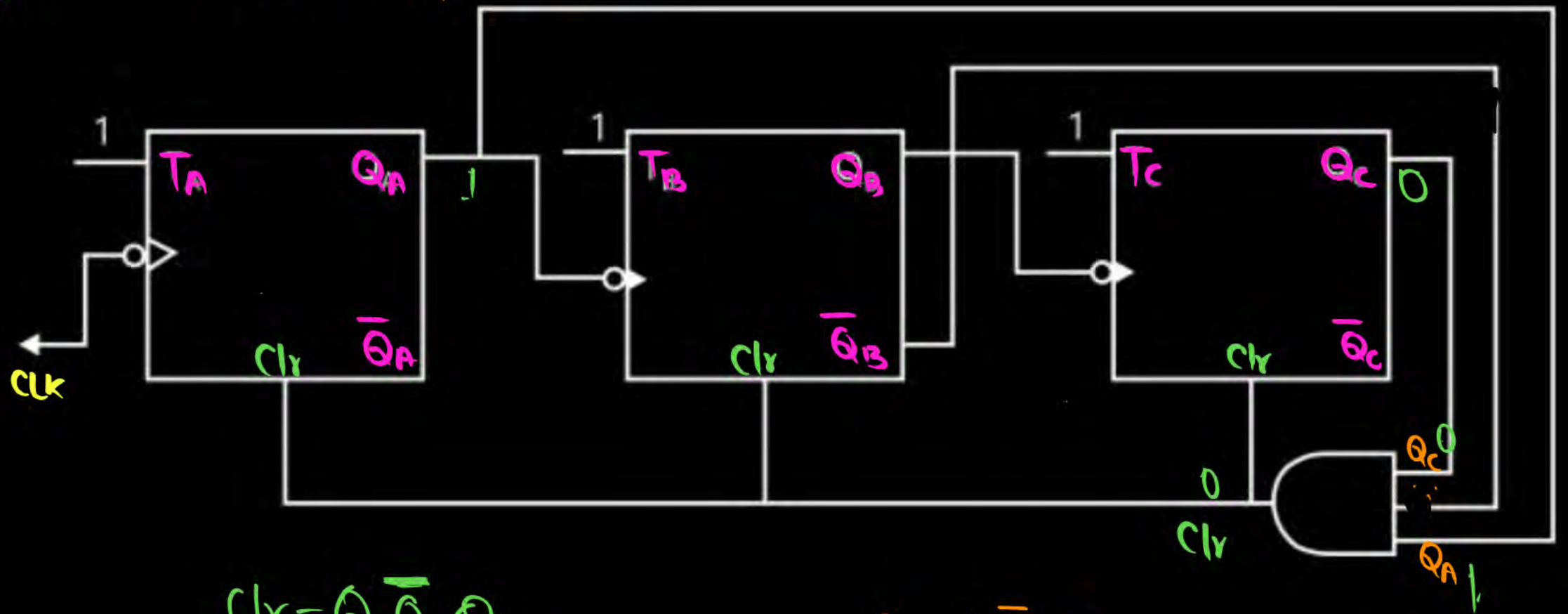
PRESET



FEEDBACK REDUCES THE NUMBER OF STATES

Ex.

Mod (5) up Ripple counter.



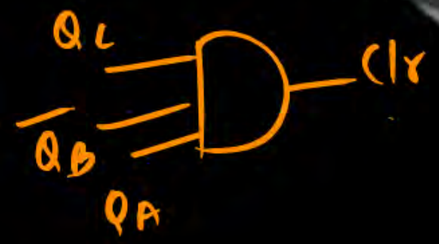
$Clr = Q_C \bar{Q}_B Q_A$

1 0 1 = (5)

$Clr = Q_C \bar{Q}_B Q_A$

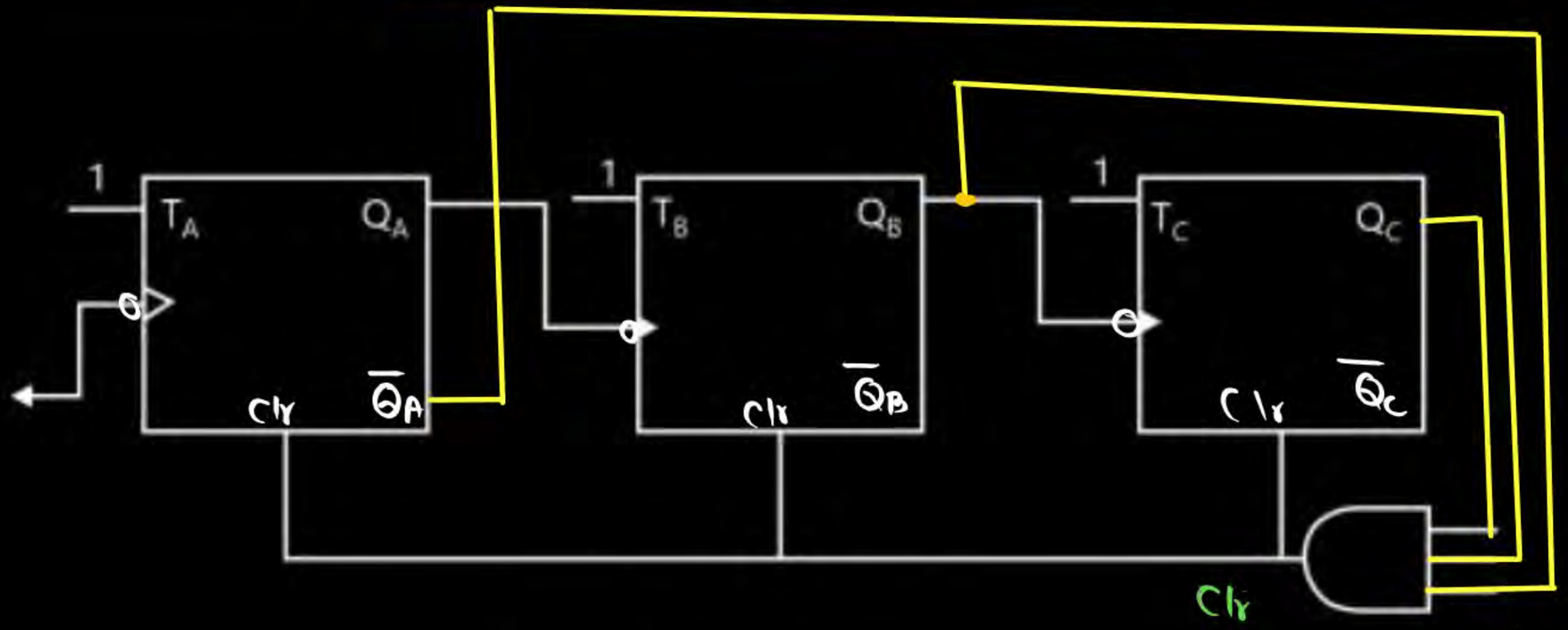
1 0 1 = (5)

FEEDBACK REDUCES THE NUMBER OF STATES



CLK	Q_C	Q_B	Q_A	CLR = $Q_C \bar{Q}_B Q_A$
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	~~1~~ 0	~~0~~ 0	~~1~~ 0	~~1~~ 0
6	0	0	1	0
7	0	1	0	0
8	0	1	1	0

MOD-6 UP RIPPLE COUNTER →



$Clr = Q_C Q_B \bar{Q}_A$

$000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101$

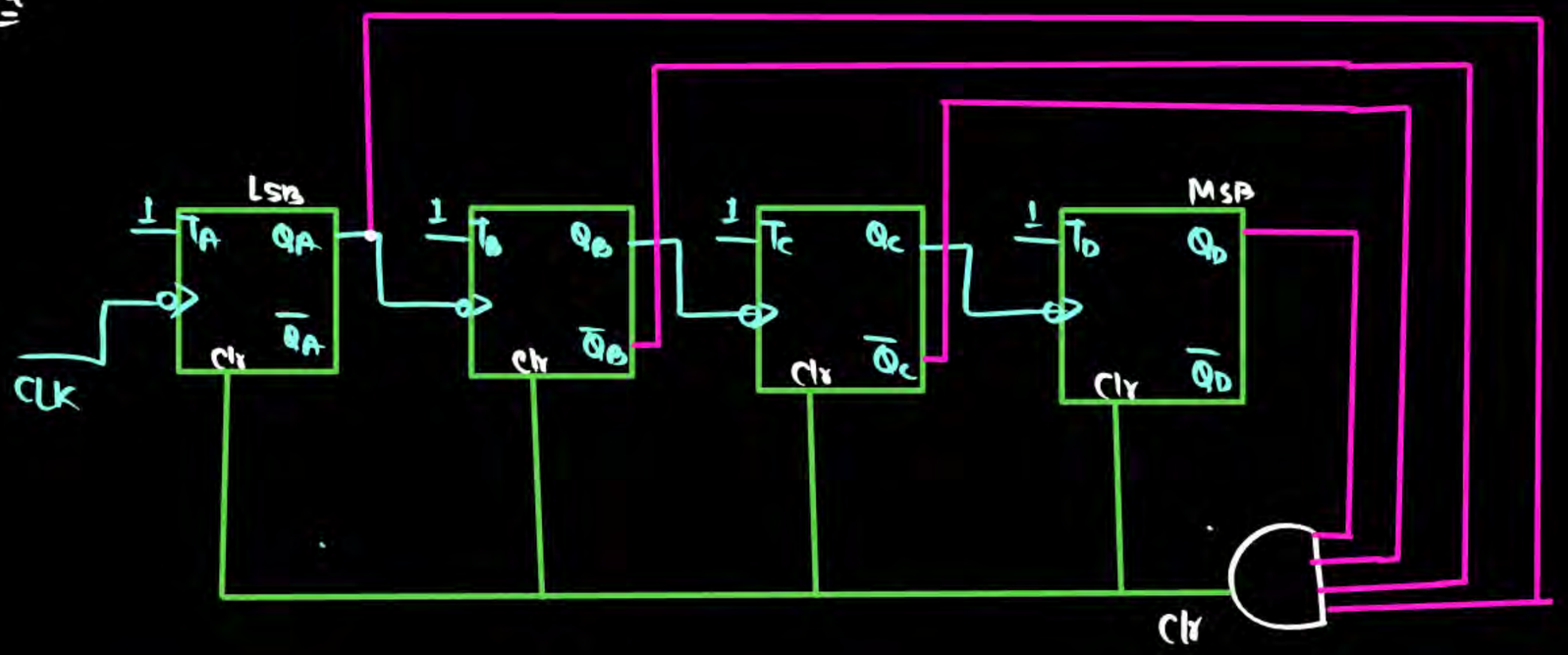
$Clr = Q_C Q_B \bar{Q}_A$

$1 \cdot 1 \cdot 0 = 6$

$Clr = Q_C Q_B \bar{Q}_A$

CLK	Q_C	Q_B	Q_A	Clr
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1→0	1→0	0→0	1→0
7	0	0	1	0
8	0	1	0	0

Q.



MOD-(9) UP Ripple counter.

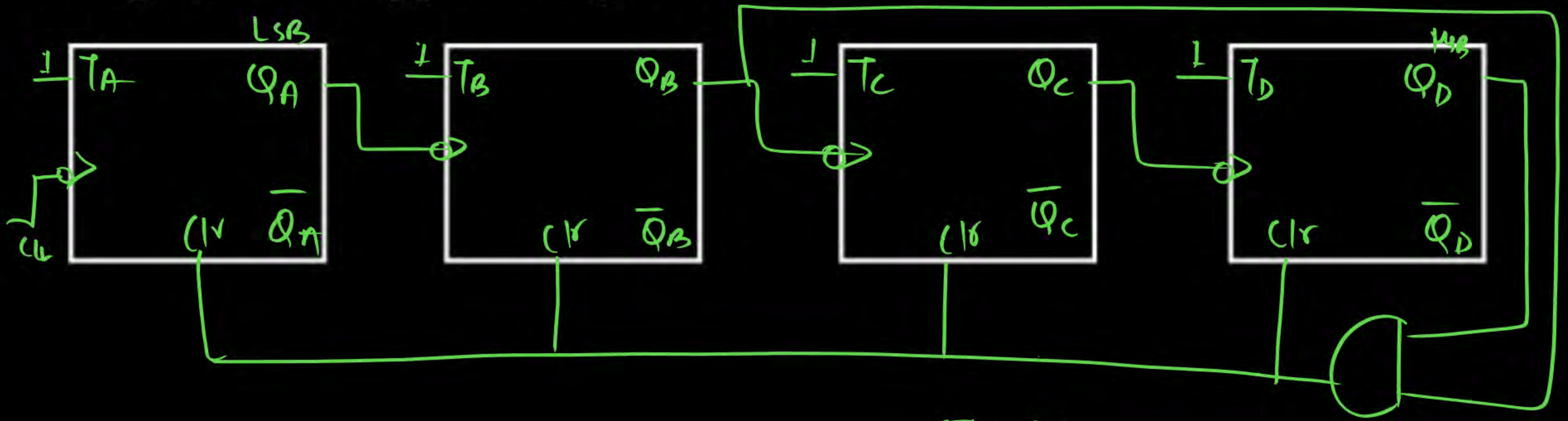
$Clr = Q_D \overline{Q_C} \overline{Q_B} Q_A$

$1001 = (9)$

CLK	Q_D	Q_C	Q_B	Q_A	Clr
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	0	0	0	1	
11	0	0	1	0	

Q.

Design a BCD Ripple Carry counter?

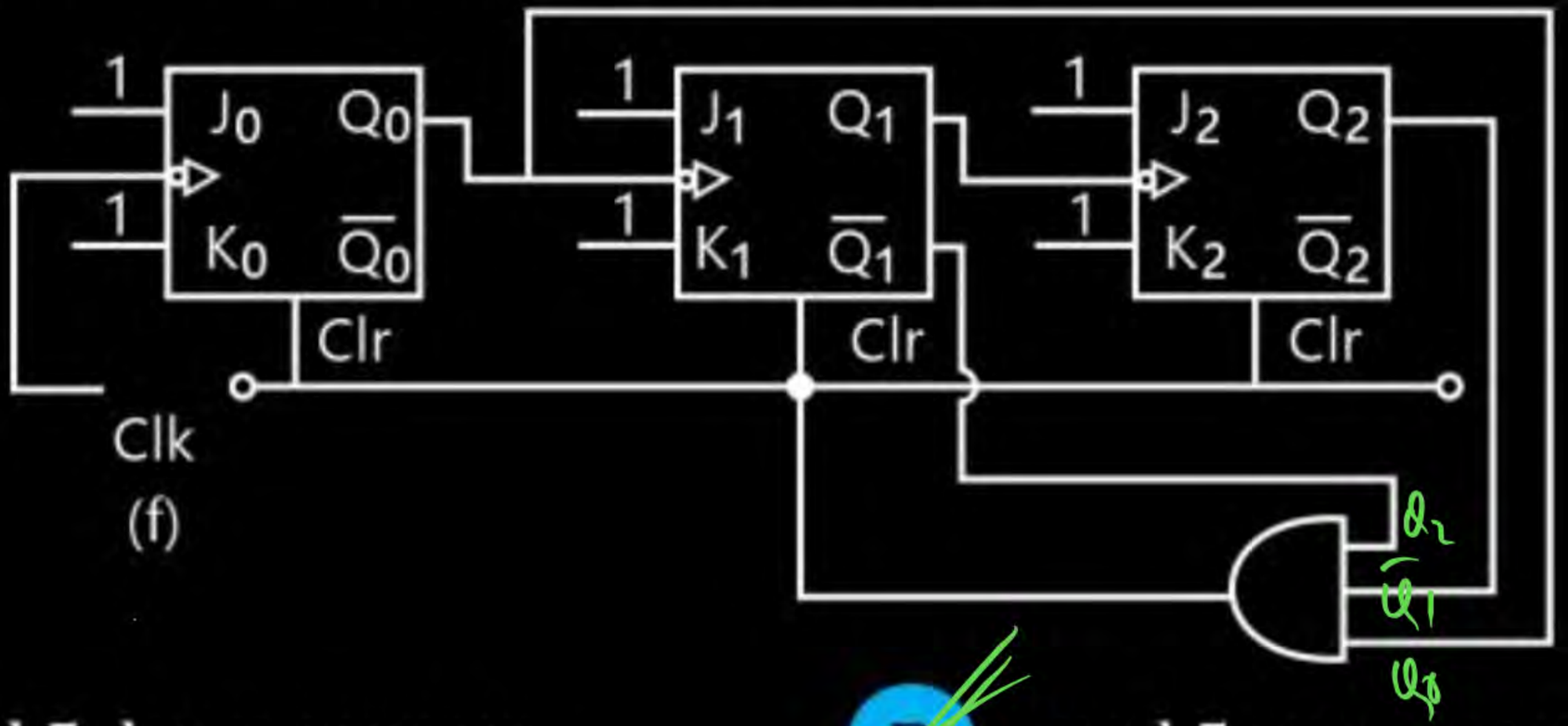


$$Clr = Q_D \overline{Q}_C Q_B \overline{Q}_A$$

1 0 1 0

Q.

Which type of counter is shown below?



Clr = Q2 Q1 Q0
(0 | f5)

A mod 5 down counter

B mod 5 up counter

C mod 6 up counter

D mod 6 down counter

Q.

Consider the following counter

If counter starts at 000, what will be the count after 13 clock pulses?

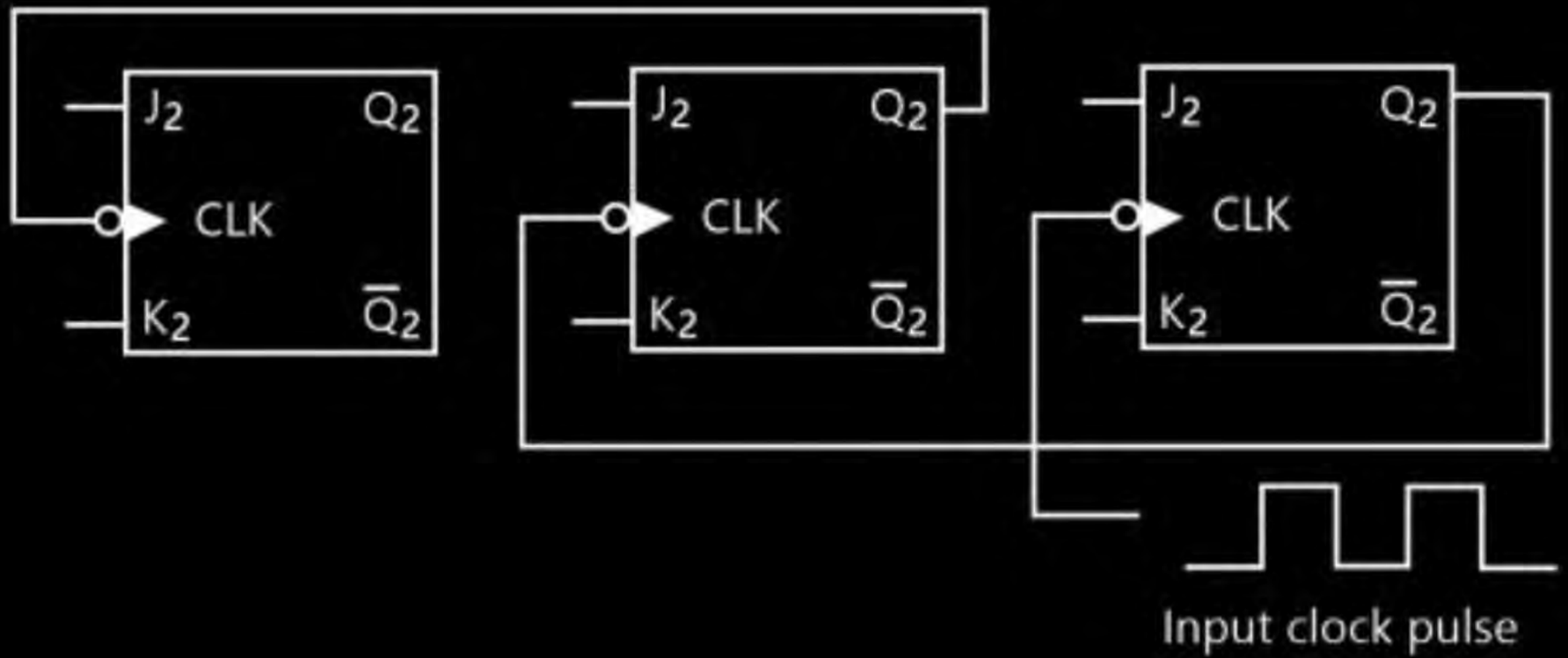
HW

A 100

B 101

C 110

D 111



Discussion

Q Design a MOD-13 UP Ripple counter.

Q Design a MOD-21 UP Ripple counter

Q Design a MOD-27 UP Ripple counter.

Q Design a MOD 14 UP Ripple counter.

Thank you

GW

Soldiers !