CS & IT ENGINEERING

DIGITAL LOGIC

Sequential Circuit

Lecture No. 1

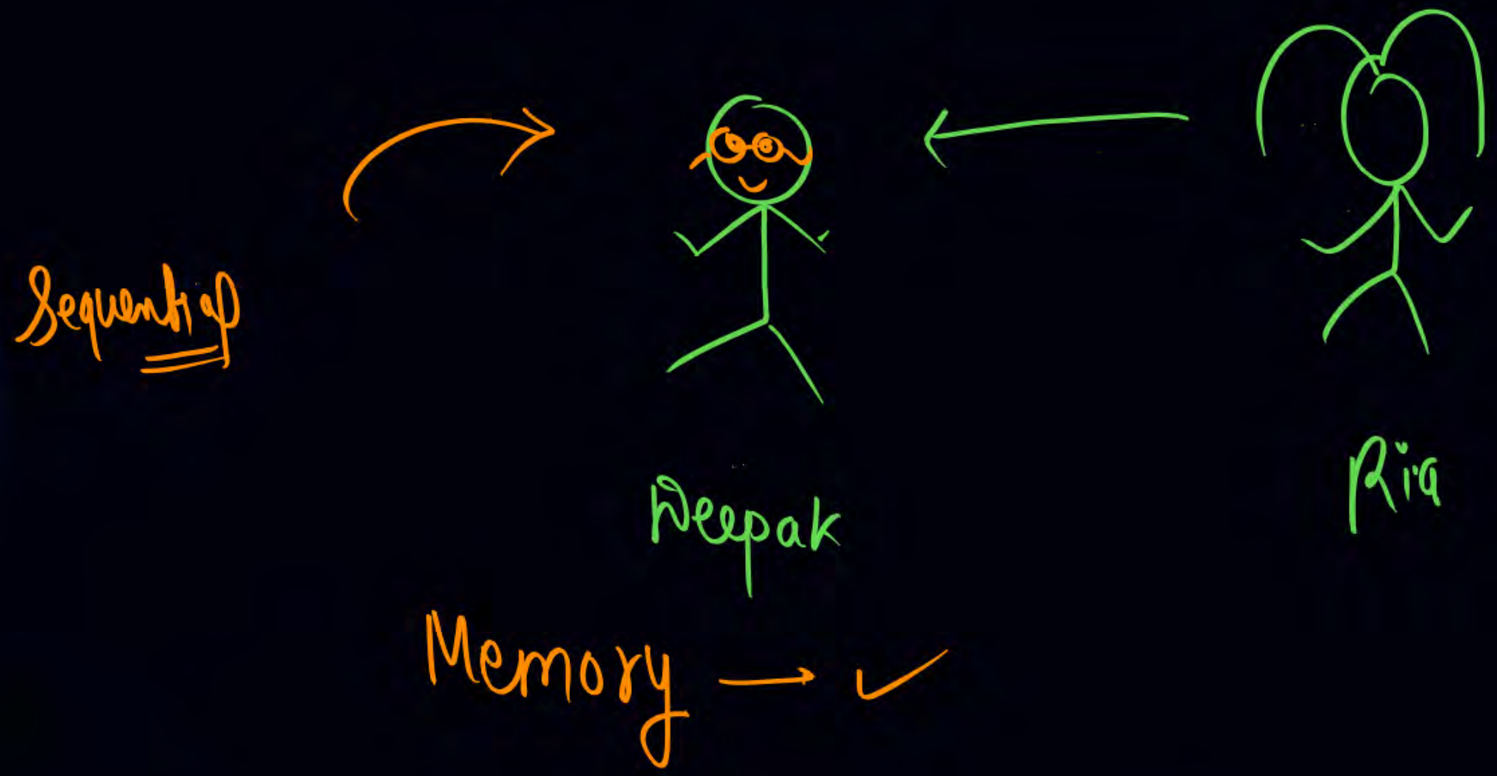
By- CHANDAN SIR

01 LATCHES

02 PRACTICE

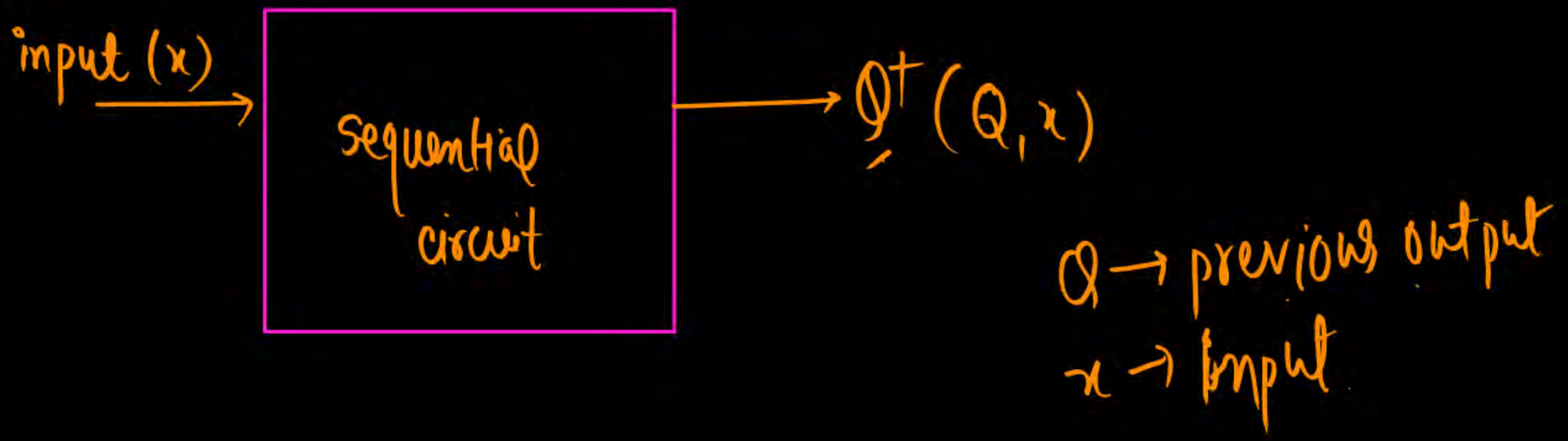
04 DISCUSSION

Sequential circuit :→

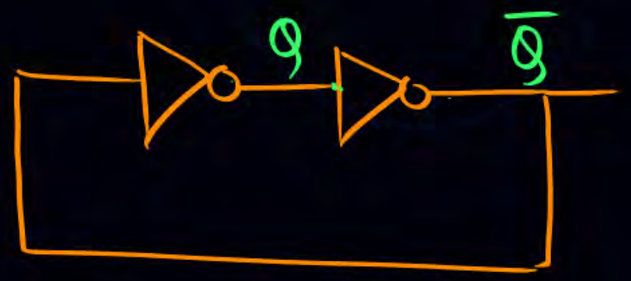


SEQUENTIAL CIRCUIT

- A circuit with feedback and memory are called sequential circuit.
- Output of the sequential circuit depends on previous output as well as present state of input.

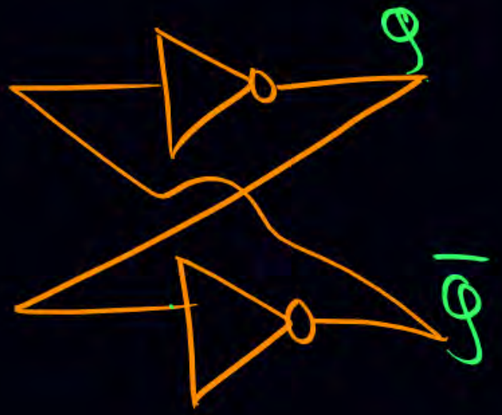


(i)



Basic memory element

(ii)



(A) i = ii

(B) i ≠ ii

(C) Mujhe nahi ata

(D) I am intreseted in Ria only

Sequential circuit

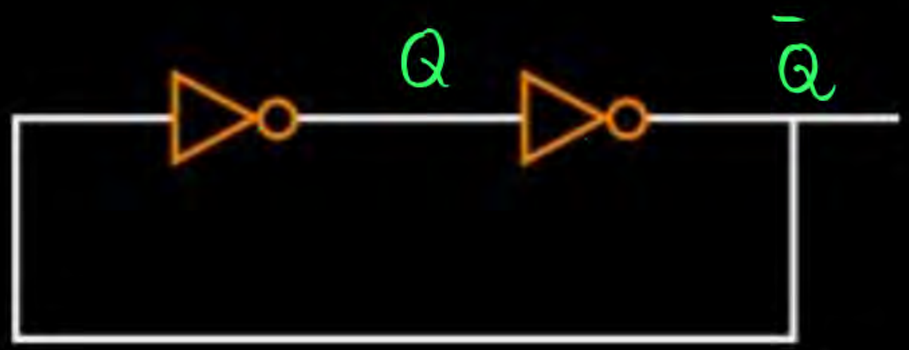
1. Latches → Basic memory element
2. Flip-Flops
3. Registers
4. Counters

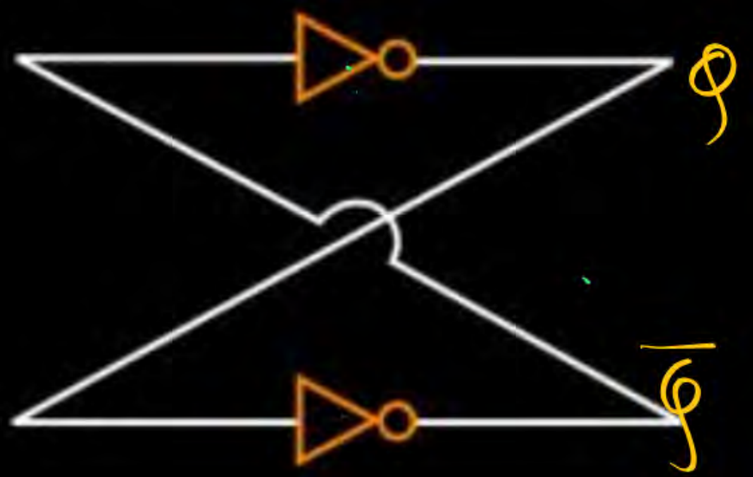
LATCHES

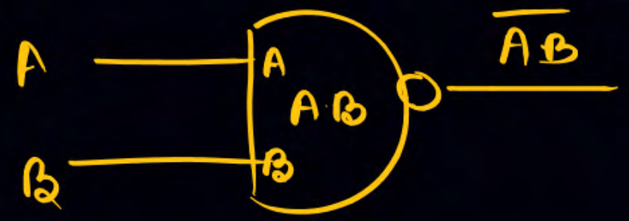
t.me/CJSIR

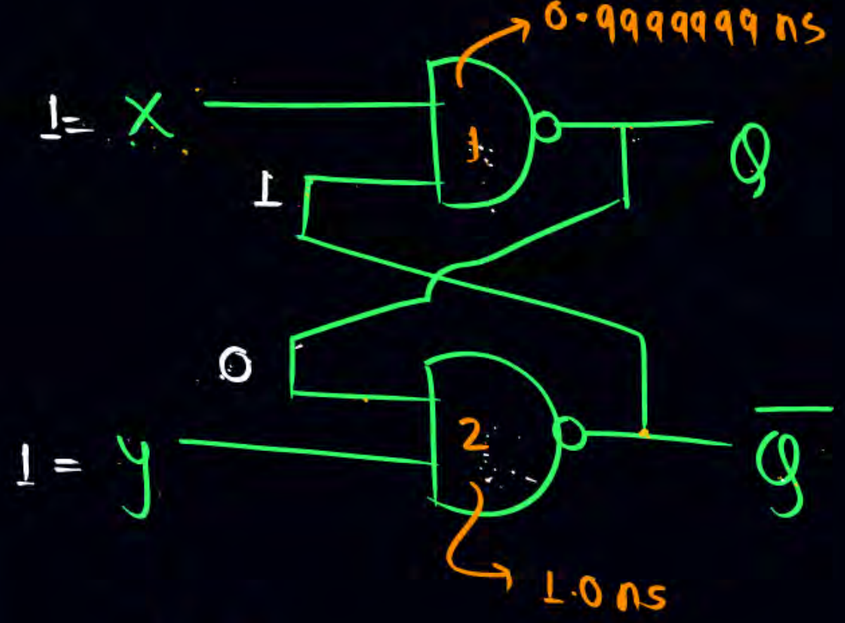
- Basic memory element

- Latches are level triggered
- Latches has two output which is complement of each other






A
B
A
B
A.B
$\overline{A.B}$



$1 \rightarrow 0$

$1 \rightarrow 1$

NAND

A	B	$y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

X	Y	Q	$\overline{Q}$	
0	0	1	1	✗ InValid
0	1	1	0	
1	0	0	1	
1	1	Q	$\overline{Q}$	→ HOLD

Racing Problem

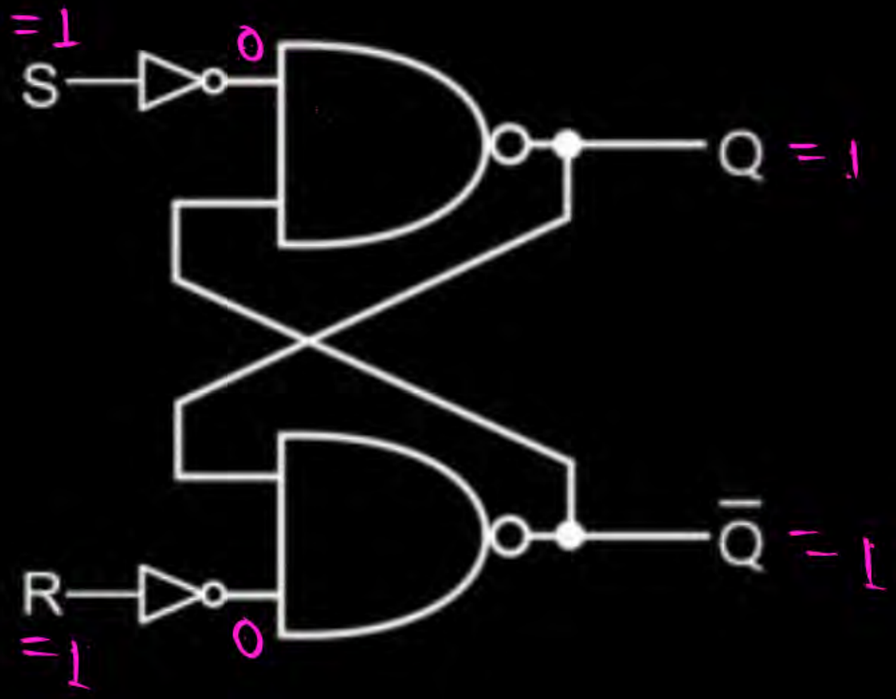

x
y
Q
Q̄
Q
Q̄

LATCHES

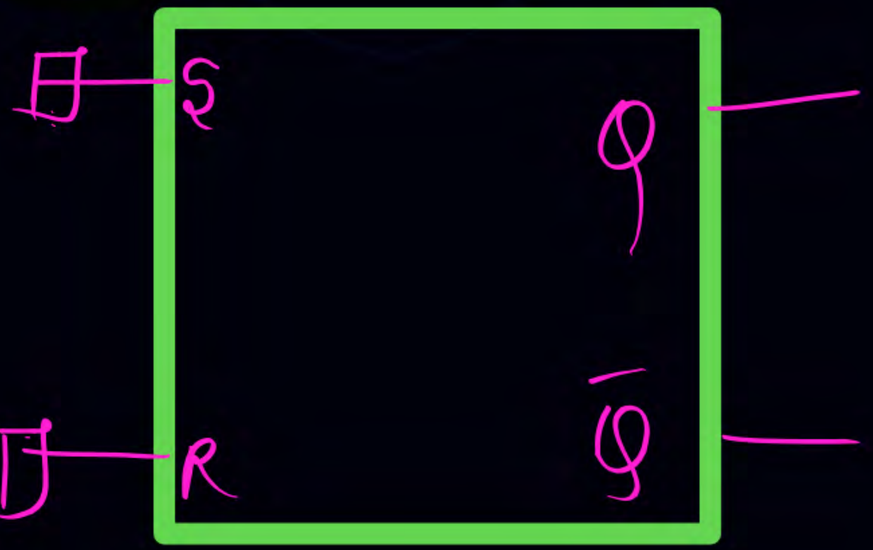
Note : Whenever $X = Y = 1$ is applied and invalid condition occurs than a NAND having lower propagation delay first change its output and other remain on its previous state are called racing problem or raising problem.

LATCHES

SR → Set-Reset Latch

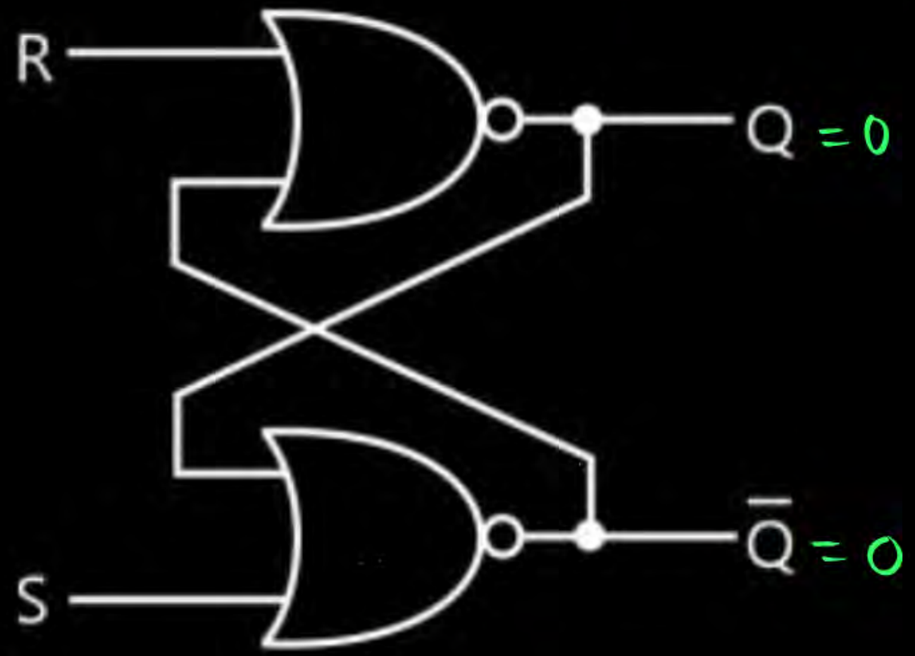


S	R	Q	$\overline{Q}$	
0	0	Q	$\overline{Q}$ →	HOLD
0	1	0	1	RESET
1	0	1	0	SET
1	1	X	X	(Invalid)


S
R
Q
$\bar{Q}$

LATCHES

S-R Latch by using NOR GATE



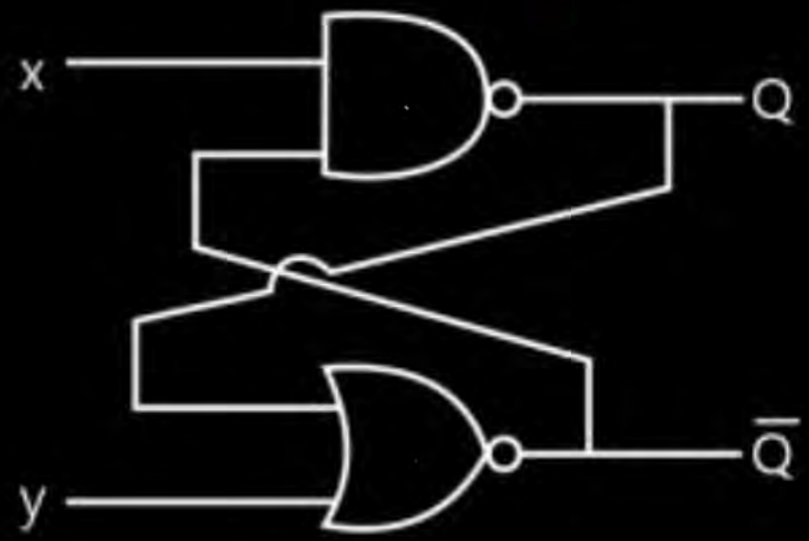
S	R	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	(HOLD)
0	1	0	1	(RESET)
1	0	1	0	(SET)
1	1	X	X	(Invalid Forbidden don't care Mai nahi khelrahe)

NOR

A	B	$y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

LATCHES

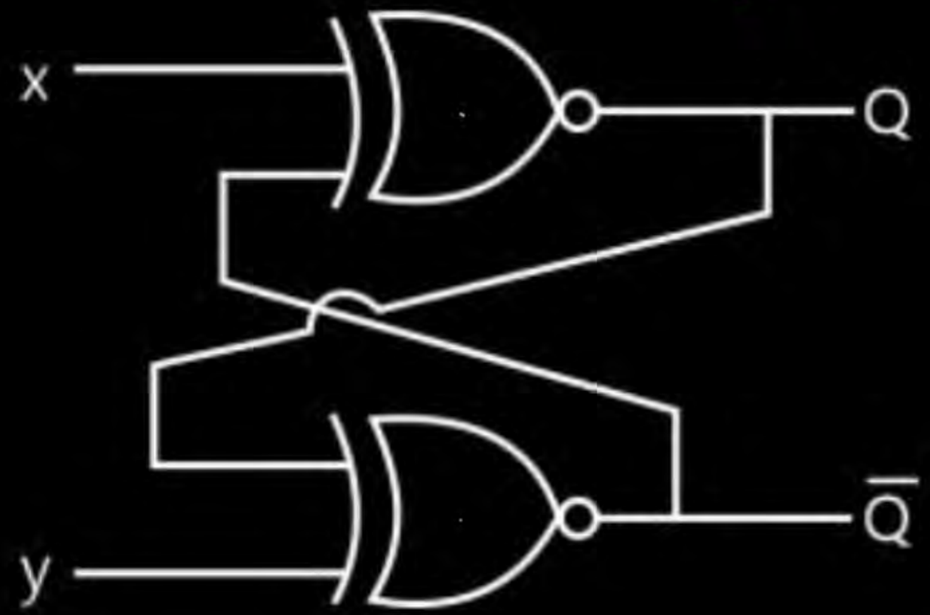
HW



X	Y	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

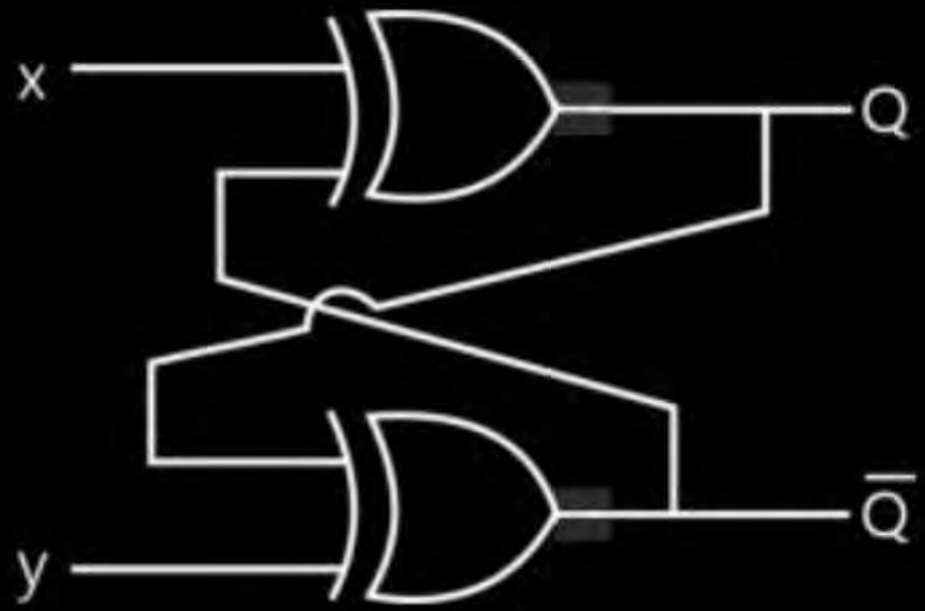
LATCHES

Hw



X	Y	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

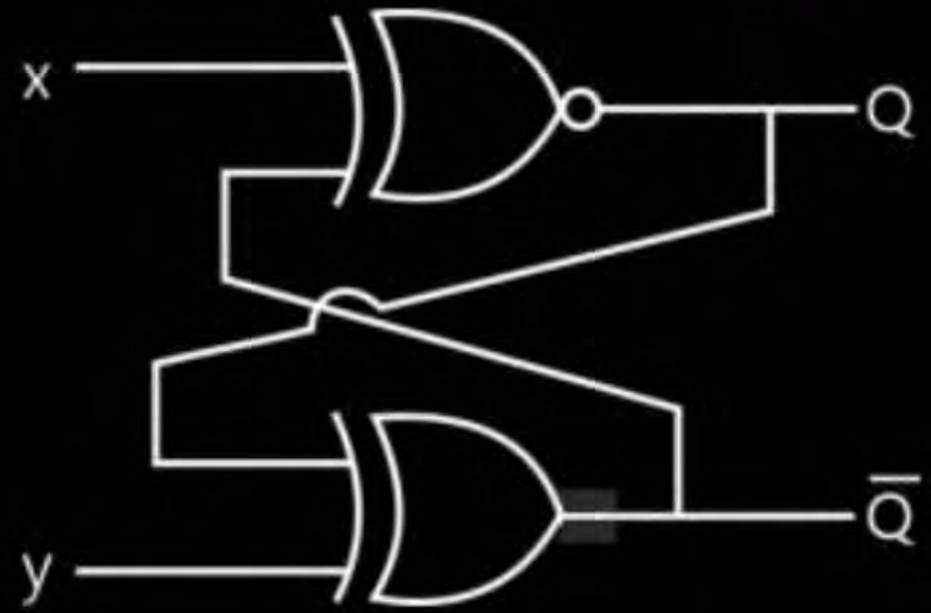
LATCHES



X	Y	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

LATCHES

Hw



X	Y	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

Thank you

GW

Soldiers !