

CS & IT ENGINEERING

Digital Logic



Sequential Circuit
Lecture No. 11



By- CHANDAN SIR

TOPICS TO BE COVERED

01 Synchronous counter

02 Designing

03 QUESTION PRACTICE

04 DUAL & SELF DUAL

05 DISCUSSION

time/cjsir

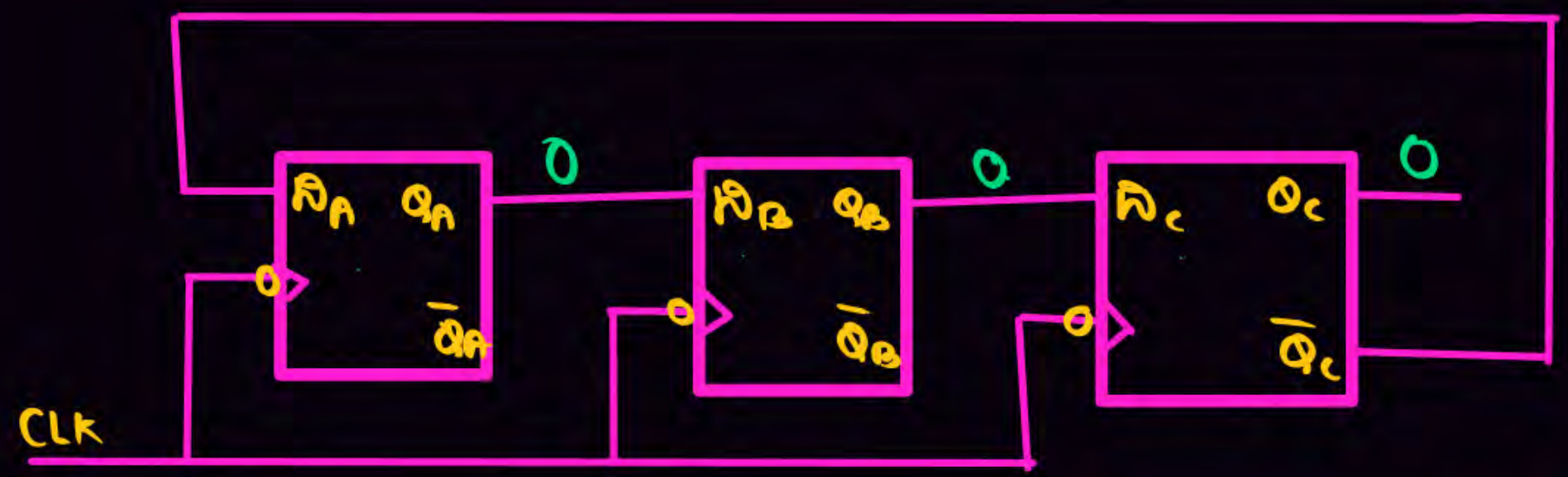
JOHNSON COUNTER

↳ Twisted Ring counter

↳ Creeping counter

↳ Mobies counter

↳ Walking counter



MOD 6

CLOCK	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1
6	0	0	0
7	1	0	0
8	1	1	0

3 bit Johnson counter

MOD-6

0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1

4 bit Johnson counter

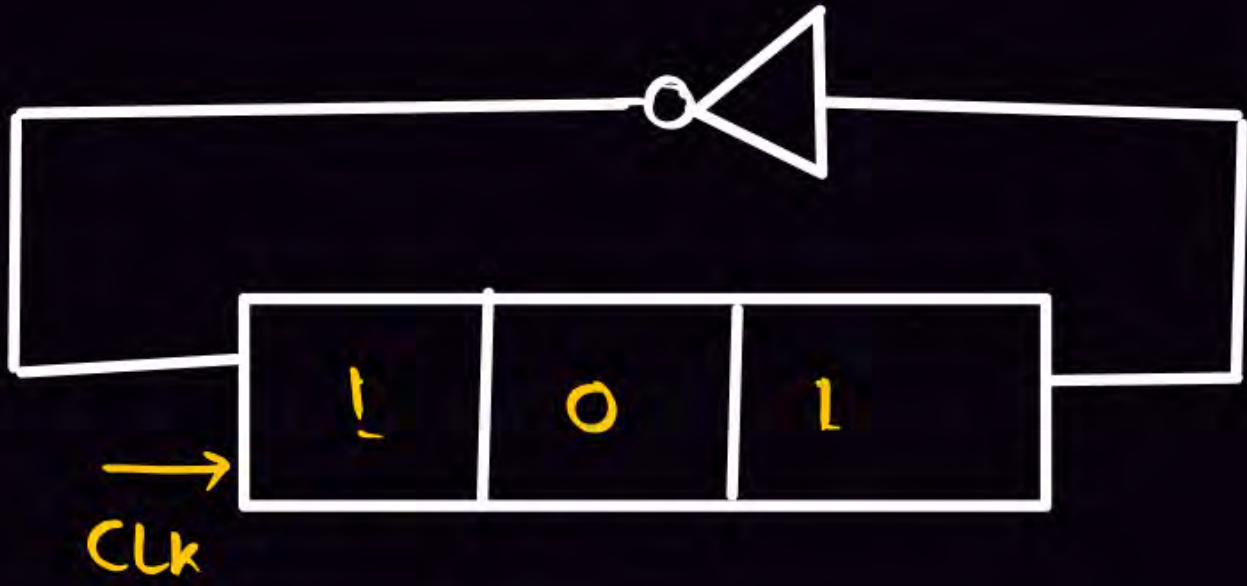
MOD-8

0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

N bit Johnson counter $\Rightarrow \text{MOD}(\text{used state}) = 2N$

$$\text{unused states} = 2^N - 2N$$

Symbolic Representation



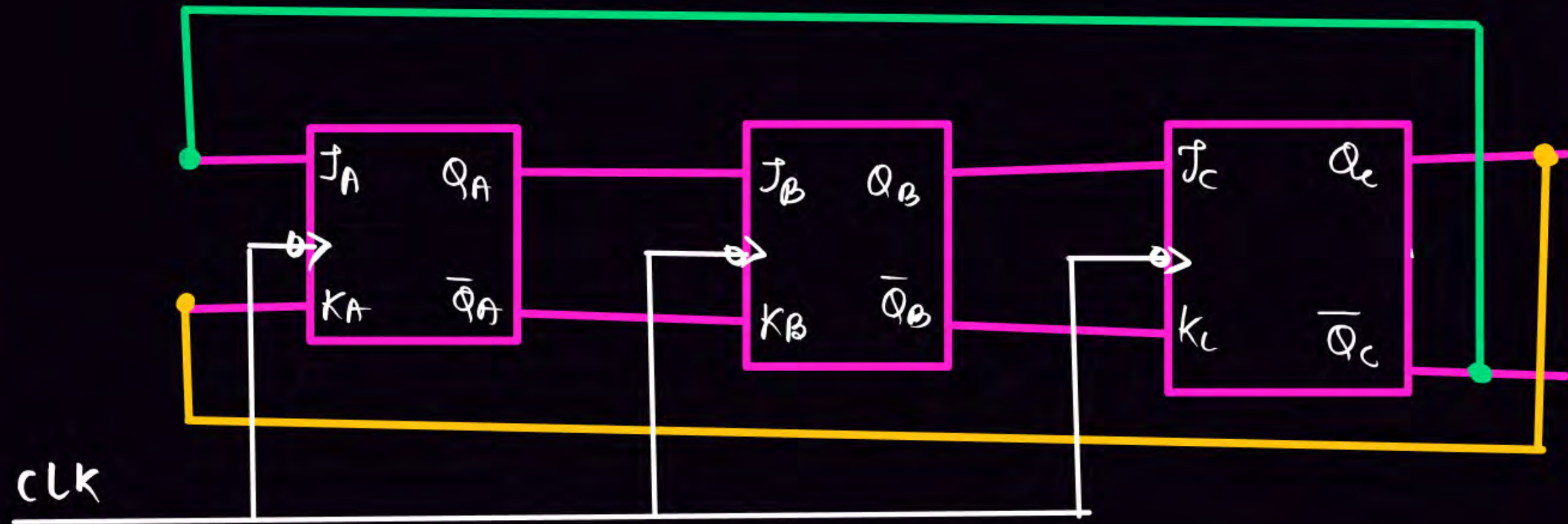
MOD-2 {

CLK	Q ₁	Q ₂	Q ₃
0	1	0	1
1	0	1	0
2	1	0	1
3	0	1	0
4	1	0	1
5			

Lockout problem :->

→ Whenever Johnson counter enters into its unused state, it will be trap or Lock into unused state, are called Lockout problem

Johnson counter by JK FF.



SYNCHRONOUS COUNTER DESIGN $\therefore \rightarrow$



Step 1 \rightarrow Write the Previous and Present state

Step 2 \rightarrow Write the excitation Table of Flip-Flop.

Step 3 \rightarrow Write the logical expression

Step 4 \rightarrow Minimization

Step 5 \rightarrow Hardware Implementation.

Question → Design a synchronous counter by using "T" FF which count the sequence $\Rightarrow 0 \rightarrow 3 \rightarrow 1 \rightarrow 2 \rightarrow 0 \rightarrow \dots$
 $\{ 00 \rightarrow 11 \rightarrow 01 \rightarrow 10 \rightarrow 00 \rightarrow \dots \}$

2 FF's required.

Step 1.
& Step 2.

Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	1	1	1	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	1	1	0

Step 3.
& Step 4

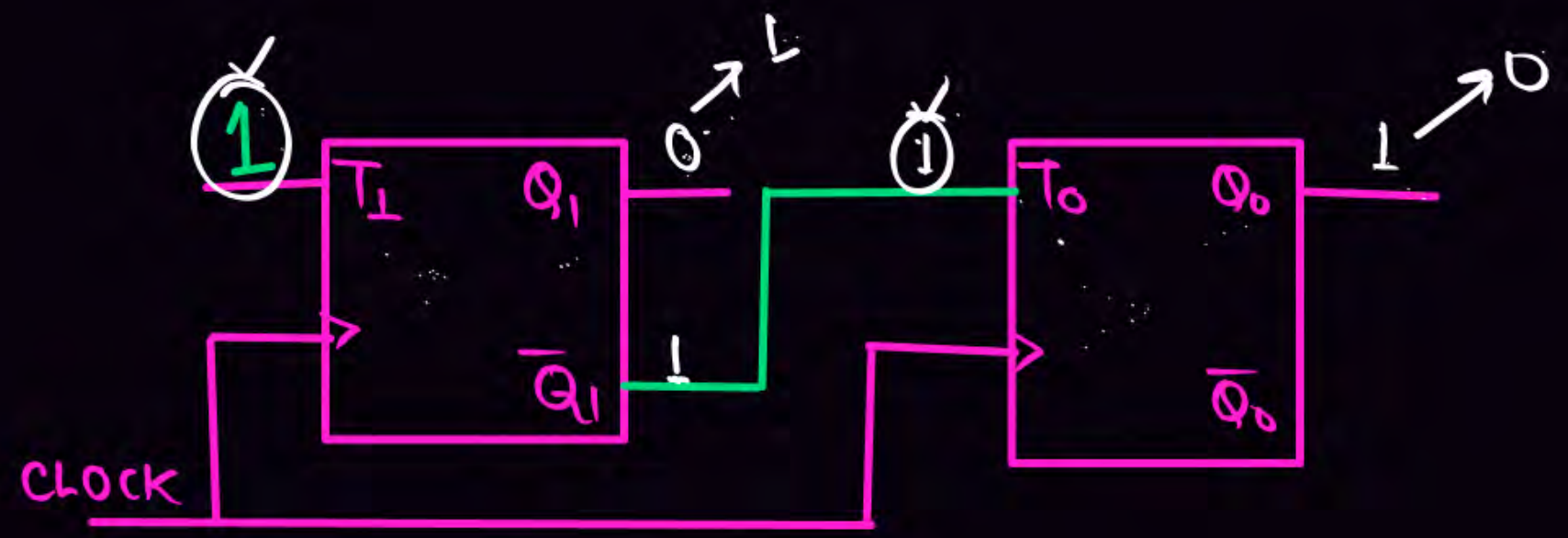
$T_1 = 1$

$$T_0 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0$$

$$T_0 = \bar{Q}_1 [\bar{Q}_0 + Q_0]$$

$T_0 = \bar{Q}_1$

Step 5:



Justification

Clock	Q_1	Q_0
0	0	0
1	1	1
2	0	1
3	1	0
4	0	0

Q Design a Synchronous counter by using "D" FF which count

$00 \rightarrow 11 \rightarrow 01 \rightarrow 00 \rightarrow \dots$

Method ①

Step 1
& Step 2.

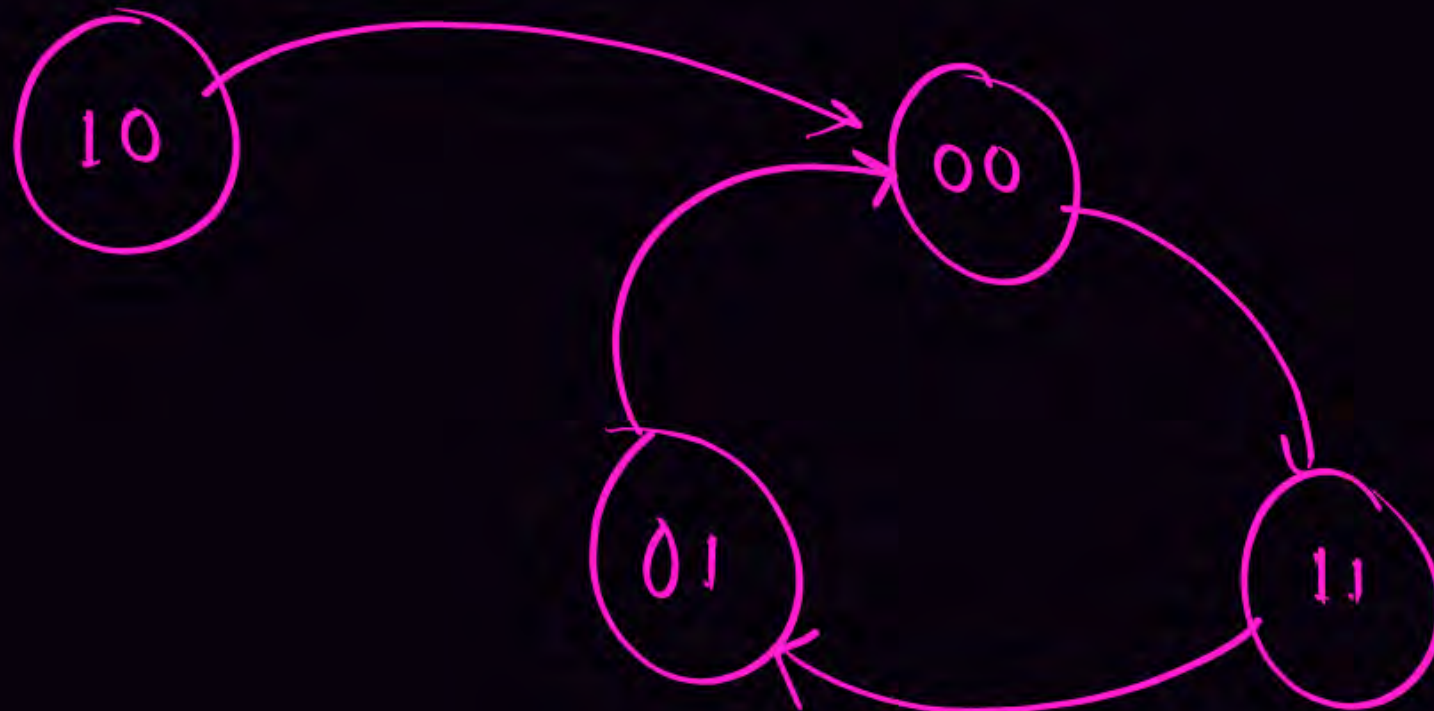
Q_1	Q_0	Q_1^+	Q_0^+	D_1	D_0
0	0	1	1	1	1
1	1	0	1	0	1
0	1	0	0	0	0

Step 3
& Step 4

$$D_1 = \overline{Q_1} \overline{Q_0}$$

$$D_0 = \overline{Q_1} \overline{Q_0} + Q_1 Q_0$$

$$D_0 = Q_1 \odot Q_0$$



4. L 1

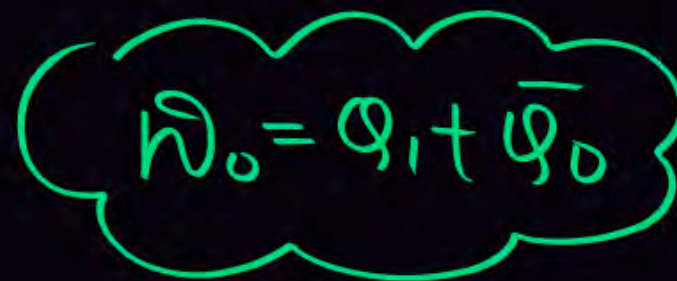
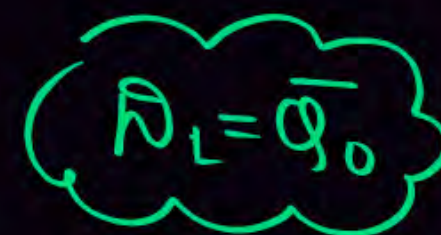
5. 0 1

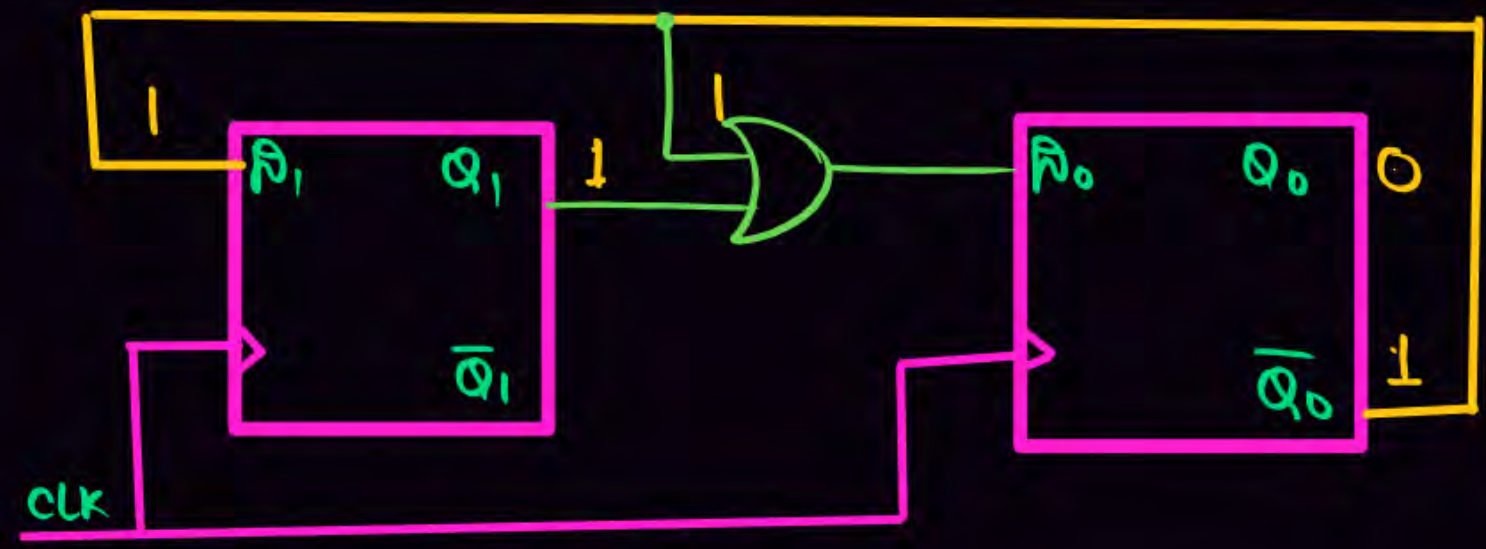
6. 0 0

Method (2)

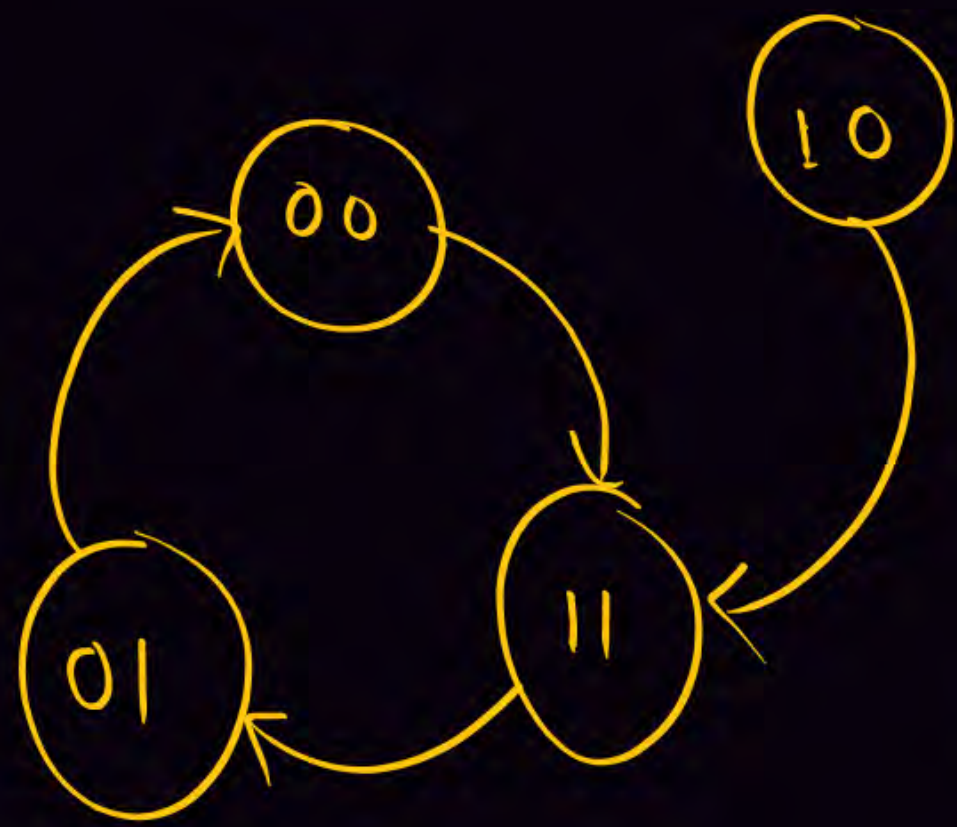
	Q_1	Q_0	Q_1^+	Q_0^+	R_1	R_0
0	0	0	1	1	1	1
1	0	1	0	0	0	0
2	1	0	x	x	x	x
3	1	1	0	1	0	1

R_1





Clock	Q_1	Q_0
0	0	0
1	1	1
2	0	1
3	0	0
4	1	1
5	0	1



No Lockout

Q Design a synchronous counter by using T-FF which count -

$000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101 \rightarrow 110 \rightarrow 111 \rightarrow 000 \rightarrow \dots$

$$T_0 = 1$$

$$T_1 = Q_0$$

$$T_2 = Q_1 Q_0$$

