CS & IT ENGINEERING

DIGITAL LOGIC

Combinational Circuit

By- CHANDAN SIR

Lecture No. 10

01 HS

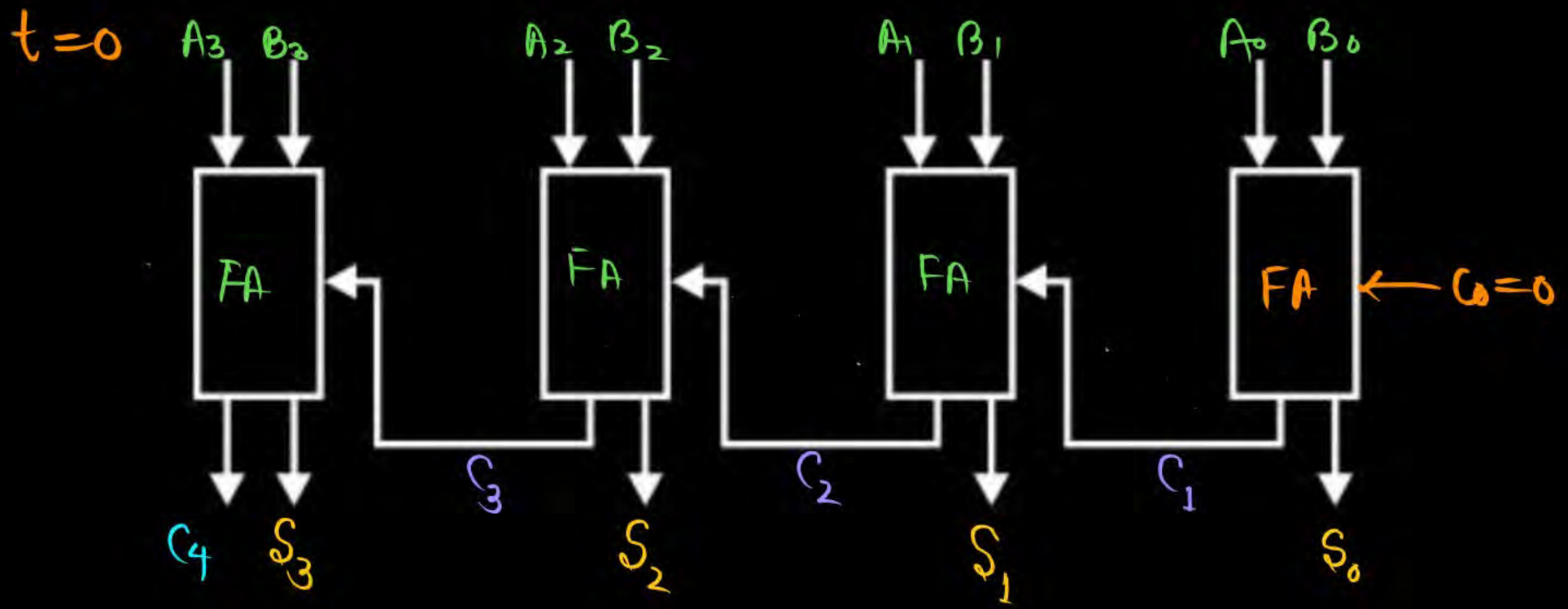
02 FS

03 SERIAL ADDER

04 PARALLEL ADDER

PARALLEL ADDER, LACA

PARALLEL ADDER [Ripple Carry Adder] :→



n bit Parallel adder

① $(n-1)$ FA + 1 HA

② n-FA

③ $(2n-1)$ HA + $(n-1)$ OR

Delay

* $T = (n-1)\,T_{carry} + \text{Max}\{T_{sum}, T_{carry}\}$

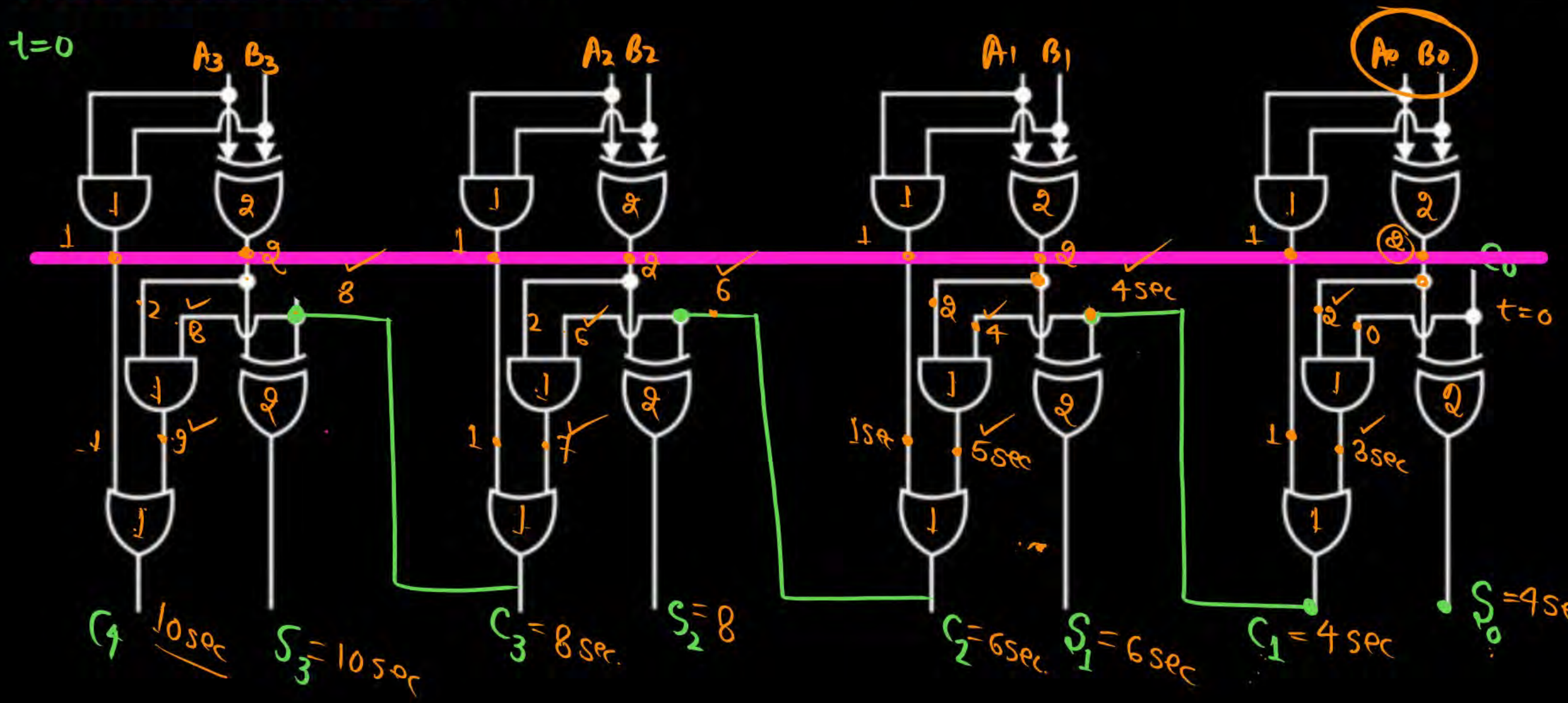

A B C
Sum
Carry

PARALLEL ADDER, LACA

PARALLEL ADDER [4 bit]

T_{XOR} = 2 second

$T_{AND} = T_{OR}$ = 1 second



$$T = (n-1)\{T_{AND} + T_{OR}\} + Max\{T_{sum}, T_{carry}\}$$

$$T = (4-1)\{1+1\} + Max\{4, 4\}$$

$$T = 3 \times 2 + 4$$

$$= \underline{10\,ns}$$

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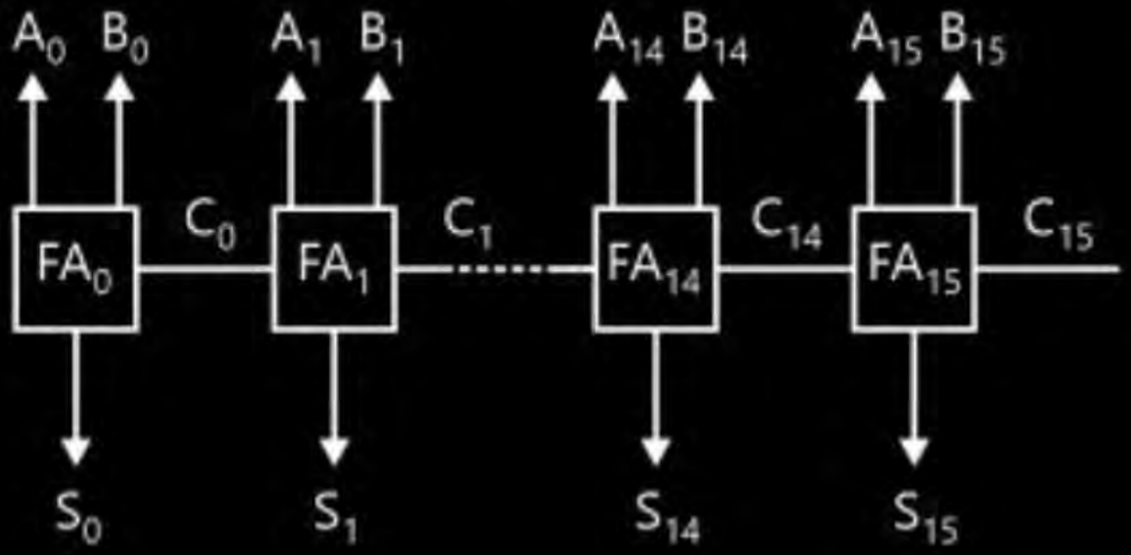
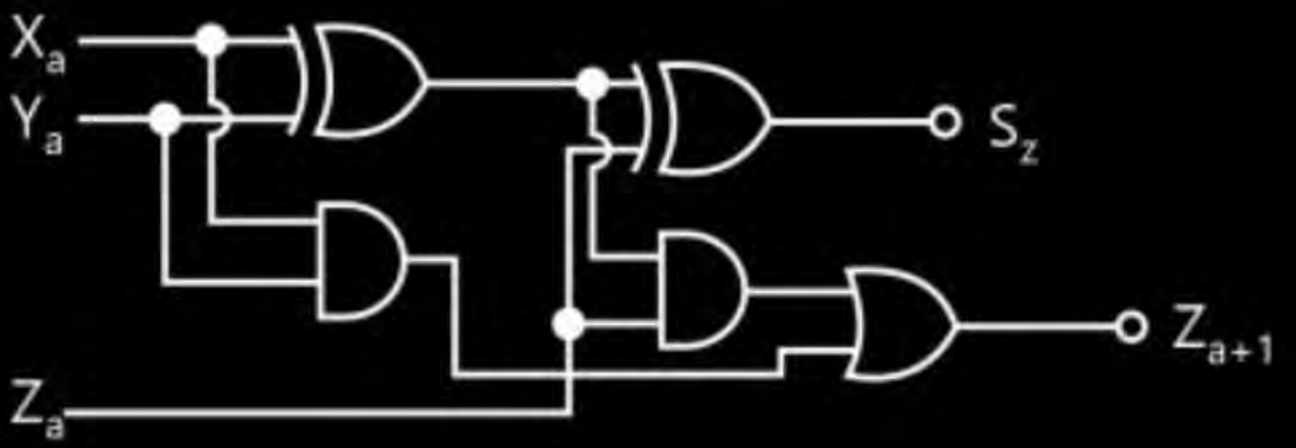
Q.3

$T_{sum} = 15$ ns $T_{carry} = 12$ ns $n = 16$

A 16-bit ripple carry adder is realized using 16 identical full adders (FA) as shown in the figure. The carry-propagation delay of each FA is 12 ns and the sum-propagation delay of each FA is 15 ns. The worst case delay (in ns) of this 16-bit adder will be _____ .





$$T = (n-1)T_{carry} + \max\{T_{sum}, T_{carry}\}$$

$$= (16-1) \times 12\,ns + \max\{15\,ns, 12\,ns\}$$

$$= 15 \times 12 + 15$$

$$= 195\,ns$$

PARALLEL ADDER, LACA

Q.4 A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders. The total propagation time of this 4-bit binary adder in microseconds is,

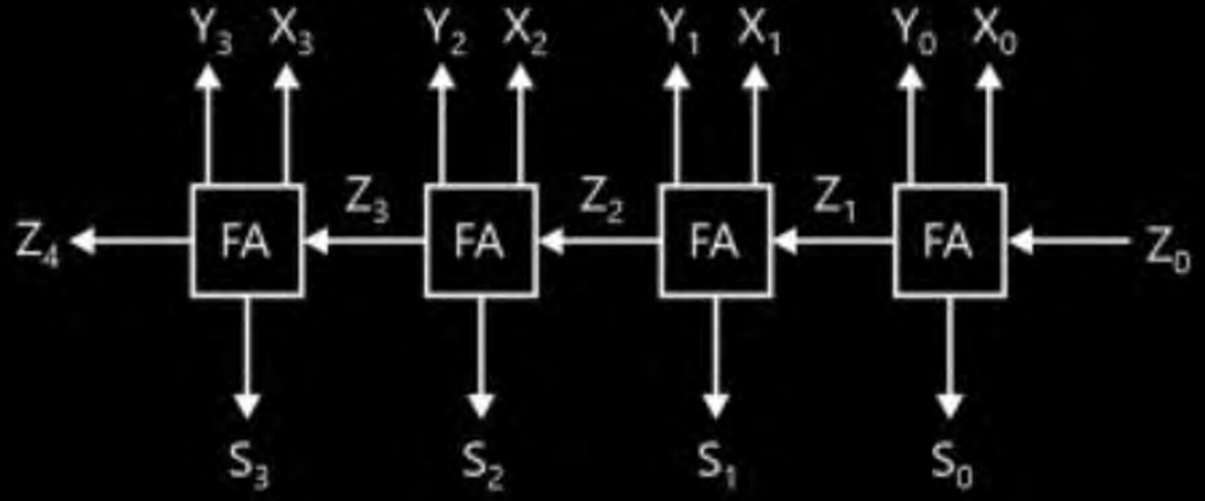


Figure-I

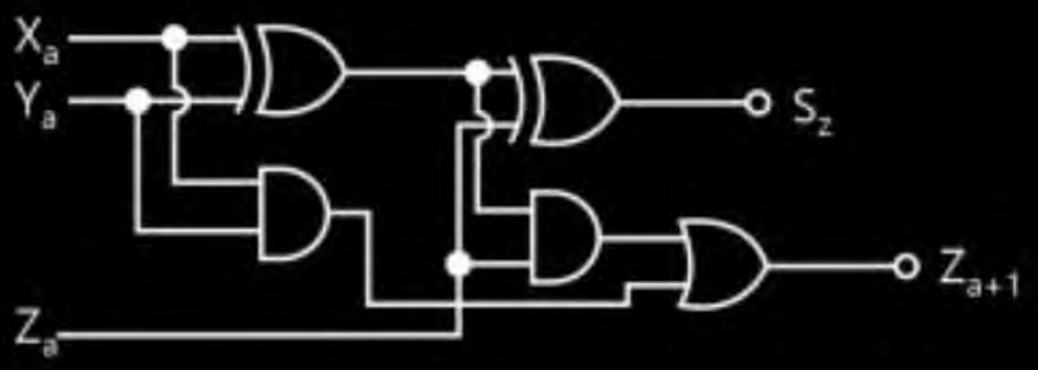


Figure-II

$T_{XOR} = 2.4\ \mu s$

$T_{AND} = T_{OR} = 1.2\ \mu s.$

$T_{sum} = 2T_{XOR}$

$T_{carry} = T_{XOR} + T_{AND} + T_{OR}$

$n = 4$

$$T = (n-1)\{T_{AND} + T_{OR}\} + Max\{T_{sum}, T_{carry}\}$$

$$= 3 \times \{1.2 + 1.2\} + 2 \times 2.4$$

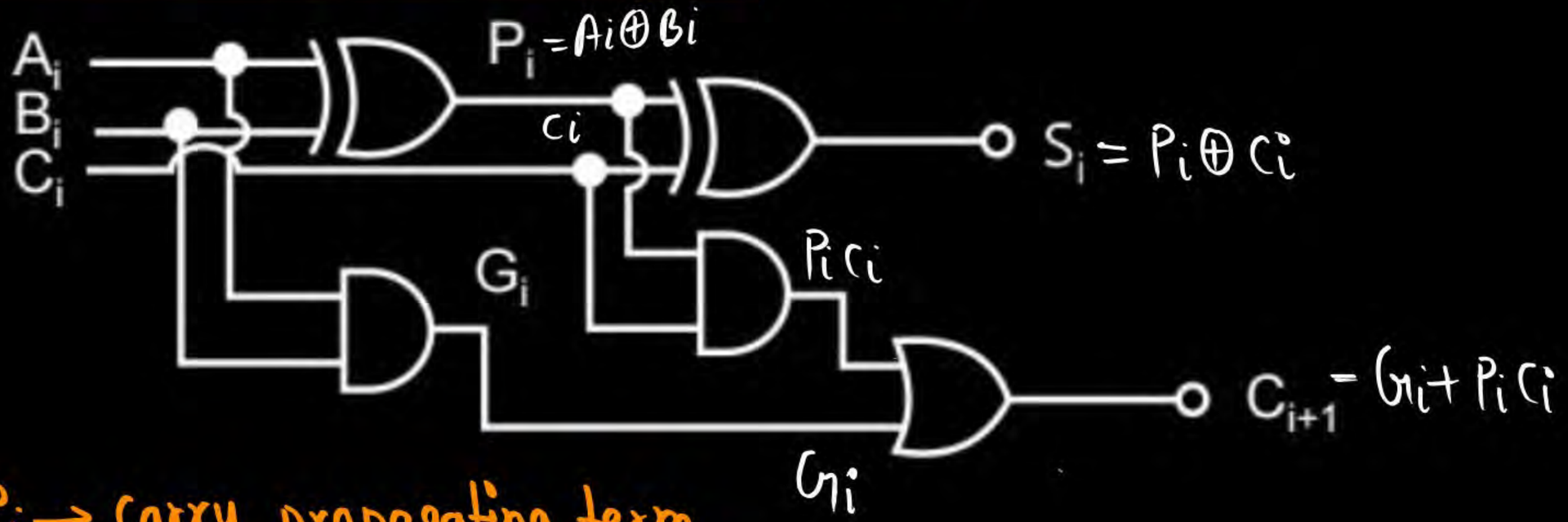
$$= 3 \times 2.4 + 4.8$$

$$= 12\ \mu s$$

PARALLEL ADDER, LACA

LOOK AHEAD CARRY ADDER [LACA]

→ fastest Adder among all the adder.



P_i → carry propagating term

G_i → carry generating term

✓ $P_i = A_i \oplus B_i$

$P_0 = A_0 \oplus B_0$

$P_1 = A_1 \oplus B_1$

$P_2 = A_2 \oplus B_2$

✓ $G_i = A_i B_i$

$G_0 = A_0 B_0$

$G_1 = A_1 B_1$

$G_2 = A_2 B_2$

✓ $S_i = P_i \oplus C_i$

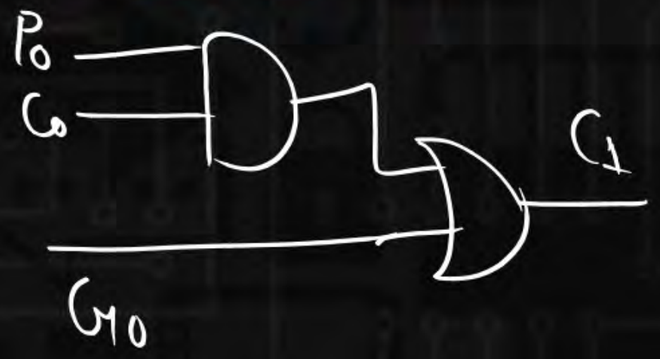
$S_0 = P_0 \oplus C_0$

$S_1 = P_1 \oplus C_1$

$S_2 = P_2 \oplus C_2$

$$C_{i+1} = G_i + P_i C_i$$

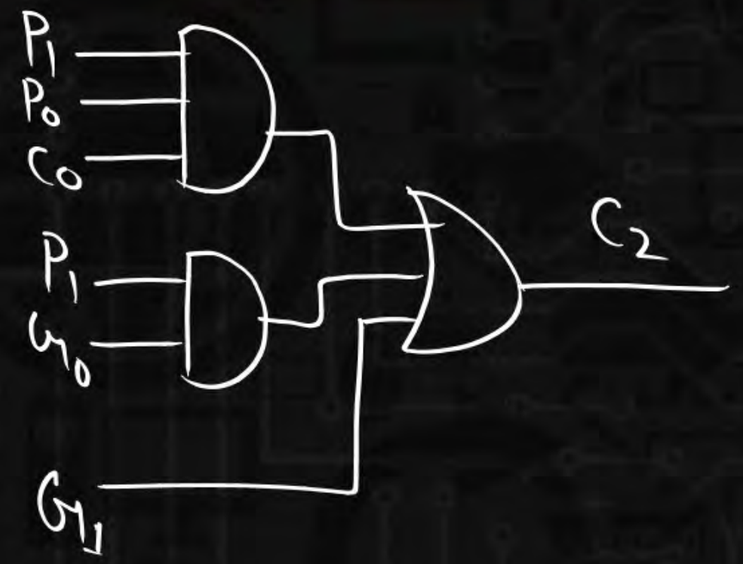
$C_1 = G_0 + P_0 C_0$



$C_2 = G_1 + P_1 C_1$

$C_2 = G_1 + P_1 [G_0 + P_0 C_0]$

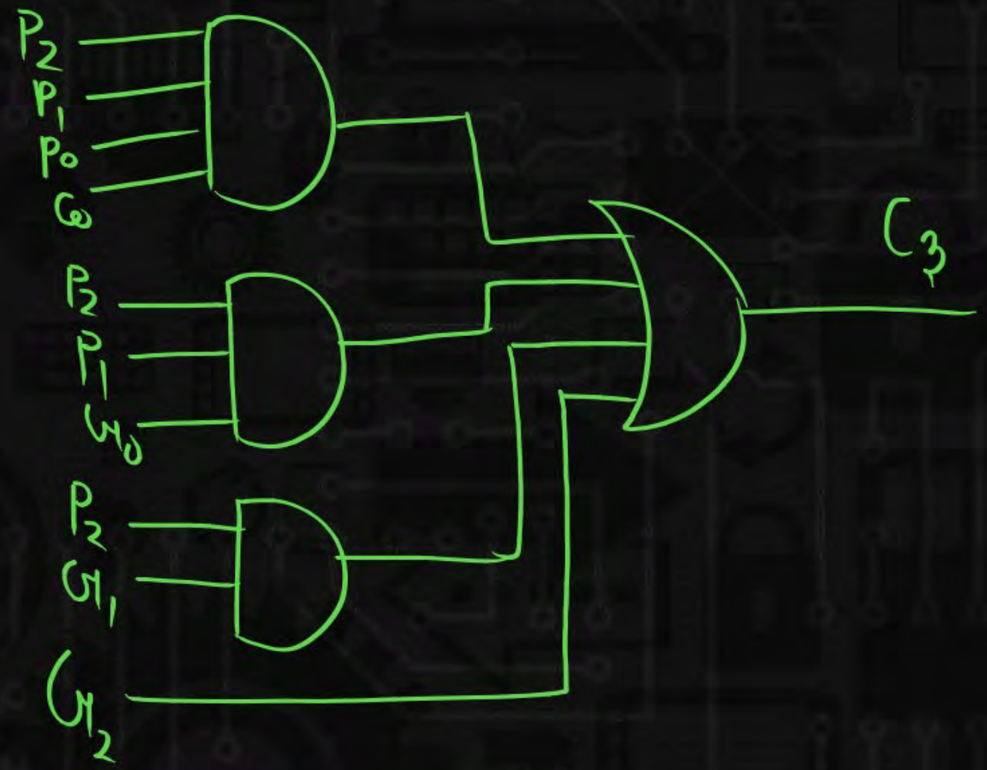
$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0$

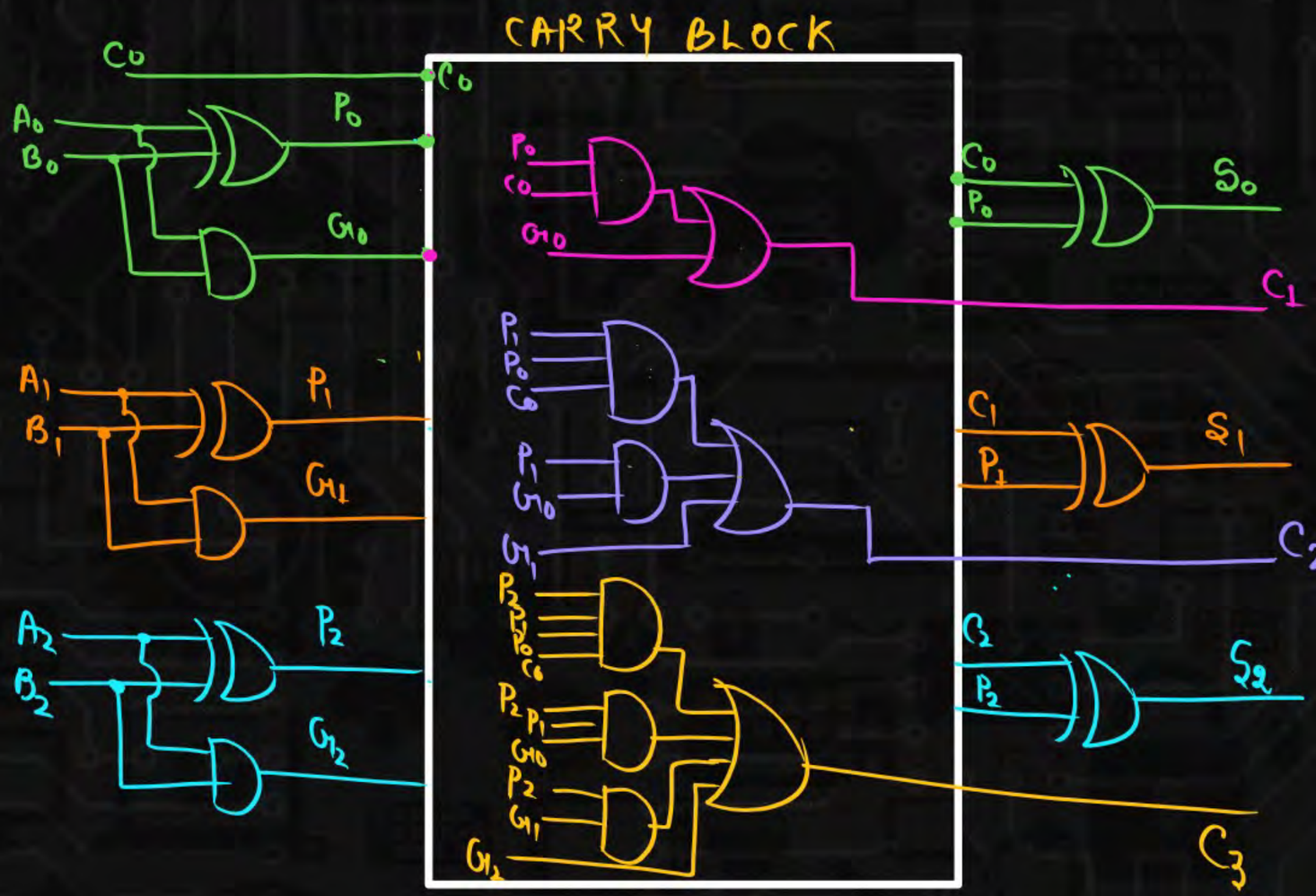


$$C_3 = G_2 + P_2 C_2$$

$$C_3 = G_2 + P_2 [G_1 + P_1 G_0 + P_1 P_0 C_0]$$

$$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$$





CARRY Block will be always two Level implementation.

Delay for carry Block

2T

For entire circuit

4T

'n' bit LACA

For Carry Block

No. of AND GATE = $\frac{n(n+1)}{2}$

No. of OR GATE = n

Multiplier :→

2bit

$A \rightarrow A_1\ A_0$

$B \rightarrow B_1\ B_0$

A X B

5 2

5 2

2	5X2	2X2
5X5	2X5	—

2 7 0 4

P_4 P_3 P_2 P_1 P_0

A_1 A_0

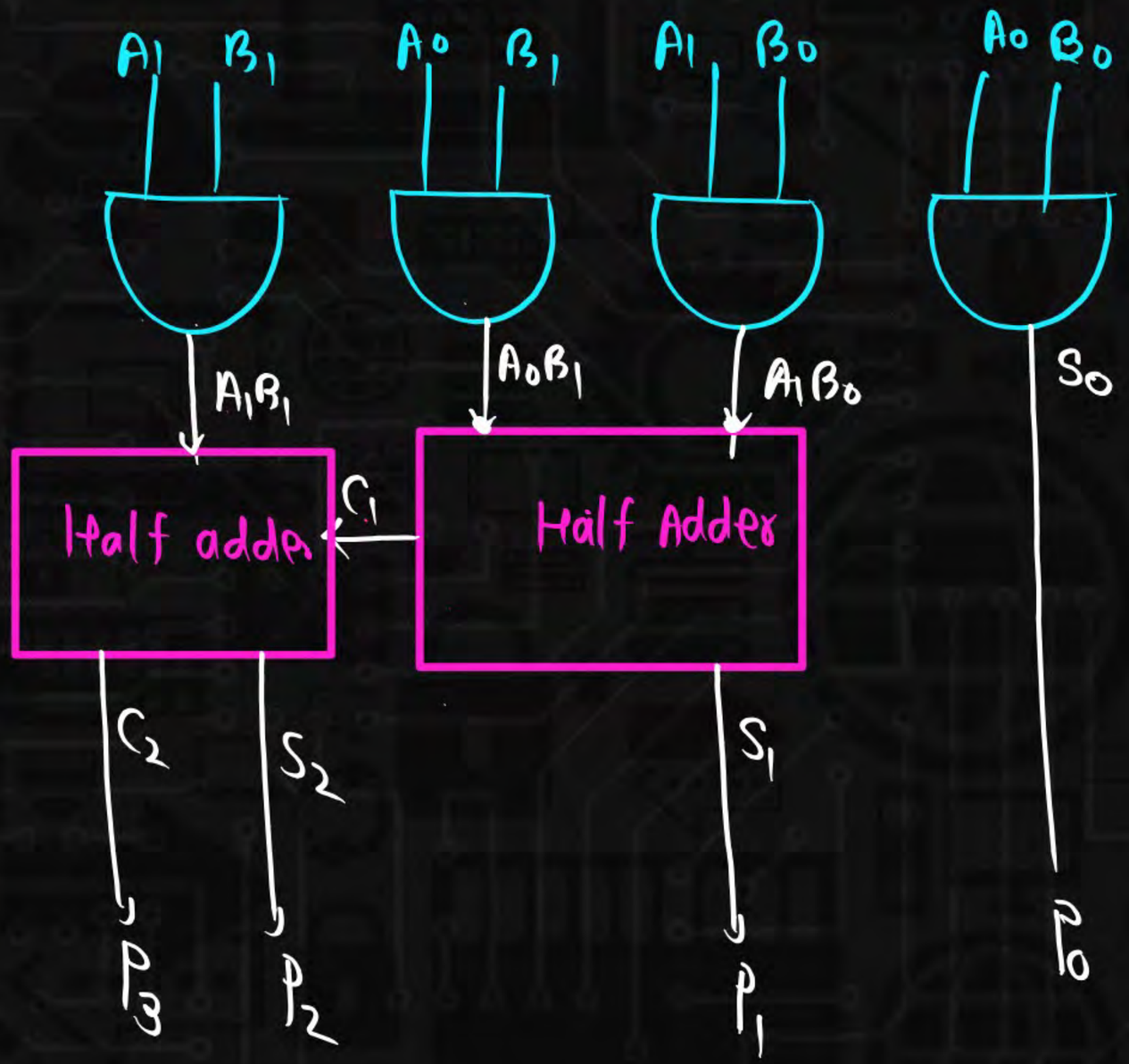
X B_1 B_0

C_1 A_1B_0 A_0B_0

A_1B_1 A_0B_1 —

C_2 S_2 S_1 S_0

C_2 → P_3, S_2 → P_2, S_1 → P_1, S_0 → P_0



H.W

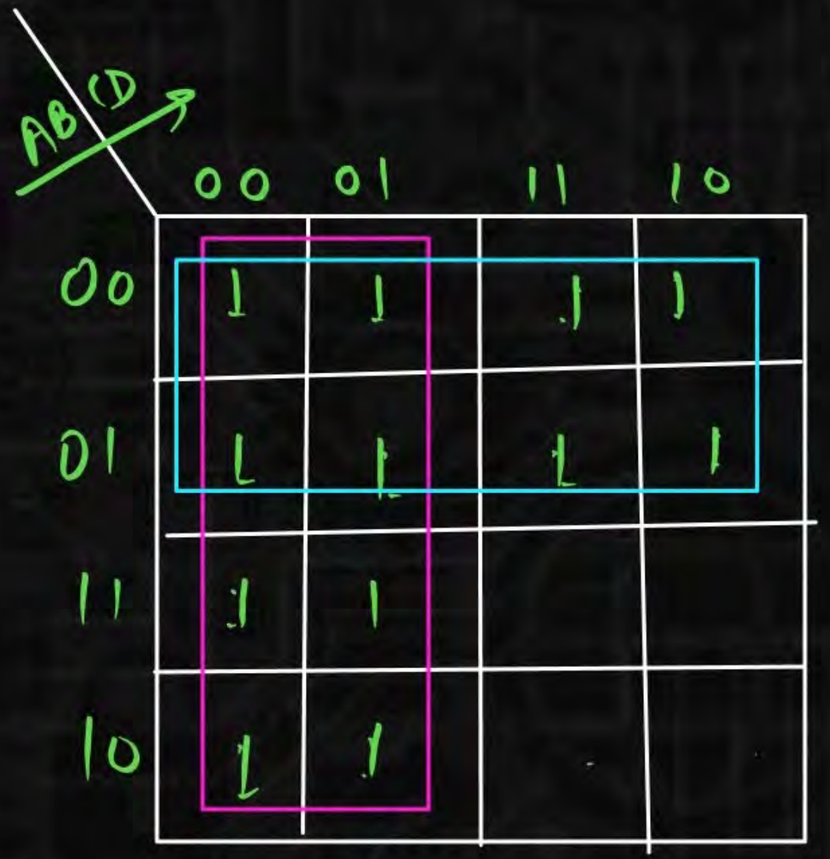
Design $A = A_2 A_1 A_0$

$\times$ $B = B_1 B_0$

Q Design a circuit in which 4 inputs A, B, C, D are there. if in decimal AB = X and CD = Y Then if $X \cdot Y \leq 3$ Then o/p will be high otherwise Low.

$X \cdot Y \leq 0$

A	B	C	D	x.y	z
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	1	1
0	1	1	0	2	1
0	1	1	1	3	1
1	0	0	0	0	1
1	0	0	1	2	1
1	0	1	0	4	0
1	0	1	1	6	0
1	1	0	0	0	1
1	1	0	1	3	1
1	1	1	0	6	0
1	1	1	1	9	0



$\bar{A}+\bar{C}$

$\overline{AC}$

combinational circuit { static circuit }

✓ Comparator

$(A>B)$ $X \Rightarrow A_1\bar{B}_1 + (A_1+\bar{B}_1)A_0\bar{B}_0$ → minimized

✓ $A_1\bar{B}_1 + (A_1 \odot B_1)A_0\bar{B}_0$ → Semiminimized

MUX, DE-MUX

Encoder, Decoder

HA

$S = A \oplus B$

$C_{carry} = AB$

(5)

FA

$Sum = A \oplus B \oplus C$

$Carry = \Sigma m(3,5,6,7)$

$= (A \oplus B)C + AB$

$= AB + AC + BC$

(9)

HS

$Diff = A \oplus B$

$Carry = \bar{A}B$

(5)

FS

$Diff = A \oplus B \oplus C$

$Carry = \Sigma m(1,2,3,7)$

$= \bar{A}B + (\overline{A \oplus B})C$

$= \bar{A}B + \bar{A}C + BC$

(9)

Serial adder

$n \cdot T$

Parallel add ✓

$T = (n-1) T_{carry} + Max\{T_{sum}, T_{carry}\}$

$T = (n-1)\{T_{AND} + T_{OR}\} + Max\{T_{sum}, T_{carry}\}$

LACA

Total Delay = 4T

Carry Block = 2T

Carry Block

$$AND = \frac{n(n+1)}{2}$$

$$OR = n$$

Thank you GW Soldiers !