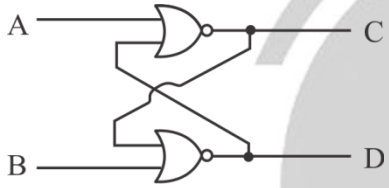
Branch :CSE & IT Batch : Hinglish

Subject : Digital Logic
Chapter : Sequential Circuit

DPP - 1

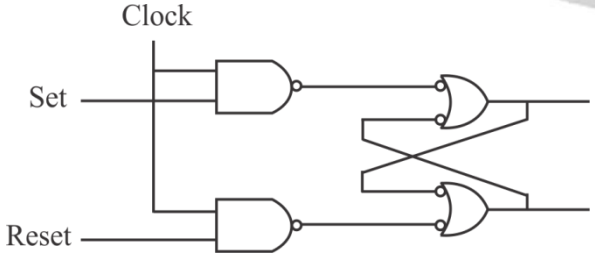
1. In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in
(a) $Q = 0, Q' = 1$
(b) $Q = 1, Q' = 0$
(c) $Q = 1, Q' = 1$
(d) Indeterminate states

2. In the circuit shown below, when inputs $A = B = 0$, the possible logic states of C and D are



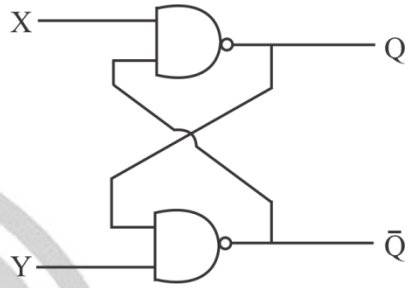
(a) $C = 0, D = 1$ or $C = 1, D = 0$
(b) $C = 1, D = 0$
(c) $C = 1, D = 1$ or $C = 0, D = 0$
(d) $C = 0, D = 1$

3. The two NAND gates before the latch circuit shown below, are used to



(a) act as buffers
(b) operate the latch faster
(c) avoid racing
(d) invert the latching action

4. In the circuit shown below, outputs $Q\bar{Q} = 01$, the possible values of X and Y are



(a) $X = 1, Y = 0$
(b) $X = 1, Y = 1$
(c) $X = 0, Y = 1$
(d) $X = 0, Y = 0$

5. Latch is a device with
(a) One stable state
(b) Two stable state
(c) Three stable state
(c) Infinite stable states

Answer Key

1. **(c)**
2. **(a)**
3. **(d)**
4. **(d)**
5. **(b)**