CS & IT ENGINEERING

DIGITAL LOGIC

Combinational circuit

Lecture No. 1

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TOPICS TO BE COVERED

Dual

01 Comparator

02 Question Practice

03 Discussion

Logic

+ve Logic $\xleftrightarrow{\text{Dual}}$ −ve Logic

+ve Logic:

$1 \rightarrow$ High

$0 \rightarrow$ Low

−ve Logic:

$1 \rightarrow$ Low

$0 \rightarrow$ High

$\left.\begin{array}{l} 1 \rightarrow 10V \\ 0 \rightarrow 5V \end{array}\right\}$ +ve Logic

$\left.\begin{array}{l} 1 \rightarrow 5V \\ 0 \rightarrow 0V \end{array}\right\}$ +ve Logic

$\left.\begin{array}{l} 1 \rightarrow 0V \\ 0 \rightarrow -5V \end{array}\right\}$ +ve Logic

$\left.\begin{array}{l} 1 \rightarrow -5V \\ 0 \rightarrow -10V \end{array}\right\}$ +ve Logic

$\left.\begin{array}{l} 1 \rightarrow 5V \\ 0 \rightarrow 10V \end{array}\right\}$ −ve Logic

$\left.\begin{array}{l} 1 \rightarrow 0V \\ 0 \rightarrow 5V \end{array}\right\}$ −ve Logic

$\left.\begin{array}{l} 1 \rightarrow -10V \\ 0 \rightarrow -5V \end{array}\right\}$ −ve Logic

AND GATE (+ve)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

R

Dual → +ve Logic $\xleftrightarrow{\text{Dual}}$ −ve Logic.

1. $1 \xleftrightarrow{\text{Dual}} 0$
2. AND $\xleftrightarrow{\text{Dual}}$ OR
3. $\cdot \xleftrightarrow{\text{Dual}} +$
4. NAND $\xleftrightarrow{\text{Dual}}$ NOR
5. X-OR $\xleftrightarrow{\text{Dual}}$ X-NOR
6. Buffer $\xleftrightarrow{\text{Dual}}$ Buffer
7. INVERTER $\xleftrightarrow{\text{Dual}}$ INVERTER

$0 \xleftrightarrow{\text{Dual}} 1$

$A \xleftrightarrow{\text{Dual}} A$

$\bar{A} \xleftrightarrow{\text{Dual}} \bar{A}$

$f = A \cdot 1$

$f^D = A + 0 = A$

$A \xleftrightarrow{\text{Dual}} A$

t.me/CJSIR

Ex 1. $f = AB + CD + \bar{E}F$

$$f^D = (A+B)\cdot(C+D)\cdot(\bar{E}+F)$$

Ex. 2. $f = \overline{ABC + DEF}$

$$f^D = \overline{(A+B+C)\cdot(D+E+F)}$$

$f = \overline{A+B}$ NOR

$f^D = \overline{A \cdot B}$ NAND

$$f^{D^D} = f$$

Ex

$$f = AB + CD$$

$$f^D = (A+B)\cdot(C+D)$$

$$f^{D^D} = AB + CD$$

$=$

$f = A$

$f^D = A$

$$\boxed{f^D = f}$$

Self Dual

$n=1$

$$\left\{ \begin{matrix} A \\ \bar{A} \\ 0 \\ 1 \end{matrix} \right\}$$

Self Dual $= 2$

$n=2$

$\bar{A}\bar{B}$	$\bar{A}+\bar{B}$	A	0
$\bar{A}B$	$\bar{A}+B$	$\bar{A}$	1
$A\bar{B}$	$A+\bar{B}$	B	$\bar{A}B+A\bar{B}$
AB	$A+B$	$\bar{B}$	$\bar{A}\bar{B}+AB$

Self Dual $= 4$

₹0.25

"n" Variables $\longrightarrow 2^{2^n} \longrightarrow 2^{2^{n-1}}$

Expression

Self Dual Expression

COMBINATIONAL CIRCUIT

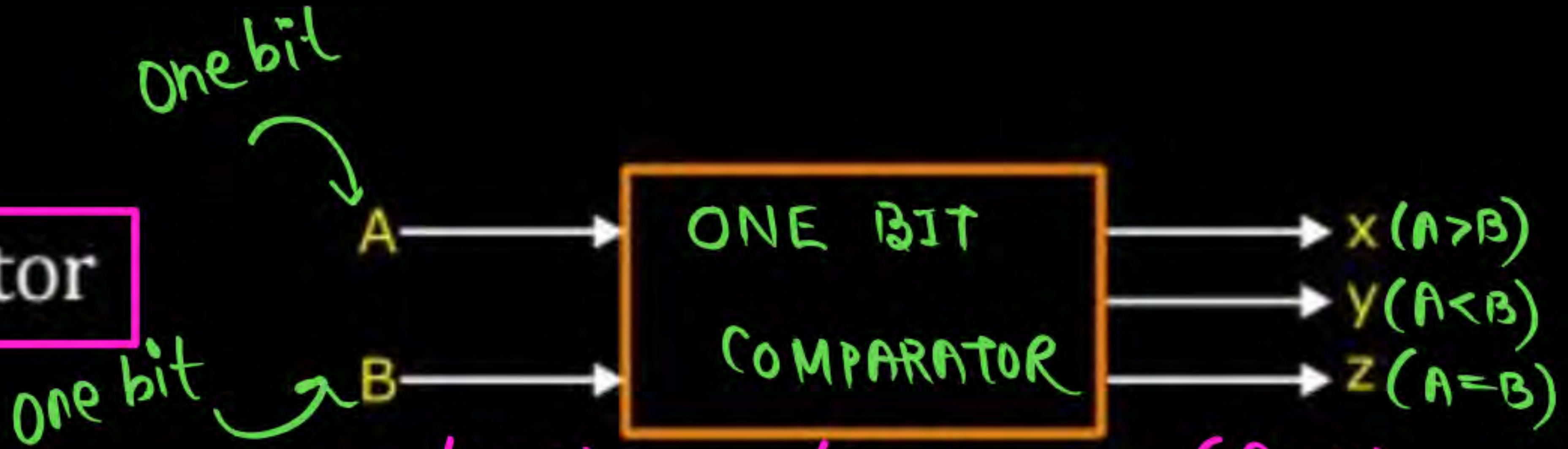
- A circuit without feedback or memory are called Combinational circuit.
- Static circuit

DESIGNING OF COMBINATIONAL CIRCUIT

Step 1. Find the number of inputs and outputs.
Step 2. Write the truth table.
Step 3. Write the logical expression.
Step 4. Minimize the logical expression.
Step 5. Hardware implementation.

Magnitude COMPARATOR

1. Design a one-bit comparator



Step 1.

Step 2. Truth Table

A	B	X (A>B)	Y (A<B)	Z (A=B)
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

COMPARATOR

DESIGNING OF COMBINATIONAL CIRCUIT

Step 3. Logical expression

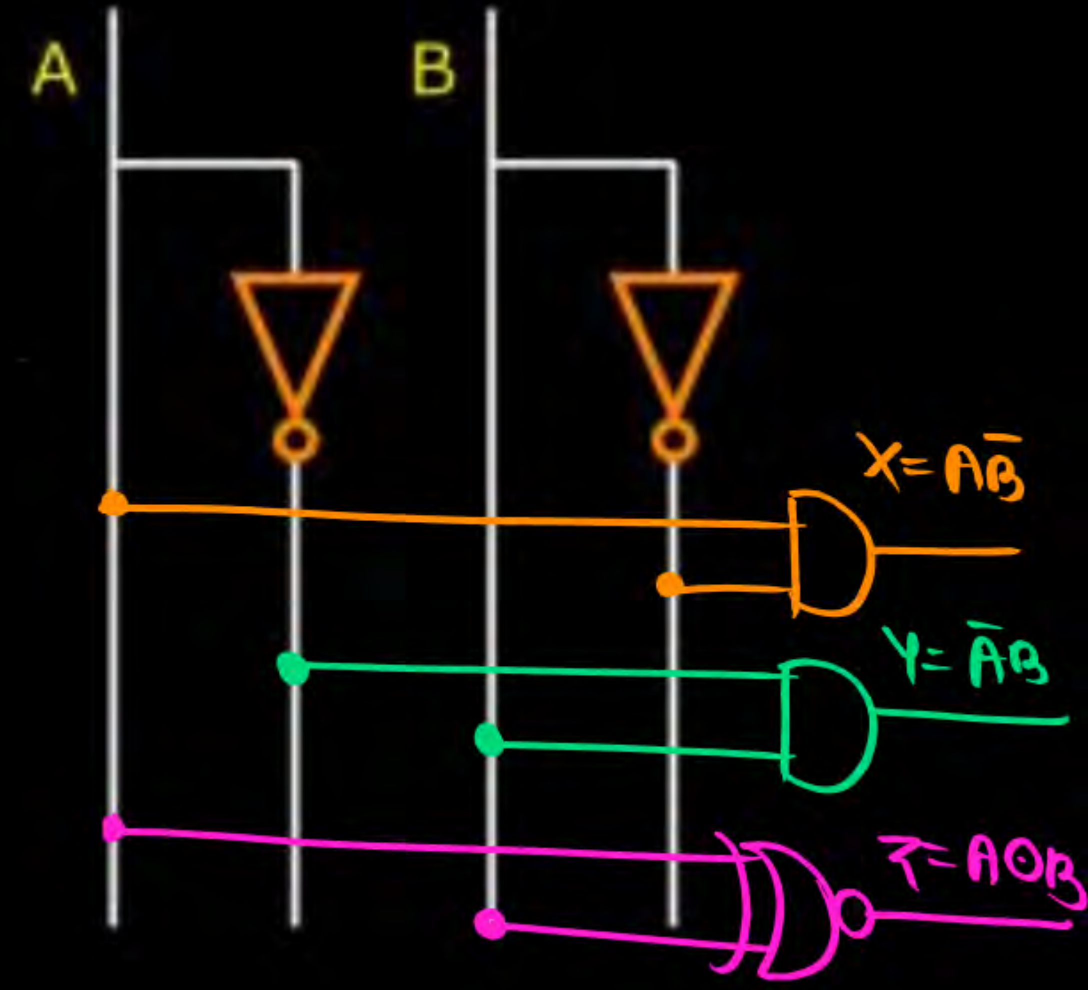
$X(A > B) = A\overline{B}$

$Y(A < B) = \overline{A}B$

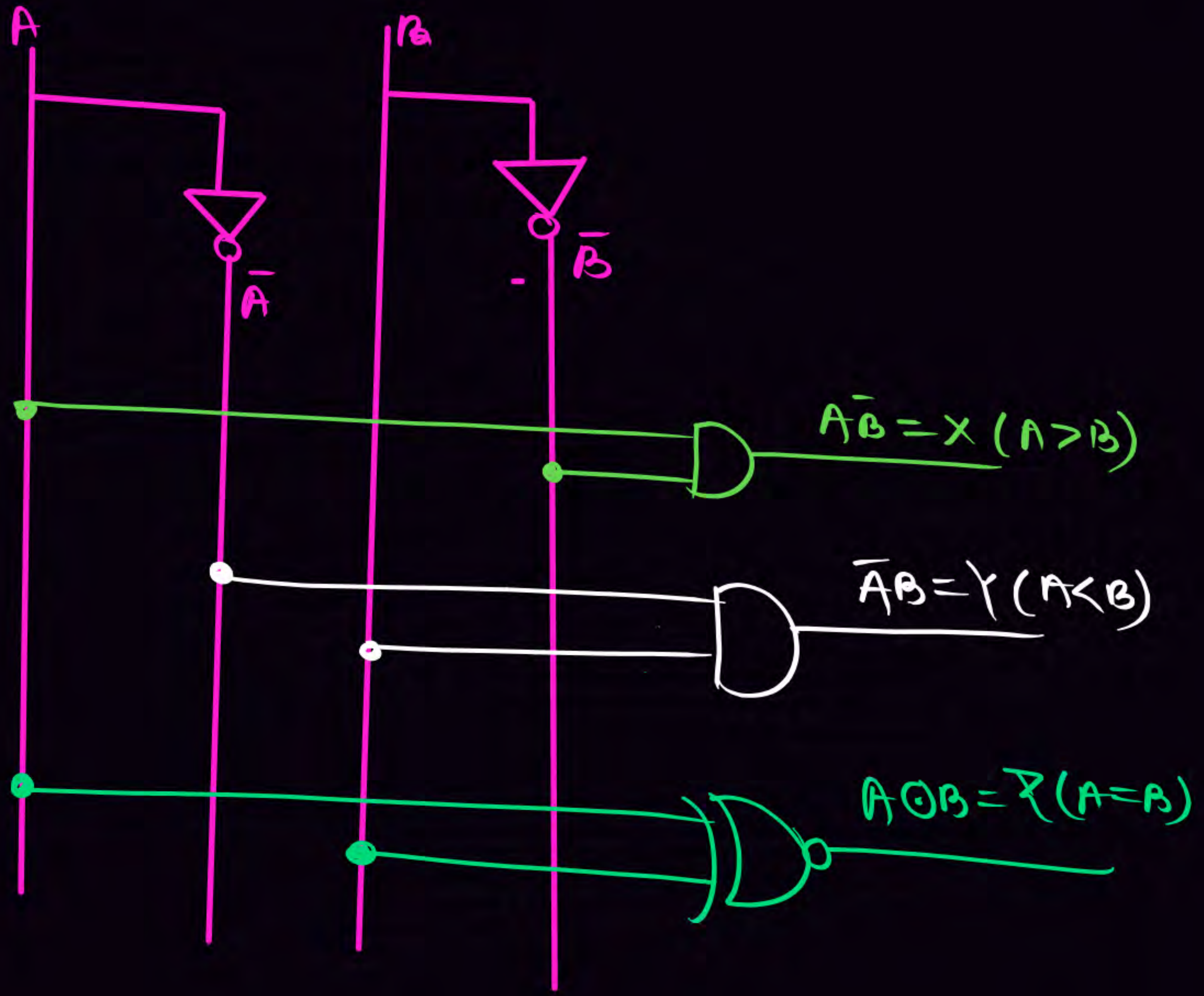
$Z(A = B) = \overline{A}\,\overline{B} + AB = A \odot B$

Step 4. Minimization → Already minimize.

Step 5. Hardware implementation



Step 5.



TWO BIT COMPARATOR

Decimal	Binary
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

$$\overbrace{A_1 \quad A_0}^{A} \qquad \overbrace{B_1 \quad B_0}^{B}$$

$$\underset{3}{1\ 1} > \underset{2}{1\ 0}$$

COMPARATOR

2. Design a two-Bit comparator?

Step 1.

Step 2. Truth table

	A		B		A > B	A < B
	A_1	A_0	B_1	B_0	x	y
0 →	0	0	0	0		
1 →	0	0	0	1		
2 →	0	0	1	0		
3 →	0	0	1	1		
4 →	0	1	0	0		
5 →	0	1	0	1		
6 →	0	1	1	0		
7 →	0	1	1	1		
8 →	1	0	0	0		
9 →	1	0	0	1		
10 →	1	0	1	0		
11 →	1	0	1	1		
12 →	1	1	0	0		
13 →	1	1	0	1		
14 →	1	1	1	0		
15 →	1	1	1	1		

(A = B
z

COMPARATOR

DESIGNING OF COMBINATIONAL CIRCUIT

Step 3. Logical expression

$X(A > B) = \Sigma m($

$Y(A < B) = \Sigma m($

$Z(A = B) = \Sigma m($

COMPARATOR

DESIGNING OF COMBINATIONAL CIRCUIT

Step 4. Minimization

For X

$A_1A_0 \backslash B_1B_0$	00	01	11	10
00				
01				
11				
10				

For Y

$A_1A_0 \backslash B_1B_0$	00	01	11	10
00				
01				
11				
10				

COMPARATOR

DESIGNING OF COMBINATIONAL CIRCUIT

Step 4. Minimization

For Z

$A_1A_0 \backslash B_1B_0$	00	01	11	10
00				
01				
11				
10				

Thank you

GW Soldiers !