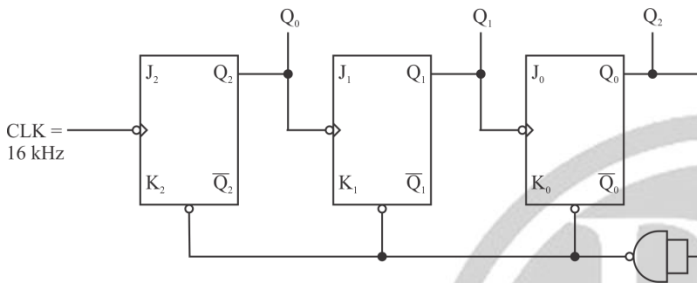


## Subject : Digital Logic

DPP - 04

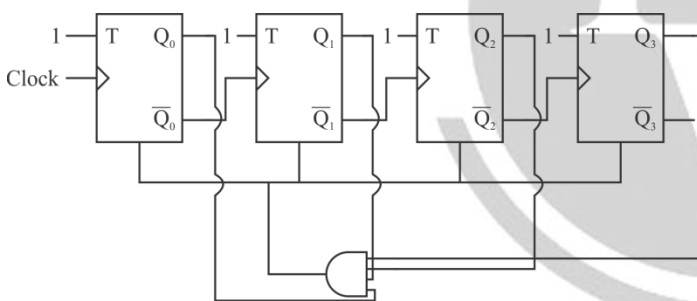
## Chapter : Sequential Circuits

1. What is the output signal frequency of the following counter if the clock signal frequency is 16 kHz? All 'J' and 'K' inputs are connected to 1.



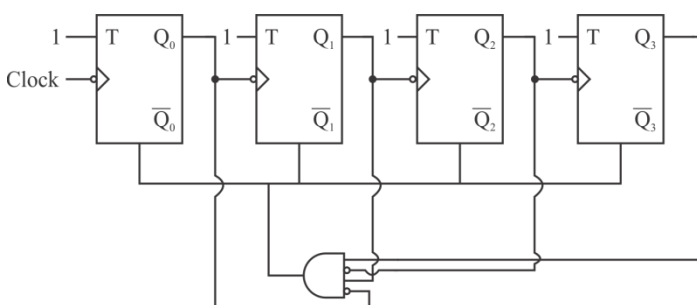
- (a) 4 kHz                      (b) 8 kHz  
(c) 10 kHz                    (d) 16 kHz

2. The circuit is counter of mod

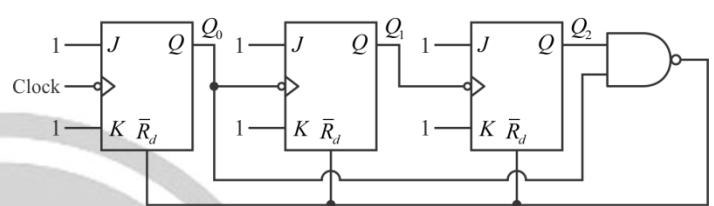


- (a) Mod-0                      (b) Mod-16  
(c) Mod-15                    (d) Mod-14

3. The circuit is a counter of mod

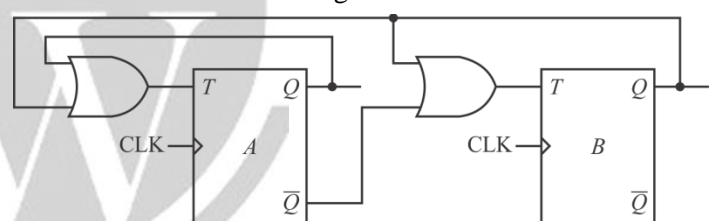


4. The circuit shown consists of J-K flip-flops, each with an active low asynchronous reset ( $\bar{R}_d$  input). The counter corresponding to this circuit is



- (a) a modulo-5 binary up counter.  
(b) a modulo-6 binary down counter.  
(c) a modulo-5 binary down counter.  
(d) a modulo-6 binary up counter.

5. The circuit shown in figure is



- (a) a MOD-2 counter  
(b) a MOD-3 counter  
(c) generate sequence 00, 10, 01, 00.....  
(d) generate sequence 00, 10, 00, 10, 00

## Answer Key

1. (a)
2. (c)
3. (10)
4. (a)

5. (b)



Any issue with DPP, please report by clicking here:- <https://forms.gle/t2SzQVvQcs638c4r5>

For more questions, kindly visit the library section: Link for web: <https://smart.link/sdfez8ejd80if>



PW Mobile APP: <https://smart.link/7wwosivoicgd4>