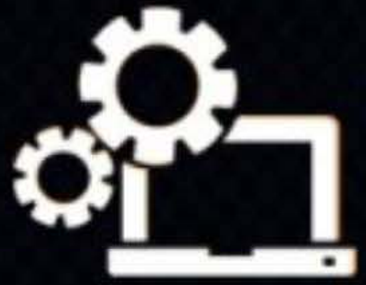
CS & IT ENGINEERING

DIGITAL LOGIC

Combinational Circuit



Lecture No. 3

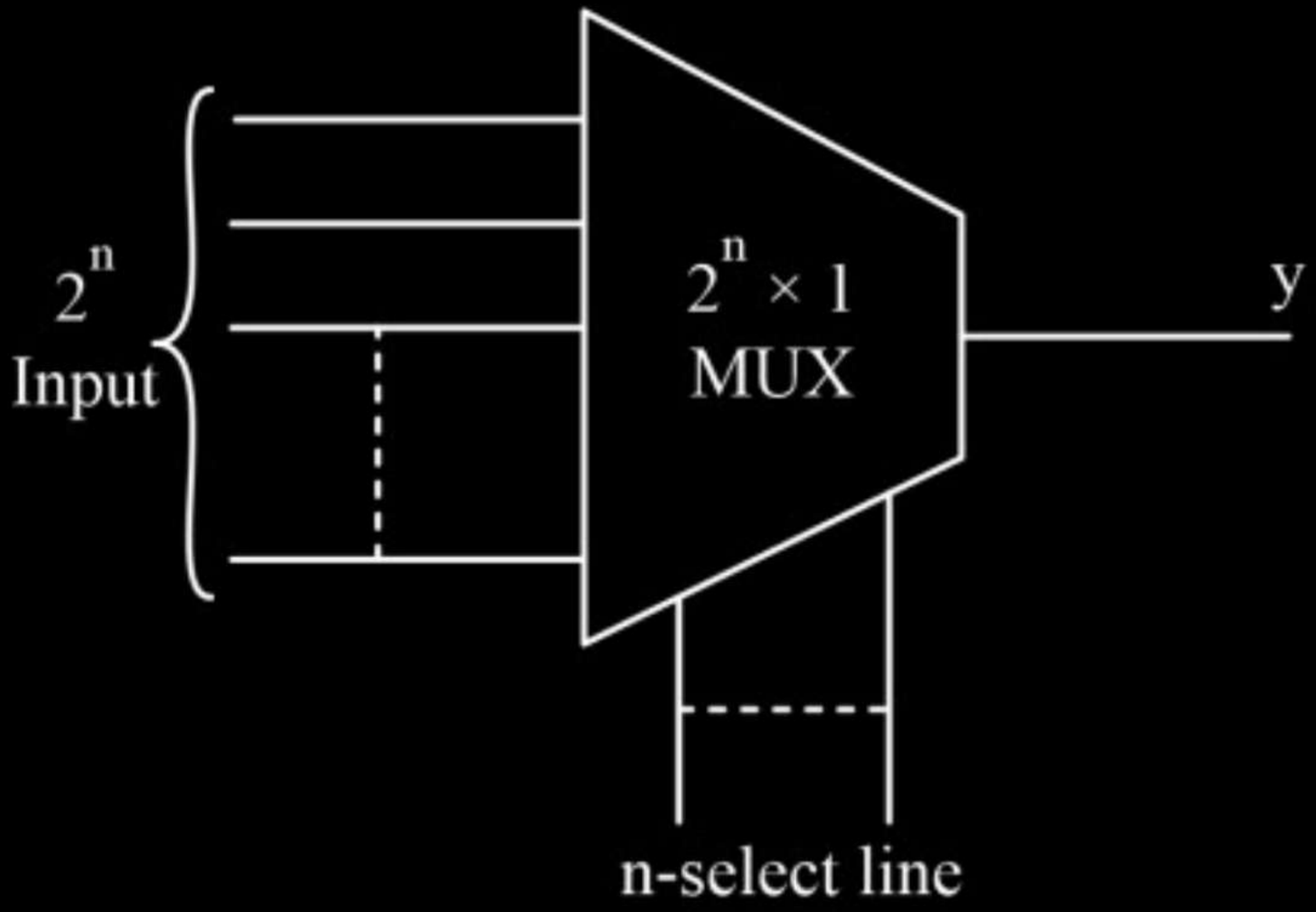
By- CHANDAN SIR

01 MULTIPLEXER

02 QUESTION PRACTICE

03 DISCUSSION

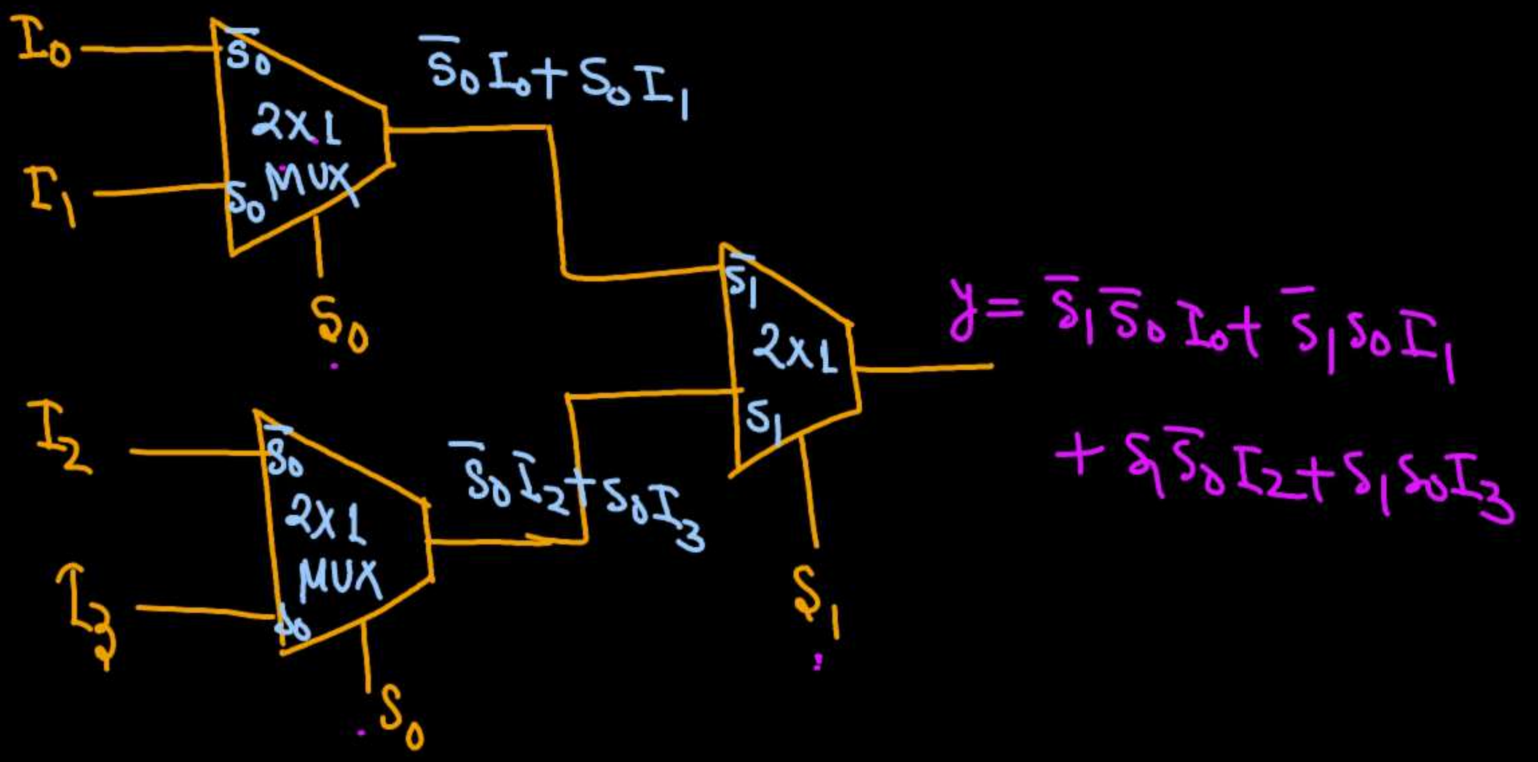
MULTIPLEXER



Type 1. Designing of higher order MUX by using lower order MUX

Ex: 2x1 MUX $\xrightarrow{\frac{4}{2}+\frac{2}{2}}$ 4x1 MUX

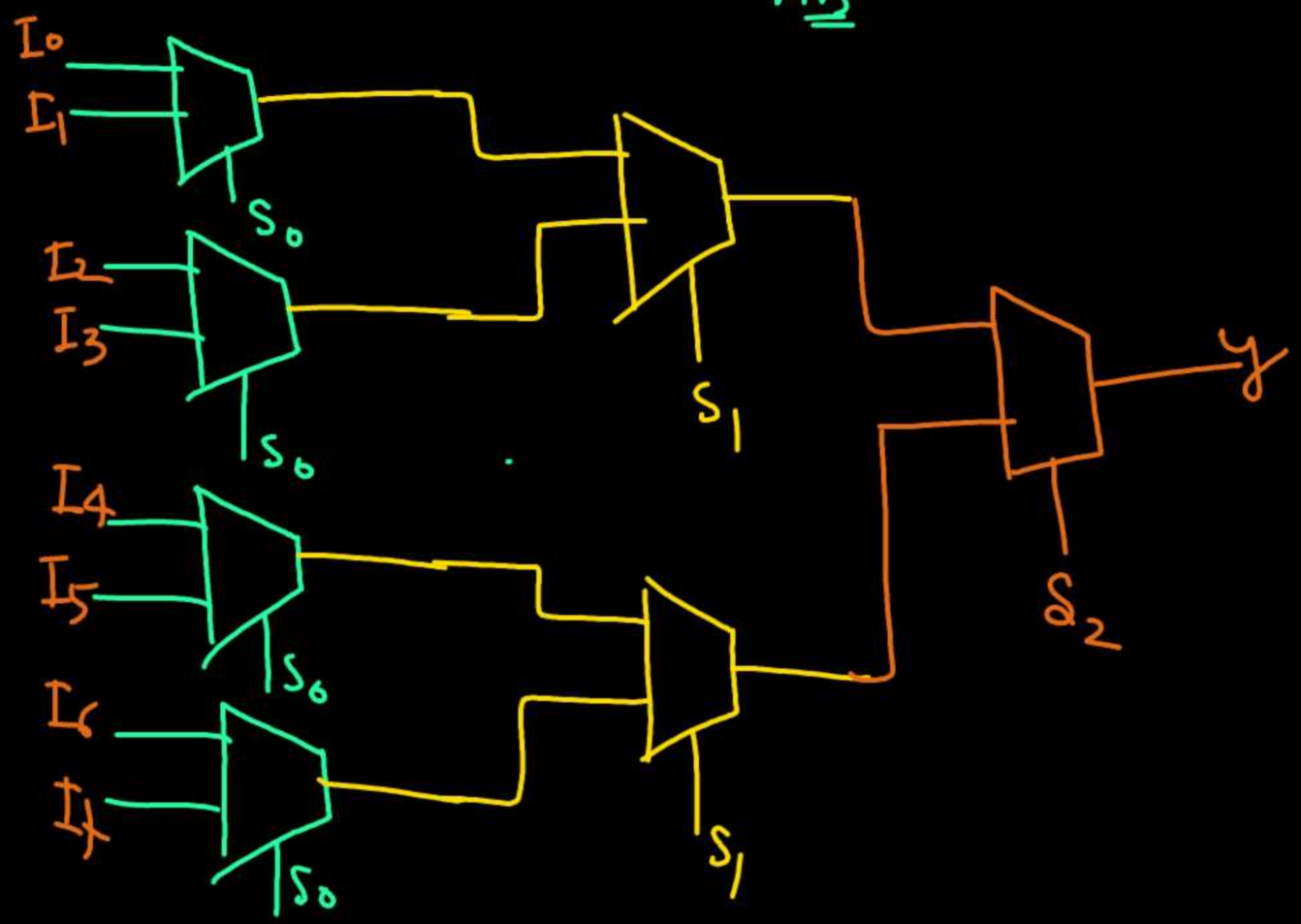
$2+1=3$



2
4
6
8
10
12
14
16
18
26

Ex. 2. 2×1 MUX $\xrightarrow{\frac{8}{2} + \frac{4}{2} + \frac{2}{2}}$ 8×1 MUX

$4 + 2 + 1 = 7$ Ans



③ 2×1 MUX $\xrightarrow{\frac{16}{2}+\frac{8}{2}+\frac{4}{2}+\frac{2}{2}}$ 16×1 MUX

$8+4+2+1=15$

$= A_{ns}$

④ 2×1 MUX $\xrightarrow{63\ A_{ns}}$ 64×1 MUX

⑤ 2×1 $\xrightarrow{2^n-1\ A_{ns}}$ 2^n ×1 MUX

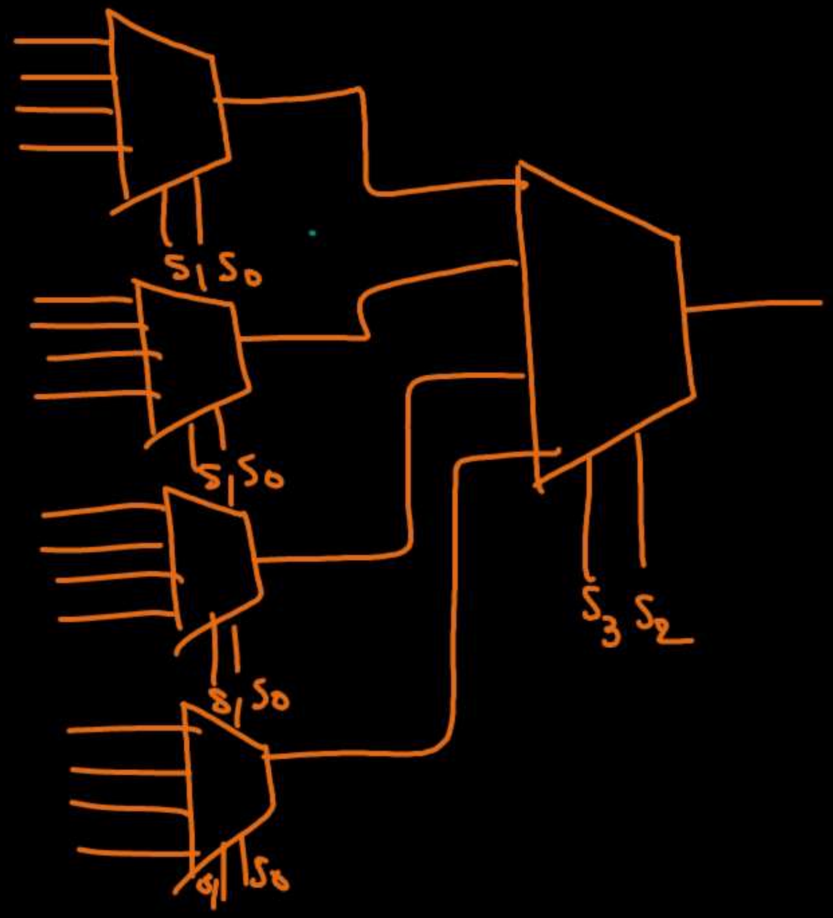
Q. 4x1 MUX → 16x1 MUX

$\frac{16}{4} + \frac{4}{4}$

4 + 1 = 5 Ans

2 select line

Select line = 4



Q = 4x1 MUX $\xrightarrow{\frac{64}{4}+\frac{16}{4}+\frac{4}{4}}$ 64x1 MUX

$16+4+1=21$

Q ≡ 4x1 MUX $\xrightarrow{\frac{8}{4}+\frac{2}{4}}$ 8x1 MUX

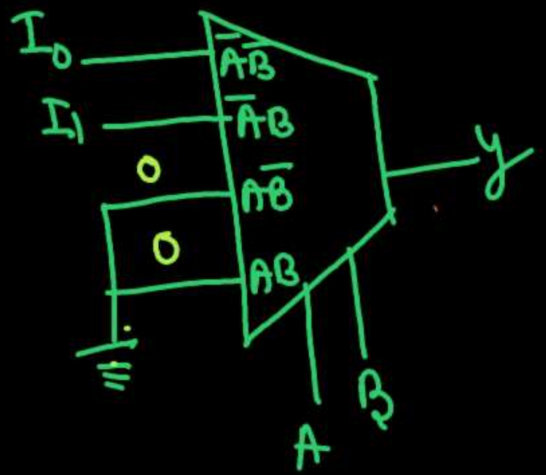
2 select line

2+1=3

A B

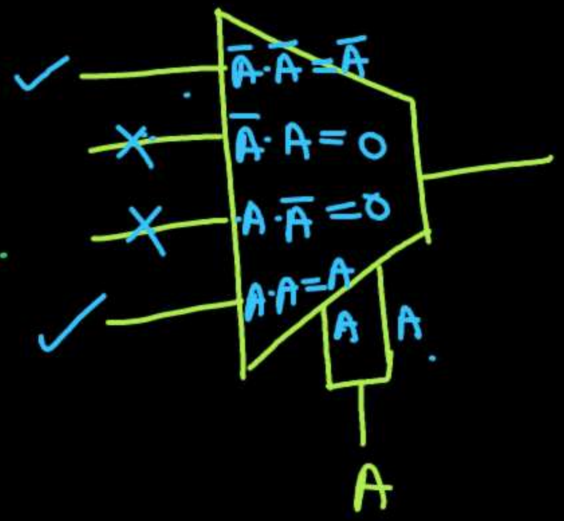
3 select line

Method 1.

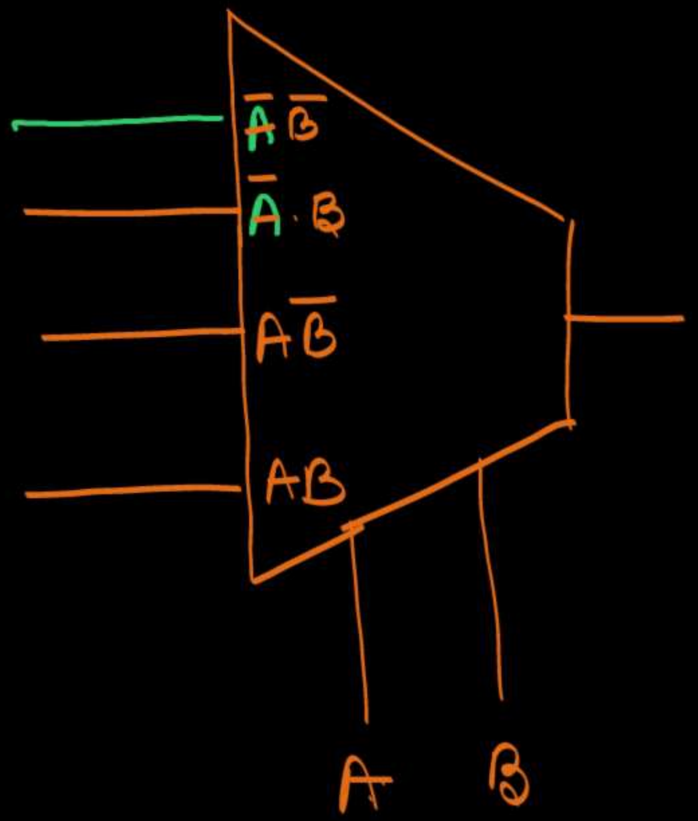


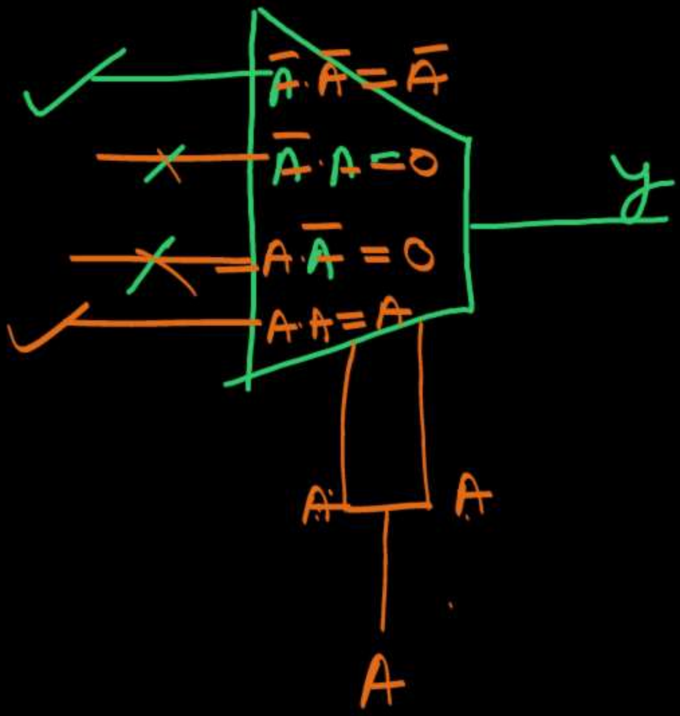
select line=2

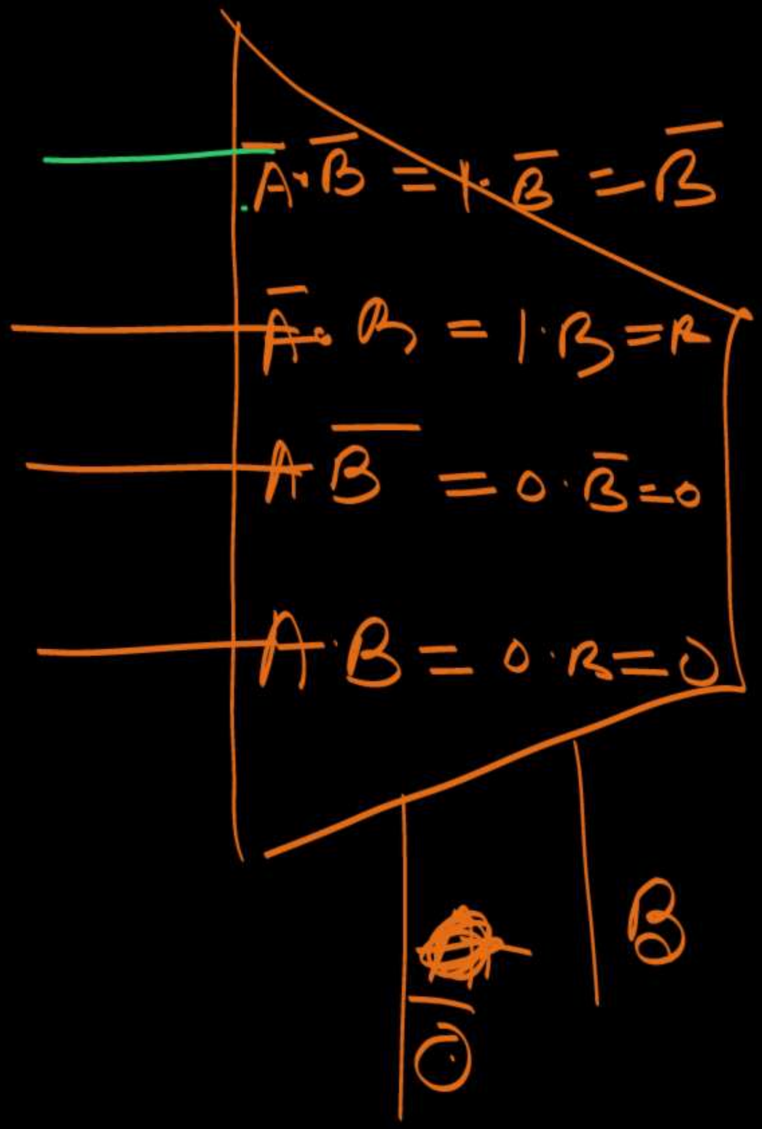
Method 2.



Select Variable=1

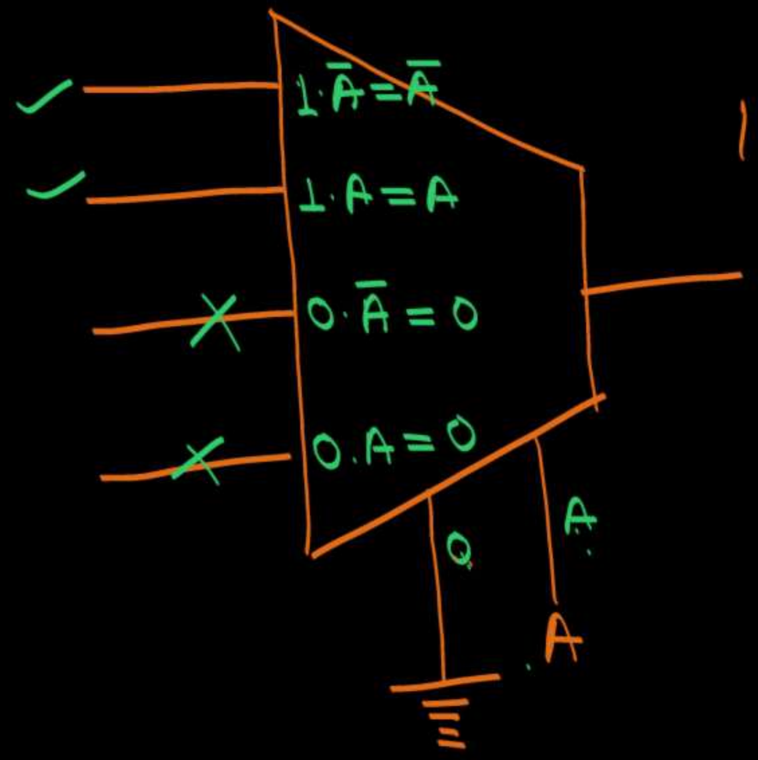

$\bar{A}\bar{B}$
$\bar{A}B$
$A\bar{B}$
AB
A
B


$\bar{A}\cdot\bar{A}=\bar{A}$
$\bar{A}\cdot A=0$
$A\cdot\bar{A}=0$
$A\cdot A=A$
Y
A
A
A


$\bar{A} \cdot \bar{B} = 1 \cdot \bar{B} = \bar{B}$
$\bar{A} \cdot B = 1 \cdot B = B$
$A \bar{B} = 0 \cdot \bar{B} = 0$
$A \cdot B = 0 \cdot B = 0$
B
0

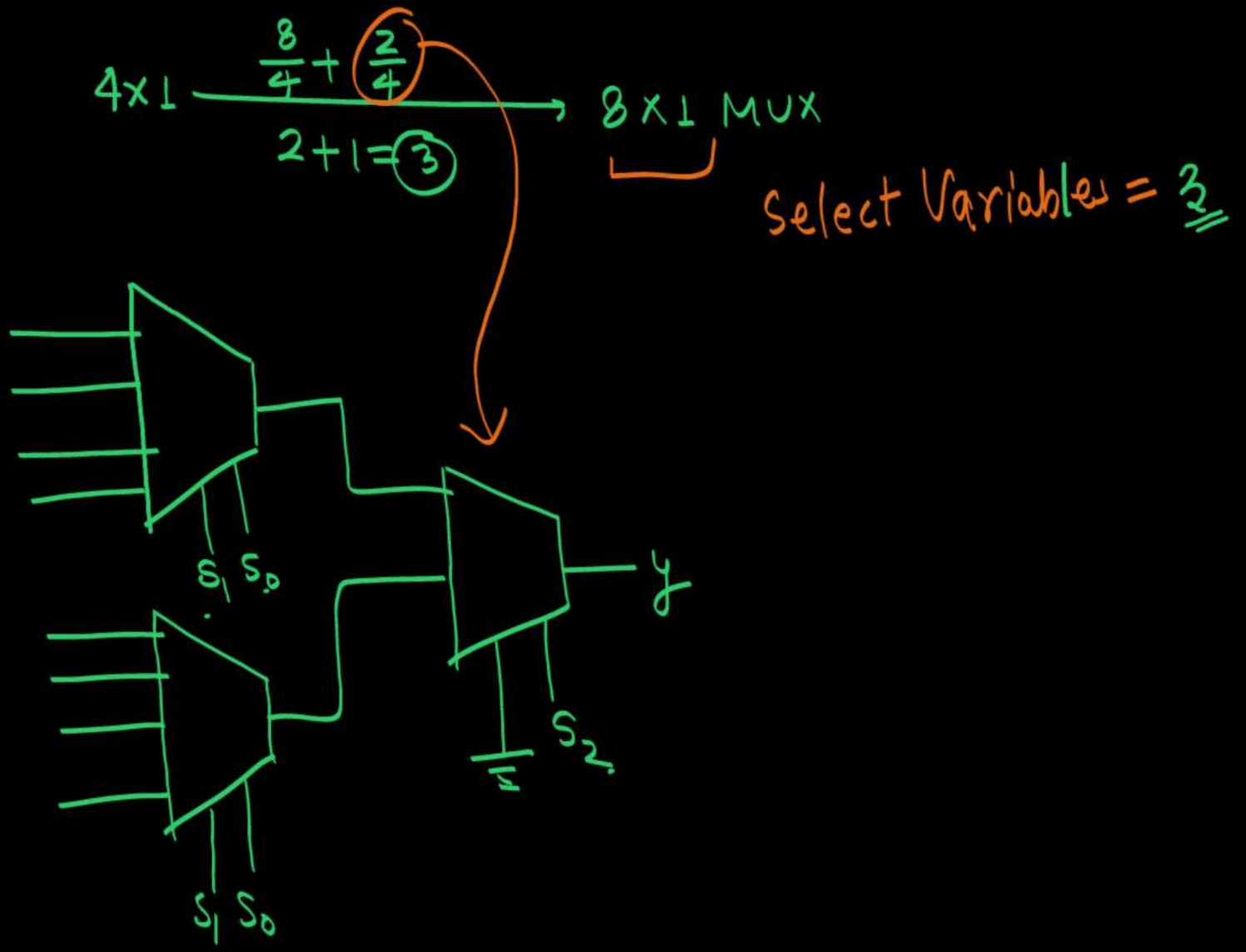
NOTE →

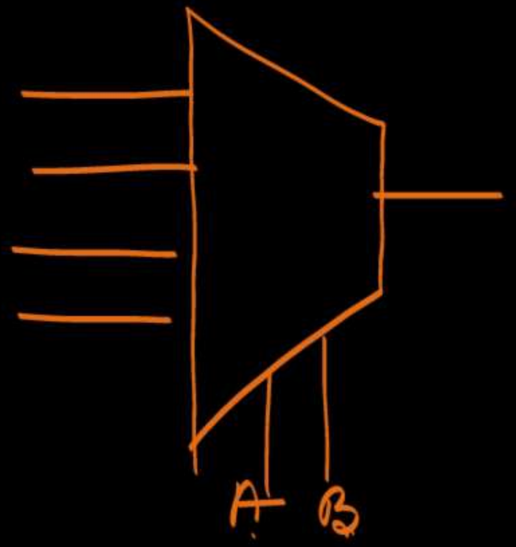
Method (3)



1. Ā =

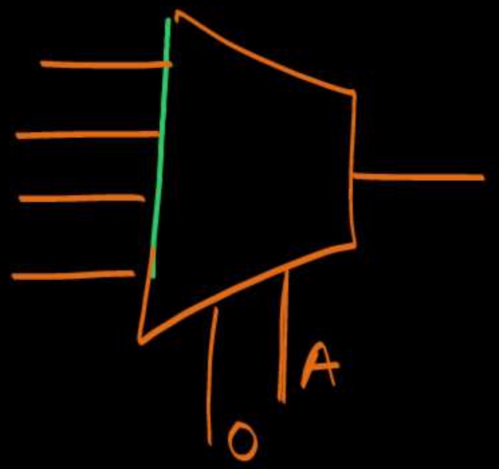
Select Variable = One


8/4 + 2/4
4x1
2+1=3
8x1 MUX
Select Variables = 3
S1 S0
y
S2
S1 S0



Select line = 2

Select Variable = 2



Select line

Select Variable = 1

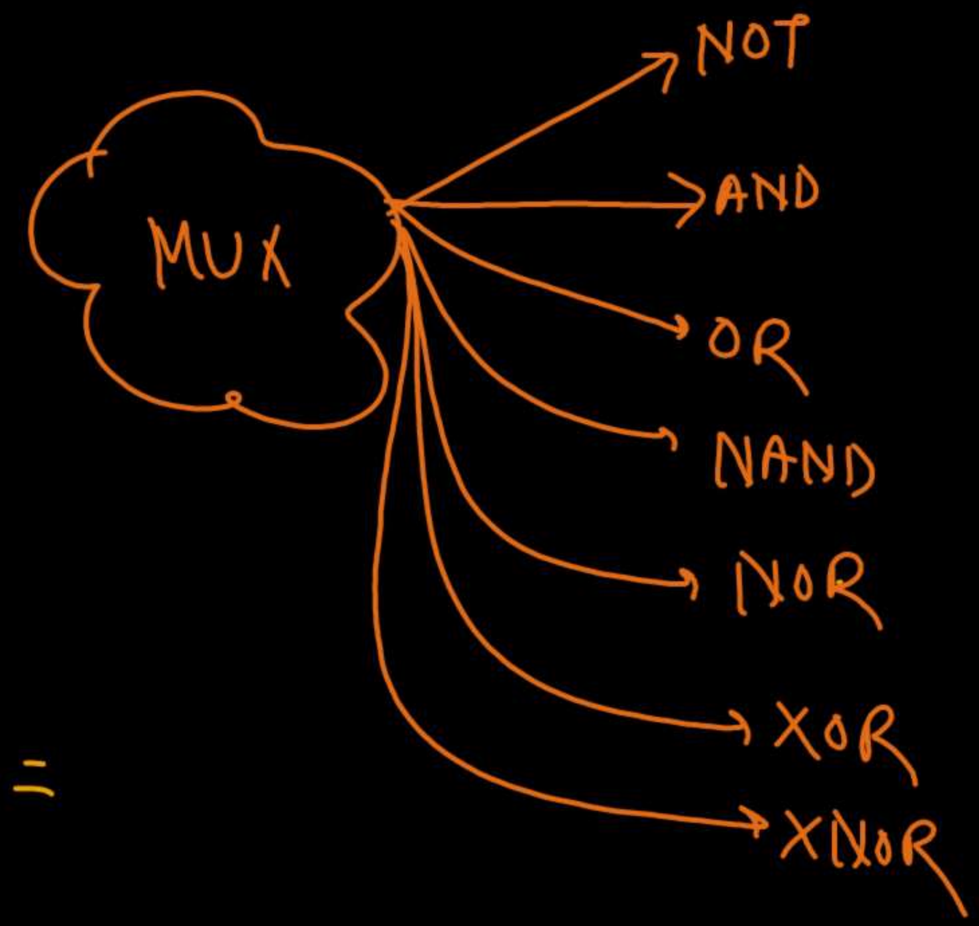
Q. 4x1 MUX $\xrightarrow{\frac{32}{4}+\frac{8}{4}+\frac{2}{4}}$ 32x1 MUX

$8+2+1=11$

Q. 8X1 MUX $\xrightarrow[8+1=9]{\frac{64}{8}+\frac{8}{8}}$ 64X1 MUX

Q. 16X1 MUX $\xrightarrow[16+1=17]{\frac{256}{16}+\frac{16}{16}}$ 256X1 MUX

Type (2) MUX As a universal Logic.



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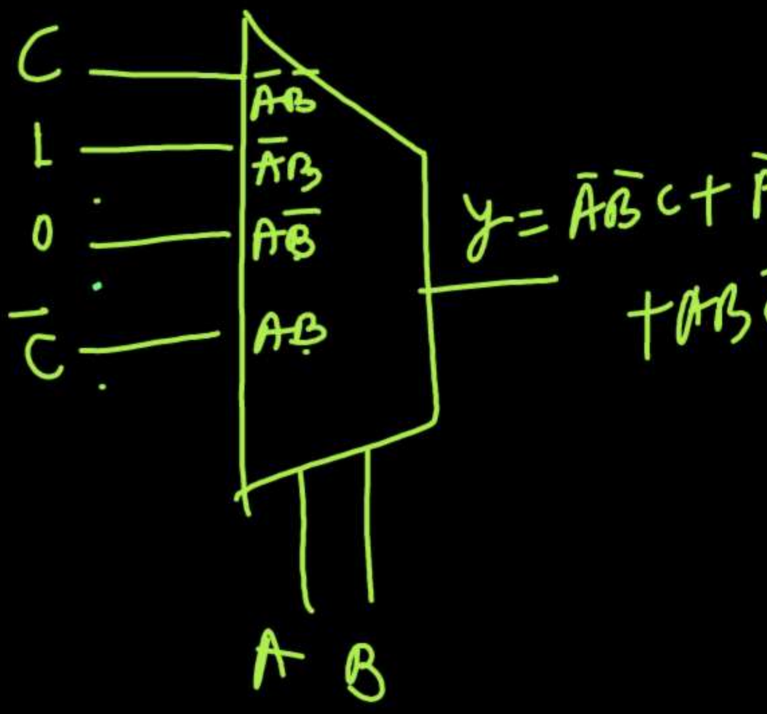
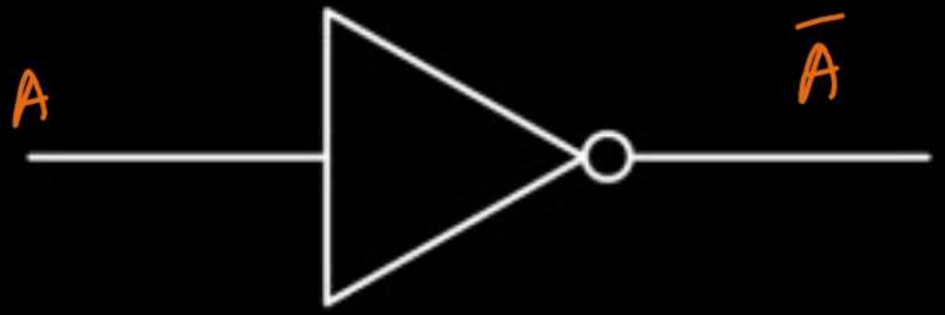
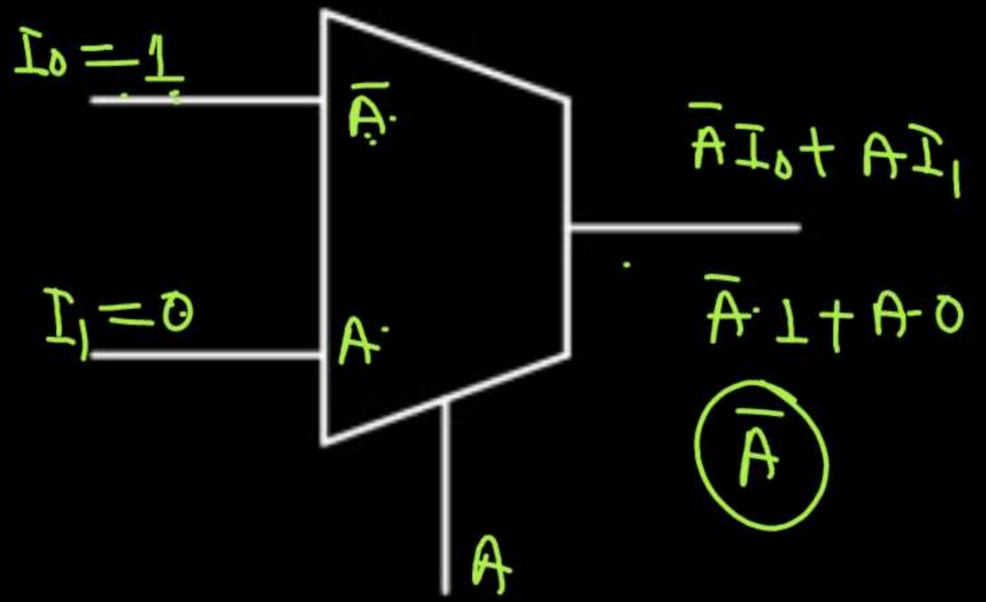


Type-2 MUX as a Universal Logic

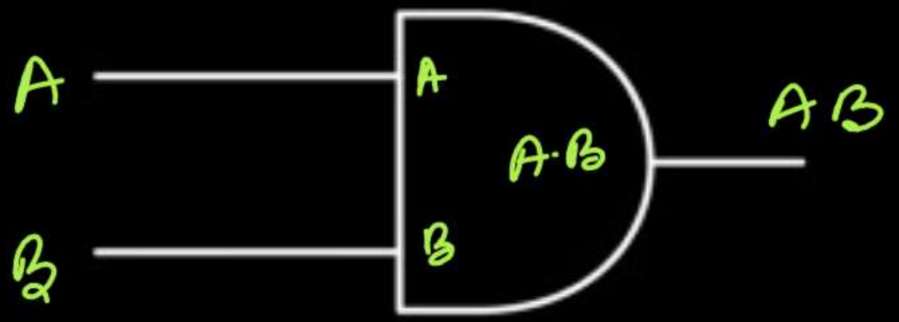
1. Not GATE

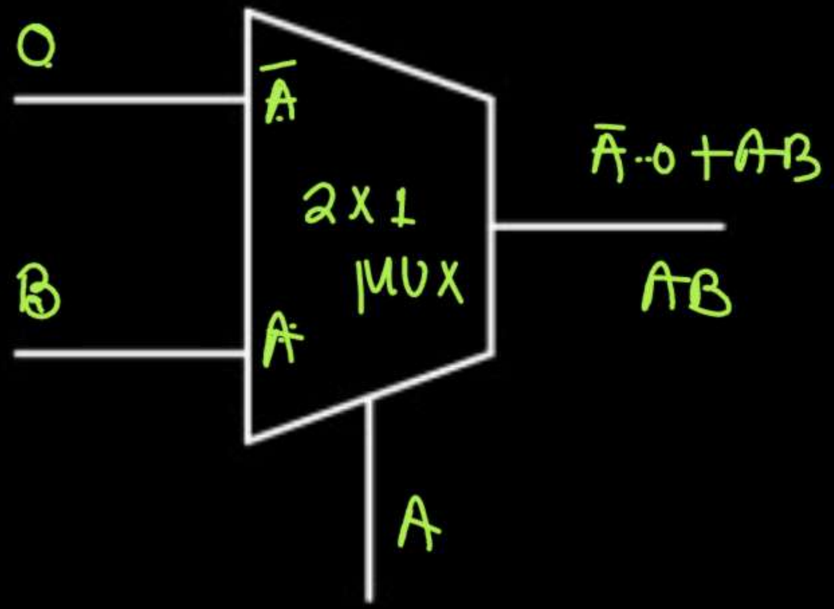




MULTIPLEXER

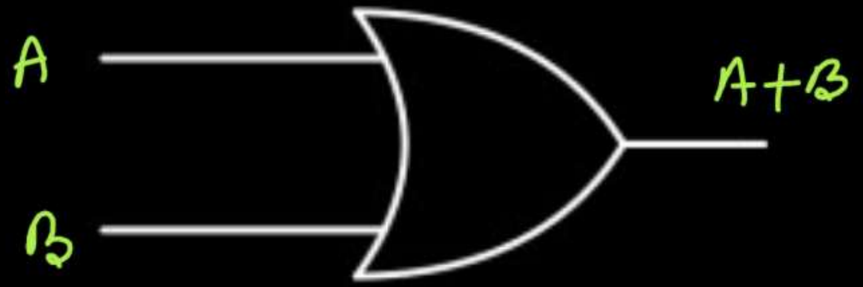
2. AND GATE

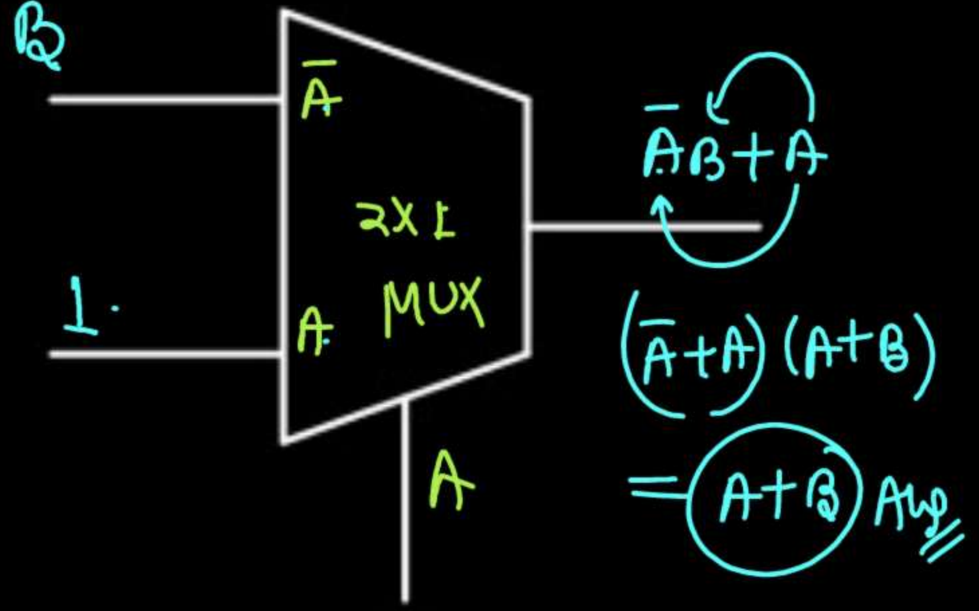




MULTIPLEXER

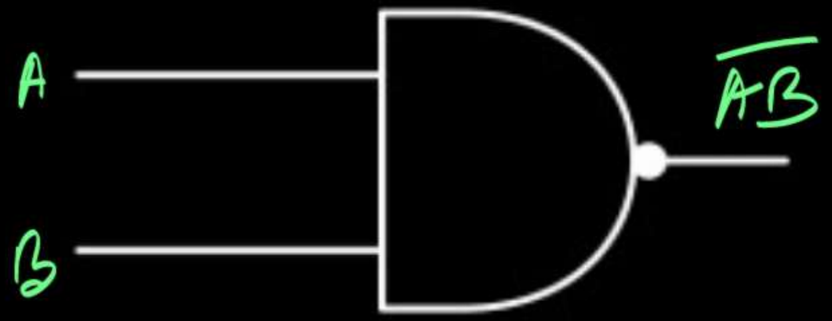
3. OR GATE

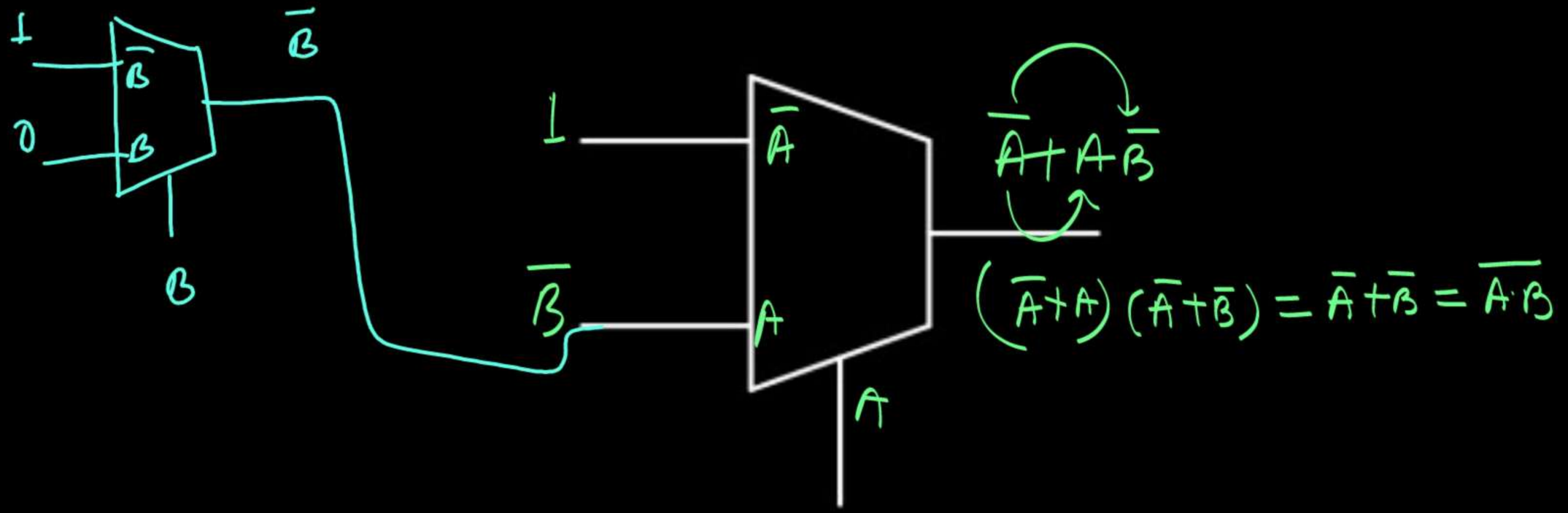




MULTIPLEXER

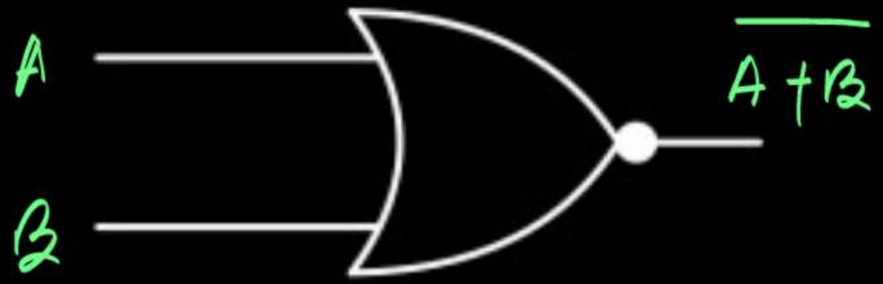
4. NAND GATE

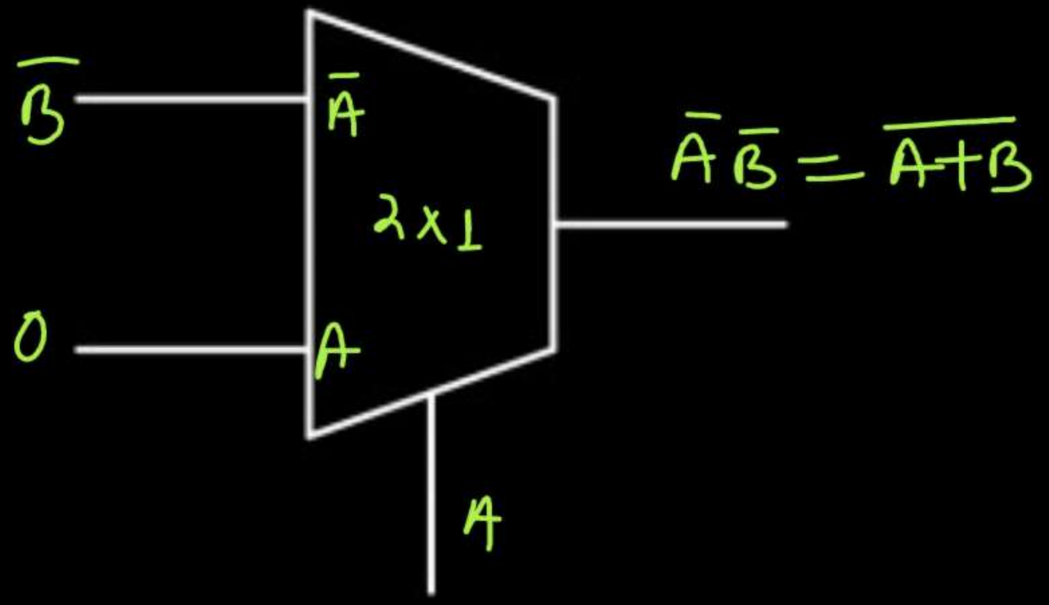




MULTIPLEXER

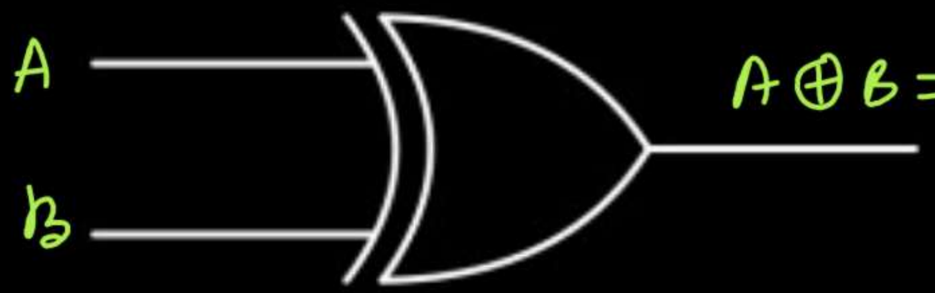
5. NOR GATE



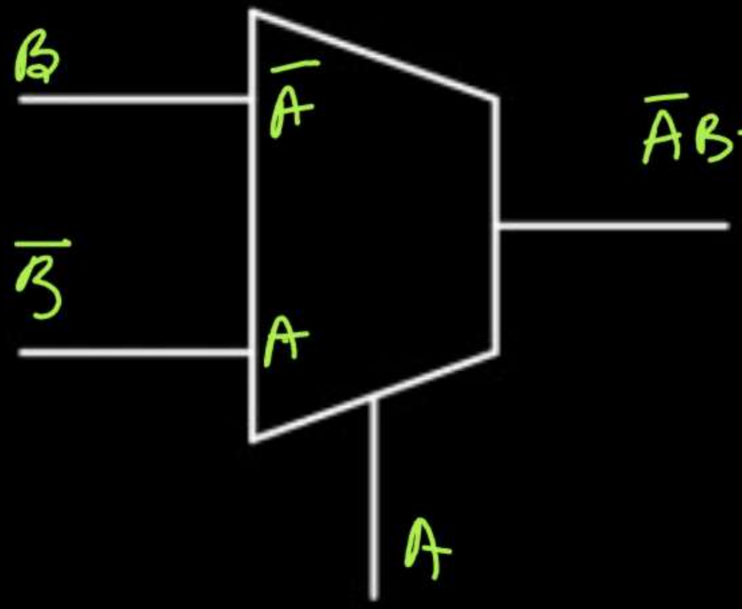


MULTIPLEXER

6. X-OR GATE



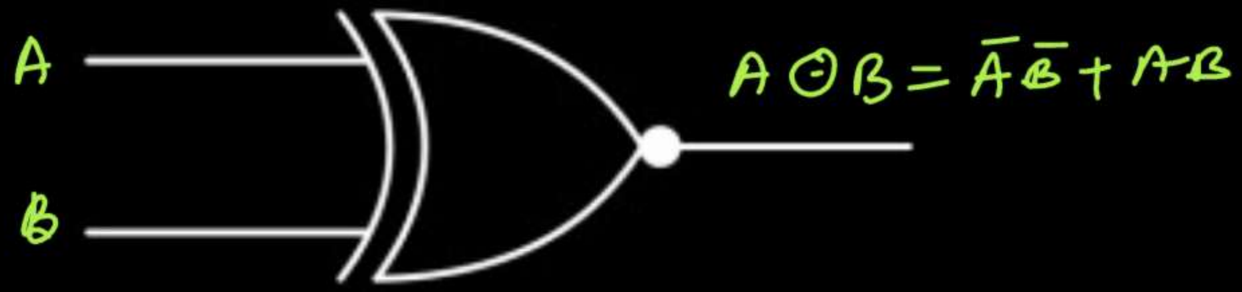
$A \oplus B = \bar{A}B + A\bar{B}$

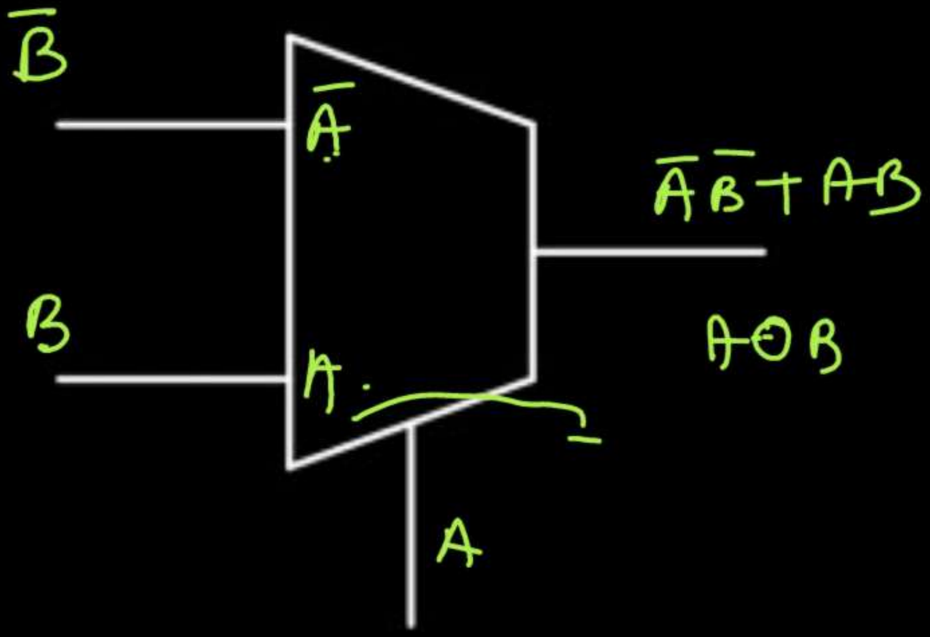


$\bar{A}B + A\bar{B} = A \oplus B$

MULTIPLEXER

7. X-NOR GATE





EZ

NOTE :- To Design NOT, AND, OR

→ One 2X1 MUX required

To Design NAND, NOR, X-OR, X-NOR

→ Two 2X1 MUX required.

Q. Design all Logic GATE by 4X1 MUX?

Thank you

GW

Soldiers !