CS & IT ENGINEERING

DIGITAL LOGIC

Logic Gate

Lecture No. 1

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ISRO

AIR - 23

26

01 Syllabus

02 Weightage

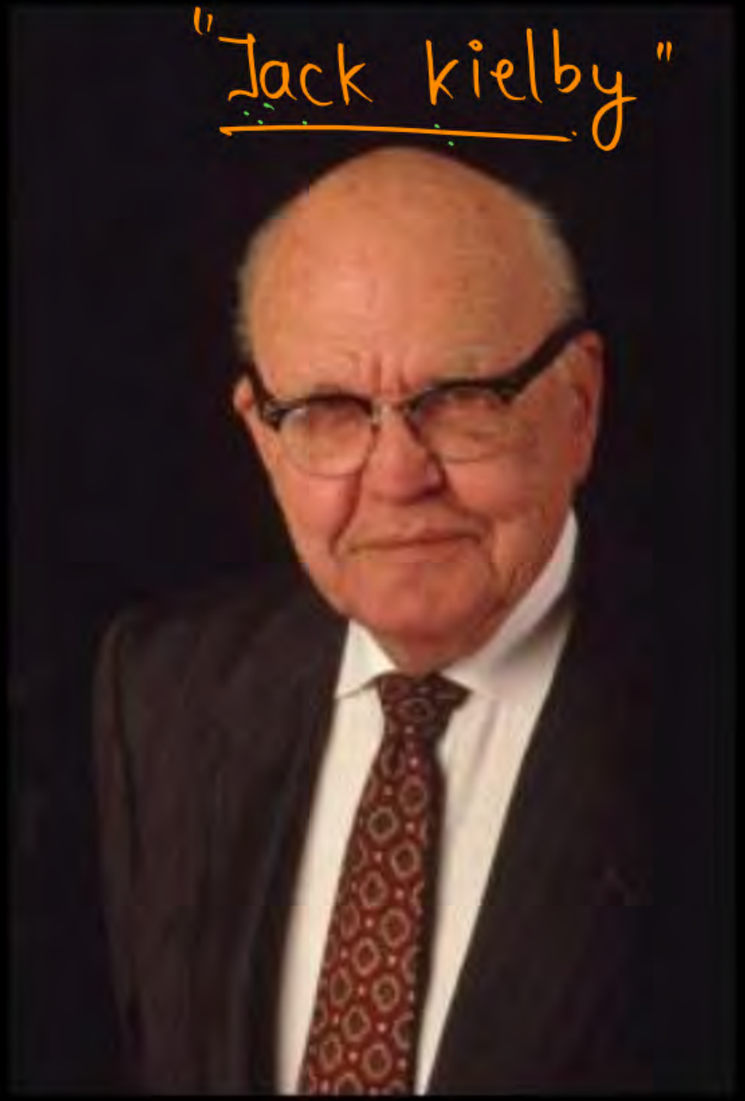
03 Reference Books

04 NOT GATE

Connect me on Telegram-

t.me/CJSIR

"Jack kielby"



Gorden E. Moore.

Flip Flop

JK - FLIP-FLOP → IC → Integrated circuit

↳ Jack keilby

↳ papa of Ic

Gorden E. Moore

1962

1965

दुकान (shop) → INTEL

Statement

Nobel prize

Moore's Law

1 element → 1958

2 element → 1960

4 element → 1962

8 element → 1964

CS & IT ENGINEERING

Digital Logic

Boolean algebra. Combination and sequential circuits. Minimization. Number representations and computer arithmetic (fixed and floating point).

CS & IT ENGINEERING

DIGITAL LOGIC	
Number of Questions	2 to 4
Marks	4 to 6
Frequently Asked Topics	Boolean algebra. Combinational and sequential circuits. Minimization. Number representation.

Reference Books

CJ sir की Notes

Book Name: Digital Design
Author: M. Morris Mano & Michael D. Ciletti
Publisher: Pearson Publisher

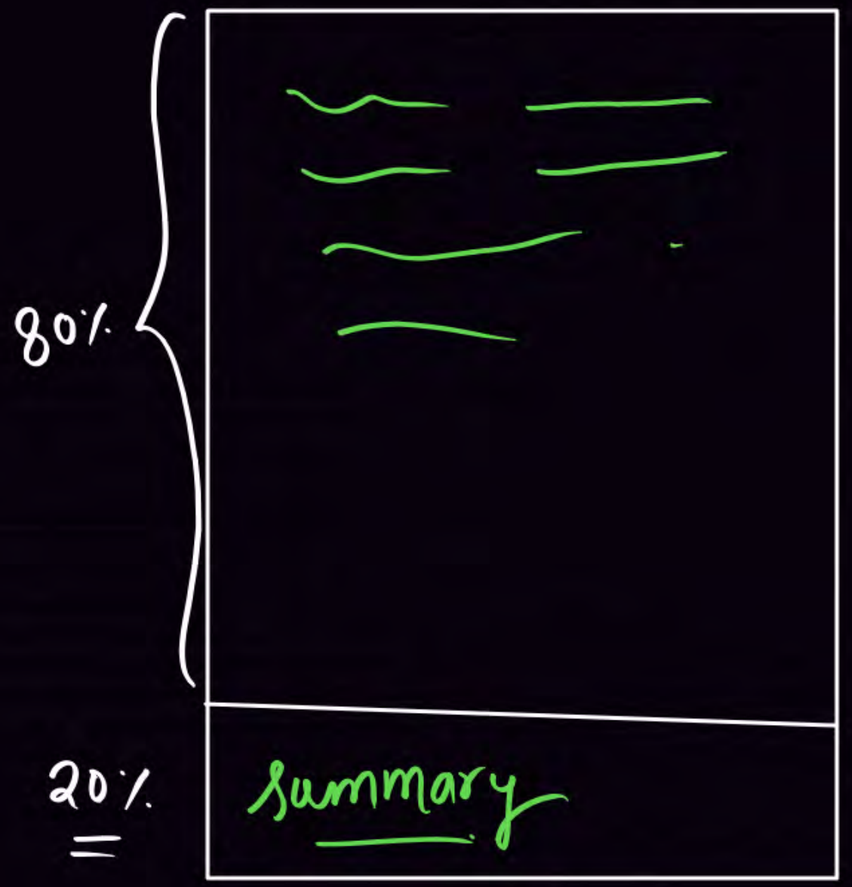
Book Name: Digital fundamental
Author: Thomas L. Floyd
Publisher: Pearson Publisher

Guidelines to Attend Live Class

- Attend the class with positive attitude.
- Punctuality is necessary.
- Follow the day-wise study plan.
- Attempt DPP daily as per the schedule.
- Hold chat while attending the class. We will allow you to ask and put your questions in the comment box.

DPP → 13 question

S.N.	Chapter	Topic
1	Logic Gate	NOT, AND, OR, NAND, NOR, X-OR, X-NOR, Inhibition.
2	Minimization	Boolean algebra K-MAP
3	Combinational Circuit	Comparator, MUX, DE-MUX, Encoder, Decoder Half adder, Full adder, Half subtractor, Full subtractor. Serial adder, parallel adder, LACA, Multiplier. complement subtractor.
4	Sequential Circuit	Latches, Flip-Flops, Registers, counters, state diagram Representation
5	Number System	Base conversion Magnitude Representation



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Chapter-1

→ 20 pages

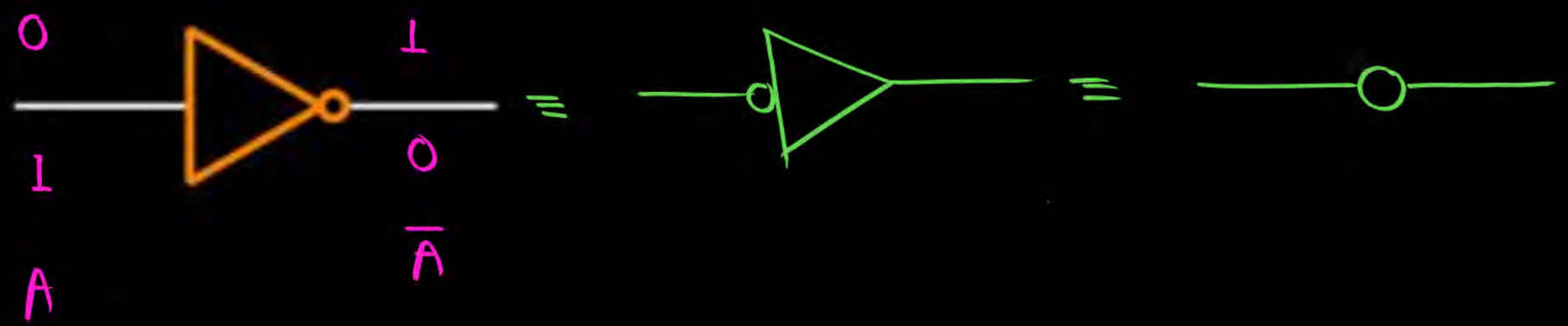
→ 4 pages

INVERTER

NOT GATE, NEGATION, COMPLEMENT LOGIC

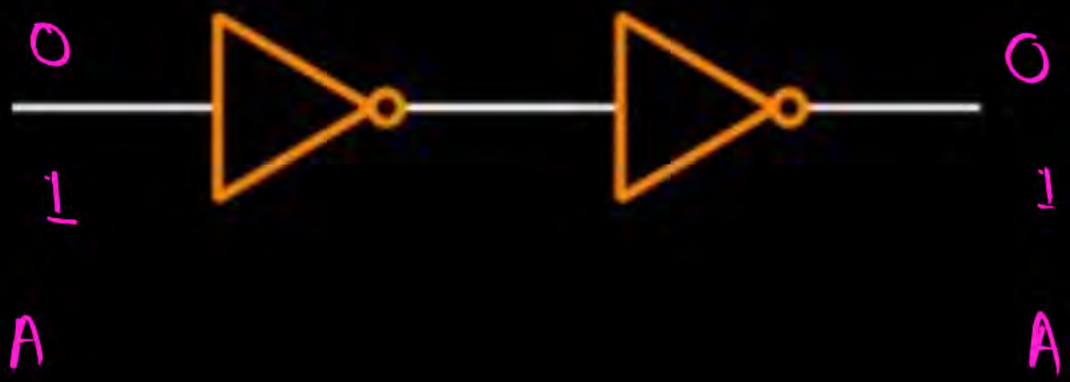
1. NOT GATE

"Propagation delay" ["τ_{Pd}"]



INVERTER

"BUFFER"



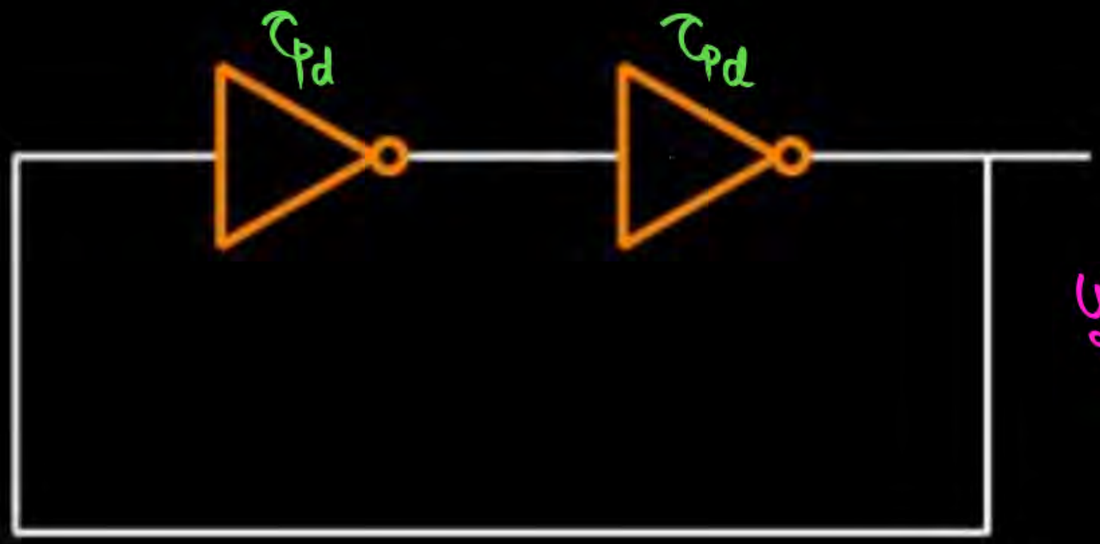
N → Even BUFFER

N → Odd INVERTER

"Multivibrator"

circuit

INVERTER



HIGH

$2\tau_{pd}$ $2\tau_{pd}$ $2\tau_{pd}$ $2\tau_{pd}$

1 → 1 → 1 → 1 → 1 → ...

$2\tau_{pd}$ $2\tau_{pd}$ $2\tau_{pd}$ $2\tau_{pd}$

0 → 0 → 0 → 0 → ...

Low

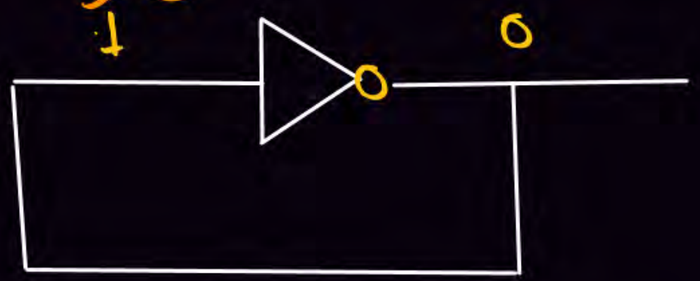
Whenever EVEN no. of NOT GATE in Loop :→

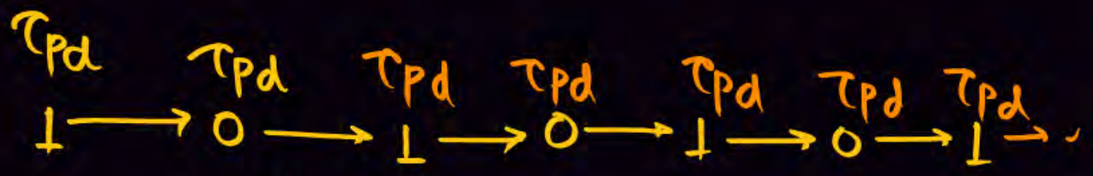
1> Basic Memory element

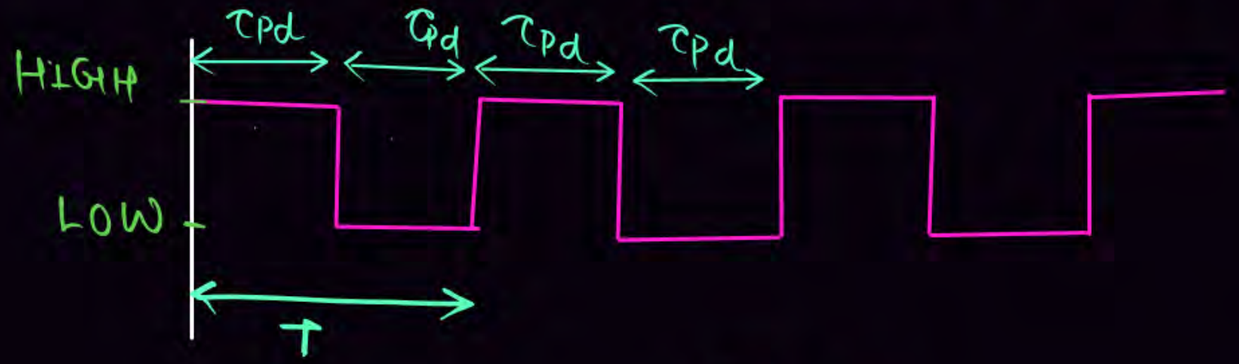
2> Bistable Multivibrator

3> DC generator ($f = 0H_z$)

When ODD no. of NOT GATE in Loop →







1> Astable Multivibrator
2> Square wave generator
3> Clock generator
4> Free Runing circuit.
5> Ring oscillator

$T = 2\tau_{pd}$

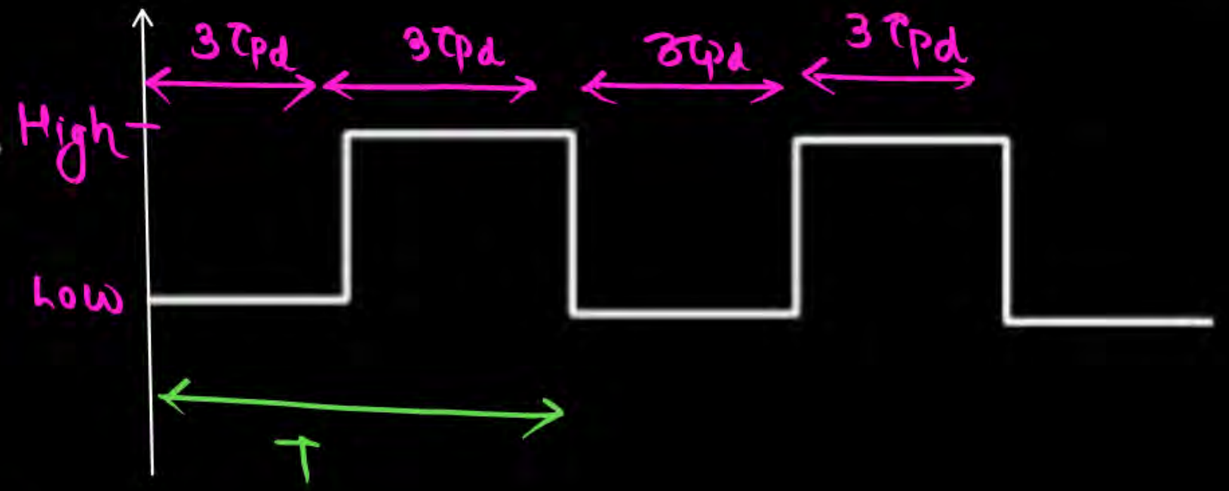
$f = \frac{1}{T}$

$f = \frac{1}{2\tau_{pd}}$

INVERTER

$3\tau_{pd}$ $3\tau_{pd}$ $3\tau_{pd}$ $3\tau_{pd}$ $3\tau_{pd}$

$0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow \ldots$



$T = 2 \times N \times \tau_{pd}$

N → No. of NOT GATE in Loop. (odd)

$T = 6\tau_{pd}$

$T = 2 \times 3 \times \tau_{pd}$

$f = \frac{1}{2N \times \tau_{pd}}$

Q.1

For the circuit given below, all NOT Gates are identical to each other and having propagation delay 10 ps. Find the frequency of generated wave form?

10^{-12}

A. 10 GHz
B. 100 GHz
C. 1 GHz
D. None

$N \rightarrow 5 \quad \tau_{pd} \rightarrow 10 \times 10^{-12}$

$$f = \frac{1}{2N \times \tau_{pd}}$$

$$f = \frac{1}{2 \times 5 \times 10 \times 10^{-12}} \text{ 1/sec}$$

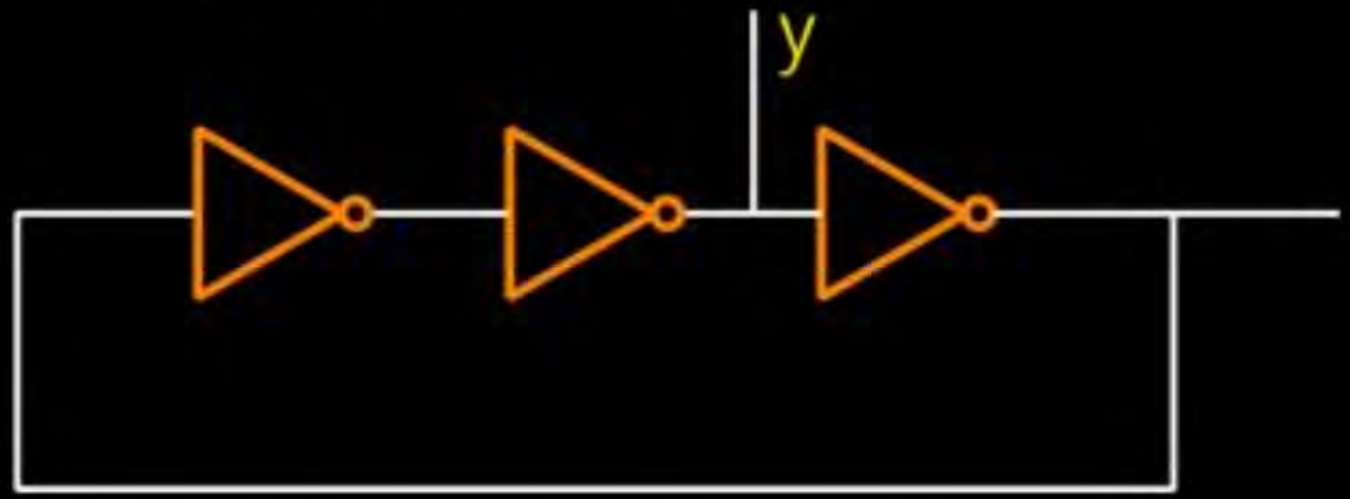
$$f = \frac{10^{12}}{10 \times 10} \text{ Hz}$$

$$f = \frac{10^{9}}{10 \times 10} \times 10^{9} \text{ Hz}$$

$f = 10 \text{ GHz}$

Q.2

Circuit given below are called.



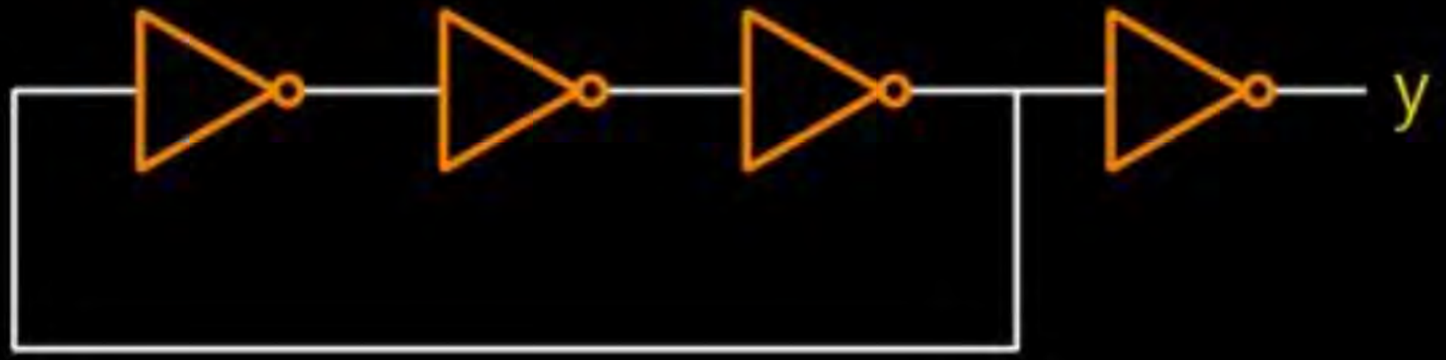
A. Astable Multivibrator

B. Bistable Multivibrator

Q.3

Hw

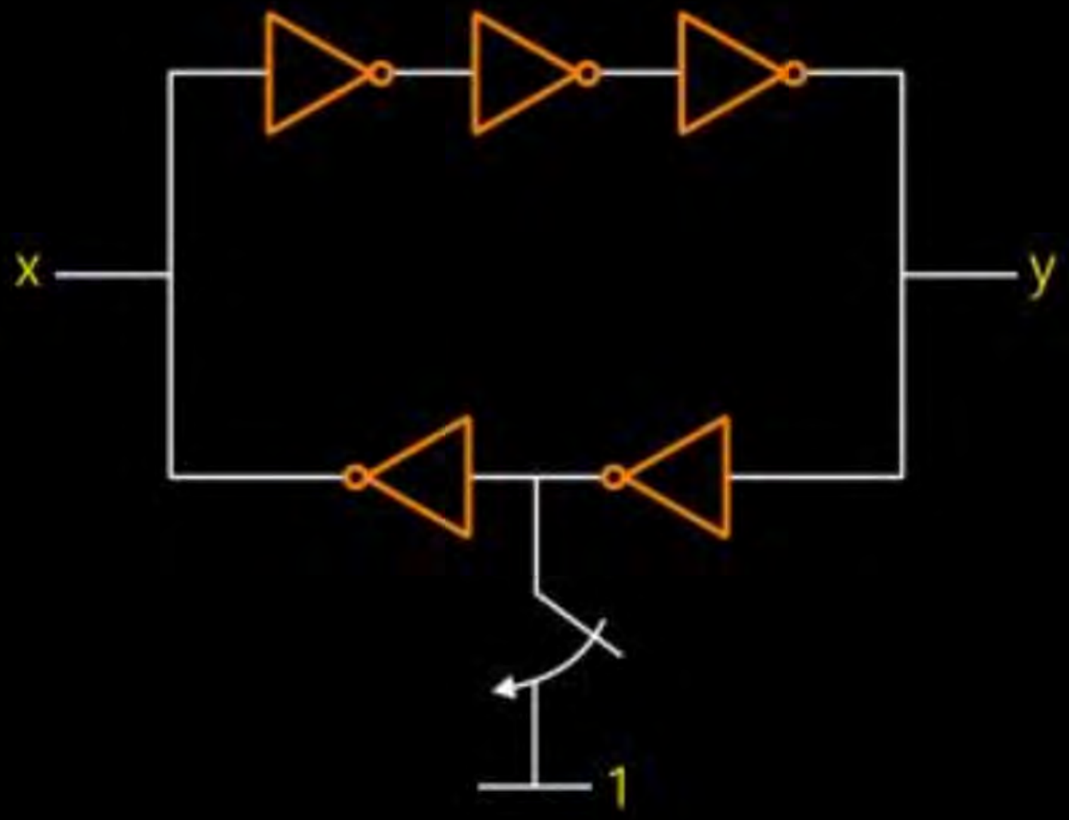
Sketch the waveform of y if all NOT GATES are identical and having propagation delay of 1 microsecond ?



Q.3

HW

For the circuit given below x & y condition will be–



A. x stable y toggle

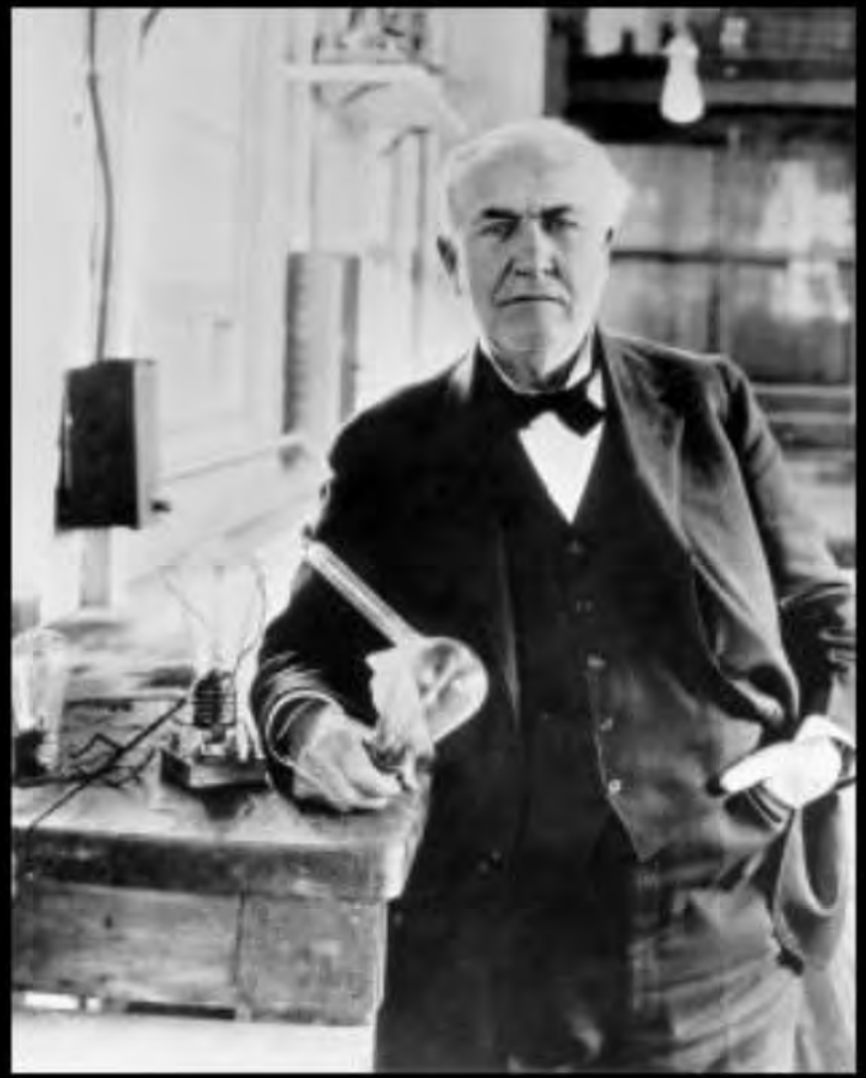
B. x toggle y stable

C. x & y both toggle

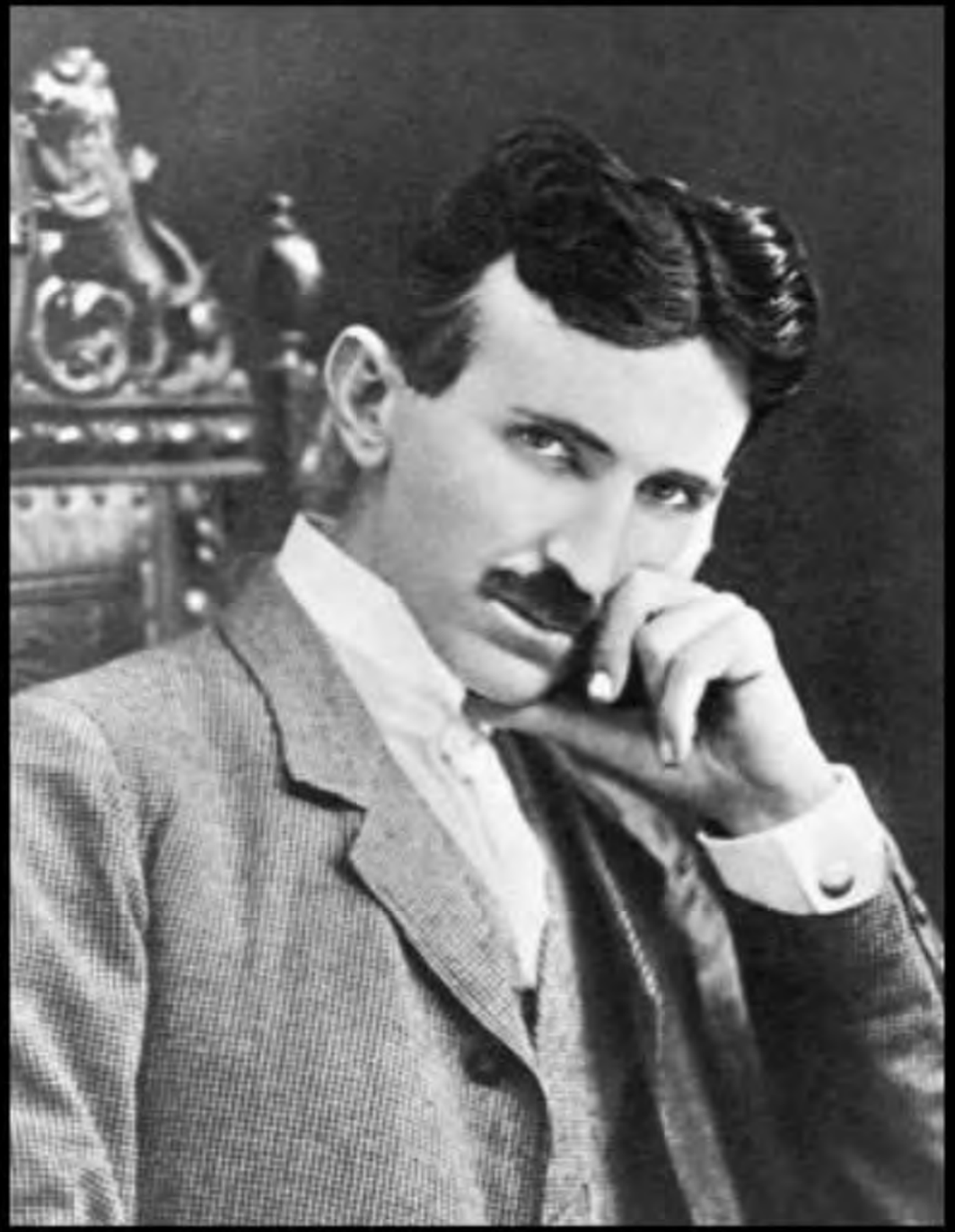
D. x & y both stable

INVERTER

- Revision



AC



Tesla

AC

GATE

Thank you

GW *Soldiers !*