CS & IT



ENGINEERING



Sequential Circuit

Lecture No. 4



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TOPICS TO
BE
COVERED

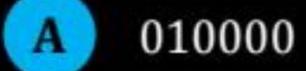
01 SR, JK, D, T Flip Flop

02 PRACTICE

03 DISCUSSION



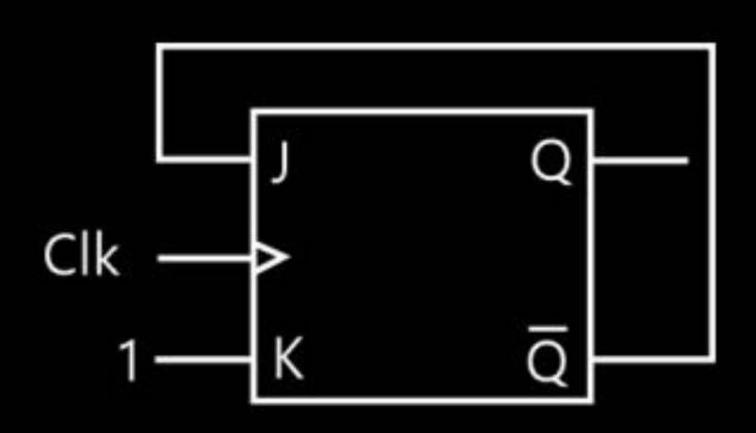
The J-K FF shown below is initially cleared and then clocked for 5 pulses, the sequence at the Q output will be



B 011001

C 010010

D 010101



D FLIP-FLOP



- (i) It is known as Delay FF or Transparent FF.
- (ii) In the D FF what ever the input is applied it will directly come to the output along with the clock.
- Symbol

 Q_n Clk

Figure 1: D Flip Flop

D	Q_{n+1}
0	0
1	1

Truth Table

Table 1: Truth Table of D Flip Flop

D FLIP-FLOP

3. Characteristics Table

D	Q _n	Q _{n+1}
0	0	0
0	1	0
1	0	7
1	1	1

4. Characteristics Equation

Table 2: Characteristic Table of D Flip Flop



D FLIP-FLOP

Excitation table

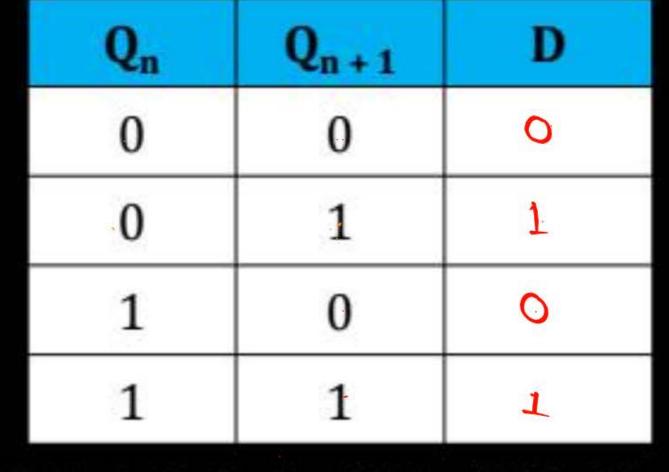
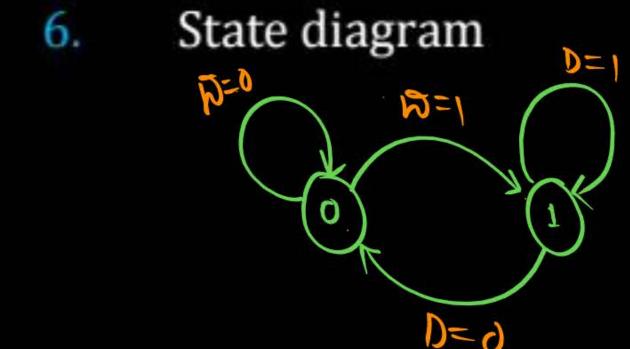
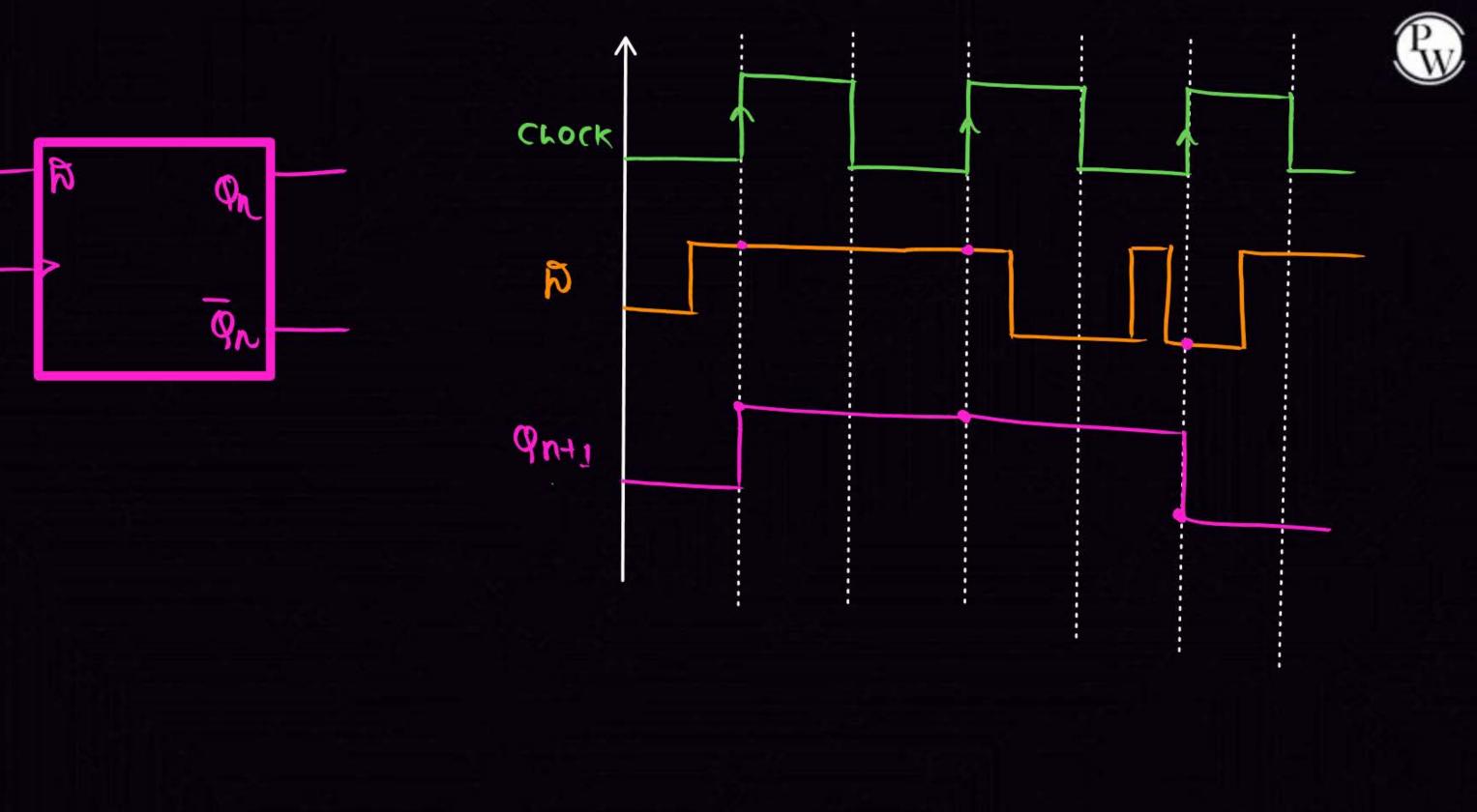
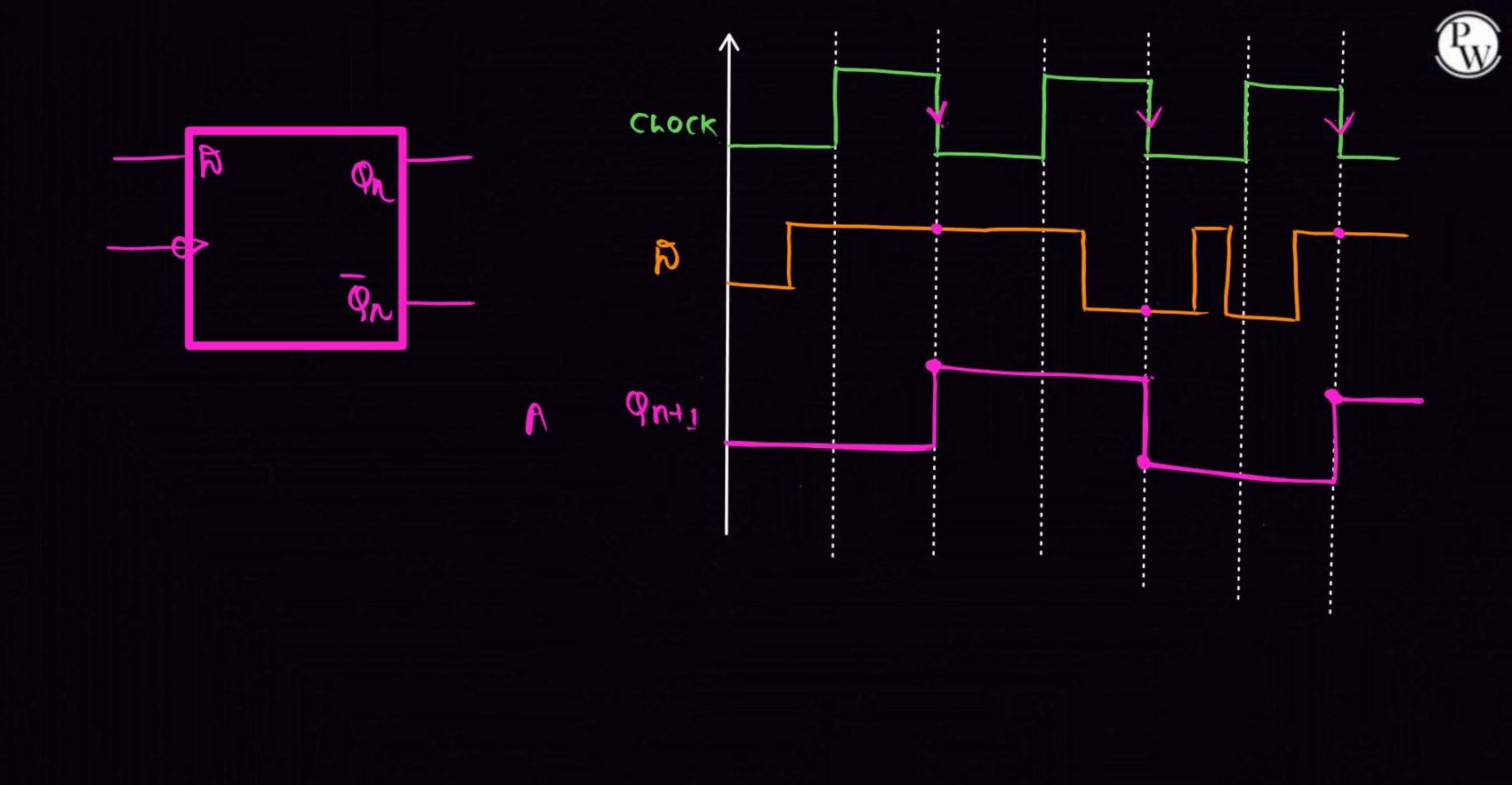


Table 3: Excitation Table of D Flip Flop









T FLIP FLOP (TOGGLE FLIP-FLOP)



Symbol

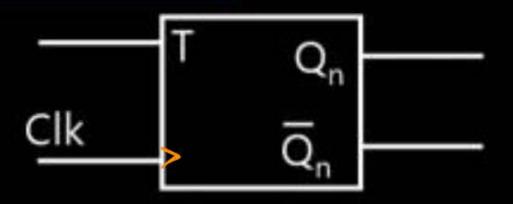


Figure 2: T Flip Flop

Truth Table

T	Q _{n+1}
0	Q~
1	Qn

Table 4: Truth Table of T Flip Flop

T FLIP FLOP (TOGGLE FLIP-FLOP)



3. Characteristics Table

T	Q _n	Q _{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Table 5 : Characteristic Table of T Flip Flop

4. Characteristics Equation

T FLIP FLOP (TOGGLE FLIP-FLOP)



Excitation table

Qn	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

State diagram

Table 6: Excitation Table of T Flip Flop

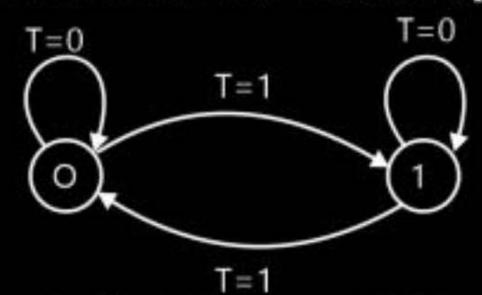


Figure 3: State diagram of T Flip Flop

MASTER-SLAVE FF



Note: J-K FF is also known as universal FF.

	J	K	Q _{n+1}	
SR f/f	(0	0	Q _n	
	{ 0	1	OT BIFF.	FF
	1	0	1	
	1	1	Qn K	



SR FF

9n+1= StRan

હ	R	antı
0	0	9n
S	1	0
1	0	4
Ł	1	×

JK FF

anti=Jan+Kan

t	K	Q _{n+1}
0	0	QV
0	J	0
1	0	J
1	1	91

A.FF

 $Q_{n+1} = \aleph$

anti=todu

T-FF

R	Qnt1
0	0
+	1

7	anti
0	On
7	92

Excitation Table.



Qn	Qn+L	Ş	R	t	K	R	+
0	0	0	×	0	×	0	0
0	1	1	0	J	×	1	J
Į	0	0	1	×	ţ	0	J
1	1	X	0	×	0	J	0

Resigning of Flip-Flop



Cocharaeteristic Besixe

Step 1: - Write the characteristic Table of desired FF.

Step 2: - Write the excitation table of avaliable FF.

Step3: - Write the Logical expression.

step 4: > Minimize the Logical expression.

Steps: -> Hardware Implementation.

Q Besign JK FF by using SR FF?

Aestreat

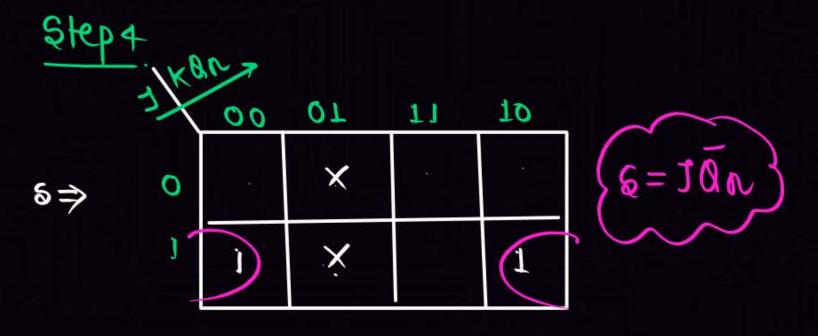
Available

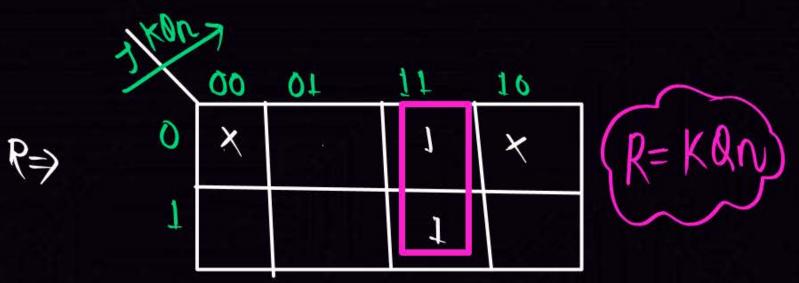
Step 1 Step 2

J	K		Qn+1	S	R
0	0	0	0		X
	0	L	1.	×	0
0	1	0	0	0	X
Ò	Action to the second second second second	1	0		1
Į		Anna market and a second	1	1	0
1	Ò	:1	1	×	0
1	1	0	J	1	0
1	1	.	0	0	L

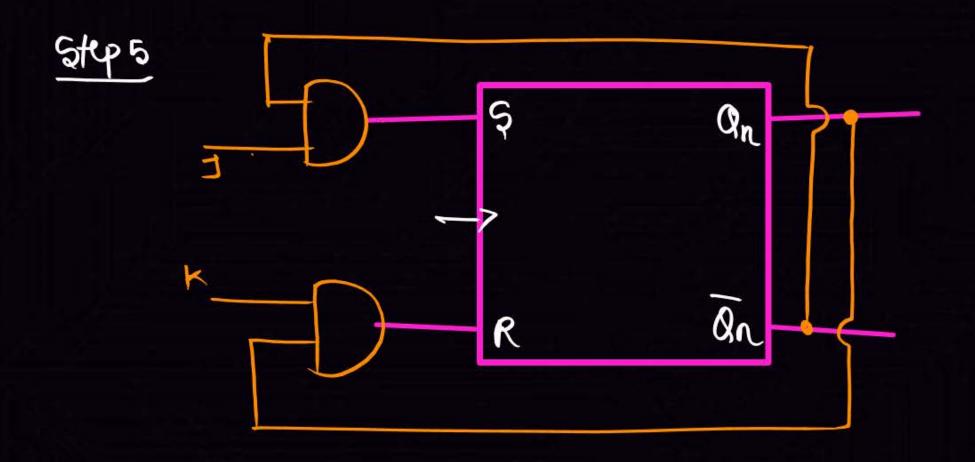


$$\frac{5 + p_3}{R(J_1 k_1 Q_0)} = \sum_{m} (4_1 c) + \sum_{m} (1_1 c) +$$



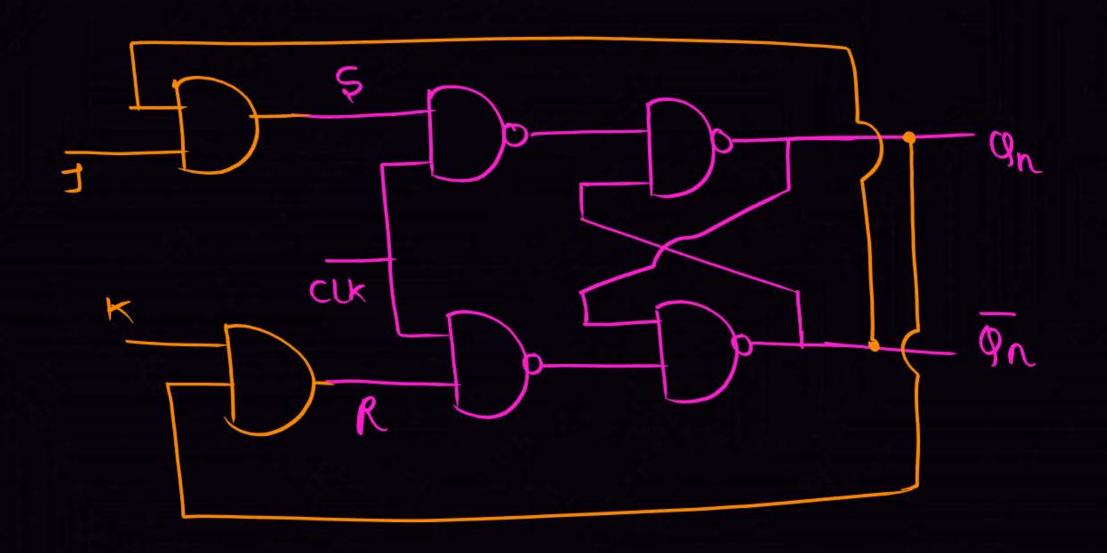










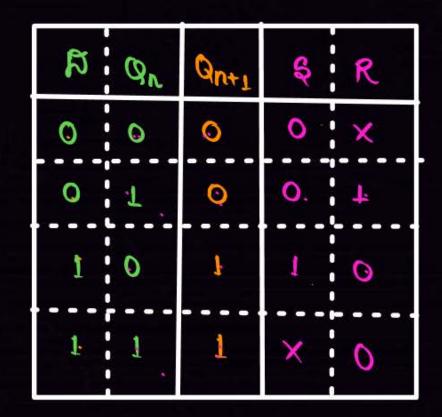


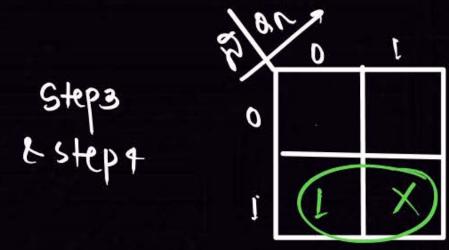


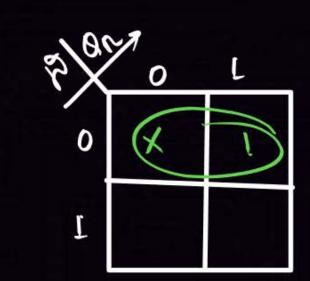
Pw

Step 1:

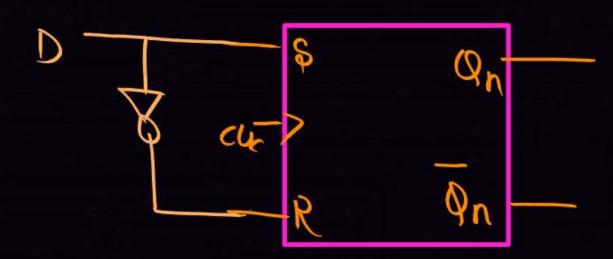
Stepa



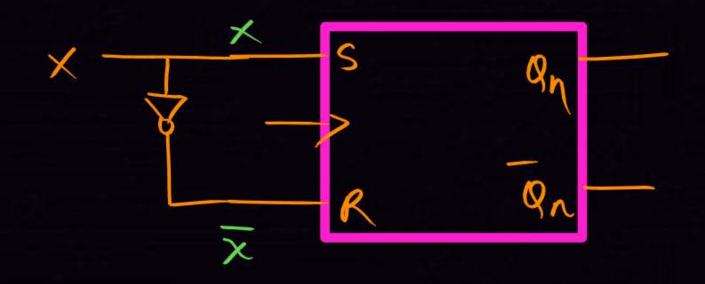




steps:







$$S = X \qquad R = \overline{X}$$

$$Q_{n+1} = S + \overline{R}Q_n$$

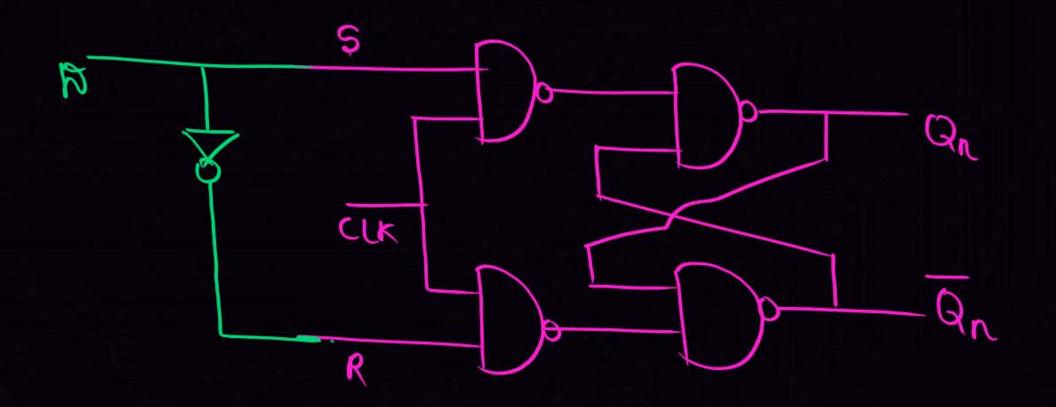
$$= X + \overline{X}Q_n$$

$$= X + XQ_n = X(1+Q_n)$$

$$Q_{n+1} = X$$







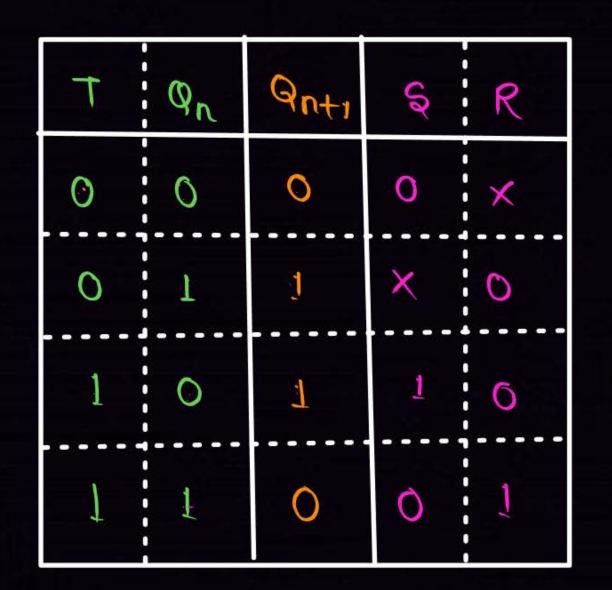
Q Resign a T-FF by Using &R FF?

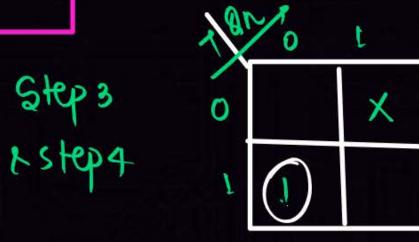


1 an

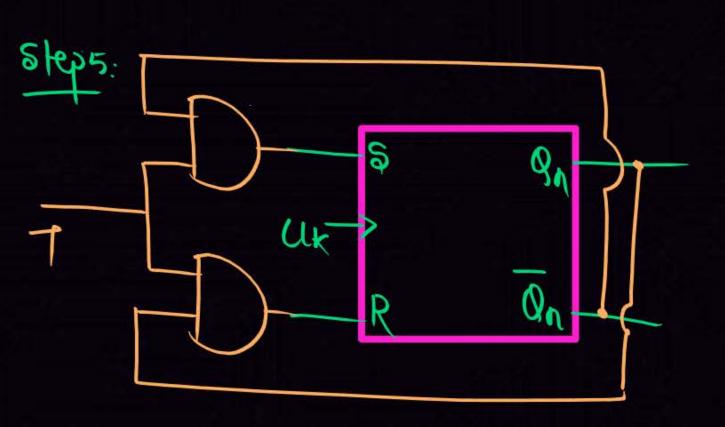
0

Step 1 1 Step 2.

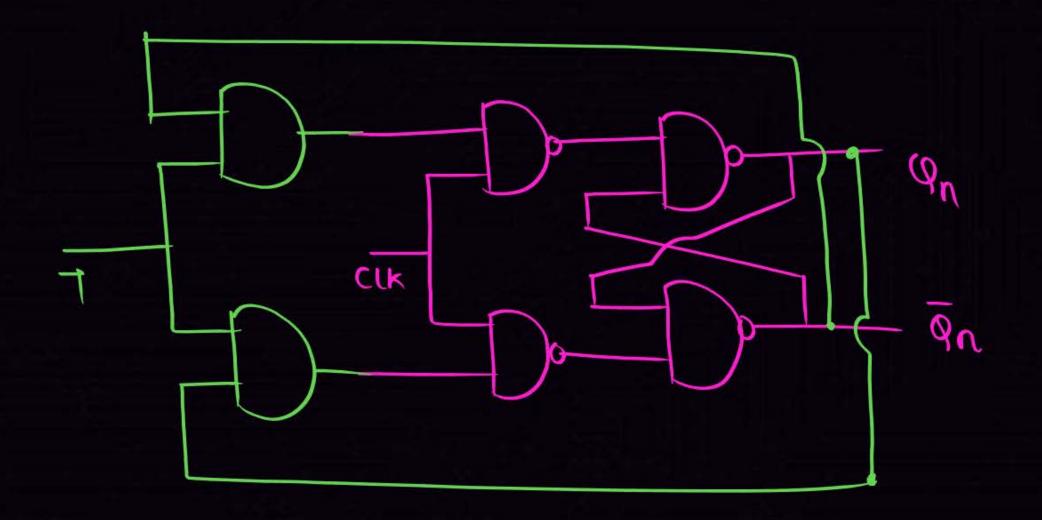












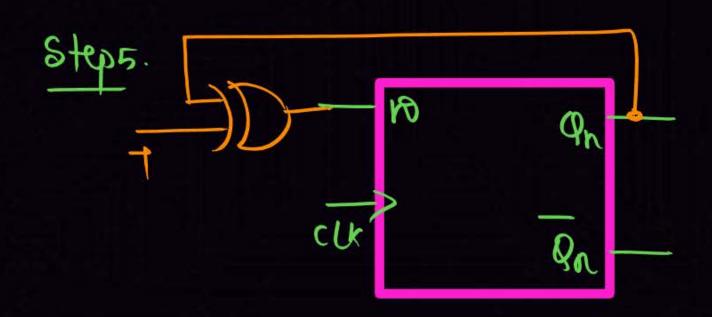
a Resign a T-FF by using 12-FF?



CIA.			
शर	P	1	•-
			-

Step2.

Т		Qnti	B
0		0	0
0	1	L	1
į	0	3	1
	Ţ	0	0



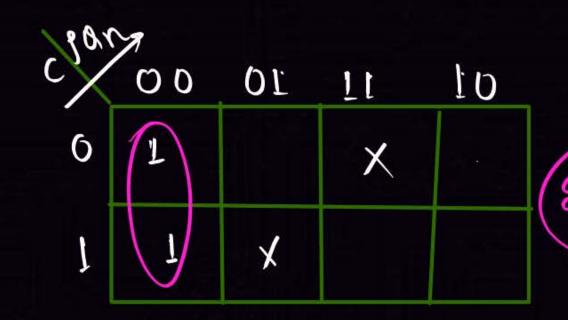
Q Besign a CJFF by Using SRFF?

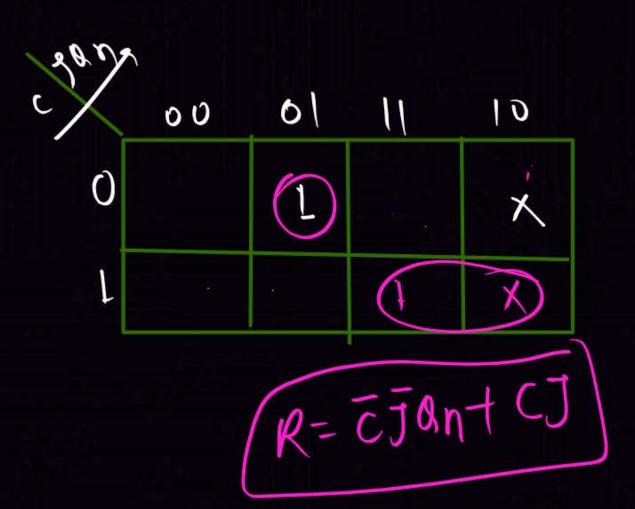


truth tuble

С	j	anti
0	0	Qn
0	1	9n
L	Ō	l
Ĺ	J	0

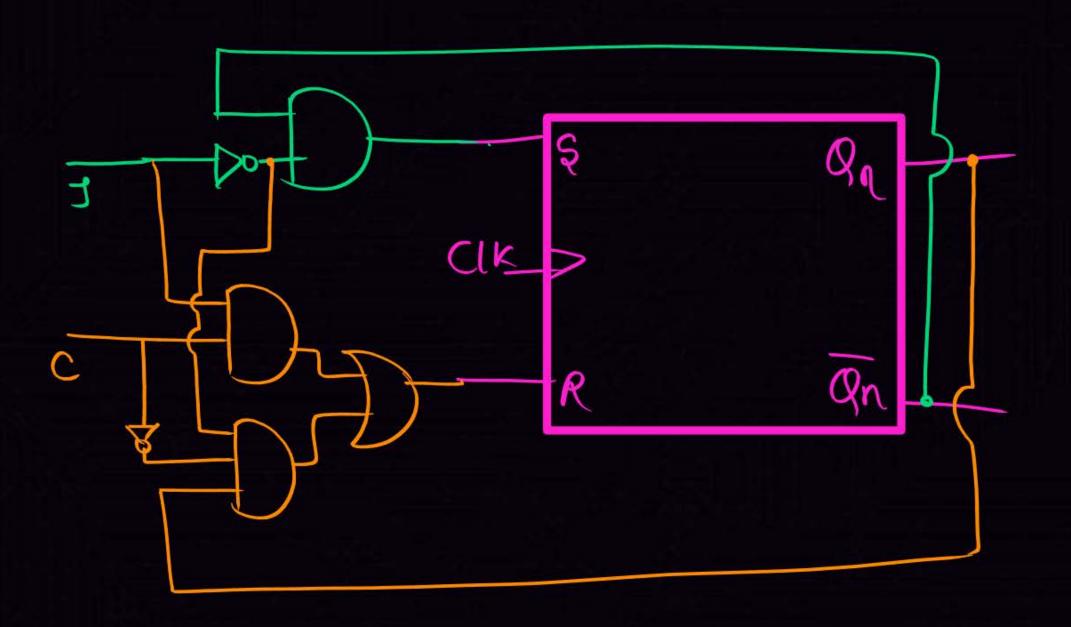
	C		Qr	Q _{n+1}	Sa	R
	0	0	0	1	1	0
	0	0	1	O .		1
1	0	L	0	0	0	×
	0	L	1	1	X	0
		O	Ø	1	Ţ	0
	T	0	1	1	×	O
	1	1	Ø	0	8	×
	L	1	J	Ò	0	1



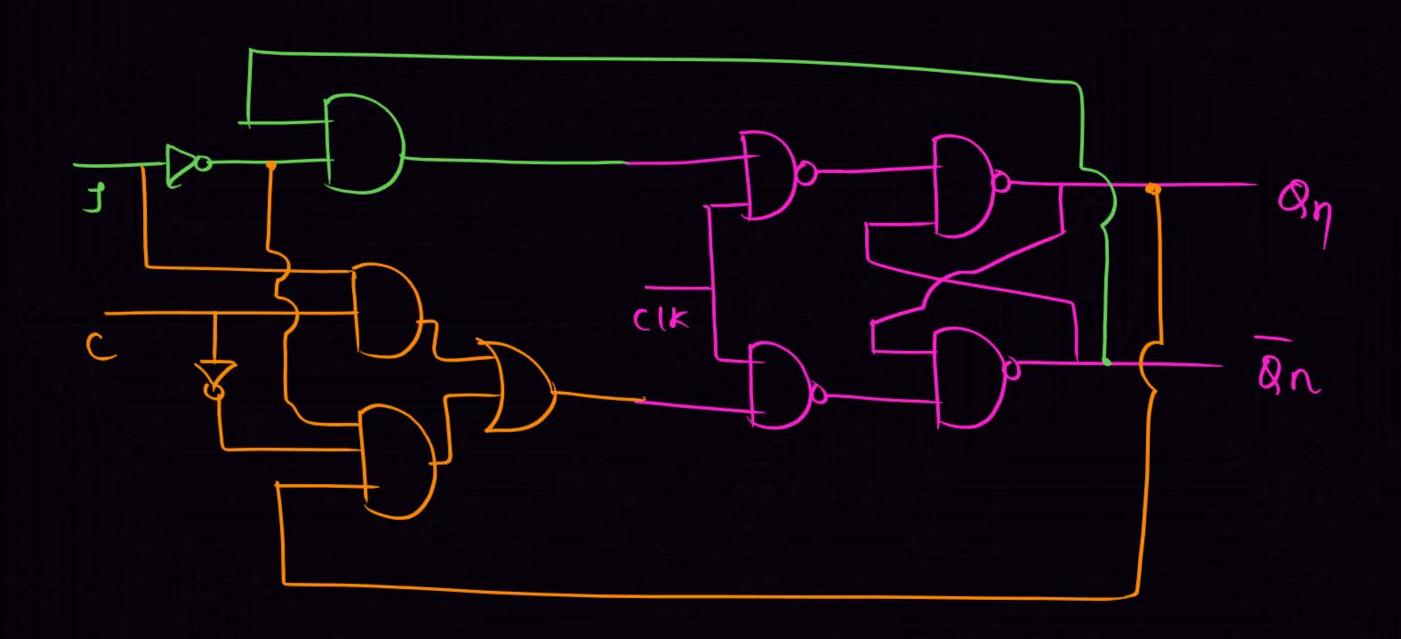














SR JK D T.

HND (12)

Discussion

Pw

HIP Of Resign a HS FF by using 7-1=F?

H	8	Patl
0	0	1
0	1	0
1	0	an
1	1	an



Thank you

Seldiers!

