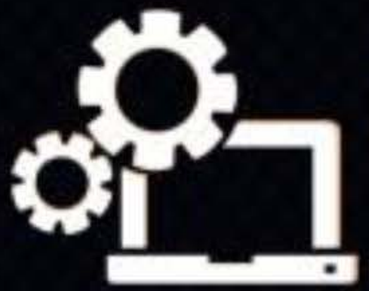
CS & IT ENGINEERING

DIGITAL LOGIC

Combinational Circuit



Lecture No. 7

By- CHANDAN SIR

01 DMux

02 Encoder

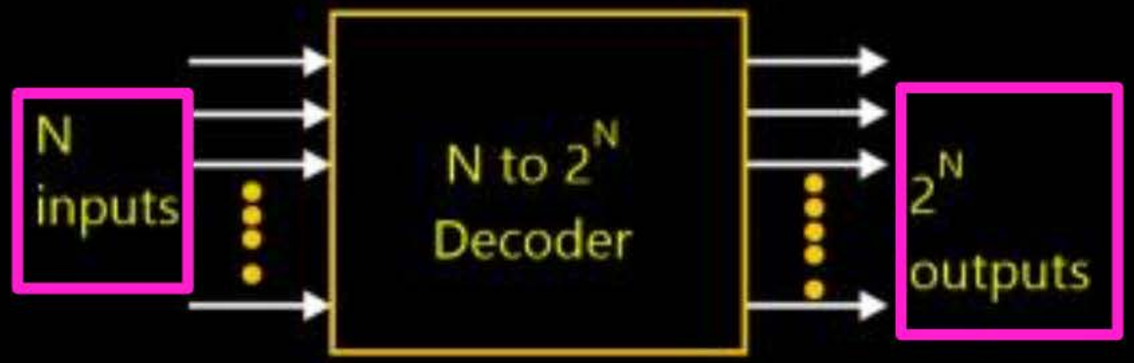
03 questons

05 Discussion

DECODER, HA, FA

DECODER → Circuit which is use to convert Binary into any other code.

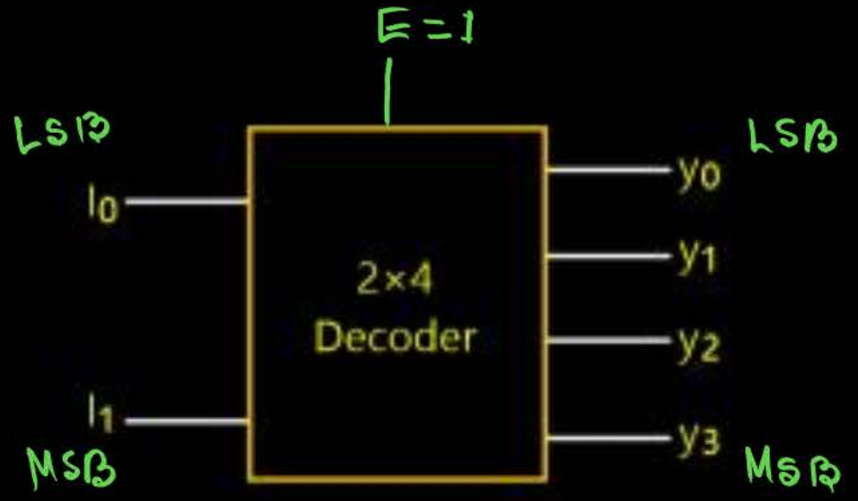
1. 2 × 4 Decoder
2. 3 × 8 Decoder
3. 4 × 16 Decoder



DECODER, HA, FA

2 × 4 DECODER

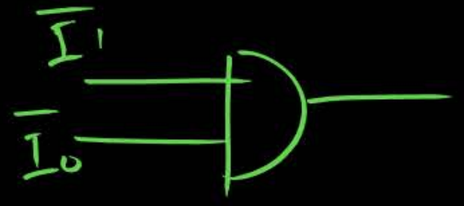
Step 1.



Step 2.

I_1	I_0	y_3	y_2	y_1	y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

DECODER, HA, FA



2 × 4 DECODER

$y_0 = \bar{I}_1 \bar{I}_0$

$y_1 = \bar{I}_1 I_0$

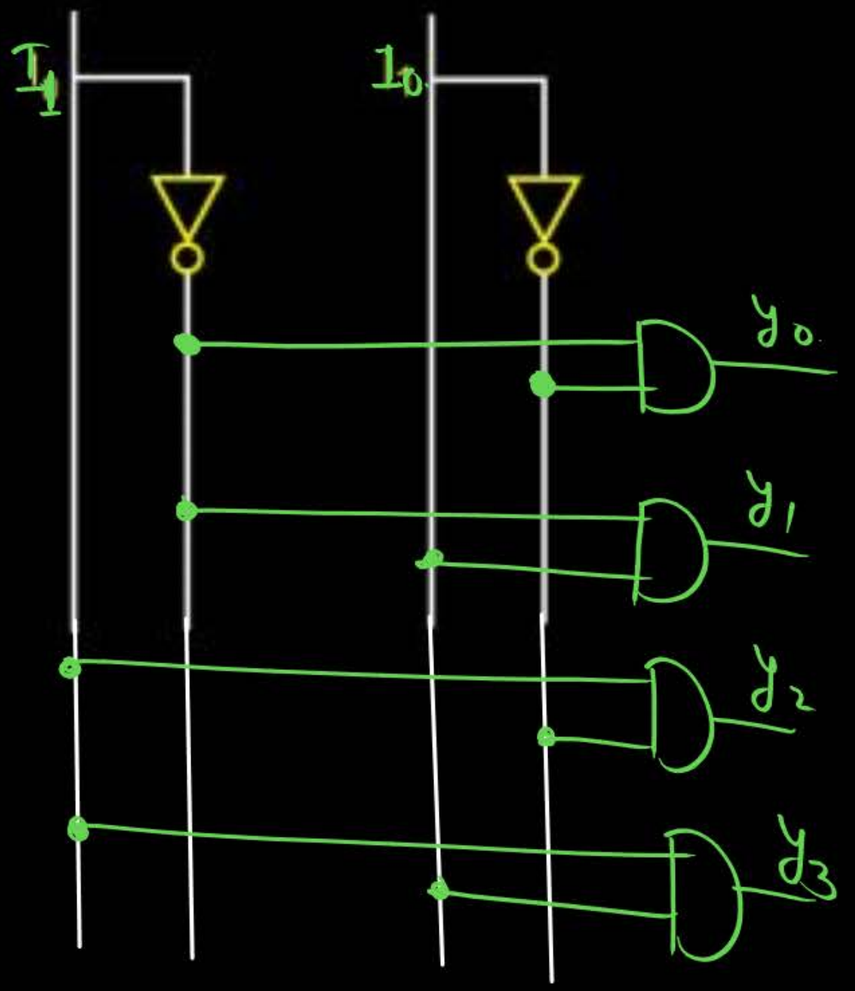
$y_2 = I_1 \bar{I}_0$

$y_3 = I_1 I_0$

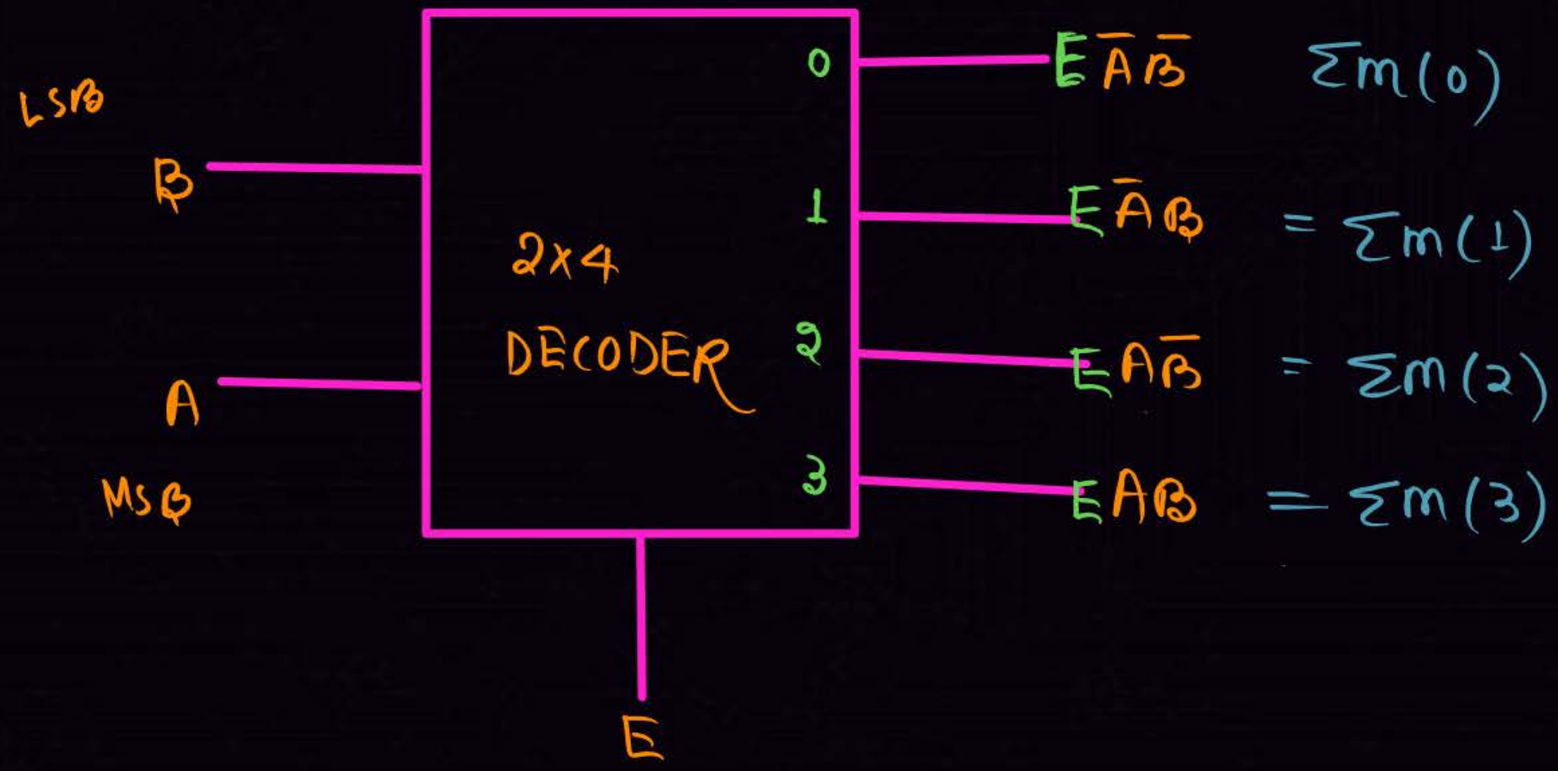
Step 3.

Step 4. Minimization

Step 5. Hardware Implementation

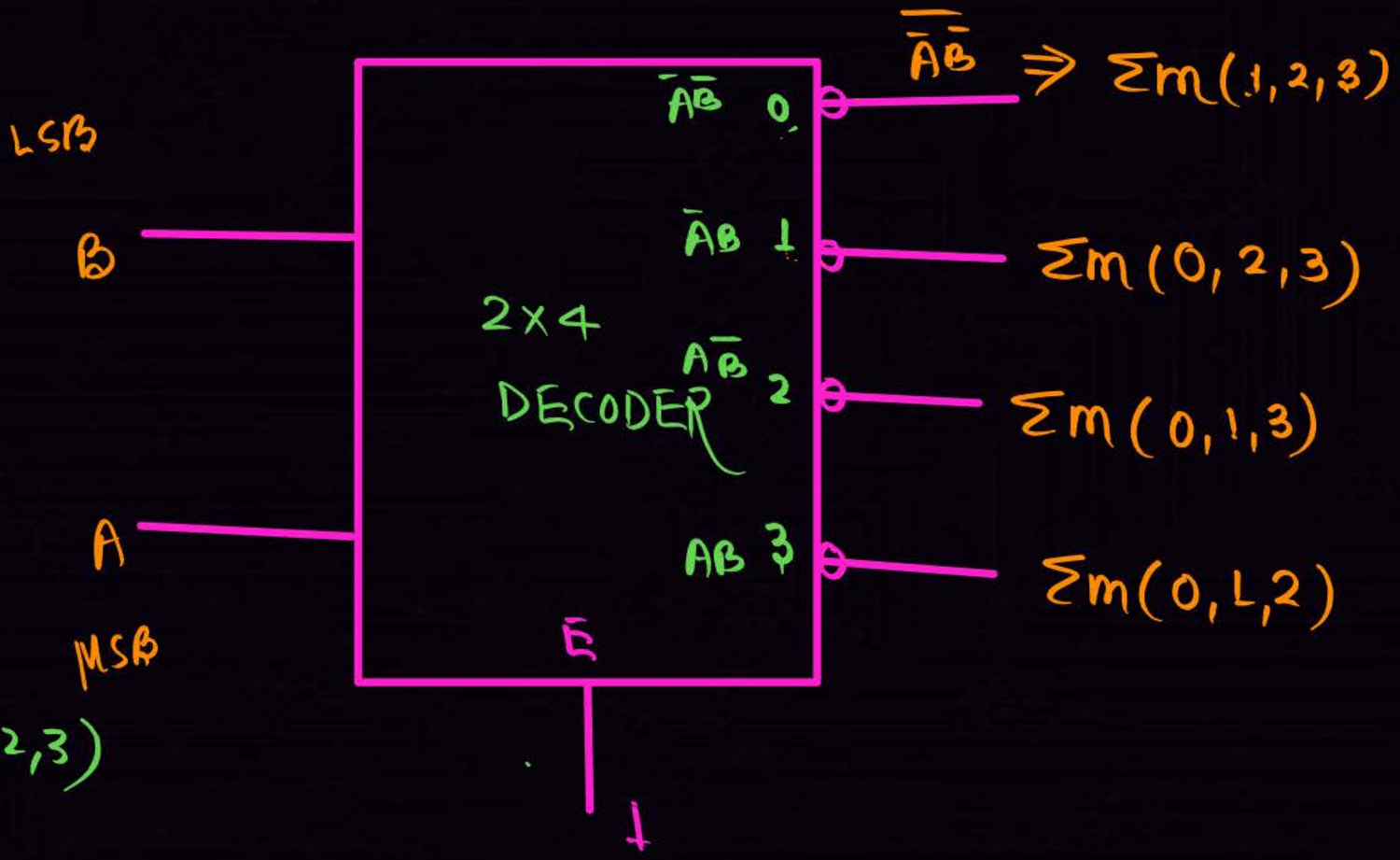


Example :


LSB
B
A
MSB
2×4
DECODER
0
1
2
3
E
$E\bar{A}\bar{B}$ $\Sigma m(0)$
$E\bar{A}B = \Sigma m(1)$
$EA\bar{B} = \Sigma m(2)$
$EAB = \Sigma m(3)$

A	B	f
0	0	0
0	1	1
1	0	1
1	1	1

$\overline{\bar{A}\bar{B}} = A+B$



POS

$f = (A+B)$

$= \Pi M(0)$

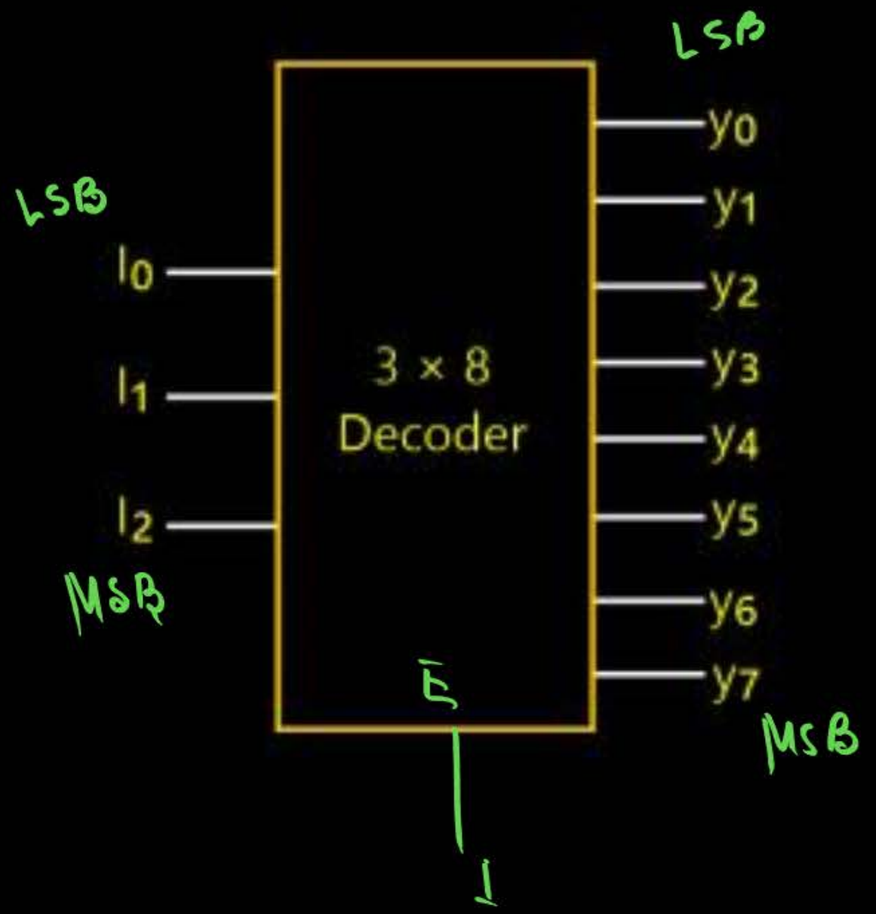
SOP

$f = \Sigma m(1,2,3)$

DECODER, HA, FA

3 × 8 DECODER

Step 1.



DECODER, HA, FA

3 × 8 DECODER

Step 2.

I_2 (MSB)	I_1	I_0 (LSB)	y_7 (MSB)	y_6	y_5	y_4	y_3	y_2	y_1	y_0 (LSB)
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

DECODER,

Step 4

Step 5

Step 3.

$$y_0 = \bar{I}_2 \bar{I}_1 \bar{I}_0$$

$$y_1 = \bar{I}_2 \bar{I}_1 I_0$$

$$y_2 = \bar{I}_2 I_1 \bar{I}_0$$

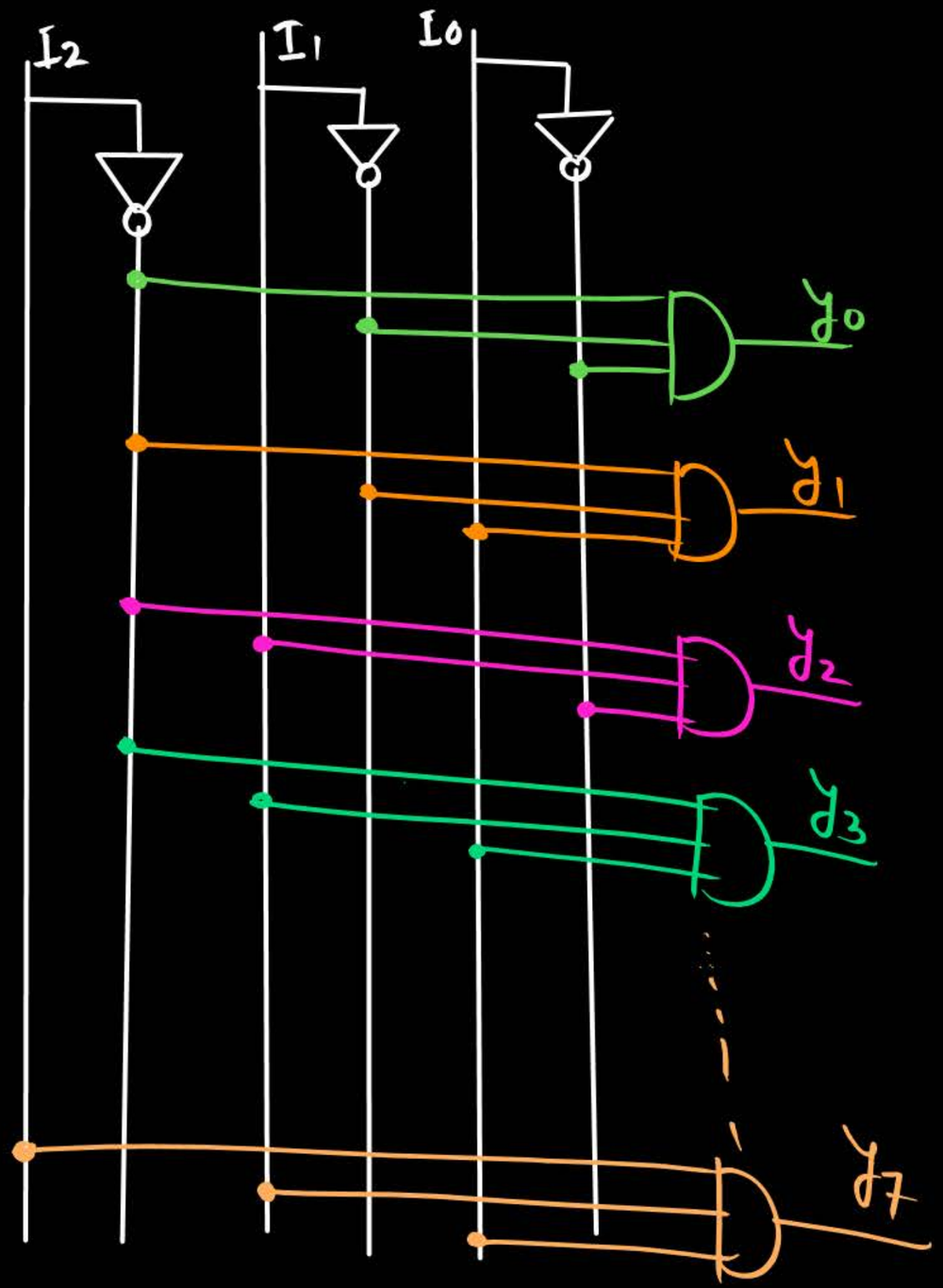
$$y_3 = \bar{I}_2 I_1 I_0$$

$$y_4 = I_2 \bar{I}_1 \bar{I}_0$$

$$y_5 = I_2 \bar{I}_1 I_0$$

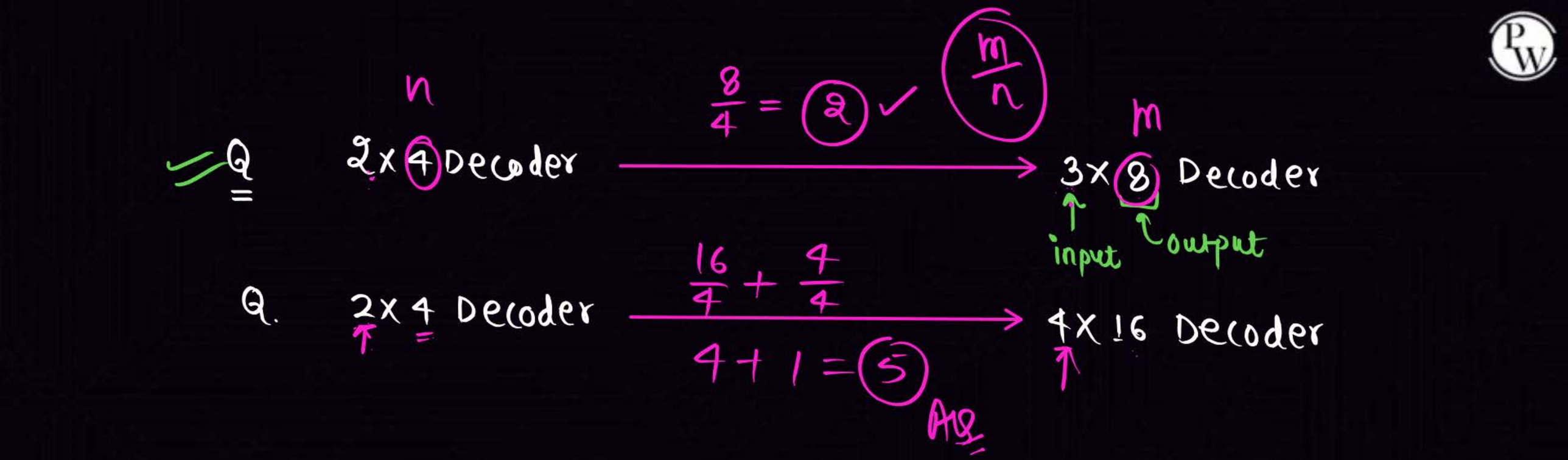
$$y_6 = I_2 I_1 \bar{I}_0$$

$$y_7 = I_2 I_1 I_0$$

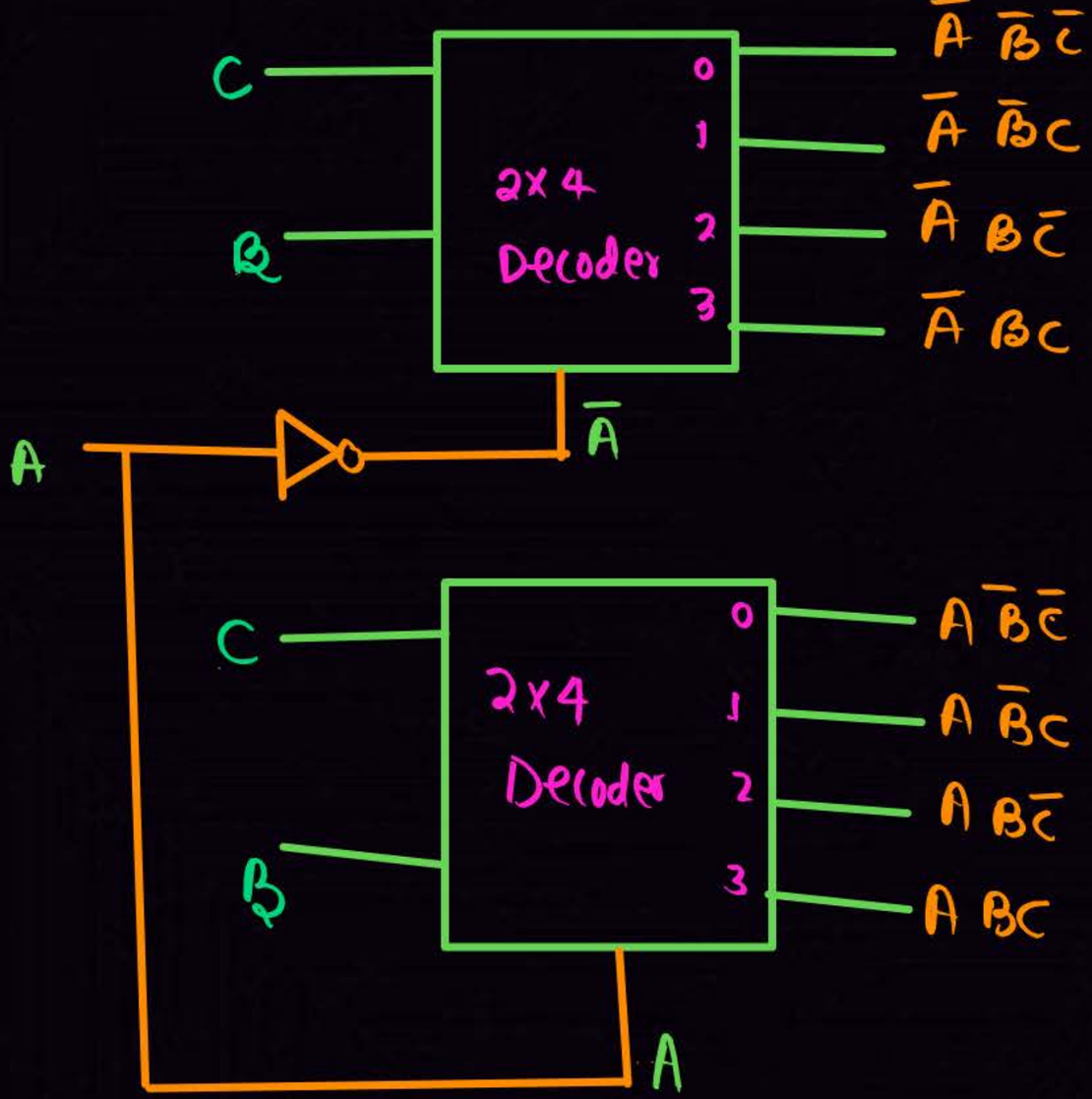


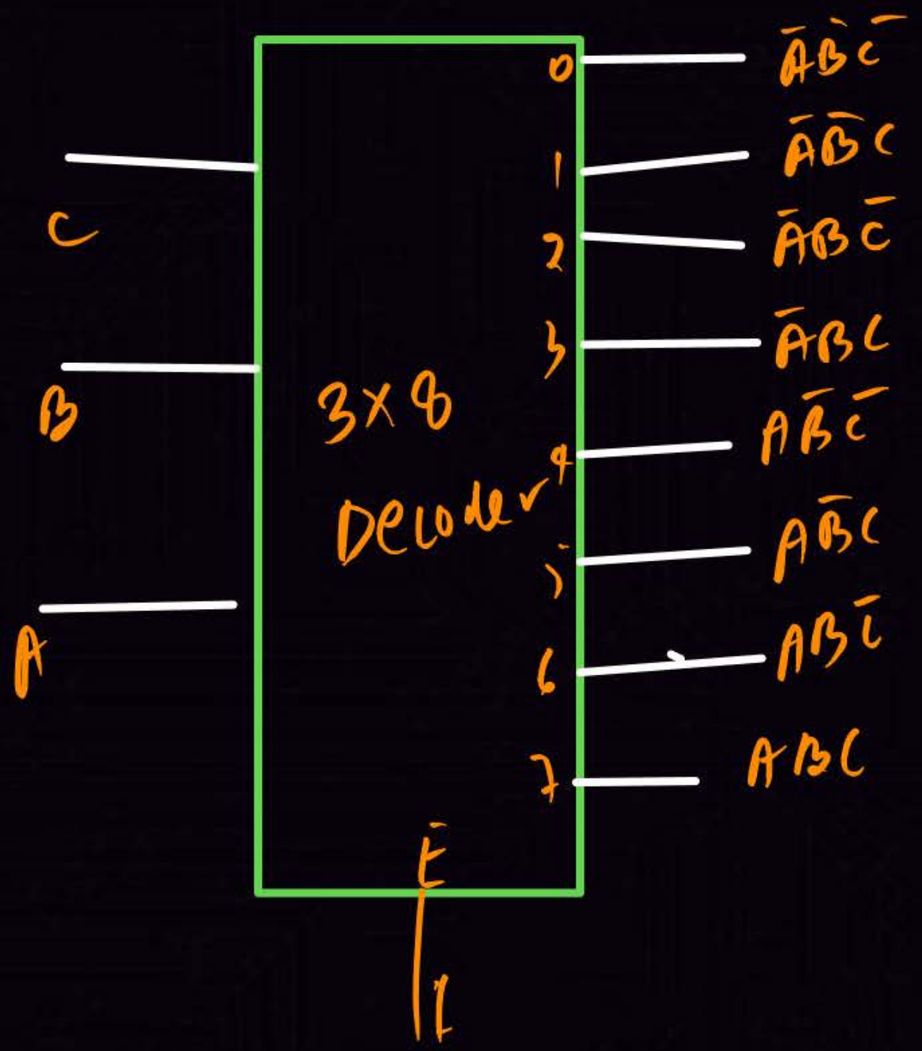
Q 4 X 16 Decoder

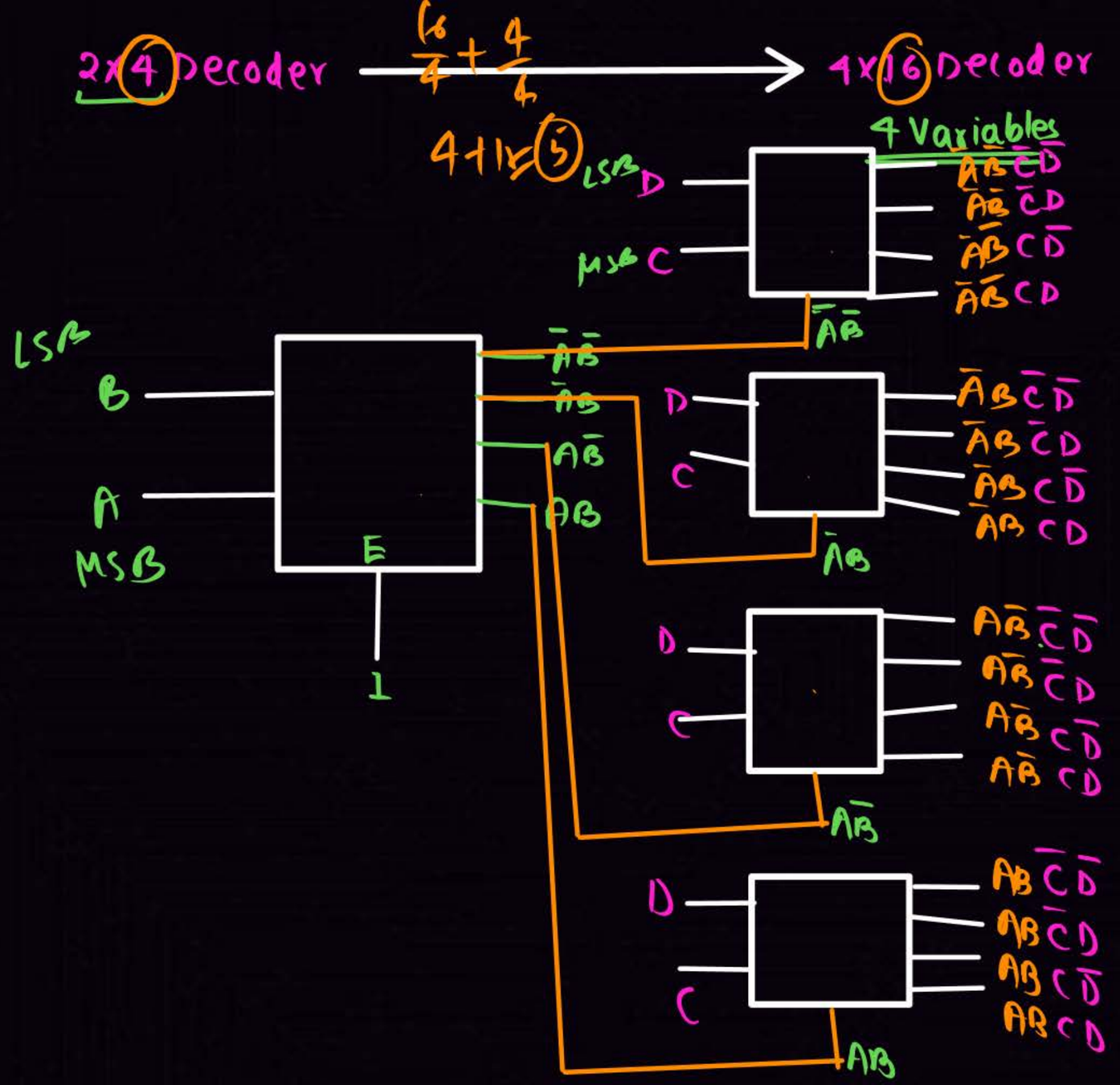
H.W


n
m
m/n
8/4 = 2 ✓
Q
2x4 Decoder
3x8 Decoder
input
output
Q.
2x4 Decoder
16/4 + 4/4
4+1 = 5
Ans
4x16 Decoder

2×4 ⟶ 3×8 Decoder

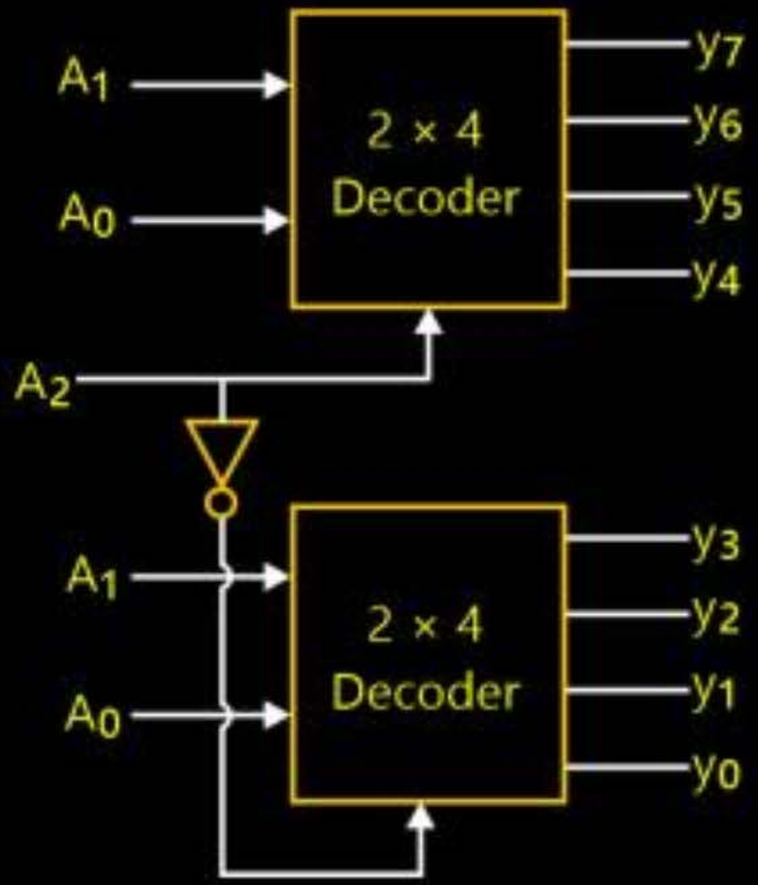





2x4 Decoder
16/4 + 4/4
4x16 Decoder
4+1=5
LSB D
MSB C
4 Variables
LSB
B
A
MSB
E
1
D
C

DECODER, HA, FA

DESIGN 3 × 8 DECODER BY USING 2 × 4 DECODER



3X8 Decoder $\xrightarrow{\frac{16}{8}}$ 4X16 Decoder

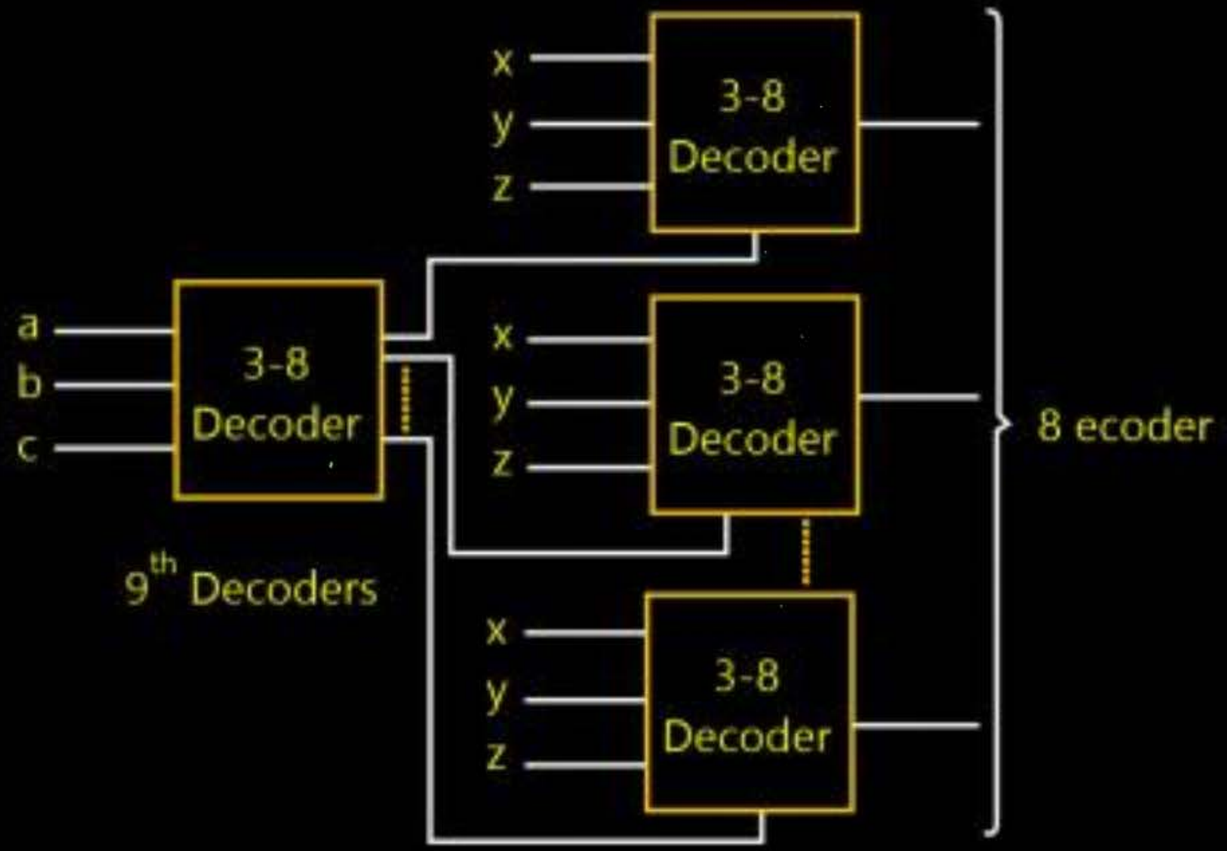
(2) Ans

3X8 Decoder $\xrightarrow{\frac{64}{8}+\frac{8}{8}}$ 6X64 decoder

8 + 1 = (9) Ans

DECODER, HA, FA

3x8 Decoder ⟶ 6x64 Decoder



HW

Q = Design Binary to Decimal Decoder?

Q.1

A logic circuit consist of two 2 × 4 decoders as shown in the figure. The output of decoder are as follow:

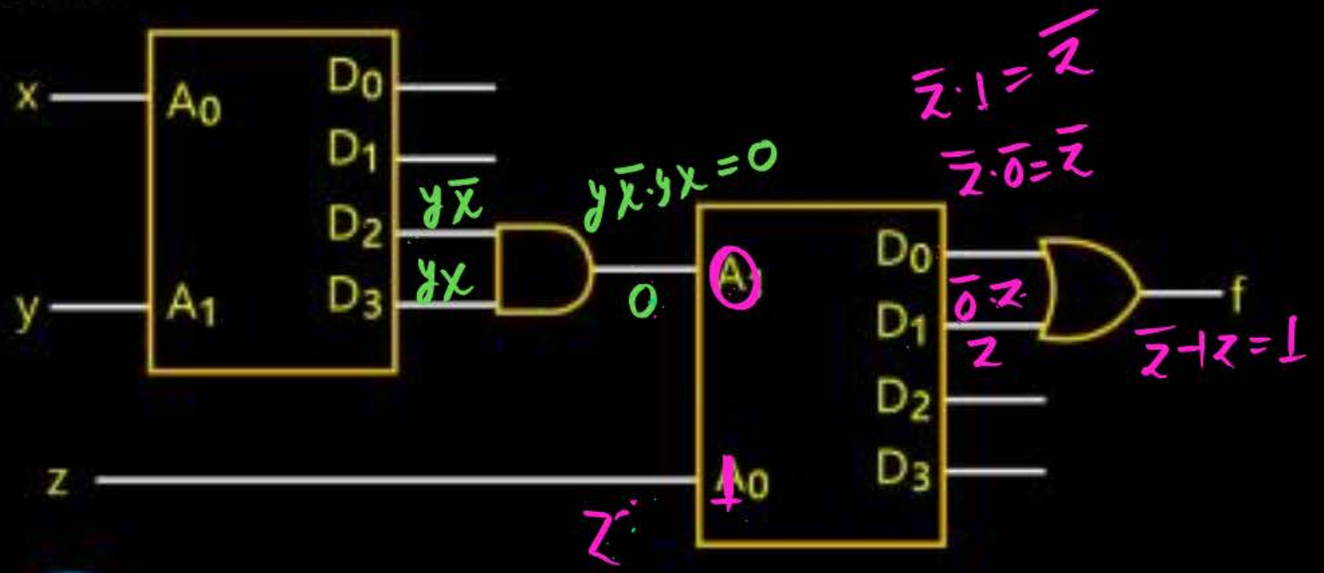
D0 = 1 when A0 = 0, A1 = 0

D1 = 1 when A0 = 1, A1 = 0

D2 = 1 when A0 = 0, A1 = 1

D3 = 1 when A0 = 1, A1 = 1

The value of f(x, y, z) is



A_1 (y)	A_0 (x)	y
0	0	$D_0 = 1$
0	1	D_1
1	0	D_2
1	1	D_3

(A) 0

(B) z

(C) $\bar{z}$

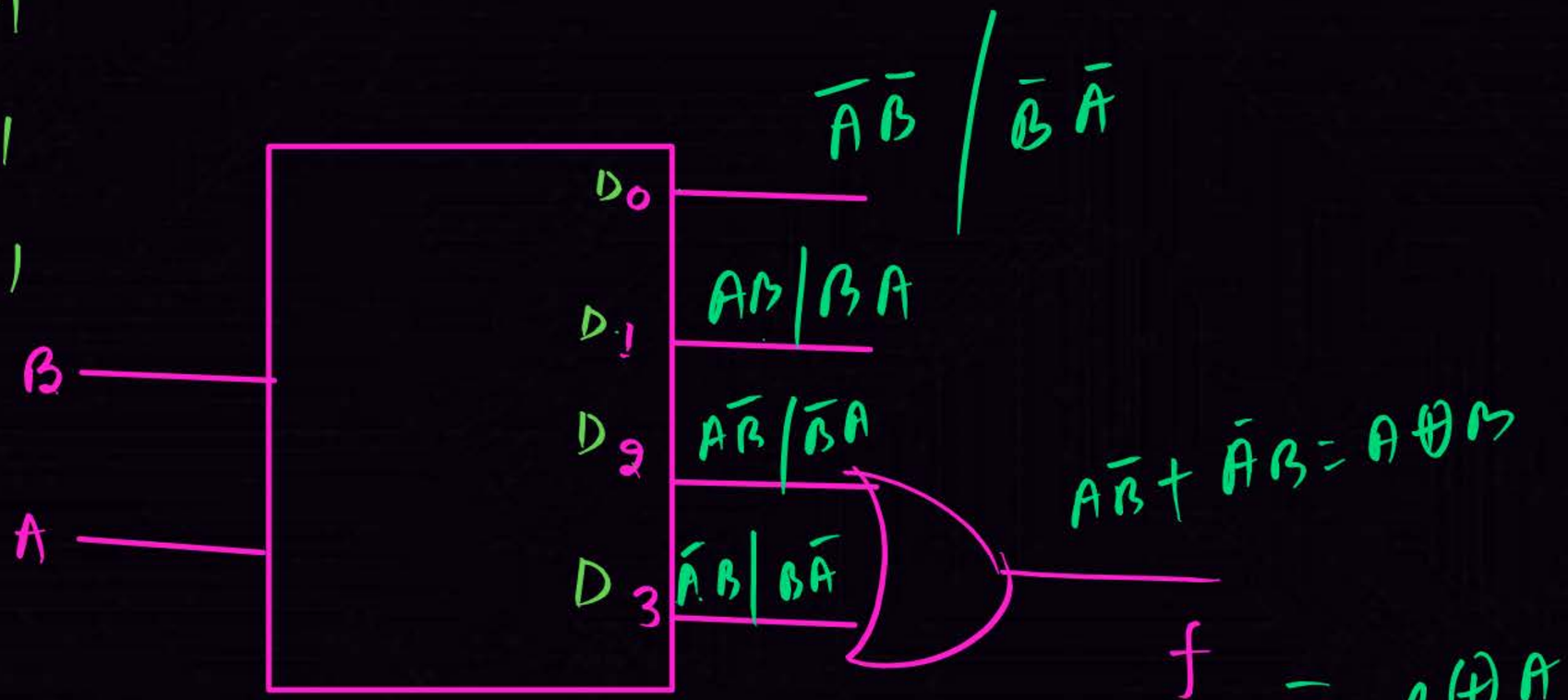
(D) 1

$A=0 \quad B=0 \quad D_0=1$

$A=1 \quad B=0 \quad D_2=1$

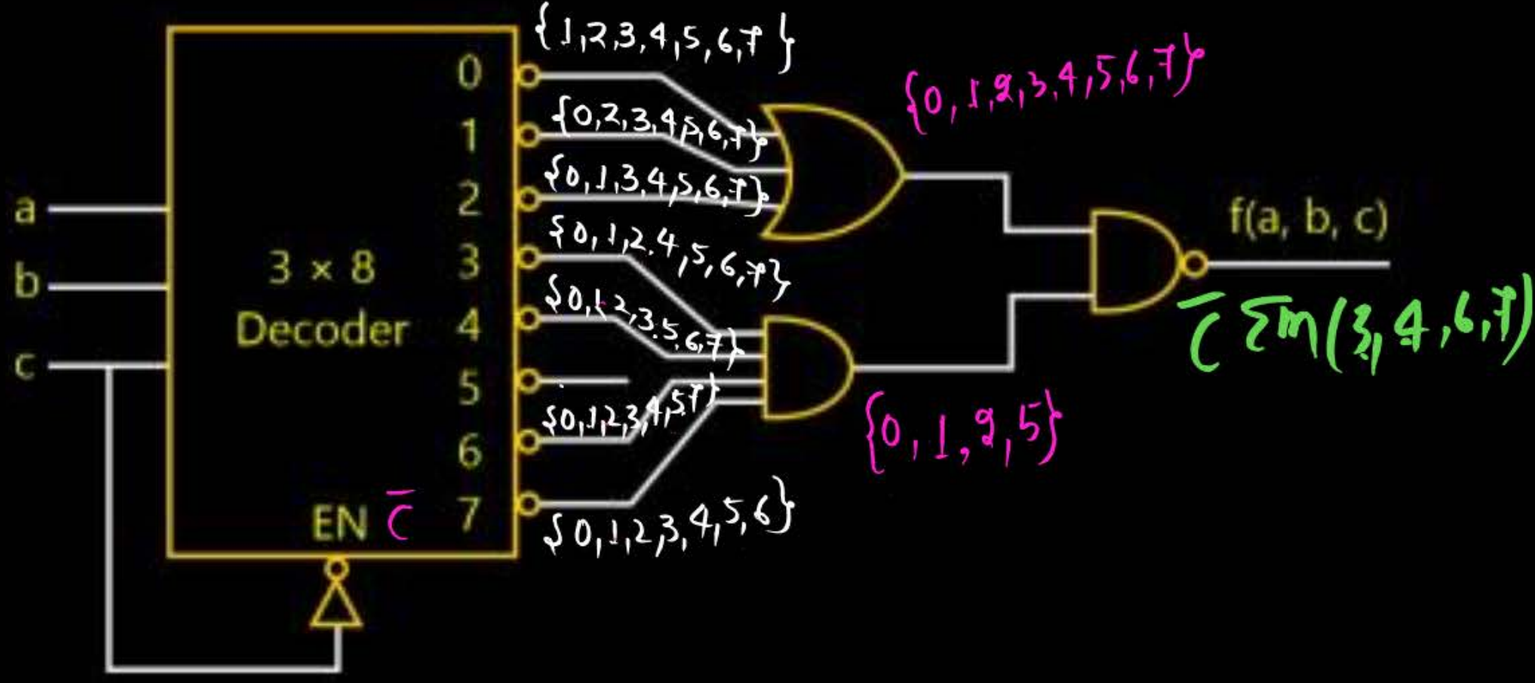
$A=0 \quad B=1 \quad D_3=1$

$A=1 \quad B=1 \quad D_1=1$



Q.2

The Boolean expression f(a, b, c) in its canonical form for the decoder circuit shown below is

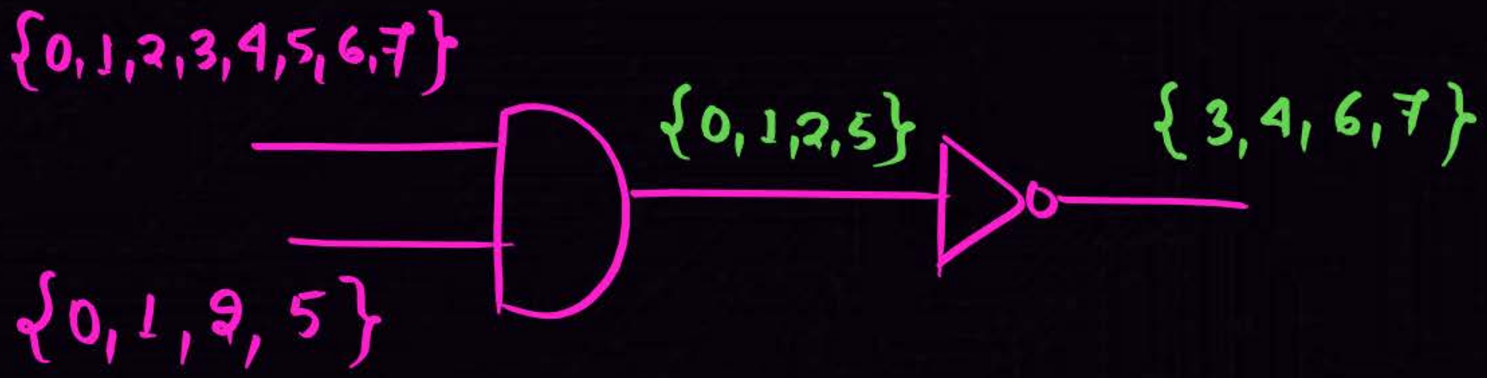


A. $\Pi M(4, 6)$

B. $\Sigma m(0, 1, 2, 3, 5, 7)$

C. $\Sigma m(4, 6)$

D. $\Pi M(0, 1, 2, 3, 5)$



$$f = \bar{C} \cdot \Sigma m(3,4,6,7)$$

$$= \bar{C} \cdot [\bar{A}BC + A\bar{B}\bar{C} + AB\bar{C} + ABC]$$

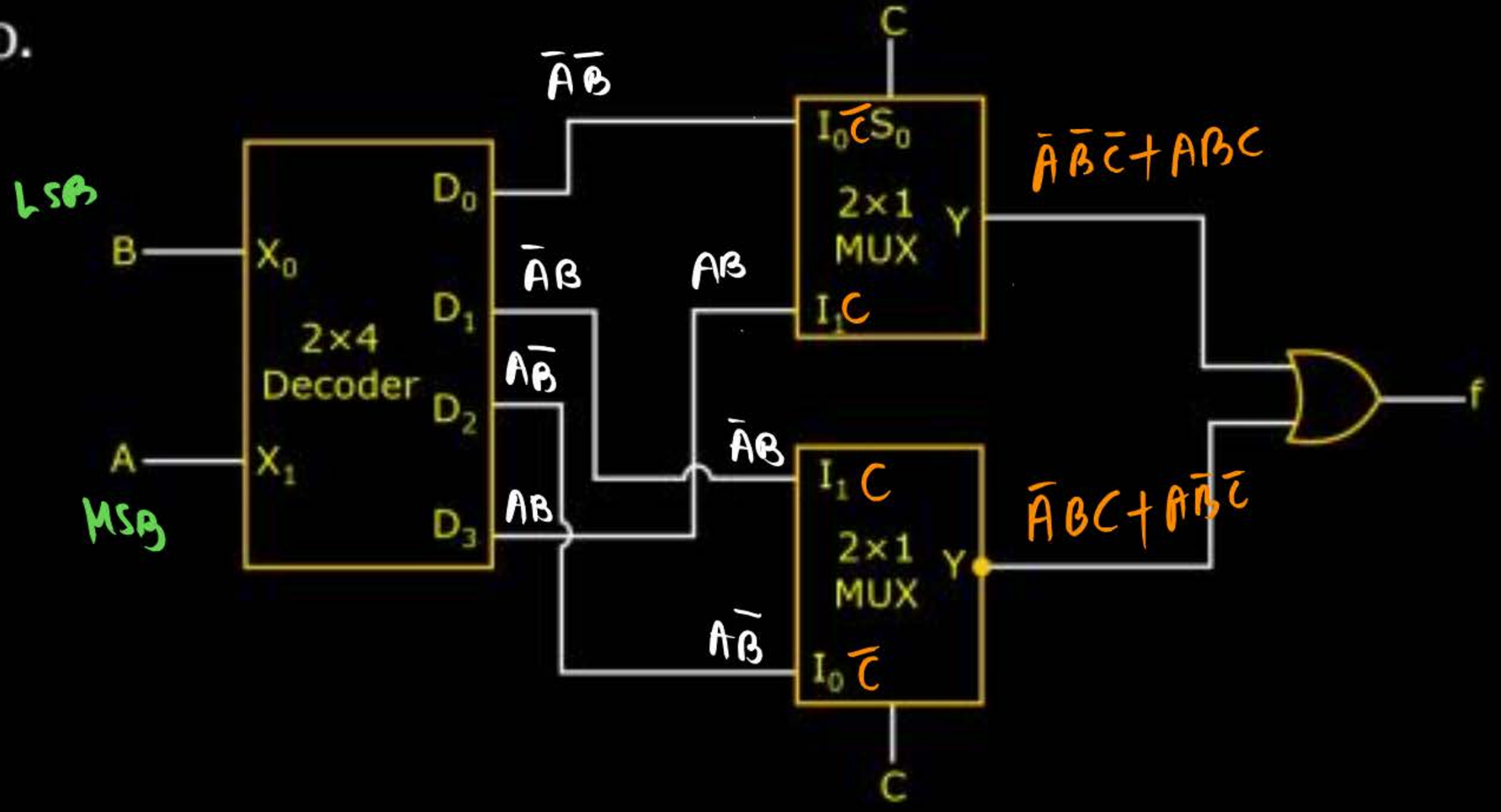
$$= \bar{A}BC \cdot \bar{C} + A\bar{B}\bar{C} \cdot \bar{C} + AB\bar{C} \cdot \bar{C} + ABC \cdot \bar{C}$$

$$= A\bar{B}\bar{C} + AB\bar{C}$$

$$= \Sigma m(4,6)$$

Q.2

A logic function 'f' is implemented by the circuit shown in the figure below. The circuit consists of one 2×4 decoder, two 2×1 multiplexers and a two input or gate connected in cascade. Then the function f is equal to.



A. $A \oplus B$

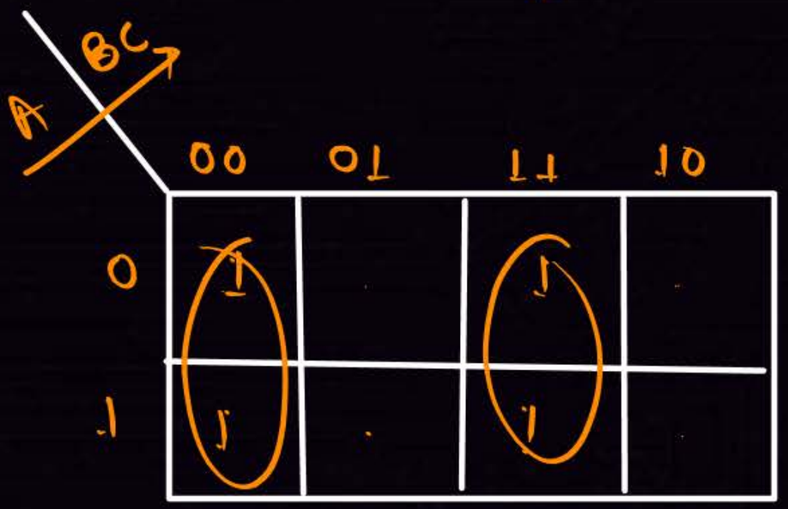
B. $A \oplus B \oplus C$

C. $B \odot C$

D. $A \odot B$

$$f = \bar{A}\bar{B}\bar{C} + ABC + \bar{A}BC + A\bar{B}\bar{C}$$

$$= \Sigma m(0, 3, 4, 7)$$



$$\bar{B}\bar{C} + BC = B \odot C$$

Ans.

Q.3

time/CJSIR

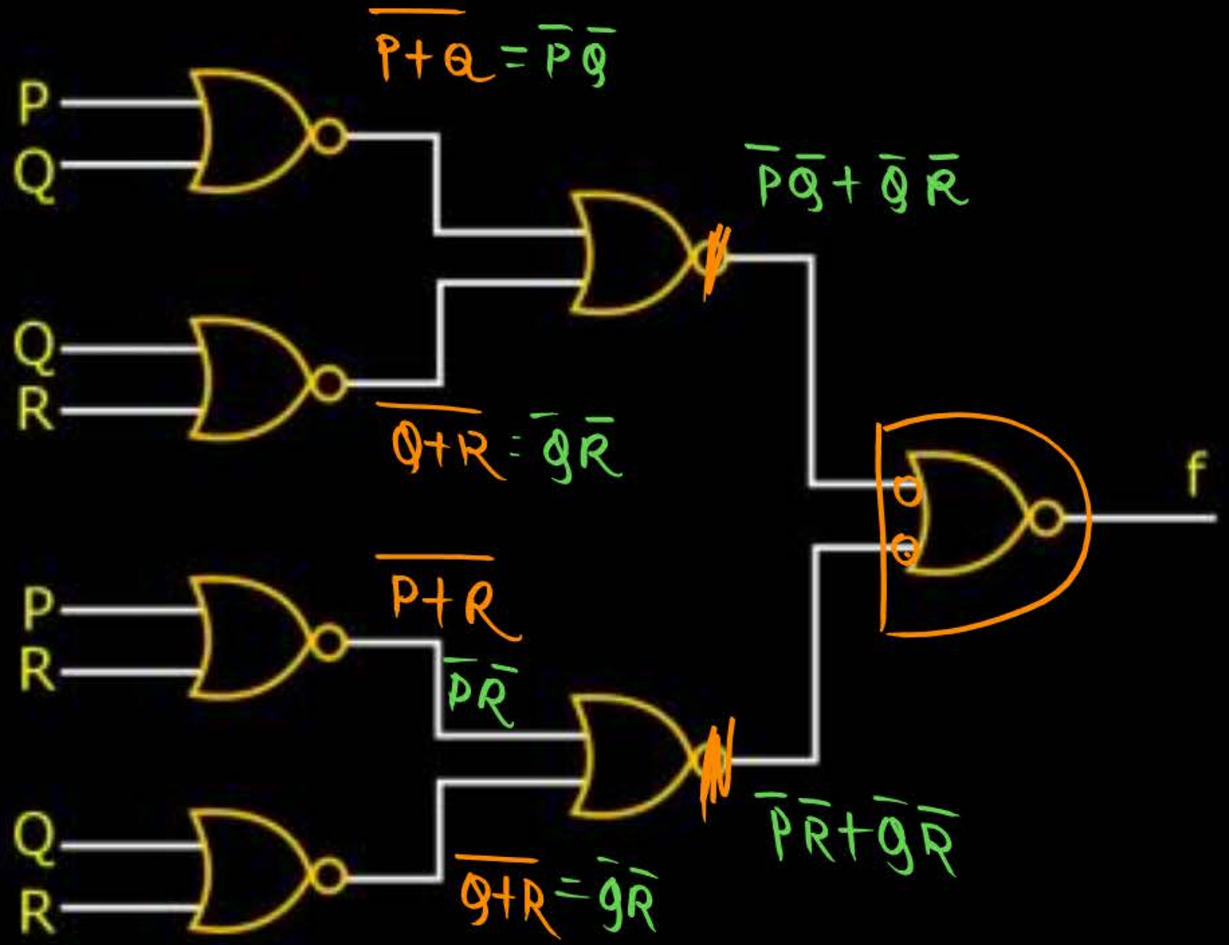
What is the Boolean expression for the output f of the combinational logic circuit of NOR gates given below?

A $\overline{Q+R}$

B $\overline{P+Q}$

C $\overline{P+R}$

D $\overline{P+Q+R}$



$$f = [\bar{P}\bar{Q} + \bar{Q}\bar{R}] \cdot [\bar{P}\bar{R} + \bar{Q}\bar{R}]$$

$$= \bar{P}\bar{Q}\bar{R} + \bar{P}\bar{Q}\bar{R} + \bar{P}\bar{Q}\bar{R} + \bar{Q}\bar{R}$$

$$= \bar{P}\bar{Q}\bar{R} + \bar{Q}\bar{R}$$

$$= \bar{Q}\bar{R}[1 + \bar{P}]$$

$$= \bar{Q}\bar{R}$$

$$= \overline{Q + R}$$

option (A)

Q.4

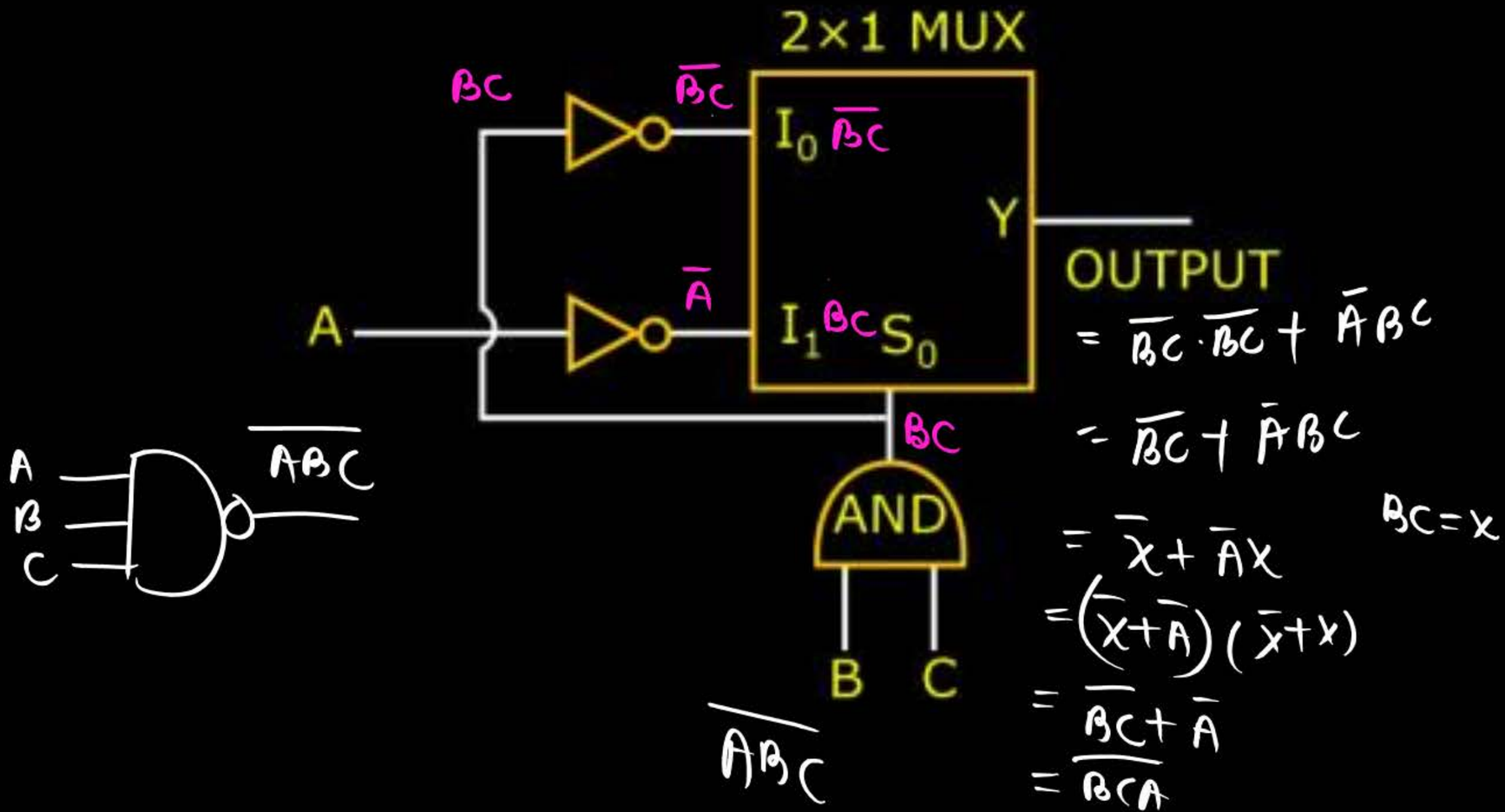
The combinational circuit given below implements which of the following

A. NOR gate

B. XOR gate

C. NAND gate

D. None of these



Q.5

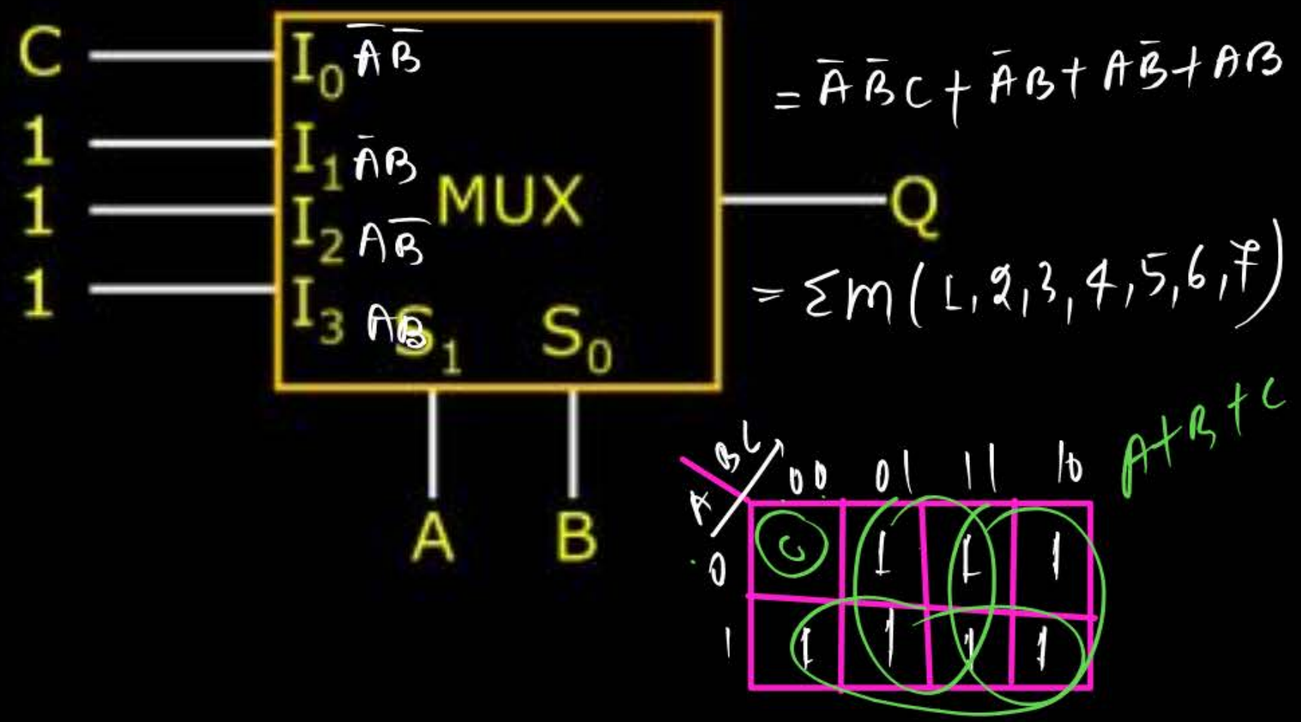
The combinational logic circuit shown in the given figure has an output Q which is

(A) ABC

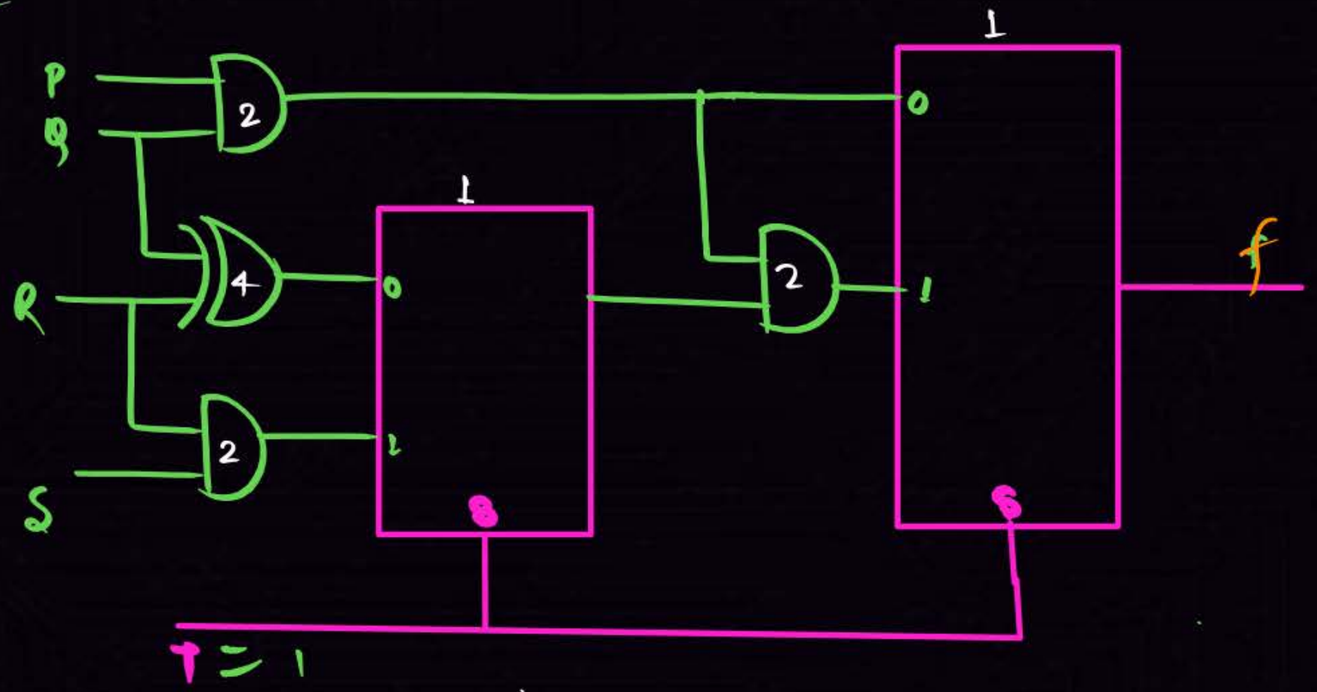
(B) A + B + C

(C) $A \oplus B \oplus C$

(D) A.B + C



Q



Max = 6ns

Case T=0

$T = T_{AND} + T_{MUX_2}$

$T = 2 + 1 = 3ns$

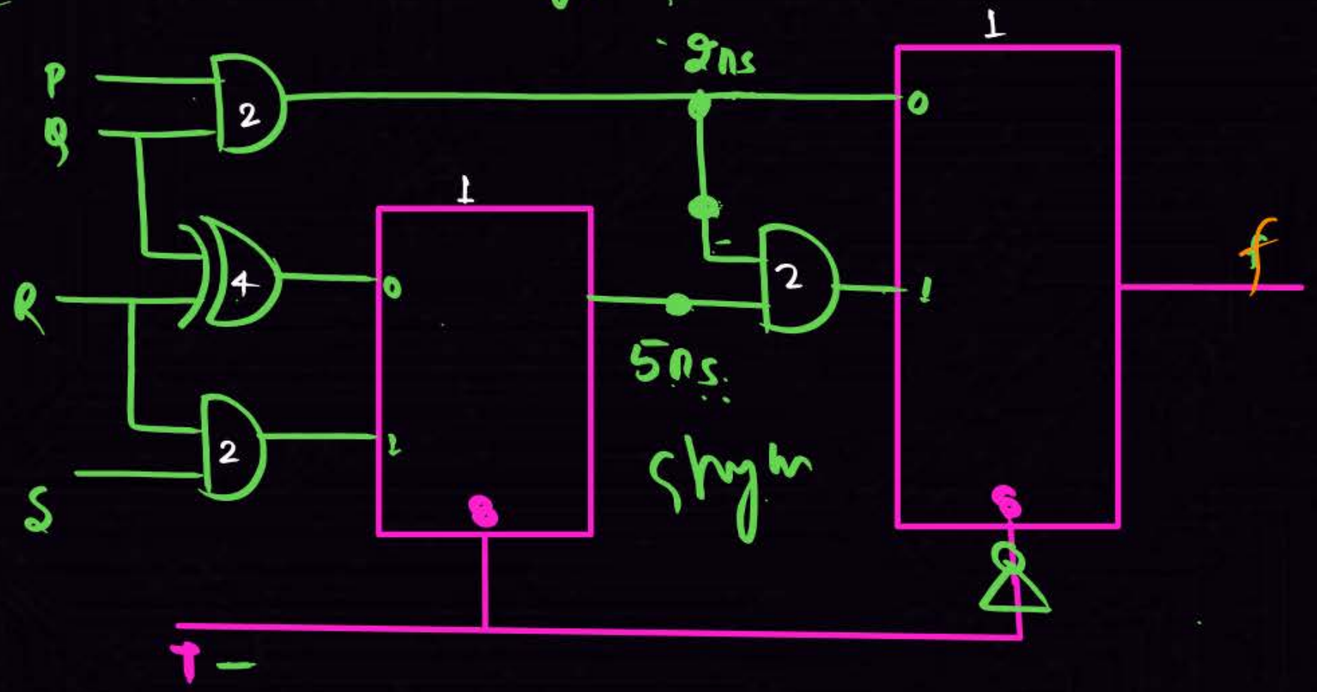
Case(2) T=1

$T = T_{AND_2} + T_{MUX} + T_{AND} + T_{MUX}$

$= 2 + 1 + 2 + 1$

$= 6ns$

Q



case(1) T=0

$T = T_{XOR} + T_{MUX} + T_{AND} + T_{MUX}$

$= 4 + 1 + 2 + 1$

$= 8ns$

case(2) T=1

$T = T_{AND} + T_{MUX}$

$T = 2 + 1 = 3ns$

Thank you

GW

Soldiers !