CS & IT ENGINEERING

Digital Logic

LOGIC GATE

Lecture No. 2

By- CHANDAN SIR

01 AND GATE

02 OR GATE

03 Discussion

04 Question Practice

Basic GATE

- NOT
- # AND
- OR

Universal GATE

- NAND
- NOR

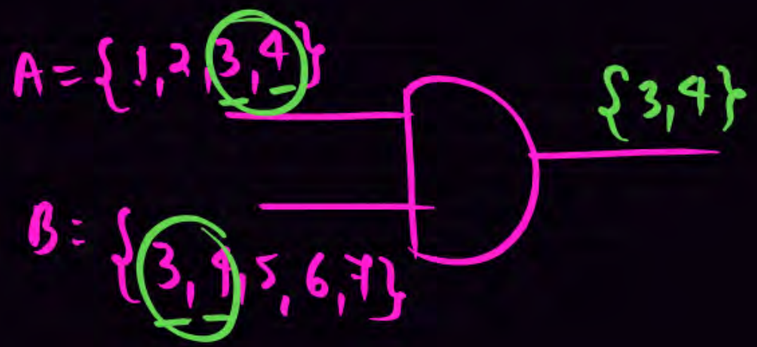
Exclusive GATE

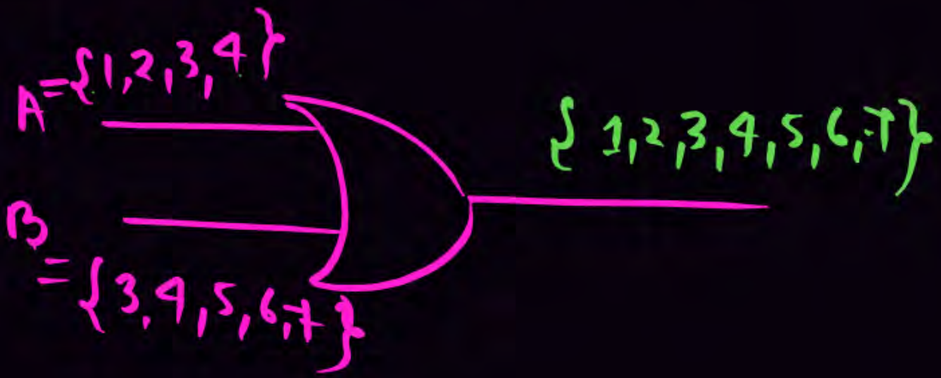
- X-OR
- X-NOR

AND

t.me/CJsir

OR





AND

$0 \cdot 0 = 0$

$0 \cdot 1 = 0$

$1 \cdot 0 = 0$

$1 \cdot 1 = 1$

$A \cdot A = A$

$A \cdot 1 = A$

$A \cdot 0 = 0$

$A \cdot \bar{A} = 0$

OR

$0 + 0 = 0$

$0 + 1 = 1$

$1 + 0 = 1$

$1 + 1 = 1$

$A + A = A$

$A + 0 = A$

$A + 1 = 1$

$A + \bar{A} = 1$

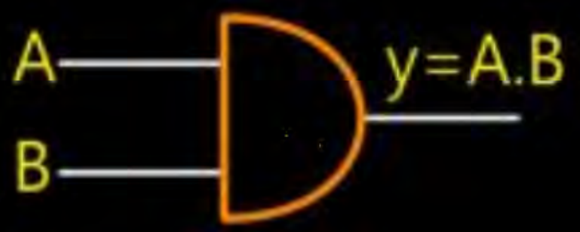
$1 + A + AB = 1$

AND GATE

time/CJSLR

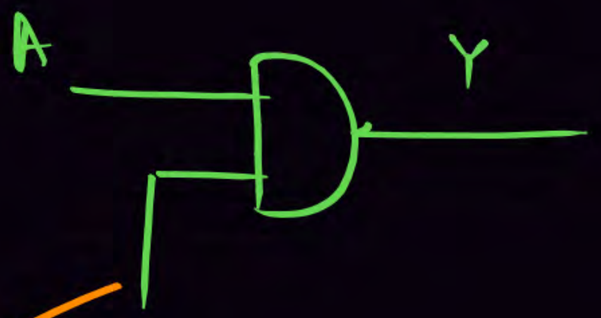
- **AND GATE** → Intersection

1. Symbol



2. Symbol

Truth Table		
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1



floating terminal

Control input

Strobe

AND GATE

- **AND GATE**

3. Enable/Disable

CONTROL '0' DISABLE

CONTROL '1' ENABLE

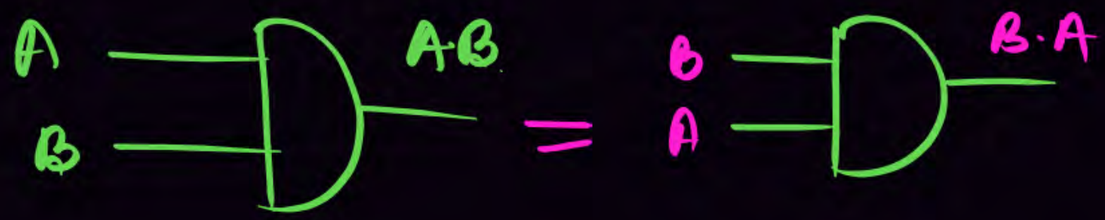
4. Commutative Law

$A.B = B.A$

Associative Law

$A.B.C = (A.B).C$

Commutative Law: ✓



Associative Law: ✓

$$(A \cdot B) \cdot C = A \cdot (B \cdot C)$$ ✓

Fanin

₹20

₹20

A, B

A.B

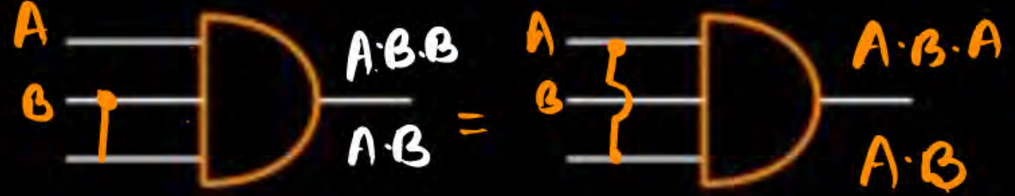
₹10

AND GATE

TTL → Transistor-Transistor Logic

5.

(1) ~~X~~



Fanout ↓

(2) ~~X~~

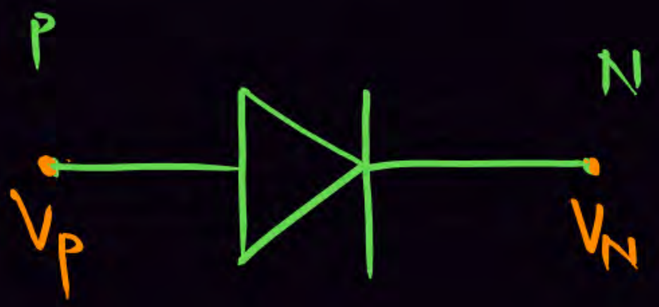
Pull up arrangement

Costly

(3) ~~X~~

NOISE MARGIN ↓

"Diode"

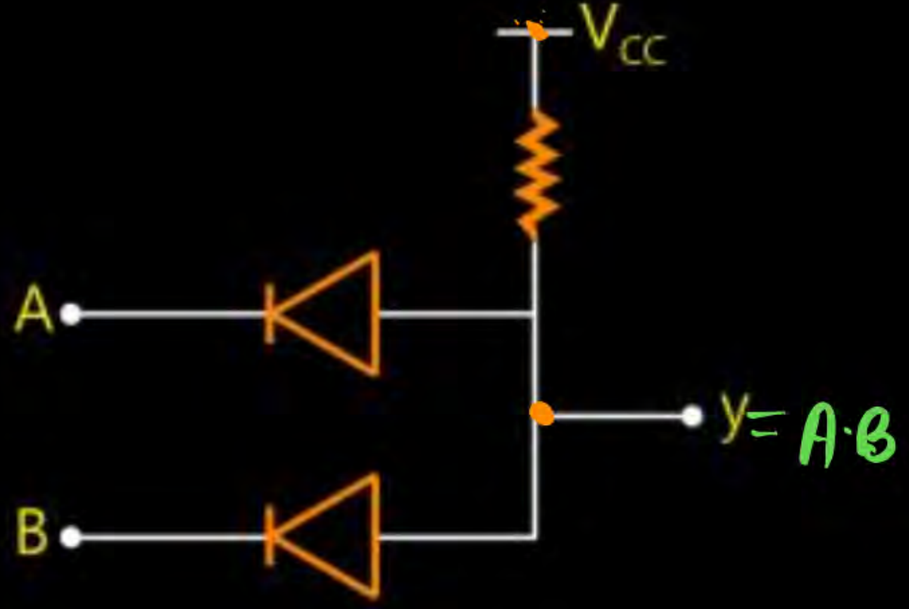


$V_P > V_N$ → Forward Bias → Short circuit

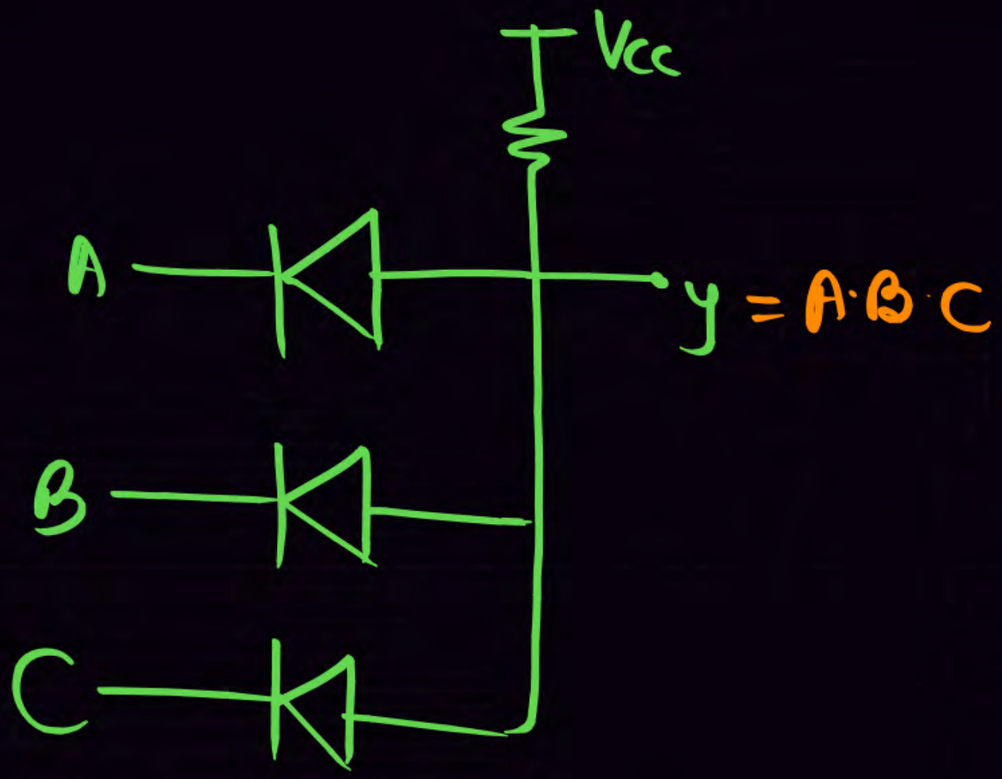
$V_P < V_N$ → Reverse Bias → Open circuit

AND GATE

6. Circuit Diagram



A	B	D_A	D_B	y
0	0	FB	FB	0
0	1	FB	RB	0
1	0	RB	FB	0
1	1	RB	RB	1


Vcc
A
B
C
y = A·B·C

- **NOTE**

1. Whenever logic are designed by TTL (Transistor transistor logic) then floating terminal always works as a high.
2. Whenever logic are designed by ECL (Emitter coupled logic) then floating terminal always works as a low.
3. Noise margin- Maximum noise added to the input which will not affect the output are called Noise Margin
4. Fan out

   The number of logic driven by the logic are called fan out
5. Fan in

   Number of input of a logic are called fan in.
6. ECL is the fastest logic among all the logic family.

OR GATE

t.me/cjs2R

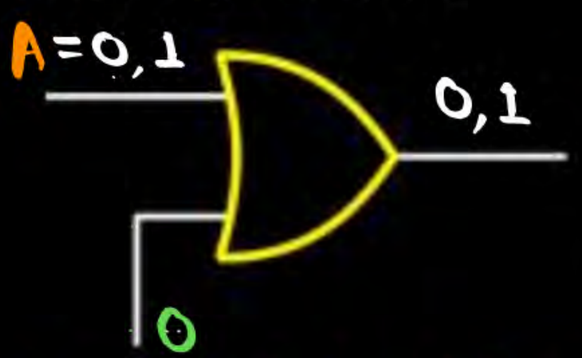
1. Symbol

2. Truth Table

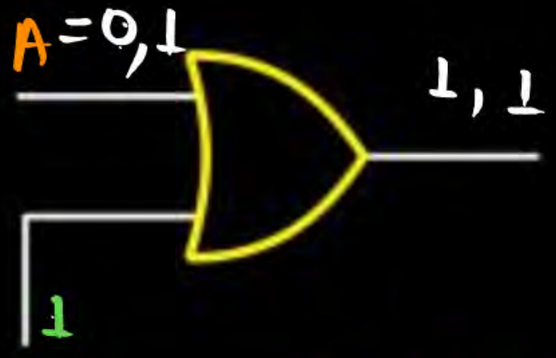
Truth Table		
A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

OR GATE

3. Enable/disable



CONTROL '0' ENABLE



CONTROL '1' DISABLE

4. Commutative Law

$$A + B = B + A$$ ✓

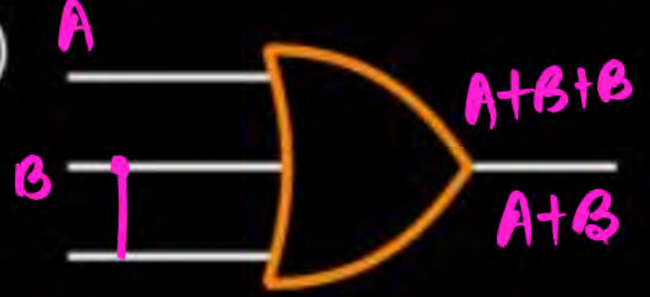
5. Associative Law

$$A + (B + C) = (A + B) + C$$ ✓

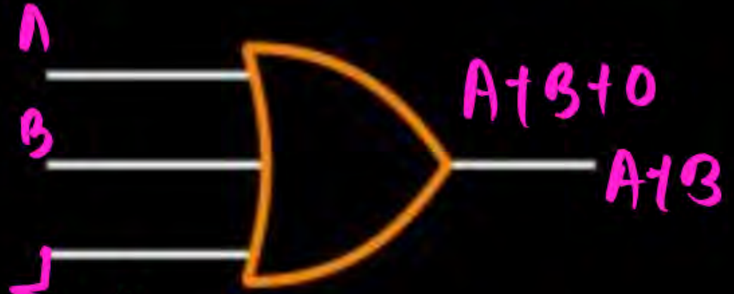
OR GATE

ECL
↳ Emitter coupled logic

(a)



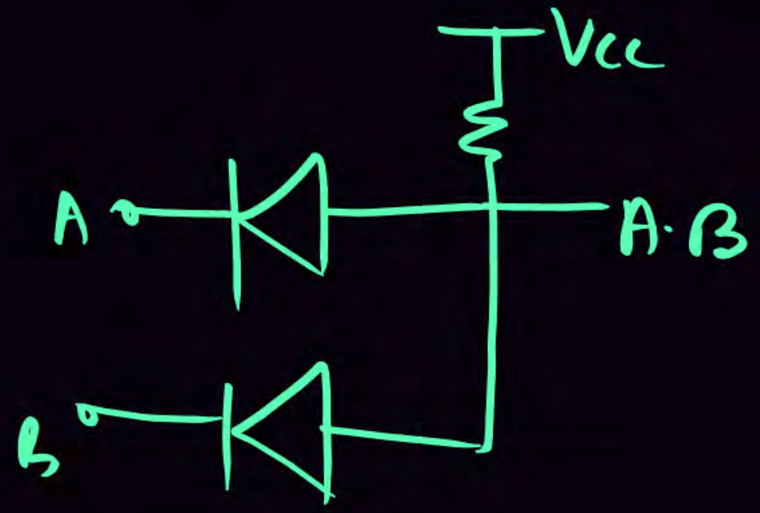
(b)



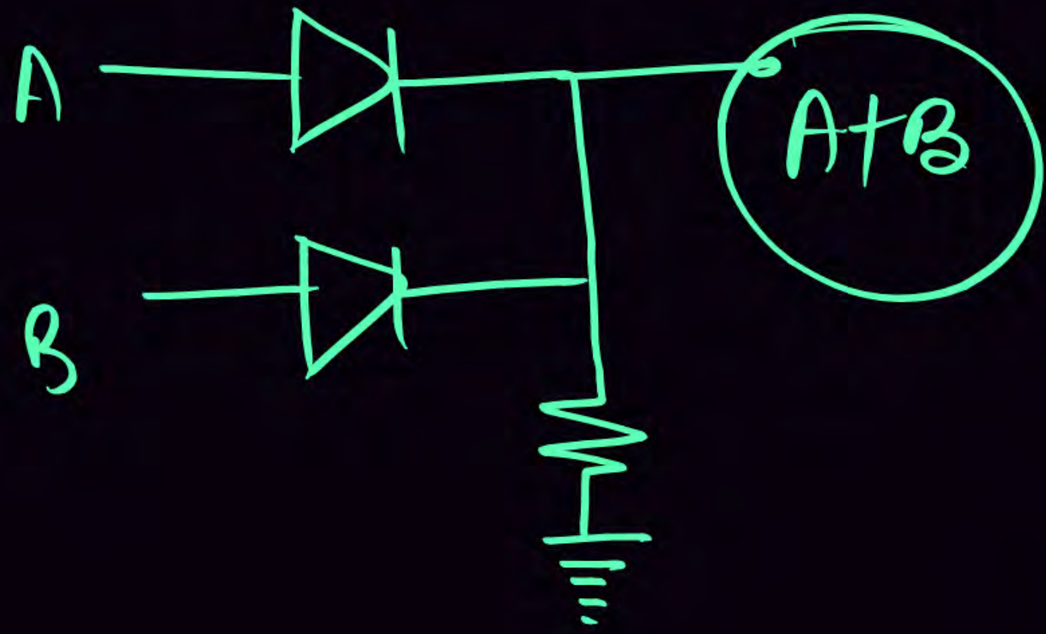
pull down arrangement

(c)

A+B+0 = A+B

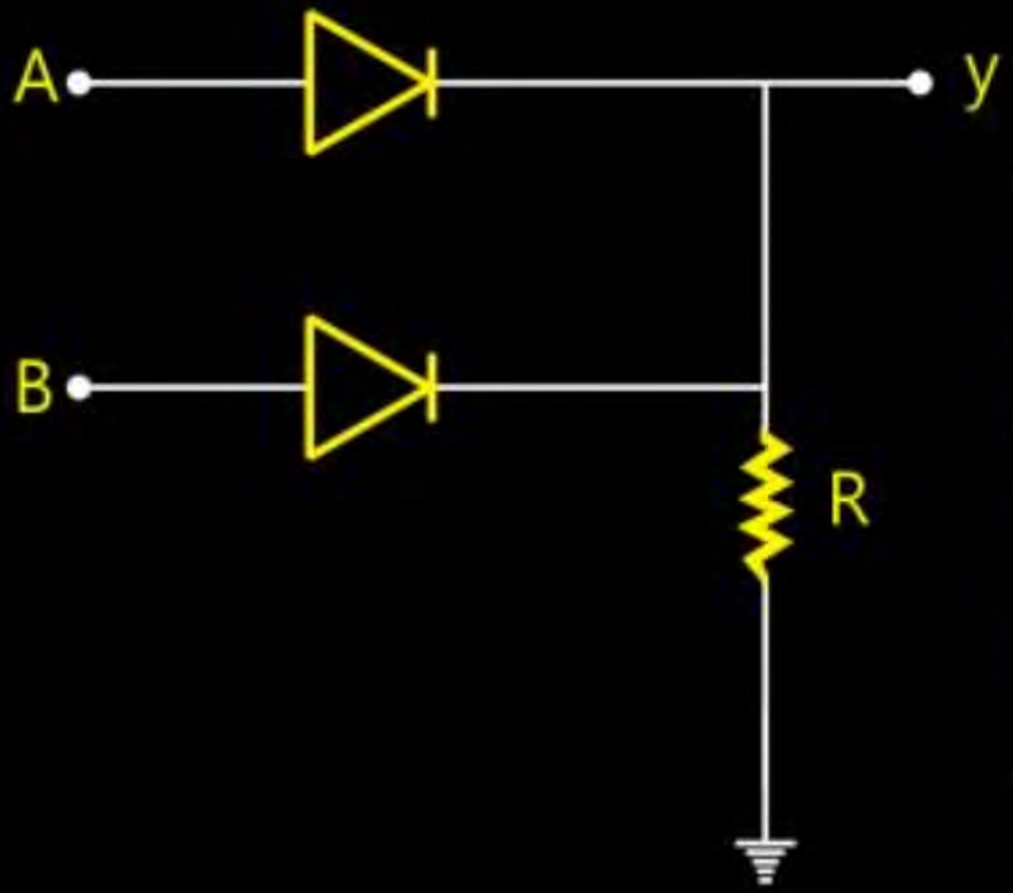

Vcc
A
A·B
B


R GATE


A
B
A+B

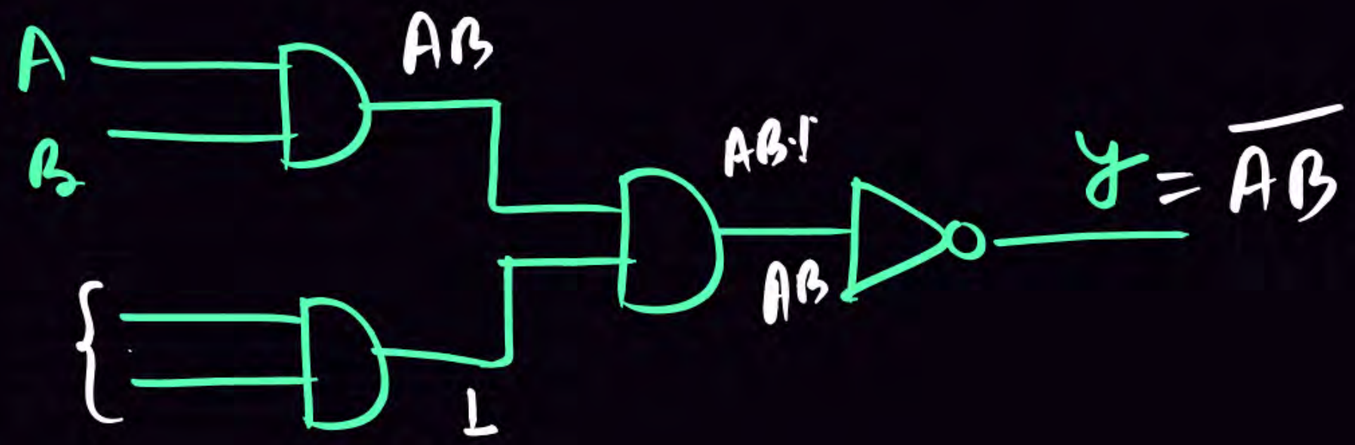
OR GATE

Circuit Diagram



A	B	D_A	D_B	y
0	0			
0	1			
1	0			
1	1			

If the Logics are designed by TTL, Then o/p will be -



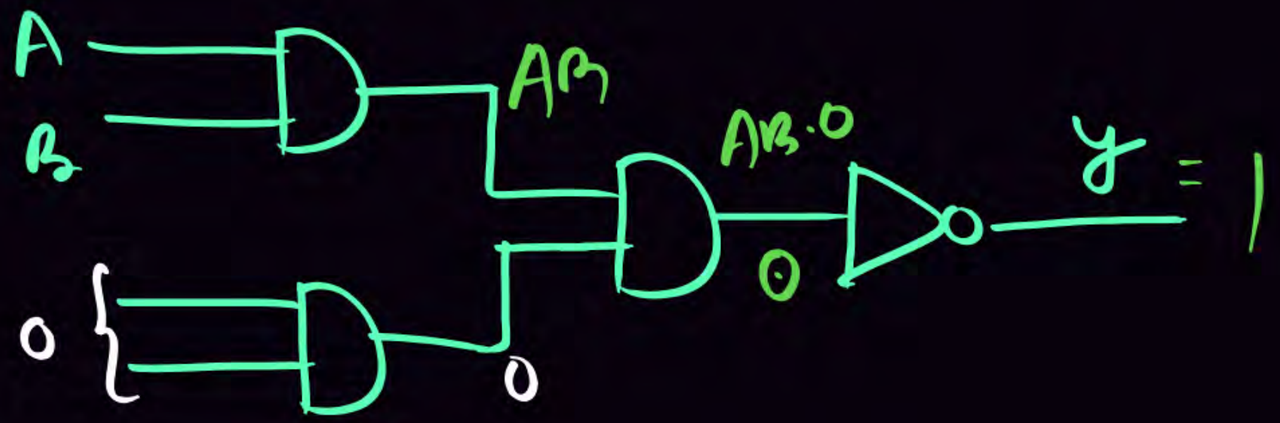
(A) A

(B) B

(C) AB

(D) $\overline{AB}$

If the Logics are designed by (ECU), Then o/p will be -



(A) 0

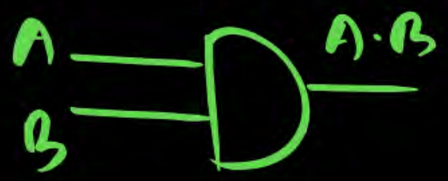
(B) 1

(C) $\overline{AB}$

(D) Mai Gajni hu.

AND & OR GATE

- **Discussion**



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

control '0' Disable

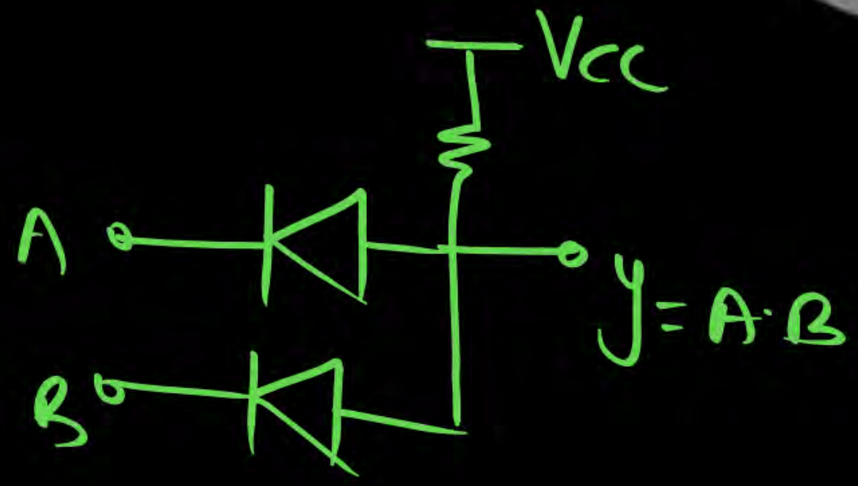
Control '1' Enable

commutative ✓

Associative ✓

TTL

floating terminal = 1



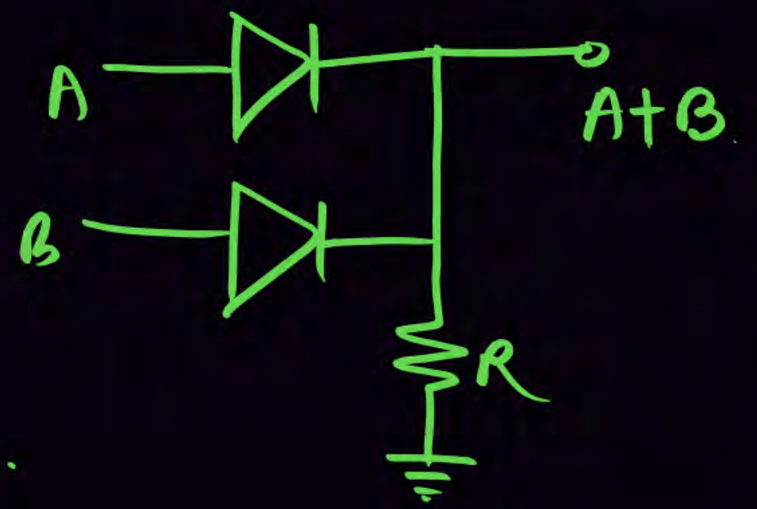
OR

A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

Control '0' Enable
Control '1' Disable.

Commutative Law ✓
Associative Law ✓

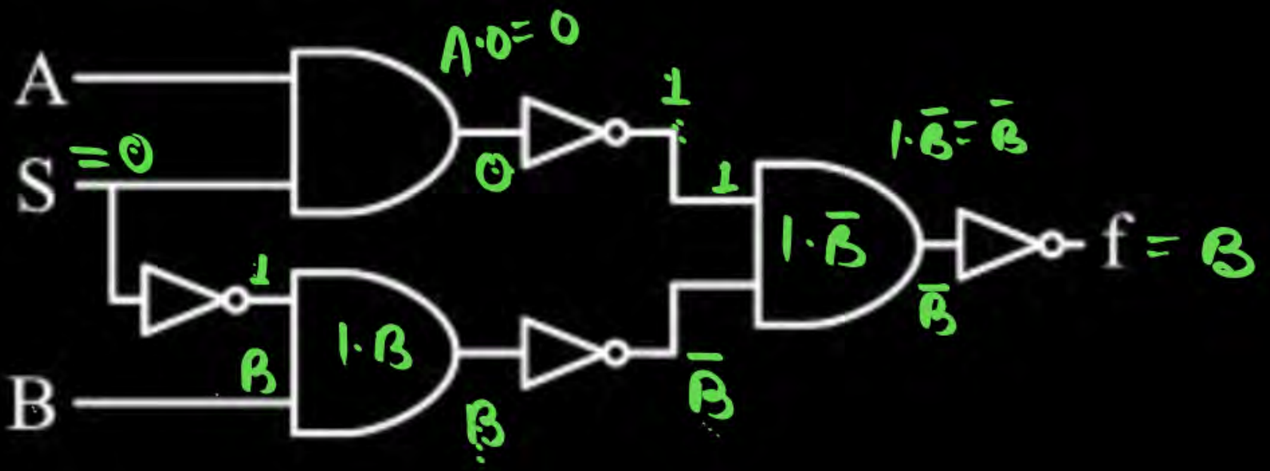
ECL → floating terminal → LOW.



Q.

MCQ

Output at S = 0 is



A. A

B. B

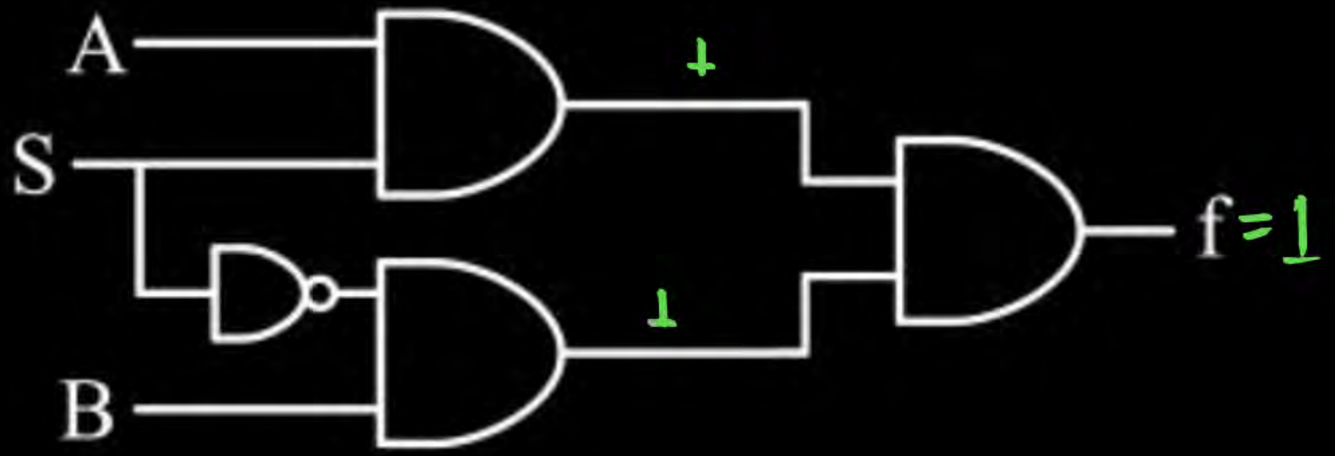
C. $\overline{A \cdot B}$

D. $\overline{A}B$

Q.

MCQ

f = 1 for combination of A, B , S



A. A = 0, B = 0, S = 0 ✗

B. A = 0, B = 1, S = 0 ✗

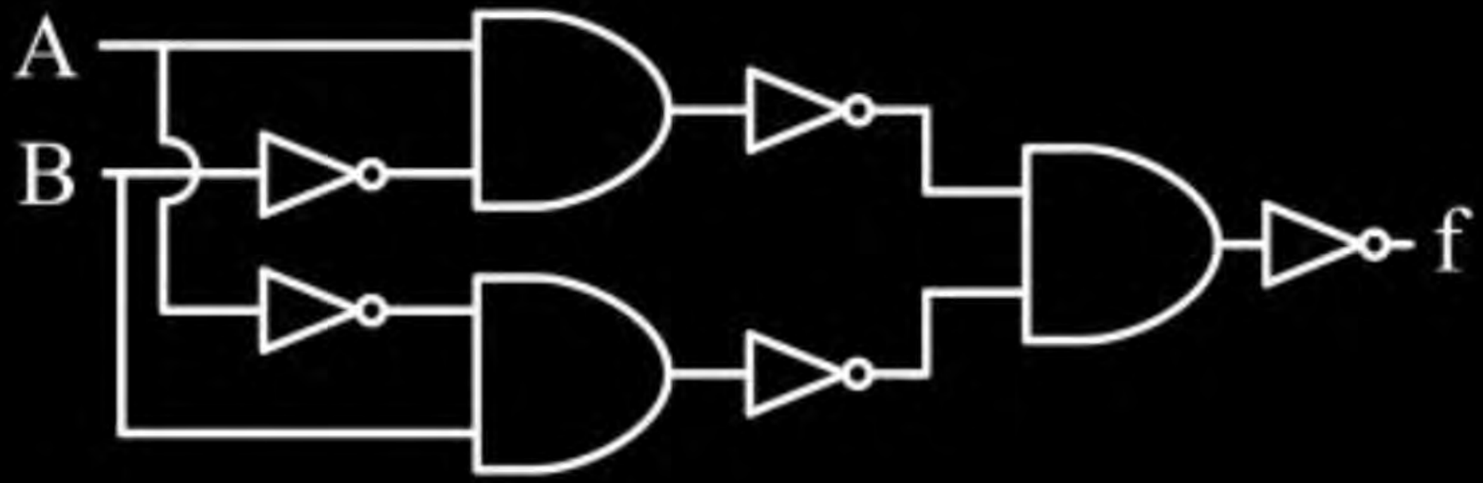
C. A = 1, B = 1, S = 0 ✗

D. None ✓

Q.

MCQ

f is an



A Equality Detector

B Inequality Detector

C All zero-input detector

D All one input detector

Q.

MCQ

$f = A + B$

For the given truth table

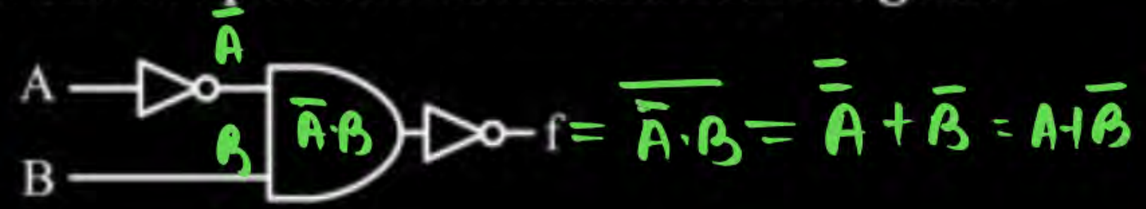
A	B	f
0	0	0
0	1	1
1	0	1
1	1	1

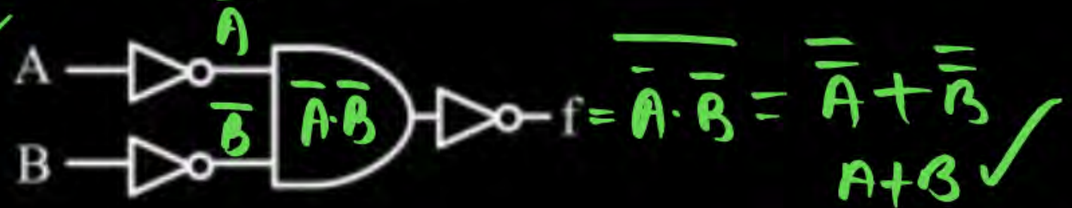
A- Morgan's Law

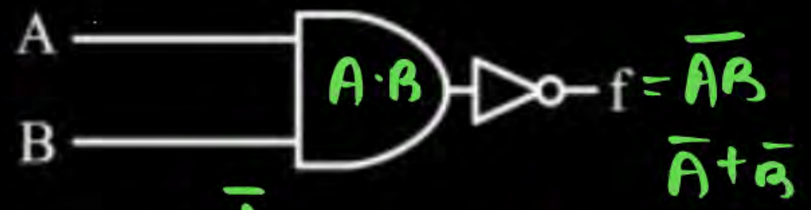
$\overline{AB} = \bar{A} + \bar{B}$

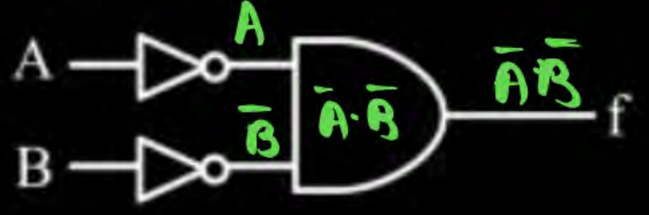
$\overline{A+B} = \bar{A} \cdot \bar{B}$

Select the respective combination diagram

(A) 

(B) 

(C) 

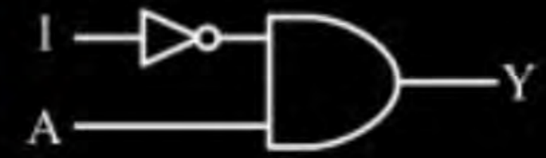
(D) 

Q.

HW.

MCQ

A logical circuit is as shown below, which of the following circuit can be used to get the desired expression.

A 

B 

C 

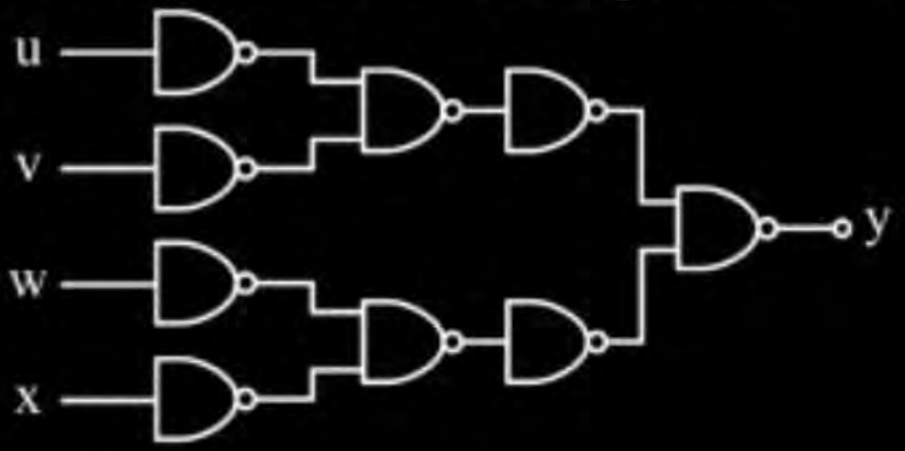
D 

Q.

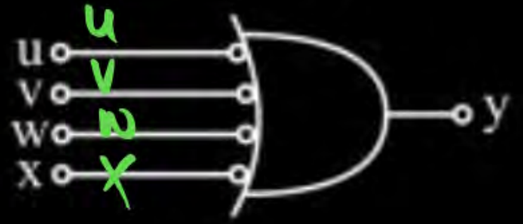
HW

MCQ

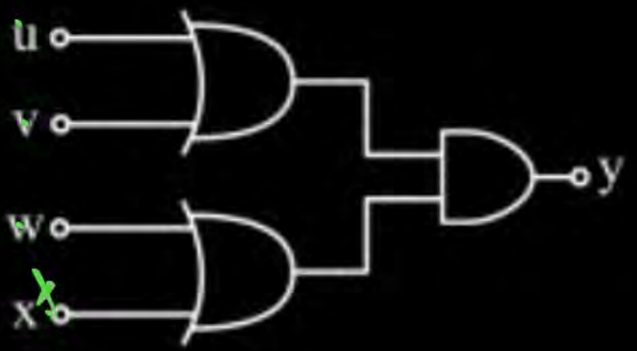
The logic circuit shown below, is equivalent to



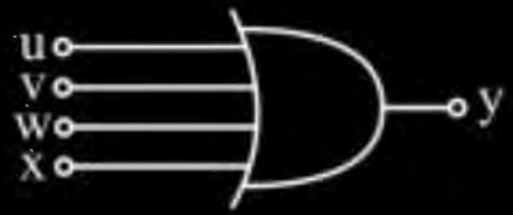
A



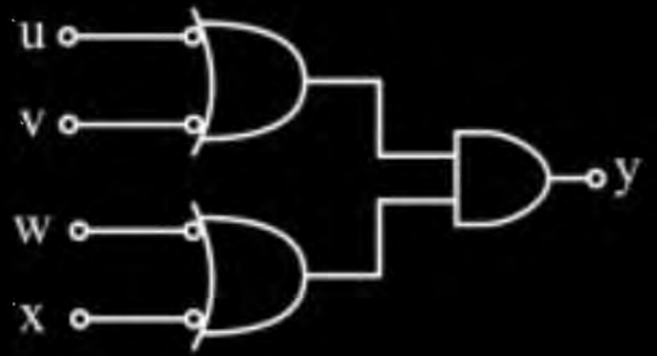
B



C



D



t.me/cjsir #GATE मतलब GATE WALLAHA.

Thank you GW Soldiers !