CS & IT ENGINEERING

DIGITAL LOGIC

Sequential Circuit

Lecture No. 05

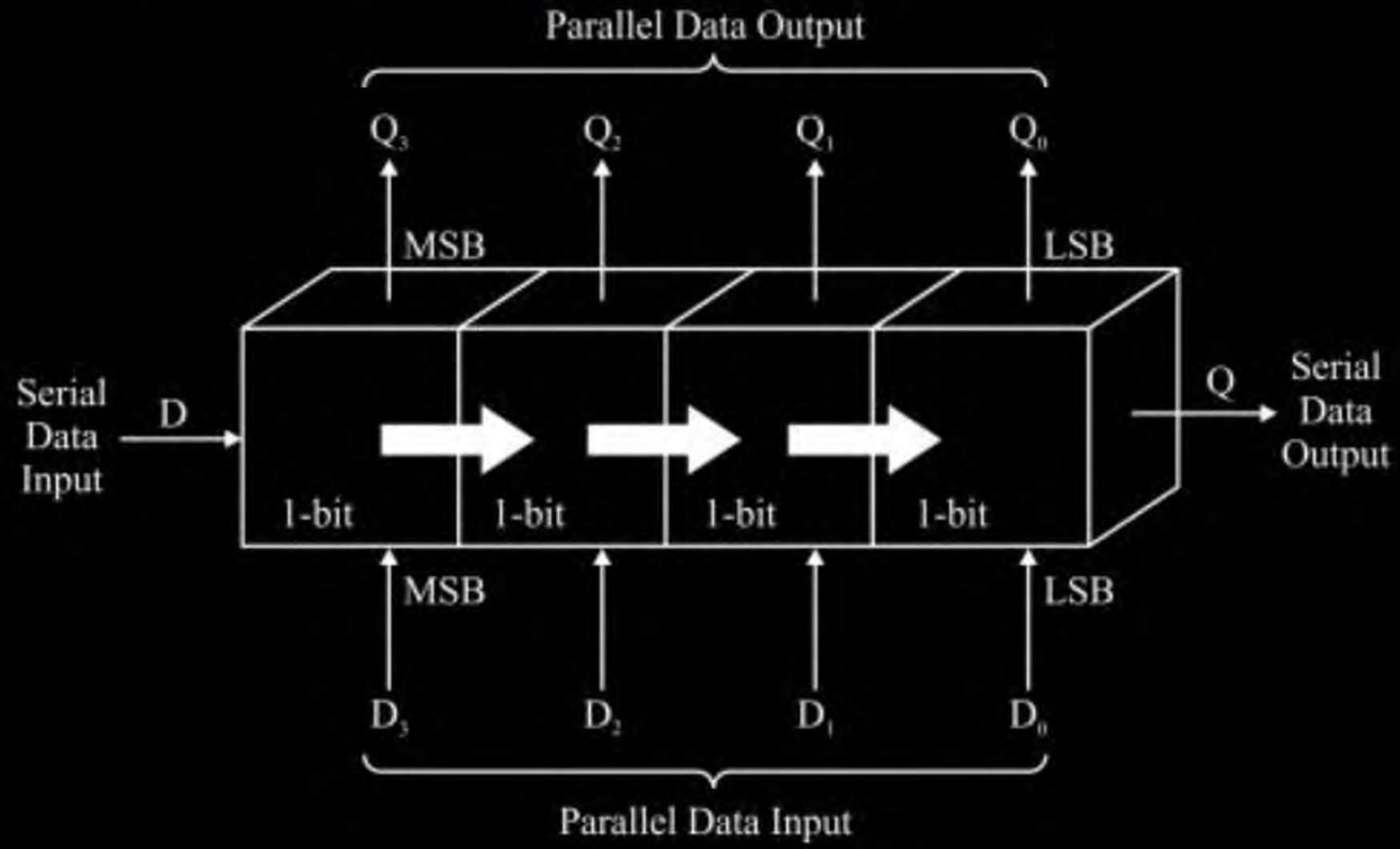
By- CHANDAN SIR

01 Registers, Basic of Counters

02 PRACTICE

03 DISCUSSION

SHIFT REGISTER



SHIFT REGISTER

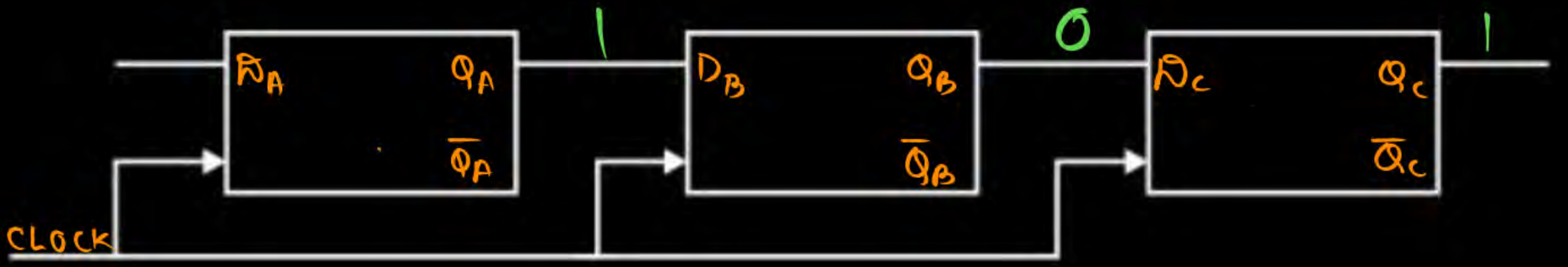
1. Registers are used to store group of bits
2. To store "n" bits minimum "n" Flip Flips are required
3. Generally D Flip Flops are used to Design Register

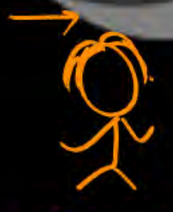
SHIFT REGISTER

1. Serial input serial output shift register [SISO]
2. Serial input parallel output shift register [SIPO]
3. Parallel input serial output shift register [PISO]
4. Parallel input parallel output shift register [PIPO]

SERIAL INPUT SERIAL OUTPUT (SISO) SHIFT REGISTER {3 bits}

Ankit sir





Bhabhi

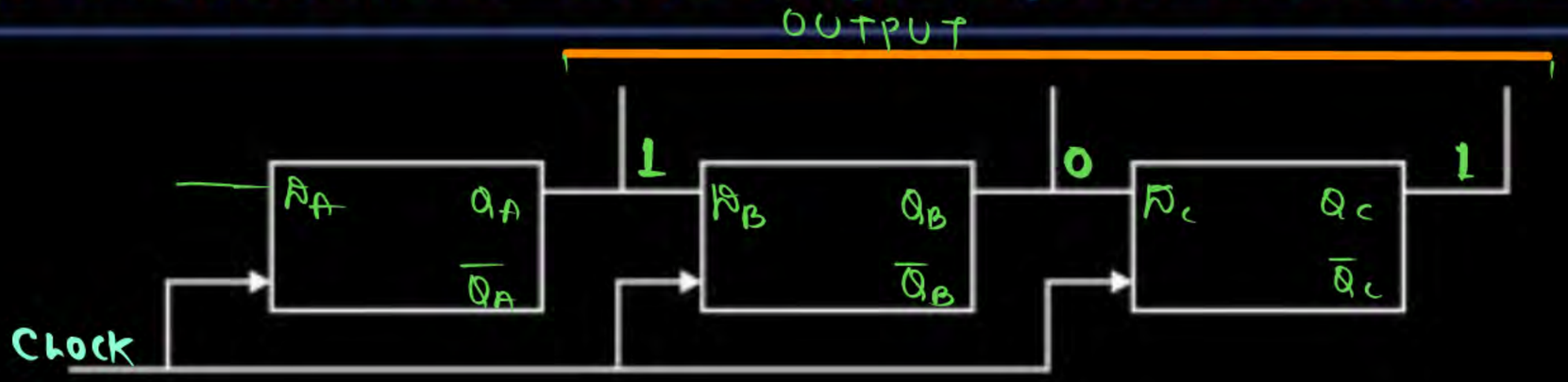
Clock	Input	Q_A	Q_B	Q_C
0	1 0 1	0	0	0
1		1	0	0
2		0	1	0
3		1	0	1

↳ To store "n" bits in "n" bit SISO minimum 'n' clocks are required.

↳ To Retrive 'n' bits from 'n' bit SISO minimum "n-1" clocks are required

↳ It is slowest shift Register among all the shift Register.

SERIAL INPUT PARALLEL OUTPUT (SIPO) SHIFT REGISTER

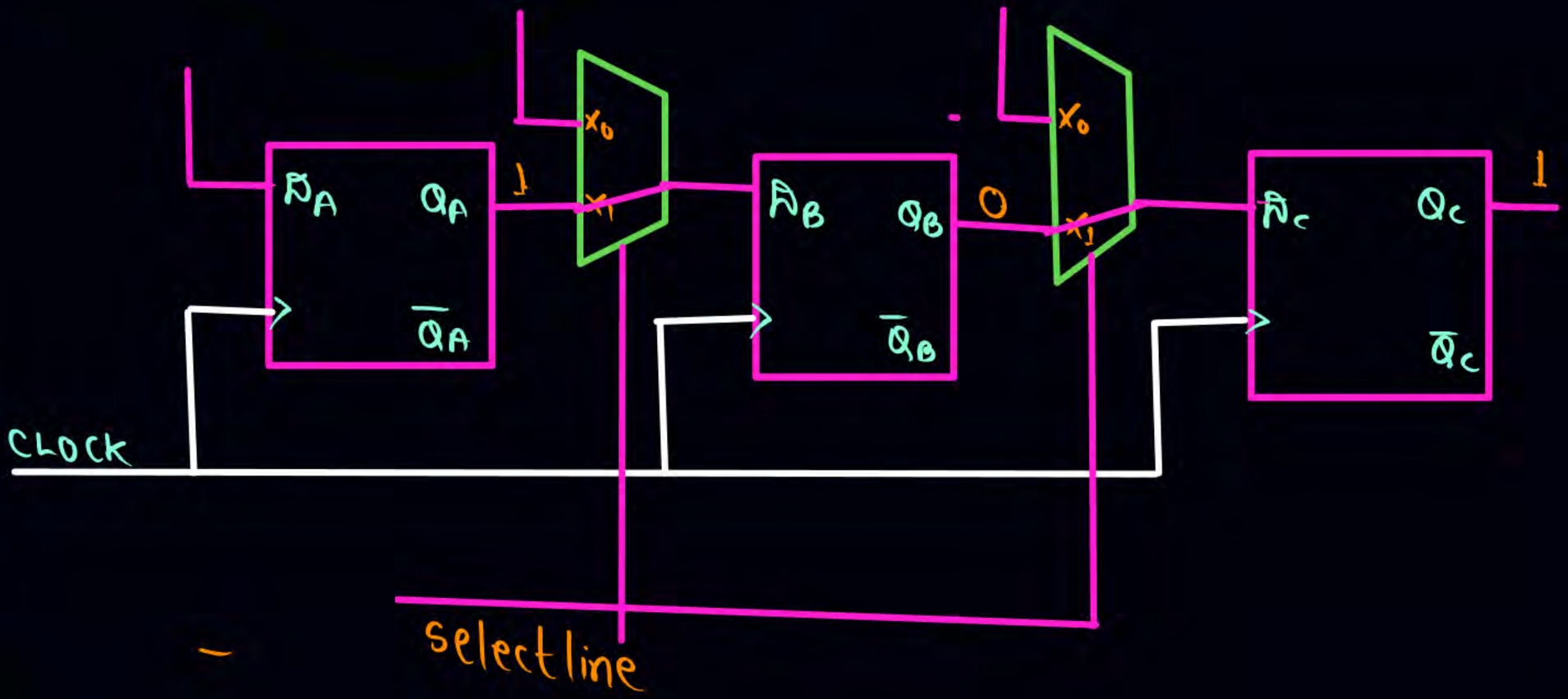


Clock	Input	Q_A	Q_B	Q_C
0				
1				
2				
3				

↳ To store 'n' bit in 'n' bit SIPO minimum 'n' clocks are required.

↳ To Retrive 'n' bits from 'n' bit SIPO no clock required.

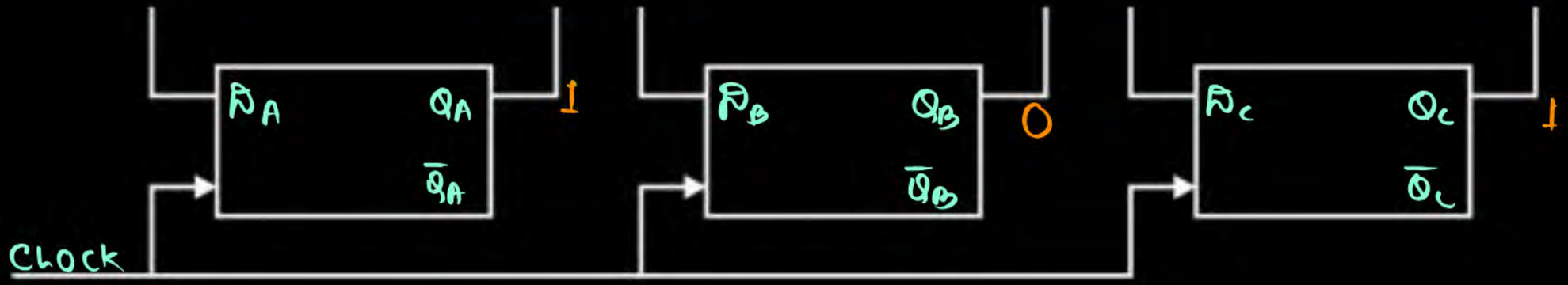
③ PISO SHIFT REGISTER



↳ To store 'n' bits in 'n' PISO only one clock is required.

↳ To Retrive 'n' bits from 'n' bit PISO minimum (n-1) clocks are required.

PARALLEL INPUT PARALLEL OUTPUT (PIPO) SHIFT REGISTER



Clock	Input	Q_A	Q_B	Q_C
0				
1				
2				
3				

↳ To store 'n' bit in 'n' bit PIPO only one clock is required.

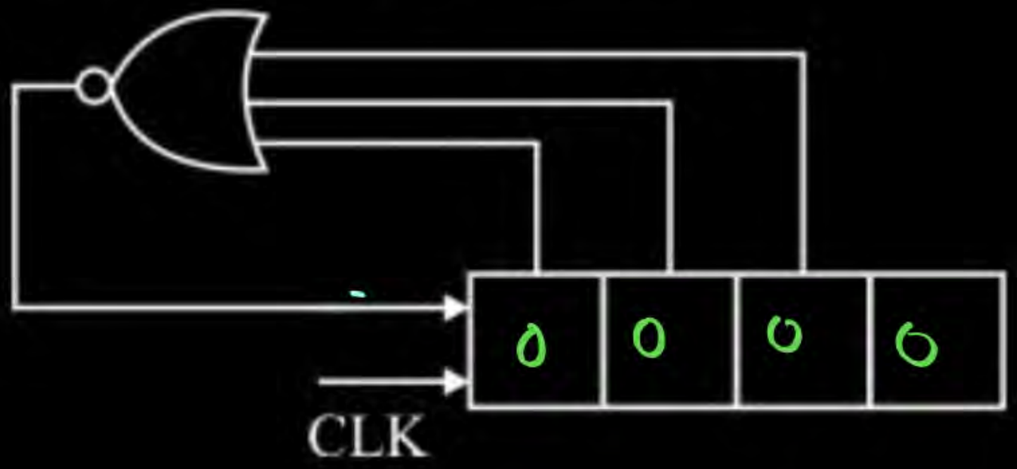
↳ There is no clock requirement in PIPO to retrive 'n' bits

↳ fastest shift Register among all the shift Register.

	Store	Retrive	Total	
SISO	n	n-1	2n-1	→ Slowest
SIPO	n	0	n	
PISO	1	n-1	n	
PIPO	1	0	1	→ Fastest

Q.

Write the state of the Register given below? (Assume initially all flips flops are reset)



Clock	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0
7	0	0	1	0
8	0	0	0	1
9				

What is output after 50th clock?

				Remainder
9	5	1	1000	1
10	6	2	0100	2
11	7	3	0010	3
12	8	4	0001	0

$\frac{50}{4}$ R = 2

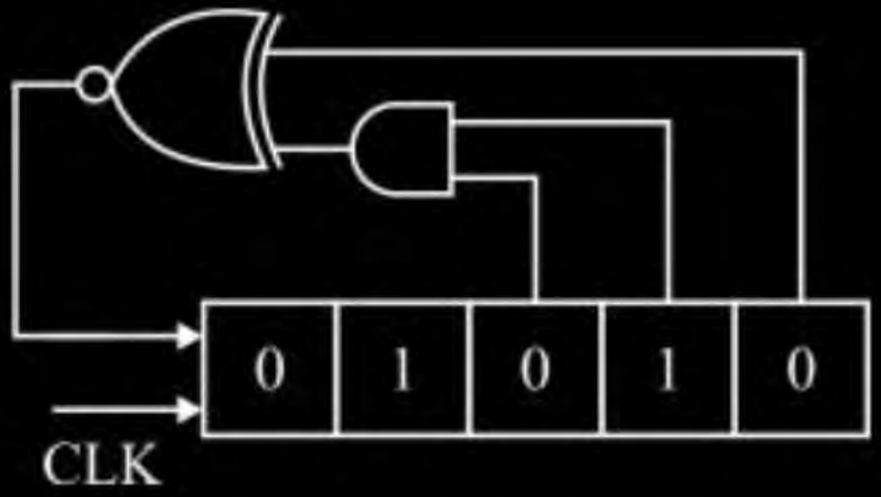
Ans = 0100

Ans

Q.

HW.

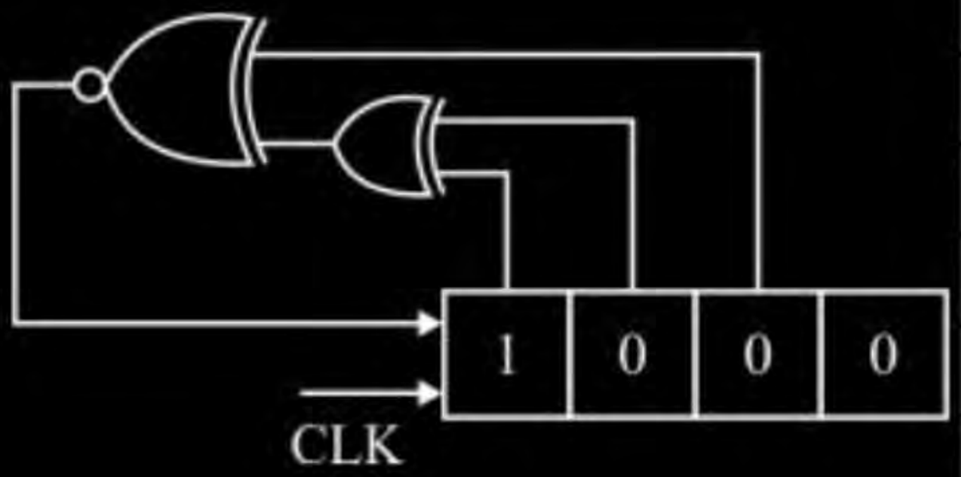
After 137^{th} clock the output will be?



Clock	Q_4	Q_3	Q_2	Q_1	Q_0
0	0	1	0	1	0
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

Q. HW

After 97th clock the output will be?



Clock	Q_3	Q_2	Q_1	Q_0
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				

THANK YOU

DOSTO