CS & IT ENGINEERING

Digital Logic

Sequential Circuit

Lecture No. 12

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01 Synchronous Counter Design

02 Practice

03 Discussion

DESIGNING OF SYNCHRONOUS COUNTER

STEP 1. Write the Previous and Present State.

STEP 2. Write the Excitation Table of FF.

STEP 3. Write the Logical Expression.

STEP 4. Minimize the Logical expression.

STEP 5. Hardware Implementation.

Q.

Design a Synchronous Counter by using T Flip Flop which count the sequence $0 \rightarrow 2 \rightarrow 3 \rightarrow 0$

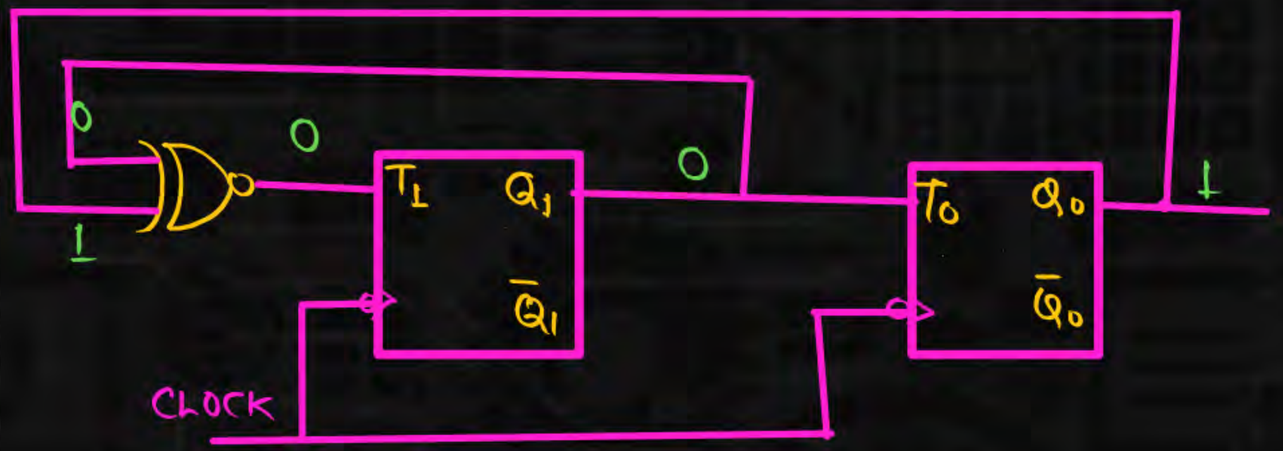
$00 \rightarrow 10 \rightarrow 11 \rightarrow 00$

2 bits

→ 2 FF's are required

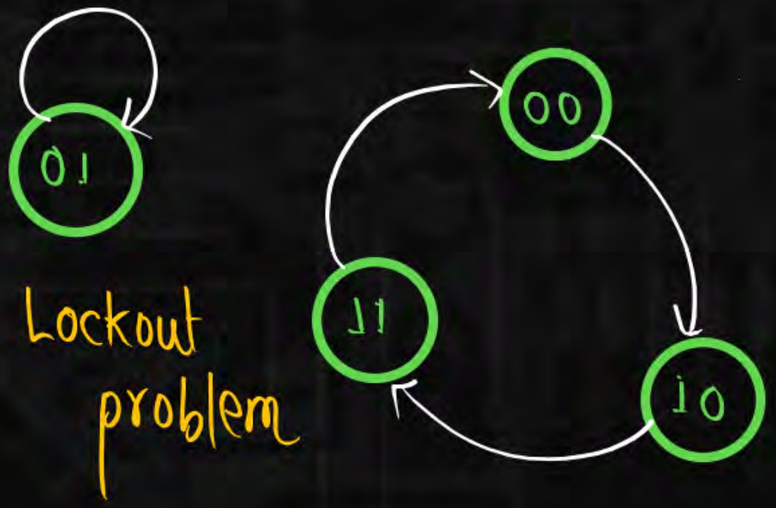
Method -1

Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	1



$$T_1 = Q_1 \odot Q_0$$

$$T_0 = Q_1$$

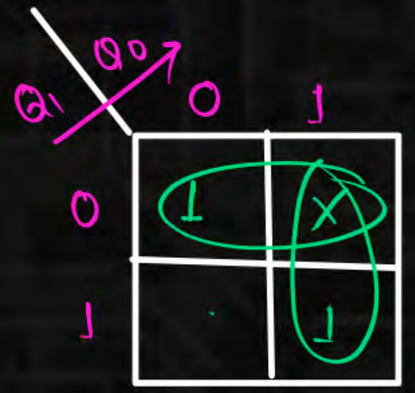


Lockout problem

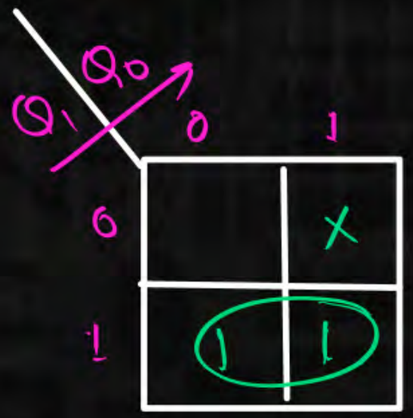
Clock	Q_1 Q_0
0	0 0
1	1 0
2	1 1
3	0 0

Method -2

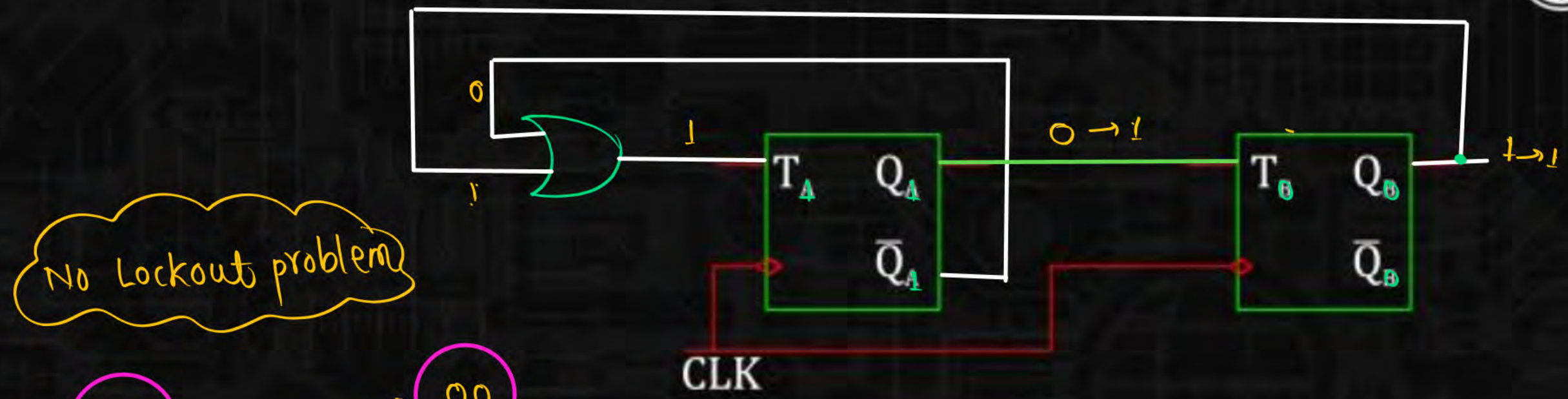
Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	1	0	1	0
0	1	X	X	X	X
1	0	1	1	0	1
1	1	0	0	1	1



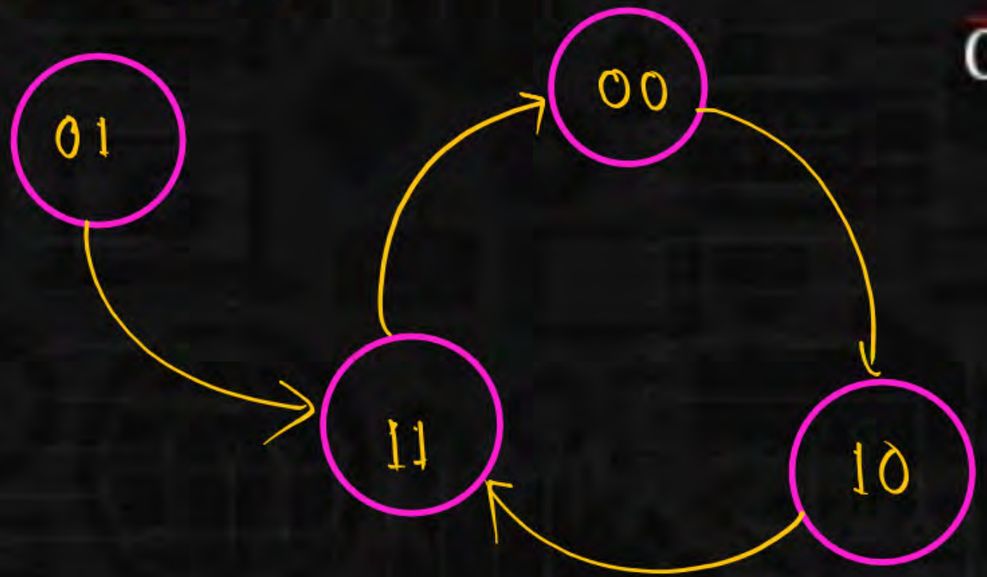
$$T_1 = \bar{Q}_1 + Q_0$$



$$T_0 = Q_1$$



No Lockout problem



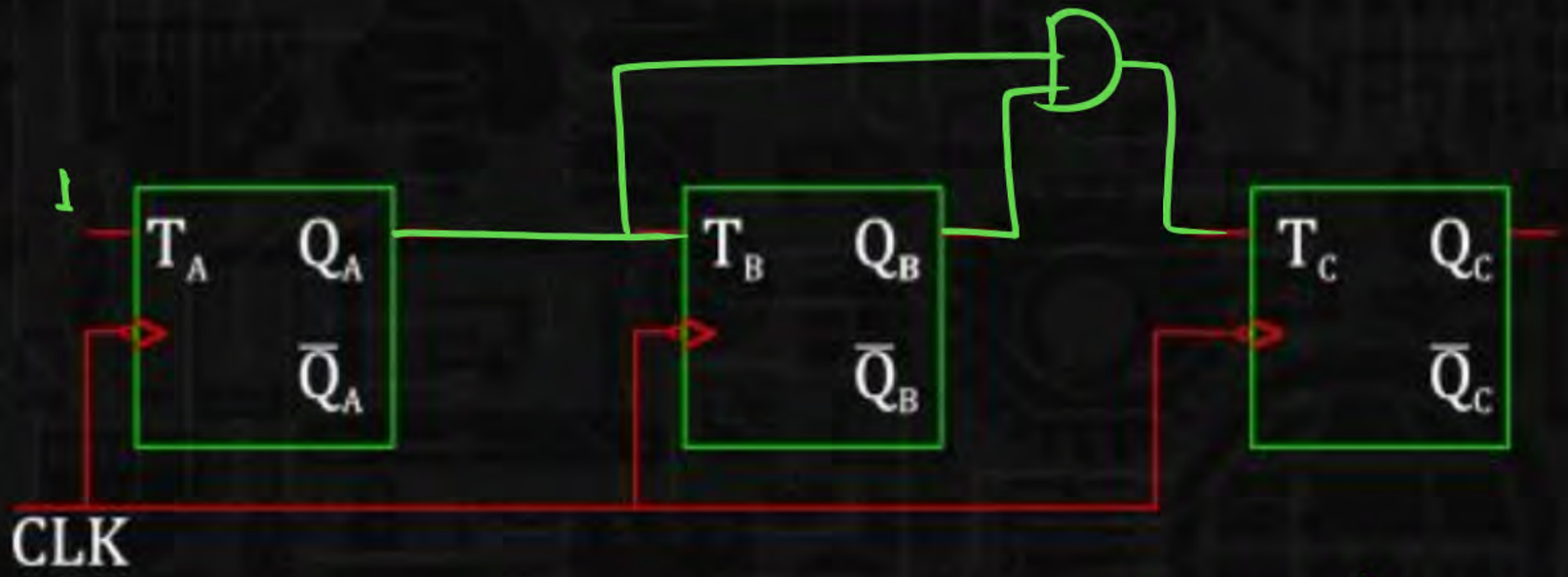
Q.

Design a Synchronous Counter by using T Flip Flop which count the sequence $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 0$

$T_A = 1$

$T_B = Q_A$

$T_C = Q_A \cdot Q_B$



$$T = T_{pd_{ff}} + T_{pd_{AND}}$$

$$T_{clk} \geq T_{pd_{ff}} + T_{pd_{AND}}$$

$$\frac{1}{T_{clk}} \leq \frac{1}{T_{pd_{ff}} + T_{pd_{AND}}}$$

$$f_{clk} \leq \frac{1}{T_{pd_{ff}} + T_{pd_{AND}}}$$

$$(f_{clk})_{max} = \frac{1}{T_{pd_{ff}} + T_{pd_{AND}}}$$

4 bit

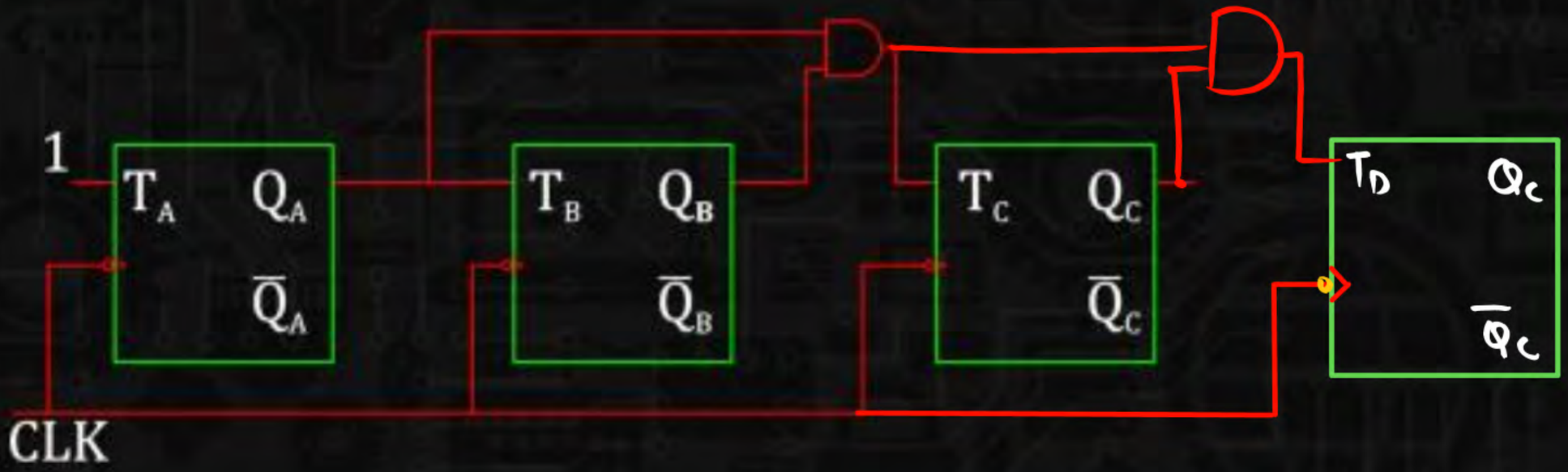
$T_A = 1$

$T_B = Q_A$

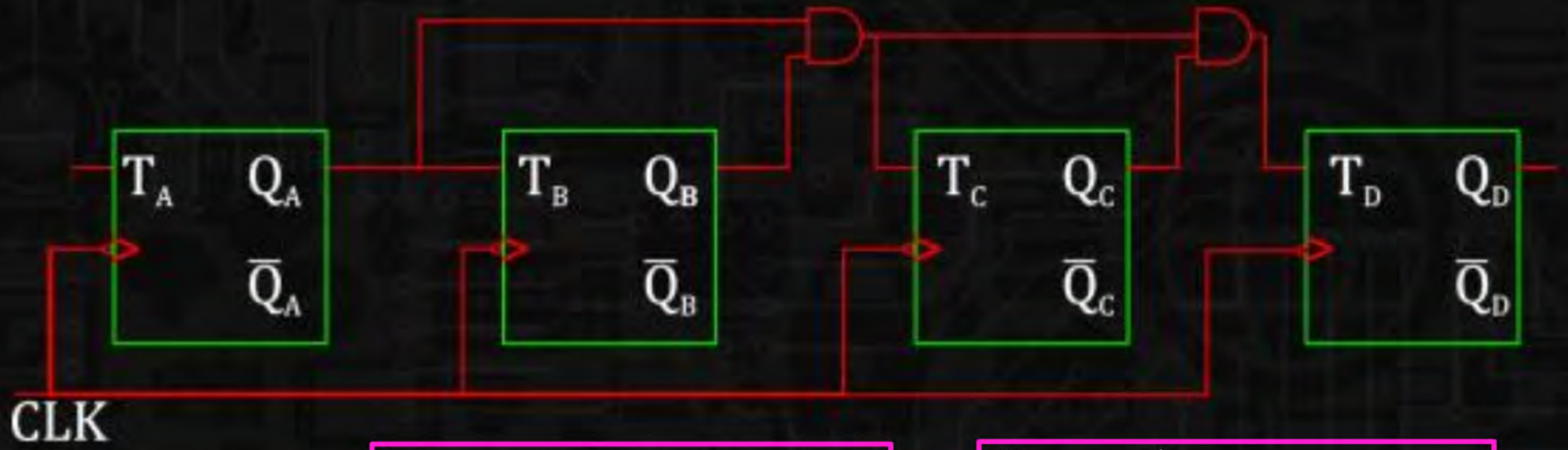
$T_C = Q_A \cdot Q_B$

$T_D = Q_A \cdot Q_B \cdot Q_C$

SERIES CARRY SYNCHRONOUS COUNTER



SERIES CARRY SYNCHRONOUS COUNTER



$$T_{clk} \geq T_{pd_{ff}} + 2 \cdot T_{pd_{AND}}$$

$$f_{clk} \leq \frac{1}{T_{pd_{ff}} + 2 \cdot T_{pd_{AND}}}$$

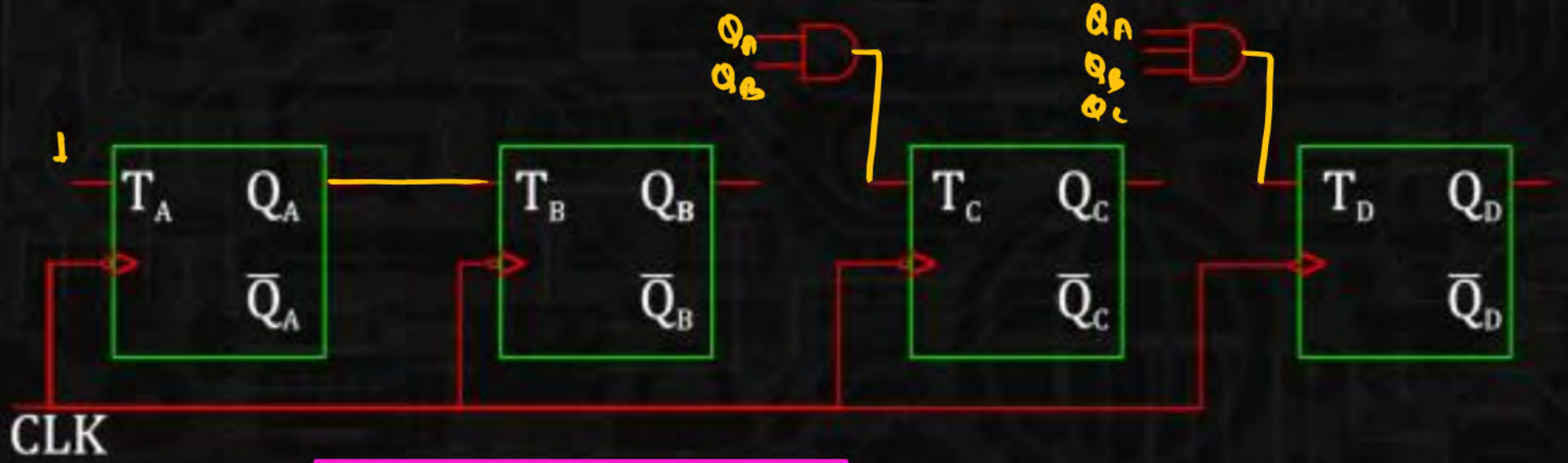
SERIES CARRY SYCHRONOUS COUNTER

$$T_{CLK} \geq T_{Pd_{ff}} + (N-2)T_{Pd_{AND}}$$

N → No. of bits

$$f_{CLK} \leq \frac{1}{T_{Pd_{ff}} + (N-2)T_{Pd_{AND}}}$$

PARALLEL CARRY SYNCHRONOUS COUNTER



$$T_{clk} \geq T_{pd_{ff}} + T_{pd_{AND}}$$

$$f_{clk} \leq \frac{1}{T_{pd_{ff}} + T_{pd_{AND}}}$$

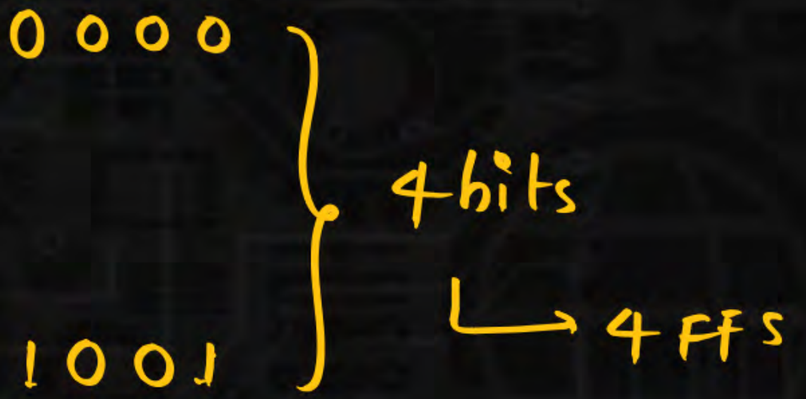
Q. Minimum number of flip flops required to construct BCD counter is

A. 4

B. 3

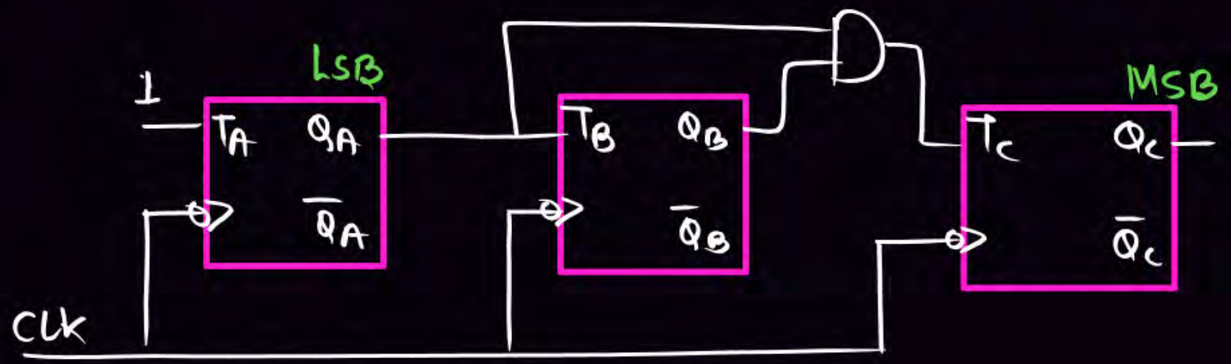
C. 1

D. 5



Q Minimum no. of FF required to design counter state given below.

$0 \to 0 \to 1 \to 1 \to 2 \to 2 \to 3 \to 3 \to 0 \to 0 \to \cdots$



Q_C	Q_B	Q_A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0
0	0	1

3 bit synchronous up counter

3-FF required

Q.

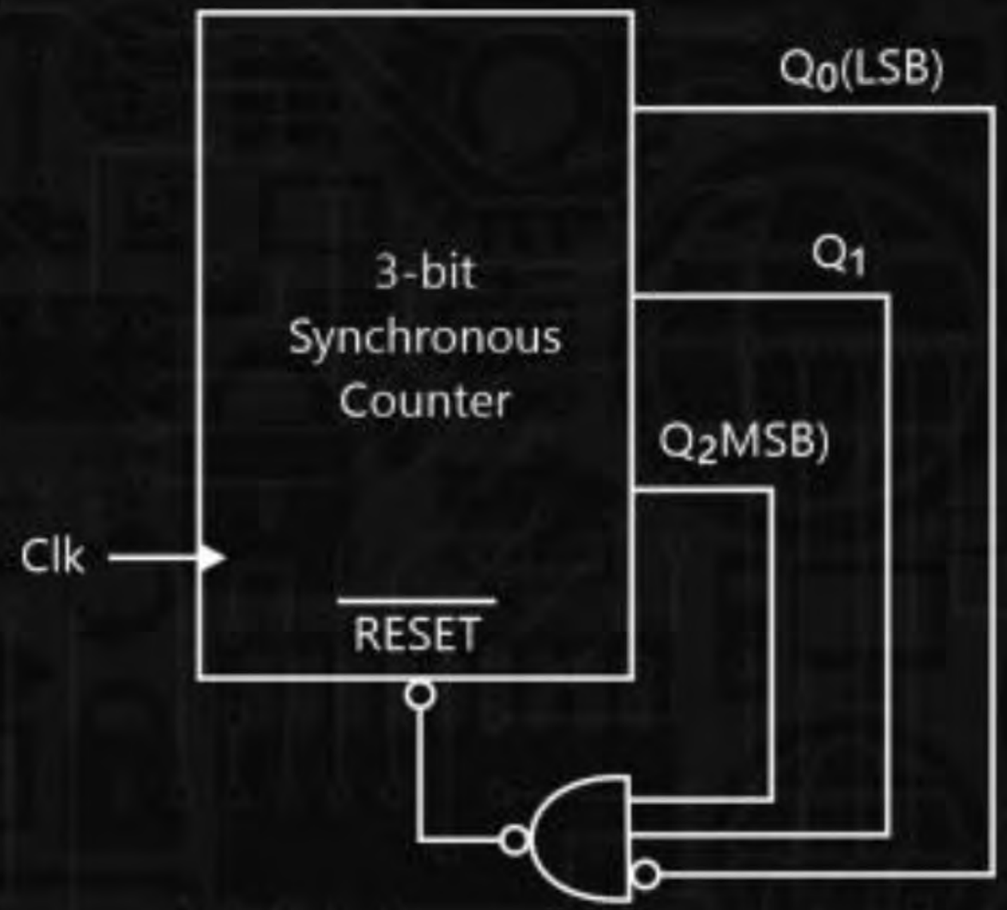
What is the MOD of the counter

A. mod-5 counter

B. mod-6 counter

C. mod-7 counter

D. mod-8 counter



Q.

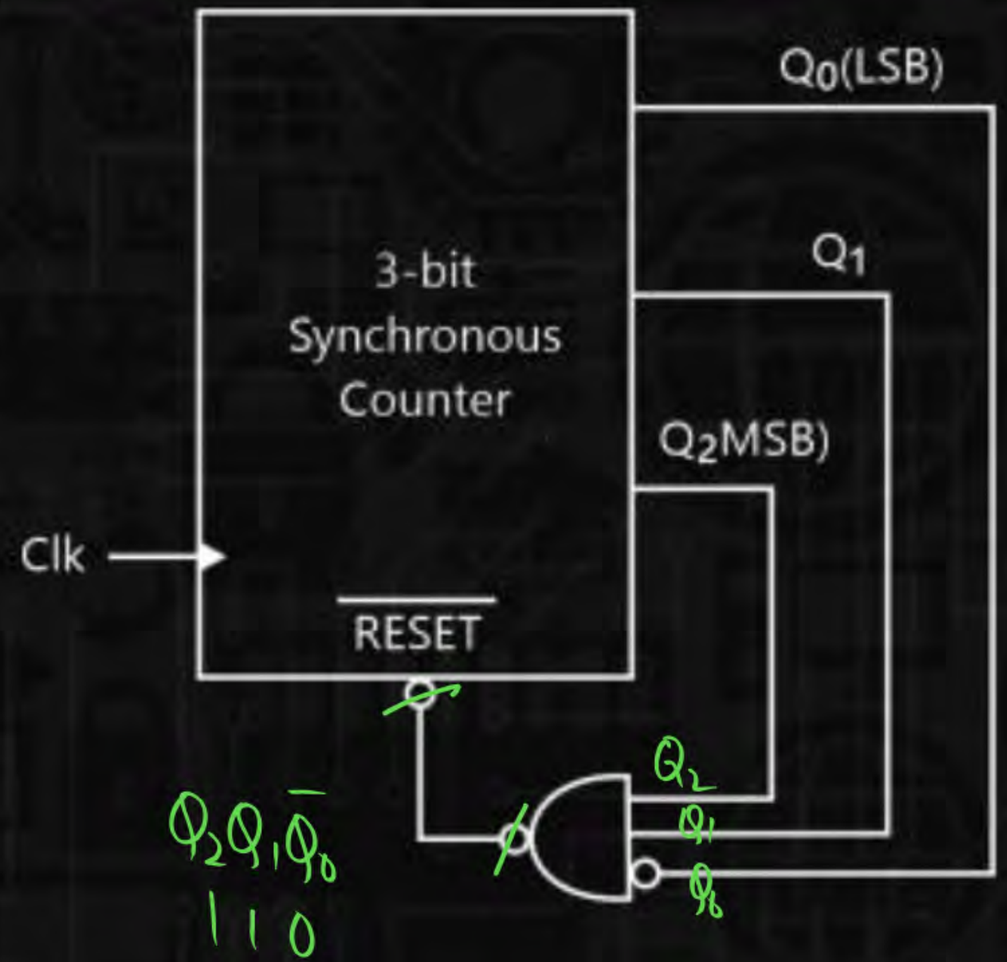
$Q_2Q_1Q_0$

0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1
1 1 0
0 0 0

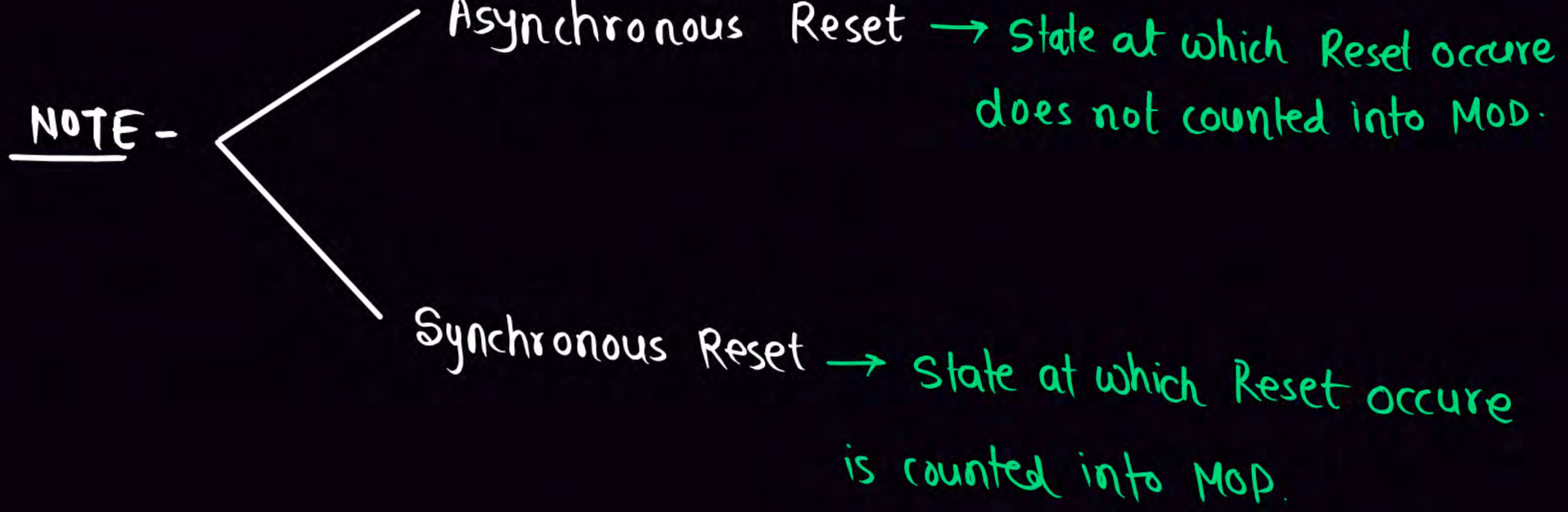
1 1 0 → 6
Reset

0 → 1 → 2 → 3 → 4 → 5 → 6

MOD = 7



$Q_2Q_1\bar{Q}_0$
1 1 0


NOTE -
Asynchronous Reset → State at which Reset occure does not counted into MOD.
Synchronous Reset → State at which Reset occure is counted into MOD.

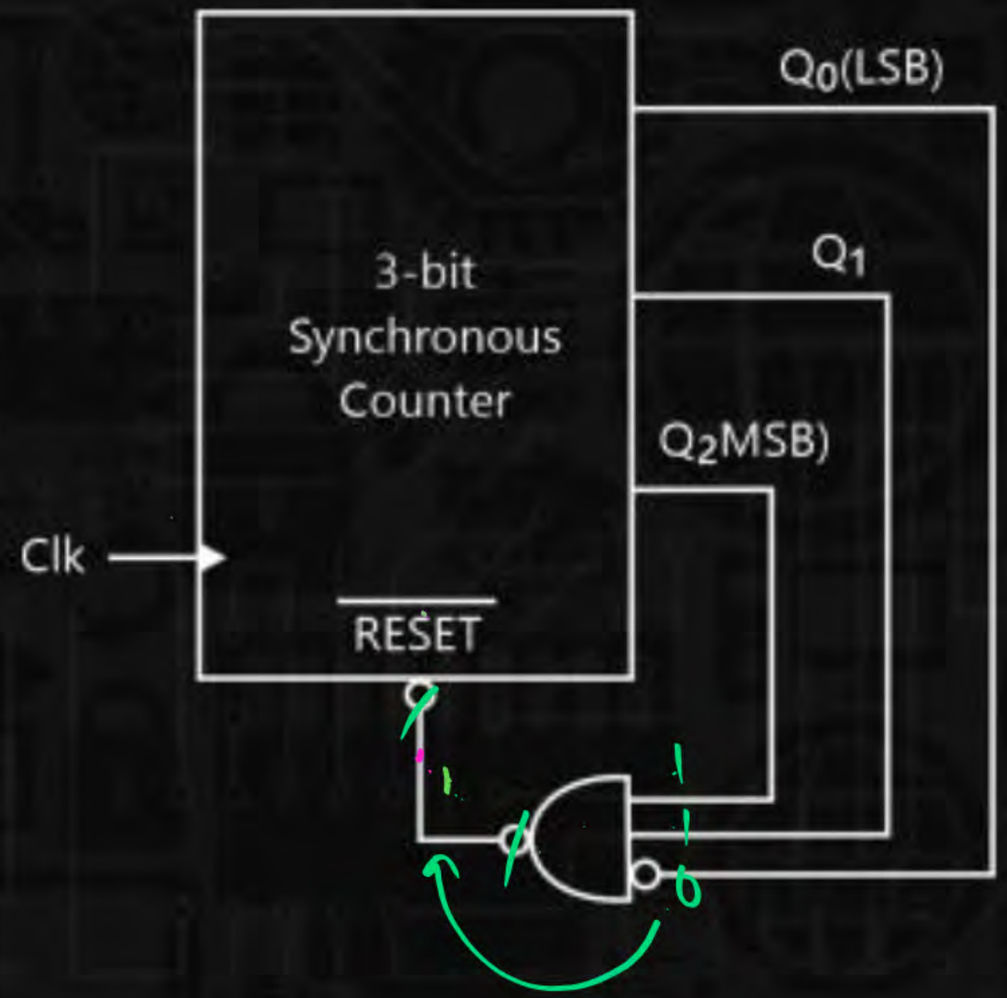
Q. For the circuit shown in the figure, the delay of the bubbled NAND gate is 2 ns and that of the counter is assumed to be zero. If the clock (Clk) frequency is 1 GHz, then the counter behaves as a

A. mod-5 counter

B. mod-6 counter

C. mod-7 counter

D. mod-8 counter



$T_{CLK} = \frac{1}{f_{CLK}} = \frac{1}{1 \times 10^9}$

$= 1ns$

Q.

Consider the below circuit:

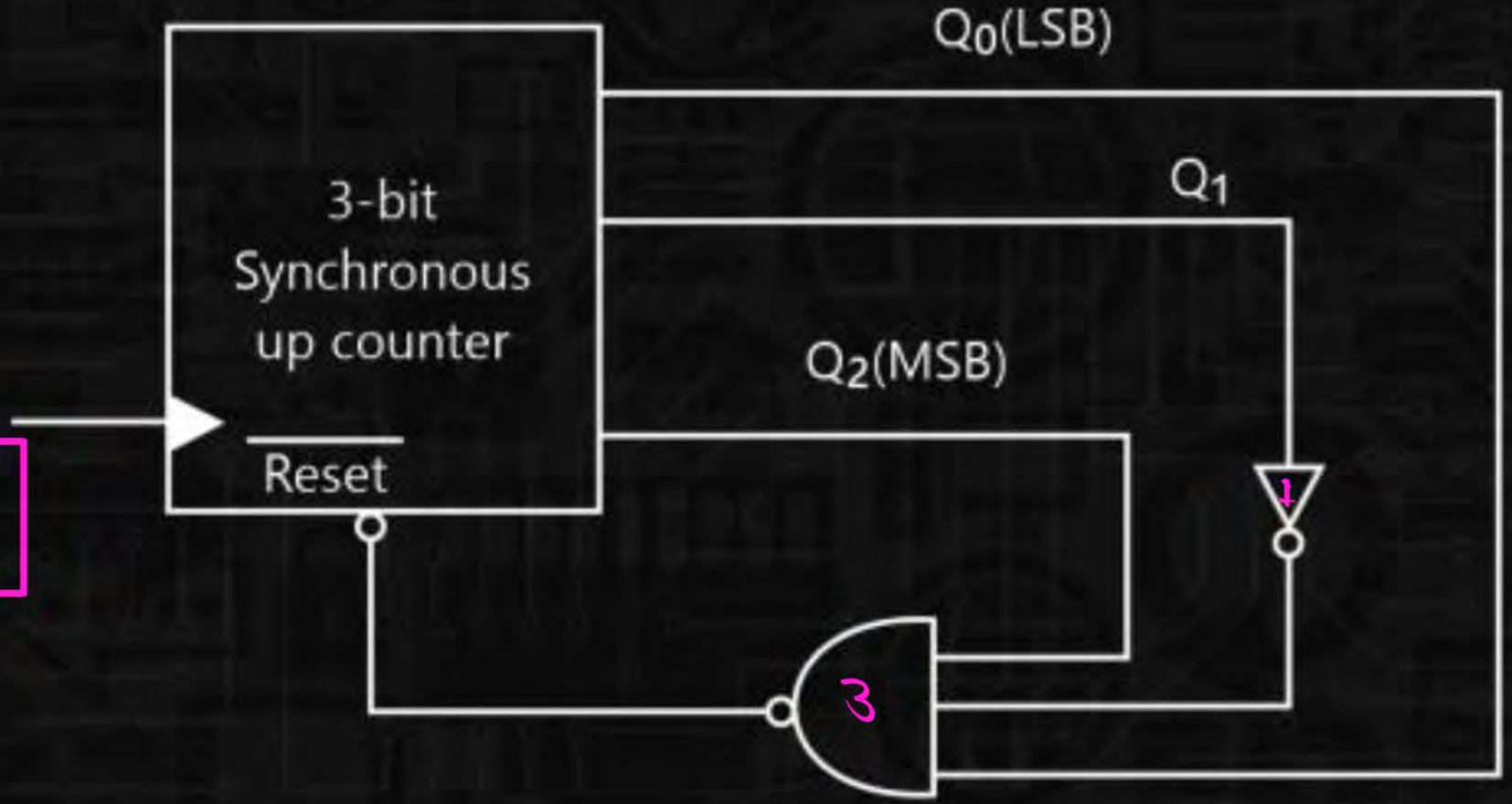
The delay of NAND, NOT gate is 3 ns, 1 ns respectively and that of the counter is assumed to be zero. If the clock frequency is 500 MHz, then the counter behaves as a

A. mod-5 counter

B. mod-6 counter

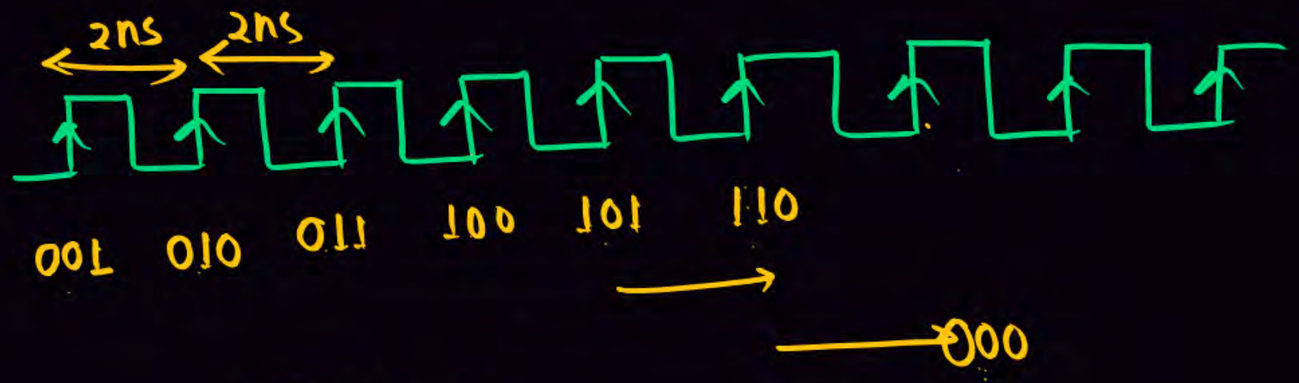
C. mod-7 counter

D. mod-8 counter



1 0 1

$Clr = Q_2 \bar{Q}_1 Q_0$



MOD = 7

$f_{Clk} = 500 \times 10^6$ Hz

$T_{Clk} = \frac{1}{500 \times 10^6}$ sec.

$= \frac{1}{500} \times 10^{-9}$

$= 2$ ns sec.

Q.

Consider the circuit below with initial state $Q_0 = 1$, $Q_1 = Q_2 = 0$.

The state of the circuit is given by the value of $4Q_2 + 2Q_1 + Q_0$

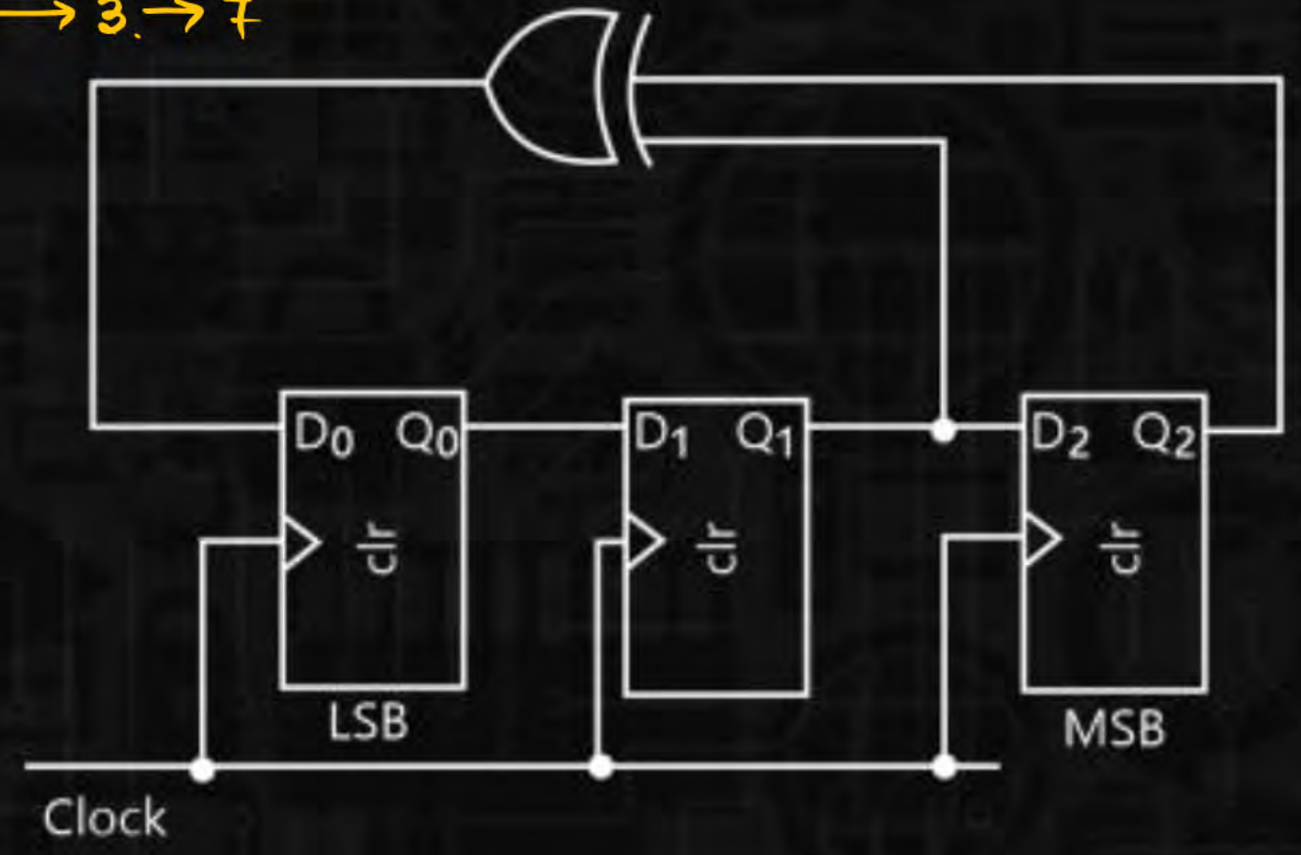
Which one of the following is the correct state sequence of the circuit? $1 \rightarrow 2 \rightarrow 5 \rightarrow 3 \rightarrow 7$

A. 1,3,4,6,7,5,2

B. 1,2,5,3,7,6,4

C. 1,2,7,3,5,6,4

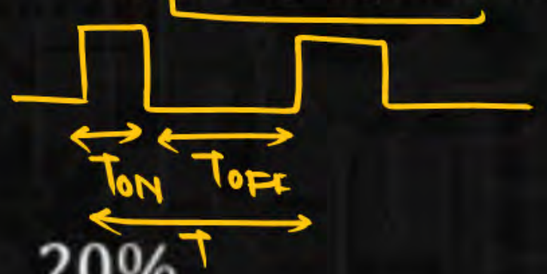
D. 1,6,5,7,2,3,4



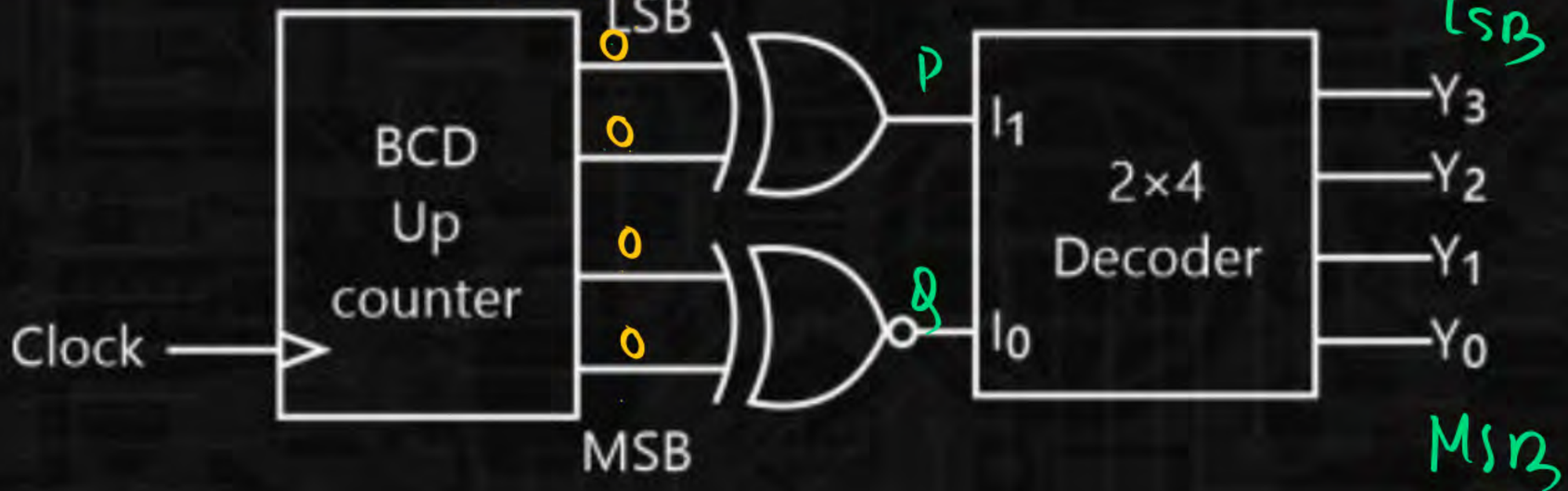
Q.

Consider the circuit given below.

The duty cycle of Y_2 is



Duty cycle = $\frac{T_{ON}}{T_{ON}+T_{OFF}} \times 100$



A. 20%

B. 40%

C. 30% ✓

D. 25%

C⊕Q A⊙B

A	B	C	D	P	Q	y_0	y_1	y_2	y_3
0	0	0	0	0	1	0	1	0	0
0	0	0	1	1	1	0	0	0	1
0	0	1	0	1	1	0	0	0	1
0	0	1	1	0	1	0	1	0	0
0	1	0	0	0	0	1	0	0	0
0	1	0	1	1	0	0	0	1	0
0	1	1	0	1	0	0	0	1	0
0	1	1	1	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0
1	0	0	1	1	0	0	0	1	0

y_2

$T = T_{ON} \rightarrow$ Total time

$37 = T_{ON}$

$$D = \frac{T_{ON}}{T} \times 100$$

$$= \frac{37}{107} \times 100$$

$= 30\%$


THANK YOU
DOSTO !