CS & IT



ENGINEERING



Combinational Circuit

Lecture No. 8



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TOPICS TO BE COVERED 01 HA

02 FA

03 HS

04 FS

05 Discussion



HALF ADDER

Two bit adder are known as half adder.



Step 1.





Sum= AB+AB

-AAR

Step 2.

A	В	Sum	Carry
0	0	0	0
0	1	1	0.
1	0	1	0
1	1	0	1



HALF ADDER

Step 3.

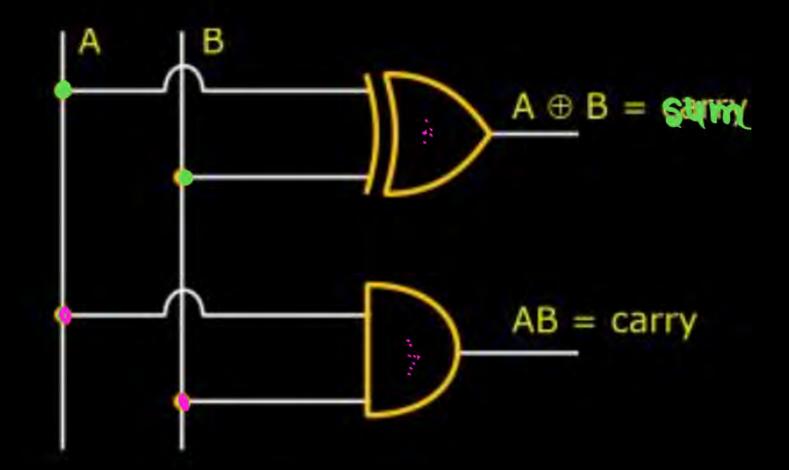
$$sum = \overline{AB} + A\overline{B} = A \oplus B$$
$$carry = AB$$

Step 4. Minimization

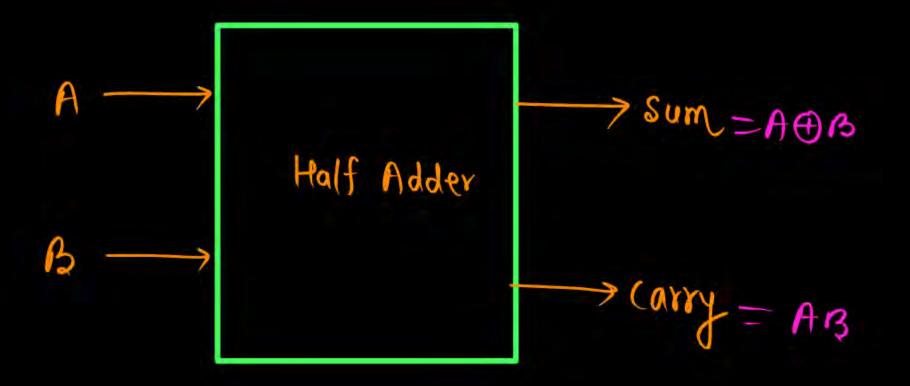


HALF ADDER

Step 5.



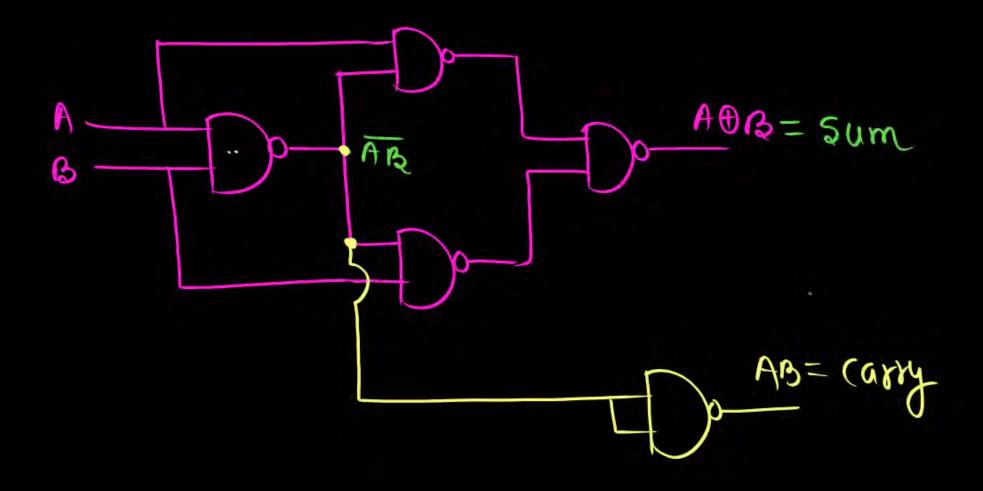






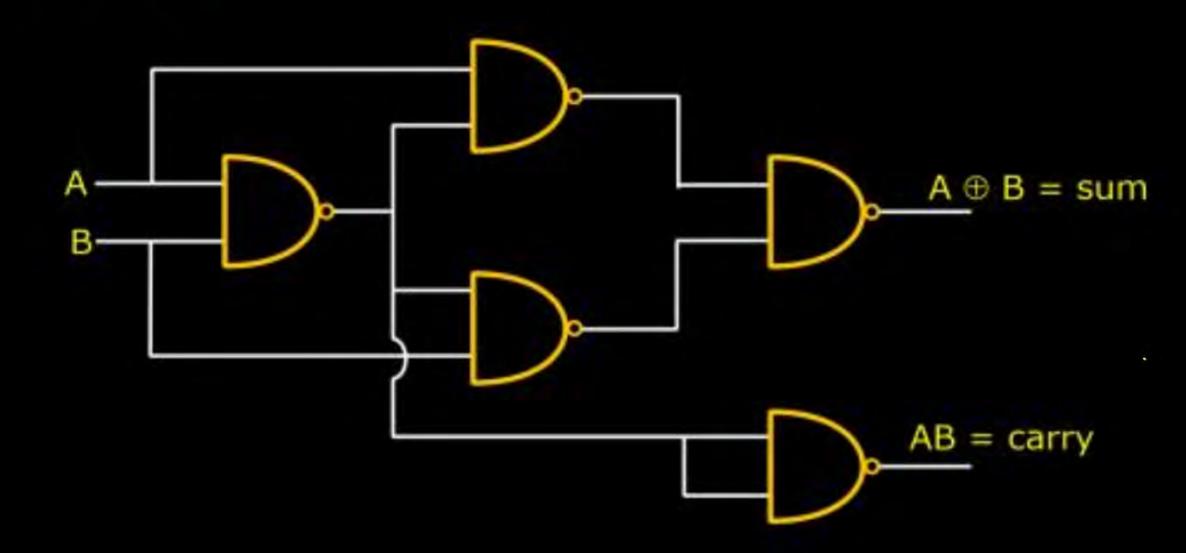
HA

NAND = 5

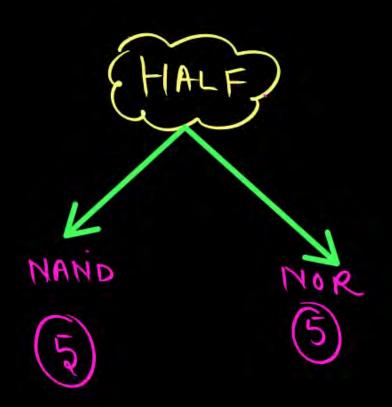


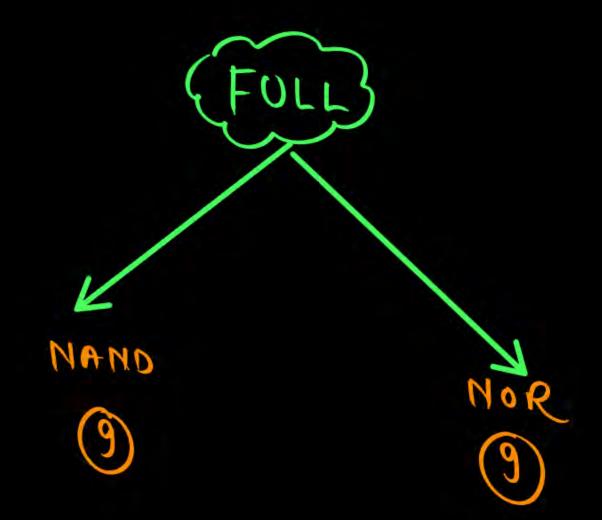


By NAND GATE









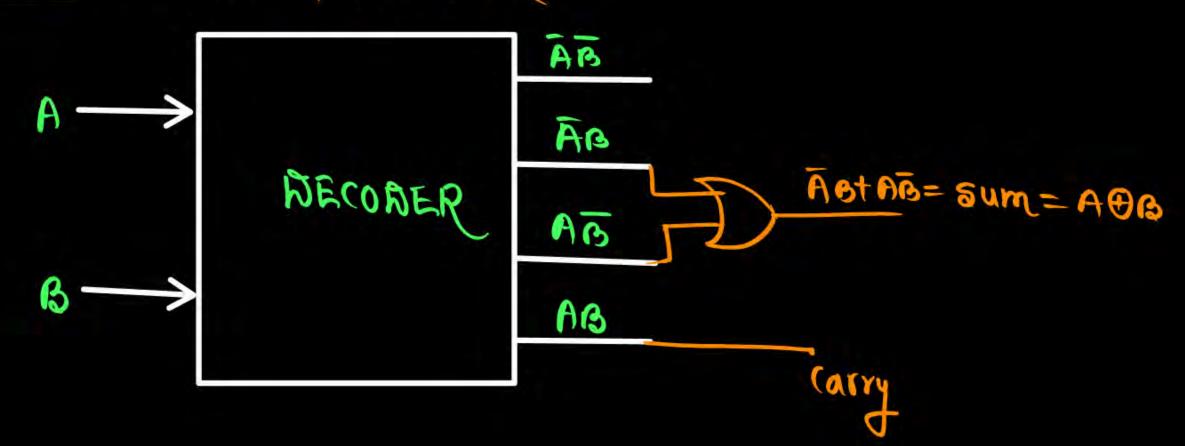


By NOR GATE

$$\overline{A}+\overline{S}=AB=CAMY$$
 $\overline{A}+\overline{S}=AB=CAMY$
 $\overline{AB+BB}=\overline{AB}$
 $\overline{AB+BB}=\overline{AB}$
 $\overline{AB+BB}=\overline{AB}$
 $\overline{AB+BB}=\overline{AB}$
 $\overline{AB+BB}=\overline{AB}$
 $\overline{AB+BB}=\overline{AB}$
 $\overline{AB+BB}=\overline{AB}$

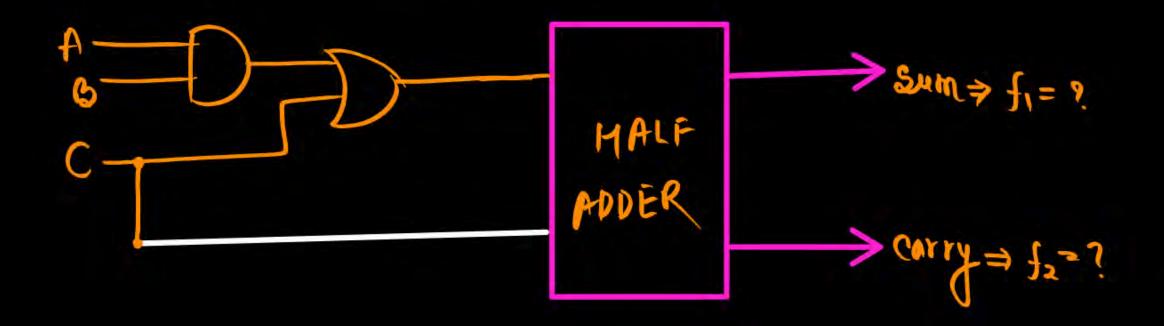
HALF ADDER BY USING DECODER





Pw

a what is the value of fi and fz?





a what is the value of fi and fz?

AB
$$+C$$

AB $+C$

AB $+C$

AB $+C$

AB $+C$

AB $+C$

ADDER

Carry $\Rightarrow f_1 = \chi \oplus C$

FULL ADDER: >



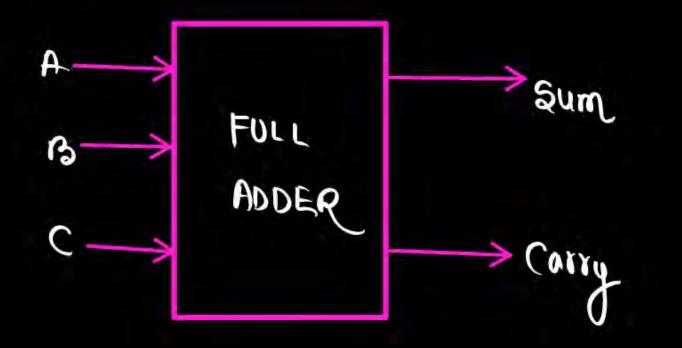
Three bit adder are known as full adder.

$$\frac{0}{0}$$
 $\frac{0}{0}$
 $\frac{1}{0}$
 $\frac{1}{0}$
 $\frac{1}{0}$
 $\frac{1}{0}$
 $\frac{1}{0}$
 $\frac{1}{0}$
 $\frac{1}{0}$



. .

Step 1:



Full Adder

Pw

majority high input Logic

FULL ADDER

Step 2.

	A	В	C	Sum	Carry
0	0	0	0	0	0
T	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	O	1 ~
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1 ,.
7	1	1	1	1	1.

Full Adder



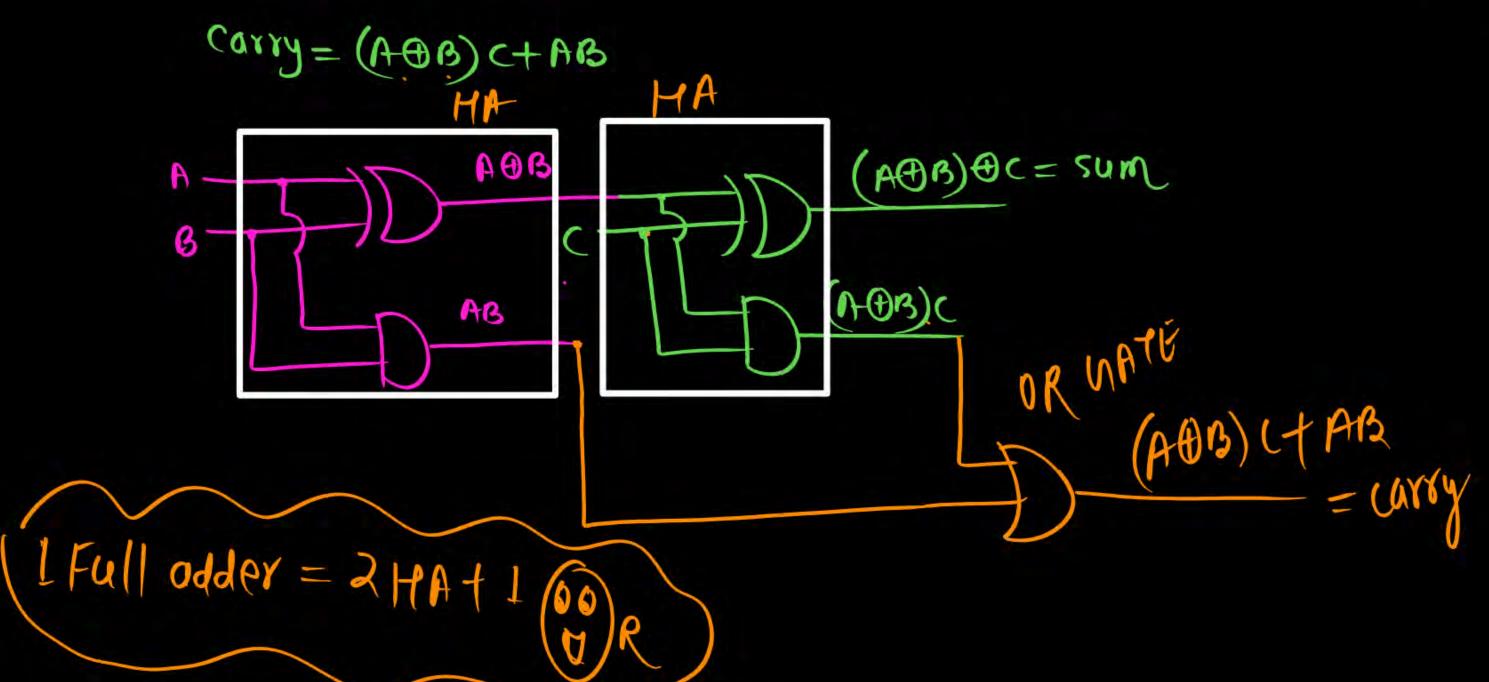
FULL ADDER

Step 3. Sum (A, B, C) =
$$\overline{ABC} + \overline{ABC} + \overline{AB$$

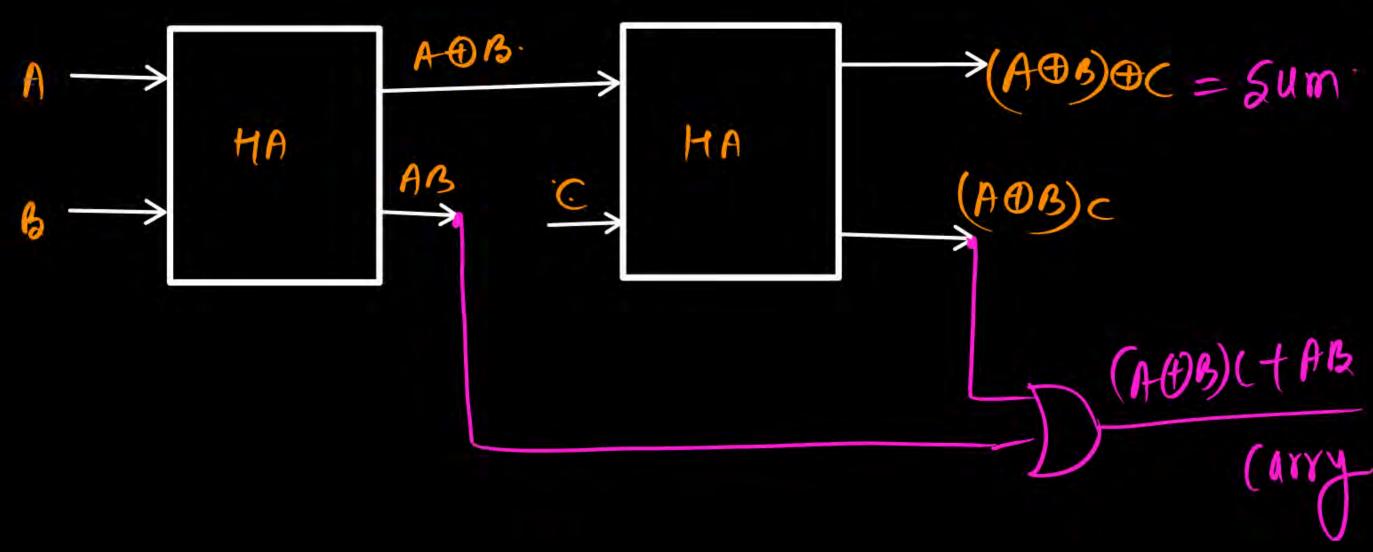








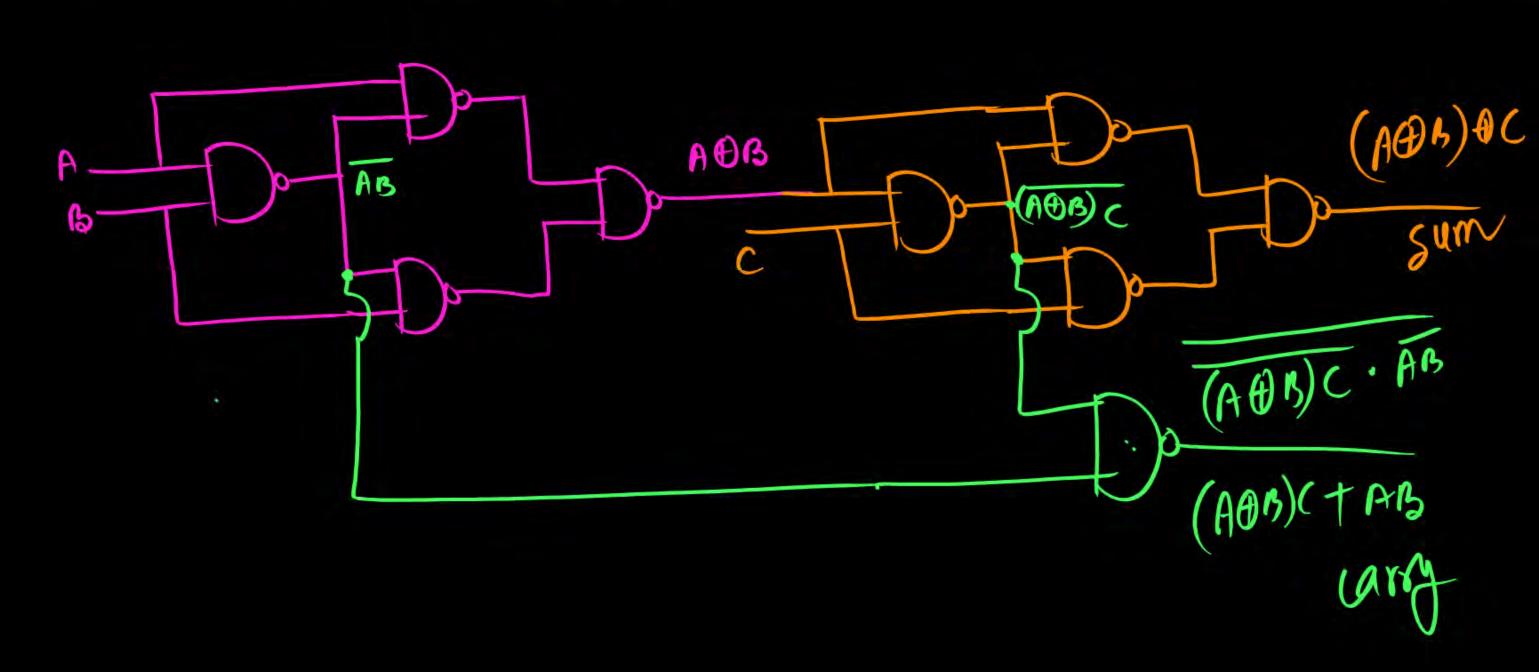




Full adder by using NAND GATE

(AOB)OC





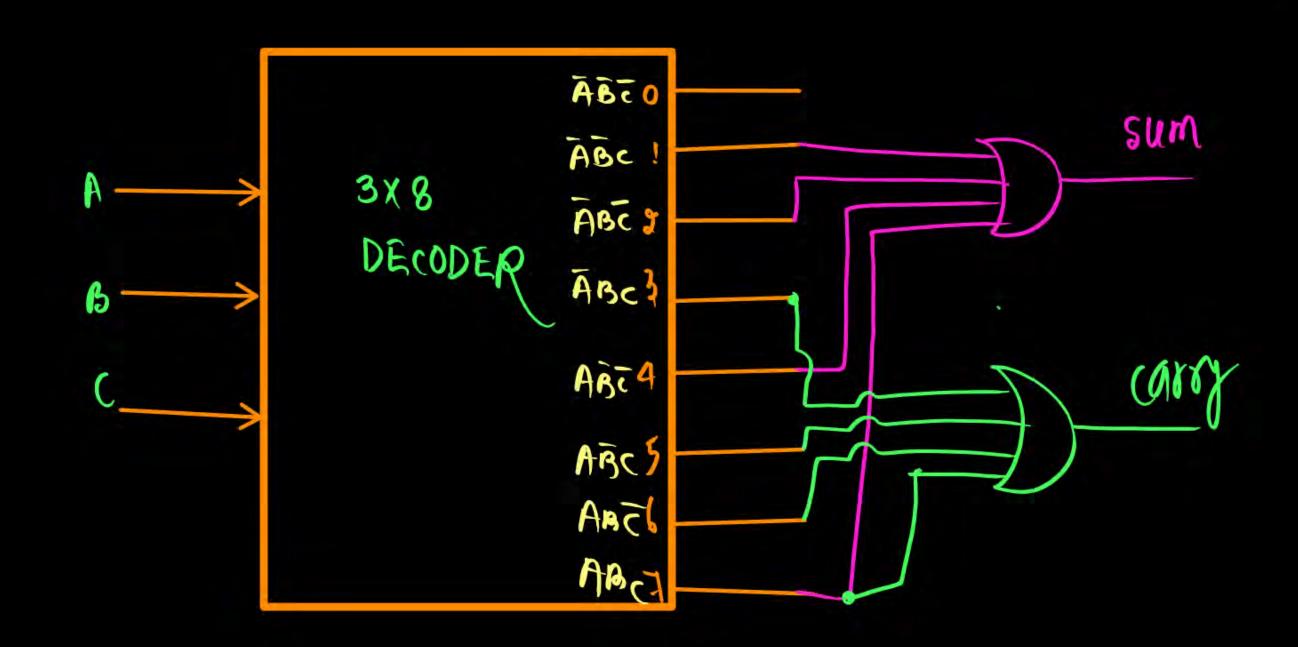


Full adder by using NOR GIATE



Full adder by using decoder



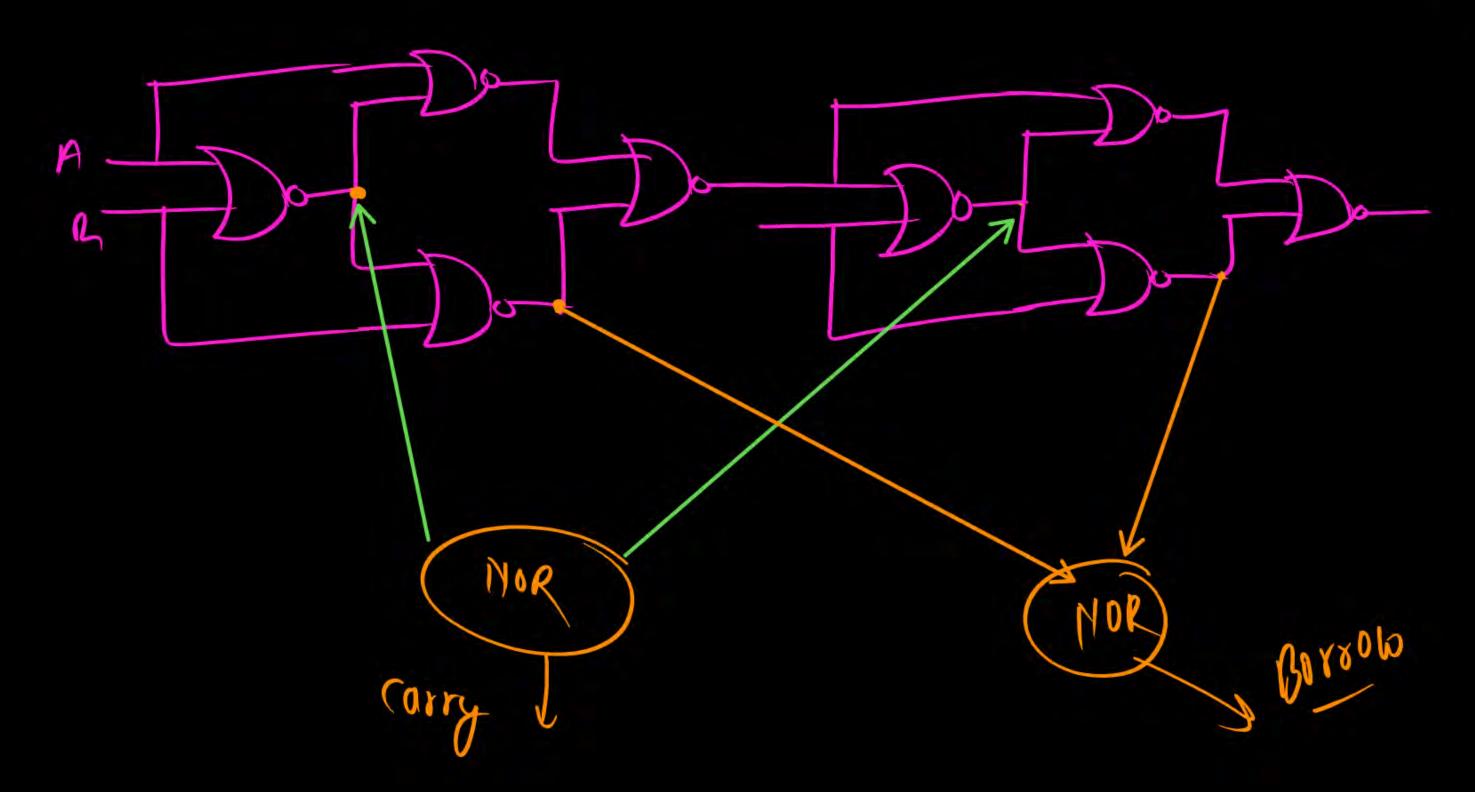




(AOB) OC AOBOC = Sum AOB. AtB (AOB)+L B (AOB)+L+ A+B T(A00)+C] [A+B]

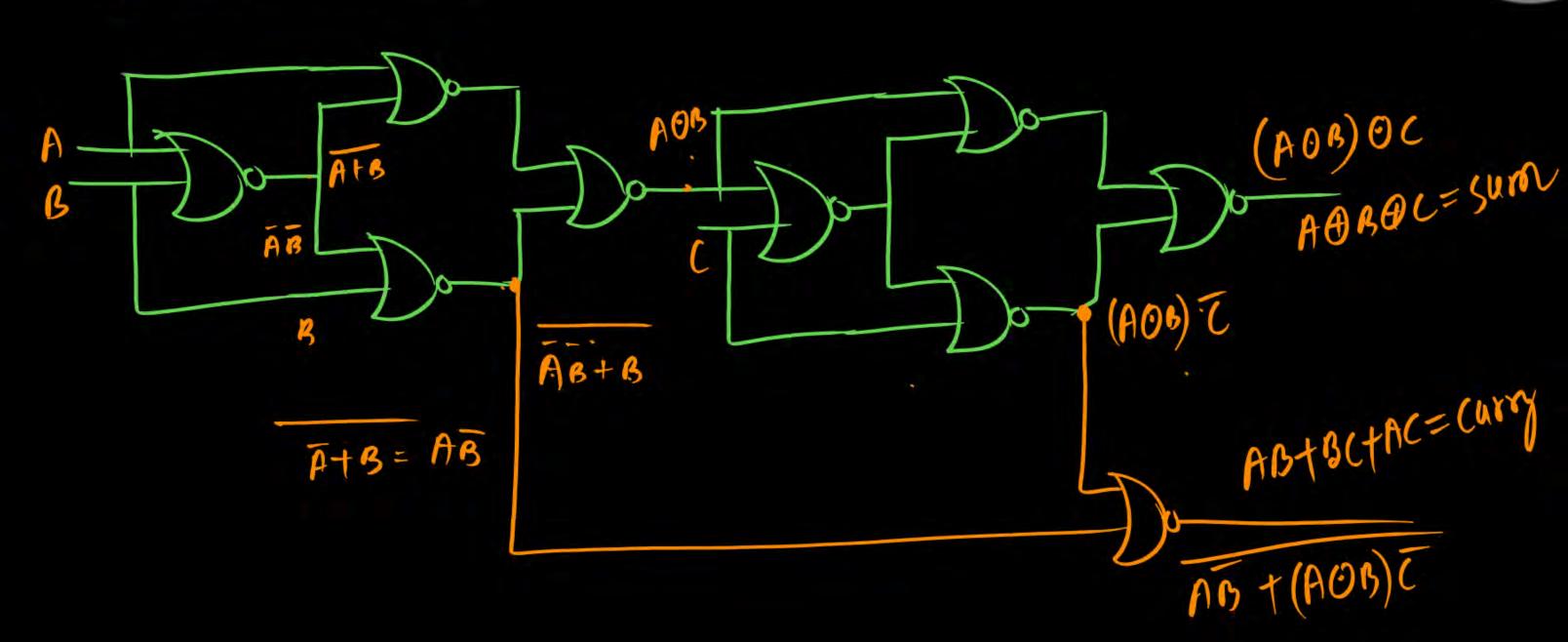






Full subtractor

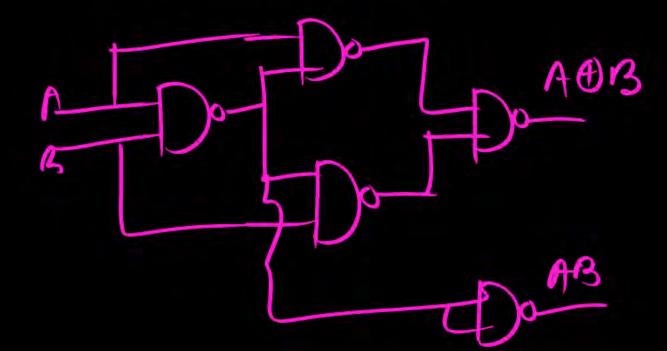




Pw

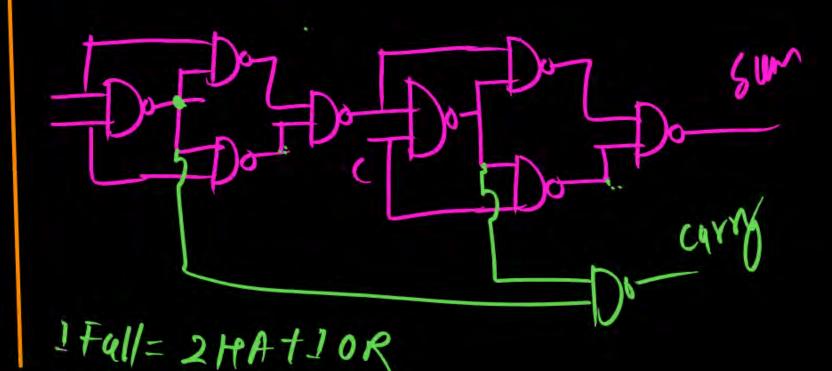
AB+ (AOB) = AB· (AOB) C (THB) (TABB)+c] (A+B) [AB+AB+C] AB+ AC+ AB+ BC AB+AC+BC 7 BOYYOW





(arry=
$$\Sigma M(3,5,6,7)$$

= $(ABB)(+AB$
= $AB+B(+AC$



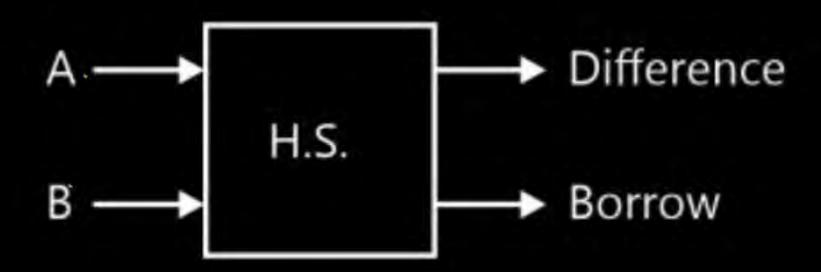
Q.1



A full adder is implemented with two half adders and one OR gate. OR gate is used to derive the final carry function of full adder. In each half adder, $T_{sum} = 25$ ns and $T_{carry} = 20$ ns and $T_{OR} = 25$ ns. The minimum time required to derive both the sum and carry function of a full adder after applying the inputs is ____ ns

Two bit subtractor ore known as half subtractor.

Step - 1





Biff = ABB

Borrow = AB

Step - 1

Α	В	Diff.	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	O	0

Step - 2

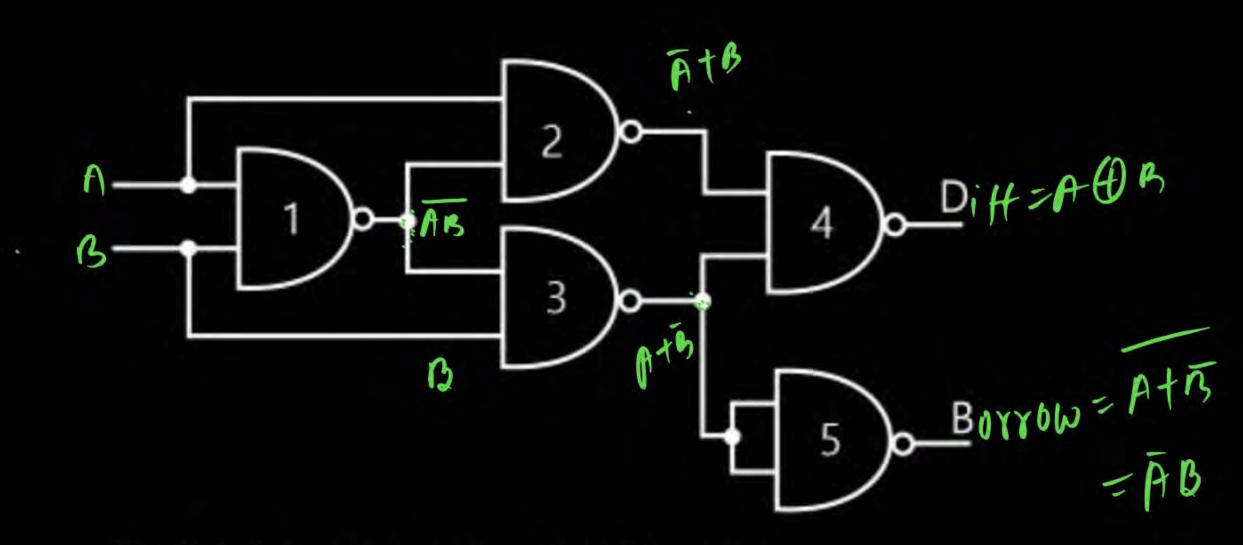
Step - 3

Diff. - A TB

Borrow - AB

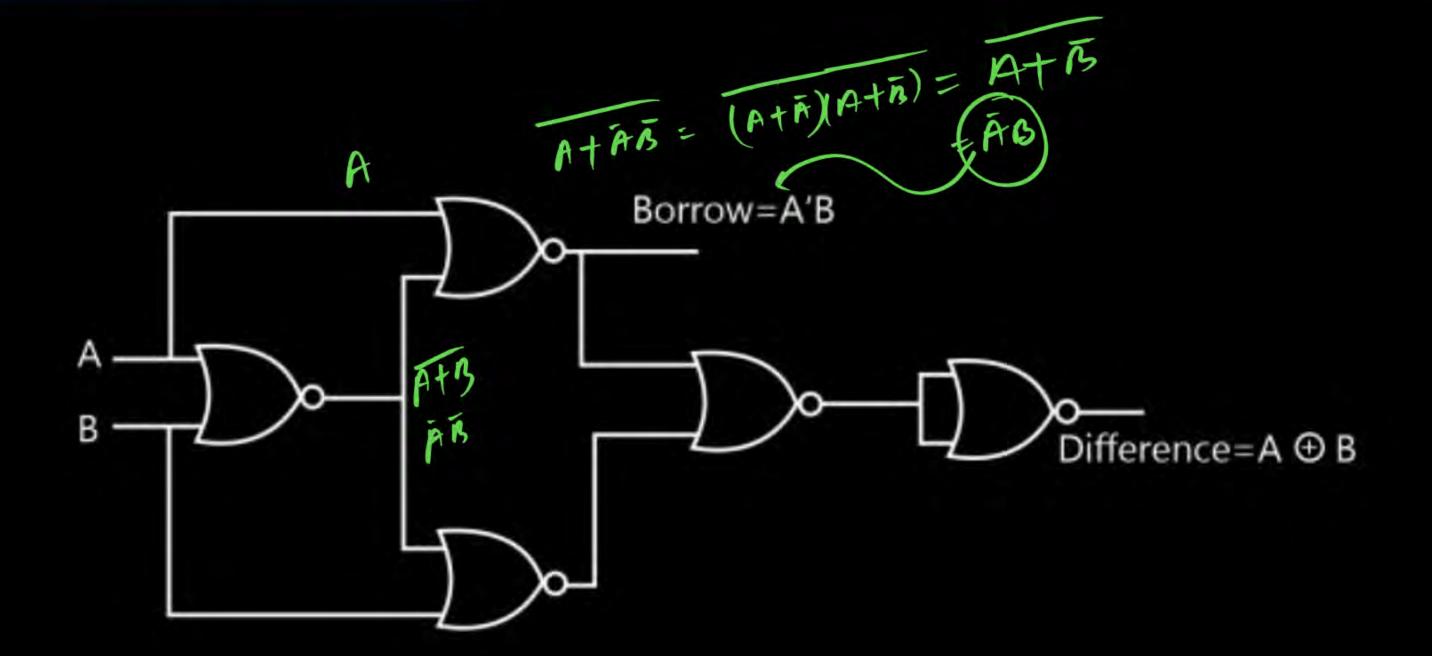






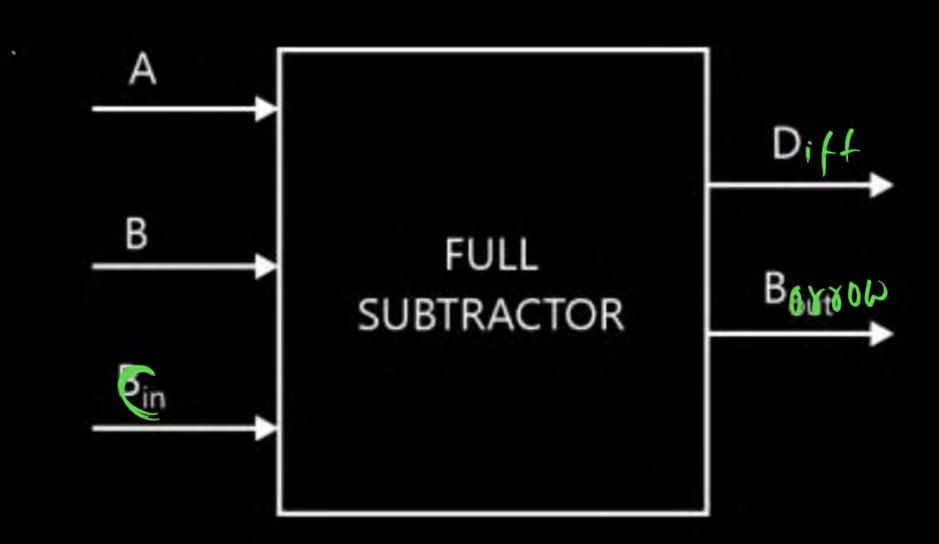
Half-Subtractor using NAND gates





FULL SUBTRACTOR





FULL SUBTRACTOR



(A-B)-C

	INPUT			OUTPUT	
Α	В	С	D	B orrow	
0	0	0	0	0	
0	0	1	1	1	
0	1	0	1	1	
0	1	1	0	1	
1	0	0	1	0	
1	0	1	0	0	
1	1	0	0	0	
1	1	1	1	1	



HA

Sum= ADB

Carry - AB

4.5

Diff - AOB

Borrow = AB

FA

Sum = A + BAC

Carry = AB+AC+BL

FS

Diff = ADBEC

BOTTOW: AB+ AC+BC

AMÁ



Pw

Thank you

Soldiers!

