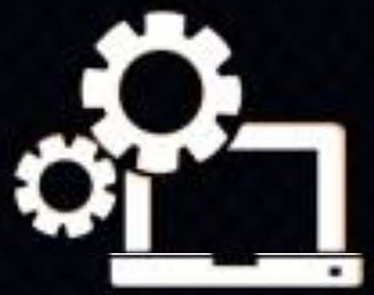
CS & IT ENGINEERING

Digital Logic

Logic Gate



Lecture No. 3

By- CHANDAN SIR

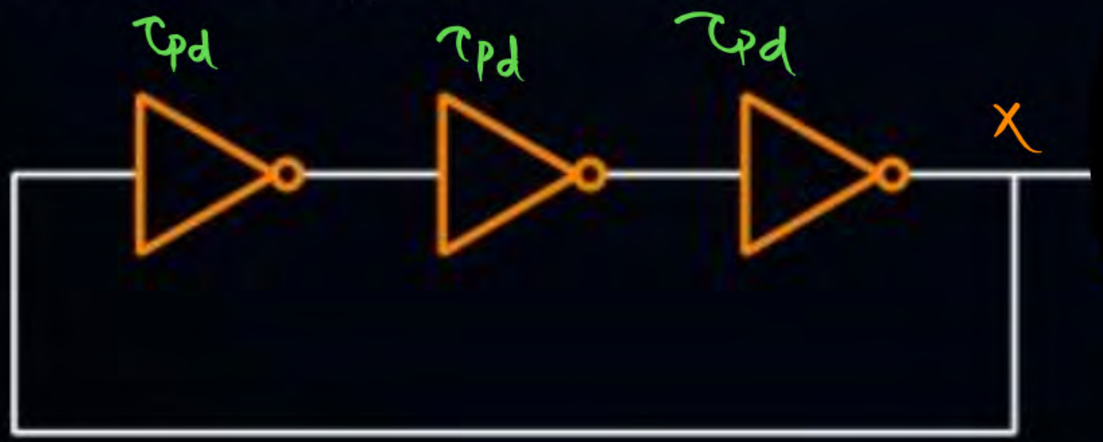
01 NAND GATE

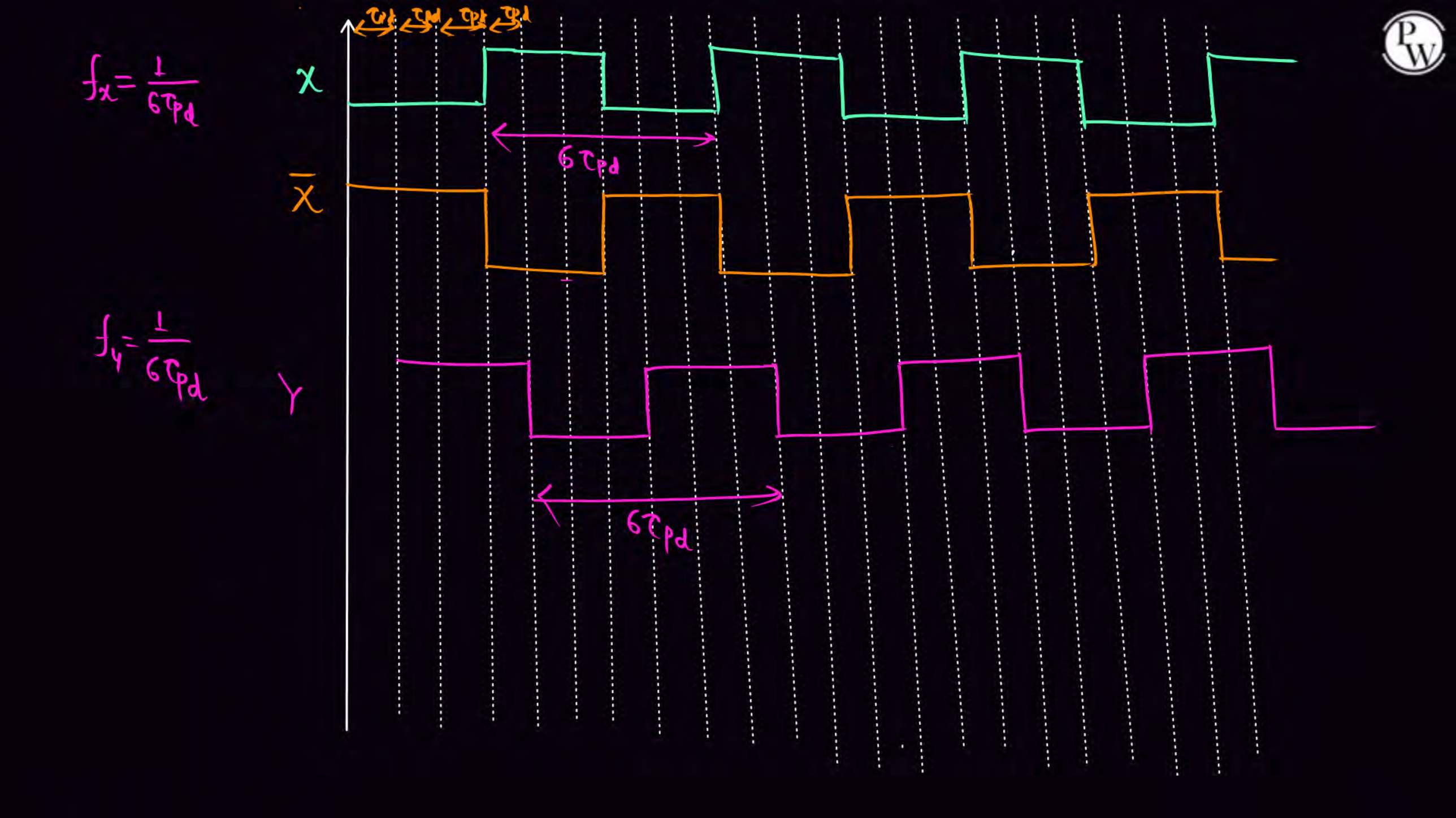
02 NOR GATE

03 Discussion

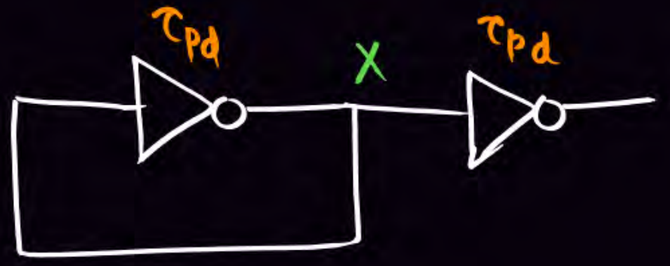
Q.

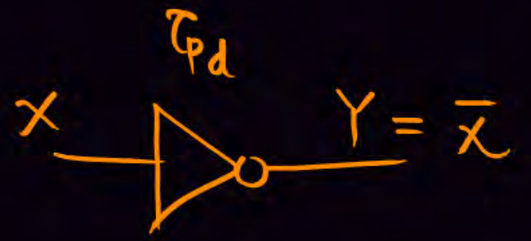
Sketch the waveform of y?

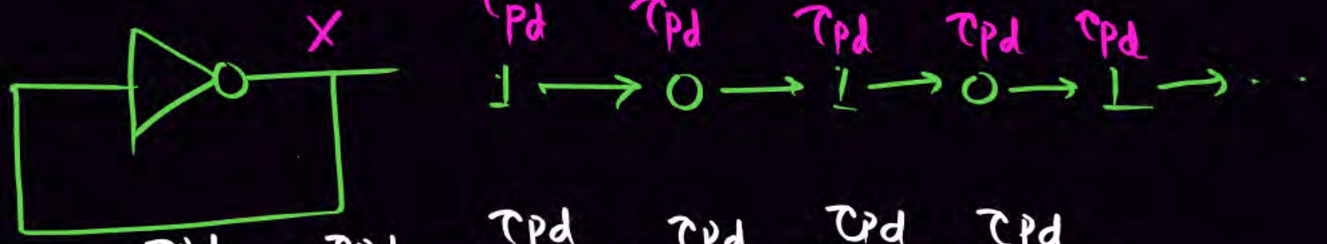



$f_x = \frac{1}{6\tau_{pd}}$
$f_y = \frac{1}{6\tau_{pd}}$
X
$\bar{X}$
Y
$6\tau_{pd}$
$6\tau_{pd}$

Q.

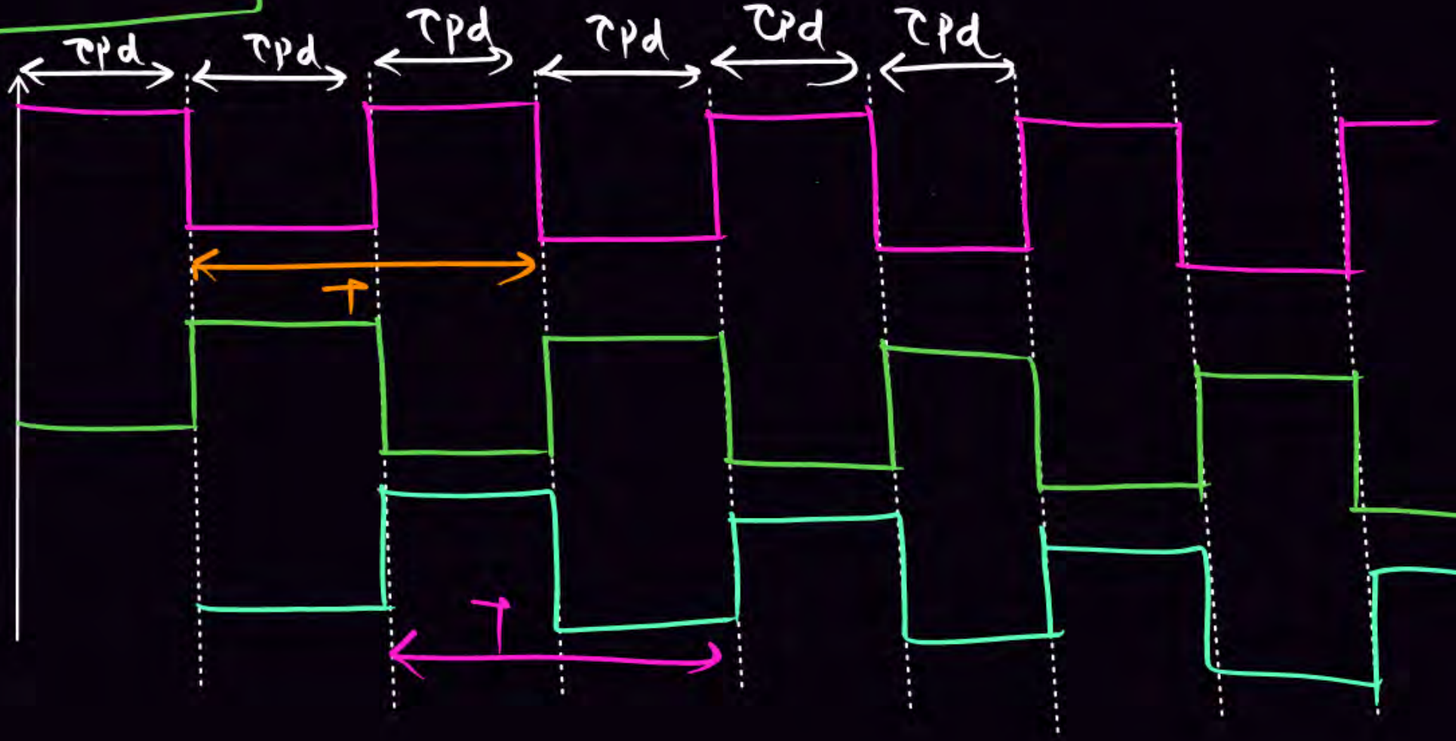






$T = 2\tau_{pd}$

$f_X = \frac{1}{T} = \frac{1}{2\tau_{pd}}$

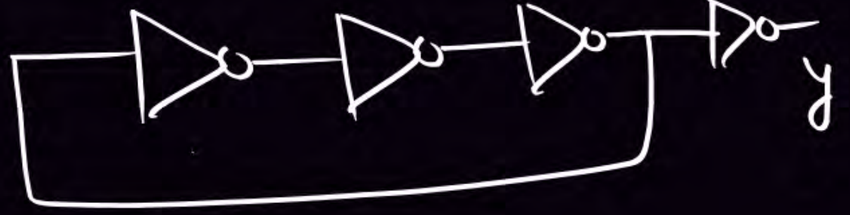


$\bar{X}$ after $1\tau_{pd}$ y

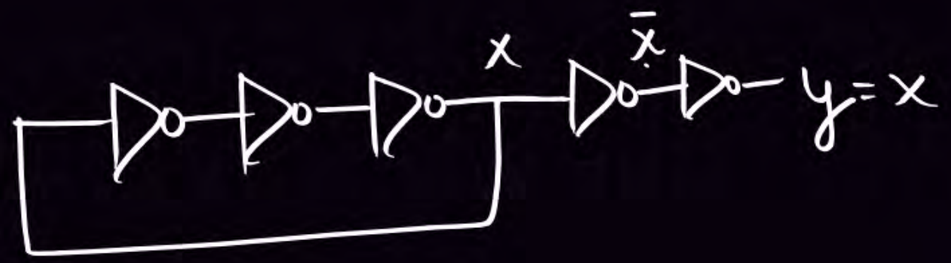
$f = \frac{1}{2\tau_{pd}}$

$T = 2\tau_{pd}$

NOTE :→ always, for calculation of frequency Consider no. of NOT GATE in Loop →



f_1



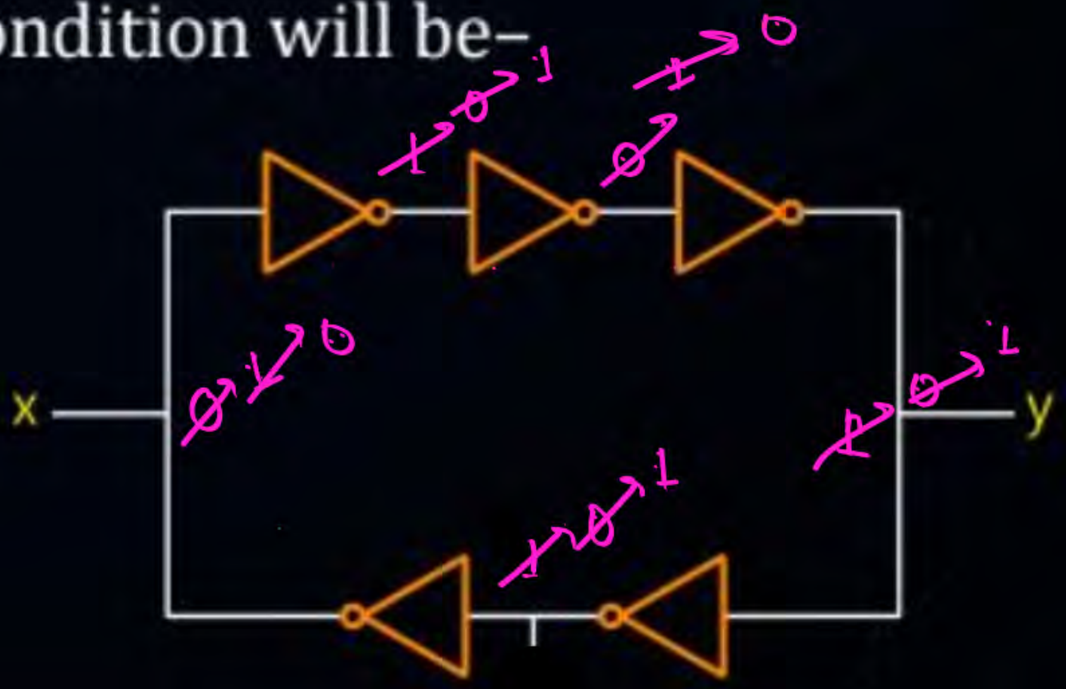
f_2

$$f_1 = f_2$$

Q.

Toggle → 0 → 1 → 0 → 1 → . . .

For the circuit given below x & y condition will be–



A. x stable y toggle

B. x toggle y stable

C. x & y both toggle

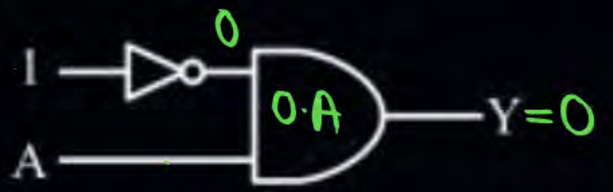
D. x & y both stable

Q.

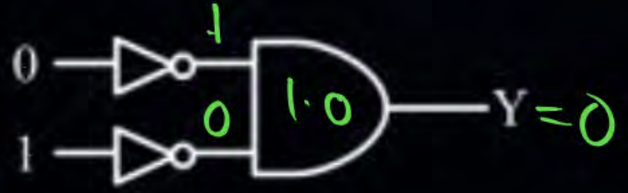
HW

A logical circuit is as shown below, which of the following circuit can be used to get the desired expression.

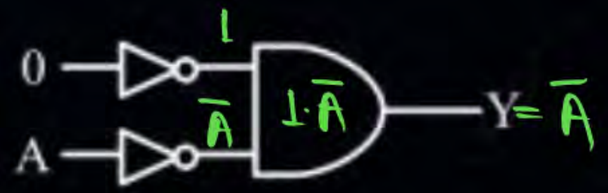
A



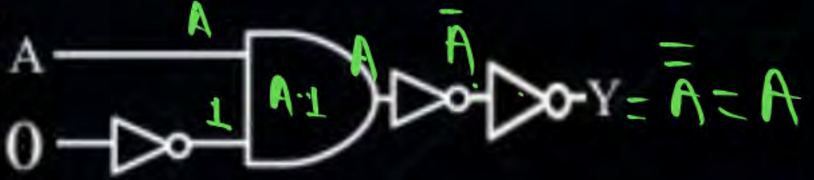
B



C



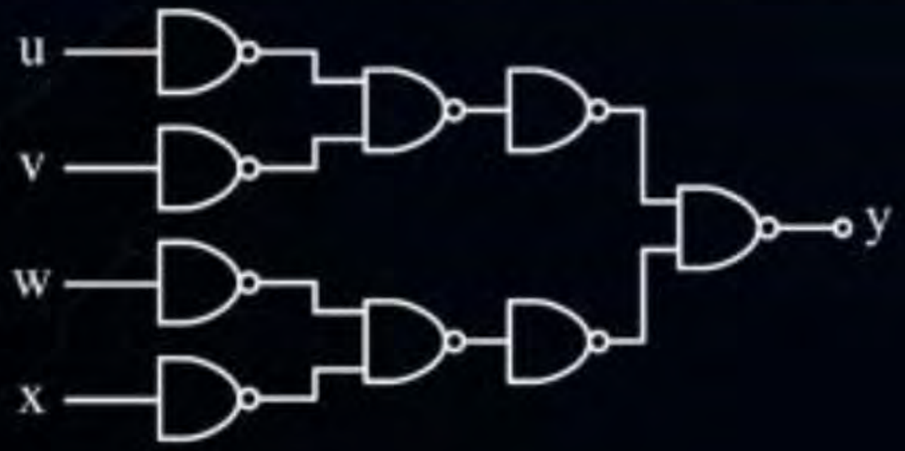
D



Q.

HW

The logic circuit shown below, is equivalent to



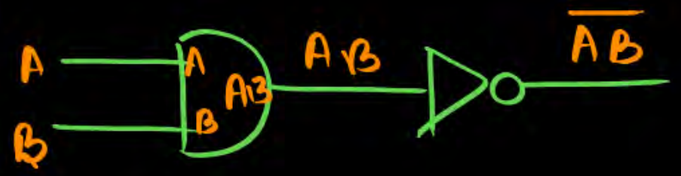
A

B

C

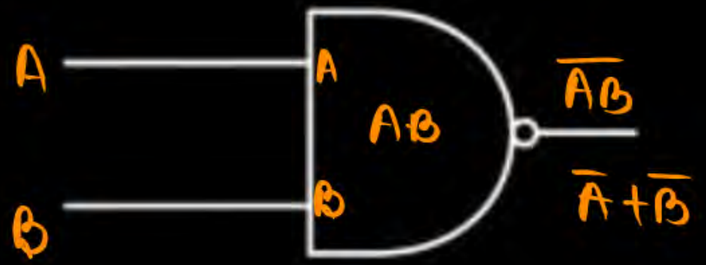
D

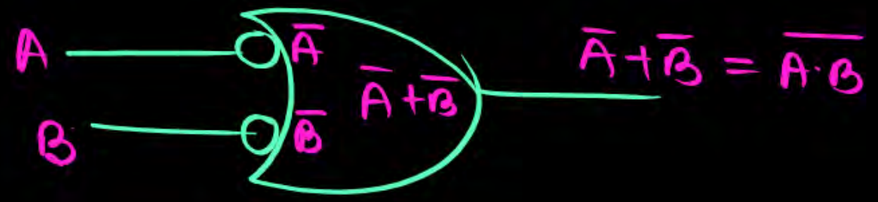
NAND, NOR GATE



- **NAND GATE**

1. Symbol





Bubbled OR ≡ NAND

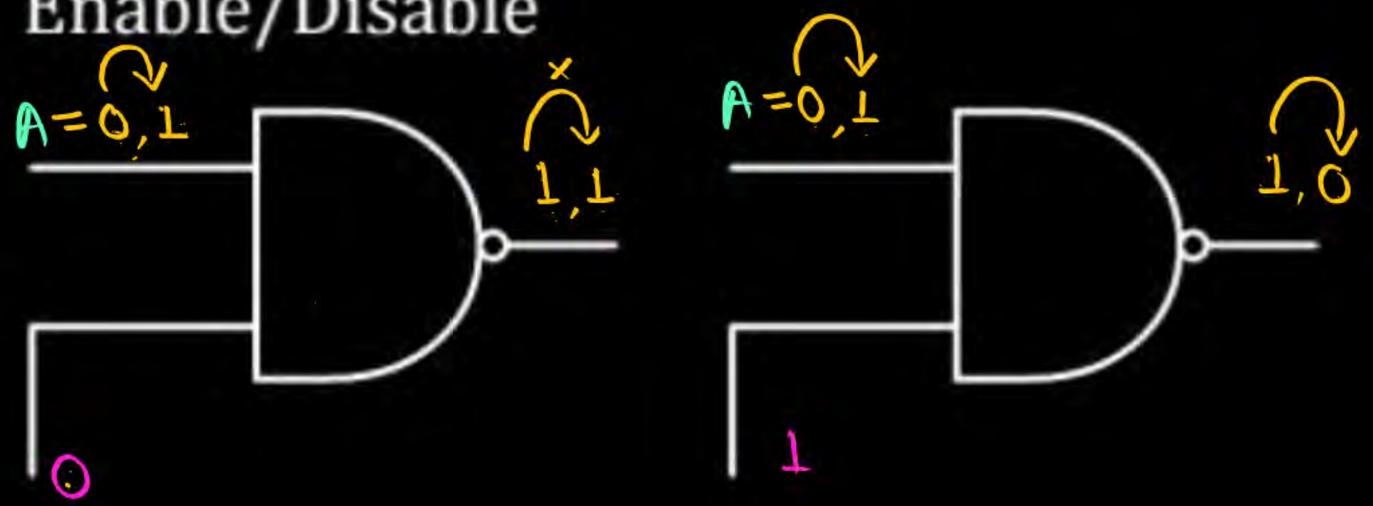
2. Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NAND, NOR GATE

- **NAND GATE**

3. Enable/Disable



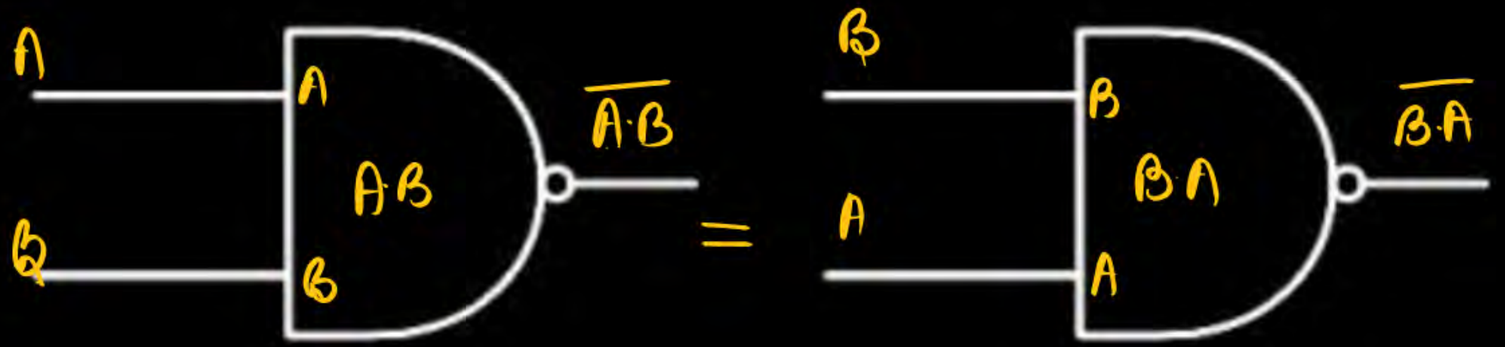
CONTROL '0' DISABLE

CONTROL '1' ENABLE

NAND, NOR GATE

- **NAND GATE**

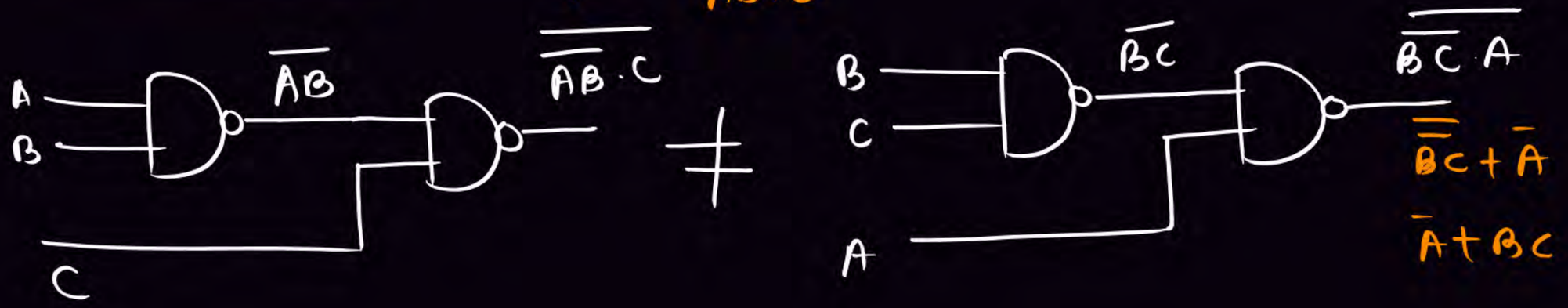
4. Commutative Law



Associative Law ✗

$\overline{\overline{AB}}+\bar{C}$

$AB+\bar{C}$



✡ NAND, NOR follow the commutative Law But does not follow Associative Law

Transistor

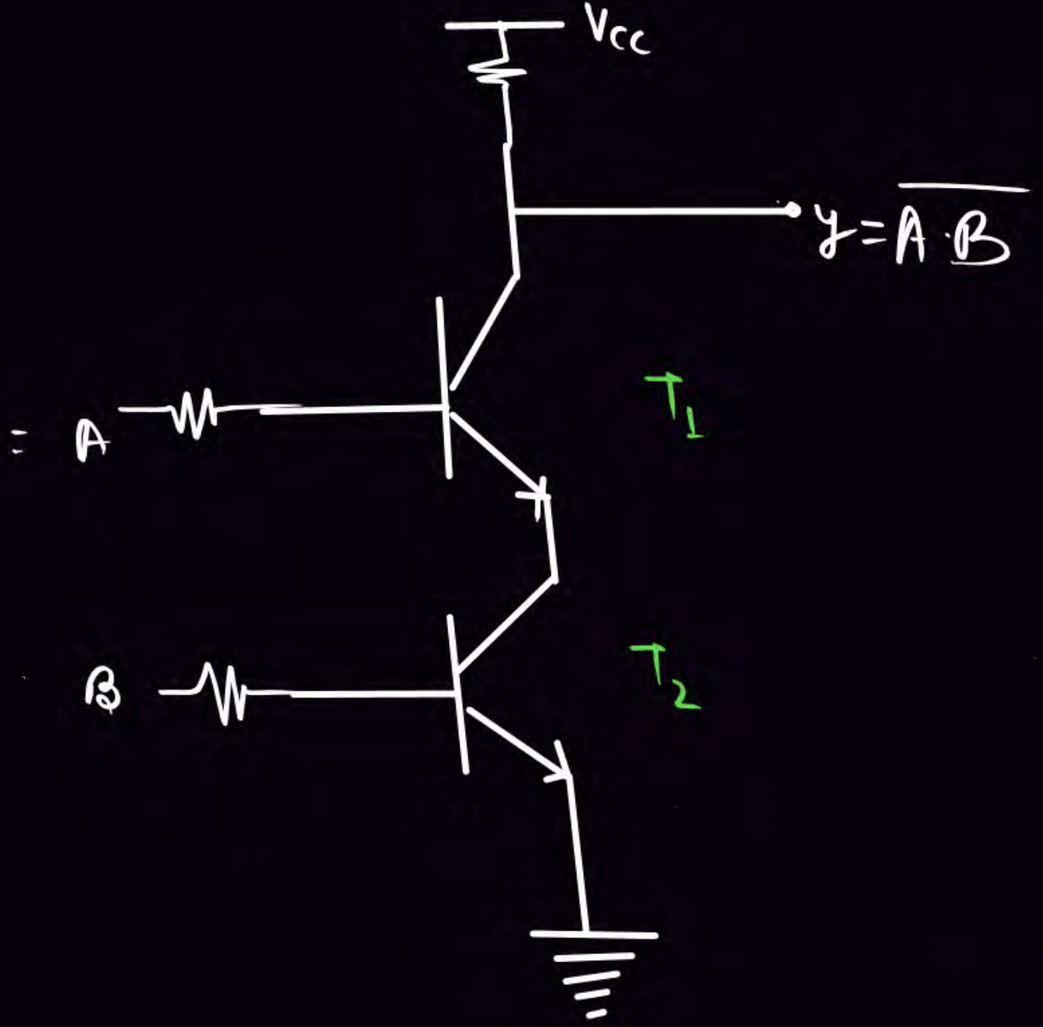
NPN

INPUT = 1

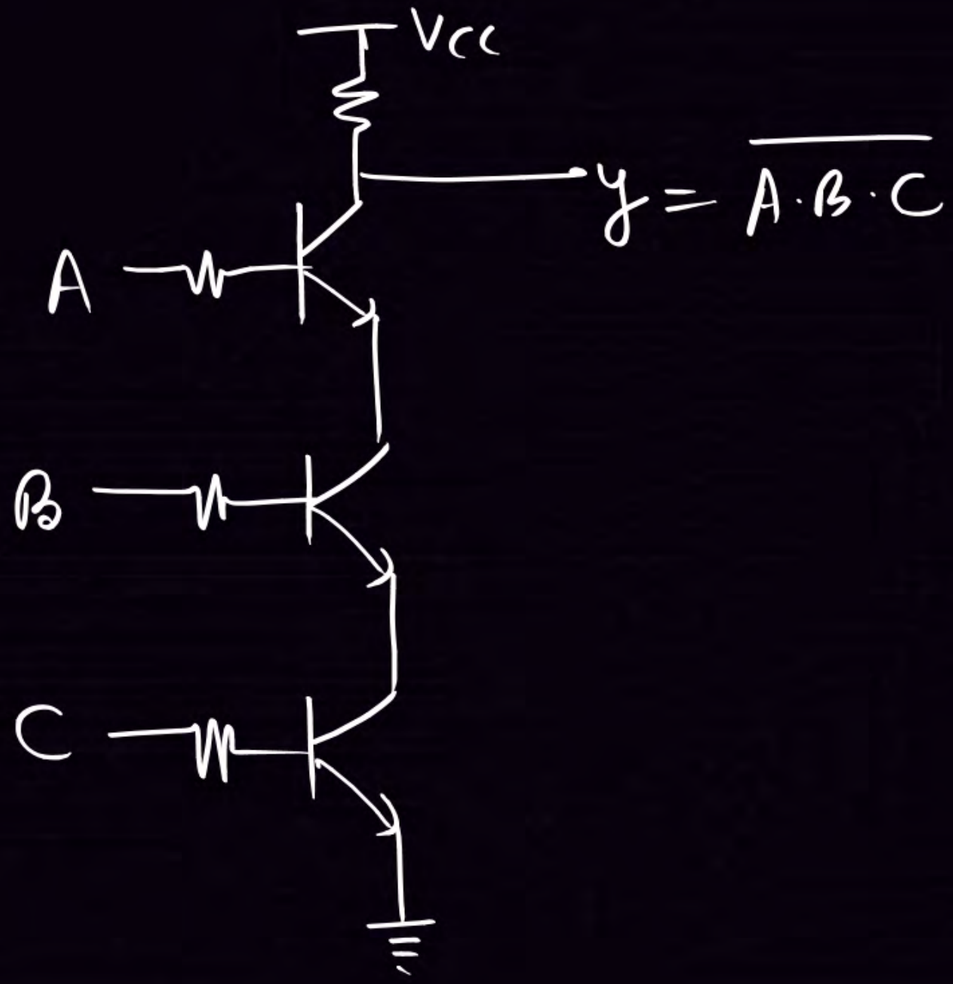
INPUT = 0

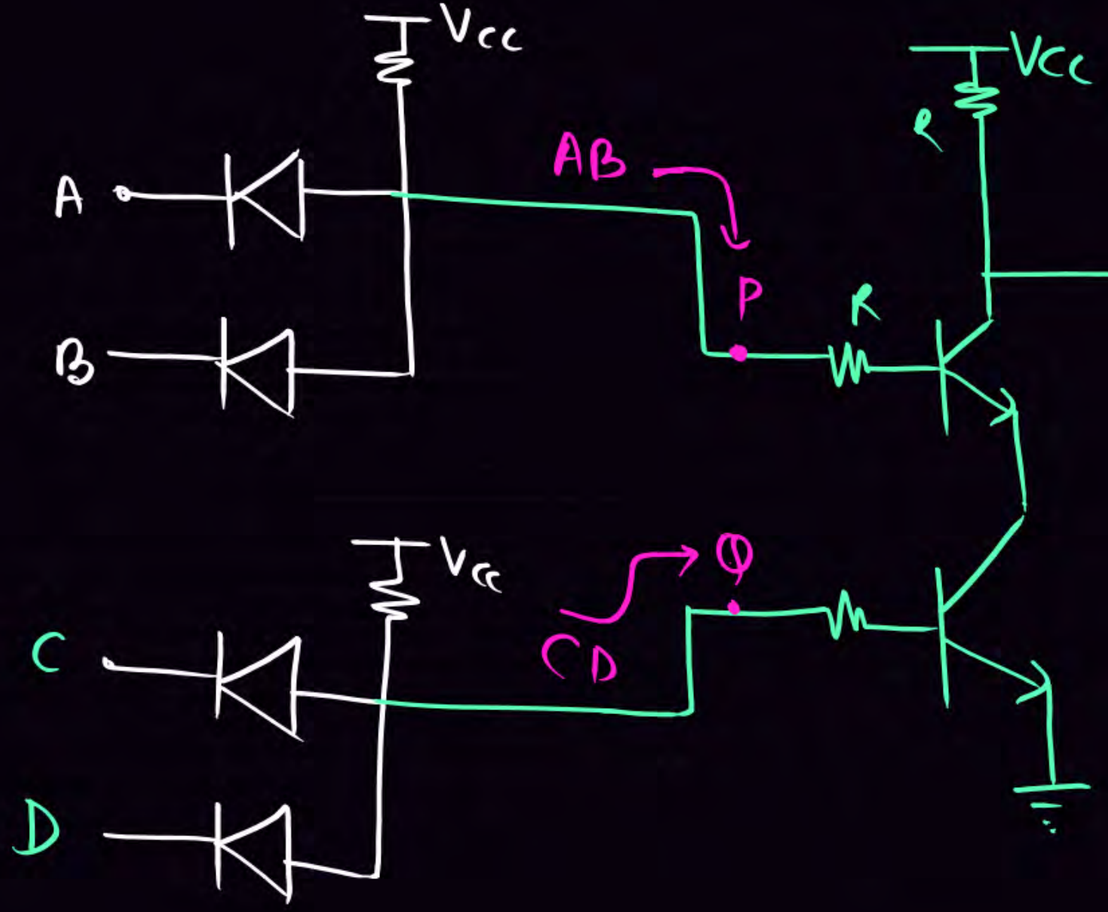
ON → Saturation → Short ckt

OFF → CUTOFF → Open ckt



A	B	T_1	T_2	Y
0	0	Cutoff	Cutoff	1
0	1	Cutoff	Saturation	1
1	0	Saturation	Cutoff	1
1	1	Saturation	Saturation	0


Vcc
$y = \overline{A \cdot B \cdot C}$
A
B
C

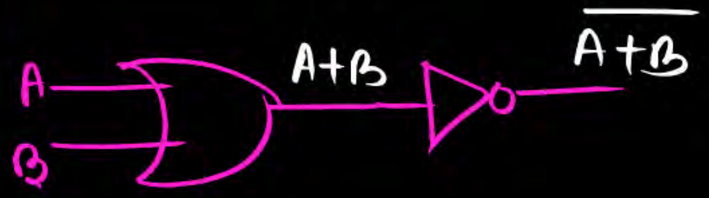


P = AB

Q = CD

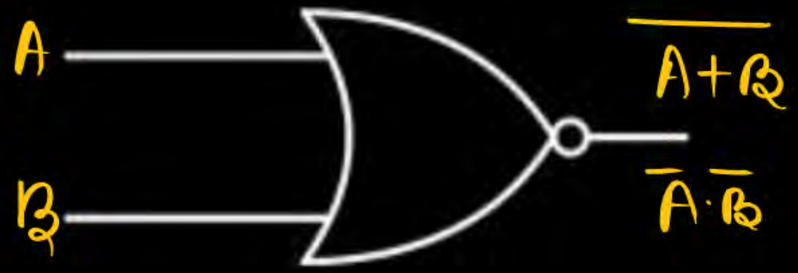
Ans

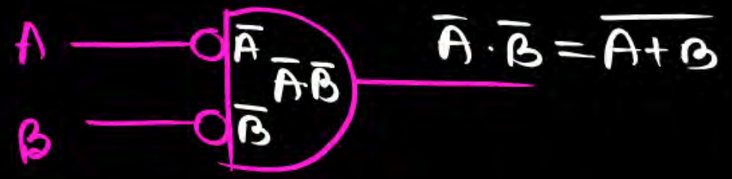
., NAND, NOR GATE



- **NOR GATE**

1. Symbol





Bubbled AND = NOR

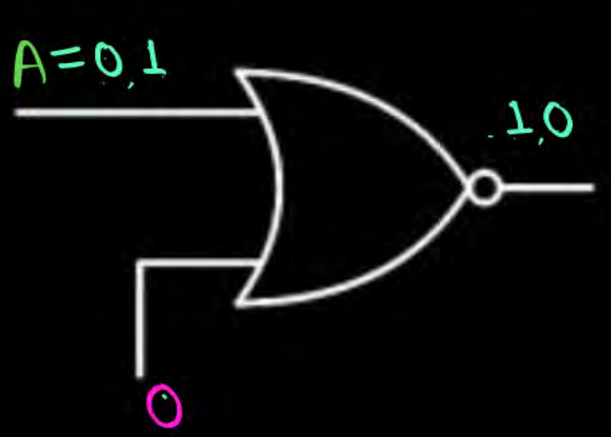
2. Truth Table

A	B	$Y=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

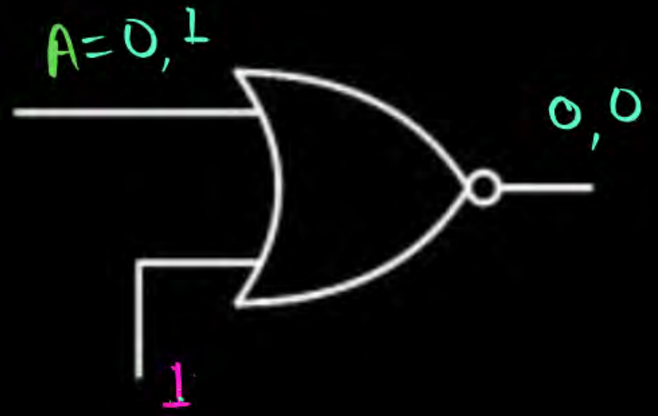
NAND, NOR GATE

- **NOR GATE**

3. Enable/Disable



CONTROL '0' ENABLE

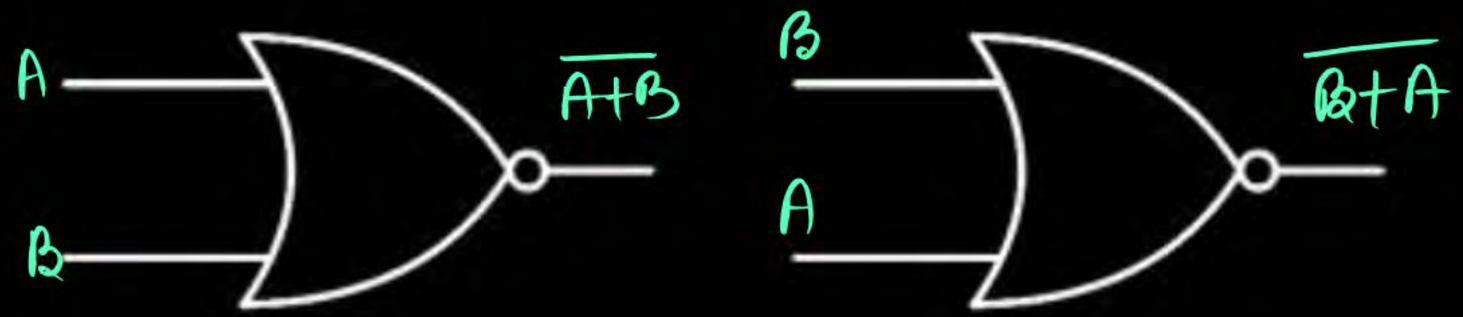


CONTROL '1' DISABLE

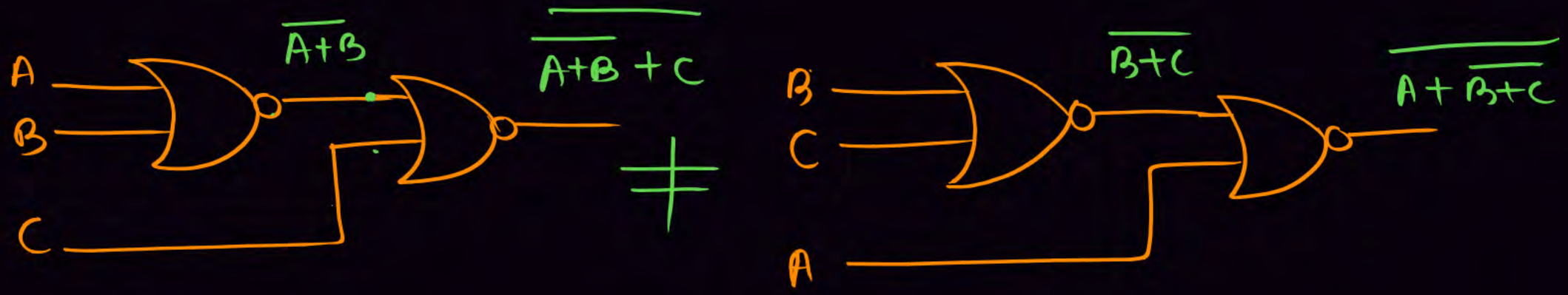
NAND, NOR GATE

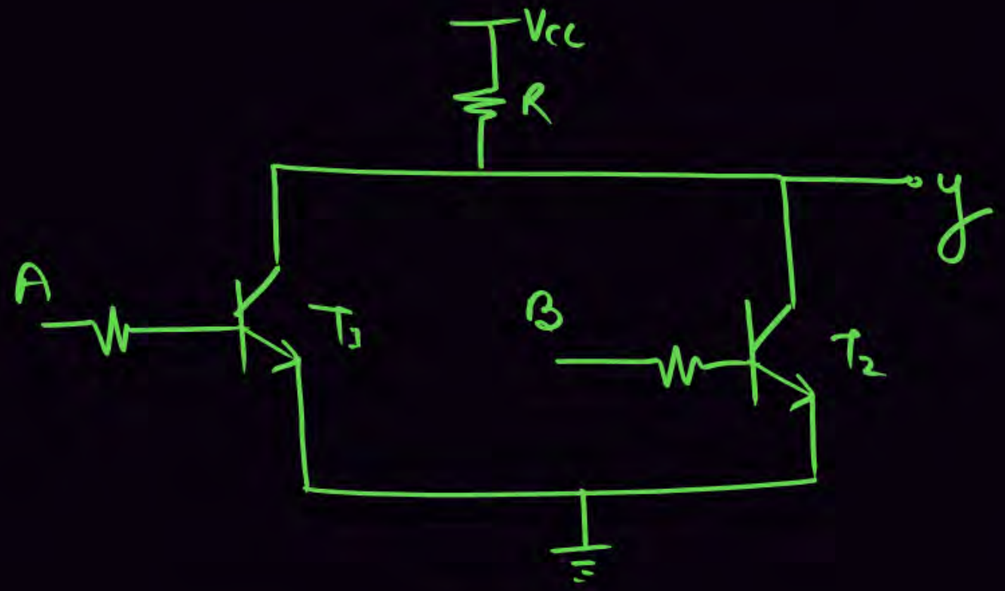
- **NOR GATE**

4. Commutative Law ✓



Associative Law ✗

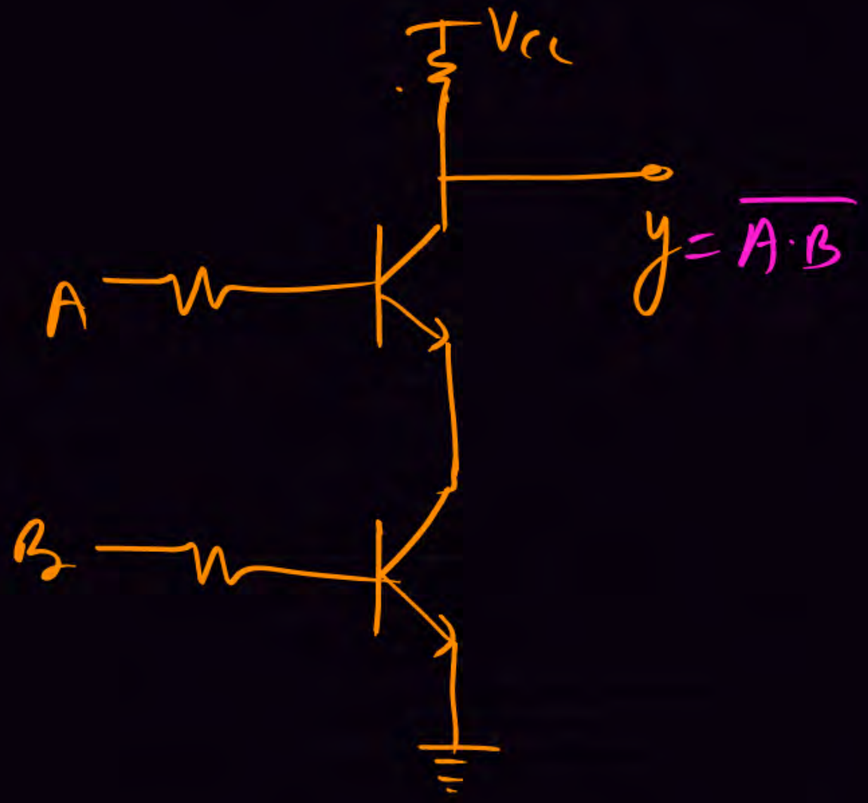


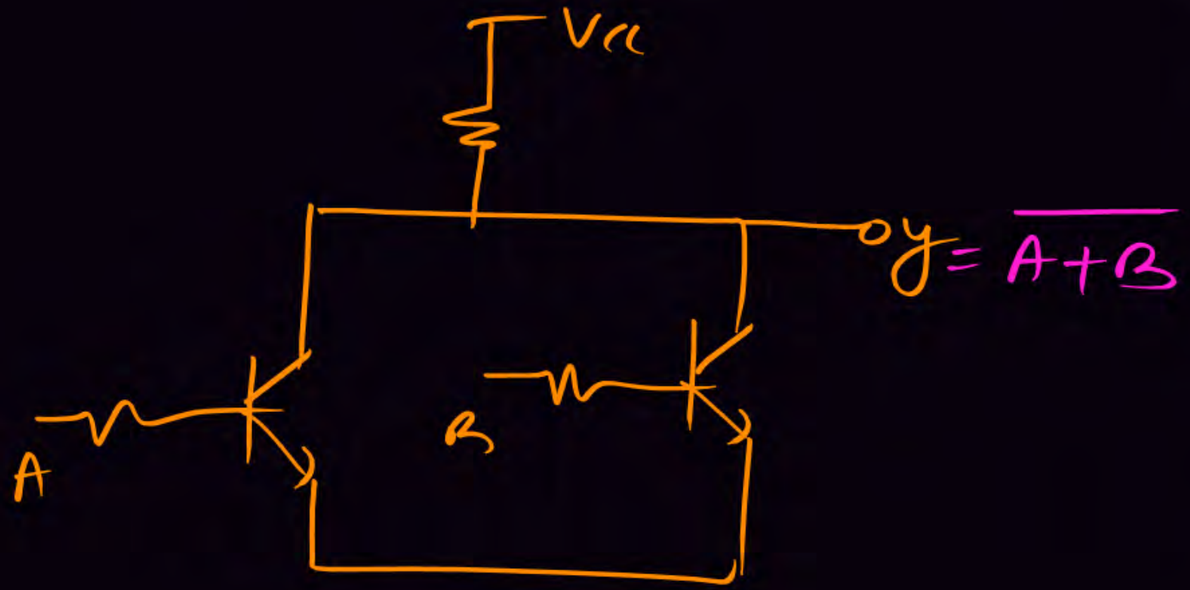


Raja

Rani

A	B	T_1	T_2	y
0	0	cutoff	cutoff	1
0	1	cutoff	saturation	0
1	0	saturation	cutoff	0
1	1	saturation	saturation	0


V_{cc}
$y = \overline{A \cdot B}$
A
B


V_{cc}
$y = \overline{A + B}$
A
B

Ex 100

NOTE :→ NAND, NOR are called universal Logic.

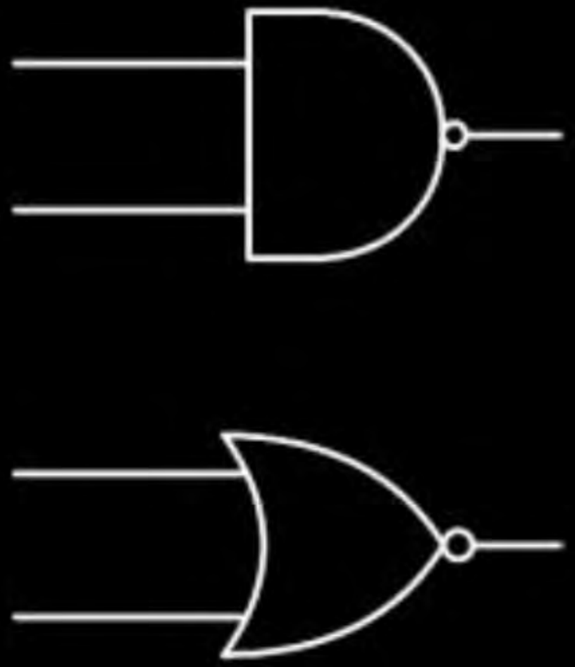
NAND, NOR GATE

- **NAND AS UNIVERSAL LOGIC**

1. NOT GATE
2. AND GATE
3. OR GATE
4. XOR GATE
5. XNOR GATE

NAND, NOR GATE

- **Alternate Symbol**



Q.

MCQ

Which of the following option is called universal logic?

A NAND

B NOR

C Both A & B

D None

Q.

MCQ

Which of the following option is called universal logic?

A NAND

B NOR

C AND

D OR

Q.

MSQ

Which of the following option(s) is/are called universal logic?

A $\overline{(A+B)}$

B $\overline{(A \cdot B)}$

C $(A+\overline{B})$

D $A \cdot \overline{B}$

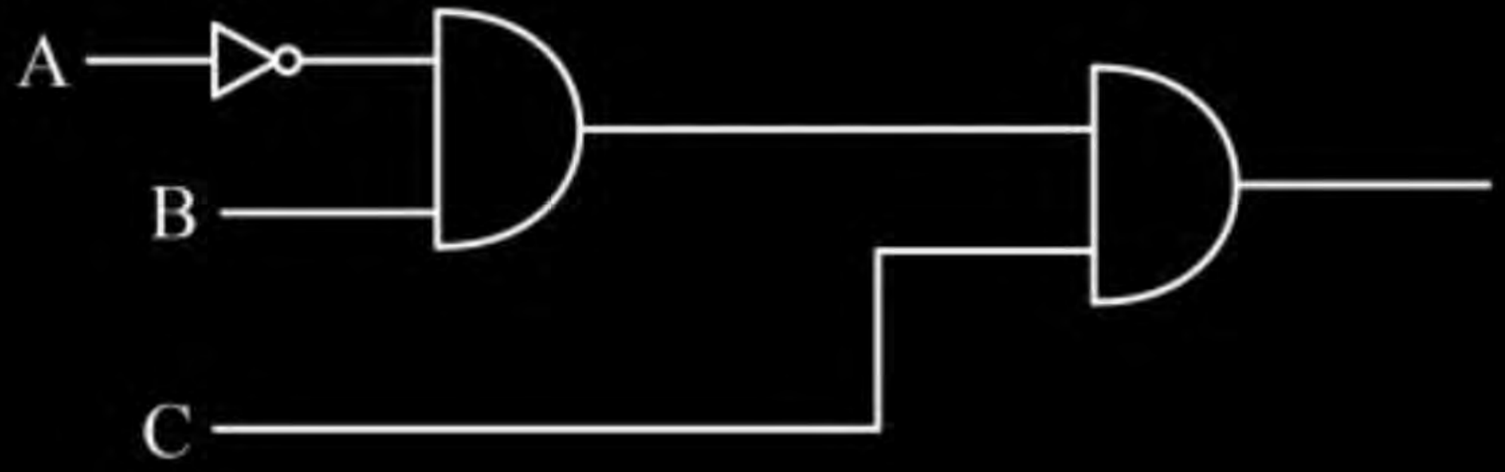
$\overline{A \cdot B}$ → NAND

$\overline{A+B}$ → NOR

Q.

NAT

For the following circuit diagram minimum numbers two NAND gate required.



Thank you GW Soldiers !

मां
पापा
Teacher

#Self confidance