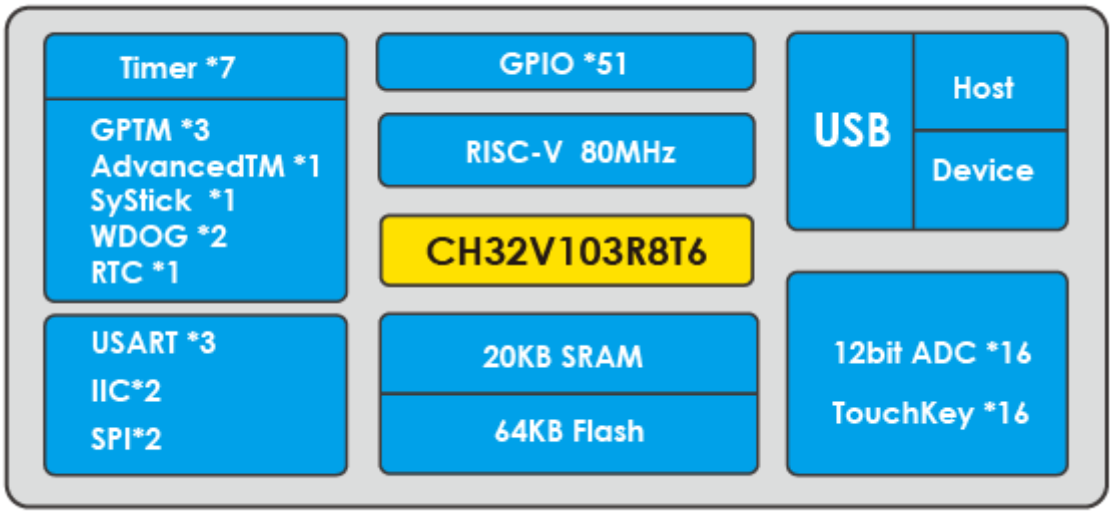
32-bit General Enhanced RISC-V MCU – CH32V103

Overview

The CH32V103 is a general purpose microcontroller based on the 32-bit RISC processor RISC-V3A. The CH32V103 provides clock security system, multi-level power management and general DMA controller. The CH32V103 is also equipped with abundant peripheral resources, such as single USB2.0 host/device interface, multi-channel 12-bit ADC module, multi-channel TouchKey, several timers, and multi-channel IIC/USART/SPI interfaces, etc.

System Block Diagram



Features

- Qingke V3A processor, max 80MHz system clock frequency.
- Single-cycle multiplication and hardware division.
- 20KB SRAM, 64KB CodeFlash.
- 2.7V to 5.5V supply voltage, supplies to GPIO simultaneously.
- Low-power modes: sleep/stop/standby.
- Power-on/power-down reset (POR/PDR).
- Programmable voltage detector (PVD).
- 7-channel DMA controller.
- 16-channel TouchKey detection.
- 16-channel 12-bit ADC.
- 7 timers.
- One USB2.0 host/device interface (full-speed and low-speed).
- Two I2C interfaces (support SMBus/PMBus).
- 3 USARTs.
- 2 SPIs (Master mode and Slave mode).
- 51 I/O ports, all I/O ports can be mapped to 16 external interrupts.
- CRC calculation unit, 96-bit unique ID.
- Serial debug interface (SDI).

- Packages: LQFP64M, LQFP48, QFN48.

Product Selection Guide

Part NO.	Flash	SRAM	Host/Device	Timer				Connectivity			ADC/ TouchKey	GPIO	VDD/V	Package
				GPTM	Advanced TM	WDOG	SysTick	SPI	I²C	USART				
CH32V103R8T6	64K	20K	1	3	1	2	1	2	2	3	16/16*12b	51	2.7~5.5	LQFP64M
CH32V103C8T6	64K	20K	1	3	1	2	1	2	2	3	10/10*12b	37	2.7~5.5	LQFP48
CH32V103C8U6	64K	20K	1	3	1	2	1	2	2	3	10/10*12b	37	2.7~5.5	QFN48
CH32V103C6T6	32K	10K	1	2	1	2	1	1	1	2	10/10*12b	37	2.7~5.5	LQFP48

Technical Resources

1. Datasheet: **CH32V103DS0.PDF**, **CH32xRM.PDF**
2. CH32V103EVT evaluation board manual and reference routines: CH32V103EVT.ZIP
3. Integrated development environment (IDE): **MounRiver Studio(MRS)**