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Performance Analysis of NMOS for Higher Speed and Low Power Applications

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Abstract—**Integrated circuits based on low supply voltage and subthreshold operations of NMOS devices are very attractive for low power applications. An effective way to reduce supply voltage and resulting in power consumption without losing the circuit performance of NMOS is to increase the drive current of NMOS. This paper reports the scaling analysis of NMOS from deep-submicron to nanometer technologies, in which channel length has been scaled down from 600nm to 90nm. For simulation, ATLAS device simulator is used, by using the models LAMBARDI (CVT) mobility model and fixed Shockley-read-hall model recombination model. Simulation result depicts that threshold voltage is 0.26V at 600nm, 0.04V at 180nm and 0.01V at 90nm so nanometer range NMOS devices can be very attractive for low power and subthreshold operations.**

Keywords- Low voltage; low power; nano-NMOS device.

I. INTRODUCTION

For last few years, scaling of the devices for smaller dimensions, higher packing density, faster speed and lower power dissipation has been done enormously [1]. CMOS technology has been useful to get low power consumption, at the cost of low noise immunity and low performance. CMOS devices were scaled for more than three decades, later it replaced by single NMOS or PMOS to achieve higher noise immunity, reduces power and improves circuit robustness [2]. Transistor delay time reduces more than 30% per technology generation. This results in doubling of microprocessor performance every two years [3]. Supply voltage has been scaled down in order to keep lower power consumption. The transistor threshold voltage has to be scaled to maintain a high drive current and achieve performance improvement. However, the threshold voltage scaling results in increase of the subthreshold leakage current [4].

The path of scaling has been determined by following goals [5]:

1) Increased transistor current- To get less charging and discharging time of parasitic capacitances, this require short channel and higher electric field.

2) Reduced size for density- To achieve higher packing density device dimensions i.e. source/drain diffusion area, channel length and width should be small.

In order to tackle the various design issues and challenges of nanometer devices, a detailed study and analysis has been carried out by scaling down the NMOS device from deep-submicron to nanometer technologies using SILVACO TOOL. In the next section, description of the structure by using tool is given. In section III, simulation results by using DC and AC analysis is given. Last section concludes the paper.

II. DEVICE STRUCTURE AND SIMULATION

ATLAS provides general capabilities for physically-based two-dimensional and three-dimensional simulation of semiconductor devices. ATLAS is designed to be used with VWF interactive tools. The VWF interactive tools are DECKBUILT, TONYPLOT and DEVEDIT. For NMOS, silicon substrate with boron doping concentration of 10^{15} cm^{-3} and polysilicon gate with arsenic doping concentration of 10^{19} cm^{-3}, DEVEDIT is used. DECKBUILD is the interface between DEVEDIT and the device simulator ATLAS. In this environment, NMOS structure is called through command which is made at DEVEDIT environment, ATLAS device simulator simulates it. The values of supply voltage used are 3.3V for 600nm, 1.8V for 180nm and 1V for 90nm. The value of drain voltage is 0.1V. Mobility and recombination models are used for simulation of NMOS. Mobility model comprises parallel electric field, vertical electric field, traverse field, doping dependent and temperature dependent parts of mobility model is combined by Matthiessen's rule. In recombination model carrier generation–recombination is the process through which the semiconductor material attempt to return equilibrium after being distributed from it. Fixed Shockley-Read-Hall (SRH) recombination model at 300k temperature is used. Simulator gives the value of device parameters i.e. threshold voltage, leakage current, transconductance coefficient, sub threshold voltage for DC analysis, and capacitance and transconductance for AC analysis. The graphical representation of simulation results of NMOS device in three technologies is shown in TONYPLOT.

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III. RESULTS AND DISCUSSION

A. DC Analysis

In this analysis device start with zero bias at all electrodes of AC sources. It shows the relationship between input and output characteristics with gate and drain voltage. In dc analysis, simulator gives the value of threshold voltage, transconductance coefficient, mobility modulation parameter, leakage current, subthreshold voltage. This section shows the comparisons at 600nm, 180nm and 90nm in dc analysis. Fig. 1 shows relation between input gate voltage (Vgs) and drain current (Ids). As technology scales down, drain current increases.

Table 1 shows the comparison of different parameters with technologies. In this table, V_t is the threshold voltage, β is the transconductance coefficient, θ is mobility modulation parameter & subvt is the subthreshold voltage. This paper reports the change in the values of leakage current & threshold voltage by scaling the NMOS device from deep-submicron to nanometer. When technology scales down, threshold voltage decreases, as the barrier for the majority carriers to enter the channel also reduces [6]. Supply voltage reduces to maintain reliability. When V_{dd} is reduced towards the short channel length, it becomes increasingly difficult to satisfy both the performance and off-current requirements. One often faces a tradeoff between leakage current versus circuit speed. As threshold voltage is reduced, transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available. The circuit design is a compromise between strong current in the "on" case and low current in the "off" case [7].

Table 1 Comparison of different parameters with different technologies

Parameters	600nm	180nm	90nm
V_t	0.26169 V	0.048628 V	0.0106667 V
β	3.98821e-05 A/V^2	0.000193524 A/V^2	0.000327498 A/V^2
θ	0.0696549 1/V	0.187401 1/V	0.223613 1/V
Leakage current	1.00009e-05 A/um	2.5518e-05 A/um	2.65311e-05 A/um
Subvt	0.194549 V/decade	0.58334 V/decade	0.689965 V/decade

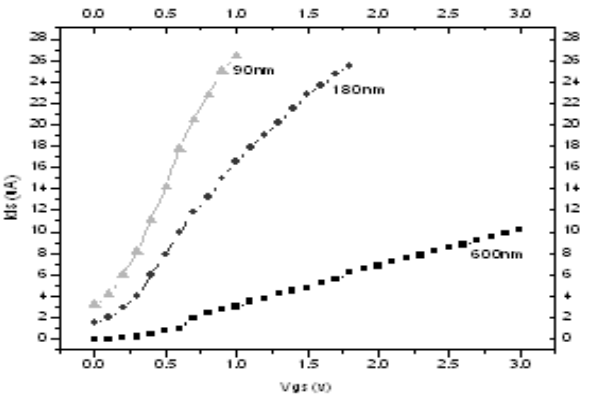

Figure 1. Gate voltage Vs Drain current

With technology scaling, V_{dd} is also scaled down. However, the threshold voltage V_t, cannot be scaled down significantly, since the source/drain subthreshold leakage current, $I_{sd,leak}$ increases sharply with decreased V_t, and it is important to keep $I_{sd,leak}$ with in tolerable limits. Because $I_{d,sat}$ depends on $(V_{dd}-V_t)$, the scaling of V_t tend to reduce and hence to make it difficult to improve the transistor performance [8].

As the technology scales down, gate oxide thickness reduces and electric field increases by which kinetic energy of charge carriers increases due to which charge carriers penetrates in to polysilicon via gate oxide, this increases the gate leakage current. To overcome this phenomenon, dielectric constant of gate oxide should be high. Another reason of degradation in transistor characteristics due to charge trapping, there is rapid shifting in device thresholds which is depend upon the bias voltage. Injection of hot carriers can results in degradation in threshold voltage and transconductance [9].

B. AC Analysis

Fig. 2 shows the capacitance Vs gate voltage with technology variation. Capacitance decreases as the technology scales down. Due to the reduction in capacitance switching speed increases and device performance improves.

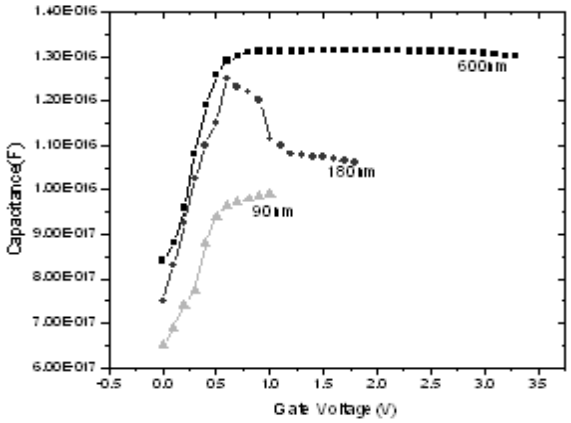

Figure 2. Gate Voltage Vs Capacitance.

Fig. 3 shows transconductance Vs gate voltage with technology variation. This figure shows that transconductance increases at lower gate voltage and decreases at higher gate voltage. For high gain, device can operate at low gate voltage. The transconductance of MOSFET decides its gain and is proportional to hole or electron mobility, at least for low drain voltages. As MOSFET size is reduced, the field in the channel and dopant impurity level increases. Both changes reduce the carrier mobility, and hence the transconductance. As channel length are reduced without proportional reduction in drain voltage, raising the electric field in the channel, this result in velocity saturation in the carriers, limiting the current and the transconductance.

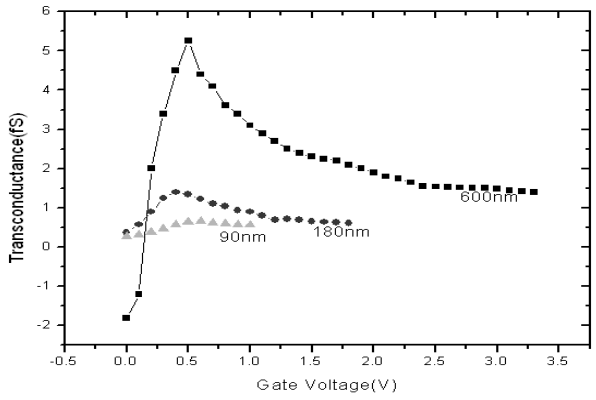

Figure 3. Gate Voltage Vs Transconductance

IV. CONCLUSION

Scaling of NMOS makes it possible to decrease the threshold voltage; it leads the NMOS to take less time to on and off. The different device parameters for low voltage, low power applications have been investigated for the NMOS devices. Threshold voltage is 0.26V at 600nm, 0.04V at 180nm and 0.01V at 90nm. By Scaling down NMOS device, capacitance and transconductance drastically decreases. Improvement in the drain current and transconductance have been observed for NMOS device from 600nm to 90nm showed huge improvement of drain current and transconductance at lower gate voltage in comparison to high gate voltage. Further, the performance of NMOS devices is also studied. Therefore, nanometer range NMOS devices can be very attractive for ultra low power, low voltage applications. Scaling of NMOS device increases drive current, but there is increase in leakage current, this current is responsible for leakage power. As technology scales down, the value of leakage current becomes significant and it cannot be neglected. At 600nm device leakage current is 0.1μA, at 180nm is 0.25μA and at 90nm is 0.26μA. To reduce the leakage current, oxide thickness should be higher. As the device scales down oxide thickness reduces, to compensate this dielectric constant should be higher.

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REFERENCES

[1] Yaur Taur, Douglas A. Buchanan, Wei Chen, David J. Frank, Khalid E. Ismail, Shih-Hsien Lo, George A. Sai-Halasz, Raman G. Viswanathan, Hsing-Jen C. Wann, Shalom J. Wind, Hon-Sum Wong "CMOS Scaling into the Nanometer Regime", proceedings of the IEEE, vol.85, No. 4, pp. 486-504, April 1997.

[2] Shekhar Borkar, "Electronics Beyond Nano-scale CMOS" DAC 2006, pp. 807-808, July 2006.

[3] "Progress in Digital Integrated Electronics" *IEEE*, IEDM Tech Digest (1975) pp.11-13.

[4] Kaushik Roy, Saibal Mukhopadhya, Hamid Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in deep-submicrometer CMOS circuits" proceedings of the IEEE, vol 91, no.2, pp.305-327, 2003.

[5] Chenming HU, "Future CMOS Scaling and Reliability" proceeding of the IEEE, vol.81, No.5, pp.682-689, May 1993.

[6] Siva G. Narendra, Portland, "Challenges and Design Choices in nanoscale CMOS" ACM Journal on Emerging Technologies in Computing Systems, , vol.1, No.1, pp.7-49, April 2005

[7] Y. Taur, T.H. Ning, "Fundamentals of Modern VLSI Devices." Cambridge University Press, New York, 1998

[8] The International Technology Roadmap for Semiconductors, 2007 Edition, executive summary.

[9] Jeffrey Hicks, "Logic Technology Development Quality and Reliability, Intel's 45nm CMOS Technology." Intel Technology Journal, vol.12, Issue 2, pp. 41-54,17 June, 2008.