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New harmonic mitigation scheme for modular multilevel converter – an experimental approach

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Abstract: The multilevel converter has been brought into limelight in this study; however, particular attention has been provided to the form and function of modular multilevel converter (MMC) with new controller to mitigate the circulating currents and harmonics present in the system. Till date, research in this field is very limited with circulating currents and harmonics as the major problem. The stability analysis of proposed controller has been derived and analysed with its experimental results. The system is examined before and after application of controller and results is analysed. This article effectively addresses the problem with prototype of 1 KVA implementation and attempts to make a detailed analysis with their functions in comprehensive manner with HVDC application under different conditions. Also, the applicability of zero voltage switching at turn on, zero current transition at turn off has been verified experimentally. Computer simulations and experiment on a 50 Hz power supply show that the new controller is effective and easy to implement for modular multilevel inverters.

1 Introduction

Many investigations in the field of modular multilevel converters (MMCs) have led to successful operation in high-voltage DC (HVDC) systems. In recent times, in the power transmission era, very-long distances HVDC transmission lines-based current source converters (CSC) and voltage-source converters (VSC) offered more economic and cost-effective power transmission. However, recently HVDC transmission systems based on VSC's have received increasing attention owing to many opportunities like the grid access of weak AC networks, independent control of active and reactive power, supply of passive networks and black start capability, high dynamic performance and small space requirements. In particular, the novel power converter topology for MMC has been intensively researched and developed, valuated by many features like high modularity, simple scalability, low expense of filters, robust control, simple in design and redundancy. This converter is composed by identical power cells connected in series, each one build up with standard components, enabling the connection to high-voltage poles. Although the MMC and derived topologies offer several advantages, they also introduce a more complex design of the power circuit and control goals, which have been the main reasons for the recent and ongoing research. Furthermore, medium-voltage converters are an interesting area for the application of MMCs.

The important features of the multilevel converters are as follows:

- Voltage sharing of the devices is handled automatically by the topology.
- The waveform shape will lead to sinusoidal waveform because of which the total harmonic distortion (THD) is reduced and the harmonics as well.
- The operating voltage of the converters can be increased, instead of connecting the devices in series or in parallel, which makes the system more complex.

The ever increasing demand of industry for stability, adjustability and accuracy of control of power electronic equipment at very-high voltages led to the development of relatively less THD-based modern power electronic static converters. Although solid state power electronic switches, such as the insulated-gate bipolar transistor (IGBTs) have brought notified variance in control techniques, but the main disadvantage is that they produce multiple frequency components called as harmonics. Harmonic voltages can cause an unacceptable disturbance on the supply network and adversely affect the operation of other connected electrical equipment. Hence, there is requirement to reduce the harmonic content to an acceptable level. One should design a converter with proper controllers by keeping THD within limits. Harmonic currents can never be totally eliminated from an electrical system. They can, however, be very significantly reduced by using a harmonic controllers. All power electronic converters produces complex waveforms, that can be resolved into a series of sinusoidal waves of various frequencies, hence any complex waveform is the sum of a number of odd or even harmonics, that can be eliminated by designing the proper controller by tuning to the distorted frequencies.A new transformer less four-leg topology is suggested for shunt compensation [1]. In 'accelerated model of MMCs in PSCAD/EMTDC' [2] and

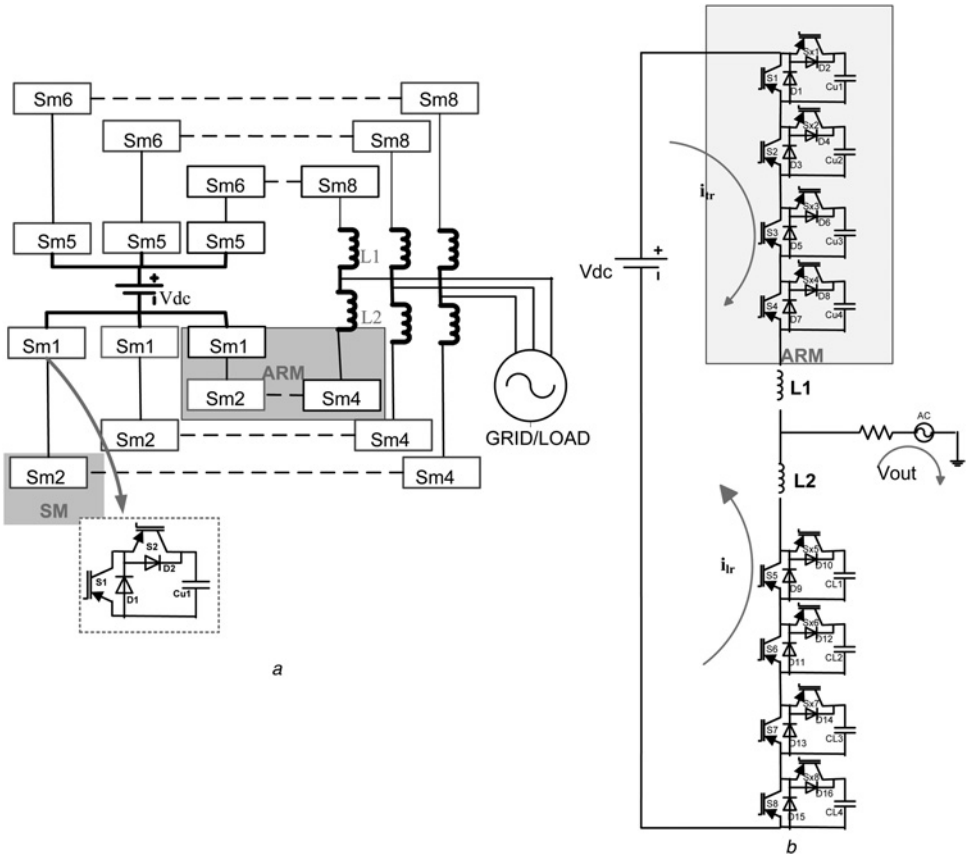

Fig. 1 *Basic circuit topology*

a Three phase five level MMC
b Expanded MMC for a '*R*' Phase leg

in 'high-power MMCs, with silicon carbide (SiC) JFETs' [3], the possibility of building a MMC using SiC switches has been studied. In [4], the MMC is based on the cascaded connection of identical sub modules (SMs) enabling additional redundancies. In [5], the configuration of the MMC topology with redundant SMs is proposed and the effects of active redundancies are demonstrated. In [6], it is mentioned that the MMC has become an increasingly important topology in medium- and high-voltage applications. In [7], the various configurations of a multilevel modular capacitor-clamped converter (MMCCC) are presented, and it also reveals many useful and new formations of the original MMCCC for transferring power in either an isolated or no isolated manner. In [8], it proposes a novel topology of a multilevel modular capacitor-clamped DC–DC converter. In [9], it provides the idea of voltage balancing of the capacitors of different SMs comprising the converter. In [10], it proposes a modulation strategy for the MMC which provides the voltage balancing of the capacitors of different SMs comprising the converter. In [11] it states that HVDC transmission systems are becoming increasingly popular when compared with conventional AC transmission. HVDC VSCs can offer advantages over traditional HVDC CSC topologies, and as such, it is expected that HVDC VSCs will be further exploited with the growth of HVDC transmission. In [12], the modular multilevel cascade converter (MMCC) family based on cascade connection of multiple bidirectional chopper cells or single-phase full-bridge cells are discussed. In [13], a discussion on new AC/AC modular multilevel topology for connecting two three-phase systems is provided. The operating principle is explained, and characteristic waveforms are given. In [14], it is clearly mentioned that an onshore horizontal axis wind turbine, generator and converter are usually in the nacelle on the top of the tower, while the grid step-up transformer is placed at the bottom. Also, a new AC/AC MMC [15] (M^2LC) family is expected to be introduced. The new concept stands out because of its modularity and superior control characteristics. Multilevel voltage-source converter topologies are widely used today in high-power applications such as medium-voltage drives [16]. On the other hand, studies on matrix converters (MCs) have been mainly limited to the low power range. A MMCC based on double-star bridge-cells is expected to be one of the next-generation medium-voltage pulse-width modulation converters intended for grid connections [17, 18]. In [19–21], it proposes different harmonic mitigation techniques for MMC's. In MCs, M^2LC, MMCC and MMCCC, the mitigation of harmonics by using controllers is a quite complex but mitigation of harmonics in MMC is under different conditions can be easily achieved.

This paper is organised in six sections. In Section 1, it introduces about the MMC and its literature survey. In Section 2, it shall be discussed about the proposed circuit and its operation. In Section 3, the controller design and its stability analysis. In Section 4, it shall discuss about the switching schemes and its implementation. In Section 5, the application of proposed technique to HVDC is discussed. In Section 6, it shall discuss about the simulation and experimental results and in the last section, the conclusion has been provided.

Table 1 Basic switching operation of a five level MMC

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	State
+*Vdc*/2	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	+*Vdc*/2
+*Vdc*/4	1	1	1	0	1	0	0	0	0	0	0	1	0	1	1	1	+ *Vdc*/4
	1	1	1	0	0	1	0	0	0	0	0	1	1	1	0	1	
	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	0	
	0	1	1	1	1	0	0	0	1	0	0	0	0	1	1	1	
0	1	1	0	0	1	1	0	0	1	0	1	0	1	1	0	0	0
	1	1	0	0	0	1	1	0	1	0	1	0	0	1	1	0	
	1	1	0	0	0	0	1	1	1	0	1	0	0	0	1	1	
	1	1	0	0	1	0	0	1	1	0	1	0	1	0	0	1	

2 Proposed circuit and its operation

The basic circuit topology is shown in Fig. 1*a*. It is a three phase five level MMC having four SMs in upper limb and four SMs in lower limb. Each SM basic circuit is shown in dotted lines of Fig. 1*a* and expanded circuit shown in Fig. 1*b*. This circuit mainly consists of an inductor having self-inductance L_1 and L_2. Each module consists of main switch S_1 and auxiliary switch Sx_1 with their anti-parallel diodes D_1 and D_2, respectively. Main switch and auxiliary switch consists of a capacitor connected in parallel as C_{u1}.

It has been considered the five level MMC for validation. The basic switching operations have been shown in Table 1 for some operating states. The top four switches in '*R*' phase limb is considered as S_1, S_2, S_3, S_4 and the bottom four switches considered as S_5, S_6, S_7, S_8 of a single leg. Whereas the auxiliary switches are in anti-operation of main switches provided with delay, which will be explained in subsequent sections. In Table 1, it shows the switching states of a MMC. Here, switch ON condition is indicated by '1' and '0' indicates the OFF condition of a switch. It mainly consists one state of 'V/2'output voltage, '16' states of 'V/4' output voltage and '16' states of '0' voltage condition. In Table 2, it shows the basic operation of some redundancies switch state condition of upper limb of a phase. In Table 3, it shows the capacitor charging status of an upper limb of a phase. The modified module has been presented in Fig. 3. This circuit mainly consist of a transformer having self-inductance L_1 and L_2 with an assumption of the coefficient of coupling $M = 1$. It has main switch S_1 and auxiliary switch S_2 with their anti-parallel diodes D_1 and D_2, respectively. Main switch and auxiliary switch consists of a capacitor connected in parallel as C_{u1} and C_{u2} to provide soft switching operations. Whereas the auxiliary switches are in anti-operation of main switches provided with delay, which will be explained in subsequent sections.

Table 2 Basic switching operation of a redundance switching state in mmc

State	Current	Switching	Capacitor	Capacitor
1010	$i_r > 0$	S_1 D_2 S_4 D_3	$Cs_2 \uparrow$	$Cs_4 \downarrow$
1010	$i_r < 0$	S_2 D_1 S_3 D_4	$Cs_4 \uparrow$	$Cs_2 \downarrow$
0110	$i_r > 0$	S_2 D_1 S_4 D_3	$Cs_1 \uparrow$	$Cs_4 \downarrow$
0110	$i_r < 0$	S_2 D_1 S_4 D_3	$Cs_4 \uparrow$	$Cs_1 \downarrow$
0101	$i_r > 0$	S_2 D_1 S_3 D_4	$Cs_1 \uparrow$	$Cs_3 \downarrow$
0101	$i_r < 0$	S_1 D_2 S_4 D_3	$Cs_3 \uparrow$	$Cs_1 \downarrow$
1001	$i_r > 0$	S_1 D_2 S_3 D_4	$Cs_1 \uparrow$	$Cs_3 \downarrow$
1001	$i_r < 0$	S_2 D_1 S_4 D_3	$Cs_3 \uparrow$	$Cs_2 \downarrow$

Owing to the uneven voltage distribution in the legs of a phase, circulating currents will flow through the system. It consists of current harmonics which deteriorates the system performance. Here, an attempt is made to derive the current harmonics present in circulating currents and its necessary controller to suppress the same. The instantaneous voltage across the capacitors are denoted as V_{c1}, V_{c2}, V_{c3}, $V_{c4}\ldots V_{cN}$ Also, the voltage distribution across the capacitors is considered as unequal. The current flowing through the *R* phase top limb, bottom limb, circulating current and *R* phase currents are represented by 'it_r', 'i_{lr}', 'i_{cir}' and 'i_r', respectively. In order to find out voltage for the '*R*' phase, Kirchhoff's voltage law (KVL) is applied to Fig. 1*b*. Then the voltage across the *R* phase top limb, 'Vt_r' and resistance, R_{top}, for bottom limb, 'V_{lr}' and resistance, R_{low}, circulating currents, 'i_{cir}', with supply voltage, 'V_{dc}', 'Vnt_r' represents the voltage of limb '*n*', and '*N*' represents the number of modules. Initially, it assumes that the voltage across all SM capacitors are equal and shown in (1)

$$V_{c1} = V_{c2} = V_{c3} = V_{c4} \cdots = V_{cN} \tag{1}$$

Under any switching conditions, the average voltage across the upper arm switches are shown in (2)

$$\frac{V_{C_u}}{N} = \frac{V_{Dc} + \Delta V_{cu}}{N} \tag{2}$$

The total capacitor voltage of the capacitor is shown in (3) and the differential capacitor voltage is shown in the (4)

$$V_{C_u} = V_{c1} + V_{c2} + V_{c3} + \cdots V_{cN} \tag{3}$$

$$\Delta V_{C_u} = \Delta V_{c1} + \Delta V_{c2} + \Delta V_{c3} + \cdots \Delta V_{cN} \tag{4}$$

$$\frac{V_{C_L}}{N} = \frac{V_{Dc} + \Delta V_{CL}}{N} \tag{5}$$

$$V_{CL} = V_{c(N+1)} + V_{c(N+2)} + \cdots V_{c2N} \tag{6}$$

$$\Delta V_{CL} = \Delta V_{c(N+1)} + \Delta V_{c(N+2)} + \cdots \Delta V_{c2N} \tag{7}$$

The circulating currents in the arm inductors consists of both DC and AC components. These AC components are called as the harmonics, since those are rotating with the higher

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Table 3 Basic capacitor switching operation of a redundance switching state in mmc

S_1	S_2	V_{out}	Current	Power	Capacitor
on	off	0	$i_{out} > 0$	S_1	undefined
on	off	0	$i_{out} < 0$	D_1	undefined
off	on	V_{dc}	$i_{out} > 0$	D_2	charge
off	on	V_{dc}	$i_{out} < 0$	S_2	discharge

frequencies in the system

$$i_{\text{cir}} = \frac{i_{\text{dc}}}{3} + \sum_{n=1}^{\infty} \left(i_{acn}\right) \tag{8}$$

$$i_{\text{cir}} = \frac{i_{\text{dc}}}{3} + i_{\text{ac1}} + i_{\text{ac2}} + i_{\text{ac3}} + \cdots i_{acn} \tag{9}$$

In order to derive the circulating voltage and current, we need the output voltage of a single phase from the three phases

$$V_R = \frac{V_{\text{dc}}.m.\sin(\omega_o t)}{2} \tag{10}$$

$$I_R = I_o.\sin(\omega_o t - \varphi) \tag{11}$$

'm' is the modulation index of a signal. Yet again, the actual voltages are shown below

$$V_{\text{acu}} = N.\frac{V_{\text{dc}}}{2}(1 - m.\sin(\omega_o t))(V_{\text{ac}} + \Delta V_{cu}) \tag{12}$$

$$V_{\text{acl}} = N.\frac{V_{\text{dc}}}{2}(1 + m.\sin(\omega_o t)(V_{\text{ac}} + \Delta V_{cl}) \tag{13}$$

Therefore the total voltage is

$$V_{\text{ac}} = V_{au} + V_{aL} \tag{14}$$

$$= \frac{V_{\text{dc}}}{2}(1 - m.\sin(\omega_o t))\left(\Delta V_{cu} + V_{\text{ac}}\right) + \frac{V_{\text{dc}}}{2}(1 + m.\sin(\omega_o t)(V_{\text{ac}} + \Delta V_{cl})) \tag{15}$$

$$V_{au} + V_{aL} = V_{\text{dc}} + \frac{\Delta V_{cu} + \Delta V_{cl}}{2} + \frac{m.\sin\omega_o t.(\Delta V_{au} - \Delta V_{cl})}{2} \tag{16}$$

In order to derive the disturbance voltage for the upper and lower cell capacitors of a leg, that is, ΔV_{cv} and ΔV_{CL}

$$V_{c1} = \frac{1}{C_1}\int i_1(t).\mathrm{d}t \tag{17}$$

$$V_{cu} = \frac{1}{C_v}\int i_u(t).N_u.\mathrm{d}t \tag{18}$$

At this instance

$$i_u = \sum_{n=0}^{\infty} i_{un} \tag{19}$$

$$i_L = \sum_{n=0}^{\infty} i_{Ln} \tag{20}$$

$$N_u = \frac{1 - m.\cos\omega t}{2} \tag{21}$$

$$N_L = \frac{1 + m.\cos\omega t}{2} \tag{22}$$

$$V_{cu} = \frac{1}{C_u}\int \sum_{n=0}^{\infty} i_{un}.\frac{1 - m.\cos\omega t}{2} \tag{23}$$

$$V_{cL} = \frac{1}{C_L}\int \sum_{n=0}^{\infty} i_{Ln}.\frac{1 - m.\cos\omega t}{2} \tag{24}$$

$$C_U = C_1 + C_2 \ldots . C_n \tag{25}$$

$$C_L = C_{n+1} + C_{n+2} \ldots . C_{2n} \tag{26}$$

by considering the currents of the limb

$$i_{au} = i_{\text{dc}} + i_{a1} + \sum_{n=2}^{\infty} i_{\text{ac}}n \tag{27}$$

$i_{au} \rightarrow$ The current present in the phase 'a' upper arm, $i_{\text{dc}} \rightarrow$ DC component of the current, $i_{\text{ac}} \rightarrow$ Fundamental component of the current, $i_{\text{ac}}.n \rightarrow$ Harmonic component of current

$$i_{aL} = i_{\text{dc}} - i_{a1} + \sum_{n=2}^{\infty} i_{\text{ac}}.n \tag{28}$$

$$i_{\text{ac}} = i_{\text{ac}}m.\cos(n\omega t + \varphi_n) \tag{29}$$

$\therefore$ The total current

$$i_a = i_{au} + i_{aL} \tag{30}$$

$$i_a = \left(i_{dc} + i_{a1} + \sum_{n=2}^{\infty} i_{\text{ac}}.n\right) + \left(i_{\text{dc}} - i_{a1} + \sum_{n=2}^{\infty} i_{\text{ac}}.n\right) \tag{31}$$

By considering voltage for 'Nth' module in terms of capacitance

$$i_a = I_o.\sin(\omega t - \varphi) \tag{32}$$

$$= \left(i_{\text{dc}} + i_{a1} + \sum_{n=2}^{\infty} i_{\text{ac}}.n\right) + \left(i_{\text{dc}} - i_{a1} + \sum_{n=2}^{\infty} i_{\text{ac}}.n\right) \tag{33}$$

$$\Delta V_{\text{CU}} = \frac{1}{2C}.N.\int (1 - m.\sin(\omega_o t).\left(\frac{i_a}{2} + \frac{i_{\text{dc}}}{3} + \sum_{n=1}^{\infty} i_{acn}\right).\mathrm{d}t \tag{34}$$

$$\Delta V_{\text{CL}} = \frac{1}{2C}.N.\int (1 + m.\sin(\omega_o t).\left(-\frac{i_a}{2} + \frac{i_{\text{dc}}}{3} + \sum_{n=1}^{\infty} i_{acn}\right).\mathrm{d}t \tag{35}$$

$\therefore$ The total 'R' phase voltage is shown in (36)

$$V_a = V_{aU} + V_{aL} \tag{36}$$

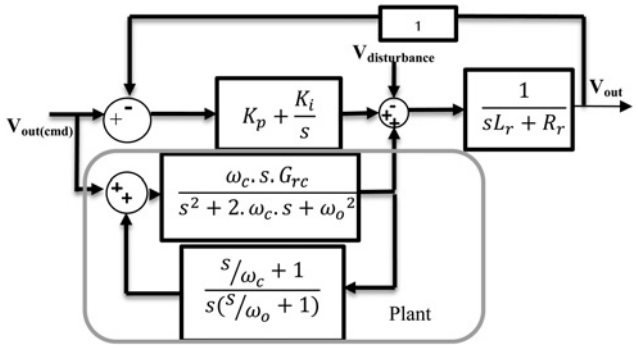

Fig. 2 *Repetitive Controller used for MMC*

By substituting (34) and (35) in (37); we shall have (see (37), (38) and (39) at the bottom of the next page)

From above (40) it concludes that, the system consists of both DC and AC components. Most important issue here is the steady state of a system with controller, if applied. To maintain its fundamental and eliminate the DC and AC components, a controller is needed to be implemented in the system. The controller should be designed so as to be fully suffice the (41) and (42)

$$\left[\int (1 - m\sin\omega_o t)\frac{i_{\rm dc}}{3} + (1 - m\sin\omega_o t).\sum\nolimits_{n=1}^{\infty} i_{acn}\right] = 0 \tag{40}$$

$$=> \frac{i_{\rm dc}}{3} + \sum\nolimits_{n=1}^{\infty} i_{acn} = 0 \tag{41}$$

From the (41) and (42), it is found that, load voltage depends upon the current i_V, difference between upper and lower capacitors; $i_{\rm cir}$ depends only on the DC-link voltage, the sum of the arm voltages.

3 Optimal controller used to compensate the circulating currents

Taking into account the (39), (40) and (41), the designed controller should eliminate both the lower order even harmonics and higher even harmonics, since all odd harmonics are absent and evident. Even though the higher-order harmonics are less in number, as the order of converter increases the effect on system can be noted. Practically the system may be designed for 400 levels or higher. To proficiently eliminate the harmonics from the system a repetitive controller is then added to the system. A repetitive control system is a type of servomechanism for a periodic reference input. In other words, the repetitive control system follows a periodic reference input without steady-state error, even if a periodic disturbance or uncertainty exists in the plant. The optimum values of proportional and integral controller are obtained with the use of the integral square error (ISE) technique and controller shown in Fig. 2*a*. Balancing a system needed to have the net energy transfer to be zero. $\omega_c \rightarrow$ Bandwidth of the controller$Grc \rightarrow$ Gain of the resonant controller, $\omega_o \rightarrow$ Resonant frequency of the controller, $K_{\rm p}$ is the proportional gain and $K_{\rm i}$ is the integral gain of the controller.

3.1 Derivation of proposed controller

The transfer function of controller shown in Fig. 2 can be written as (see (42))

The difference between the command signal and actual signal is error of the controller. The error is specified in (44) (see (43) at the bottom of next page)

3.2 Stability analysis

To define the stability, the eigen values should be in the left-hand side (LHS) side of the locus. Hence, the designed controller should obey the following conditions.

$$= V_{\rm dc} + \left(\frac{\Delta V_{CU} + \Delta V_{CL}}{2}\right) + \left(\frac{m\sin(\omega_o t).\Delta V_{CU} - m\sin(\omega_o t).\Delta V_{CL}}{2}\right) \tag{37}$$

$$= V_{\rm dc} + \frac{1}{2C}.N.\int\left(1 - m.\sin(\omega_o t).\left(\frac{i_{aU}}{2} + \frac{i_{\rm dc}}{3} + \sum\nolimits_{n=1}^{\infty} i_{acn}\right).{\rm d}t + \frac{1}{2C}.N.\int\left(1 + m.\sin(\omega_o t).\left(-\frac{i_{aL}}{2} + \frac{i_{\rm dc}}{3} + \sum\nolimits_{n=1}^{\infty} i_{acn}\right).{\rm d}t\right.\right. \tag{38}$$

$$= \frac{m\sin(\omega_o t).(1/2C).N.\int(1 - m.\sin(\omega_o t).((i_{aU}/2) + (i_{\rm dc}/3) + \sum_{n=1}^{\infty} i_{acn}).{\rm d}t}{2} - \frac{m\sin\sin(\omega_o t).(1/2C).N.\int(1 + m.\sin(\omega_o t).(-(i_{aL}/2) + (i_{dc}/3) + \sum_{n=1}^{\infty} i_{acn}.){\rm d}t}{2} \tag{39}$$

$$V_{\rm out} = \frac{\left(K_{\rm p} + (K_{\rm i}/s)\right) + \left\{((\omega_c.s.G_{rc})/(s^2 + 2.\omega_c.s + \omega_0^2)) + (((s/\omega_c) + 1)/(s.((s/\omega_0) + 1)))\right\}.(1/(R_r + s.L_r))}{1 + \left[\left(K_{\rm p} + (K_{\rm i}/s)\right) + \left\{((\omega_c.s.G_{rc})/(s^2 + 2.\omega_c.s + \omega_0^2)) + (((s/\omega_c) + 1)/(s.((s/\omega_0) + 1)))\right\}.(1/(R_r + s.L_r))\right]}$$

$$V_{\rm out(cmd)} - \frac{(1/(R_r + s.L_r)).V_{\rm disturbance}}{1 + \left[\left(K_{\rm p} + (K_{\rm i}/s)\right) + \left\{((\omega_c.s.G_{rc})/(s^2 + 2.\omega_c.s + \omega_0^2)) + (((s/\omega_c) + 1)/(s.((s/\omega_0) + 1)))\right\}.(1/(R_r + s.L_r))\right]} \tag{42}$$

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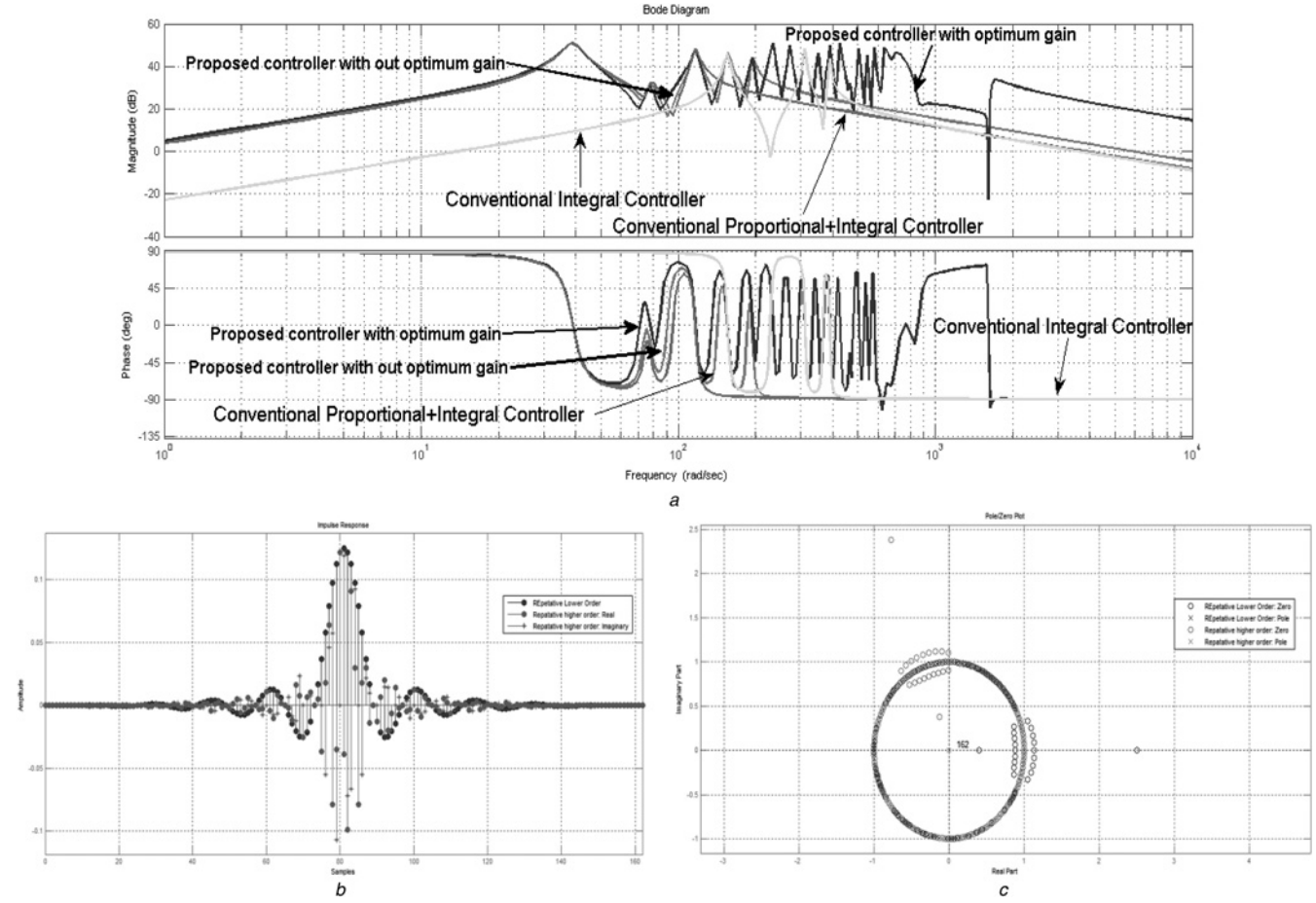

Fig. 3 *Stability analysis*

a Repetitive Controller used for MMC showing magnitude and phase responses
b Repetitive Controller used for MMC showing impulse responses. (*X*-axis-samples and *Y*-axis-amplitude)
c Repetitive Controller used for MMC showing pole/zero responses. (*X*-axis-real part and *Y*-axis-imaginary part)

1. The poles and zeros of polynomial should be within the LHS of the locus.
2. The zeros of polynomial, which is shown in (44) should be in LHS side.

From [17], the stability condition has been designed as follows. The characteristic polynomial equation for which the system should be in stable condition as shown in (45) (see (44))

The pole and zero plot for the characteristic equation is shown in Fig. 3*c*, in which all poles and zero's are lying in LHS side, so it can concludes that the proposed controller is completely stable.

The stability of controller has been checked by further providing different inputs such as impulse. By providing the impulse input, which is assumed as sudden change in load for practical condition; the response is shown in Fig. 3*b*, in which it has been checked with lower and higher order. From this, it is evident that controller reaches steady state for impulse conditions. Hence, it can conclude that the proposed controller is stable for worst conditions as well. The proposed controller stability further analysed with different conditions by plotting the magnitude and phase response as shown in Fig. 3*a*. Primarily, the system is analysed with proportional controller without optimum gain and then with optimum gain. System with optimum gain shows better response compared without optimum gain. But, it's consisting of steady state error. In order to reduce

$$V_{\text{out(cmd)}}-V_{\text{out}}=\frac{V_{\text{out(cmd)}}+\left(1/(R_r+s.L_r)\right).V_{\text{disturbance}}}{1+\left[\left(K_{\text{p}}+(K_{\text{i}}/s)\right)+\left\{\left((\omega_c.s.G_{rc})/(s^2+2.\omega_c.s+\omega_0^2)\right)+\left(((s/\omega_c)+1)/\left(s.\left((s/\omega_0)+1\right)\right)\right)\right\}.\left(1/(R_r+s.L_r)\right)\right]} \tag{43}$$

$$T(s)=\left[\left(1+\left(K_{\text{p}}+\frac{K_{\text{i}}}{s}\right).\left(\frac{1}{R_r+s.L_r}\right)\right)\right]\left[\frac{\left((\omega_c.s.G_{rc})/(s^2+2.\omega_c.s+\omega_0^2)\right)+\left(((s/\omega_c)+1)/\left(s.\left((s/\omega_0)+1\right)\right)\right)}{1+\left(K_{\text{p}}+(K_{\text{i}}/s)\right)\left(1/(R_r+s.L_r)\right)}\right]\left(\frac{1}{R_r+s.L_r}\right) \tag{44}$$

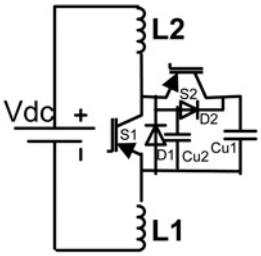

Fig. 4 *Modified SM used in MMC under ZVCTS conditions*

Table 4 Design of inductor and capacitor under ZVCTS condition

Design of capacitor	Design of inductor
C_{u1} and C_{u2} should be selected based on the value of L_1 and L_2 taking in to account the resonance condition.	the value of L_2 can be selected in such a way that $(V_{out}/L_{S2}).t_{rS2} \leq I_{maxin}$ the value of L_{S1} can be selected in such a way that $L_{S1} = 2*L_2$

the system steady-state error, it has been implemented an inner integral controller by which it ensures the steady-state error. However, comparatively, system with optimum gain is giving better results. However, the proportional and integral controllers has not been effective for all frequencies and may system became unstable, hence to maintain stability it introduced an inner second order resonant controller which ensures the system stability as shown in Fig. 3*a* at all frequencies. The optimum values for the controller was obtained by the ISE technique with circulating currents as an objective function as shown in (42).

4 ZVCTS-based switching scheme in MMC by using proposed scheme

A new switching losses mitigated SM scheme is proposed for MMC is shown in Fig. 4.

The active snubber circuit, proposed, is discussed in the aspects of design and validation for a five level MMC. Furthermore, it provides a zero voltage transition (ZVT) at turn-on and zero current transition (ZCT) at turn-off for switch 'S_1'. Again zero current switching at turn ON for a auxiliary switch 'S_2' and ZCT at turn-off will be achieved.

4.1 Assumptions

(i) If I_{S2}(current passing through the switch S_2) increases, resonance will occur in between $L_1 - C_{u1} - L_2$. If S_2 conducts, then, resonance will occur in between $L_2 - C_{u2} - L_1$ and will achieve ZCS.
(ii) A resonance will occur in between C_{u1}-L_1-L_2-C_{u2} then the condition of ZVS will be achieved.
(iii) If S_2 is in conducting state, it leads to a conduction of a resonant current between L1-L2-C_{u1}, Where ZVT kept turned on for S_1.

4.2 ZVT turn ON and ZCT turn OFF for S_1

1. First, turn ON the Switch 'S_2', then the capacitor C_{u1} discharges its energy because of which the capacitor 'C_{u2}'

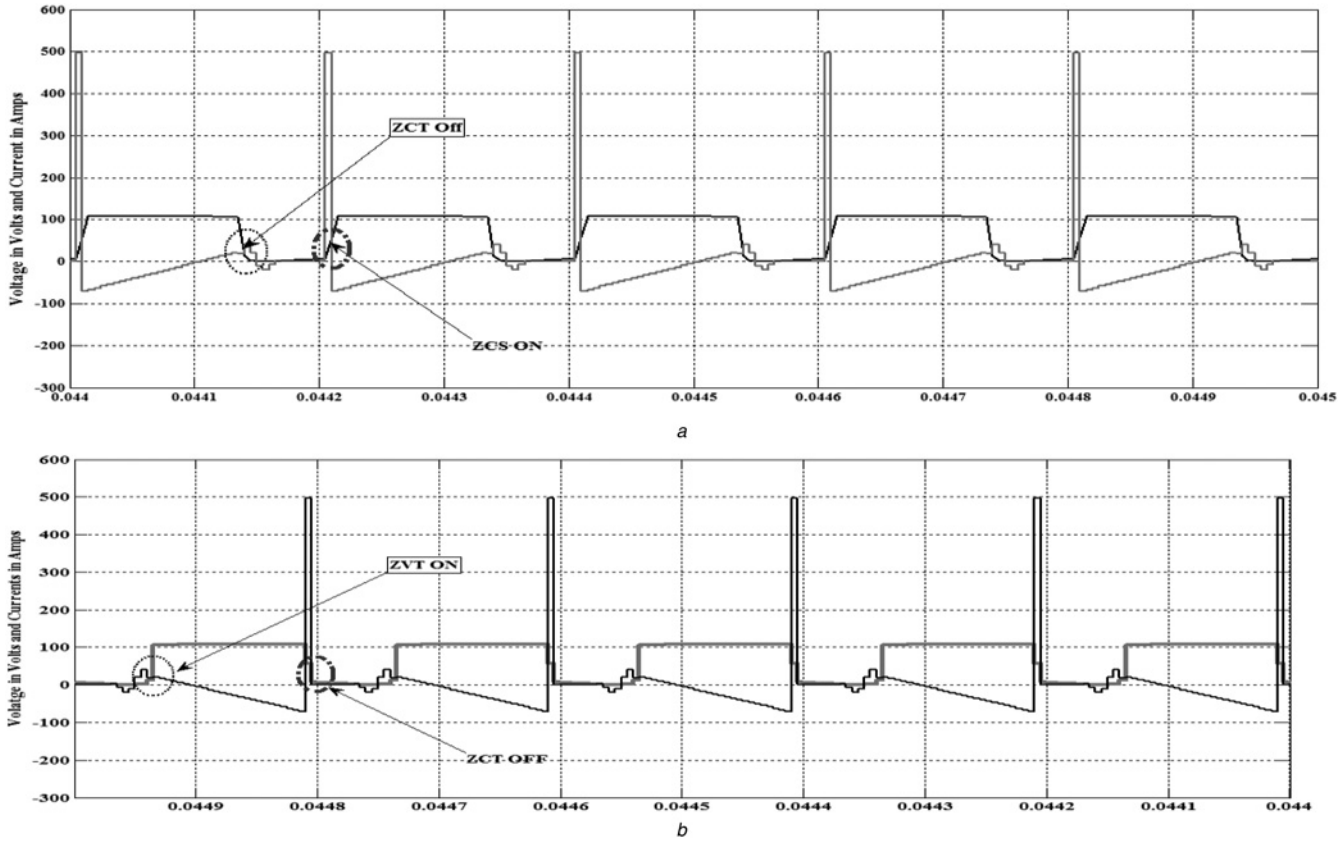

Fig. 5 *ZVT and ZCT*

a ZVT turn on and ZCT turn off condition for switch S1
b ZCS turn ON and ZCT turn OFF condition for S_2

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and 'L_2' will get charged. Owing to coupling effect, the primary winding will also get transferred and instantly energy will concentrate on L_1-C_{u1}-L_2 which leads to response. This is the ideal time to switch on 'S_1'. This signal can be applied as along as the C_{u1} completely discharges. Thus emerges the ZVT.

2. Although the switch 'S_1' conducts the current, the signal is applied to the switch 'S_2' for creating a resonance current higher than that of an input current. At this time, current is always zero. Therefore 'S_1' can be cancelled and ZCT can be possible for the same time, as shown in Fig. 5*a*.

4.3 ZCS turn ON and ZCT turn OFF for S_2

1. When the switch 'S_1' gets suddenly switched OFF, the resonance conduction will take place. Resulting in the application of ZCS.

2. Although turning OFF, 'S_2' current should reach to zero with a resonance. Hence, ZCT can be provided here and shown in Fig. 5*b*.

The values of capacitor and inductor have been selected as per Table 4.

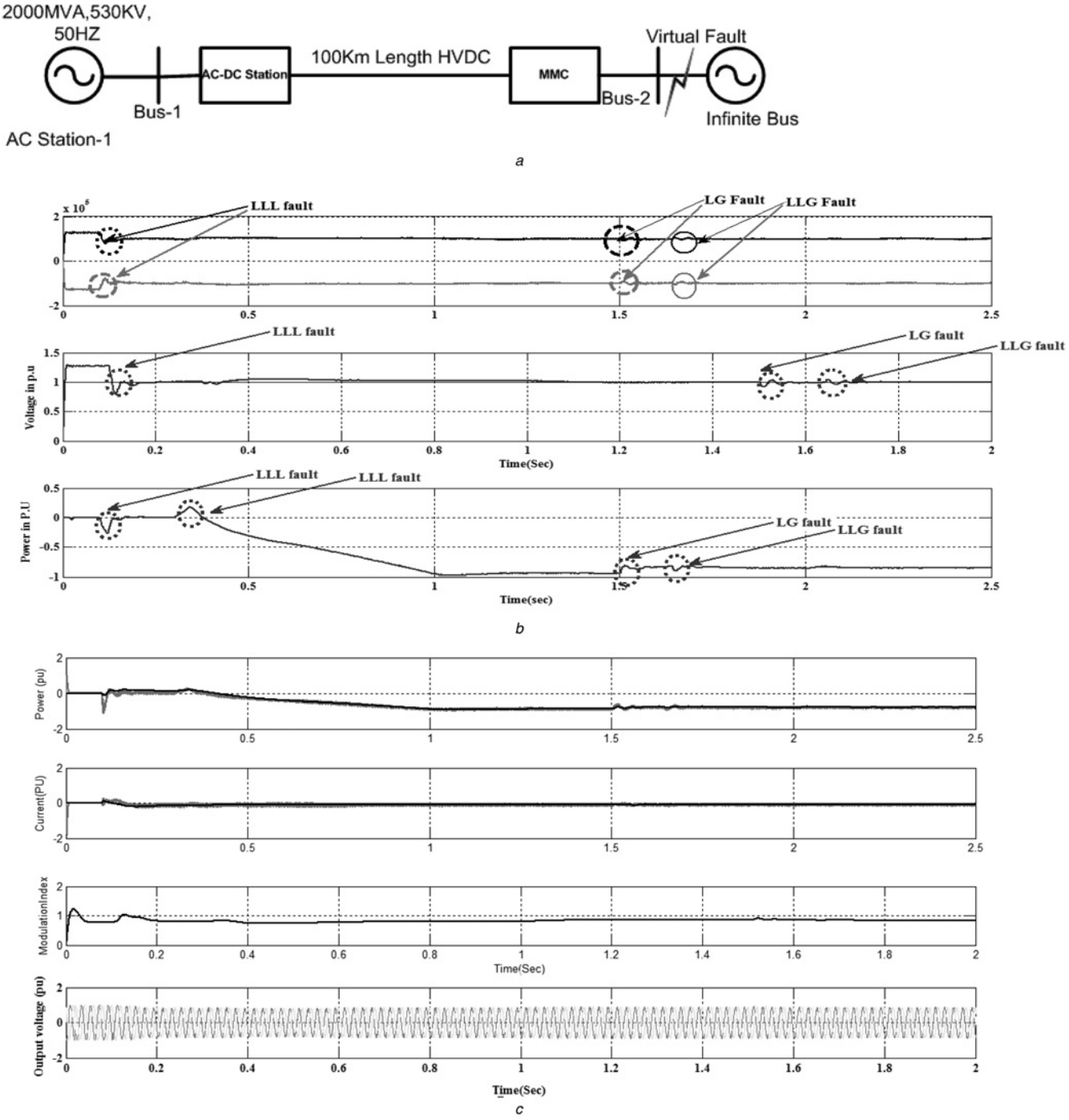

Fig. 6 *HVDC line with the power capacity of 2000 MVA, 530 KV, 50 Hz*

a HVDC Block diagram
b System verification by applying different faults at different time
c System verification by different faults for change in modulation index

Table 5 Optimum gain for proportional and integral controller

Five level MMC	Optimum integral controller gain of K_i*	Optimum proportional controller gain Kp*
1% step load for $m = 1$	1.4	3.6
10% step load	2.4	1.8

Table 6 Parameters used for five level MMC simulation and experiment

MMC Level	Five
DC Voltage	$V_{dc} = 200$ V Dc
circulating current reference	$I_{cref} = 0$
arm inductors	$L_1 = L_2 = L = 3$ mH
switching frequency	$S_f = 100$ Hz
capacitor value	$C = 16$ μF/400 V
bandwidth of the controller	$\omega_c = 2000$
load parameters	$L_r = 10$ mH/$R_r = 30$ Ω
gain of resonant controller	$Gr_c = 1250$
resonant frequency of controller	$\omega_0 = 2000$

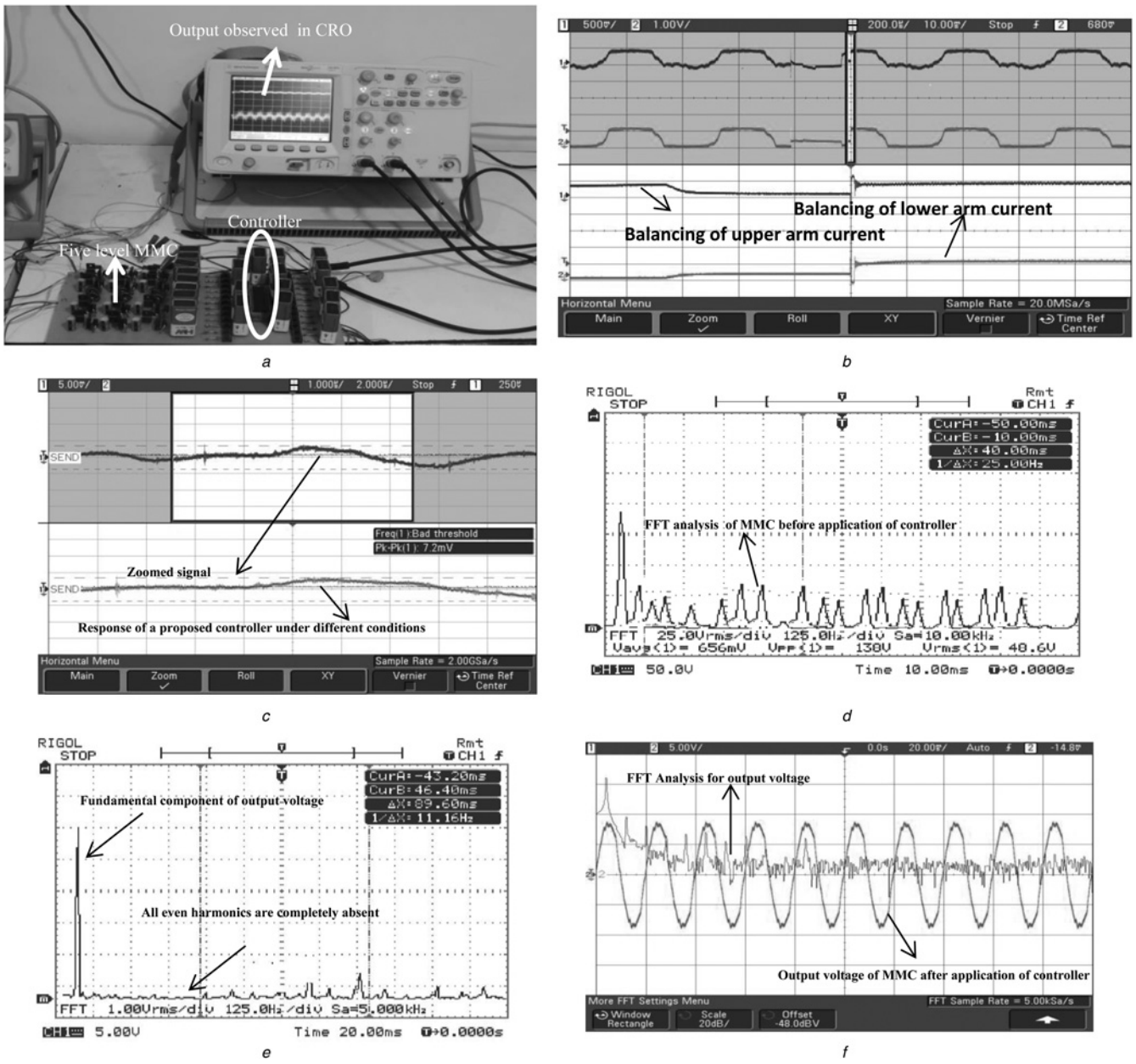

Fig. 7 *Experimental setup*

a Experimental setup for five level MMC
b Circulating current control for upper and lower arms
c Response of a proposed controller for bounded input
d Output voltage FFT analysis of MMC before application of controller
e FFT analysis in time domain after application of controller
f Output voltage and its FFT analysis in frequency domain after application of controller

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5 Application of proposed scheme

The proposed scheme is developed and applied to HVDC transmission system with consideration of fault conditions. For this case, a HVDC line having parameters as 100 Km length, HVDC line with the power capacity of 2000 MVA, 530 KV, 50 Hz is considered as shown in Fig. 6*a*. The system is investigated for different conditions as explained below: The HVDC system is connected to grid with experimental verification of MMC. A virtual fault condition is created at three different conditions as LLL, LLG and LG faults and investigation results are as follows.

The AC voltage step 10% is applied at $t = 0.2$ s during 0.14 s. The above results clarifies that the active and reactive power deviation from the pre-disturbance is less than 0.09 and 0.2 pu, respectively. The recovery time is less than 0.3 s and the steady state is reached before next perturbation initiation. The LLL fault is applied at $t = 1.5$ s during 0.9 s. Consequently results in the active and reactive power deviation from the reference. During the three-phase fault, the transmitted DC power is almost halted and the DC voltage tends to increase (1.2 pu) since the DC side capacitance is being excessively charged. The proposed controller in the active power control at AC attempts to limit the DC voltage within a fixed range. The system recovers well after the fault, within 0.5 s damped oscillations are negligible in the reactive power. The systems with different conditions are shown in Figs. 6*b* and *c* which are self-explanatory. At different loading condition's, the output, capacitor voltages and inductor currents are shown in Fig. 6*c*, respectively, and it is evident that, system is running ideally without any significant losses.

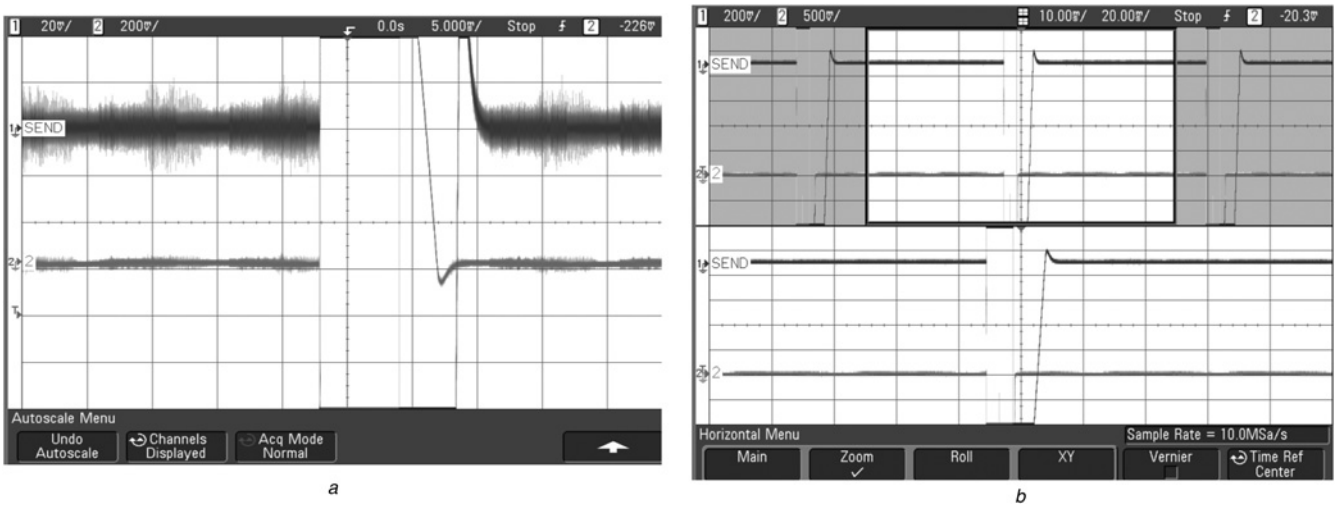
6 Simulation and experimental results

In order to test the proposed method for mitigating the circulating currents of the MMC, computer simulation is carried out first and then verified experimentally as well.

The system has been tested with the parameters listed in Tables 5 and 6. The experimental setup has been shown in Fig. 7*a*. It has been developed a model, with proposed controller which is suitable for wide range of load with different modulation index.

Firstly, System has been investigated before and after application of controller. Before application of controller, the system consist of even and odd harmonics with THD of 34.2% as shown in Fig. 7*d*. Although after application of controller, THD has been reduced to 1.2% which is far better than the specified in standard's by maintaining all even and odd harmonics are completely absent as shown in Fig. 7*e*. From this, it is evident that system with controller is giving better harmonic mitigation for wide range of frequencies. The output voltage and its FFT (Fast Fourier Transform) analysis in time domain and frequency domain have shown in Figs. 7*e* and *f*, respectively. From Fig. 7*d* it shows that all lower order harmonics and even harmonics are present by maintaining its fundamental harmonic component. Since, it is one of the important factors to access the controller performance. In order to test the stability of controller experimentally, it has been given a sudden step load of 10% of actual load and limits of controller observed are in bounded region as shown in Fig. 7*c*. Further, the upper and lower arm currents are stabilised perfectly as shown in Fig. 7*b* and hence circulating currents are absent in the system because of which losses are reduced. The root mean square (RMS) values of phase to neutral current are 31.4 A with controller and 29.2A without controller. From those values it is clear that, output current is also distorted because of circulating currents. Please note that, each division is taken as 5 ms. From the Figs. 8*a* and *b*, it is clear that, ZVCTS operation is verified. Owing to which, the losses in the system is drastically decreased and efficiency has been increased by 14% compared with system without controller. The system is exposed to sudden change in the load of 10% from its actual value at $t = 0.032$ s, because of which a sudden dip in the capacitor voltage happens at $t = 0.033$ s. Suddenly, controller sensed the module voltage and send it's signal to the distorted module and make it's uniform within 0.02 s. Then the controller reaches its steady state in 0.007 s.

At time $t = 20$ ns, the load on the system is suddenly increased by 1%, Then controller receives the signal and reciprocates appropriate signal to module, finally settled at $t = 2$ ns. Then at time $t = 60$ ns, The load on the system is suddenly increased by 10%, then the controller responded quickly and settled with in time $t = 10$ ns. After which, the



a *b*

Fig. 8 *ZVCTS operation*

a ZCS turn ON and ZCT turn OFF condition for S_2
b ZVT turn on and ZCT turn off condition for switch S1

load on the system is then increased suddenly by 30% and it is settled in $t = 12$ ns. From which it is concluded that, as load increases, the controller takes the little time to settle down. All the cases have been shown in Fig. 7*c*. As modulation index changes, accordingly controller response has been observed. From the above analysis, it concludes that, controller can be used for various loads and various modulation indexes. From Fig. 7*b*, it is clear that upper and lower limb current currents are equal and opposite to each other. The circulating currents are completely eliminated, there by the losses in the system has been decreased drastically and efficiency has been increased. The above obtained results are compared with [4], and shown better than those proposed technique.

7 Conclusion

This paper proposed a closed-loop control method for mitigating circulating currents with ZVT and ZCT obtained by a new snubber circuit applied to the MMC. In this article, a new controller scheme has been proposed to mitigate the lower and higher-order harmonics of the system. The stability analysis of proposed controller has been derived and analysed with its experimental results. This scheme shows its effectiveness by theoretical calculations, verified by simulation and experimental results. This article effectively addresses the problem with prototype of 1 KVA implementation and attempts to make a detailed analysis with their functions in comprehensive manner with HVDC application under different conditions. This method is simple in design and can substantially eliminate the RMS value of the circulating current compared with the existing methods in literature, while the voltages of the SM capacitors are kept well balanced. This method is very helpful for reducing power losses of the MMC in real HVDC applications and also verified by experimental results. The proposed system can be applied to wide range of loads with various modulation indexes. The steady-state analysis and harmonics can substantially reduce by the proposed method. Both simulation and experimental results have shown the validity and effectiveness of the proposed method.

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