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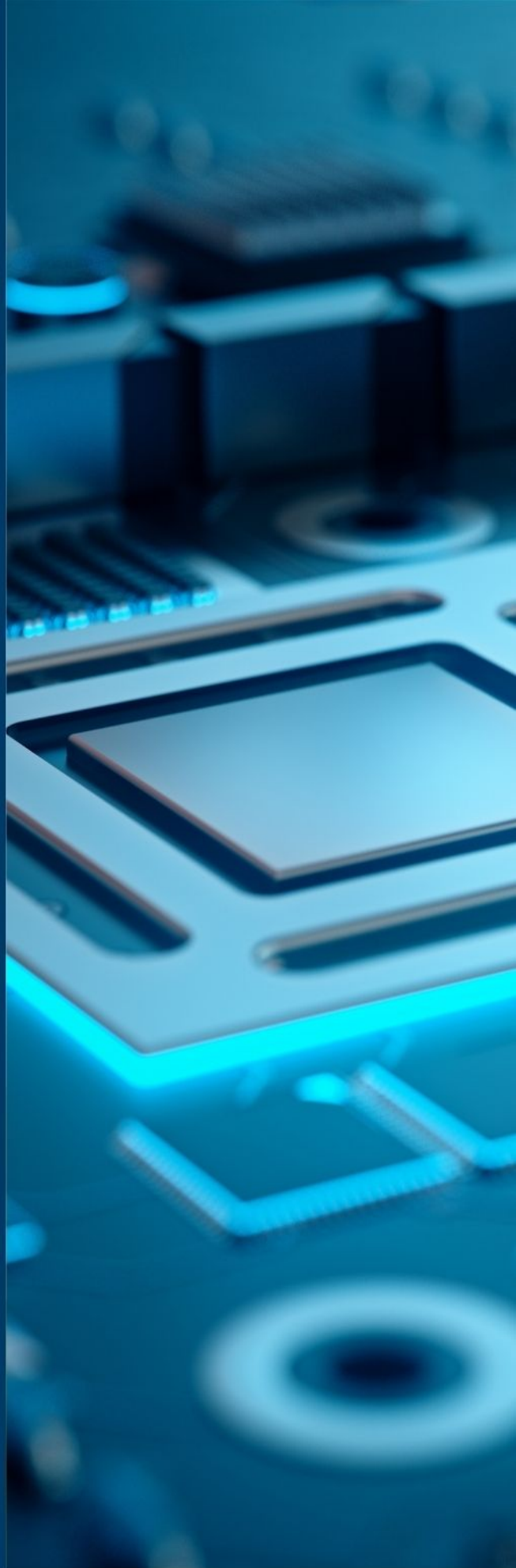
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Analysis and modelling of circulating current in two parallel-connected inverters

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Abstract: Parallel-connected inverters are gaining attention for high power applications because of the limited power handling capability of the power modules. Moreover, the parallel-connected inverters may have low total harmonic distortion of the ac current if they are operated with the interleaved pulse-width modulation (PWM). However, the interleaved PWM causes a circulating current between the inverters, which in turn causes additional losses. A model describing the dynamics of the circulating current is presented in this study which shows that the circulating current depends on the common-mode voltage. Using this model, the circulating current between two parallel-connected inverters is analysed in this study. The peak and root mean square (rms) values of the normalised circulating current are calculated for different PWM methods, which makes this analysis a valuable tool to design a filter for the circulating current. The peak and rms values of the circulating current are plotted for different PWM methods, and a discontinuous PWM is identified which offers the minimum peak and rms value of the circulating current. Experimental results are presented to verify the analysis.

1 Introduction

Parallel-connected voltage source inverters have several advantages, such as low current ripple, modularity, improved thermal management, increased power capability, redundancy and easy maintenance [1–22]. In addition, it has been shown in [7] that the system has high efficiency with the parallel-connected inverters. The parallel-connected inverters have a common dc link, and the ac sides of the inverters are connected through chokes, as shown in Fig. 1. The parallel-connected inverters operation with synchronised pulse-width modulation (PWM) is presented in [22]. However, the parallel-connected inverters operated with the interleaved PWM result in reduction of the ac current ripple. For this case, a detailed analysis for the current harmonics is presented in [8]. The analysis is based on a graphical approach used for a single inverter output current ripple presented in [23, 24]. If the carrier waveforms of the interleaved PWM for two parallel-connected inverters are phase shifted by 180°, the current harmonics because of the switching frequency and its sidebands are cancelled, and a reduction in the ac side current ripple is achieved.

Although the ac side current ripple is reduced, the interleaved PWM causes a circulating current. If there is no interleaving, inverter output voltages of a phase will be in synchronisation. Therefore there is no circulating current. However, in the case of most of the interleaved PWM, the inverter output voltages of a phase will not be in sync, which causes the circulating current between the inverters. The circulating current can be limited by many ways, and few of them are listed below [9]

1. Single phase chokes between the ac terminals of the two inverters that supply the same phase output.
2. Common mode (CM) or inter-phase chokes at the ac side of the inverters.
3. Use of an isolation transformer on the ac side and so on.

The transformer isolation requires a line frequency transformer which is bulky. So, it is not preferred.

The circulating current for sinusoidal PWM (SPWM) [9], discontinuous PWM (DPWM) [11–14], harmonic elimination PWM [15] are analysed in details for the two-parallel-connected inverters. However, a general approach is not presented, and these models are used to design a circulating current controller. A controller presented in [9] controls the circulating current for the inverters operated with two different switching frequencies. The controller presented in [13] adds different CM offsets to the PWM reference signals for the parallel-connected inverters. Similar implementations are presented in [11, 14]. Since these models are developed to design a controller for the circulating current, they are not useful for the filter design of the circulating current. These models do not consider the circulating current behaviour within a switching period. To design the filter, the circulating current within a switching period and averaged over a switching period should be modelled. This paper discusses both of these models.

The paper is organised as follows. The system under consideration is described in Section 2. A model of the system is also presented in Section 2. In addition, the dynamic equation of the circulating current is also derived. Using this equation, an averaged dynamic model of the circulating current is described in Section 3. This model relates the circulating current averaged over a sampling period to the CM offset added to the PWM reference signals. Furthermore, the peak and root mean square (rms) value of the circulating current during a sampling period are calculated in Section 3 for different PWM methods. A DPWM is identified which yields minimum peak and rms value of the circulating current. A closed form solution for the peak value of the circulating current for the SPWM, the space vector PWM (SVPWM) and the DPWM are also presented. This can be a useful tool to design the circulating current filter. It is shown that the circulating current does not depend on the load current. It depends on the PWM method, interleaving angle between carrier signals, and the PWM reference signals. The experimental results are presented in Section 4 to verify the analysis. Conclusions are presented in Section 5.
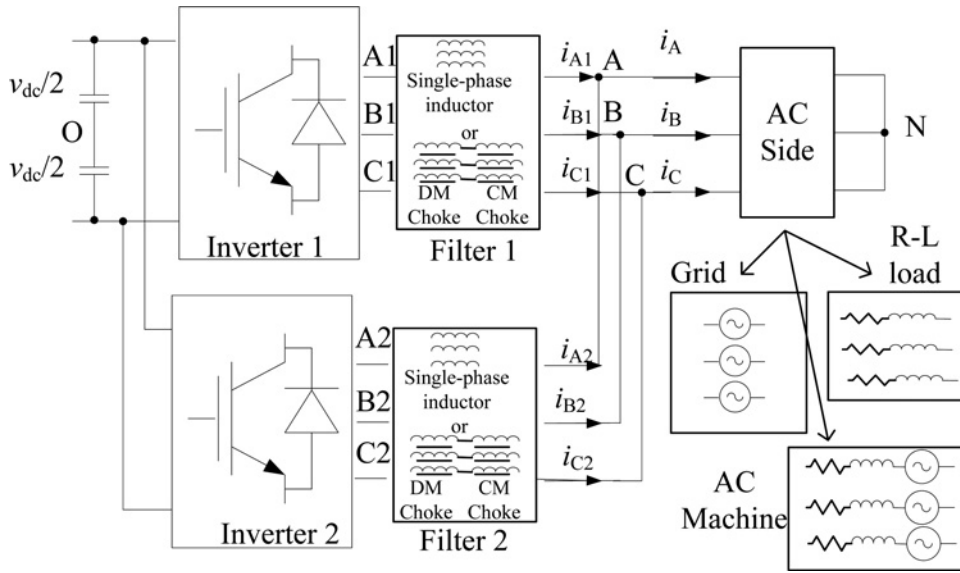
Fig. 1 *Parallel-connected inverter*

2 System model

The block schematics of the two-parallel-connected inverters are shown in Fig. 1. The ac sides of the inverter can be connected to the grid, a passive load, or an ac machine depending on the application. Typically, the ac side inductor may be realised by three single-phase inductors or a series combination of a three-limb differential mode (DM) and a CM choke. Irrespective of the inductor configuration, the resistance, self-inductance and mutual inductance for a phase can be represented by R, L_s and L_m, respectively. i_{Yx} denotes the inductor current of phase Y of inverter x. The ac side current of phase A, which is the sum of phase A currents of inverter 1 and inverter 2, is denoted by i_A. Similarly, the ac side currents of phases B and C are represented by i_B and i_C, respectively.

To model the system, the dynamic equations for the inductor currents are required, and they can be written as (see (1))

where $v_{cmx} = (1/3)(v_{AxO} + v_{BxO} + v_{CxO})$; and $x = 1, 2$. v_{YxO} represents the pole voltage of phase Y with respect to the fictitious midpoint of the dc link O of the inverter x. v_{cmx} represents the CM voltage of the inverter x. v_{AN}, v_{BN} and v_{CN} represent the ac side load voltage for phases A, B and C, respectively. The dynamic equations for the inductor current are represented in a stationary reference frame, which can be transformed into a rotating $dq0$-reference frame as given by

$$Ri_{dx} + (L_s - L_m)\frac{d}{dx}i_{dx} - \omega(L_s - L_m)i_{qx} = v_{dx} - e_d$$

$$Ri_{qx} + (L_s - L_m)\frac{d}{dx}i_{qx} + \omega(L_s - L_m)i_{dx} = v_{qx} - e_q \qquad (2)$$

$$Ri_{0x} + (L_s + 2L_m)\frac{d}{dx}i_{0x} = v_{cmx} - \frac{1}{2}\left(v_{cm1} + v_{cm2}\right)$$

where d, q and 0 subscript represent the d-, q- and 0-axis components of a variable. For example, v_{dx} represents the d-axis component of the pole voltages (v_{AxO}, v_{BxO} and v_{CxO}) of the inverter x. e_d and e_q represent the

d- and q-axis components of the ac-side load voltage. The 0-axis component of the ac-side load voltage will be zero since a balanced load condition is assumed. However, (2) shows that the 0-axis component of the inductor current, which is the average of inductor currents of an inverter, is not zero and depends on the CM voltages of both inverters. In addition, the i_{0x} does not affect the dynamic equations of the d- and q-axis components of the inductor currents.

To determine the total system dynamic behaviour, the dynamic equations for the ac-side currents are required in $dq0$-reference frame, which can be obtained by adding the respective axis inductor current dynamic equations of both inverters. The dynamic equations for the ac-side currents are given by

$$Ri_d + (L_s - L_m)\frac{d}{dt}i_d - \omega(L_s - L_m)i_q = v_d - 2e_d$$

$$Ri_q + (L_s - L_m)\frac{d}{dt}i_q + \omega(L_s - L_m)i_d = v_q - 2e_q \qquad (3)$$

$$Ri_0 + (L_s + 2L_m)\frac{d}{dt}i_0 = 0$$

where i_d is the d-axis component of the ac-side current, and it is equal to the sum of i_{d1} and i_{d2}. Similarly, i_q, i_0, v_d and v_q are sum of i_{q1} and i_{q2}; i_{01} and i_{02}; v_{d1} and v_{d2}; and v_{q1} and v_{q2}; respectively. The sum of the 0-axis current is zero since the ac-side load is a three-wire load. So, $i_{01} = -i_{02}$. In other words, the 0-axis components of the inductor currents do not contribute to the ac-side currents and circulate between inverters. Thus, it can be termed as the circulating current. It contributes to additional losses and thus should be reduced.

If the resistance of the filters connected to the inverter output is neglected ($R \simeq 0$), the circulating currents can be given by

$$L\frac{d}{dt}i_{01} = -L\frac{d}{dt}i_{02} = \frac{1}{2}(v_{cm1} - v_{cm2}) \qquad (4)$$

where $L = L_s + 2L_m$. If a combination of a DM and a CM chokes is used, $L_s = (2L_{dm} + L_{cm})/3$ and $L_m = (L_{cm} - L_{dm})/3$. L_{dm} and L_{cm}

$$Ri_{Ax} + (L_s + L_m)\frac{d}{dt}i_{Ax} + L_m\frac{d}{dt}i_{Bx} + L_m\frac{d}{dt}i_{Cx} = v_{AxO} - \frac{1}{2}\sum_{k=1,2} v_{cmk} - v_{AN}$$

$$Ri_{Bx} + L_m\frac{d}{dt}i_{Ax} + (L_s + L_m)\frac{d}{dt}i_{Bx} + L_m\frac{d}{dt}i_{Cx} = v_{BxO} - \frac{1}{2}\sum_{k=1,2} v_{cmk} - v_{BN} \qquad (1)$$

$$Ri_{Cx} + L_m\frac{d}{dt}i_{Ax} + L_m\frac{d}{dt}i_{Bx} + (L_m + L_s)\frac{d}{dt}i_{Cx} = v_{CxO} - \frac{1}{2}\sum_{k=1,2} v_{cmk} - v_{CN}$$

represent the inductance of the DM and the CM chokes, respectively. If three single-phase inductors are used, $L_s = L_{sp}$ and $L_m = 0$, where L_{sp} is the inductance of the single-phase inductor.

The circulating current is the time integral of the difference of the CM voltages divided by the inductance value. So the circulating current depends on the inductance value, switching frequency and the CM voltage. For a given system, the switching frequency and the inductor configuration are decided by the output harmonics. For a given switching frequency and the inductance value, the circulating current is affected by difference of the CM voltages, which is affected by the PWM methods. Typically, carrier-based PWM methods are used for the inverters, and the phase shift of the carrier signals affect the difference of the CM voltages. The effects of the PWM methods and the phase shift of the carrier signal on the CM voltage, and the circulating current are discussed in the following section.

3 Circulating current

The circulating current depends on the difference of the CM voltages of the parallel-connected inverters. The difference of the CM voltages depends on the reference signals and the carrier signals of the PWM. The paper is focused on the case of the most commonly used triangular carrier signals. The reference signal generation considered for the paper is discussed in the following subsection.

3.1 Circulating current averaged over a sampling period

The parallel-connected inverters are required to generate three-phase balanced sinusoidal voltages as given by

$$v_A = m\frac{v_{dc}}{2}\cos(\omega t)$$
$$v_B = m\frac{v_{dc}}{2}\cos\left(\omega t - \frac{2\pi}{3}\right)$$
$$v_C = m\frac{v_{dc}}{2}\cos\left(\omega t + \frac{2\pi}{3}\right)$$

(5)

where m is the modulation index. To generate this voltage, the reference signals for the PWM can be sampled at the positive peak, the negative peak or both the positive and the negative peaks of the carrier signal. This is also referred to as regular-sampled PWM (RSPWM). If the reference signals are sampled at either the positive or the negative peak of the carrier signal, it is referred to as symmetric RSPWM. If the reference signals are sampled at both positive and negative peaks of the carrier signal, it is referred to as asymmetrical RSPWM. This paper considers asymmetrical RSPWM, as shown in Fig. 2a since it results in the minimum voltage harmonics. The details of the harmonic component can be found in [25], and it is not repeated here. For the asymmetrical RSPWM, the sampling period is half of the switching period (T_s).

If the asymmetrical RSPWM is used for the parallel-connected inverters where the carrier signals are phase shifted by ϕ, the sampling instants of the reference signals for the inverters are shifted accordingly. In this case, phase A reference signals for inverter 1 and inverter 2 are given by (see (6))

respectively, for SPWM. The reference signals for phases B and C are phase shifted by 120° and 240°, respectively. Moreover, a general PWM reference signal can be given by [26]

$$v^u_{Yx,ref} = v_{Yx,ref} + v_{offx}$$
$$Y = A, B, C; \text{ and } x = 1, 2$$

(7)

where u superscript represents the updated PWM reference signals, and v_{offx} is the CM offset added to the reference signals for inverter x. The CM offset for the inverter x (v_{offx}) can be added to change the PWM reference signal without affecting the line-to-line ac-terminal voltage of the inverter. However, the maximum and minimum values of the CM offset for a sampling period is equal to $(v_{dc}/2) - \max(v_{Ax,ref}, v_{Bx,ref}, v_{Cx,ref})$ and $-(v_{dc}/2) - \min(v_{Ax,ref}, v_{Bx,ref}, v_{Cx,ref})$, respectively, and it is possible to apply the CM offset within the range of the maximum and minimum values. A general expression for the CM offset is presented in [26] as a function of a factor k and is given by $v_{offx} = k((v_{dc}/2) - \max(v_{Ax,ref}, v_{Bx,ref}, v_{Cx,ref})) + (1 - k)(-(v_{dc}/2) - \min(v_{Ax,ref}, v_{Bx,ref}, v_{Cx,ref}))$, where $0 \le k \le 1$. The factor k is defined as a factor of the maximum value of the CM offset that can be applied.

The PWM reference signals affect the pole voltages, which in turn affect the circulating current. Using (4), the circulating current averaged over a sampling period can be given by

$$L\frac{d}{dt}\langle i_{o1}\rangle_{T_s/2} = \frac{1}{2}\left(\langle v_{cm1}\rangle_{T_s/2} - \langle v_{cm2}\rangle_{T_s/2}\right) = \frac{1}{2}(v_{off1} - v_{off2})$$

(8)

The difference in the CM offset influences the net change in the circulating current in a sampling period. If the difference of the CM offset is zero, the net change in the circulating current will be zero and vice versa. As an example, if SVPWM ($k = \frac{1}{2}$) is considered, the difference of the CM offset can be given by

$$v_{off1} - v_{off2} = -0.5(v_{max\,1} + v_{min\,1}) + 0.5(v_{max\,2} + v_{min\,2})$$

(9)

The CM offset of the inverters and their difference are plotted for $\phi = 90°$ and 180° in Figs. 2b and c, respectively. The difference in the CM offset for $\phi = 180°$ is zero because the PWM reference signals are sampled at the same instant for both inverters. It is the instant when the carrier signals of inverter 1 and inverter 2 have their positive and negative peaks, respectively, or vice versa. For other values of phase shift angle ϕ, the PWM sampling instants are not synchronised, and the difference in the CM offset for a sampling period is non-zero similar to the case shown in Fig. 2b. For those cases, there is a net change in the circulating current in a sampling period. Therefore the circulating current contains a low frequency component. Fig. 2b shows that the frequency of the component is three times the fundamental output frequency. This component is absent in the case of $\phi = 180°$.

In addition, another advantage of the 180° phase shift between carrier signals is low total harmonic distortion (THD) in the ac side currents (the sum of the inductor currents of individual phases). It has been shown in [8] that the harmonic component of the ac side current because of the switching frequency and its sidebands is zero for $\phi = 180°$. The first major harmonic component exists at twice the switching frequency. A detailed explanation is given in [8], and it is not repeated in this paper. Therefore, a phase shift of 180° between the carrier signals is considered in this paper for further analysis.

3.2 Peak and rms values of the circulating current

In case of the asymmetrical RSPWM, the PWM reference signals are sampled at the positive and negative peaks of the carrier signals. The positive (negative) peak of inverter 1 carrier signal coincides with the negative (positive) peak of inverter 2 carrier signal because of the 180° phase shift between carrier signals, the PWM reference signals are sampled at the same instant. Therefore the PWM

$$v_{A1,ref}(t) = m\frac{v_{dc}}{2}\cos\left(\omega p\frac{T_s}{2}\right) \qquad p\frac{T_s}{2} < t < (p+1)\frac{T_s}{2}$$
$$v_{A2,ref}(t) = m\frac{v_{dc}}{2}\cos\left(\omega\left(p\frac{T_s}{2} + \frac{\phi}{2\pi}T_s\right)\right), \qquad p\frac{T_s}{2} + \frac{\phi}{2\pi}T_s < t < (p+1)\frac{T_s}{2} + \frac{\phi}{2\pi}T_s$$
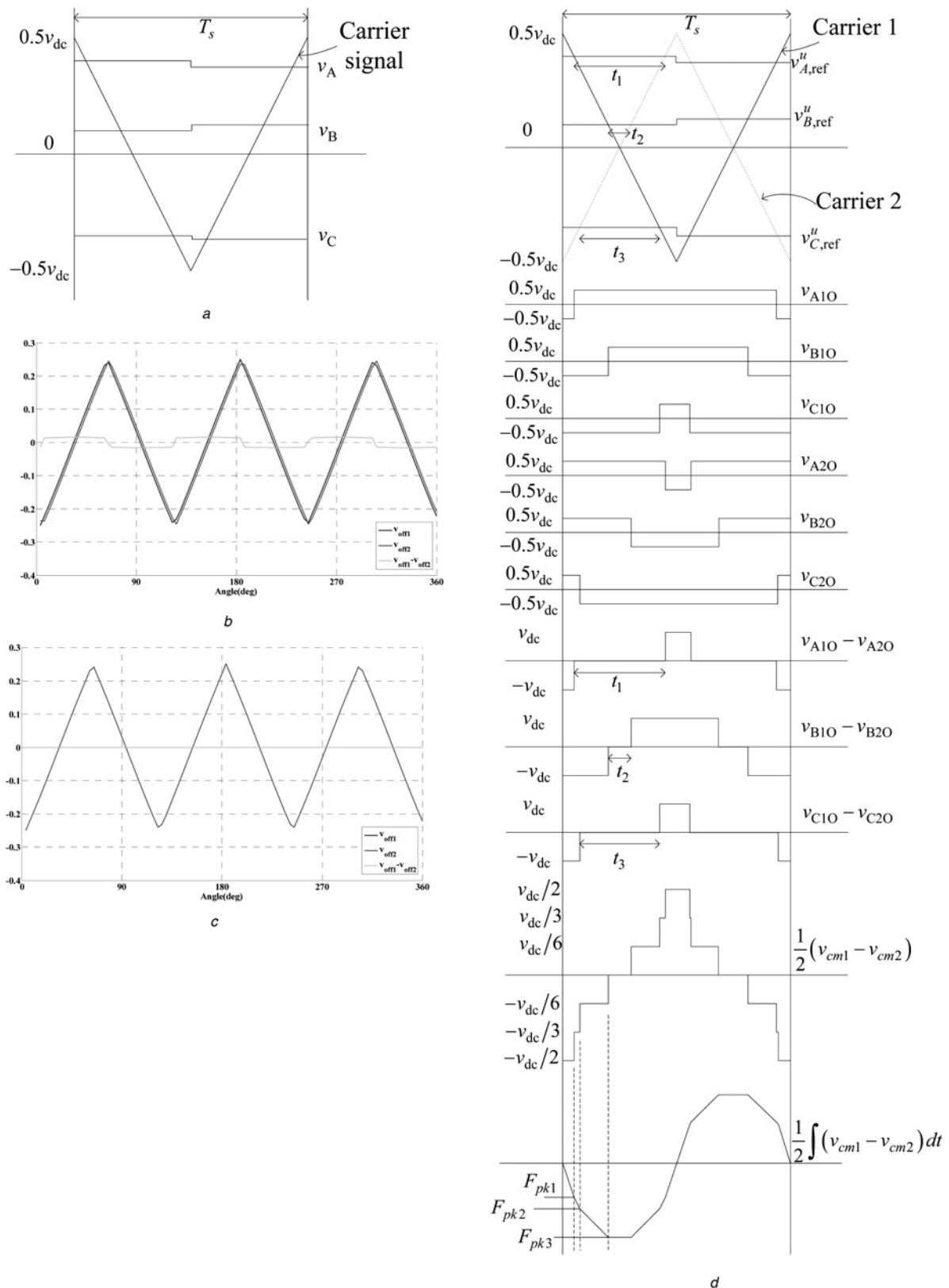
(6)

Fig. 2 *PWM and CM offsets of the inverters and their differences*

a Asymmetrical carrier-based RSPWM
b CM offsets of the inverters and their differences for ø = 90°
c ø = 180°
d PWM voltage waveform and the voltage waveform causing the circulating current

reference signals for the inverters are given by

$$v_{Y,\text{ref}}^{u} = v_{Y1,\text{ref}}^{u} = v_{Y2,\text{ref}}^{u} \tag{10}$$

The reference signals are compared with the carrier signal to generate the PWM output voltages, as shown in Fig. 2*d* for a particular switching period where phase *A* has maximum voltage value, phase *C* has minimum voltage value and phase *B* has middle
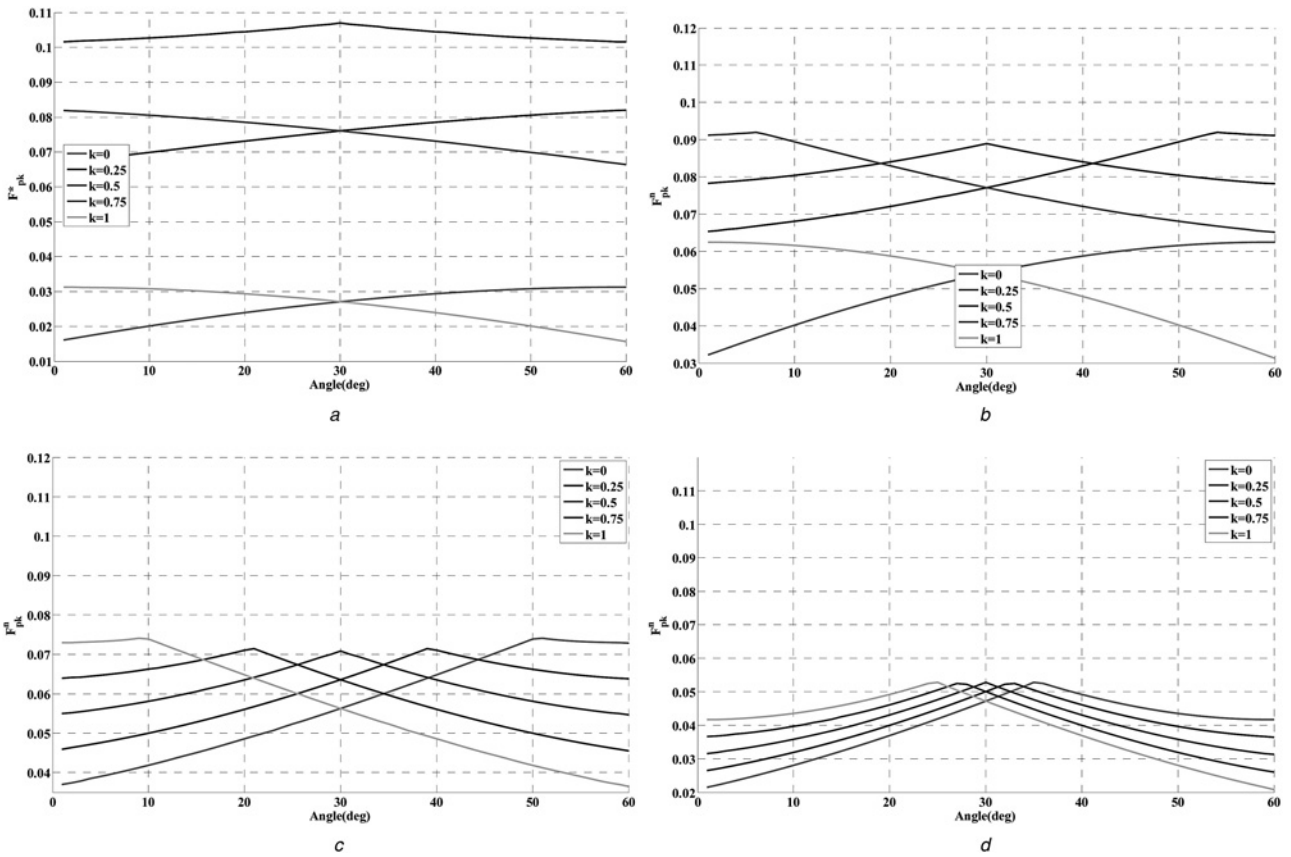
Fig. 3 *Peak value of the normalised circulating current for different CM offset*
a m = 0.25
b m = 0.5
c m = 0.75
d m = 1.0

voltage value. The difference in phase *A* pole voltages ($v_{A1O} - v_{A2O}$) is zero for the time t_1, which can be given by

$$t_1 = \frac{v_{A,\text{ref}}^u}{v_{\text{dc}}} T_s \tag{11}$$

Similarly the time, when the difference in phase *B* pole voltages and the difference in phase *C* pole voltages are zero, can be given by

$$t_2 = \frac{v_{B,\text{ref}}^u}{v_{\text{dc}}} T_s \tag{12}$$

and

$$t_3 = \frac{-v_{C,\text{ref}}^u}{v_{\text{dc}}} T_s \tag{13}$$

Using (11)–(13), and Fig. 2*d*, the difference in the CM voltages for $0 < t < T_s/4$ can be given as (see (14))

The integration of the difference of the CM voltages is proportional to the circulating current. Since the difference of the CM voltages can have only discrete values $\pm v_{\text{dc}}$, $\pm 2v_{\text{dc}}/3$, $\pm v_{\text{dc}}/3$ and 0, the peak value of the circulating current in a sampling period can be calculated by adding the values obtained by multiplying the discrete values of the CM voltage difference with the time for which it is present assuming that the initial value of the circulating current is zero

$$I_{o,pk} = \frac{v_{\text{dc}} T_s}{4L} \left(\frac{1}{2} - \frac{1}{3v_{\text{dc}}} \left(|v_{A,\text{ref}}^u| + |v_{B,\text{ref}}^u| + |v_{C,\text{ref}}^u| \right) \right) \tag{15}$$

Since the peak value of the circulating current depends on the switching period, inductance and so on, it is normalised so that the system parameters have no effect on the circulating current. The peak value of the normalised circulating current is given by

$$F_{pk}^n = \frac{I_{pk} L}{v_{\text{dc}} T_s} = \frac{1}{8} - \frac{1}{12v_{\text{dc}}} \left(|v_{A,\text{ref}}^u| + |v_{B,\text{ref}}^u| + |v_{C,\text{ref}}^u| \right) \tag{16}$$

The peak value of the normalised circulating current (F_{pk}^n) depends on the sign of the updated PWM reference signals, and it can be different for different values of the CM offset in a

$$\frac{1}{2}\left(v_{\text{cm1}} - v_{\text{cm2}}\right) = \begin{cases} -\dfrac{1}{2} v_{\text{dc}} & 0 < t < \dfrac{T_s}{4}\left(1 - \dfrac{2\left|v_{A,\text{ref}}^u\right|}{v_{\text{dc}}}\right) \\[2ex] -\dfrac{1}{3} v_{\text{dc}} & \dfrac{T_s}{4}\left(1 - \dfrac{2\left|v_{A,\text{ref}}^u\right|}{v_{\text{dc}}}\right) < t < \dfrac{T_s}{4}\left(1 - \dfrac{2\left|v_{C,\text{ref}}^u\right|}{v_{\text{dc}}}\right) \\[2ex] -\dfrac{1}{6} v_{\text{dc}} & \dfrac{T_s}{4}\left(1 - \dfrac{2\left|v_{C,\text{ref}}^u\right|}{v_{\text{dc}}}\right) < t < \dfrac{T_s}{4}\left(1 - \dfrac{2\left|v_{B,\text{ref}}^u\right|}{v_{\text{dc}}}\right) \\[2ex] 0 & \dfrac{T_s}{4}\left(1 - \dfrac{2\left|v_{B,\text{ref}}^u\right|}{v_{\text{dc}}}\right) < t < \dfrac{T_s}{4} \end{cases} \tag{14}$$
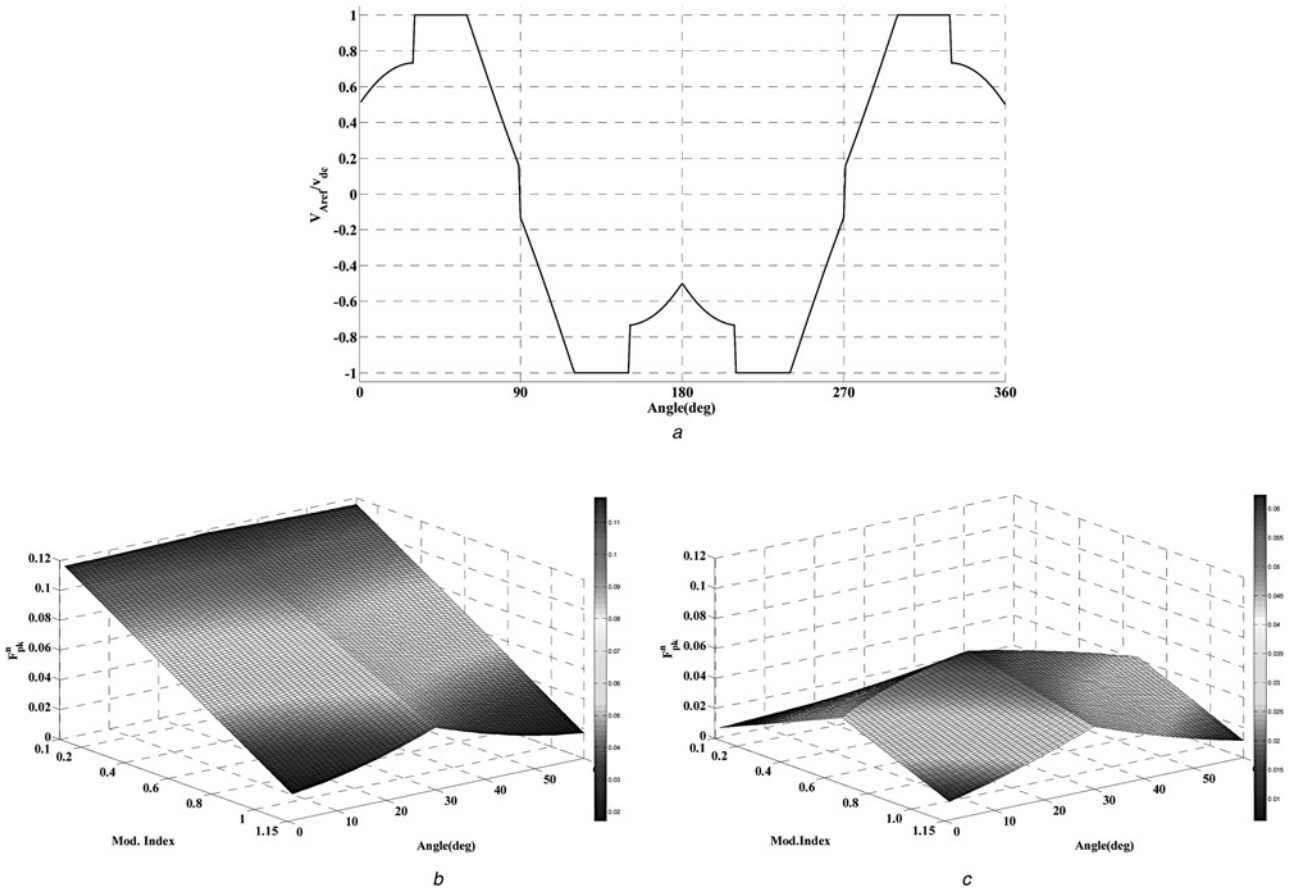
Fig. 4 *SVPWM and DPWM3*

a Updated phase *A* voltage reference for minimum peak value of the circulating current ($m = 1$)
b F_{pk}^n for different modulation index for SVPWM
c DPWM3

switching period for a phase. However, for the SPWM and the SVPWM, the sign of the PWM reference signals are known. The phase with the maximum voltage value (v_{max}) is always positive. Similarly, the phase with the minimum voltage value (v_{min}) is always negative, but the phase with the middle voltage value (v_{mid}) can be positive or negative and does not change sign if the CM offset corresponding to SVPWM ($k = \frac{1}{2}$) is added. Using these facts, the peak value of the normalised circulating current can be given by

$$
F_{pk}^n\Big|_{\text{SPWM}} =
\begin{cases}
\dfrac{1}{8} - \dfrac{v_{max}}{6v_{dc}} & v_{mid} < 0 \\[2mm]
\dfrac{1}{8} + \dfrac{v_{min}}{6v_{dc}} & v_{mid} > 0
\end{cases}
\tag{17}
$$

$$
F_{pk}^n\Big|_{\text{SVPWM}} =
\begin{cases}
\dfrac{1}{8} - \dfrac{1}{12v_{dc}}\left(2v_{max} + \dfrac{1}{2}v_{mid}\right) & v_{mid} < 0 \\[2mm]
\dfrac{1}{8} + \dfrac{1}{12v_{dc}}\left(2v_{min} + \dfrac{1}{2}v_{mid}\right) & v_{mid} > 0
\end{cases}
\tag{18}
$$

The different values of F_{pk}^n are plotted for different values of k and $m = 0.25$, 0.5, 0.75 and 1.0 in Figs. 3*a–d*, respectively.

Fig. 3 shows that the CM offset for which F_{pk}^n is minimum can be given by

$$
v_{\text{off}} =
\begin{cases}
-v_{min} - \dfrac{v_{dc}}{2} & 0° \le \omega t < 30° \text{ or } v_{mid} < 0 \\[2mm]
-v_{max} + \dfrac{v_{dc}}{2} & 30° \le \omega t < 60° \text{ or } v_{mid} > 0
\end{cases}
\tag{19}
$$

The PWM reference signal of phase *A* for this CM offset is shown in Fig. 4*a*. This is the reference signal for a DPWM, and it is known as DPWM3 in the literature [24]. For DPWM3, the value of F_{pk}^n is summarised in Table 1. F_{pk}^n for SVPWM and DPWM3 is shown in Figs. 4*b* and *c* for full range of modulation index.

F_{pk}^n is minimum for the CM offset given by (19), and it is proportional to the maximum absolute value of the reference signals for low modulation signals, as shown in Figs. 3*a* and *b*. However, for higher modulation indices, F_{pk}^n depends on all the reference signal values. However, the minimum value of the F_{pk}^n is obtained by DPWM3. An important point should be noticed that the normalised circulating current does not depend on the load. It

Table 1 Peak value of the circulating current for DPWM3

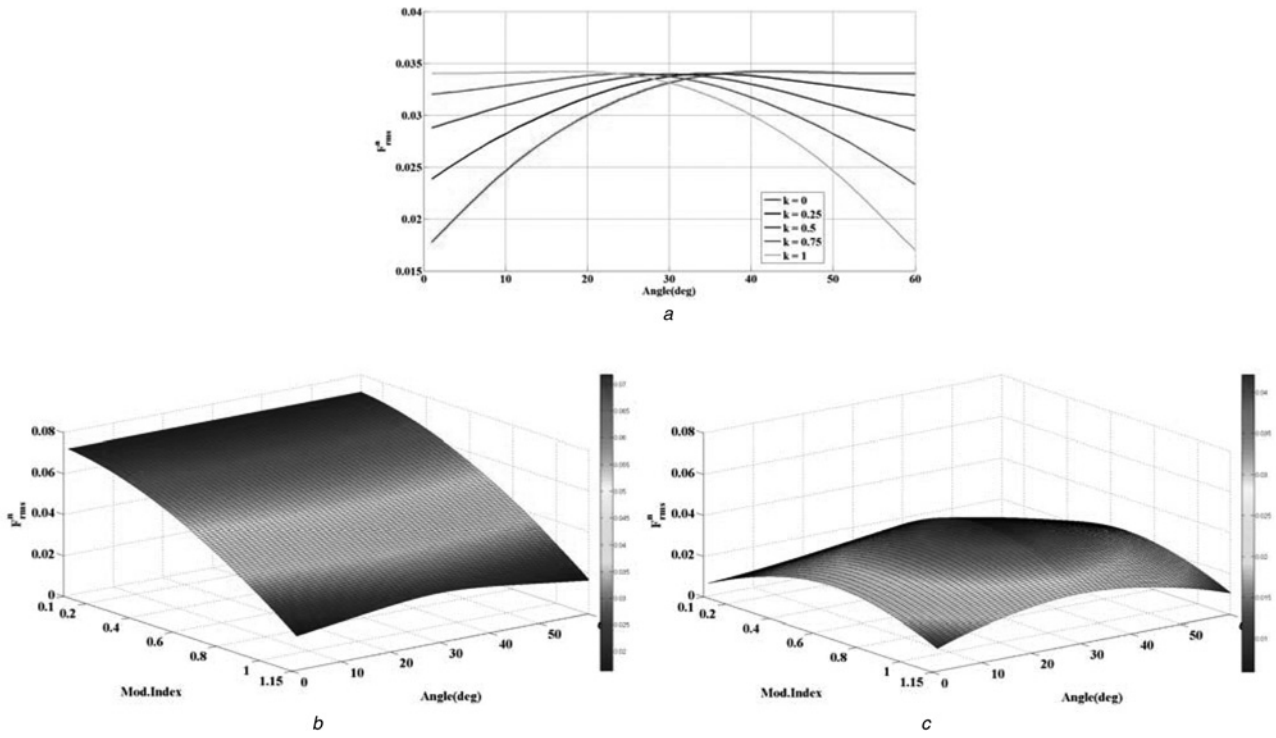| Condition		PWM reference signal sign	Peak of the normalised circulating current
$v_{max} - v_{min} < \frac{1}{2}v_{dc}$	$v_{mid} < 0$	all negative	$-(v_{min}/4v_{dc})$
	$v_{mid} > 0$	all positive	$v_{max}/4v_{dc}$
$v_{max} - v_{min} > \frac{1}{2}v_{dc}$	$v_{mid} < 0$	do not change	$v_{dc} - v_{max} + v_{mid}/12v_{dc}$
	$v_{mid} > 0$	do not change	$v_{dc} - v_{mid} + v_{min}/12v_{dc}$

Fig. 5 *RMS of the circulating current for*

a Different CM offset for $m = 1$
b Different modulation indices for SVPWM
c Different modulation indices for DPWM3

depends only on the PWM reference signals for a given dc-link voltage and inductance value.

Another important value of the circulating current which governs the choice of the PWM is the rms value of the circulating current. Using (14), the rms value of the voltage-second integral responsible for the circulating current can be calculated for a general PWM method, and it is given by (see (20)) where

$$F_{pk1} = \frac{v_{dc}}{2} \frac{T_s}{4} \left(1 - \frac{2v_{A,ref}}{v_{dc}} \right)$$

$$F_{pk2} = F_{pk1} + \frac{v_{dc}}{3} \frac{T_s}{4} \left(\frac{2v_{C,ref}}{v_{dc}} + \frac{2v_{A,ref}}{v_{dc}} \right) \quad (21)$$

$$F_{pk} = F_{pk2} + \frac{v_{dc}}{6} \frac{T_s}{4} \left(-\frac{2v_{B,ref}}{v_{dc}} - \frac{2v_{C,ref}}{v_{dc}} \right)$$

The rms value of the normalised circulating current can be given by

$$F_{rms}^{n} = F_{rms} \frac{1}{v_{dc} T_s} \quad (22)$$

Equation (20) requires complex calculation for calculating the rms value of the circulating current. Therefore numerical methods are used to calculate the rms value of the circulating current. F_{rms}^{n} for different CM offsets are plotted and shown in Fig. 5a for the modulation index of 1. The curve is plotted for $0 \leq \omega t < 60°$. It can be seen that the minimum rms value of the circulating current can be achieved for DPWM3. F_{rms}^{n} for SVPWM and DPWM3 is shown in Figs. 5b and c for full range of modulation index.

The analysis presented in the paper is useful in calculating the ripple current flowing in the filter. If a CM inductor is considered in the system, the total flux linkage in the CM inductor is proportional to the circulating current. The size of the CM inductor can be made smaller by reducing the peak circulating current. If three single-phase inductors are present in the system, they act as the CM inductor and the DM inductor both. The knowledge of the circulating current together with d- and q-axis components of the inductor current is required to find the current through the inductor. This information is an input for the design of the inductor. Since the circulating current consists of the high frequency components only, it is required for the calculation of the core losses. To reduce the core losses, the ripple in the circulating current should be minimised.

$$F_{rms} = \left[\frac{4}{T_s} \left[\frac{1}{3} F_{pk1}^2 \frac{T_s}{4} \left(1 - \frac{2v_{A,ref}^u}{v_{dc}} \right) + \frac{1}{3} (F_{pk1}^2 + F_{pk2}^2 + F_{pk1}F_{pk2}) \frac{T_s}{4} \left(\frac{2v_{C,ref}^u}{v_{dc}} + \frac{2v_{A,ref}^u}{v_{dc}} \right) \right. \right.$$

$$\left. \left. + \frac{1}{3} (F_{pk2}^2 + F_{pk3}^2 + F_{pk2}F_{pk3}) \frac{T_s}{4} \left(-\frac{2v_{B,ref}^u}{v_{dc}} - \frac{2v_{C,ref}^u}{v_{dc}} \right) + F_{pk3}^2 \frac{T_s}{4} \frac{2v_{B,ref}^u}{v_{dc}} \right] \right]^{1/2}$$

$$F_{rms} = \left[\frac{1}{3} F_{pk1}^2 \left(1 - \frac{2v_{A,ref}^u}{v_{dc}} \right) + \frac{1}{3} (F_{pk1}^2 + F_{pk2}^2 + F_{pk1}F_{pk2}) \left(\frac{2v_{C,ref}^u}{v_{dc}} + \frac{2v_{A,ref}^u}{v_{dc}} \right) \right.$$

$$\left. + \frac{1}{3} (F_{pk2}^2 + F_{pk3}^2 + F_{pk2}F_{pk3}) \left(-\frac{2v_{B,ref}^u}{v_{dc}} - \frac{2v_{C,ref}^u}{v_{dc}} \right) + F_{pk3}^2 \frac{2v_{B,ref}^u}{v_{dc}} \right]^{1/2} \quad (20)$$
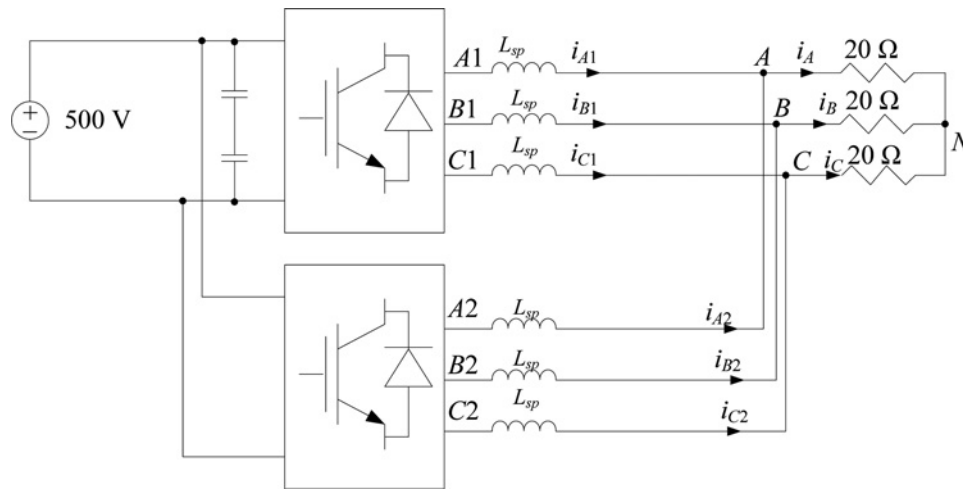
Fig. 6 *Block diagram of experimental setup*

4 Experimental results

A block diagram of the experimental setup is shown in Fig. 6. The inductance of the choke in each phase is equal to 6.5 mH (L_{sp} = 6.5 mH). The inverters are operated with a dc-link voltage equal to 500 V. The carrier frequency used for modulation is equal to 2.5 kHz. The fundamental frequency of the output current is 50 Hz. The load resistance is chosen as 20 Ω.

Figs. 7a and c show phase A inductor currents and the load current when the carrier signals are phase shifted by 180° and 90°, respectively, for SVPWM and m = 1. Figs. 7b and d show that the sum of all phase currents of inverter 1 inductor currents, which is equal to three times the circulating current, has high frequency component because of the phase shift between the carrier signals.

To show the advantage of the 180° phase shift between the carrier signals, the fast Fourier transform (FFT) of the load current for ø = 0° and 180° are shown in Fig. 8a for SVPWM and m = 1.0. It can be seen that the load current does not contain frequency components at the switching frequency and its sidebands for ø = 180°. In addition, the FFT plot of the circulating current is shown in Fig. 8b for ø = 90° and 180°. The plot shows that the circulating current does not have a frequency component at three times the output frequency for ø = 180°. Therefore the phase shift between the carrier signals is selected as 180°. Phase A inductor currents and load current for the SVPWM, m = 0.5 and ø = 180° are shown in Fig. 9a. The sum of all phase currents of inverter 1 inductor currents is shown in Fig. 9b. The peak and rms values of the circulating current are 2.2 and 1.4 A, respectively. Phase A inductor currents and load current for the DPWM3, m = 0.5 and ø = 180° are shown in Fig. 9c. The

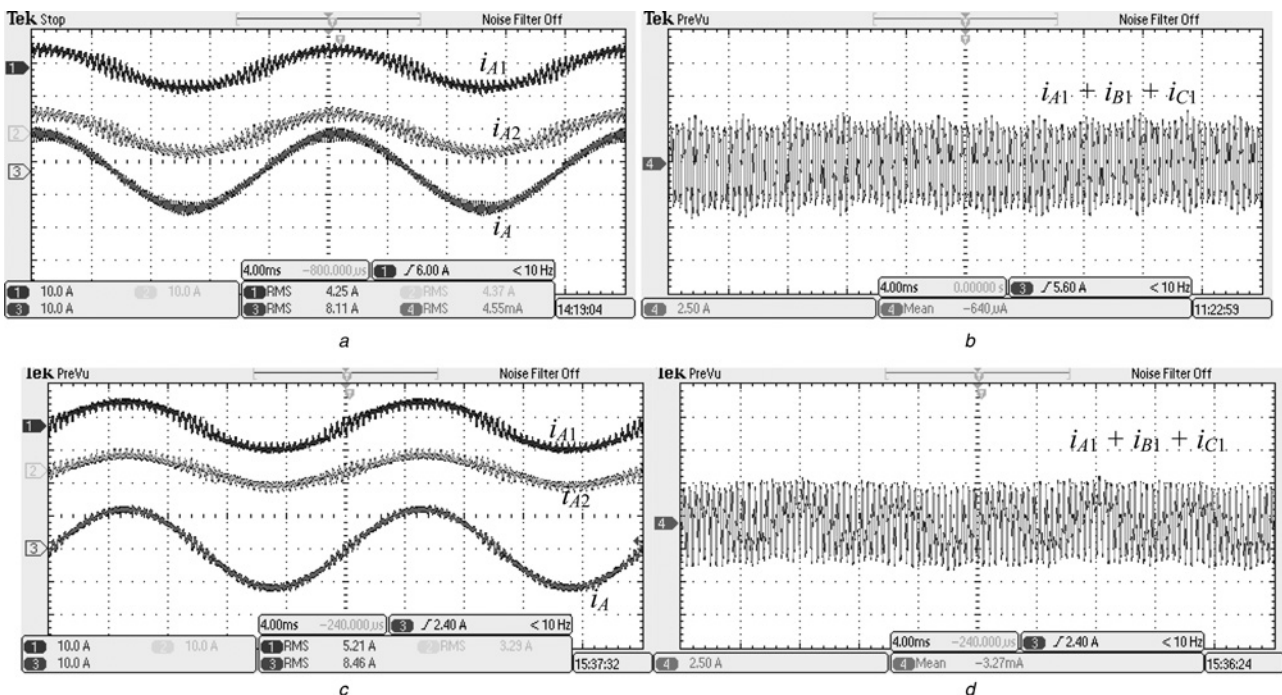**Fig. 7** *Phase A inductor currents, the load current and the sum of all phase currents of inverter 1 for m = 1 and SVPWM with ø = 180°, 90°*

a Phase A inductor currents and load current
b Sum of all phase currents of inverter 1 for ø = 180°
c Phase A inductor currents and load current
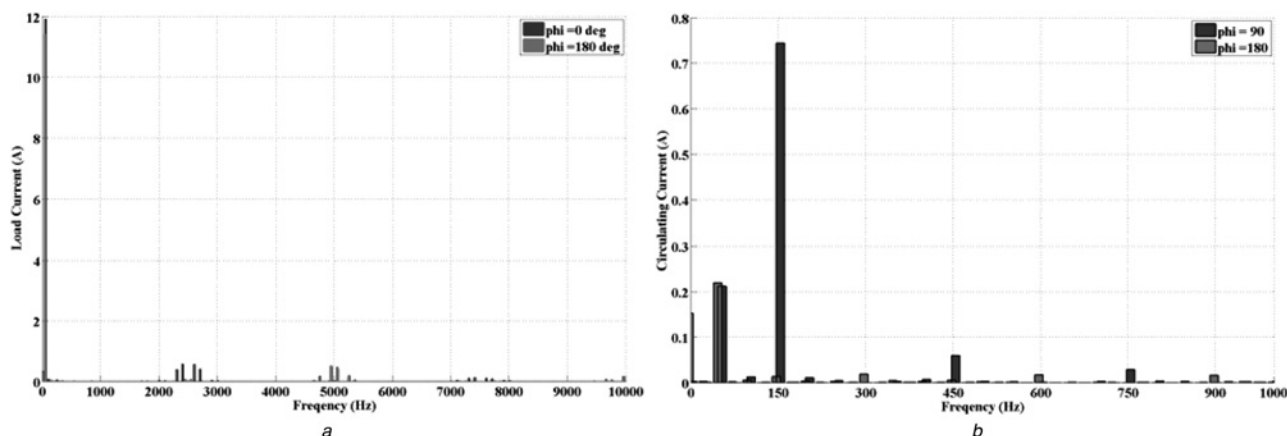d Sum of all phase currents of inverter 1 for ø = 90°, for SVPWM, m = 1

Fig. 8 *FFT plot of*

a Phase *A* load current for *ø* = 0° and 180°
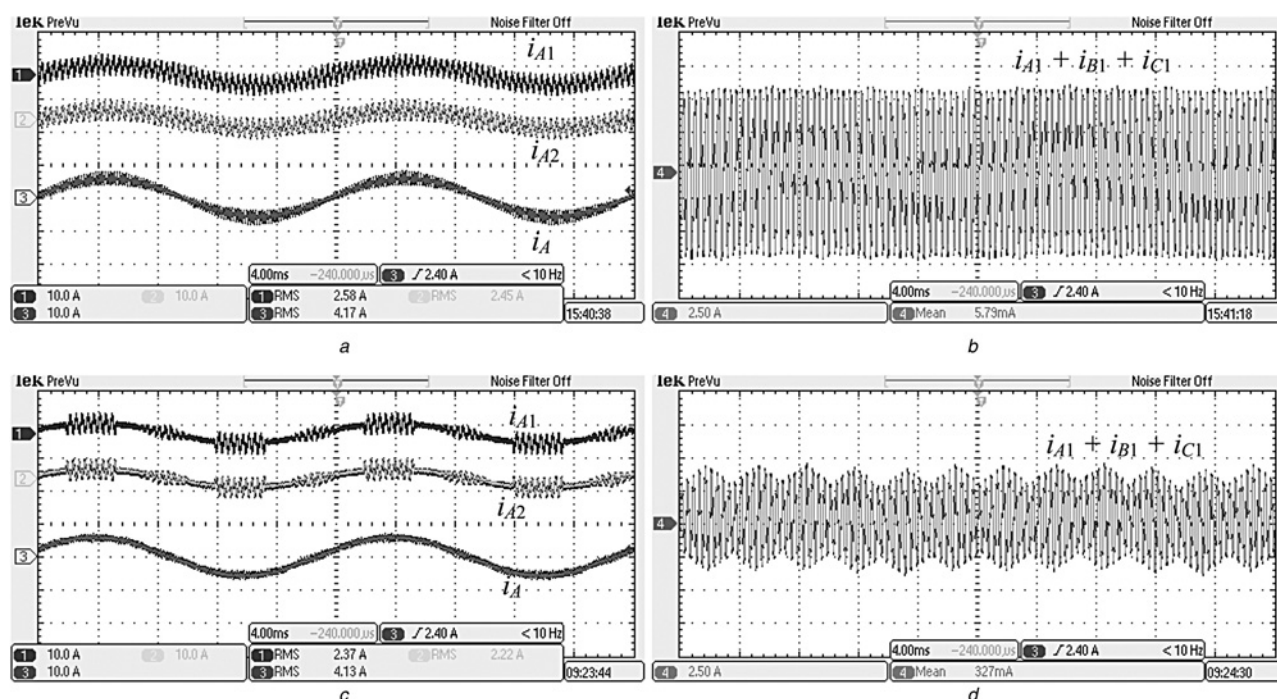*b* Circulating current for *ø* = 90° and 180°

Fig. 9 *Phase A inductor currents, the load current and the sum of all phase currents of inverter 1 for m = 0.5 and ø = 180° with SVPWM and DPWM3*

a Phase *A* inductor currents and load current
b Sum of all phase currents of inverter 1 for SVPWM
c Phase *A* inductor currents and load current
d Sum of all phase currents of inverter 1 for DPWM3, *m* = 0.5 and *ø* = 180°

sum of all phase currents of inverter 1 is shown in Fig. 9*d*. The reduction in the peak and the rms values of the circulating current can be noticed. The peak and the rms values of the circulating current are 1.48 and 0.74 A, respectively. Phase *A* inductor currents and phase *A* load current for the DPWM3, *m* = 1 and *ø* = 180° are shown in Fig. 10*a*. The sum of all phase currents of inverter 1 is shown in Fig. 10*b*. These results can be compared with Figs. 7*a* and *b* which shows the results for the SVPWM at *m* = 1.0. The peak and rms values of the circulating current for the DPWM3 are 1.17 and 0.68 A. These results are summarised in Table 2.

The load resistor is changed to 16 Ω from 20 Ω. The inverters are operated with DPWM3 at *m* = 1. Phase *A* inductor currents, the ac side current and the circulating current are shown in Figs. 10*c* and *d*. It can be seen from Figs. 10*b* and *d* that the circulating current does not change with the change in the load. It depends on the PWM method, the modulation index and the phase shift between the carrier signals.

5 Conclusions

This paper analyses and models the circulating current for two parallel-connected inverters. The paper describes the relationship between the CM voltage and the circulating current. The difference in the sampling instant for the PWM reference signals causes a low frequency component in the circulating current. The asymmetrical regular sampled PWM with 180° phase shift between the carrier signals should be used to avoid the low frequency harmonic content. In addition, the paper presents an analysis for the circulating current within a sampling period. The peak and the rms values of the circulating current in a switching period are analysed. A DPWM method is identified which causes minimum peak and rms values of the circulating current. A closed form solution for the peak value of the circulating current for the DPWM is also presented. The experimental results are presented to verify the analysis.
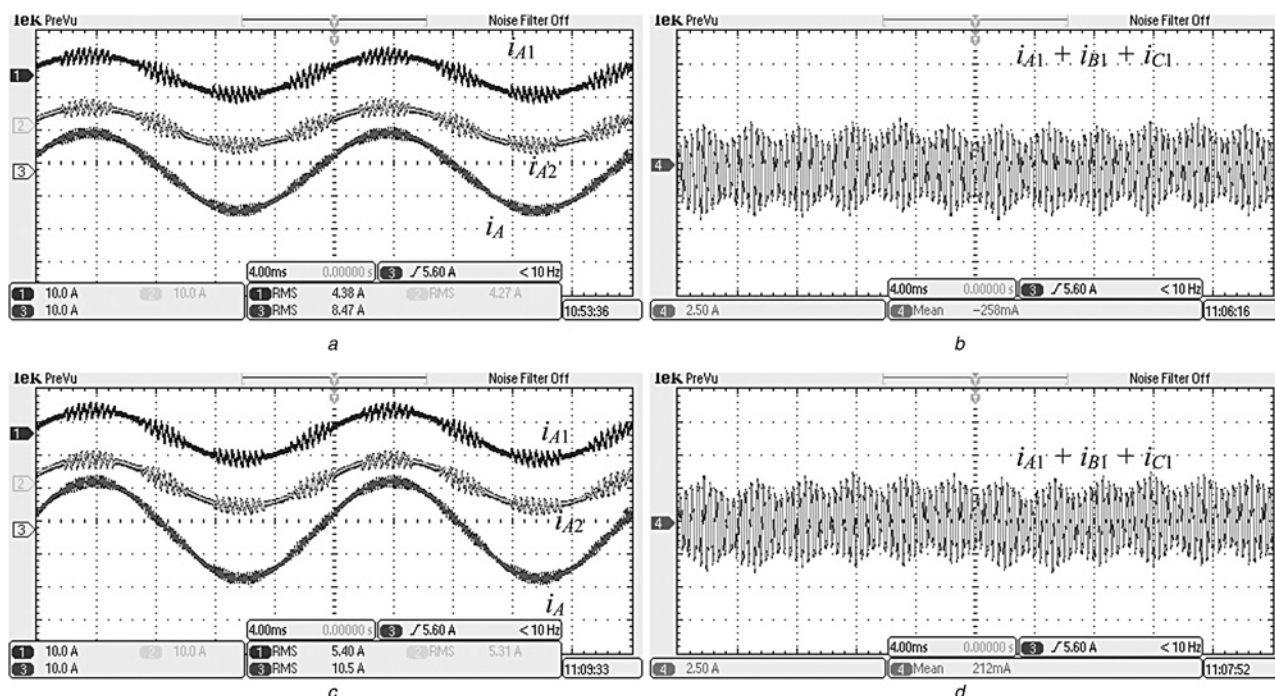
Fig. 10 *Phase A inductor currents, the load current and the sum of all phase currents of inverter 1 for DPWM3, m =1 and ø =180° with R = 20 Ω, 16 Ω*

a Phase *A* inductor currents and load current
b Sum of all phase currents of inverter 1 for *R* = 20 Ω
c Phase *A* inductor currents and load current
d Sum of all phase currents of inverter 1 for *R* = 16 Ω
DPWM3, *m* = 1.0 and ø = 180°

Table 2 Peak and rms values of the circulating current

Modulation index	PWM method	Circulating current peak, A		Circulating current rms, A	
		Calculated	Measured	Calculated	Measured
0.5	SVPWM (20 Ω load)	2.73	2.2	1.8	1.4
	DPWM3 (20 Ω load)	1.66	1.48	0.96	0.74
1.0	SVPWM (20 Ω load)	1.62	1.5	0.99	0.88
	DPWM3 (20 Ω load)	1.45	1.17	0.83	0.68
	DPWM3 (16 Ω load)	1.45	1.17	0.83	0.69

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