CPE 233 Winter 2019 Benson Midterm (Feb 14th) Study Guide
Morning Midterm: 9:40-11am. Afternoon Midterm: 12:10-1:30

What you need to 'memorize':

- How the PC, ProgRom, Register File, ALU, Scratch RAM, Flags and Control Unit work
- How to interpret SystemVerilog (you will not be asked to write it)
- Assembler Directives: .CSEG, .ORG, .EQU, .DSEG, .DB
- How the following RAT instructions work:
  - Program Control: BRN, BRNE, BRCS, BRCC, CLC, SEC
  - I/0: IN, OUT
  - Logical: AND, OR, EXOR, TEST
  - Arithmetic: ADD, ADDC, SUB, SUBC, CMP
  - SH & Rot: LSL, LSR, ROL, ROR, ASR (RTL will be given for these)
  - Storage: ST, LD

What you will be provided:

- Machine code patterns when needed
- Architecture diagram (if needed)
- RTL for shift and rotate instructions
- Reminder that logical operations clear the carry and load the zero flag, arithmetic operations load both

Types of Questions:

1. Fill in the contents of the prog_rom, register file, and scratch pad for a given Rat assembly program.
   How to practice:
   Try out the examples provided from past exams
   Write your own assembly programs and write down what you think the contents of the prog_rom, scratch pad, and register file should be at the end of the program. Run the code in RatSim to check your answer
2. Calculate the timing for a given Rat assembly program
   How to practice:
   Try out the examples provided from past exams
   Write your own assembly programs and write down what you think the timing is. Run the code in RatSim and count how many mouse clicks you do until the program is over.
3. Design a flow chart and write a program in RAT Assembly
   How to practice:
   Redo you your software assignments and the example RAT assembly assignments shown in class. Make up what you want your program to be able to do, write the RAT assembly program, and use RatSim to test if your program does what you intended it to do
4. Fill out the timing diagram for a given RAT component
   How to practice:
   Change your Sim file for each of your RAT assignments. Draw the timing diagram that you would expect and then check your result with the output of the simulator.
5. Fill out the timing diagram for the CPU for a given Rat assembly program
   How to practice:
   Write a simple RAT assembly program that can be supported by your CPU. Fill out the timing diagram for this program on paper. Check your solution with the output of the simulation file.