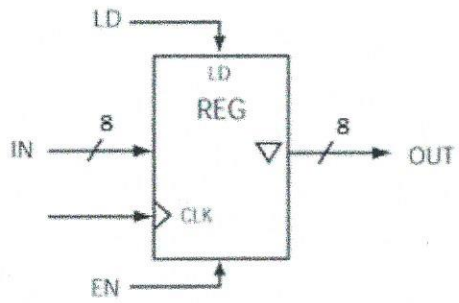
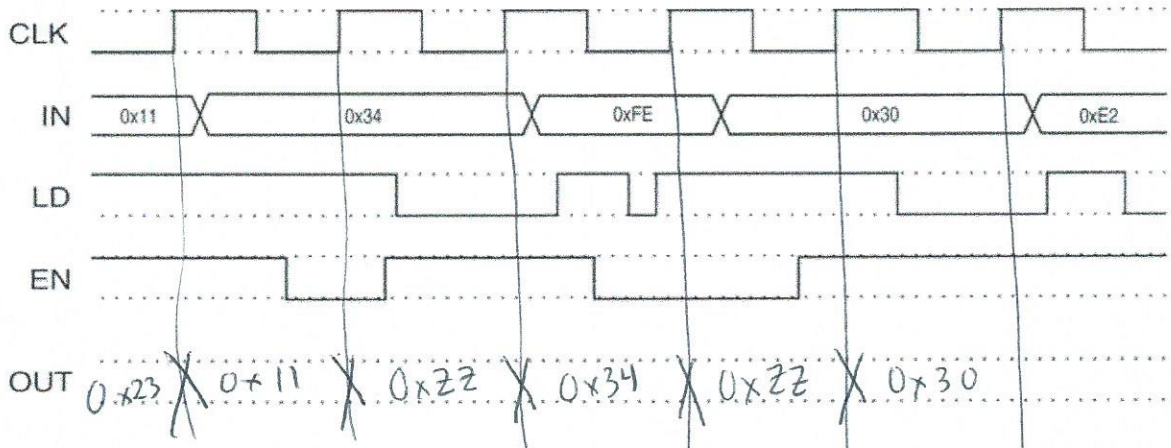
Name: SOLUTIONS

CPE 233 Quiz 1

1. Complete the timing diagram below (in hex) for the given 8-bit **rising-edge** triggered, tri-state register. Reading is asynchronous, writing is synchronous. LD must be asserted in order to load the register. EN is the enabler of the tri-state buffer. Assume the initial value of stored in the register is 0x23. Ignore all propagation delay issues.

NOT ON TEST





2. How large is the address bus (in bits) of a 2G x 48 memory device?

$G = 2^{30}$ so $2G = 2^1 \cdot 2^{30}$ → 31 bits

NOT ON TEST

3. What is the memory capacity (in Bytes) of the signal *reg* created below? Provide your answer as a decimal number.

16 (0 to 15) 24 (23 downto 0)

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TYPE memory is array (0 to 15) of std_logic_vector(23 downto 0);
signal reg: memory := (others=>(others=>'0'));
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$$\frac{2^{16} * 24^{3}}{8} = 3 * 2^{16} = 196608 \text{ Bytes}$$