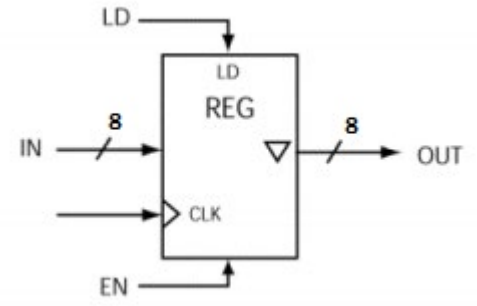
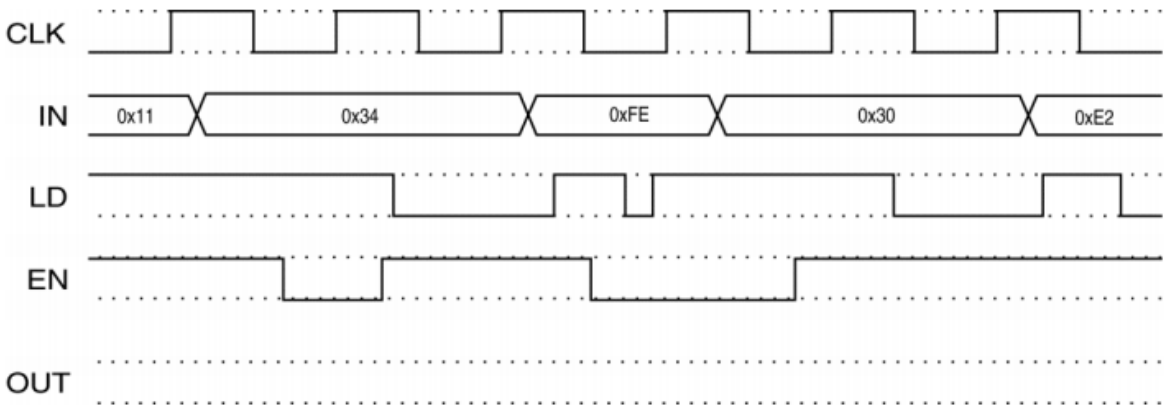
Name:

# CPE 233 Quiz 1

1. Complete the timing diagram below (in hex) for the given 8-bit **rising-edge** triggered, tri-state register. Reading is asynchronous, writing is synchronous. LD must be asserted in order to load the register. EN is the enabler of the tri-state buffer. Assume the initial value of stored in the register is 0x23. Ignore all propagation delay issues.




2. How large is the address bus (in bits) of a 2G x 48 memory device?

3. What is the memory capacity (in Bytes) of the signal *reg* created below? Provide your answer as a decimal number.

```
TYPE memory is array (0 to 15) of std_logic_vector(23 downto 0);

signal reg: memory := (others=>(others=>'0'));
```

The tables below show the current contents of the register file and of the scratch pad memory.

```
.CSEG
.ORG          0x29

label: ADD    R1, R2
       BRCS    label
       ST     R5, (R5)
       LD     R31, (R3)
       XOR    R30, R29
       BREQ   end:
       LD      R4, 0xFE
end:   ADD    R0, 0x00
```

Modify the register and scratch pad memory contents that result from executing the program.

| | |
|---|---|
| 0 | 0x04 |
| 1 | 0xF1 |
| 2 | 0x0F |
| 3 | 0x00 |
| 4 | 0x02 |
| 5 | 0x11 |
| . | |
| 29 | 0x98 |
| 30 | 0x32 |
| 31 | 0x98 |

Register File

| | |
|---|---|
| 0 | 0x23 |
| 1 | 0x11 |
| . | |
| 16 | 0x1F |
| 17 | 0x54 |
| 18 | 0x99 |
| . | |
| 253 | 0x0B |
| 254 | 0x28 |
| 255 | 0x54 |

Scratch Pad Memory