Exp 4: 4-Bit Ripple Carry Adder (RCA)

Objectives:

- To receive yet even more exposure to the Xilinx Design Methodology
- To use a verilog structural model to support notion of hierarchical digital design
- To use verilog structural model to support the notion of modular design and reuse in verilog

Somewhat Meaningful Comments: Arithmetic circuits are massively common out there in digital design land. One of the most basic and useful circuits the Ripple Carry Adder (RCA). For the purpose of this activity, the RCA is comprised of a HA for the LSB and a FA for all the other bits. Figure 11 shows a schematic diagram of the RCA.

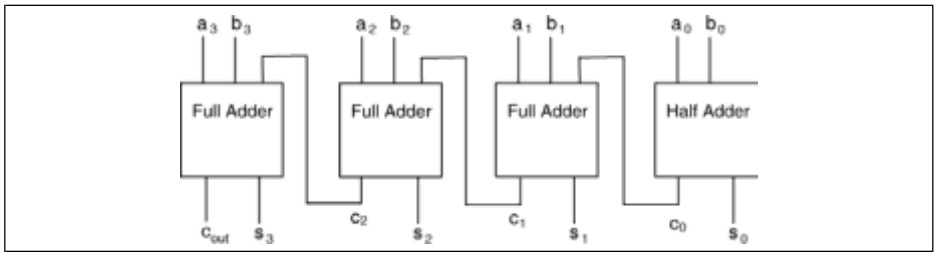


Figure 1: Schematic diagram for a 4-bit Ripple Carry Adder.

Assignment: Using the half adder and full adder that you designed previously, design and implement the 4-bit Ripple Carry Adder shown in Figure 11. Use verilog structural modeling for your implementation using both the HA and FA verilog modules designed previously. Verify your design works using both the simulator and visually using the pin assignments provided in Table 0.1.

Inputs		Outputs	
A	**B**	**SUM**	**Carry-out**
a_3-a_0: SW7-SW4	b_3-b_0: SW3-SW0	s_3-s_0: LD3-LD0	C_{out} = LD7

Table 0.1: Pin assignments for the RCA.

Special Deliverables:

1. Well annotated waveforms from the simulator.

Questions:

1. In your own words, briefly but completely explain why the circuit in this lab activity is referred to as a ripple carry adder.

2. If you needed to extend the RCA from this lab activity to an 8-bit RCA by using a structural model with two 4-bit RCAs, what changes would you need to apply to the 4-bit RCA?

3. How many rows would there be in the truth table for a 4-bit RCA? How many input and output variables are there? Would it be feasible to design a 32-bit RCA using this technique?

4. If you were to implement the 4-bit RCA using discrete logic, how many logic gates would be required?

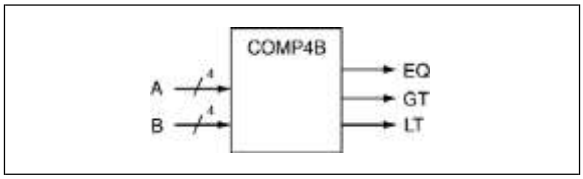
Exp 5: 4-Bit Comparator

Objectives:

- To design and implement one of the basic digital logic circuits
- To discover the power of verilog behavioral modeling

Somewhat Meaningful Comments: This experiment introduces the notion of verilog behavioral modeling in the context of 4-bit comparators. While you'll quickly find that a designing a simple 4-bit comparator is no big deal with behavioral modeling.

Assignment: Design 4-bit comparator using behavioral models. The inputs to the circuit are two 4-bit unsigned binary numbers. The circuit outputs indicate when the two inputs are equal, whether the A input is greater than the B input, or whether the A input is less than the B input.



Input		Output
A	B	EQ, LT, GT
4 left-most switches	4 right-most switches	right-most three LEDs, respectively

Questions:

1. In your own words, briefly describe the advantage of using a behavioral model as opposed to a gate-level implementation of the comparator.

2. Modify your 4-bit comparator model in this activity to be a 32-bit comparator; include this code with your lab activity report.