Exp 9: BCD Comparator Display Module

Objectives:

- To introduce and complete a block-level design of a digital circuit
- To implement a relatively complex circuit using Verilog structural modeling
- To practice the digital design principles of code reuse

Background: Although truth-table-based designs are a valid digital design technique, they suffer greatly from the fact that anything larger than a 5-variable truth table is going to severely limit the complexity of your designs. In this activity, you'll design your circuit on the block level and then implement your design using a Verilog structural model. You'll also note that if this design were attempted using the truth table approach, you probably would never finish.

Assignment: Design a circuit that inputs two BCD numbers and displays the greater to these two numbers on the 7-segment display. If the two numbers are equal, the 7-segment display will be blank.

Start your design on a block level; model your circuit using a Verilog structural model; implement your design on the development board using the switches for the two 4-bit BCD inputs and the left-most 7-segment for the numeric output.

One of the large issues in writing Verilog models is that you should always attempt to reuse your old code. The most desired approach is to reuse your old models without modifying them; the thought here is that you previously tested your old module so you must retest the model if you modify the code. The second option is to make as few modifications as possible to the code if you can't avoid modifying it.

Special Deliverables:

1. None

Questions:

1. Would it have been possible to implement this design without using some type of MUX? Briefly explain.

2. For this lab activity, is there any difference between a BCD number and a 4-bit unsigned binary number? Briefly explain.

Exp 10: BCD Comparator Display Module 2

Objectives:

- To implement a relatively complex circuit using Verilog structural modeling
- To practice the digital design principles of block-level design and code reuse

Background: This lab activity is an extension of a several previous lab activities. In this activity, you'll be using two previously designed modules: the comparator and the BCD-to-7-segment decoder. While the circuit in this activity arguably lacks interest, it does provide more practice with block-level design, code reuse, and structural modeling.

Most importantly of anything, you need to start out with a block level design. If you starting coding Verilog models as your first step, you'll for sure waste a ton of time.

Assignment: Design a circuit that inputs two BCD numbers, A and B, using the left-most and right-most switches, respectively.

- If the two numbers are equal, the two middle 7-segment displays shows the values (all other 7-segment displays are off).
- If A is greater than B, the left-most 7-segment display shows the A value (all other 7-segment displays are off).
- If B is greater than A, then B is displayed on the right-most 7-segment display (all other 7-segment displays are off).
- If BTN0 is pressed, all displays are off.

Questions:

1. Would it have been possible to modeling this entire circuit with one always block? Support your answer of why you think this is possible or not.