

CPE 133 Lab: Half Adder/Full Adder

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Summary:

Half-Adder: Digital circuit which takes two 1-bit inputs (OP_A, OP_B) and outputs their sum and carry-over as 1-bit values.

Sum of Products: $F = OP_A \& OP_B$

OP_A	OP_B	SUM	CO
0	0	00	0
0	1	01	0
1	0	01	0
1	1	10	1

Full-Adder: Digital circuit which takes three 1-bit inputs (OP_A, OP_B, Cin) and outputs their sum and carryover using the Sum of Products & Product of Sums approach.

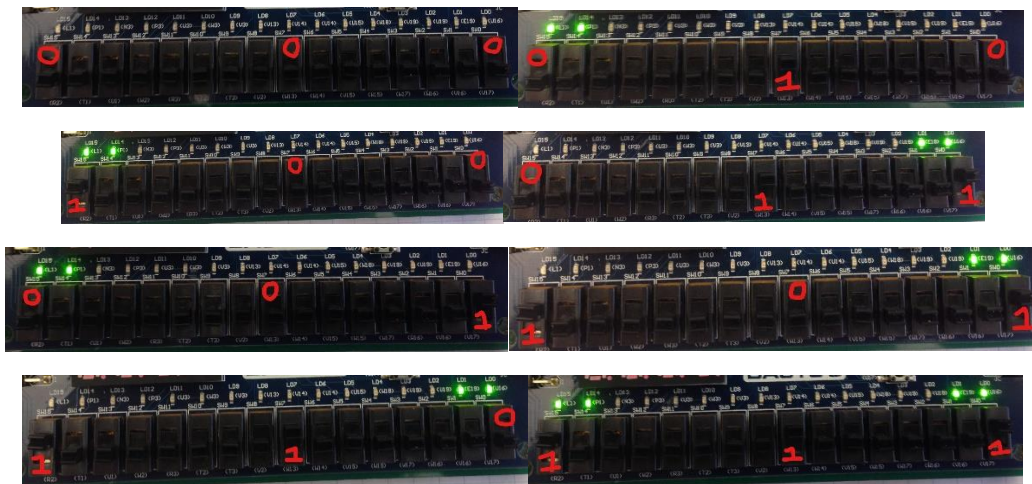
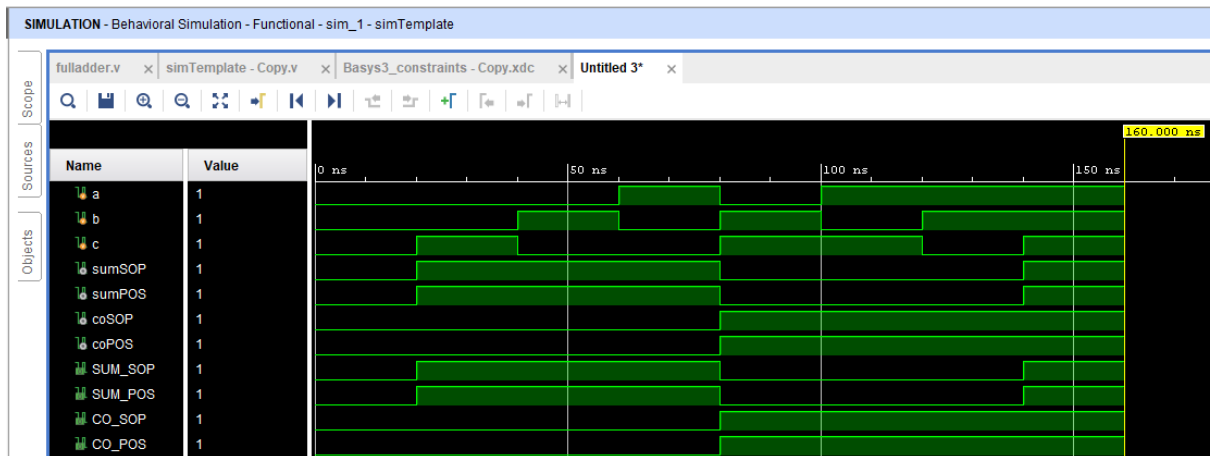
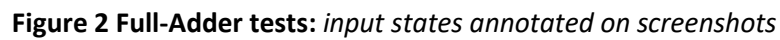
SOP (w/ abbreviated terms): $F = \sim ABC + A\sim BC + AB\sim C + ABC$

POS (w/ abbreviated terms): $F = (A + B + C) (A + B + \sim C) (A + \sim B + C) (\sim A + B + C)$

OP_A	OP_B	Cin	SUM_SOP	SUM_POS	CO_SOP	CO_POS
0	0	0	00	00	0	0
0	0	1	01	01	0	0
0	1	0	01	01	0	0
1	0	0	01	01	0	0
0	1	1	10	10	1	1
1	0	1	10	10	1	1
1	1	0	10	10	1	1
1	1	1	11	11	1	1

Verification:

For both HA & FA, we conducted behavioral simulations & board-tests to exhaustively verify the predicted behavior of the digital circuits. On the next page you will find screenshots of the resulting behavioral simulations and photos from the board-tests.



Questions

HA:

- 1) In your own words, what is meant by the term “methodology”?

At a glance, methodology suggests the study of a process for producing a desired outcome. Within the context of Digital Design, methodology suggests the study of design processes for producing digital circuits. There exist two fundamental approaches within Digital Design: Top-Down & Bottom-Up methodology.

- 2) What is a PLD? Name at least two different types of PLDs.

A PLD is a Programmable Logic Device. Programmable Read Only Memory (PROM) and Programmable Array Logic (Pal) are examples of PLDs.

- 3) In what ways, if any, could you imagine the PLD circuit implementation methodology differing with another company’s CAD software?

I can imagine that the syntax of another company’s CAD software might be different to achieve the same result with the PLD circuit implementation we have used in this lab. Perhaps other CAD software completely forgo the logical implementation and merely provide a GUI to graphically model a circuit and no more.

- 4) How many signal assignment statements did you use in your Verilog model for the HA?

Two assignment statements were utilized in the Verilog model (design source file) for the SUM output & the CO (carry-over) output. One assignment statement for $SUM = OP_A + OP_B$ & another for $CO = (OP_A \& OP_B)$.

FA:

- 1) In your own words, what is meant by the term “functionally equivalent”?

Functionally equivalent describes two non-identical digital circuits which accomplish the same thing in terms of output & required inputs.

- 2) If the sets of LEDS in this activity did not light up in pairs, what would that indicate to you?

Had the LED pairs for (SUM) & (CO) not lit up in pairs, that would have suggested that SOP & POS methods are fundamentally different in outcome, that is that they achieve logically different results.

- 3) Which was easier to implement: SOP or POS? explain.

Neither was easier to implement as there were an equal number of 0s & 1s in the CO output set. Recall that the number of terms in the Boolean expression for SOP & POS depends on the number of 0s & 1s respectively.

- 4) Could you make a general statement that either SOP or POS functions would be easier to implement? Explain.

No, you cannot make a general statement favoring SOP over POS or vice-versa, because the feasibility of either method depends on the number of 0s & 1s in the resulting solution set.

Sources:

<https://www.vlsifacts.com/digital-design-methodologies/>

http://faculty.kfupm.edu.sa/COE/abouh/Lesson6_1.pdf