Pipelined ARM Processor

Computer Architecture (CIE 439)

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modules used:

- ALU.sv
- ARM.sv
- CondCheck.sv
- Controller.sv
- DataPath.sv
- Testbench.sv
- Top.sv
- Mux2.sv
- Mux3.sv
- Flopenrc.sv
- Floprc.sv
- Hazard.sv
- Imem.sv
- Regfile.sv
- Dmem.sv
- Eqcmp.sv
- Flopenr.sv
- Extend.sv

Testbench

PROGRAM	; COMMENTS	HEX CODE
MAIN SUB R0, R15, R15	; R0 = 0	E04F000F
ADD R2, R0, #5	; R2 = 5	E2802005
ADD R3, R0, #12	; R3 = 12	E280300C
SUB R7, R3, #9	; R7 = 3	E2437009
ORR R4, R7, R2	; R4 = 3 OR 5 = 7	E1874002
AND R5, R3, R4	; R5 = 12 AND 7 = 4	E0035004

Testbench

```
ADD R5, R5, R4        ;R5 = 4 + 7 = 11      E0855004

SUBS R8, R7, R2       ;R8=3-5=-2,setFlags   E0578002
ADDLT R7, R5, #1      ;R7 = 11 + 1 = 12     B2857001
SUB R7, R7, R2        ;R7 = 12 - 5 = 7      E0477002
STR R7, [R3, #84]     ;mem[12+84] = 7       E5837054
LDR R2, [R0, #96]     ;R2 = mem[96] = 7     E5902060
ADD R12, R2, #114     ;R12 = 114 + 7 = 121  E282C072
```

Testbench

```
BIC R3, R12, R7        ; R3 = 121 & ~7 = 120  E1CC3007
EOR R5, R3, R12        ;R5 = 120 ^121 = 1     E023500C
```

PCWRITE:

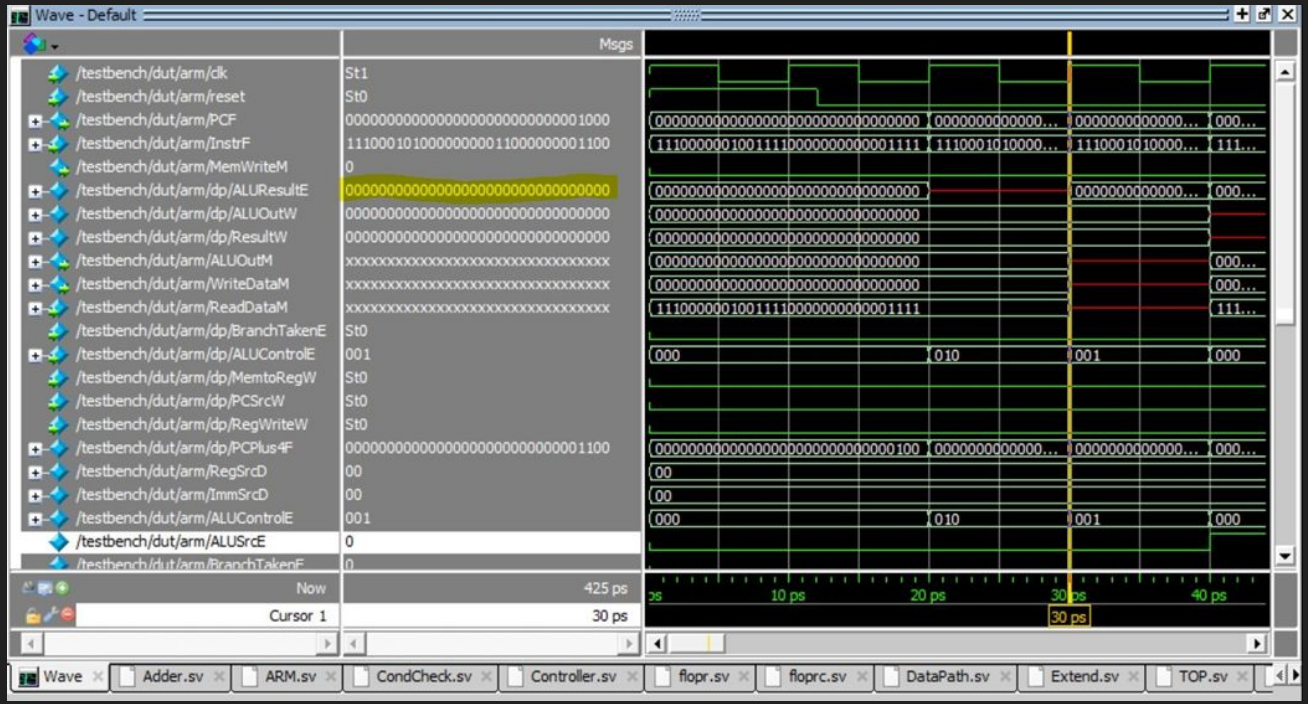
```
ADD R15, R15, #0                E28FF000
ADD R4 , R0, R0                 E2898005
ADD R5 , R0, R0                 E0805000
ADD R12 , R4, R5                E084C005
```

Testbench

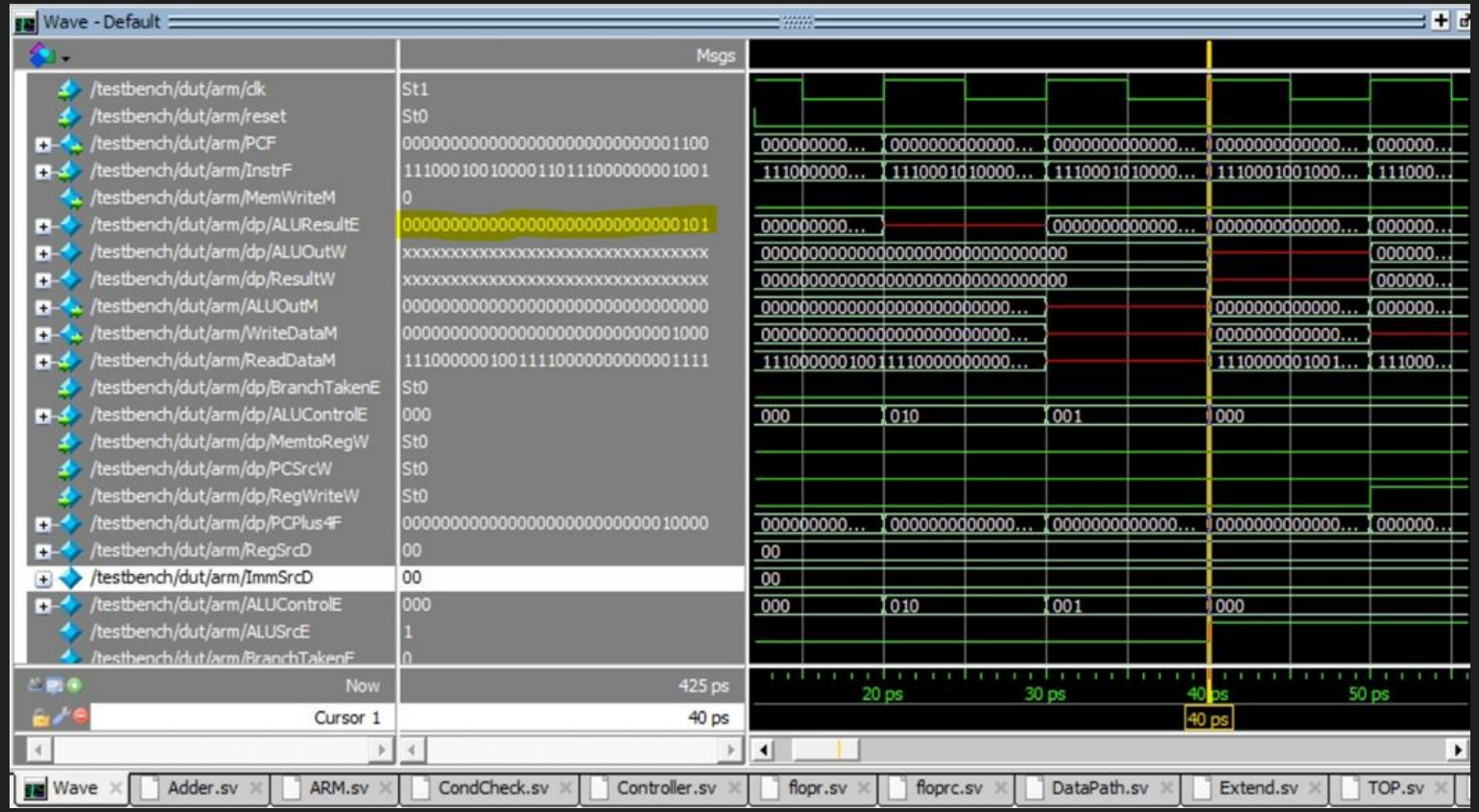
```
    B END              ;always taken        EA000001
   ADD R2, R0, #13     ;shouldn't happen    E280200D
   ADD R2, R0, #10     ;shouldn't happen    E280200A
END STR R2, [R0, #100]  ;mem[100]=7          E5802064
```

Simulation results

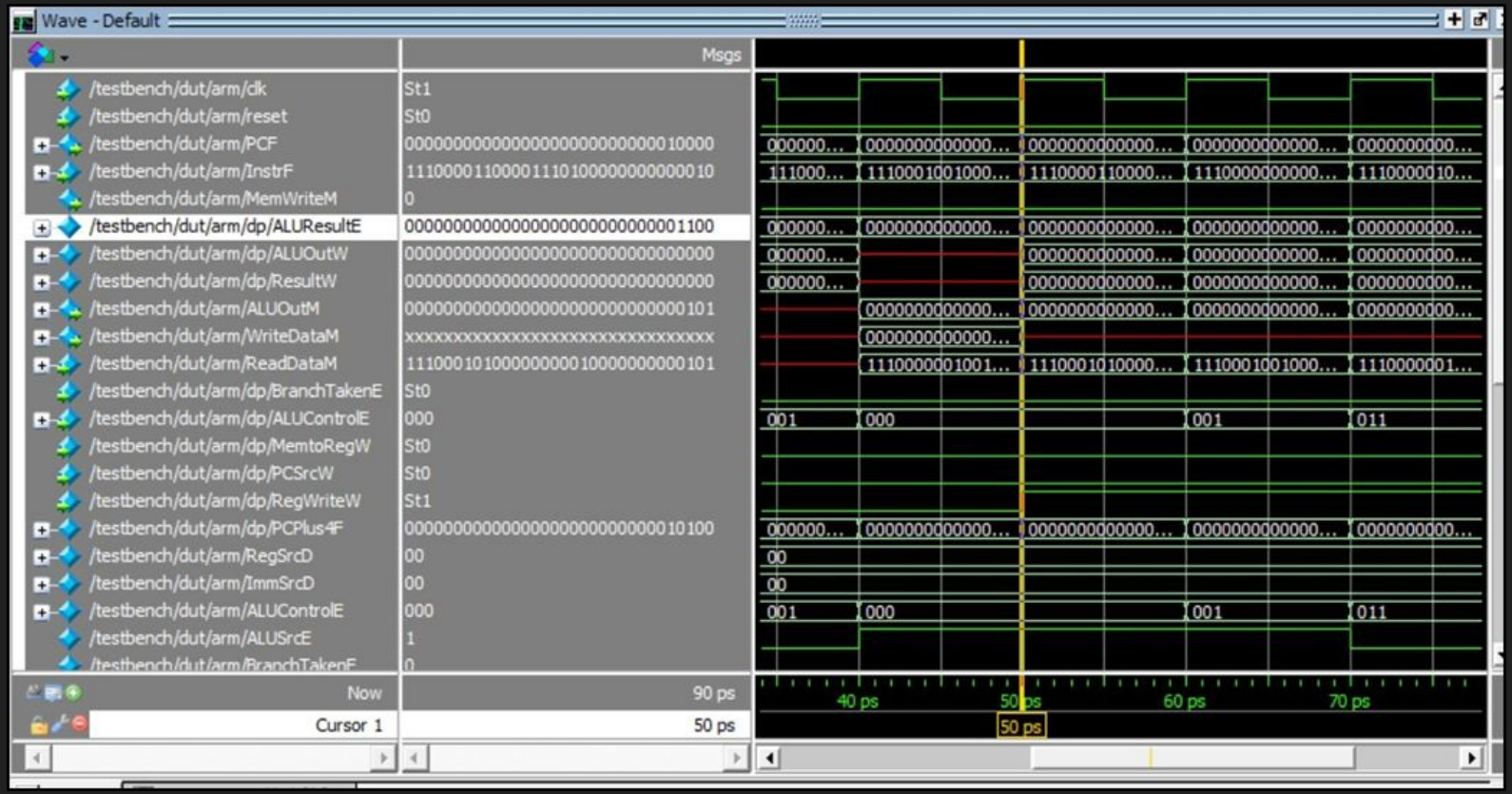
SUB R0, R15, R15



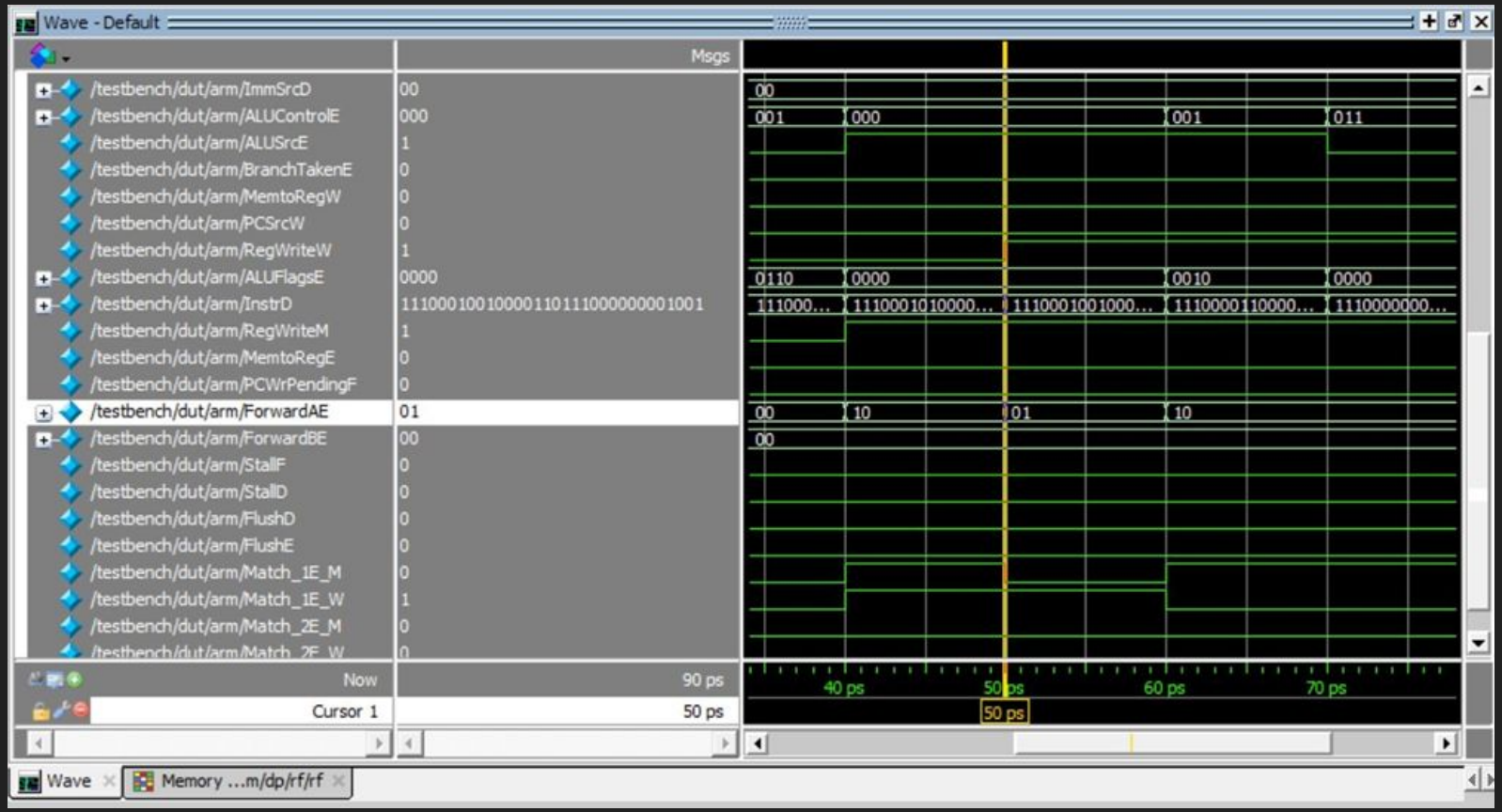
ADD R2, R0, #5 ; R2 = 5

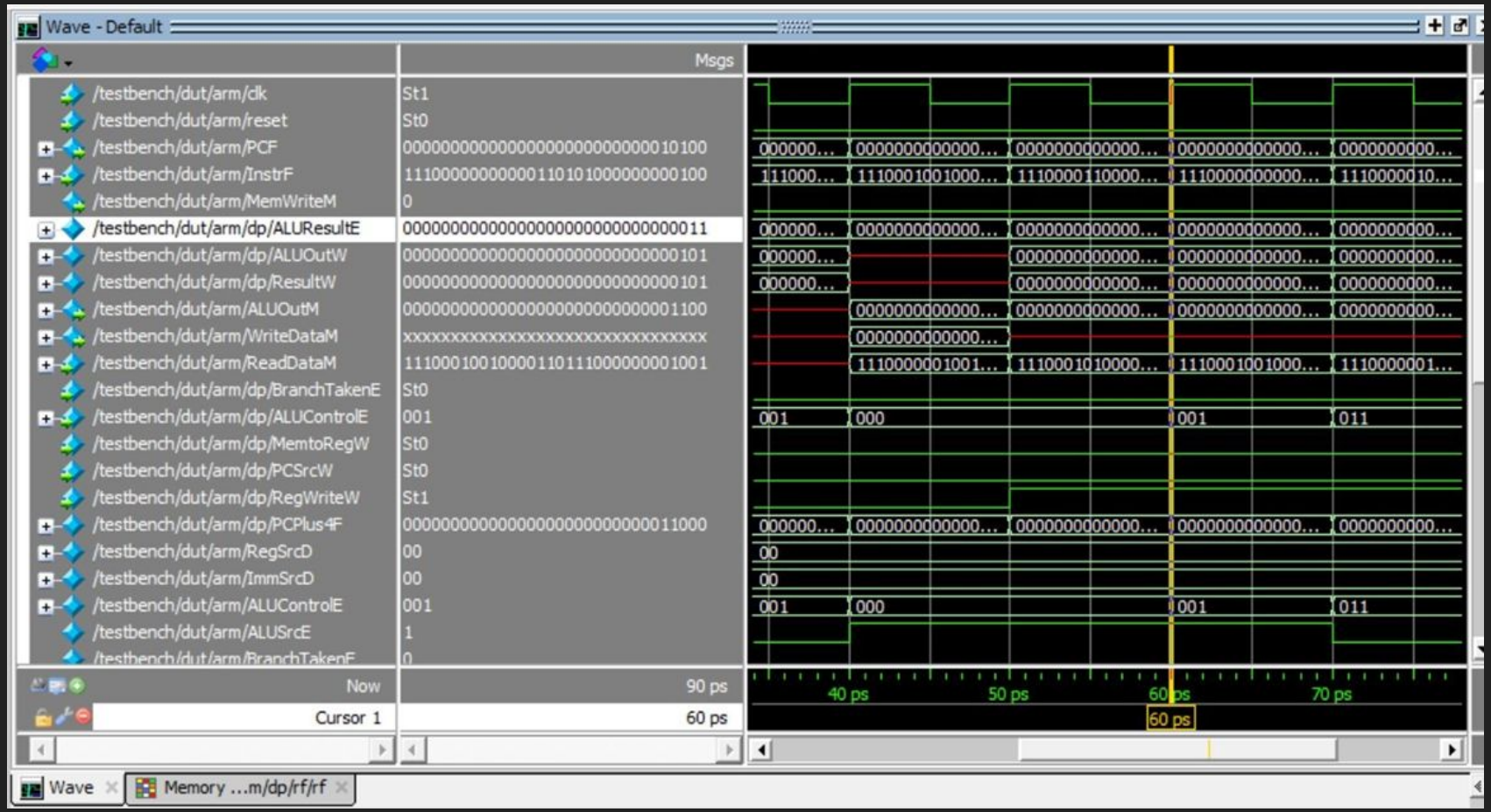


ADD R3, R0, #12 ;R3 =12

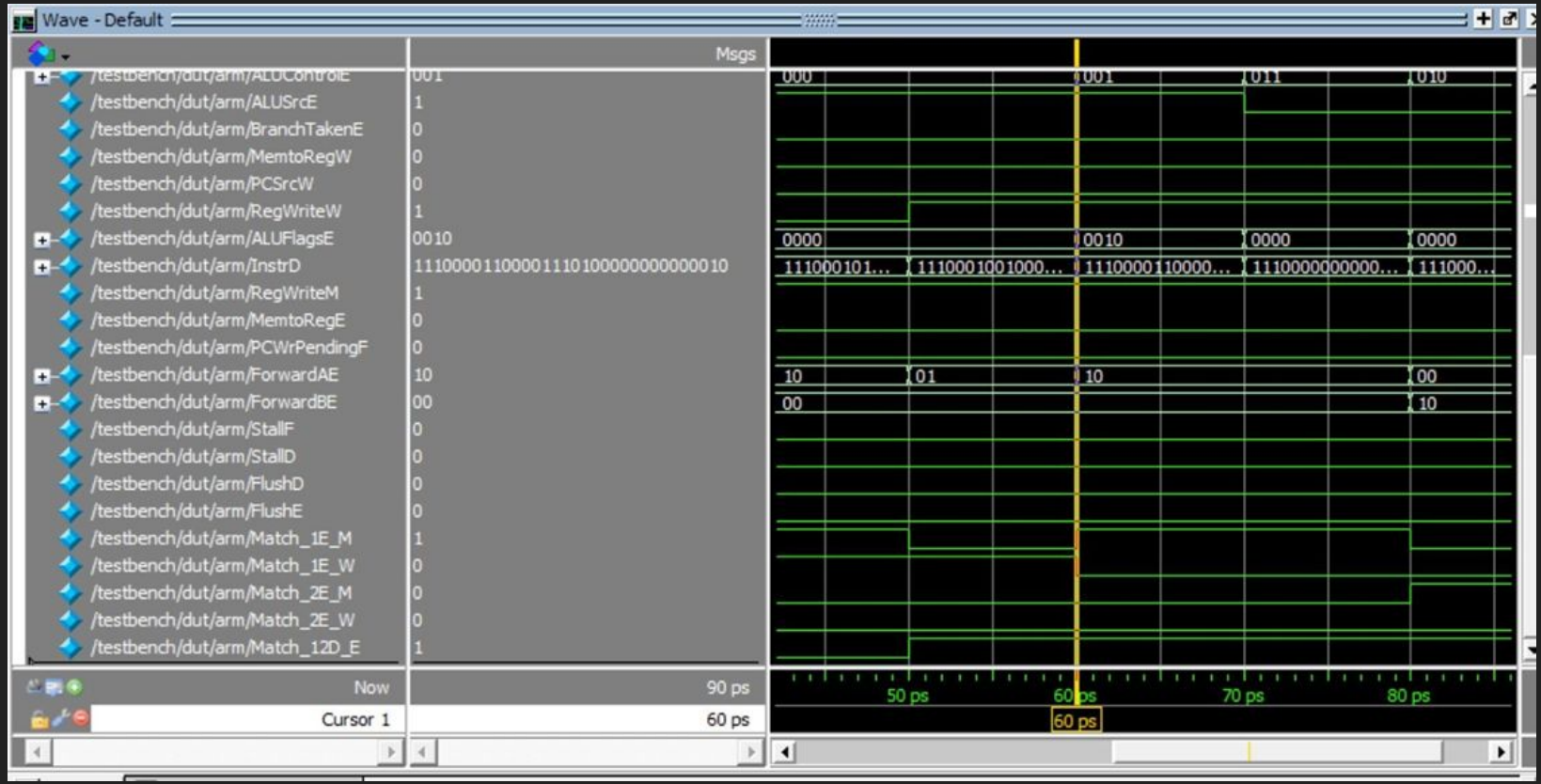


SUB R7, R3, #9 ; R7 = 3 **(Data dependency: solved by data forwarding)**

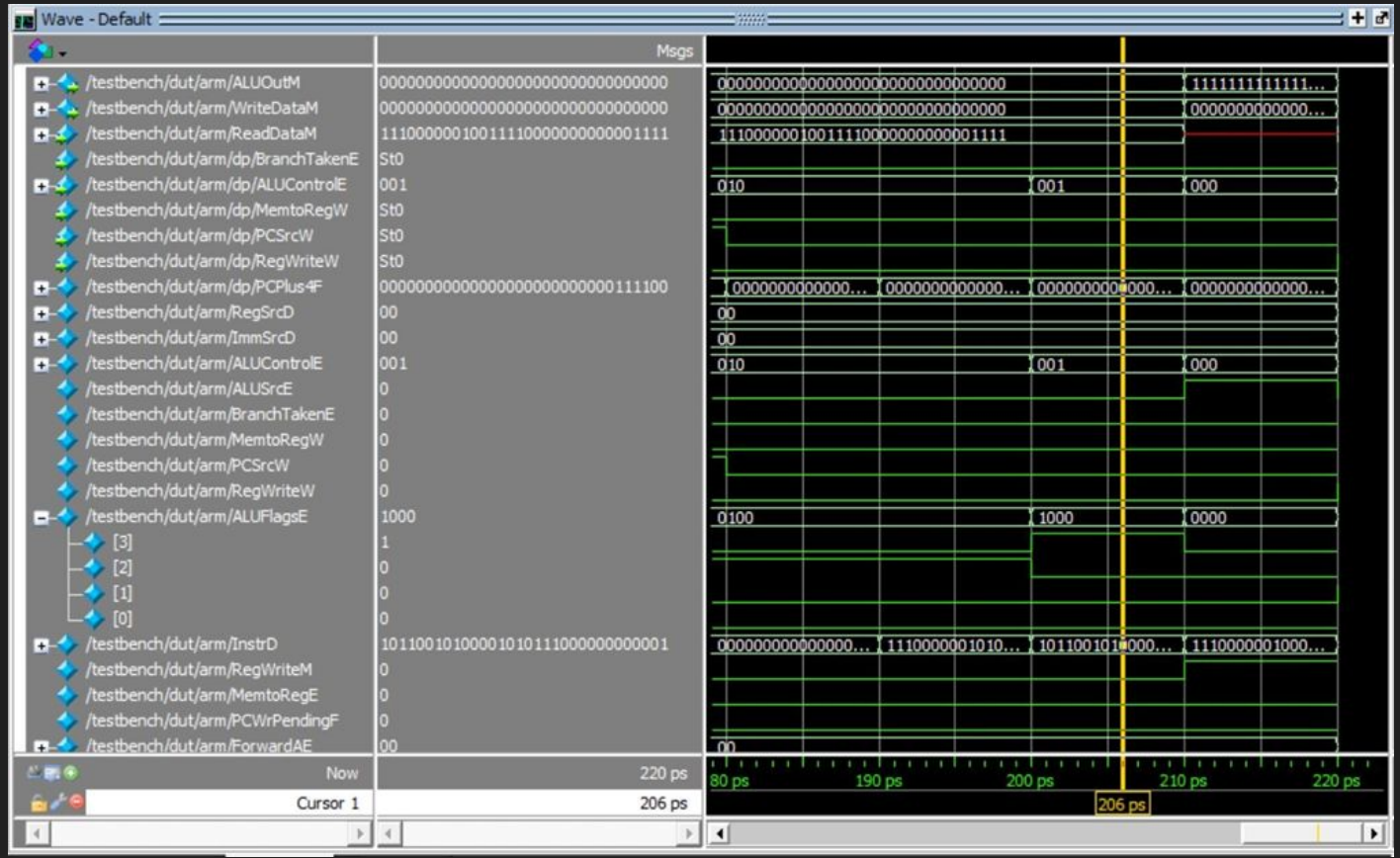


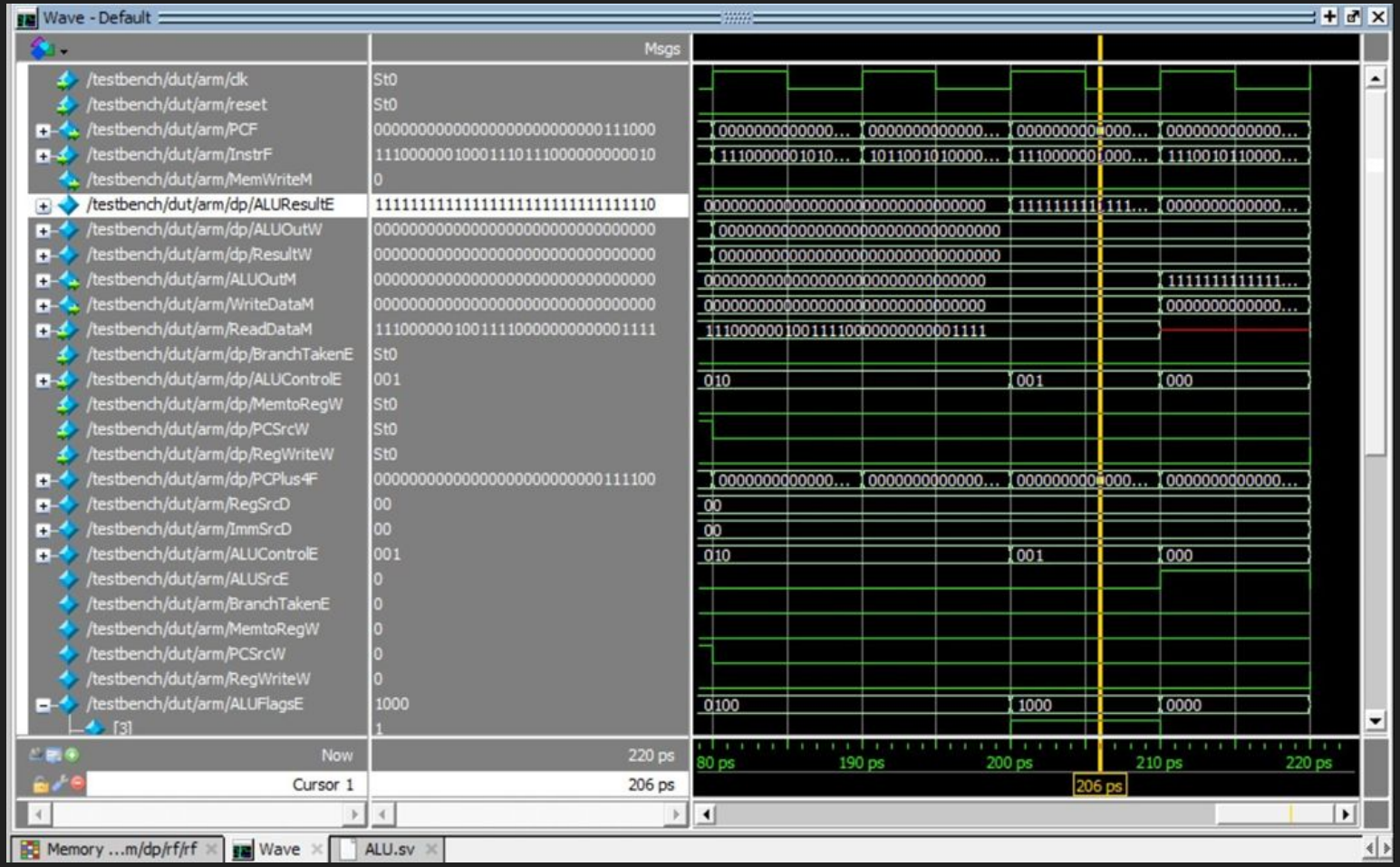

Wave - Default
Msgs
/testbench/dut/arm/clk
St1
/testbench/dut/arm/reset
St0
/testbench/dut/arm/PCF
00000000000000000000000010100
/testbench/dut/arm/InstrF
11100000000001101010000000100
/testbench/dut/arm/MemWriteM
0
/testbench/dut/arm/dp/ALUResultE
00000000000000000000000000011
/testbench/dut/arm/dp/ALUOutW
/testbench/dut/arm/dp/ResultW
/testbench/dut/arm/ALUOutM
/testbench/dut/arm/WriteDataM
/testbench/dut/arm/ReadDataM
/testbench/dut/arm/dp/BranchTakenE
/testbench/dut/arm/dp/ALUControlE
001
/testbench/dut/arm/dp/MemtoRegW
/testbench/dut/arm/dp/PCSrcW
/testbench/dut/arm/dp/RegWriteW
/testbench/dut/arm/dp/PCPlus4F
/testbench/dut/arm/RegSrcD
00
/testbench/dut/arm/ImmSrcD
/testbench/dut/arm/ALUControlE
/testbench/dut/arm/ALUSrcE
1
Now
90 ps
Cursor 1
60 ps
40 ps
50 ps
60 ps
70 ps
Wave
Memory ...m/dp/rf/rf

ADD R5, R5, R4 ;R5 = 4 + 7 = 11 E0855004 (Data forwarding)

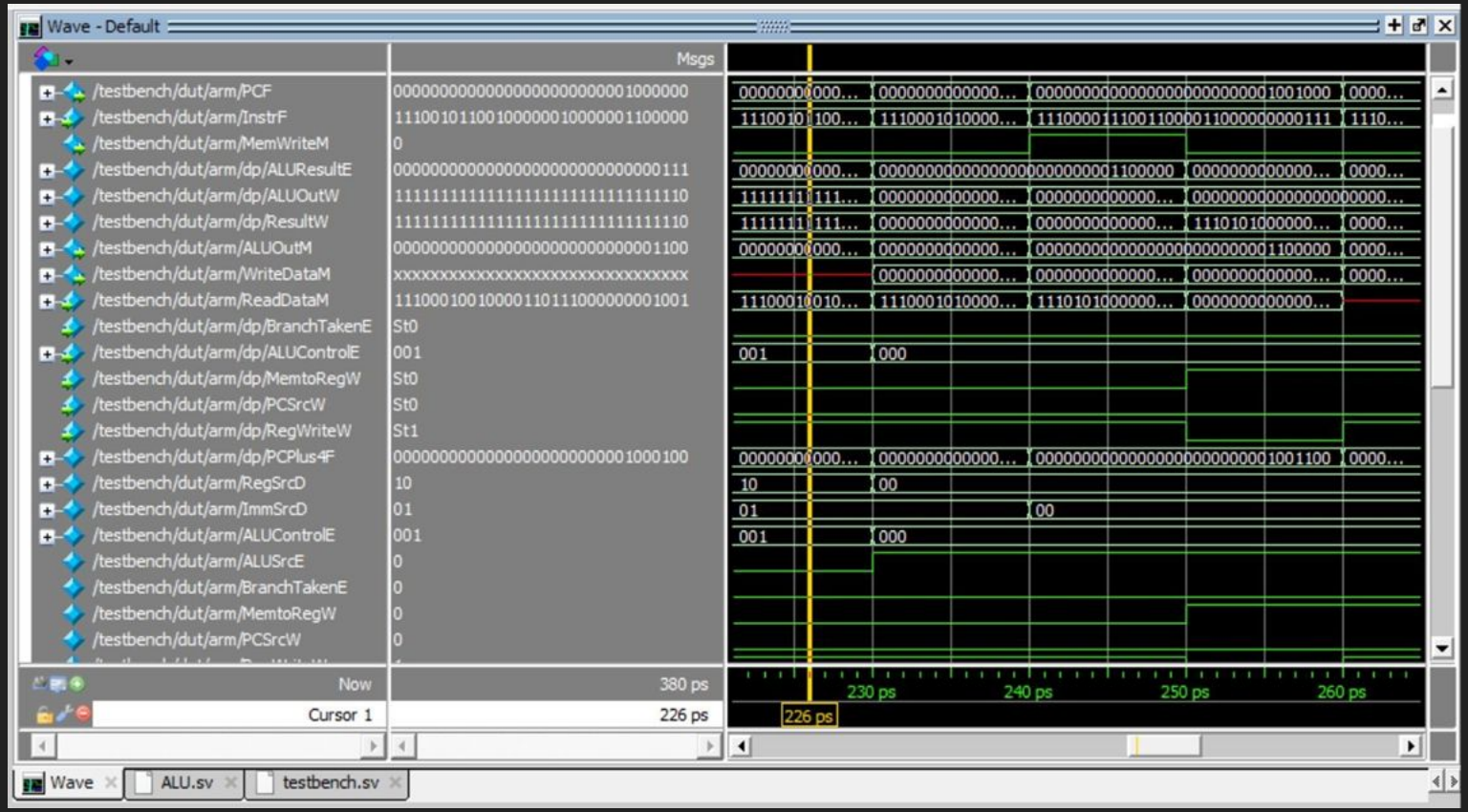


SUBS R8, R7, R2 ; R8=3-5=-2,setFlags E0578002 (n flag = 1)

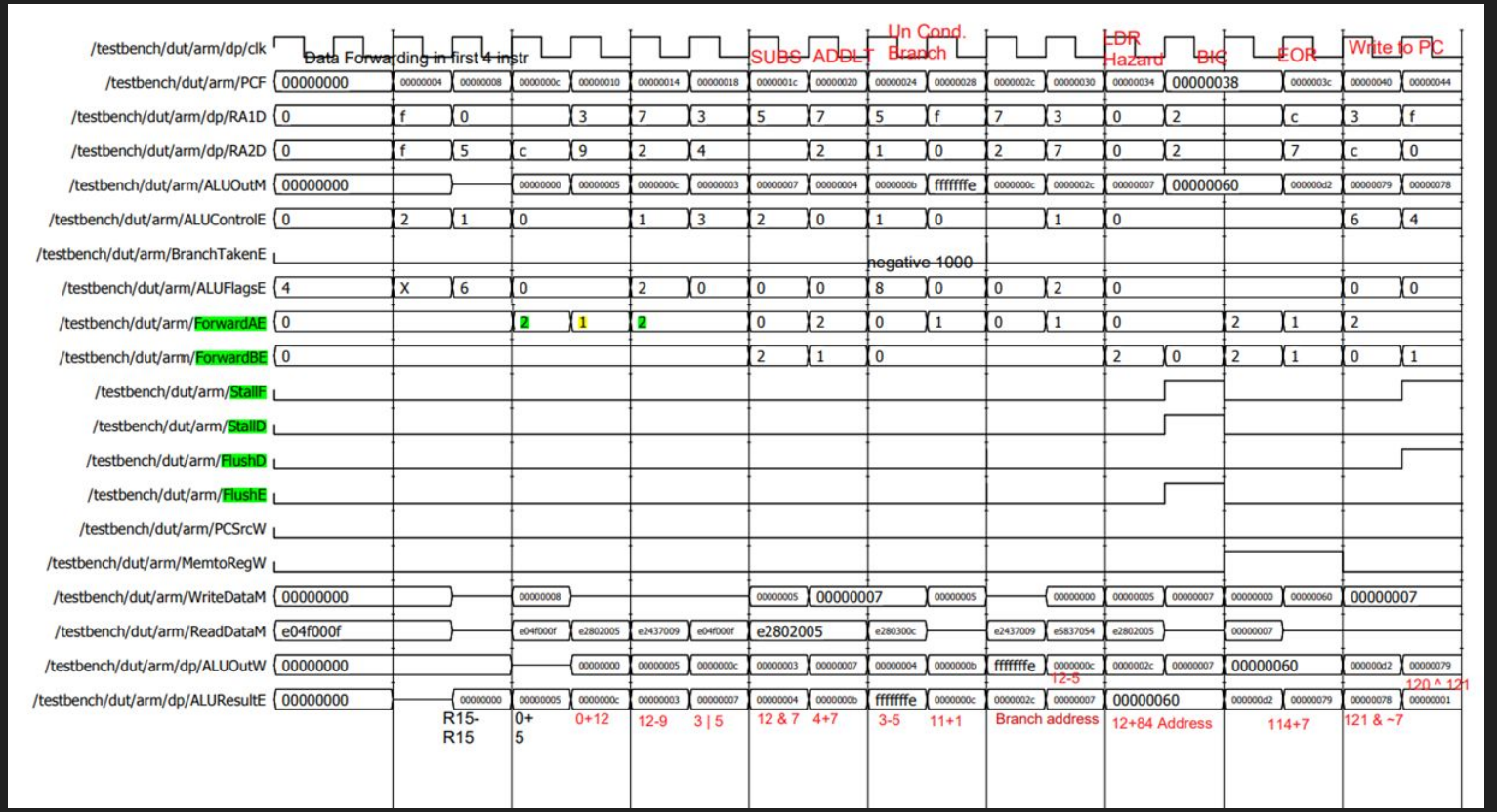



Wave - Default
Msgs
/testbench/dut/arm/clk
/testbench/dut/arm/reset
/testbench/dut/arm/PCF
/testbench/dut/arm/InstrF
/testbench/dut/arm/MemWriteM
/testbench/dut/arm/dp/ALUResultE
/testbench/dut/arm/dp/ALUOutW
/testbench/dut/arm/dp/ResultW
/testbench/dut/arm/ALUOutM
/testbench/dut/arm/WriteDataM
/testbench/dut/arm/ReadDataM
/testbench/dut/arm/dp/BranchTakenE
/testbench/dut/arm/dp/ALUControlE
/testbench/dut/arm/dp/MemtoRegW
/testbench/dut/arm/dp/PCSrcW
/testbench/dut/arm/dp/RegWriteW
/testbench/dut/arm/dp/PCPlus4F
/testbench/dut/arm/RegSrcD
/testbench/dut/arm/ImmSrcD
/testbench/dut/arm/ALUControlE
/testbench/dut/arm/ALUSrcE
/testbench/dut/arm/BranchTakenE
/testbench/dut/arm/MemtoRegW
/testbench/dut/arm/PCSrcW
/testbench/dut/arm/RegWriteW
/testbench/dut/arm/ALUFlagsE
[3]
Now
220 ps
Cursor 1
206 ps
80 ps
190 ps
200 ps
210 ps
220 ps
206 ps
Memory ...m/dp/rf/rf
Wave
ALU.sv

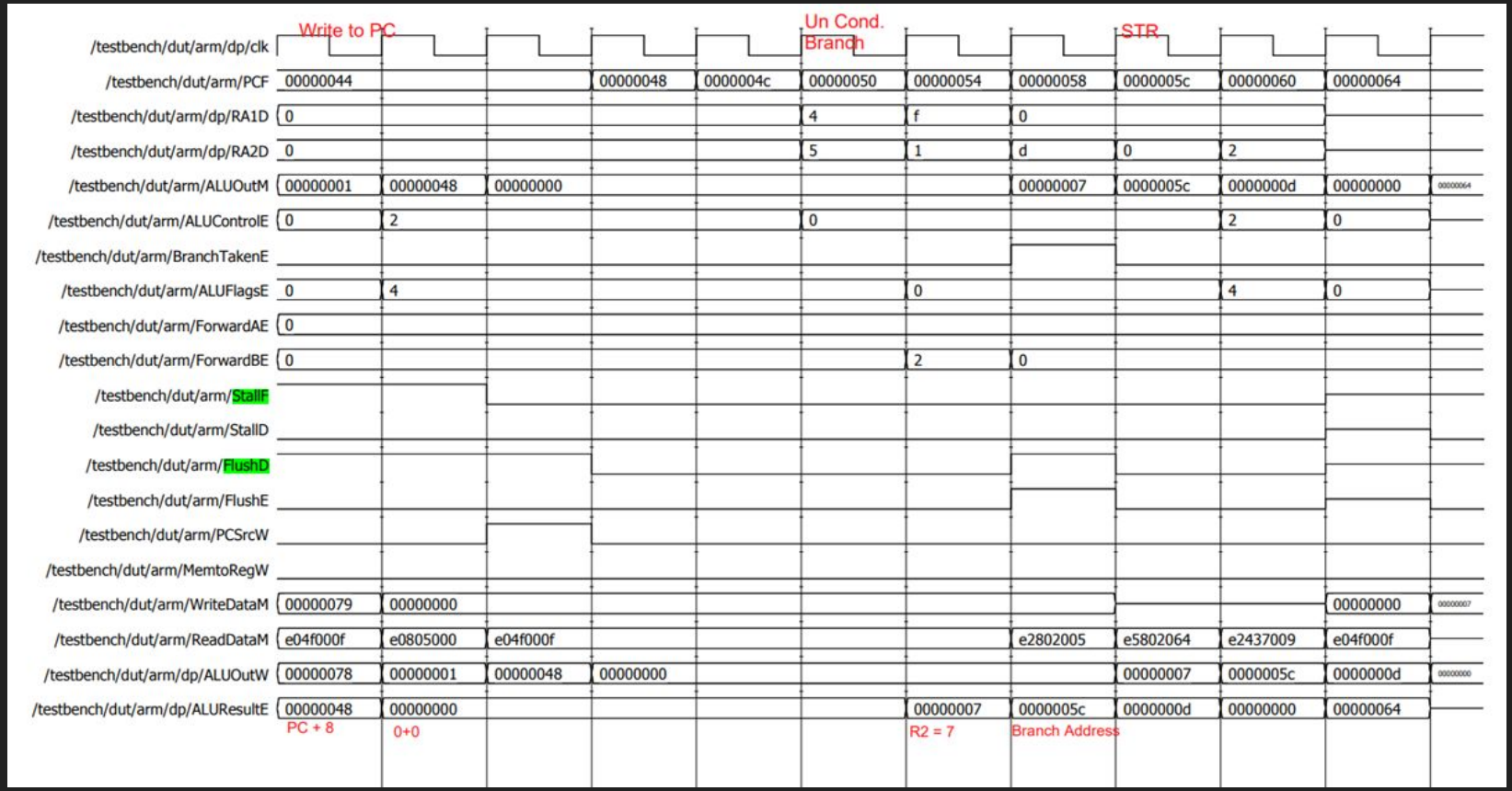
LDR R2, [R0, #96] ; R2 = mem[96] = 7 E5902060



Full simulation



Full simulation



THANK YOU !