Quantum algorithms are meant to leverage the promising power of quantum computers [5]. Commonly described as quantum circuits, quantum algorithms are hardware agnostic [13]. Due to the variety of technologies that emerged to build quantum memories, the algorithms tend to be as theoretical as possible. From ion traps [? paper on ion traps] to superconducting qubit [2], through quantum dots [8, 10], each layout has its own requirements and constraints. Also, the qubit chip layouts from IBM [9], Google [3] and Rigetti [15] are quite limited.

Moreover, quantum devices – no matter which technology – are error prone. Quantum operations are faulty and qubits are not able to hold the desired state for long times, gradually rotating to another state – the qubit decoheres. [some numbers for the technologies] [14]. This creates an undesirable environment to compute the most useful algorithms. Therefore, in order to fight the errors generated by this behaviour, fault-tolerant (FT) and quantum error correction (QEC) mechanisms have been developed during the last years [13] [? papers on error correction]. These techniques force the quantum chips layout to arrange the qubits in a particular manner [16], constraining them even more.

A link between the algorithms and the devices is required [7] thus. As in classical computation, the algorithms should go through a compilation process in order to adapt them to the hosting device. Certainly, the mapping procedure is an important part of this process based on three sub-tasks, scheduling, initial placement and routing; as we considered before.

There is a considerable amount of literature on the mapping task. Initial works on this field [12, 17, 1] focused primarily on the definition of what they defined as a *scheduler* able to parallelize operations and add the require ones to route qubits. They would consider general constraints, common for most of the hardware devices – although the works were examining ion-traps as hardware implementations. The proposed techniques examine a dependency graph looking for the best way to organize qubits and operations. The majority of the methods use latency as the metric to minimize, however some of them [6] would minimize in #SWAPS. Following a similar reasoning as the first approaches, more complex solutions [4] have been published. And, also, several works [11, 18] outlining only the routing sub-task.

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