Quantum algorithms are meant to leverage the promising power of quantum computers [5]. Commonly described as quantum circuits, quantum algorithms are hardware agnostic, which is that their behavior is not specified no any device. Due to the variety of technologies that emerged with diverse specifications, there is a vast amount of literature on the algorithms high abstraction level – forgetting hardware constraints. From ion traps [? paper on ion traps] to superconducting qubits [2, 29], through quantum dots [11, 15], each layout has its own requirements and constraints. Although all of them are arranged in a 2D – planar – structure, ion traps technologies are capable to connect the qubits in all-to-all networks while superconducting technologies connections form a grid shaped network where each qubit is connected to a maximum of four neighbors. This grid behaviour establishes one of the main limitation in today's quantum chips, the NN constraint. Also, another superconducting-based qubit chip layouts from IBM [13], Google [3] and Rigetti [25] follow this structural limitations.

Thus, a link between the algorithms and the devices is required [9]. As in classical computation, the algorithms should go through a compilation process in order to adapt them to the hosting device. Certainly, the mapping procedure is an important part of this process based on three sub-tasks: scheduling, initial placement and routing; as we considered before.

There is a considerable amount of literature on the mapping task. Initial works on this field [18, 30, 1] focused primarily on the definition of what they characterized a *scheduler* able to parallelize operations and add the require ones to route qubits. They would consider general constraints, common for most of the hardware devices – although the works were examining ion-traps as hardware implementations. The proposed techniques examine a dependency graph looking for the best way to organize qubits and operations. The majority of the methods use latency as the metric to minimize, however some of them [8] would minimize in number of SWAP operations. Following a similar reasoning as the first approaches, more complex solutions [4] have been published. Also, several publications [16, 31] outlining only the routing sub-task using the number of SWAPS as the metric to minimize. A recent review of the literature on the mapping topic [32, 26, 17, 7, 28] focused on device specific mapping algorithms, with promising results.

In addition to the previous limitations, quantum devices – no matter which technology – are error prone. Quantum operations are faulty and qubits are not able to hold the desired state for long times, gradually rotating to another state – the qubit decoheres. [some numbers for the technologies] [21].

This creates an undesirable environment to compute the most useful algorithms. Therefore, in order to fight the errors generated by this behaviour, fault-tolerant (FT) and quantum error correction (QEC) mechanisms have been developed during the last years [20] [? papers on error correction]. These techniques force the quantum chips layout to arrange the qubits in a particular manner, constraining them even more.

Many attempts have been made [6, 10, 12, 19, 14] with the purpose of develop a FT mapping able to work at the logical – qubit – level. However, due to the high complexity of the QEC techniques, quantum chips with large amounts of qubits are still theory. More recent evidence [24], proposes the Noisy Intermediate-Scale Quantum (NISQ) devices as the next step for near future hardware with an amount of 50-100 qubits and without QEC or much simpler encodings. Several studies, for instance [27, 23, 22], have been conducted on the mapping algorithms required for NISQ devices.

References

[1] Tayebeh Bahreini and Naser Mohammadzadeh. An minlp model for scheduling and placement of quantum circuits with a heuristic solution approach. *ACM Journal on Emerging Technologies in Computing Systems*, 12(3):1–20, Sep 2015.

[2] R. Barends, J. Kelly, A. Megrant, A. Veitia, D. Sank, E. Jeffrey, T. C. White, J. Mutus, A. G. Fowler, B. Campbell, and et al. Superconducting quantum circuits at the surface code threshold for fault tolerance. *Nature*, 508(7497):500–503, Apr 2014.

[3] Sergio Boixo, Sergei V. Isakov, Vadim N. Smelyanskiy, Ryan Babbush, Nan Ding, Zhang Jiang, Michael J. Bremner, John M. Martinis, and Hartmut Neven. Characterizing Quantum Supremacy in Near-Term Devices, 2016.

[4] Kyle E. C. Booth, Minh Do, J. Christopher Beck, Eleanor Rieffel, Davide Venturelli, and Jeremy Frank. Comparing and Integrating Constraint Programming and Temporal Planning for Quantum Circuit Compilation, 2018.

[5] Patrick J. Coles, Stephan Eidenbenz, Scott Pakin, Adetokunbo Adedoyin, John Ambrosiano, Petr Anisimov, William Casper, Gopinath Chennupati, Carleton Coffrin, Hristo Djidjev, David Gunter, Satish

Karra, Nathan Lemons, Shizeng Lin, Andrey Lokhov, Alexander Malyzhenkov, David Mascarenas, Susan Mniszewski, Balu Nadiga, Dan O'Malley, Diane Oyen, Lakshman Prasad, Randy Roberts, Phil Romero, Nandakishore Santhi, Nikolai Sinitsyn, Pieter Swart, Marc Vuffray, Jim Wendelberger, Boram Yoon, Richard Zamora, and Wei Zhu. Quantum Algorithm Implementations for Beginners, 2018.

[6] Mohammad Javad Dousti, Alireza Shafaei, and Massoud Pedram. Squash. *Proceedings of the 24th edition of the great lakes symposium on VLSI - GLSVLSI '14*, 2014.

[7] Gerhard W Dueck, Anirban Pathak, Md Mazder Rahman, Abhishek Shukla, and Anindita Banerjee. Optimization of circuits for ibm's five-qubit quantum computers. *2018 21st Euromicro Conference on Digital System Design (DSD)*, Aug 2018.

[8] Azim Farghadan and Naser Mohammadzadeh. Quantum circuit physical design flow for 2d nearest-neighbor architectures. *International Journal of Circuit Theory and Applications*, 45(7):989–1000, Mar 2017.

[9] X. Fu, L. Riesebos, L. Lao, C. G. Almudever, F. Sebastiano, R. Versluis, E. Charbon, and K. Bertels. A heterogeneous quantum computer architecture. *Proceedings of the ACM International Conference on Computing Frontiers - CF '16*, 2016.

[10] Jeff Heckey, Shruti Patil, Ali JavadiAbhari, Adam Holmes, Daniel Kudrow, Kenneth R. Brown, Diana Franklin, Frederic T. Chong, and Margaret Martonosi. Compiler management of communication and parallelism for quantum computation. *ACM SIGPLAN Notices*, 50(4):445–456, Mar 2015.

[11] Charles D. Hill, Eldad Peretz, Samuel J. Hile, Matthew G. House, Martin Fuechsle, Sven Rogge, Michelle Y. Simmons, and Lloyd C. L. Hollenberg. A surface code quantum computer in silicon. *Science Advances*, 1(9):e1500707, Oct 2015.

[12] Yongsoo Hwang and Byung-Soo Choi. Hierarchical System Mapping for Large-Scale Fault-Tolerant Quantum Computing, 2018.

[13] IBM. Ibm q experience backend information. `https://github.com/QISKit/ibmqx-backend-information`, 2018.

[14] L Lao, B van Wee, I Ashraf, J van Someren, N Khammassi, K Bertels, and C G Almudever. Mapping of lattice surgery-based quantum cir-

cuits on surface code architectures. *Quantum Science and Technology*, 4(1):015005, Sep 2018.

[15] Ruoyu Li, Luca Petit, David P. Franke, Juan Pablo Dehollain, Jonas Helsen, Mark Steudtner, Nicole K. Thomas, Zachary R. Yoscovits, Kanwal J. Singh, Stephanie Wehner, and et al. A crossbar network for silicon quantum dot qubits. *Science Advances*, 4(7):eaar3960, Jul 2018.

[16] Aaron Lye, Robert Wille, and Rolf Drechsler. Determining the minimal number of swap gates for multi-dimensional nearest neighbor quantum circuits. *The 20th Asia and South Pacific Design Automation Conference*, Jan 2015.

[17] David C. McKay, Thomas Alexander, Luciano Bello, Michael J. Biercuk, Lev Bishop, Jiayin Chen, Jerry M. Chow, Antonio D. Córcoles, Daniel Egger, Stefan Filipp, Juan Gomez, Michael Hush, Ali Javadi-Abhari, Diego Moreda, Paul Nation, Brent Paulovicks, Erick Winston, Christopher J. Wood, James Wootton, and Jay M. Gambetta. Qiskit Backend Specifications for OpenQASM and OpenPulse Experiments, 2018.

[18] Tzvetan S. Metodi, Darshan D. Thaker, Andrew W. Cross, Frederic T. Chong, and Isaac L. Chuang. Scheduling physical operations in a quantum information processor. *Quantum Information and Computation IV*, May 2006.

[19] Daniel C. Murphy and Kenneth R. Brown. Controlling error orientation to improve quantum algorithm success rates, 2018.

[20] Michael A. Nielsen and Isaac L. Chuang. Quantum computation and quantum information. 2009.

[21] T. E. O'Brien, B. Tarasinski, and L. DiCarlo. Density-matrix simulation of small surface codes under current and projected experimental noise. *npj Quantum Information*, 3(1), Sep 2017.

[22] Alexandru Paler. On the Influence of Initial Qubit Placement During NISQ Circuit Compilation, 2018.

[23] Alexandru Paler, Alwin Zulehner, and Robert Wille. NISQ circuit compilers: search space structure and heuristics, 2018.

[24] John Preskill. Quantum computing in the nisq era and beyond. *Quantum*, 2:79, Aug 2018.

[25] Eyob A. Sete, William J. Zeng, and Chad T. Rigetti. A functional architecture for scalable quantum computing. *2016 IEEE International Conference on Rebooting Computing (ICRC)*, Oct 2016.

[26] Marcos Yukio Siraichi, Vinícius Fernandes dos Santos, Sylvain Collange, and Fernando Magno Quintao Pereira. Qubit allocation. *Proceedings of the 2018 International Symposium on Code Generation and Optimization - CGO 2018*, 2018.

[27] Swamit S. Tannu and Moinuddin K. Qureshi. A Case for Variability-Aware Policies for NISQ-Era Quantum Computers, 2018.

[28] Davide Venturelli, Minh Do, Eleanor Rieffel, and Jeremy Frank. Compiling quantum circuits to realistic hardware architectures using temporal planners. *Quantum Science and Technology*, 3(2):025004, Feb 2018.

[29] R. Versluis, S. Poletto, N. Khammassi, B. Tarasinski, N. Haider, D.J. Michalak, A. Bruno, K. Bertels, and L. DiCarlo. Scalable quantum circuit and control for a superconducting surface code. *Physical Review Applied*, 8(3), Sep 2017.

[30] Mark Whitney, Nemanja Isailovic, Yatish Patel, and John Kubiatowicz. Automated generation of layout and control for quantum circuits. *Proceedings of the 4th international conference on Computing frontiers - CF '07*, 2007.

[31] Robert Wille, Oliver Keszocze, Marcel Walter, Patrick Rohrs, Anupam Chattopadhyay, and Rolf Drechsler. Look-ahead schemes for nearest neighbor optimization of 1d and 2d quantum circuits. *2016 21st Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan 2016.

[32] Alwin Zulehner, Alexandru Paler, and Robert Wille. An Efficient Methodology for Mapping Quantum Circuits to the IBM QX Architectures, 2017.