Contents

Compilers

References

1 List of papers for the State of the Art

1.1 Quantum Technologies

1.1.1 Superconducting

1. [?]
2. Superconducting Surface Code [?]

1.1.2 Quantum dots

1. [?]
2. [?]

1.1.3 Other chips

1. Google
   (a) [?]
2. IBM
   (a) [?]
3. Rigetti
   (a) [?]

1.2 Metrics for quantum computation quality

1.2.1 Quantum Volume

1. [?]

1.2.2 Probability of success

1. [?]

1.3 Mapping

1.3.1 General (for any device) mapping solutions

1. [?] (general but based on ion traps) (Results based on QEC encoders)

   Mapping as an algorithm (QPOS) solving the whole problem of mapping, (except the initial placement)?

2. [?] (general but based on ion traps) (Results based on QEC encoders) (whole compiler flow)

   Computer-aided design (CAD) flow to automate the laying out of a quantum circuit to generate a physical layout, an intelligent initial placement of qubits, the associated classical control logic (HDL) and annotations to help the online scheduler better use the layout optimizations as they were intended.

3. [?] (general but based on ion traps)

   Mapping that starts to care about the larger circuits.

   A mixed integer nonlinear programming model is proposed for placement and scheduling. It is proved to be NP-complete combinatorial optimization, impossible to find optimal solution for large quantum circuits within a reasonable amount of time. Therefore, a metaheuristic solution method is developed (Generic Algorithm (GA) and tabu search (TS). They split for the first time scheduling and placement.

4.

5. [?] (general but based on ion-traps) (whole compiler flow) (what is the order? is the scheduling?)

   A flow for physical design of quantum circuits on a 2D grid is proposed. It contains three algorithms for finding the order of qubit placement, physical qubit placement, and routing.

   Better than PACQS [?]

6. ? [?] (but using Rigetti's as an example)

   The previous work of cite:booth18:compar$_{\mathrm{integ\,const\,progr\,tempor}}$ where the temporal planner is coming from

7. [?] (but using Rigetti's as an example) They use Constraint Programming together with temporal planning. An hybrid solution

1.3.2 Only Routing (General)

1. [?]

   Exact scheme for nearest neighbor optimization in multi-dimensional quantum circuits.

2. [?]

   Routing looking-ahead

1.3.3 FT Mapping

1. [?]
2. [?]

1.3.4 ? Mapping with QEC (Logical Qubits mapping)

1. [?]

1.3.5 ? Mapping for NISQ devices

1. [?]
2. [?]
3. [?]

1.3.6 ? Distributed Quantum Computing

[?]

1.3.7 Ion traps mapping or general?

1. [?]
2. [?] (general but based on ion trap technology) (Design flow) (Divides the problem in scheduling and initial placement/routing as a layout export) (Results on both QEC encoders and normal benchmarks)

   Schedule a quantum application and generate the layout while taking into account the cost of communications and classical resources as well as the maximum exploitable parallelism.

1.3.8 IBM's chip mapping

1. [?]
2. [?]
3. [?]
4. [?]

1.3.9 Rigetti's chip mapping

1. [?]

1.3.10 Google's chip mapping?

1.4 NISQ

1.4.1 [?]

1.5 ? Compilers

1.5.1 [?]