Quantum algorithms are meant to leverage the promising power of quantum computers [5]. Commonly described as quantum circuits, quantum algorithms are hardware agnostic [20]. Due to the variety of technologies that emerged to build quantum memories, the algorithms tend to be as theoretical as possible. From ion traps [? paper on ion traps] to superconducting qubit [2], through quantum dots [11, 15], each layout has its own requirements and constraints. Also, the qubit chip layouts from IBM [13], Google [3] and Rigetti [25] are quite limited.

Moreover, quantum devices – no matter which technology – are error prone. Quantum operations are faulty and qubits are not able to hold the desired state for long times, gradually rotating to another state – the qubit decoheres. [some numbers for the technologies] [21]. This creates an undesirable environment to compute the most useful algorithms. Therefore, in order to fight the errors generated by this behaviour, fault-tolerant (FT) and quantum error correction (QEC) mechanisms have been developed during the last years [20] [? papers on error correction]. These techniques force the quantum chips layout to arrange the qubits in a particular manner [29], constraining them even more.

Thus, a link between the algorithms and the devices is required [9]. As in classical computation, the algorithms should go through a compilation process in order to adapt them to the hosting device. Certainly, the mapping procedure is an important part of this process based on three sub-tasks: scheduling, initial placement and routing; as we considered before.

There is a considerable amount of literature on the mapping task. Initial works on this field [18, 30, 1] focused primarily on the definition of what they characterizedp a *scheduler* able to parallelize operations and add the require ones to route qubits. They would consider general constraints, common for most of the hardware devices – although the works were examining ion-traps as hardware implementations. The proposed techniques examine a dependency graph looking for the best way to organize qubits and operations. The majority of the methods use latency as the metric to minimize, however some of them [8] would minimize in number of SWAP operations. Following a similar reasoning as the first approaches, more complex solutions [4] have been published. Also, several publications [16, 31] outlining only the routing sub-task using the number of SWAPS as the metric to minimize. A recent review of the literature on the mapping topic [32, 26, 17, 7, 28] focused on device specific mapping algorithms, with promising results.

Many attempts have been made [6, 10, 12, 19, 14] with the purpose of develop a FT mapping able to work at the logical – qubit – level. However, due to the high complexity of the QEC techniques, quantum chips with large amounts of qubits are still theory. More recent evidence [24], proposes the Noisy Intermediate-Scale Quantum (NISQ) devices as the next step for near future hardware with an amount of 50-100 qubits and without QEC or much simpler encodings. Several studies, for instance [27, 23, 22], have been conducted on the mapping algorithms required for NISQ devices.

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