Ultra-Low Power Single-Chip USB 2.0 to 10/100M Ethernet Controller

General Description

The Supereal SR9900 10/100M Ethernet controller combines an IEEE 802.3u compliant Media Access Controller (MAC), USB bus controller, and embedded memory. A linear regulator (LDO) is incorporated for reduced BOM cost.

With state-of-the-art DSP technology and mixed-mode signal technology, the SR9900 offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capabilities. The SR9900 features embedded One-Time-Programmable (OTP) memory.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-Up Frame) is supported in both ACPI and APM (Advanced Power Management) environments.

The SR9900 supports Microsoft Wake Packet Detection (WPD) to provide Wake-Up Frame information to the OS, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPD helps prevent unwanted/ unauthorized wake-up of a sleeping computer.

The SR9900 is fully compliant with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The SR9900 supports Protocol offload. It offloads some of the most common protocols to NIC hardware in order to prevent spurious wake-up and further reduce power consumption. The SR9900 can offload ARP (IPv4) and NS (IPv6) protocols while in the D3 power saving state.

The SR9900 supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The SR9900 also features USB 2.0 technology. It provides higher bandwidth and improved protocols for data exchange between the host and the device. In addition, USB 2.0 offers a more aggressive power management feature that enables selective suspend to save energy.

The SR9900 is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, docking station, and embedded applications.

Features

- Supports USB 2.0 and 1.1
- Integrated 10/100M transceiver
  - Supports Full Duplex flow control (IEEE 802.3x)
  - Fully compliant with IEEE 802.3, IEEE 802.3u
  - Supports IEEE 802.1P Layer 2 Priority Encoding
  - Supports IEEE 802.1Q VLAN tagging
  - Supports IEEE 802.3az-2010 (EEE)
  - Auto-Negotiation with Next Page capability
- Microsoft AOAC (Always On Always Connected)
  - Supports Wake-Up Frame pattern exact matching
  - Supports link change wake up
  - Supports Microsoft WPD (Wake Packet
  - Detection)
  - Supports Protocol Offload (ARP & NS)
- Microsoft NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send v1 and Large send v2) support
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Standard for sleeping hosts (see note 1)
- XTAL-Less Wake-On-LAN
- Supports 25MHz external clock (from oscillator or system clock source)
- Supports power down/link down power saving
- Transmit/Receive on-chip buffer support
- Embedded OTP memory
- Low power supply 1.2V 3.3V and 5.0V; 1.2V and 3.3V are generated by internal linear regulator (LDO)
- Supports Customizable LEDs
- Controllable LED Blinking Frequency and Duty Cycle
- Supports hardware CRC (Cyclic Redundancy Check) function
- LAN disable with GPIO pin
- Supports LPM (Link Power Management)
- SPI Flash Interface
- Supports CDC-ECM
- 24-pin QFN ‘Green’ package
- 0.11µm CMOS process

Application

- USB Dongle
- Network Printer
- Card Reader for payment
- Docking Station
- Port Replicator for Mobile Computer
- Internet Security USB Key
- Media Gateway
- Pocketable Computer
- Portable Media Player
- TiVo Box
- Game Console
- IP STB
- DVD-Recorder/DVR
- IPTV

Block Diagram

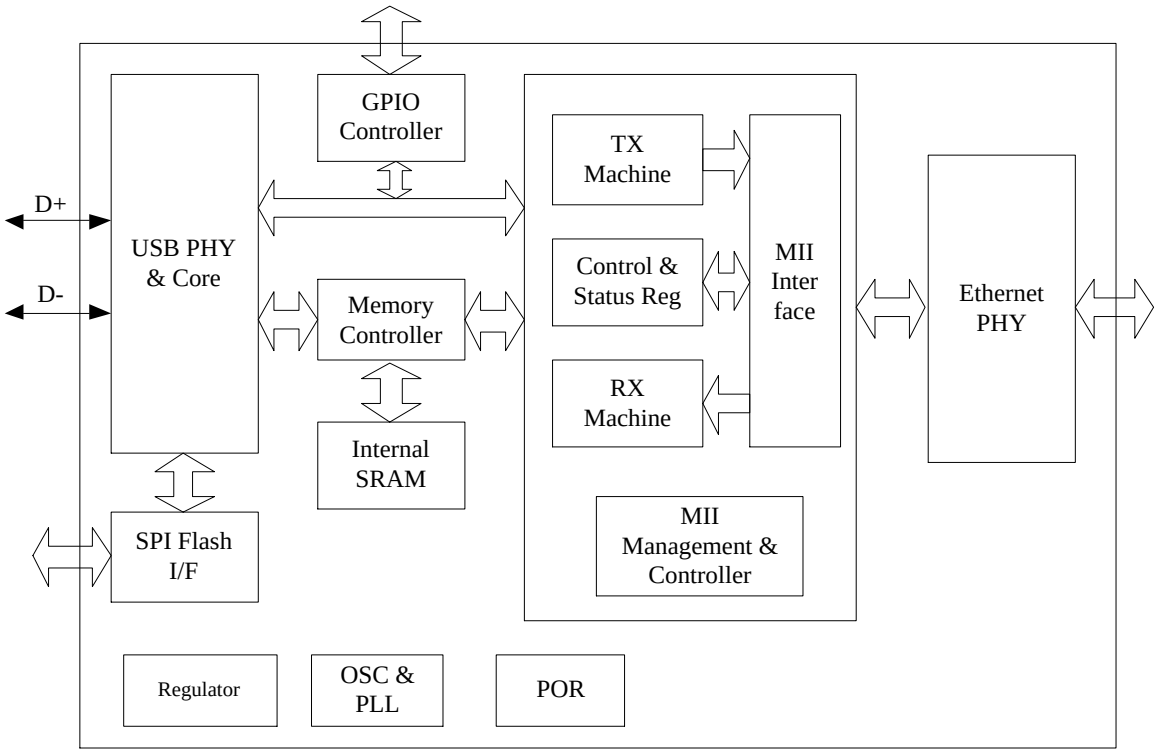


Figure 1. Block Diagram

Pin Assignment

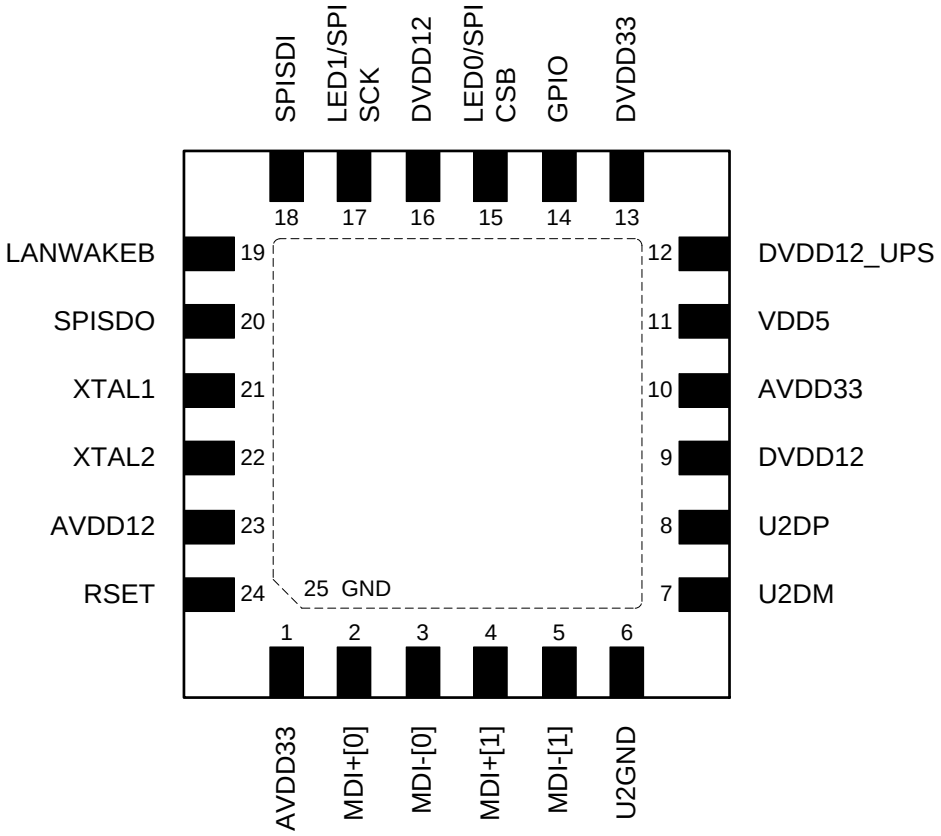


Figure2. Pin Assignments

Pin Descriptions

Pin No	Symbol	Type	Description
2,3	MDI+[0]、MDI-[0]	I/O	In MDI mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
4,5	MDI+[1]、MDI-[1]	I/O	In MDI mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
24	RSET	I	Reference input. For external resistor reference
22	XTAL2	O	Output of 25MHz Clock Reference
21	XTAL1	I	Input of 25MHz Clock Reference
8	U2DP	I/O	USB 2.0/USB 1.1 Differential Signal Pair
7	U2DM	I/O	
19	LANWAKEB	O	Power Management Event Output Pin (Active Low)
15	LED0	O	Customizable LED0
17	LED1	O	Customizable LED1
15	SPICSB	O	SPI Flash Chip Select
20	SPISDO	I	Input from SPI Flash Serial Data Output Pin
18	SPISDI	O	Output to SPI Flash Serial Data Input Pin
17	SPISCK	O	SPI Flash Serial Data Clock
14	GPIO	I/O	General Purpose Input/Output Pin
6	U2GND	P	USB Ground
25	GND	P	Ground (Exposed Pad)
11	VDD5	P	LDO 5.0V Power Supply
10	AVDD33	P	Analog 3.3V Power Supply
12	DVDD12_UPS	P	Digital 1.2V Uninterruptible Power Supply
1	AVDD33	P	Analog 3.3V Power Supply
13	DVDD33	P	Digital 3.3V Power Supply
23	AVDD12	P	Analog 1.2V Power Supply
16	DVDD12	P	Digital 1.2V Power Supply
9	DVDD12	P	USB Digital 1.2V Power Supply

I=Input, O=Output, IO= Bi-directional input and output, P=Power

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Range	Units
5.0V Supply Voltage	V_{DD5}	-0.3 ~ 5.5	V
3.3V Supply Voltage	DV_{DD33} AV_{DD33}	-0.3 ~ 3.63	V
1.2V Supply Voltage	AV_{DD12} V_{DD12} DV_{DD12_UPS}	-0.3 ~ 1.35	V
Input/ Output Voltage	V_{I33}/V_{O33}	-0.3 ~ DV_{DD33}+0.3	V
Storage Temperature Range	Tstg	-55 ~ 125	^{o}C

Recommend Operation Conditions

Parameter	Symbol	Range	Units
5.0V Supply Voltage	V_{DD5}	4.75 ~ 5.25	V
3.3V Supply Voltage	DV_{DD33} AV_{DD33}	3.14 ~ 3.46	V
1.2V Supply Voltage	AV_{DD12} DV_{DD12} DV_{DD12_UPS}	1.15 ~ 1.25	V
Input/output Voltage	V_{I33}/V_{O33}	0 ~ DV_{DD33}	V
Operating Temperature Range	Topr	0 ~ 70	^{o}C

DC Characteristics (unless otherwise specified T_{opr}=25°C, V_{DD5}=5.0V, V_{DD33}=3.3V, V_{DD12}=1.2V, V_{GND}=0V)

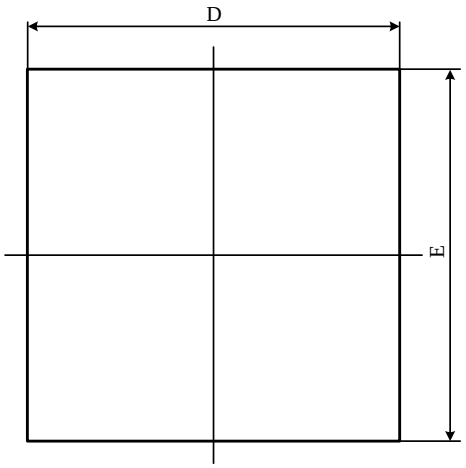
Parameter	Symbol	Condition	MIN	TYP	MAX	Units
5.0V Supply Voltage	V_{DD5}		4.2	5.0	5.5	V
3.3V Supply Voltage	DV_{DD33} AV_{DD33}		3.14	3.3	3.46	V
1.2V Supply Voltage	AV_{DD12} DV_{DD12} DV_{DD12_UPS}		1.08	1.2	1.32	V
Supply Current 1	I_{DD1}	100Base-T with heavy network traffic		75		mA
Supply Current 2	I_{DD2}	100Base-T Idle (EEE not Enable)		65		mA
Supply Current 3	I_{DD3}	100Base-T Idle with EEE		34		mA
Supply Current 4	I_{DD4}	10Base-T Full Duplex		50		mA
Supply Current 5	I_{DD5}	10Base-T Idle		30		mA
Supply Current 6	I_{DD6}	Link Down Power Saving		28		mA
AVDD33 regulator output	AV_{DD33}		3.14	3.3	3.46	V

AVDD12 regulator output	AV_{DD12}		1.08	1.2	1.32	V
DVDD12_UPS regulator output	DV_{DD12_UPS}		1.08	1.2	1.32	V
USB 2.0 Transceiver (HS)						
High speed differential input sensitivity	V_{HSDIFF}	$\|V_{I(DP)}-V_{I(DM)}\|$	300			mV
High speed data signaling common mode voltage range	V_{HSCM}		-50		500	mV
High speed squelch detection threshold	V_{HSSQ}	Squelch detected			100	mV
		No squelch detected	200			mV
High speed idle level output voltage	V_{HSQI}		-10		10	mV
High speed low level output Voltage	V_{HSOL}		-10		10	mV
High speed high level output voltage	V_{HSOH}		-360		400	mV
Chirp-J output voltage	V_{CHIPJ}		700		1100	mV
Chirp-K output voltage	V_{CHIPK}		-900		-500	mV
Driver output impedance	R_{DRV}		40.5	45	49.5	Ω
USB 1.1 Transceiver (FS/LS)						
Low-level output voltage	V_{OL}	1.5K to V_{DD33}	0		0.3	V
High-level output voltage	V_{OH}	15K to GND	2.8		3.6	V
Differential input sensitivity	V_{DI}		0.2			V
Differential common mode voltage	V_{CM}		0.8		2.5	V
Single ended receiver threshold	V_{SE}		0.8		2.0	V
Receiver capacity	C_{IN}				20	pF
Leakage current	I_{LO}		-10		+10	A
10/100M Ethernet PHY Transmitter						
Peak-to-peak differential output voltage 1	V_{PP1}	10BASE-T		3.2		V
Peak-to-peak differential output voltage 2	V_{PP2}	100BASE-TX	1.9	2.0	2.1	V
Signal rise / fall time	T_R/T_F	100BASE-TX	3	4	5	ns
Output jitter	T_{JT}	100BASE-TX Idle			1.2	ns
Overshoot	V_{OS}	100BASE-TX			5	%
Receiver input impedance	R_I			10		KΩ
Common mode input voltage	V_{CM}		1.7	2.0	2.3	V
Maximum error-free cable length	L_{RCV}		120			m
GPIO Port						
Input Voltage Low	V_{IL}				0.9	V
Input Voltage High	V_{IH}		2.0			V
Output Voltage low	V_{OL}	I_{OL}=8mA			0.4	V
Output Voltage High	V_{OH}	I_{OH}=8mA	2.4			V
Input pull-up resistance	R_{PU}		40	75	150	KΩ
Input Pull-down resistance	R_{PD}		40	75	150	KΩ
Leakage current	I_{LEAK}	V_{IN}=0 or DV_{DD33}			1	μA

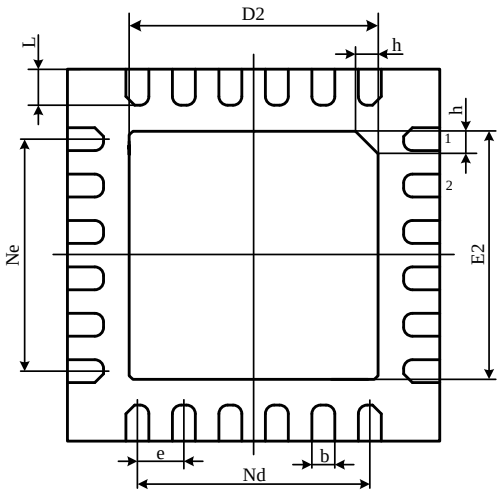
Package Diagram

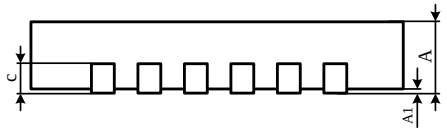
QFN24-4x4-0.50 Unit: mm

TOP VIEW



BOTTOM VIEW





Symbol	Unit (mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
A1		0.01	0.05
b		0.25	
c		0.20	
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
D	3.90	4.00	4.10
D2			2.70
E	3.90	4.00	4.10
E2			2.70
L		0.40	
h		0.30	