FM2010

Datasheet v1.94

Nov 1st 2007

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FIGURES

TABLES

Revision History

Revision	Description	Date
V1.0	Initial	2006/FEB/10th
V1.2	General	2006/MAR/14th
V1.3	Add QFN package information and update power-down current	2006/JUN/15th
V1.4	Update power-down current and add ANA_COM mode	2006/JUN/28th
V1.5	Adjust minimum V_{DD} and power down current	2006/JUL/27th
V1.51	Make Tables for minimum V_{DD} consistent at V_{DD}	2006/JUL/31st
V1.6	Revision in new format and corrective information	2006/SEP/30th
V1.7	Fixed gain table aligned with the parameter tuning guide.	2006/NOV/07th
V1.8	Update to preliminary data sheet	2006/NOV/30th
V1.9	Update package information in Section 5.	2007/MAY/20th
V1.91	Update package information	2007/SEP/15th
V1.92	Remove preliminary	2007/OCT/30th
V1.93	Incorporate comments regarding package	2007/NOV/1st
V1.94	Incorporate changes for power and processing	2007/NOV/1st

1. Introduction

Fortemedia's FM2010 is an echo canceller and noise suppressor designed with very small foot print and low power consumption for PC, navigation, and consumer applications. With the patent pending SAM (Small Array Microphone) technology, FM2010 delivers superior echo cancellation and non-stationary noise suppression with 2 closed placed microphones! The unique cone-shape beam-forming feature suppresses extreme ambient noise while reserving the voice quality to enhance the intelligibility as well as increasing the voice recognition rate. A specialized non-linear echo cancellation deployed with SAM enables small devices with integrated speakerphone and microphones in a single piece performing excellent full duplex.

Combining its low power consumption, small package size, and short distance between microphones, FM2010 is ideal for battery operated devices such as mobile phones, headsets, PND, PC Notebook, and other mobile communication devices.

1.1. Overview

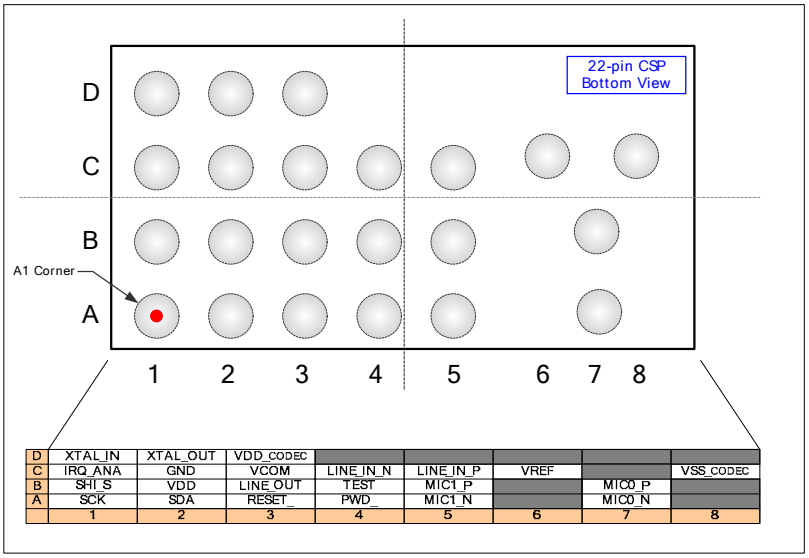
FM2010 features up to 60dB echo cancellation, up to 20dB of non-stationary noise suppression, and up to 18dB stationary noise suppression with beam-forming.FM2010 is a DSP based single chip solution integrated with Codec, ROM, RAM, and Serial Host Interface. It significantly simplifies the system design with analog only voice interface. To further lower the power consumption, FM2010 uses customized hardware accelerators to reduce the required MIPS in order to achieve 25mW of power consumption.

FM2010 also offers two package types, QFN (48pin) and CSP (22 pin), to meet various design requirements. The CSP is with only 3.93×2.04 mm² to allow designs with limited board space such as mobile phone or small modules.

1.2. Hardware Features

- Highly integrated single-chip solution :
  - Voice processor with a hardware accelerators.
  - 3 16-bit ADCs (Analog to Digital Converter) for two microphone inputs (MIC0 and MIC1) and one line-in input (LINE_IN). Each analog input channel is with 8 kHz sampling rate, 84dB SNR (Signal to Noise Ratio). And each microphone input has a built-in PGA (Programming Gain Operational Amplifier) controller as on-chip pre-amp.
  - 1 DAC (Digital to Analog Converter) for line-out output(LINE_OUT). This output is a 8 kHz sampling rate, 75 dB SNR in a single end mode.
  - Built-in RAM and ROM code. No external RAM necessary.
  - Support Analog Communication mode.
  - Software programmable gain controller is built-in in each analog input and output port.
  - 3.3V voltage tolerance for all digital inputs except the clock input (XTAL_IN).
- Low-power consumption:
  - 180 nm advanced process.
  - 2-microphone mode : ~25mW.
  - 1-microphone mode : ~20mW.
  - Analog Communication mode : ~15mW.
  - Power down mode: less than 300μA.
  - 1.8V for all analog and codec power domain.
  - 1.62V~1.8V for digital and core power domain.
- High performace:
  - Powerful AEC (acoustic echo cancellation) up to 60dB.
  - Superior full-duplex
  - Support 2 microphones and 1 microphone modes.
  - Differential analog input to reduce RF interference.
  - Acoustic echo tail length coverage : up to 100ms.
- Flexible clock sources : support crystal or external 1.8V clock source.
  - Crystal with internal clock generation circuit :
    - ✓ 13MHz.
    - ✓ 12.288MHz.
  - External clock source with 1.8V:
    - ✓ 13 MHz, 24MHz, and 48MHz.
    - ✓ 12.288 MHz.
  - Built-in PLL(Phase-Locked Loop) for the clock generation.
- External EEPROM supported through SHI interface : 24AA02 (256 bytes or other EEPROM with the same address and data format, 1.8V required).
- SHI interface supported with an external I²C compatible host controller up to 400kbps as the fast mode, and controlled by sending commands and parameters on the fly.
- Flexible package available :
  - 22-pin 3.93×2.04 mm² preprietary CSP package.
  - 48-pin 7×7 mm² standard QFN package with 0.5mm pitch.

1.3. 22-pin CSP Package Pin Configuration



D	XTAL_IN	XTAL_OUT	VDD_CODEC					
C	IRQ_ANA	GND	VCOM	LINE_IN_N	LINE_IN_P	VREF		VSS_CODEC
B	SHI_S	VDD	LINE_OUT	TEST	MIC1_P		MIC0_P	
A	SCK	SDA	RESET_	PWD_	MIC1_N		MIC0_N	
	1	2	3	4	5	6	7	8

Figure 1: 22-pin CSP Pin Configuration

1.4. 48-pin QFN Package Pin Configuration

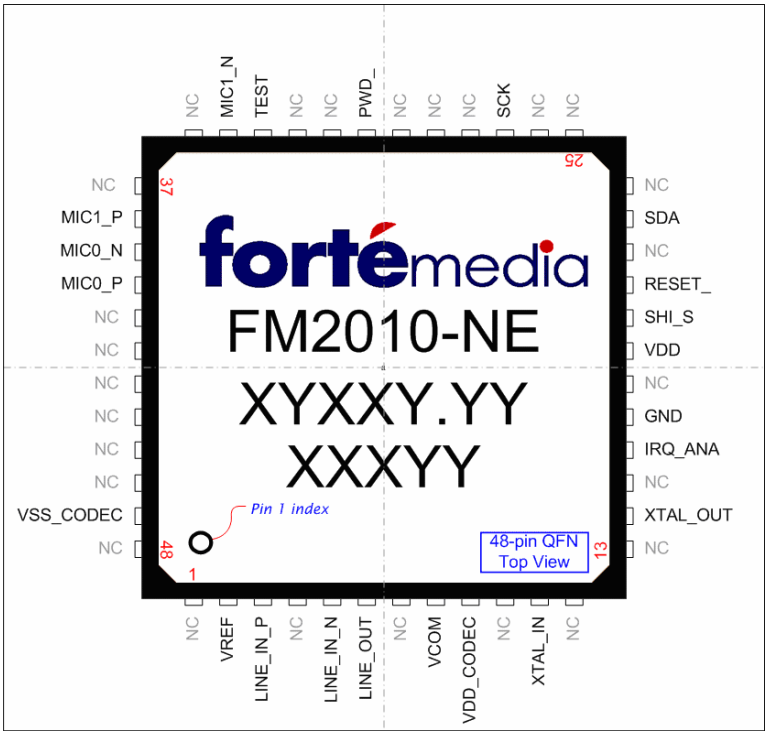


Figure 2: 48-pin QFN Pin Configuration

1.5. Internal Hardware Block Diagram

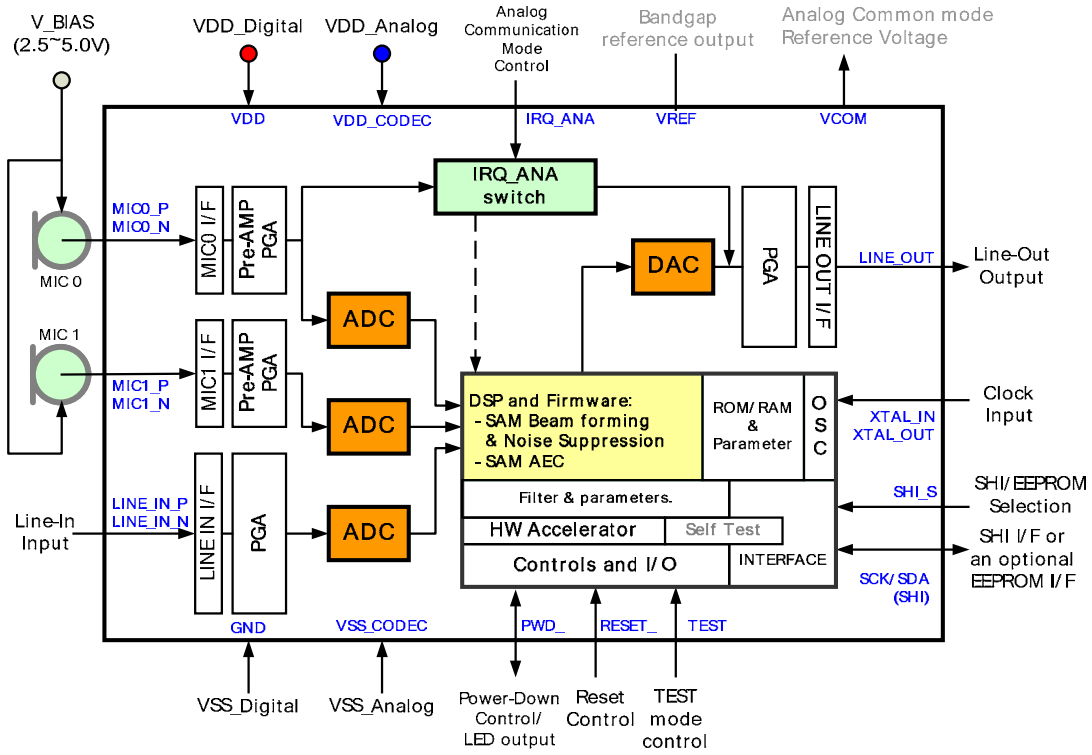


Figure 3: FM2010 Hardware Block Diagram

1.6. System Block Diagram with FM2010 am

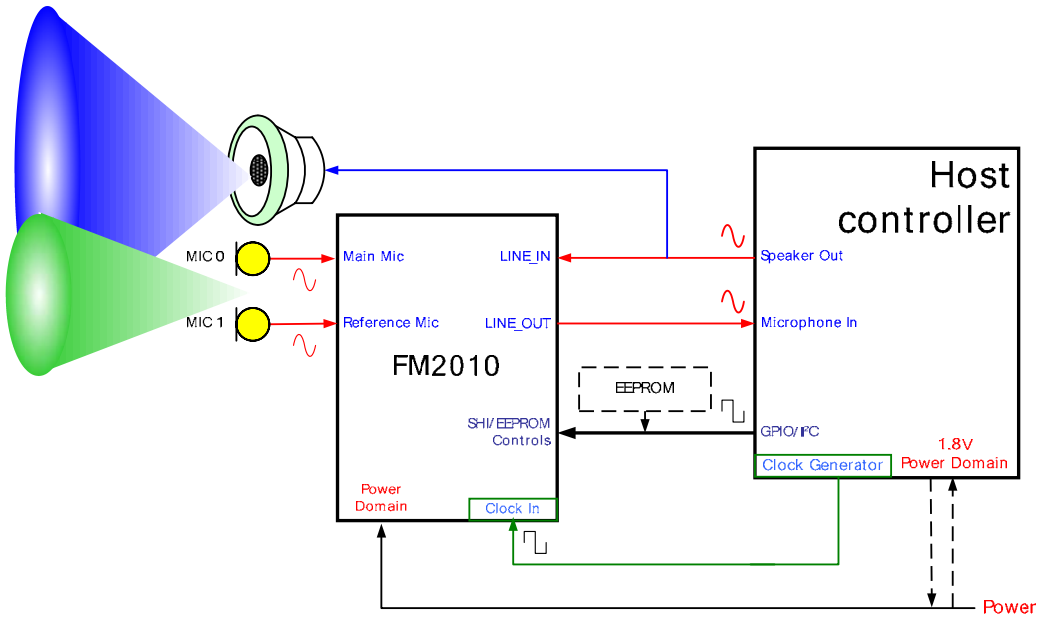


Figure 4: System Application Block Diagram

Functional Description

In this section, we describe all features and pin functions working on the FM2010.

2.1. SHI (Serial Host Interface) Mode

(Pin SCK [A1, 27], SDA [A2, 23], SHI_S [B1, 20])

The SHI Interface block is an interface to the external micro-controller (host and master device) which send control commands to FM2010 through SHI to initialize the chip or access registers on the fly. This interface supports a slave mode with an 8-bit address format and supports up to a maximum speed of 400kb/sec..

The device ID of FM2010 is **"0xC0"**. And all data are driven by transmitting party except the Acknowledge bit (ACK) which is driven by the receiving party. And the Non-Acknowledge bit (NoAck) is an open collector signal pulled–high by its bus characteristic. Refer to Figure 5.

In this mode, SHI_S [B1, 20] pin is pulled up to VCC. In this mode, FM2010 is a client in the salve mode, and controlled by an external master device such as micro-controller. SCK pin of FM2010 works as a clock input of this client from a master clock output pin (SCL) of a host controller.

In the SHI protocol (see figure 5), it always begins with a "START" or "RESTART" stage and ends with a "STOP" stage. Between "START" stage and "STOP" stage, there is a Control Byte including device ID and read/write information, Followed by a ACK symbol responded by the receiver, and NOACK (pulled high) meaning end of command.

Every SHI transaction needs a synchronized word **"0xFCF3"** to synchronize up transfer. And each transfer starts with one command entry byte, one or two address bytes, and one or two data bytes. All SHI/EEPROM pre-defined command entry bytes are listed on Table 1/2/3. Users can access the register of FM2010 through SHI. A burst write example on Figure 6.

For more details on SHI interface, please refer to *"FM2010 SHI Implement Guide"*.

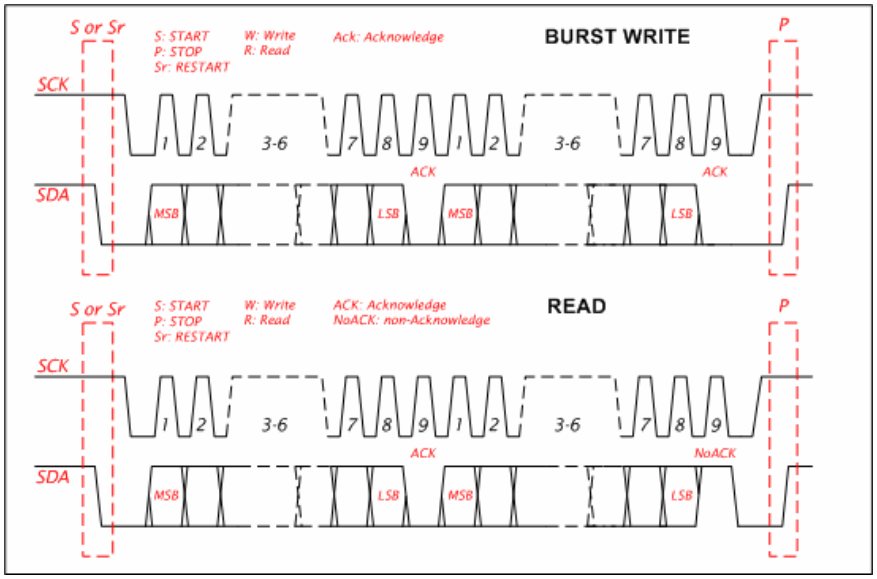


Figure 5: SHI Command Protocol with Start(S), Restart(Sr) and Stop(P)

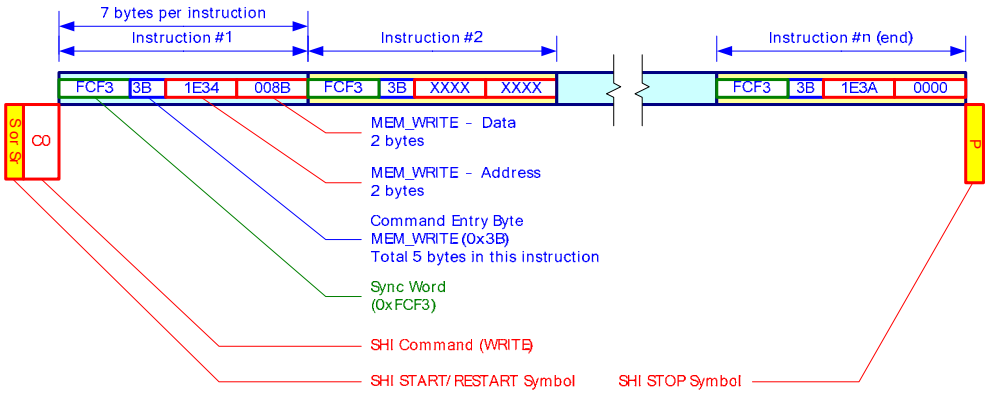


Figure 6: SHI Command sequence with "Sync" word and command entry byte

Table 1: SHI /EEPROM Command Entry Name

Command Entry Name Symbol	Command Entry Byte	Number of the bytes for each functional bytes			Available Interface
		Address Byte	Data Byte	Total (cmd+address+data)	
MEM_WRITE	0x3B	2	2	5	SHI /EEPROM
MEM_READ	0x37	2	0	3	SHI
REG_READ	0x60	1	0	2	SHI

Table 2: SHI /EEPROM Serial Command Entry Byte Descriptions (1)

Serial Command Entry Byte								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Description	Access object type				Read /Write	Data byte number		Address byte number
Value Details	Data Memory (0011b) Data Port (0110b) (e.g. Register)				R: 0 W: 1	2 bytes (01b) 1 byte (00b) 0 byte (11b)		Data Memory(1b) Date Port(0b)

Table 3: SHI /EEPROM Serial Command Entry Byte Descriptions (2)

Data length	1byte	
Bit Dx	**Pattern**	**Descriptions**
D7 - D4	0011b	For Accessing Data Memory
	0110b	For reading the Data ports (SHI only).
D3	0b	Read
	1b	Write
D2-D1	00b	1 byte data write, or in Data Port Read mode to retrieve 1 byte.
	01b	2 bytes data write
	11b	0 byte data (in Data Memory Read mode).
D0	1b	Two address bytes for accessing Data Memory
	0b	One address byte for reading Data Port (Either 0x25 for lower byte or 0x26 for upper byte.

2.2. EEPROM Mode

(Pin SCK [A1, 27], SDA [A2, 23], SHI_S [B1, 20])

In this optional mode, SHI_S pin is pulled down to GND as an EEPROM download mode. FM2010 is a master reading from an EEPROM device. The SCK is the clock output and the SCK connects to the SCL of the EEPROM. In this transmission, FM2010 device ID is still **"0xC0"** and the EEPROM device ID is **"0xA0"**. The EEPROM is powered by 1.8V. And the size is no less than 256 bytes (for instance, 24AA02). An example is shown on Figure 7.

The parameters for initial setting are down-loaded as a raw file from EEPROM in the initial stage. When the EEPROM mode is selected to initialize the parameters after reset (i.e. the power up reset or system cold reset / warm reset), EEPROM access is set to a "BURST READ" mode up to 256 bytes. The FM2010 will continuously retrieve data from EEPROM in this burst read mode until 0x1E3A is set to 0x0000. Then, FM2010 enters the normal operation mode from EEPROM download mode.

To save the board space, the SHI mode is recommended rather than the EEPROM mode.

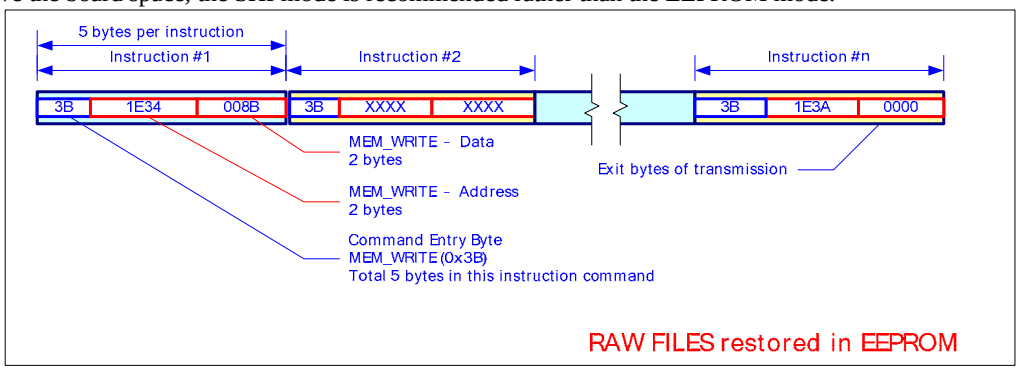


Figure 7: Command and parameter raw files stored in EEPROM

2.3. ADC (Analog to Digital Converters and Analog Inputs)

(Pin MIC0_P [B7, 40], MIC0_N [A7, 39], MIC1_P [B5, 38], MIC1_N [A5, 35], LINE_IN_P [C5, 3], LINE_IN_N [C4, 5])

The FM2010 features 3 ADCs (Ananlog-to-Digital Converter). The converters are sigma-delta ADCs with a 16-bit resolution and an 8 kHz sampling rate. All 3 coverters are differential input. And both of the microphone inputs (MIC0 and MIC1) have built-in microhphone pre-amplifiers. The line-in (LINE_IN) is used in FM2010 for the echo reference input when echo cancellation function is applied. It is connected to the line-out or speaker-out ports from the output of the audio codec system.

The differential inputs of ADCs are 2.4 V_{PP} in full scale of voltage reference. And the SNR of each differential inputs is 84dB. The ADC gain is from -2dB to +26dB with about 2 dB increments. The ADC programmable gain control table is listed on Table 4 as the following.

For details to programming the attenuation and gains of ADCs, please refer to *"FM2010 Parameters Tuning Guide"*.

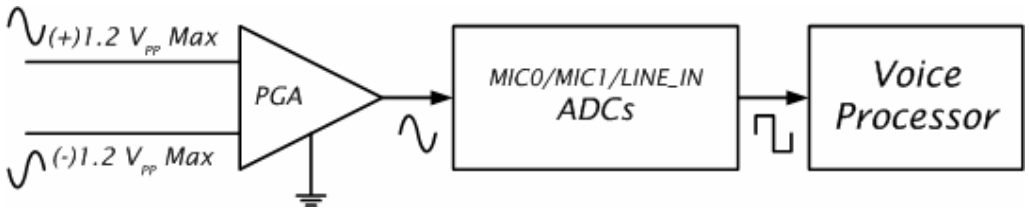


Figure 8: Analog Input Block Diagram

****Recommended Microphone Specification:**

Parameter	Value
Type	Electret Condenser Microphone Unidirectional and/or Omni-directional
Sensitivity	-44 ~ -47 dB (1V/pA)
Operating Voltage	2V (standard)
Impedance	2.2kΩ maximum

2.4. DAC (Digital to Analog Converter) and Analog Output
(Pin LINE_OUT [B3, 6])

The FM2010 also features a sigma-delta, 16 bit, DAC (Digital-to-Analog) with 8KHz sample rate. The LINE_OUT DAC provides a single-end output with programmable attenuations and gains. LINE_OUT can be connected to the analog input of the host system.
The DAC programmable gain control table is listed on Table 5 as the following. The 5 bits setting controls DAC from -29dB to +2 dB with a 1 dB increment.
For details to programming the attenuation and gains of DAC, please refer to *"FM2010 Parameters Tuning Guide"*.

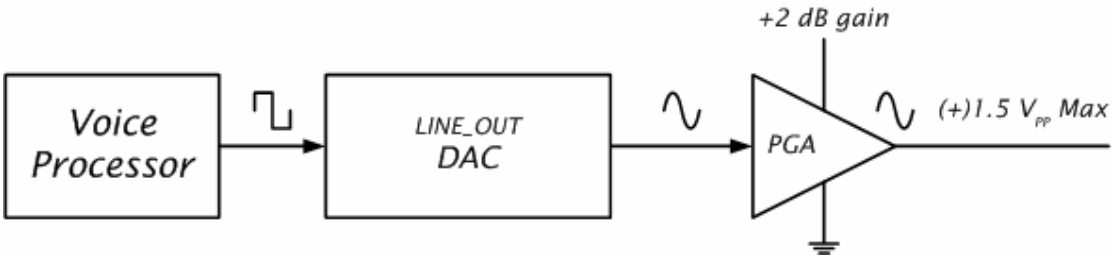


Figure 9: Analog Output Block Diagram

2.5. Power Supply
(Pin VDD [B2, 19], GND [C2, 17], VDD_CODEC [D3, 9], VSS_CODEC [C8, 47])

FM2010 has two power planes. One is a digital plane with a V_{DD} pin, and another one is an analog power plane with a V_{DD_CODEC} pin. The analog plane supplies the analog codecs and its PLL's. The digital plane supplies the DSP and I/O's. For better immunity of noise, seperating the analog and digital planes in the system board with proper ferrite beads or resistors is recommended.

2.6. Clock Source
(Pin XTAL_IN/CLK_IN [D1, 11], XTAL_OUT [D2, 16])

The FM2010 provides multiple external clocks which can be commonly found in PCs, PDAs, and cellular phone platforms. To use crystal, either a 12.288 MHz or 13 MHz crystal can be plugged between XTAL_IN and XTAL_OUT to generate the clock for the internal PLL. For the external clock input, 12.288MHz, 13MHz, 24MHz, or 48MHz can be applied. To set up various input frequency, please refer to parameter PLL_div (0x1E58) and PLL_xtal_clk (0x1E60) in "FM2010 Parameters Tuning Guide". The signal will go in XTAL_IN/CLK_IN pin, and the XTAL_OUT pin will be no connection.

****The required component of the crystal circuit recommended as follwing :**

Recommended Requirements	Recommended Value
Table coperation frequency	12.288 MHz or 13 MHz
Resonant mode	Parallel
Frequency tolerance	± 30 ppm
Aging per year	± 5 ppm/year
Operation mode	Fundamental mode
Crystal C_O	< 10 pF
Crystal Rs (ESR)	<150 Ω
C_L (external load capacitance)	20 pF
Drive level	500 μW

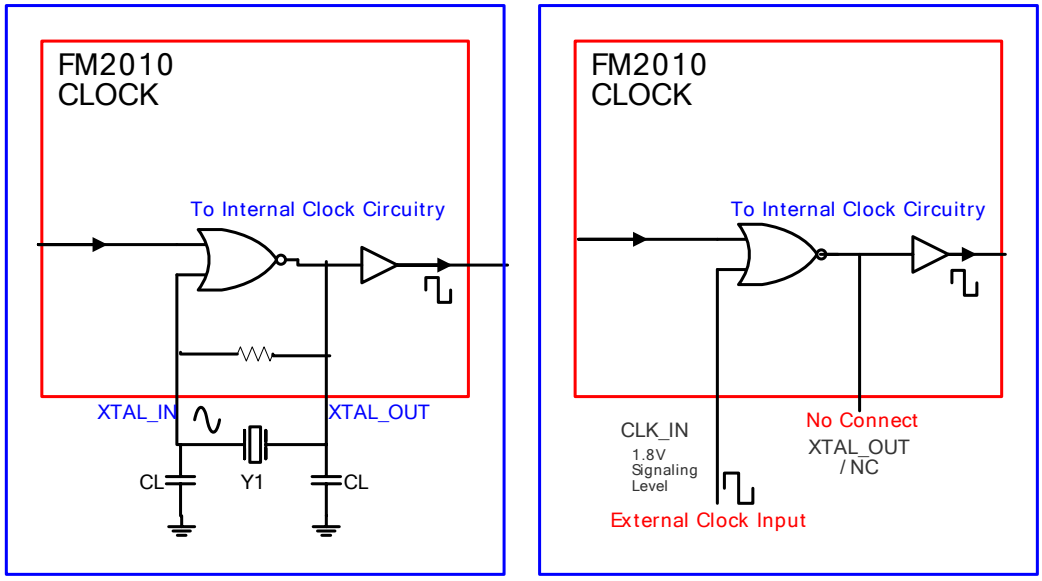


Figure 10: Crystal with Internal Clock Generator and External Clock Source reference circuit

2.7. Reset and Warm Reset

(Pin RESET_ [A3, 21])

To trigger the internal power-up reset circuit, the voltage of VDD digital power must be lower than 0.4V before ramping high to restart a reset process.
Note : there should be a minimum waiting time, t_{RST} (in table 9), between power-off and power-on. For the system with long power down discharge time, it is recommended to have a discharge circuit for power on restart process.

The RESET_ pin should have a 100kΩ pull-up resistor when this fucntion is not used.

2.8. Power Down Mode

(Pin PWD_ [A4, 31])

The FM2010 supports a power-down mode. In this mode, the device can save most of power consumption without missing the parameter settings after resume. The hardware pin control can be switched on-the-fly.

The power down sequence is initiated by applying a falling edge on this hardware PWD_ pin. The minimum power-down active low period, t_{PDA}, would be around 6.6 ms. The power-down mode can be exited and resume to the operation by applying a rising edge on this PWD_ pin.

If the power-down resume mode is not selected, the parameters for the FM2010 must be reloaded after recovering from power-off. For more details, please refer to "*FM2010 Parameter and Programming Guide*"..

2.9. Analog Communication mode
(Pin IRQ_ANA [C1, 16])

The FM2010 supports an analog communication mode by asserting IRQ_ANA pin high (This edge trigger function is programmable. 0x1E39 is set to 1 by default, which presets it to low-to-high edge trigger. Details please refer to parameter tuning guide). In this Analog Communication mode, the input signal of microphone will route to LINE_OUT directly through pre-amplifier. It bypasses the internal ADC, DSP, and DAC. The gain control and internal pre-amplifiers are still working with the input and output signal.

It requires an edge trigger to initiate the Analog Communication mode. And a opposite edge signal will resume to the normal operation mode with restored parameter settings.

In this mode, the gain settings of the programmable PGA are saved and another set of new gain settings will be reloaded for this ananlog communication mode. After exiting this Analog Communication mode, and resuming to the normal operation mode, the saved gain settings can be restored.

The mode can be switched on-the-fly by the hardware IRQ_ANA pin. The Analog Communication mode consumes less power than either 1 or 2 microphone mode since it halts the ADC/DAC and DSP operations.

2.10. Normal operation mode with 1 or 2 microphones, and with or without beam-forming function.

The normal opreation mode is working when IRQ_ANA pin is at logic low state and triggered by a falling edge. The normal operation mode would be selected by parameters setting :

Two microphones with beamforming – Uni+Omni mode.
Two microphones without beam forming – Omni+Omni mode.
One microphones mode.

In the two microphone mode, two microphones are connected properly with an external microphone bias circuit. The LINE_IN should be connected to the line-out or speaker-out of the system audio codec. And the FM2010 outputs the clear voice signal through LINE_OUT signal. In each mode, different parameter set is sent by the external host through SHI interface or a pre-loaded EEPROM.

3. Electrical and Timing Specification Functional Description

In this section, we describe all detail specification of DC, AC, timing, and performance of voice processor.

3.1. Electronics Power, DC, and AC Characteristics

Table 4: Electric Power Characteristics

Parameters	Specification			Unit	Test Conditions/ Comments
	Min	Typ	Max		
Total Power Dissipation	-	27		mW	V_{DD}=1.8V, V_{DD_CODEC}=1.8V, T_{amb}=25°C
	-	24.3		mW	V_{DD}=1.62V, V_{DD_CODEC}=1.62V, T_{amb}=25°C
ESD		2kV			HBM condition

Table 5: DC Characteristics

Parameters and Symbols		Specification			Unit	Conditions/Remarks
		Min	Typ	Max		
Power Supply for the Digital CORE domain.	V_{DD}	1.62	1.8	2.0	V	
Power Supply for the Analog CODEC domain	V_{DD_CODEC}	1.62	1.8	2.0	V	
Active Power Supply Current	I_{SU}	-	9	-	mA	In ANA_COM mode
		-	12	-	mA	In 1 microphone mode
		-	15	17	mA	In 2 microphones mode
Power Down Current	I_{PD}	-	100	300	µA	
Input Leakage Current	I_{IH}	-	-	10	µA	V_{DD}=V_{DD_CODEC}=1.8V
	I_{IL}	-	-	10	µA	V_{DD}=V_{DD_CODEC}=0
Input Voltage High	V_{IH}	0.7*VDD	1.8	3.6	V	With 3.3V tolerance in all pins except XTAL_IN/ CLK_IN pin.
Input Voltage Low	V_{IL}	0	-	0.4	V	
Output Voltage High	V_{OH}	0.9*VDD	-	VDD	V	
Output Voltage Low	V_{OL}	0	-	0.4	V	
Input Capacitance	C_{IN}	-	10	-	pF	
VDD_CODEC Power Ripple (AC element)	-	-	-	100	mV	Ripple should be limited for AC performance.
VREF Voltage Reference	V_{REF}		1.2		V	VDD_CODEC=1.8V, 25°C

Table 6: AC Characteristics (Room Temperature and PGA gain is 0 dB).

Parameters and Symbols		Specification			Unit	Conditions/Remarks
		Min	Typ	Max		
MIC0, MIC1 input range (Differential)	-	-	2.4	-	V_{PP}	Reference as 0dB full scale (1.2 V_{PP} for each pin)
LINE_IN input range (Differential)	-	-	2.4	-	V_{PP}	Reference as 0dB full scale (1.2 V_{PP} for each pin)
MIC0, MIC1 PGA gain resolution			4		Bit	*Refer to *"Programming tuning guide"*.
MIC0, MIC1 PGA gain Step Size			2*		dB	*Refer to *"Programming tuning guide"*.
LINE_OUT output range (Single-ended)	-	-	1.2	1.5	V_{PP}	0dB PGA gain (Typ) +2dB PGA gain (Max)
LINE_OUT PGA gain resolution			5		Bit	
LINE_OUT PGA gain Step Size			1*		dB	*Refer to *"Programming tuning guide"*
SNR for MIC0, MIC1 to LINE_OUT analog path	-	-	75	-	dB	
Codec sampling rate		-	8	-	kHz	
MIC0, MIC1, and LINE_IN (all analog-input) impedance	Z_{AI}	-	25	-	kΩ	At 0dB PGA gain
LINE_OUT (analog-output) load impedance	Z_{AO}	600	-	-	Ω	Any load less than 600 ohm would be a voltage drop

3.2. Timing Characteristics

Table 7: Timing Characteristics

Parameters and Symbols		Specification			Unit	Conditions/Remarks
		Min	Typ	Max		
Reset Holding Time (low)	t_{RST}	60	-	-	µs	
Power-Down Active Time	t_{PDA}	6.6	-	-	ms	
Power-Down to Power-Up Duration	t_{PDU}	1	-	-	s	
Power Off to Power On Time		500	-	-	ms	*
Parameters Restore Time after Reset or power down	t_{PARA}	4	-	-	ms	
LINE_OUT Output Signal Delay Time After Setting Parameters	t_{OUT}	-	108	-	ms	*
Digital Input Raising Time	t_{IR}	-	5	-	ns	C_L=20pF (typ and max) No load (min)
Digital Input Falling Time	t_{IF}	-	5	-	ns	
Digital Output Raising Time	t_{OR}	-	5	-	ns	R_L=1.25kΩ, C_L=20pF (typ and max). No load (min).
Digital Output Falling Time	t_{OF}	-	5	-	ns	
Crystal Clock Frequency (master clock)	f_{MCK}	-	12.28813	-	MHz	XTAL_IN/CLK_IN pin
Crystal Clock Duty Cycle (master clock)	D_{MCK}	40	50	60	%	XTAL_IN/CLK_IN pin
SHI Clock Frequency (SCK)	F_{SCK}		100	400	kHz	Input mode supports up to fast-mode (400kb/s)
SHI Clock Duty Cycle	D_{SCK}	40	50	60	%	
SHI SDA Input Setup Time	t_{DS}	10	-	-	ns	
SHI SDA Input Hold Time	t_{DH}	10	-	-	ns	

* Power-off to power-down waiting time depends on the power supply discharge time in the system. Larger power supply decoupling capacitors in the system may take longer time to discharge. The discharging component may help shortening the time.

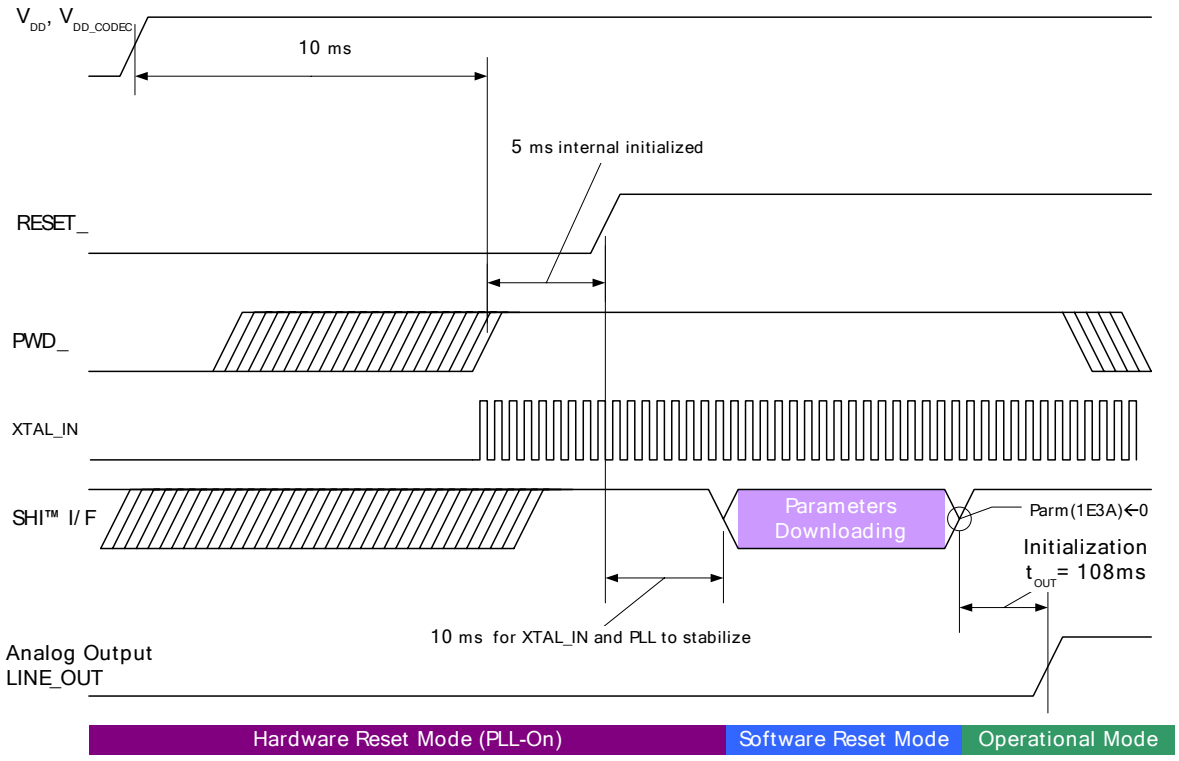


Figure 11: Cold Reset Timing Chart

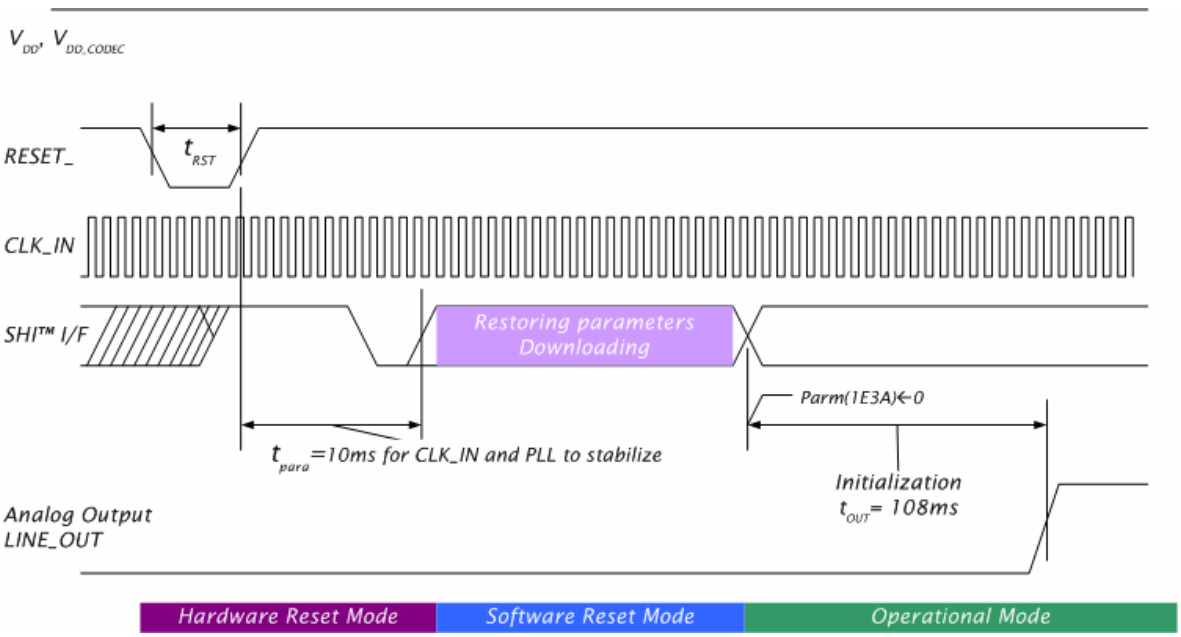


Figure 12: External Hardware Power Reset Timing Chart

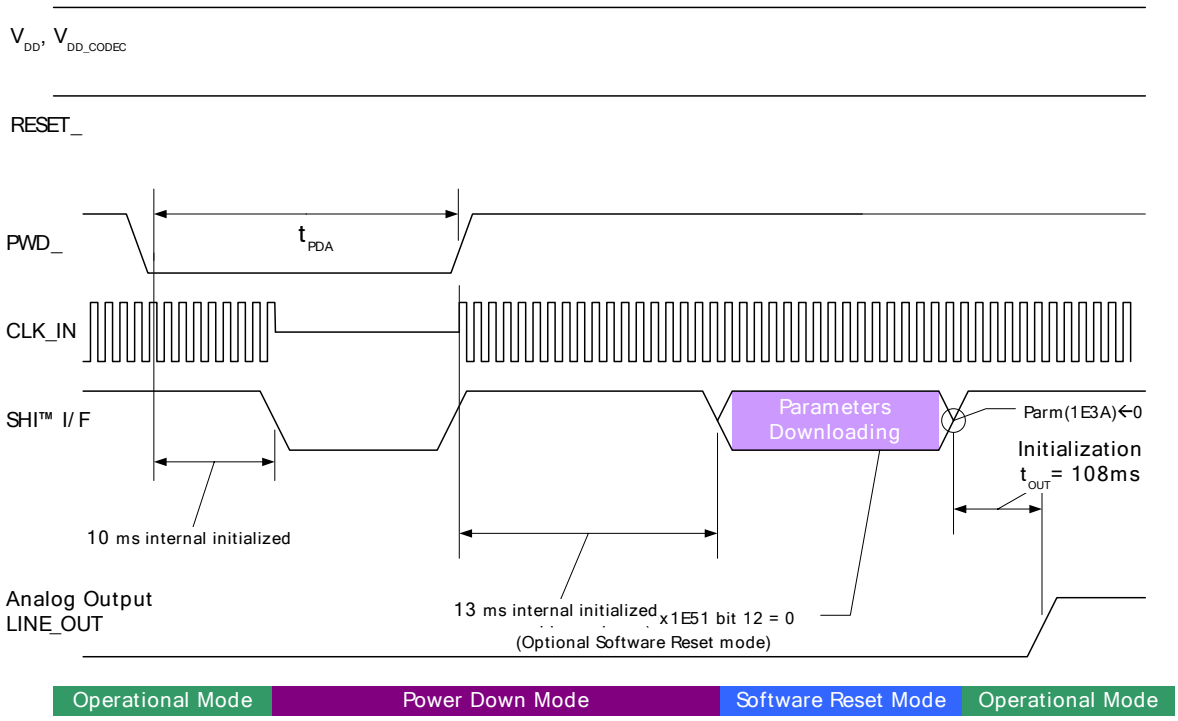


Figure 13: External Power-Down Timing Chart

3.3. Voice Processor DSP Performance details

Table 8: DSP performance details

Parameters and Symbols	Specification			Unit	Conditions/Remarks
	Min	Typ	Max		
Acoustic Echo Cancellation	-	-	60	dB	2 microphone mode (U+O) with beam-forming.
Stationary Noise Suppression	-	12	-	dB	For MIC0/MIC1 standalone
Non-Stationary Noise Suppression	-	20	-	dB	For MIC0+MIC1 (U+O) with beam-forming
Beam-forming Cone Angel	120	150	-	degree	With SAM (Small Array Microphone) technology
Echo Convergence	-	30	-	ms	2-microphone mode
Stationary Noise Convergence	-	1.5	-	sec	2-microphone mode
Acoustic Echo Tail Length (max)	-	-	100	ms	
Mic_in to Line_out Processing Delay	-	54	-	ms	

3.4. Operational State Transition Diagram

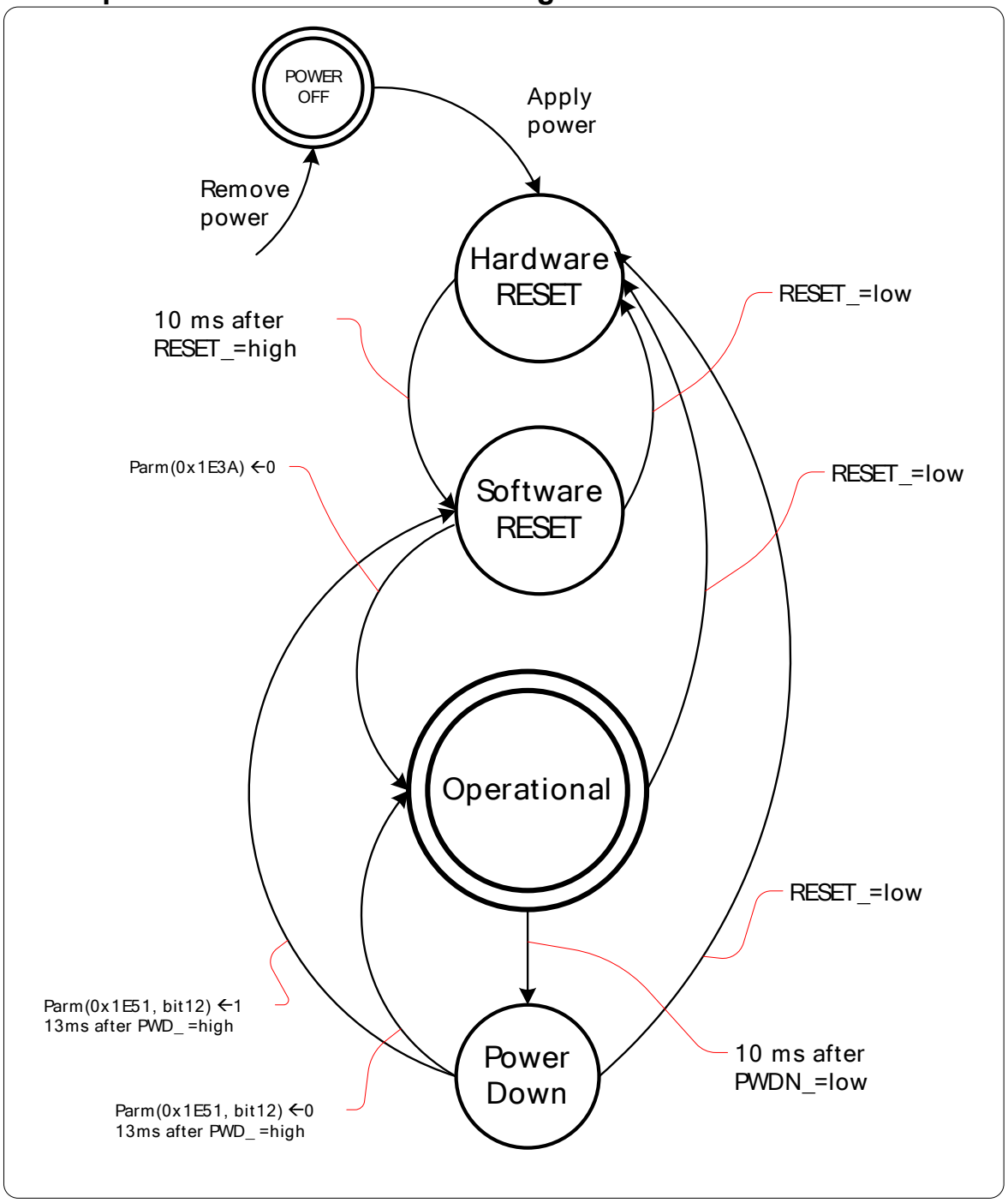


Figure 14: Operation State Transition Diagram

4. Pin Definition

Table 9: Pin Definition

Pin No.	Name	Type	Description
19	VDD	PWR VDD	Digital VDD. With minimum of 1.62V.
17	GND	PWR VSS	Digital VSS, ground.
9	VDD_CODEC	PWR VDD	Analog VDD. 1.8V
47	VSS_CODEC	PWR VSS	Analog VSS
11	XTAL_IN/ CLK_IN	IN	Crystal input : 13 MHz 12.288 MHz External clock input to XTAL_IN/CLK_IN. This pin has a built-in Schmitt trigger in order to eliminate a crystal. The input frequency is configured by SHI commands. (For the command information, refer to parameter PLL_div (0x1E58) and PLL_xtal_clk(0x1E60) in "FM2010 Parameters Tuning Guide") The options are 12.288MHz, 13 MHz, 24MHz, and .48MHz. 1.8V voltage source only. Not 3.3V tolerance.
14	XTAL_OUT	OUT	Crystal output; Leave it N.C. when external clock is used.
40	MIC0_P	IN	Microphone 0 input (+).
39	MIC0_N	IN	Microphone 0 input (-).
38	MIC1_P	IN	Microphone 1 input (+).
35	MIC1_N	IN	Microphone 1 input (-).
3	LINE_IN_P	IN	Line-in input (+) used as echo reference.
5	LINE_IN_N	IN	Line-in input (-) used as echo reference.
6	LINE_OUT	OUT	Line-out output with/without voice processing.
2	VREF	OUT	Band-gap reference output pin. Tie a 0.22μF to GND.
8	VCOM	OUT	Analog common mode reference voltage output pin. Tie a 0.22μF to GND.
27	SCK	IN /OUT	Two command modes supported: "SHI (Serial Host I/F) command mode" and "EEPROM download mode". It is selected by SHI_S (SHI mode selection pin). In the SHI mode, this pin is a slave clock input with 3.3V tolerant. And it can speed up to 400kb/s with a proper pull-up resistor. In the EEPROM mode, this pin is a clock output with 1.8V peak to the EEPROM. A 256-byte or other size of EEPROMs with the same address and data format can be used. (e.g.: a 24AA02 series).
23	SDA	IN/OUT	In the SHI mode, this pin is a serial data input/output with 3.3V tolerance. In the EERPOM mode, this pin is a serial data input/output but as the master of this signal. The pin output is an open drain pin, and tie to an external pull-up resistor 10 kΩ.
20	SHI_S	IN	SHI (Serial Host I/F) Mode Selection. This pin is 3.3V tolerant. The logic state "1" selects a SHI command mode. To download the initial parameters from host and change internal registers inside. The logic state "0" is to select an EEPROM download mode. It can be pulled up/down to VDD/GND. For the command information, please refer to *"FM2010 Parameter and Programming Guide"*.

16	IRQ_ANA	IN	Analog Communication Mode Interrupt Request (Analog Communication mode) .Edge Triggered. This pin is 3.3V tolerant. When set at the logic state ”1”, MIC0 input signal will only go through PGA (Programmable Gain Operational Amplifier) then output to LINE-OUT port. It skips the ADC, DAC, and DSP. MIC1 is not connected in this mode. The PGA gain will reset to a programmable dB number when the mode switched. This signal is a hardware control with on-the-fly function switching between normal mode and the Analog Communication mode. The logic state “0” is the normal mode. It can be pulled up/down to GND/VDD directly.
21	RESET_	IN	Reset input. Active low. This pin is 3.3V tolerant. This chip has an internal power-up reset with a de-bounce circuit. It is recommended to pull up with 10kΩ.
31	PWD_	IN /OUT	Power-down mode selection. Active low. This pin is 3.3V tolerant. Input: Power Down Mode selection. State “1” – Normal mode. State “0” – Power-Down mode. It is recommended to pull up with a 10kΩ resistor. An optional LED output pin programmed by SHI command. It can flash as the external LED indicating VAD information.
34	TEST	IN	Test pin. Active high. It is recommended to pull down with a 100kΩ resistor.

- LEGEND:
  - IN – input pin
  - OUT – Output pin
  - IN/OUT – Input/Output bidirectional pin
  - O.D – Open Drain pin
  - PWR – Power pins as VDDs and VSSs of each digital and analog power domain.

5. Package

5.1. Package Dimension – 22-pin CSP package

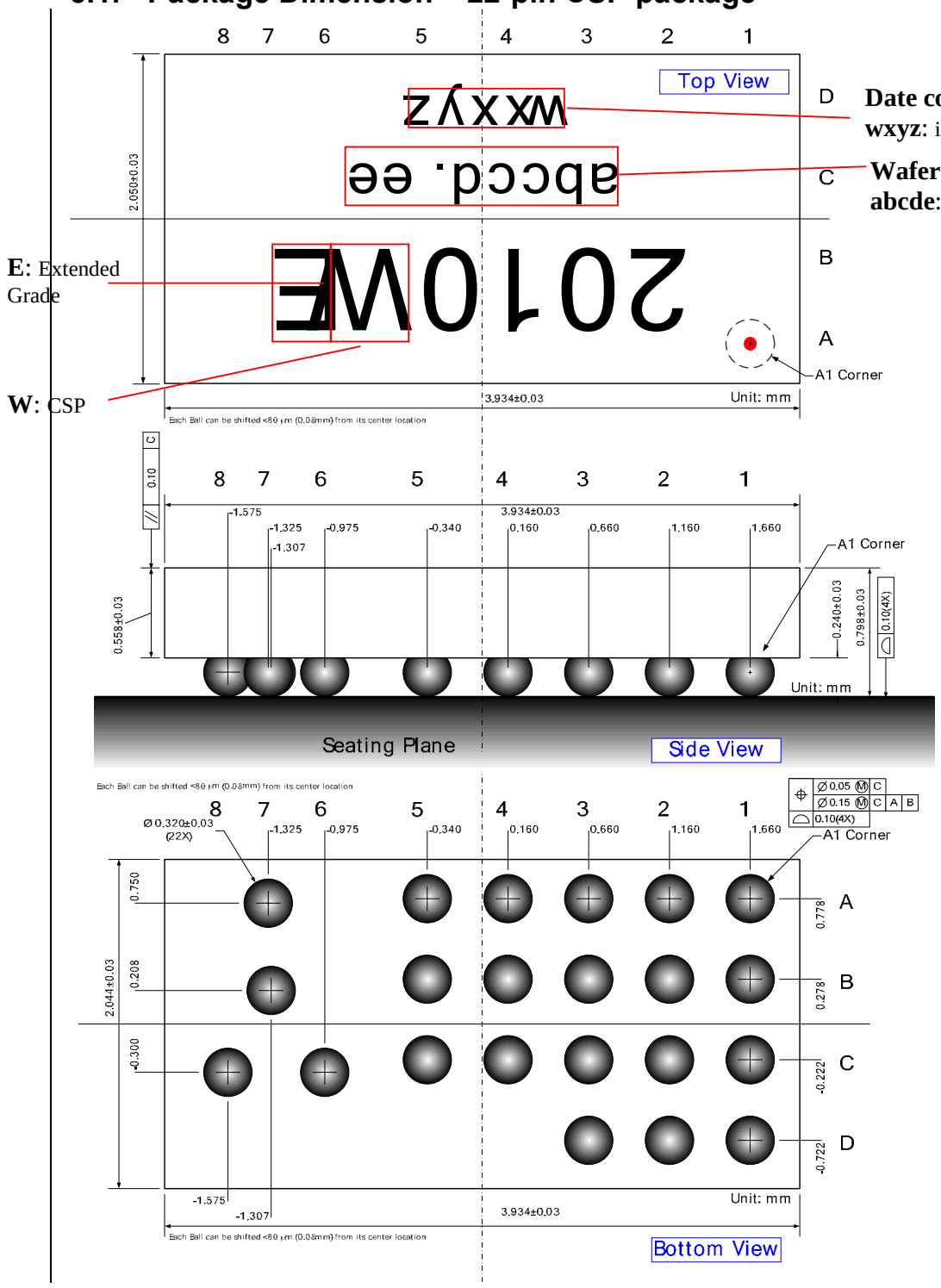
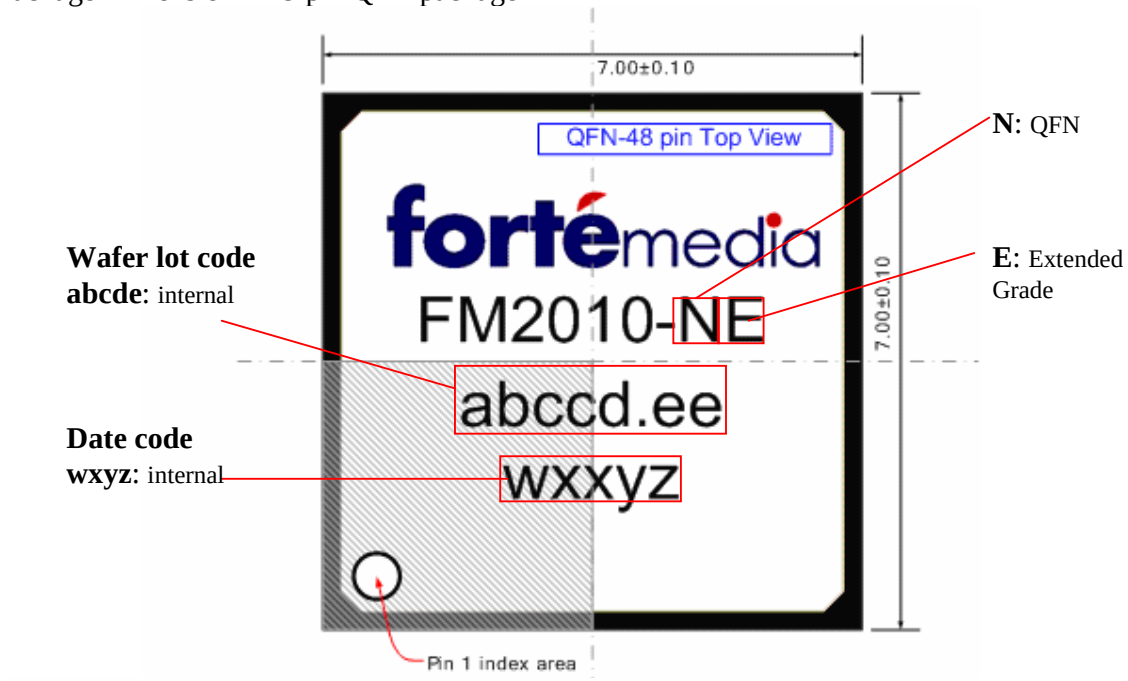
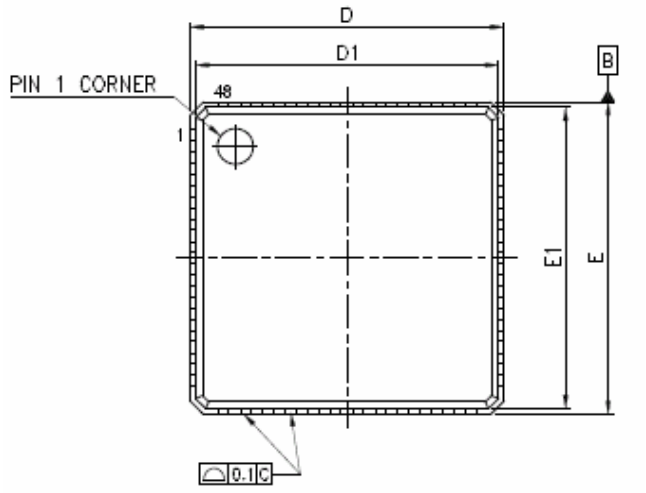
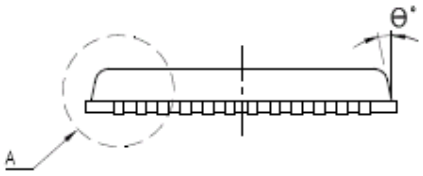


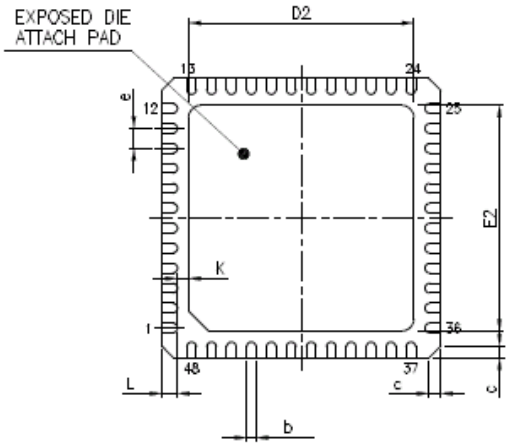
Figure 15: CSP Package Dimensions

Package Dimension – 48-pin QFN package









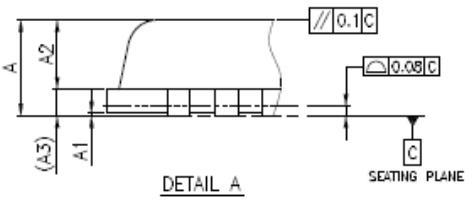


Figure 16: QFN Package Dimensions

SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2	0.65 PEF.		
A3	0.203 REF.		
b	0.18	0.25	0.30
c	0.24	0.42	0.60
D	6.90	7.00	7.10
D1	6.65	6.75	6.85
E	6.90	7.00	7.10
E1	6.65	6.75	6.85
e	0.50 BSC.		
K	0.20	-	-
L	0.30	0.40	0.50
θ°	0.00	-	12.00

Unit: mm

D2			E2		
MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
4.6	-	5.25	4.6	-	5.25

Unit: mm

Table 10. Package Dimension

6. Ordering and Storing Information

Table 11: Available Package Type and Temperature Range

Order name	**FM2010-NE**	**FM2010-WE**
Package Type	Standard 48-pin QFN Package	Proprietary 22-pin CSP Package
Package Size and Dimensions	7.0±0.15mm(L)× 7.0±0.15mm(W)× 0.9±0.15mm(H)	3.934±0.03mm(L)× 2.044±0.03mm(W)× 0.798±0.03mm(H)
Pitch	0.5 mm pitch	0.5mm (minimum pitch distance)
Non-lead	Green	Green
Temperature Range Grade	Extend Grade	Extend Grade
ESD Protection	HBM 2kV	HBM 2kV

Table 12: Operational Temperature Range and Storage Temperature Range.

Operational Temperature Ranges(T_{amb})	
Extend Grade	-20 °C to 70 °C
Storage temperature Range (T_{stg})	
green	-40°C to 150°C

7. Audio Measurement System

7.1. AEC Measurement Condition

PC Microphone: -45 dB sensitivity
Speaker: 8 Watts
Acoustic Echo Cancellation in Voice Band, typical performance = 50~60 dB.

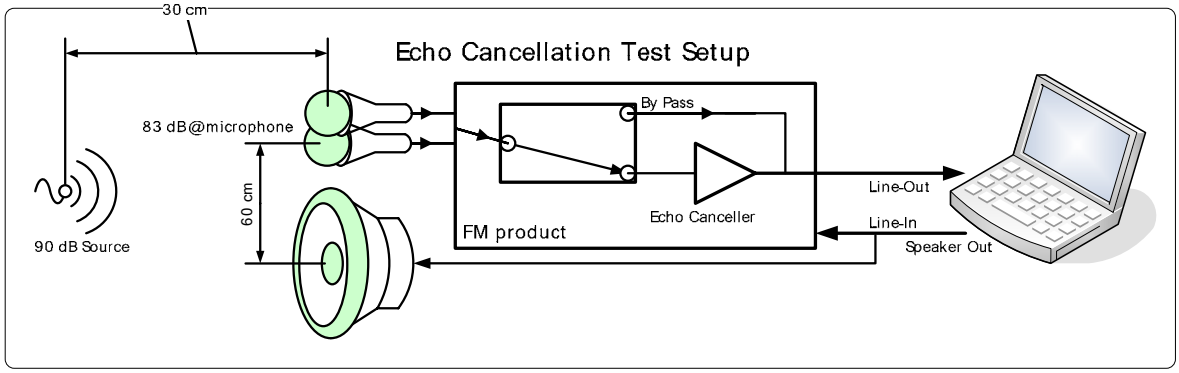


Figure 17: Echo Cancellation Test Setup

7.2. Stationary Noise Suppression Condition

Play an 1 kHz tone or a white noise.
Adaptive time is between 1 to 2 seconds and typical performance = 12dB.

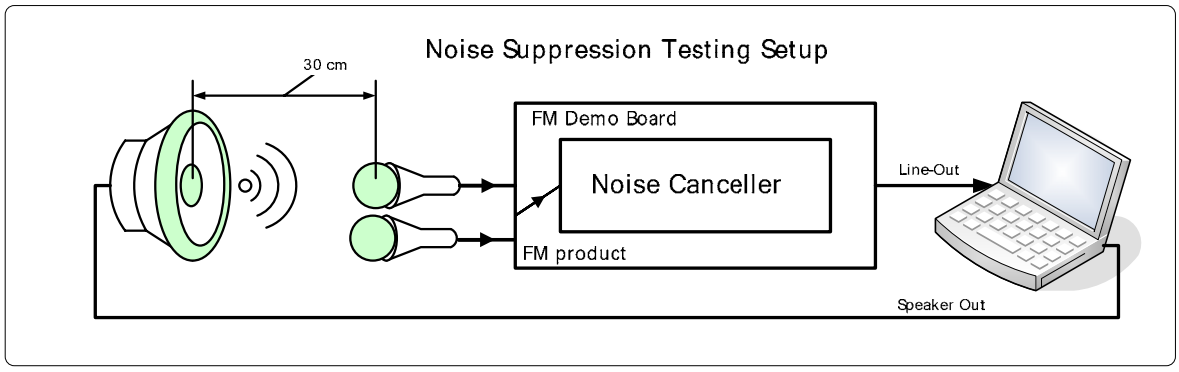


Figure 18: Noise Suppression Test Setup

8. References Audio Measurement System

8.1. Terminology

Table 13: Terminology

Term	Definition
ADC	Analog to Digital Converter
AEC	Acoustic Echo Cancellation
CSP	Chip Scale Package, it is identical to WLCSP
DAC	Digital to Analog Converter
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistor
FM	Fortemedia Inc.
GPIO	General Purpose Input/Output
I²C	Inter-Integrated Circuit
MIC	Microphone
MIPS	Million instructions per second
NC	No Connected
Omni	Omni-directional microphone
PDA	Personal Digital Assistant
PGA	Programmable Gain Operational Amplifier
PLL	Phase-locked Loop
PND	Portable Navigation Device
QFN	Quad Flat package - No leads
ROM	Read Only Memory
SAM	Small Array Microphone
SHI	Serial Host Interface
SNR	Signal-to-Noise Ratio
SPKR	Loudspeaker
SRAM	Static Random Access Memory
Uni	Unidirectional Microphone
XTAL	Crystal

8.2. Related Documents

Table 14: Related Reference Documents

- FM2010_Parameter_Tuning_Guide
- FM2010_Product_Brief
- FM2010_SHI_Implement_Guide