EE214A Project Report

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Parameter	**Given Specification**	**Achieved Specification**
Common-mode output voltage	$-0.5\text{V} < V_{CM,out} < +0.5\text{V}$	-0.251V
Power dissipation	$\leq 2\text{mW}$	0.888mW
Small-signal transresistance gain $(A = v_{out}/i_{in})$	$\geq 40k\Omega$	$40.504k\Omega$
-3dB Bandwidth	$\geq 50\text{MHz}$	70.055MHz
Figure of merit (FOM) = (gain $\times$ BW) / (power)	$\geq 1000\text{k}\Omega\cdot\text{MHz/mW}$	$3195\text{k}\Omega\cdot\text{MHz/mW}$

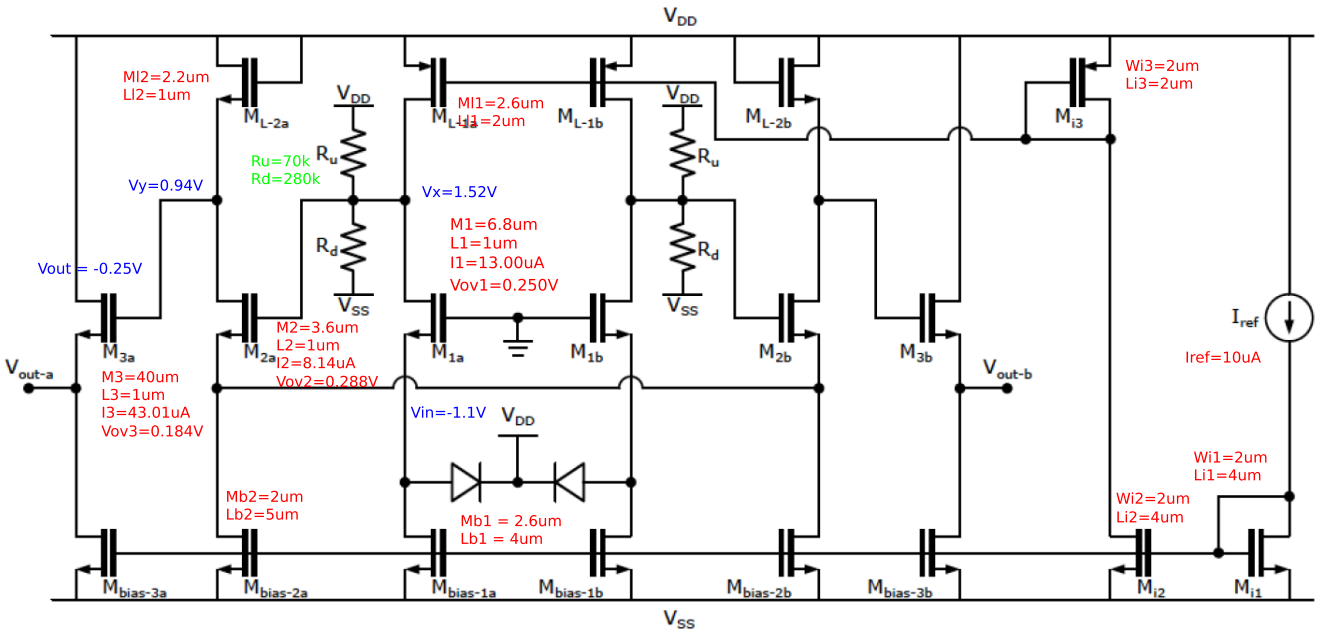


Fig. 1. Annotated Schematic with DC operation point

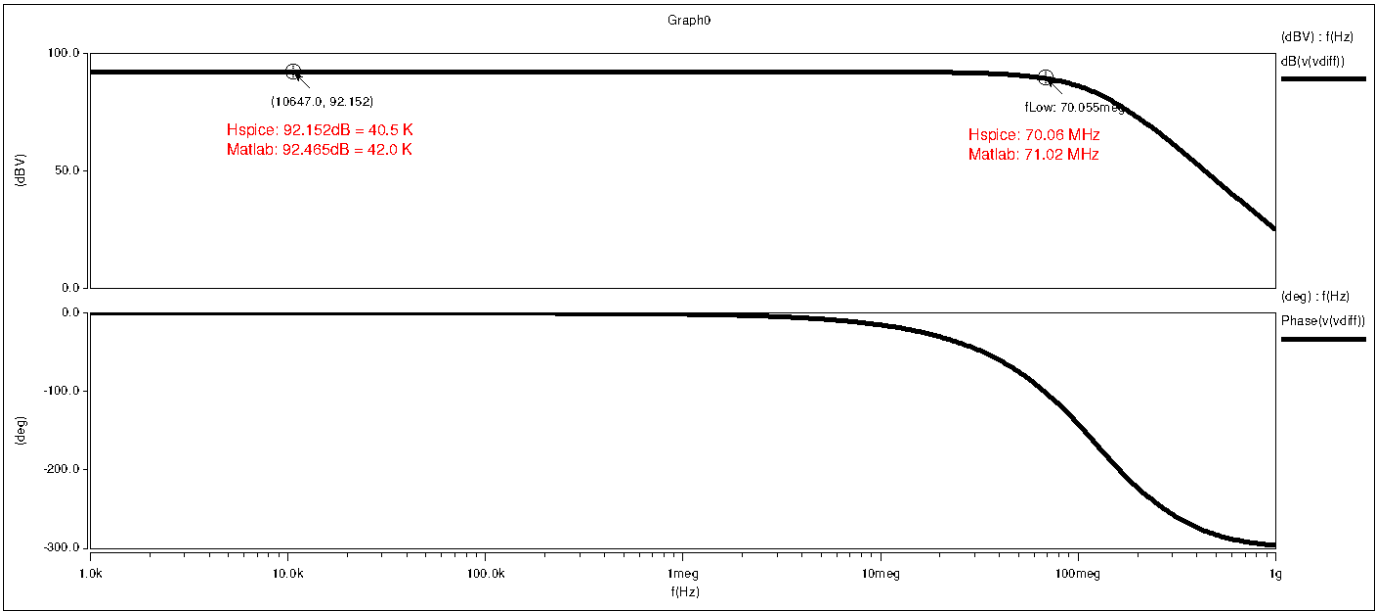


Fig. 2. Frequency Response ($f_{3dB} = 70.06MHz, Gain = 92.152dB$)

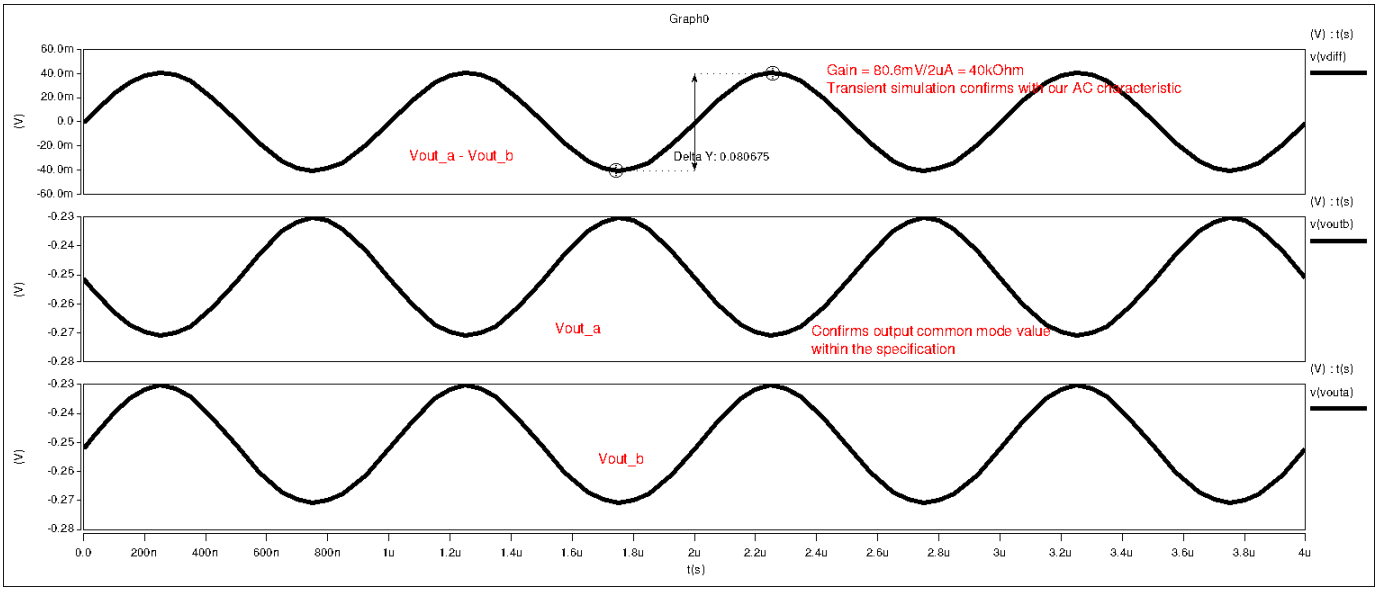


Fig. 3. Transient Analysis for $1MHz, 0.5uA$

I. Introduction

This project designs an optical sensor circuit, in which the small-signal current originated from a photo-diode is amplified by a 3-stage differential amplifier, aiming to achieve relatively high bandwidth and high trans-resistance gain with moderate power consumption.

The main branch of the circuit, i.e. the multi-stage amplifier, is symmetric both in the sense of configuration and parameters (see Fig. 1), enabling a half-circuit analysis for the reduction of design effort. The crucial and also the trickiest task of this part of the design is the specification of the operating points of the three stages of transistors. However, since the four KPIs (see Section II for a detailed analysis) – 3dB-bandwidth, power consumption, trans-resistance gain, and figure of merit – are inter-correlated and almost impossible to accurately analytically inferred from each other, a global optimized biasing point is not available from simple convex optimization techniques, and thus the task inevitably involves the recursive sweeping of different design parameters while sagaciously fixing parameters temporarily not in interest. After the determination of the operating points of the main branch, the current mirror, with its associated parameters, are determined correspondingly. The detailed design process as well as the sweeping results are discussed further in section III.

II. High Level Outline

We begin with deriving general expressions for gain and bandwidths. In addition, we will explore the effect of parameter changing on gain, bandwidth, and power. Those trade-offs are keys to understand our final optimization model.

A. Low Frequency Gain Approximation

We have a cascaded **CG-CS-CD** TIA in this project. We begin our analysis with building a rough model to approximate the range of certain parameters of our circuit.

- For the **common gate** stage, we know that its current gain is about unity, thus, its transimpedance gain depends on the value of R_u, R_d, as well as ro from the drain of M_1 and M_{L1}.
- For the **common source** stage, its voltage gain depends on the **active load** made by diode connection M_{L2}, providing a gain with $\frac{gm_2}{gm_{l2}}$, which usually range from 1 to 5.
- For the **common drain** stage, we know that its voltage gain is typically less than 1.

Consequently, the above analysis will give us a brief idea about a typical order of R_u and R_d, which is on the order of $10k\Omega$. In addition, we also know that the maximum power constrain is $2mW$, the maximum current on each branch is roughly on the order of $10\mu A$. Assuming minimum channel length, the output impedance ro is around the order of $100k\Omega$.

From all the previous results, we will state our **four important assumptions** in our approximation of gain in this circuit:

1) $ro \gg R_u, R_d, \frac{1}{gm}$ This is justified since we just proved that R_u and R_d is on the order of $10k\Omega$ while ro is on the order of $100k\Omega$.
2) $g_{mb} \approx 0.2gm$ The detail of this is proved in earlier discussion section
3) $R_u = R_d$, this assumption is made for easier analysis by fixing the DC operation point at that node to zero. We may revise it later for final optimization.
4) $I_{L1} = I_{B1}$, thus current in R_u, R_d branch will not flow in/out to the branch of transistor M_1. This is assumed for easier analysis and may subject to change.

With the assumptions listed above, we can derive the gain expression:

$$\begin{aligned} R_{tot} &= R_{CG}A_{v,CS}A_{v,CD} \\ &= \frac{R_u}{2}\frac{g_{m2}}{g'_{ml2}}\frac{g_{m3}}{g_{m3}+\frac{1}{R_{load,tot}}} \end{aligned}$$

Where,

$$R_{load,tot} = R_{load} \parallel \frac{1}{g_{mb3}}$$
$$gm' = gm + gmb$$

B. Bandwidth Approximation

In this class, we learned two ways to approximate the bandwidth, **ZVTC** and **Miller Approximation**. We will make a brief discussion on the trade-offs of each method and state our final choice of which approximation to take.

*1) **ZVTC**:*

- **PRO**: It provides fast estimation. Besides, the result it provides is always conservative.
- **CON**: ZVTC is no longer reliable if we have multiple poles close to each other, in the case of 4 poles adjacent to each other (the case of this project), it could underestimate over 44.5%.

*2) **Miller Approximation**:*

- **PRO**: Also provide fast estimation.
- **CON**: In the circuit with dominant pole, only dominant pole approximation is valid. Other non-dominant poles provided by Miller Approximation should be discarded. **With an exception where all poles are adjacent with each other, in that case, all poles are valid.** In this case, the this drawback might be an advantage of miller approximation.

We begin with **ZVTC** in this project, but we realize that ZVTC **GREATLY** underestimate our bandwidth. This would imply that the operation point we chose has multiple poles close to each other. As a result, we switch to **Miller Estimation** becasue in the case of multiple poles close to each other, every poles it approximated is valid.

Assuming that we use **Miller Approximation** to estimate the bandwidth, we calculate the effective resistance and capacitance and derive the poles associated with each node:

- At **input node**: the contribution of effective capacitance is C_{in}, $C_{sb,1}$, and $C_{gs,1}$. The contribution of effective resistance is g_m, g_{mb} for transistor M1.

$$p_1 = -\frac{g_{m1}+g_{mb1}}{C_{in}+C_{gs,1}+C_{sb,1}}$$

- At **node X**: the contribution of effective capacitance is C_{gd1}, $C_{db,1}$, $C_{gd,load1}$, $C_{db,load1}$, $C_{gs,2}$, and Millered capacitance $C_{gd,2}$. The effective resistance is dominated by R_u and R_d given our assumption in II-A.

$$p_2 = -\frac{1}{(R_u \parallel R_d)C_x}$$

where

$$C_x = C_{gd,1} + C_{db,1} + C_{gd,load1} + C_{db,load1} + C_{gs,2} + (1 + Gain_2)C_{gd,2}$$

- At **node Y**: the contribution of effective capacitance includes $C_{gs,load2}$, $C_{sb,load2}$, $C_{db,2}$, Millered capacitance $C_{gd,2}$, as well as Millered capacitance $C_{gs,3}$. The effective resistance in this node is mainly affected by $g_{m,load2}, g_{mb,load2}$.

$$p_3 = -\frac{g_{m,load2} + g_{mb,load2}}{C_y}$$

where

$$C_y = C_{gs,load2} + C_{sb,load2} + C_{db,2} + (1 + \frac{1}{Gain_2})C_{gd,2} + (1 - Gain_3)C_{gs,3}$$

- At **output node**: The main contribution of capacitance is $2C_L$ (doubled in differential half circuit). The effective resistance depends on both gm_3 and $\frac{R_L}{2}$ (halved in differential half circuit).

$$p_4 = -\frac{g_{m3} + g_{mb3} + \frac{2}{R_{load}}}{(1 - \frac{1}{Gain_3})C_{gs,3} + 2C_L + C_{sb,3}}$$

Now, we get approximations of poles on each node of interest, those analysis will help us to construct a transfer function with poles and solve for 3dB bandwidth in MATLAB.

C. Power Consumption

Power consumption is related with the current on each branch. As in our sweeping, the current on each stage is a dependent variable on Gain and V_{ov}, and thus g_m, we need an explicit expression of Power as followed:

$$\begin{aligned} P &= (V_{DD} - V_{SS}) \sum_i I_i \\ &= (V_{DD} - V_{SS})(2I_1 + 2I_2 + 2I_3 + 2I_u + I_{ref} + I_i) \\ &= (V_{DD} - V_{SS}) \times (I_{ref} + I_i + (V_{ov1}g_{m1} + V_{ov2}g_{m2} + V_{ov3}g_{m3} + \frac{2(V_{DD} - V_{SS})}{R_u + R_d}) \end{aligned}$$

This expression, together with the above ones on poles, serve as the starting points of the following trade-off analysis.

III. Qualitative Analysis on each stage over Gain, Bandwidth, and Power

Now, we can analyze each stage and discuss possible trade-offs when a certain parameter changes. Understanding those trade-offs will direct us on how to sweep variables in Section IV.

A. Common Gate stage

To begin with, we can find out that the DC gain of common gate stage is independent of sizes of M1 but dependent on its load resistance R_u, R_d given that we only have capacitor at input node. We would like to share some trade-offs associated with this stage:

- **Frequency-Frequency Trade-off**: For a fixed bias current I_{b1}, gm is proportional to $\sqrt{W}$ (suppose we use minimum L). Suppose we want to increase pole frequency at **node x**, a smaller W is preferred. However, as smaller W would imply a smaller gm. We know that the pole frequency at **input node** is proportional to $\frac{1}{gm}$, decrease the pole frequency at **input node**. Consequently, for a fixed bias current I_{b1}, there is a trade-off between improving pole frequency at **input node** and **node x**. Consequently, we did a sweep to find the best operation point associated with this trade-off at Section IV-C.
- **Frequency-Power Trade-off**: Suppose that we want to improve the power consumption at this stage, we would like to cut the current on that branch. For a fixed overdrive voltage, reduce current will reduce gm, from last part, we know that reduce gm in this stage will also reduce the pole frequency at the input node. Thus, there is a trade-off between frequency optimization and power optimization. This trade-off is also covered in Section IV-C.
- **Other Trade-offs**: There are two remaining trade-offs but they are rather obvious. A increase in the load resistance will boost the gain at a cost of lower the pole frequency at that node. In addition, a higher resistance at load will reduce the current on that branch, lower power consumption. The best operation point of this trade-off is covered in our general gain optimization step, which refers to Section IV-B.

B. Common Source Stage

To begin with, we could derive an expression of gain of this stage in terms of W_2, $W_{load,2}$, suppose we use minimum L and $gmb = 0.2gm$.

$$\begin{aligned} Gain_2 &= \frac{gm_2}{gm'_{load,2}} \\ &= \frac{5}{6}\frac{\sqrt{2I_D\mu_n C_{ox}(W/L)_{load,2}}}{\sqrt{2I_D\mu_n C_{ox}(W/L)_2}} \\ &= \frac{5}{6}\sqrt{\frac{W_2}{W_{load,2}}} \end{aligned}$$

This expression tells us that gain of second stage is **relatively independent** of its biasing current. Thus, we could size W_2 with a low overdrive voltage to minimize its power consumption without sacrificing the gain or bandwidth.

The trade-off at this stage is also obvious, suppose we fix the size of W_{load2} as small as possible, an increase in gain will result in an increase in W_2, which would introduce more parasitic capacitance at $nodex$ and $nodey$. We have a **Frequency-Gain** trade-off. This trade-off will be covered in our optimization over gains in Section IV-B.

C. Common Drain Stage

For a typical common drain stage, the analytic expression of its gain is:

$$Gain_3 = \frac{g_{m3}}{g_{m3} + \frac{1}{R_{load}}}$$

This expression display a direct relationship between $Gain_3$, V_{ov3}, and I_{d3}. If we take a fixed value of $Gain_3$, we could observe a linear relation between V_{ov3} and I_{d3}, and also a inverse proportion between V_{ov3} and W_3. The result, again, is a **Frequency-Power** trade-off: a higher overdrive voltage reduces the required width of the transistor which effectively drive down the 3dB bandwidth, at the cost of a linearly increased biasing current consuming more energy. Thus, if we plot the curve of FOM vs. V_{ov3}, we will expect initially an upward slope due to an enlarged bandwidth followed then by a falling from higher power consumption. This trade-off will also be covered in our optimization over gains in Section IV-B

IV. Optimization

A. Degree of Freedom Reduction

It is noted that the complexity of this project is a result of two aspects. On one hand, even excluding the current reference and the current mirror, the main part entails the sizing of 8 transistors and 2 resistors (only half of the total amount need to design due to symmetry), each with different functionalities. On the other hand, the function that we aim to optimized involves three quantities – bandwidth, power, gain – and each impose an additional constraint on the system. Presented before us is a sophisticated non-convex conditional optimization problem. We propose two approaches tackling the two difficulties presented above.

Firstly, the 8 transistors could be classified into three stages: M_1, M_2, M_3, are the most important transistors that determine the overall gain and bandwidth of the circuit; M_{bias-1}, M_{bias-2}, M_{bias-3} determine the current I_{d1}, I_{d2}, I_{d3} passing through the three stages, which means that their sizing are not independent variables and can be specified once the currents are known; M_{L-1} and M_{L-2} are also not independent and can be moved off the desk when we do sweeping – M_{L-1} is given by I_{d1} as we want the voltage divider to work perfectly, while M_{L-2} provides active load for the second stage and is completely determined by the gm_2 together with $Gain_2$. Thus, the degree of freedom left are: W_1, W_2, W_3, V_{ov1}, V_{ov2}, V_{ov3}, $Gain_1$, $Gain_2$, $Gain_3$.

B. Optimization on the Gain Distribution

In this part, we focus on finding the optimal combination of $Gain_1$, $Gain_2$, and $Gain_3$, in terms of the figure of merit given that we have fixed the total gain $Gain_{tot} = 40k\Omega$.

We would like to STATE our assumptions in this stage, we fixed the biasing for M_1 with an arbitrary V_{ov1} and W_1, L_1. We fixed the V_{ov2} for M_2. We fixed the V_{ov3} for M_3. In addition, we will explore the optimal value of those parameters in Section IV-C and Section IV-D.

As has been calculated in Section II-A, $Gain_1$, i.e. the trans-resistance gain of the CG amplifier make the main contribution and should have the same order of magnitude with the total required gain of $40K\Omega$. Although improving $Gain_1$ is the most direct and efficient way of improving the overall gain, the resulted larger value of R_u and R_d drive down the bandwidth and will bring detrimental effect on our figure of merit (FOM). Based on that, the sweeping range of $Gain_1$ is from $10K\Omega$ to $90K\Omega$. $Gain_2$ is slightly over 1, it is relatively independent of its biasing current but subjected to the frequency-gain trade-off we discussed in section II-C. $Gain_3$ is slightly lower than one, and we sweep it from 0.4 to 0.8 which is the common range of a common-drain amplifier. For a fixed value of $Gain_1$, we have knowledge of R_u and R_d. For a fixed value of $Gain_3$, we have knowledge of W_3, and thus I_3 (since we have an initial assumption on Vov_3). Finally, for a fixed value of $Gain_2$, we have knowledge of W_2, and thus I_2 (since we also have an initial assumption on Vov_2). **Together with our initial assumption, sweeping over gains is sufficient enough to give us all parameters to calculate our circuit performance, for a fixed $Gain_1$, $Gain_2$, $Gain_3$ combination, we could find its bandwidth through Section II-B, power through Section II-C, and thus FOM**.

Given that it is hard to visualize the optimization strategy of gain in this stage. We provide a pseudo-code for this stage as shown in Algorithm IV-B.

Algorithm 1 Algorithm for Optimization over gains

```
Fix V_ov1,V_ov2,V_ov3 and W_1, L_1
for Gain_1 = 10k : 90k do
    Get R_u, R_d from fixed Gain_1;
    for Gain_3 = 0.4 : 0.8 do
        Get Gain_2
        Get W3 from fixed Gain_3
        Get W2 from fixed Gain_2
        Approximate BW for a fixed Gain_1, Gain_2, Gain_3
        Approximate FOM for a fixed Gain_1, Gain_2, Gain_3
    end for
end for
```

Figure 4 and Figure 5 shows the distribution of figure of merit (FOM) and bandwidth in terms of $Gain_1$ and $Gain_3$ (note that $Gain_2$ is calculated by dividing $Gain_{tot}$ with $Gain_1$ and $Gain_3$). As we look for a bandwidth of over $70MHz$ (for the purpose of the bonus points), our chosen point is the point of tangency of the $70MHz$ curve in Figure 5 and the contours in Figure 4.

C. Optimization on the Operating Point of M_1

Remember that in Section IV-B we choose an arbitrary value of V_{ov1} and W_1, L_1, in this section, we will optimize those parameters to yield optimal performance. In Section III-A, we realized that there are **Frequency-Frequency** trade-off and **Frequency-Power** trade-off depends on its sizes and current(or its overdrive voltage). Here, we sweep transistor $M1$ over its size and overdrive voltage to find an optimal point for M_1.

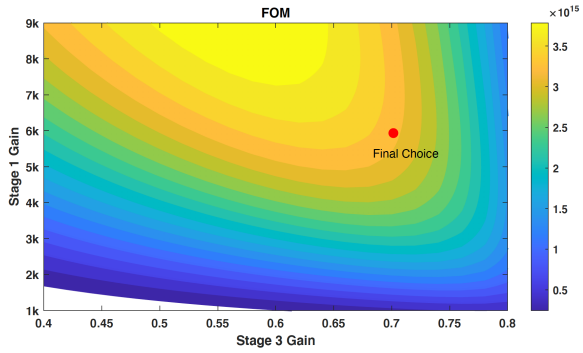


Fig. 4. FOM as of Gain Distribution

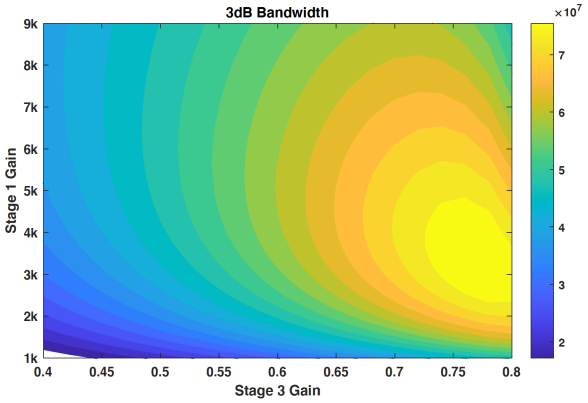


Fig. 5. Bandwidth as of Gain Distribution

In the sweeping process, we use the fixed operation point from result in Section IV-B. And we may implement a recursive optimization process between Section IV-B, Section IV-C, and Section IV-D. We will discuss it later.

Both Figure 6 and Figure 7 help us locate the best biasing point for $M1$.

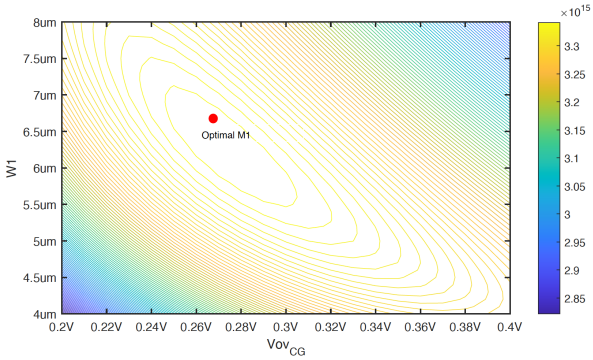


Fig. 6. FOM as of M1 Parameters (Colour Map)

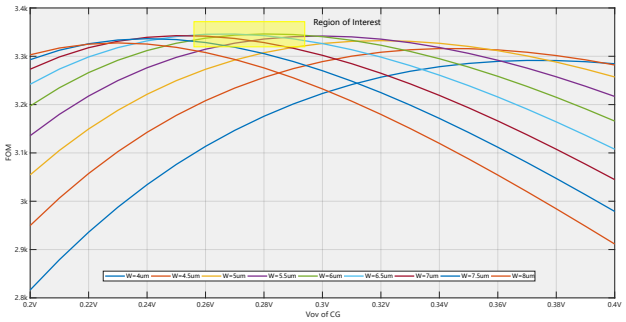


Fig. 7. FOM as of M1 Parameters (Envelope)

D. Optimization on the Operating Point of M_3

As has been discussed in Section II-C, there is no need to sweep V_{ov3} and W_3 concurrently as one is already determined by, or rather, rigorously inversely proportional to, the other when $Gain_3$ is fixed. Therefore, the optimization of M_3 becomes a single-function problem and we plot FOM and bandwidth vs. V_{ov3} in Figure 8.

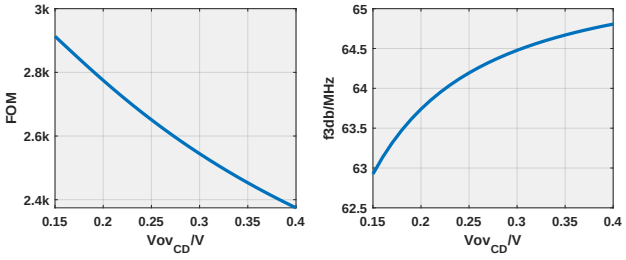


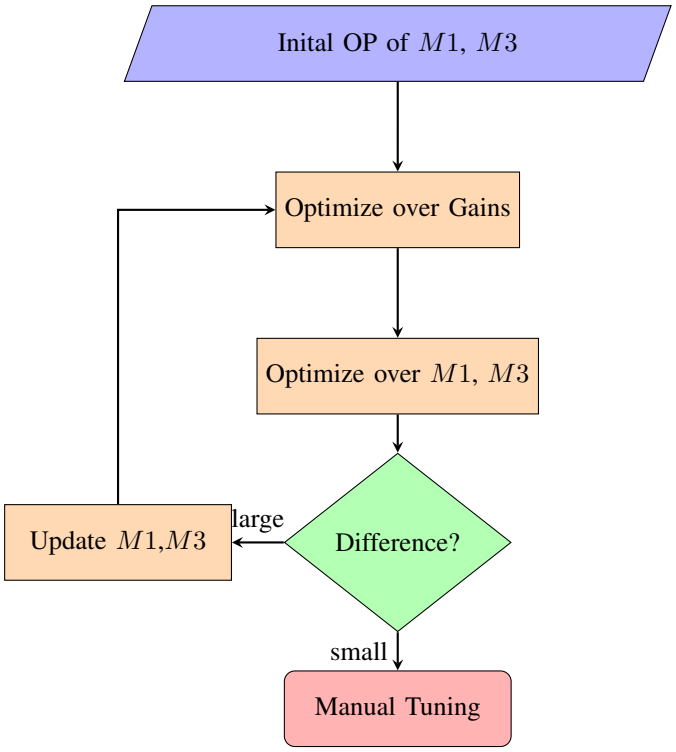
Fig. 8. Optimization Result of M3

From the result, we prefer a smallest Vov_3 possible to maximize our figure of merit. To do so, we sacrifice our bandwidth, which will be compensated by other stages.

Consequently, we choose $Vov_3 = 0.2V$ for this stage's result.

E. Recursive Optimization

You may realized that the optimization strategy in Section IV-B, IV-C, IV-D depends on the results of each other. Thus, there is no close form solution of our circuit.



What we do is that we perform a recursive optimization strategy. To begin with, we choose some initial values of operation point of $M1$, $M3$, and we find an optimal operation point in Gain optimization in Section IV-B. Then, we put this operation point in the optimization code for $M1$, $M3$ in Section IV-C and IV-D. If there is a large discrepancies between our initial assumption about $M1$ and $M3$, we shall use the updated operation point of $M1$ and $M3$ and redo the optimization in Section IV-B. Here we summarize our thought as a flow chart.

F. Biasing and Verification

What we have left the biasing our circuit properly.

To begin with, the W, L, I_d of transistor $M1, M2, M3$ are already determined by our optimization steps over best FOM. Thus, we only have to bias the current mirrors to supply we current we want, given that for a current mirror:

$$\frac{I_d}{I_{ref}} = \frac{W/L}{W_{ref}/L_{ref}}$$

We could achieve the current we want. **It is worth mentioning** that we can play with the current mirror ratio by setting a very low reference current (e.g. $10X$ smaller than that of on the branch) such that we could save power on the supply branch. We chose not to do so because it will require a large W/L ratio for the biasing transistors M_{b1}, M_{b2}, etc. on our main branch, such a large W, L will damage our bandwidth.

In addition, given that we have a specification on the output common mode value, which is determined by the overdrive voltage of M_3 and M_{L2}, we have take into account of this in our sweeping such that overdrive voltage we choose for both M_3 and M_{L2} will not pull or push the output common mode value out of the specification.

Finally, we assume equal R_u and R_d in simulation, but in this stage, we play with a different value of R_u and R_d such that $R_u \parallel R_d$ remain unchanged but $R_u + R_d$ get increased. Consequently, we could save more power on the branch of R_u and R_d.

Our last step is to put our MATLAB results into spice simulation and make some manual tuning. In our case, we slightly overestimate the frequencies. Thus, some changes are needed to pull the bandwidth to exactly 70 MHz.

V. Results and Analysis

A. Simulation-Calculation Comparison

The following table displays the comparison between the Matlab-calculated results and those from the HSPICE simulation.

Comparison	Gain ($k\Omega$)	f_{3dB} (MHz)	Power (mW)	FOM (10^{15})
Matlab	42.000	71.0245	986.58	3.024
HSPICE	40.513	70.0554	888.06	3.195
Error	3.67%	1.39%	11.04%	5.65%

Results match in general, with slight differences due to a number of approximations we made when doing Matlab calculations, including Miller Approximations, ignoring channel-length modulation, and several assumptions we made with intrinsic and extrinsic capacitance calculations.

VI. Conclusion

This report displays a complete systematic design flow of a differential multi-stage photo-diode amplifying circuit, achieving high bandwidth and trans-resistance gain with low power consumption. For a design of a complicated system, our approach was to first conduct a detailed analysis of each components of the circuit, while deriving analytic expressions of the several KPIs that are of interest, with the help of necessary approximation (in this case miller approximation). Then we extract a pool of parameters that are of significant importance and fix the trivial ones, followed by several rounds of Matlab-assisted sweeping to locate the optimal value of these parameters.

For multidimensional sweeping, it is usually a wise choice to divide the factors into categories and sweep them in order while assigning unused factors to some constants. Once a round of sweeping is finished, we then update those assigned constants with new optimized value and do a second round of optimization. This way of recursive sweeping, with enough rounds of recursion, guarantee that we arrive some locally optimal value. After the sweeping, we test our circuit with Hspice and do some slight manual manipulation to get some marginal improvements. At the stage of the checkpoint, we obtain a 3dB bandwidth of over $70MHz$, a gain of $40.5k\omega$, and a power dissipation of $0.888mW$. This demonstrates that our methodologies and design flow generate results that meet the standard. For the rest of the project, we still have plentiful room to explore further about getting better design techniques with higher level of automation; also, the noise factor has been purely excluded from our existing design, and we wish to incorporate that consideration into updated versions of our circuit.

In addition, what we also realized is the difference between a design solely for optimization and a more practical design in industry. In our project, we use Miller for best estimations. But what we also know that ZVTC is always conservative. Thus, for a practical design, we would like to choose ZVTC even though it sometimes underestimate the bandwidth by a lot given that some poles are close to each other. Besides, since most of the poles are close to each other in our design, we would like to adding some compensation techniques to separate our poles such that we will only have one dominant pole, in this way, our system is more stable.