EE114/214A Fall 2020
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DESIGN PROJECT

Checkpoint: Thursday, October 29, 2020, 11:59pm PT
Final Netlist and Report: Friday, November 20, 2020, 11:59pm PT

1. Overview and Specifications

Your task in this project is to design a fully differential optical sensor circuit whose system-level block diagram is shown in **Figure 1**. The photodiode at the input is modeled as a small-signal current source in-parallel with a capacitor. The sensor circuit drives a differential RC load, which represents the loading from subsequent stages. You are provided with one ideal reference current source; you should mirror this current to generate the bias currents in your circuit. For the purposes of this project, the photodiode is assumed to be noiseless. The circuit architecture is shown in **Figure 2**. For the main part of the project, do not change this architecture (please see the end of this document for bonus parts).

You may work on this project alone or in groups of two (we strongly encourage working in groups of two). Each team should submit one project report. You are encouraged to discuss the design problem with other teams, but your design implementation must be unique. As per the honor code, do not exchange computer files with other teams.

Your goal is to size all of the transistors and resistors and to decide the value of the reference current (I_{ref}) in order to meet the following objectives:

Parameter	Specification
Technology	1 μm CMOS
Operating temperature	25 °C
V_{DD}/V_{SS}	$+/-$ 2.5 V
Output load resistance (differential), R_L	20 kΩ
Output load capacitance (differential), C_L	250 fF
Input load capacitance, C_{in}	100 fF
Common-mode output voltage	$-0.5\text{ V} \leq V_{CM,out} \leq +0.5\text{ V}$
Power dissipation	$\leq$ 2 mW
Small-signal transresistance gain (A=v_{out}/i_{in})	$\geq$ 40 kΩ
Gain magnitude response (Bode plot)	Flat, then monotonically decreasing
-3dB bandwidth	$\geq$ 50 MHz
Figure of merit (FOM) = (gain × BW) / (power)	$\geq$1000 kΩ · MHz/mW
Current mirror channel length	$\geq 2\ \mu m$
Gate overdrive for all devices	$\geq$ 150 mV
Width/length size increments	$\Delta L_{min}, \Delta W_{min} = 0.2\ \mu m$
Maximum current mirror ratio	20

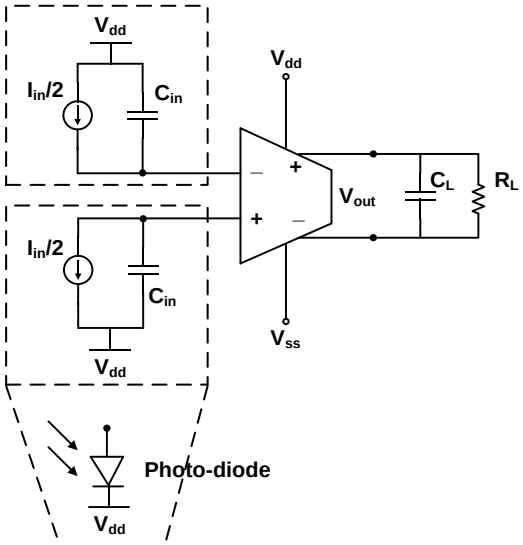

Figure 1: System-Level Block Diagram

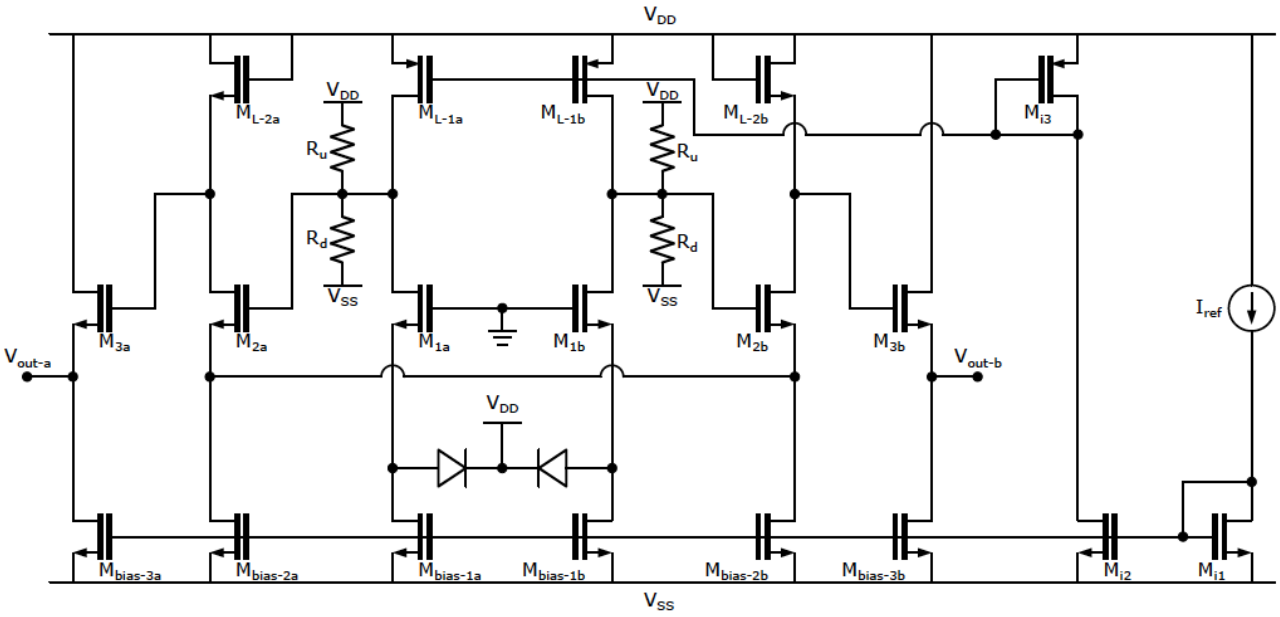

Figure 2: Circuit Architecture

2. Design Flow and Corresponding Deadlines

a) Read this handout thoroughly and ask the teaching staff if you have any questions.

b) Find a project partner (a Piazza survey will be posted).

c) Familiarize yourself with the schematic in **Figure 2** and identify how the key blocks interact. Then, draw simplified differential half-circuit models of the circuit that will allow you to identify the main design knobs.

d) Derive first-order expressions for circuit specifications as functions of parameters in your control, optimize for the specifications over these parameters, and verify your design choices via SPICE simulation; iterate as necessary to achieve the specifications (See the outlined procedure from lectures).
We recommend using the transistors' overdrive voltages and bias currents as some of the independent variables (see, e.g., the Bandwidth-Supply Current Tradeoff slides). Visualizing the design space is often helpful, so we recommend generating plots to guide your design.

To get you started with SPICE, we are providing a top-level testbench (DP_2020_top_level.sp) and a starter schematic (DP_2020_schematic.sp) on Canvas. The starter schematic defines the sensor architecture as a sub-circuit; the testbench loads this sub-circuit and runs the required simulations. You will be submitting your version of this starter schematic for both the checkpoint and the final netlist submission. For both of these submissions, we will evaluate whether your circuit meets the requirements using the provided top-level testbench, so please make sure that your SPICE file runs with that testbench before submission.

Mandatory check point (due Thursday, October 29, 2020, 11:59pm PT) for which you will submit:

1) A SPICE file with a preliminary version of your design (filename should be CP_<name1>_<name2>.sp (e.g., CP_Yueming_Zhuo_Amin_Arbabian.sp);
2) First-order symbolic estimates of the circuit's gain, bandwidth, and power consumption in terms of design parameters.
   The required intermediate specifications for this checkpoints are:
   i. All transistors should be in saturation.
   ii. Transresistance gain ≥ 1 kΩ.
   iii. Bandwidth ≥ 50 MHz.
   iv. Power consumption ≤ 5 mW.

Final netlist and report (due Friday, November 20, 2020, 11:59pm PT) for which you will submit:

1) your optimized netlist file. The file name should be:
   Final_<name1>_<name2>_power_gain_bandwidth_FOM.sp (e.g., Final_Yueming_Zhuo_Amin_Arbabian_2p0_40p0_50p0_1000.sp).
2) your final report. Format and requirements are explained in the following section.

3. Project Report

It is very important to show your design process to us. Therefore, **it is important to document your design process as you go.**

Page 1: Cover page. This should include the names of team members and a table comparing the given specifications with the achieved specifications.

Page 2: Annotated schematic diagram of your final design. **Clearly label** all device sizes, resistor values, current reference values, important node voltages.

Page 3: Attach a simulated Bode plot of the gain (both magnitude and phase) and a transient simulation plot for each output and also the differential output with a 1 MHz, 0.5 μA sinusoidal differential input current. **Clearly annotate** the achieved gain and bandwidth, as well as your calculated values for gain bandwidth (on the same plot).

$\leq$ 5 pages: Describe your design flow.

1) Begin with a high-level outline:
    - How did you approach this problem?
    - What were some of your key design choices?
    - Visualizations (e.g., flow charts or conceptual plots that explain how the tradeoffs are connected) are a good idea here (suggested).

2) Then, a more detailed description of the design process:
    - What design knobs and equations were used to optimize for the desired specifications?
    - It is a good idea to include quantitative plots showing how different design knobs affect performance (suggested).
    - Compare hand calculations with SPICE results in a table (show percentage differences) and discuss why there are discrepancies.

$\leq$ 1 page: Comments and conclusions. Here, you can convey issues you may have had, or things you learned (or did not learn) in this project.

4. Late Submission and Grading Policy

The deadline for each milestone is at 11:59pm. After 11:59pm, 10% of the total possible score for that milestone per hour will be deducted.

1. Checkpoint	10 points
2. Specifications (Final netlist)	20 points
3. Design flow, insights, optimization strategy (Report: content)	50 points
4. Documentation (Report: diagram annotation, formatting, etc.)	20 points
Total	100 points

5. Bonus parts (Maximum 30 points)

Bonus bandwidth: The achievable bandwidth is well above (e.g., 75 MHz) the minimal stated in this project. For each 10-MHz improvement in bandwidth, 5 bonus points will be awarded.

Bonus Problem 1 (10 points): Calculate your low-frequency input-referred differential spot noise considering only the transistors in the first stage (M_{L-1}, $M_{bias,1}$ and M_1) and the resistor branch ($R_{u,d-a}$ and $R_{u,d-b}$). Run an HSPICE noise simulation of your complete circuit at 1 kHz. How do the calculated and simulated values compare, and what is the percent error? Comment on why considering only the first branch is a reasonable first-order approximation.

Bonus Problem 2 (20 points): For this bonus problem, we have defined a new FOM that takes into account noise:

$$\mathbf{FOM_{bonus} = (Gain \times Bandwidth) / (Input\text{-}Referred\ Differential\ Spot\ Noise @ 1\ kHz)}$$

Calculate the FOM_{bonus} of the circuit you designed in the main part of the project. Your goal is to improve your FOM_{bonus}, using a new architecture if you so desire.

a) Analyze your circuit to find which parts limit the FOM_{bonus}. What are the major tradeoffs?
b) Suggest and implement modifications to the architecture that can help you improve FOM_{bonus} by 50%. Your circuit should still meet all the other specifications listed in the two tables above. Slide 3 in lecture 19 provides a good starting point for choosing topologies (especially point 2: literature review).
c) Simulate your new circuit to demonstrate the improvement in FOM_{bonus}.
d) Document your insights, modifications, and performance in a report.

There are no checkpoints for the bonus problem. The deadlines for the bonus netlist and report are the same as for the core project. The grading for the bonus will not be based solely on the FOM_{bonus} you achieve; it will also be based on the insights you present about the limitations of your original circuit and your explanation of proposed architectural modifications. Please refrain from blindly tweaking your circuit in HSPICE – even if you achieve a very good FOM_{bonus} by doing so, you will not get any points unless you can explain how and why you arrived at those results.