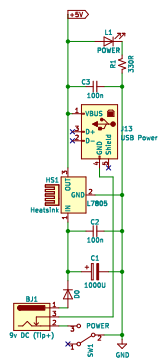
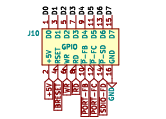


TEC-1G

Power Delivery

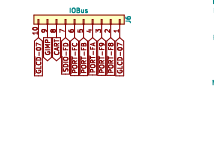


General Input/Output



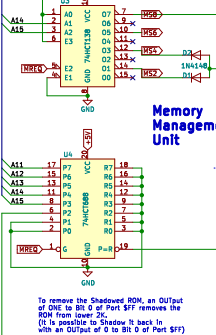
The TEC Deck

The new way to expand your TEC-1G with appropriate jump-jumper headers, expansion boards can be slotted on top of each other. Just the original TEC-1G and now you have access to ALL the 280 pins as well as port and memory select lines. Memory Expansion of 512K with ease. Input/Output options for ease.

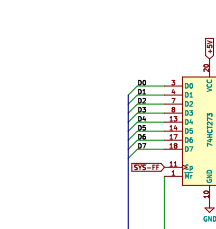


With the Shadow ROM switch ON (on Reset or OUT FF.501), the lower 2K of the 16K ROM is mapped to the lowest 2K of the memory map. This is to provide backward compatibility to older TEC-1 machines and their ROMs.

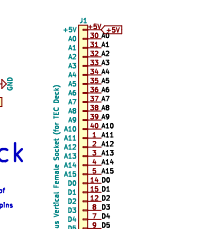
The ROM is selected (asserted LOW) if:
Any address in the lower 2K is requested (with Shadow ON)
If an address is within the top 16K of 64K. Otherwise, the RAM is selected if the address falls within the lower half (32K) of the memory map.



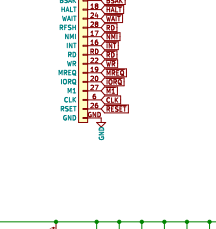
To remove the Shadowed ROM, an Output of ONE to Bit 0 of Port FFF removes the ROM from lower 2K. (It is possible to Shadow it back in with an Output of 0 to Bit 0 of Port FFF)



On Reset, all RAM is writable. Under software control, sending Bit 1 High of Port FFF turns ON write protect of the RAM in the second 16K memory space. Sending to Port FFF a value with Bit 2 clear will remove write protection.



This critical latch controls a lot of important functions, and will also be the center of huge memory expansions to come.



Static status showing the which output options are active.



These three jumpers allow for High ROM/RAM to be used in the Expansion socket.



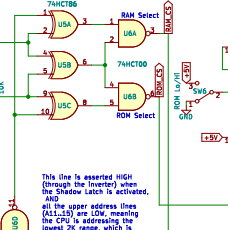
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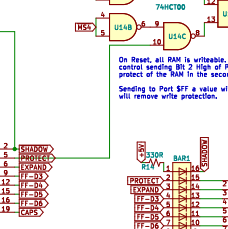
This line is asserted HIGH (through the Inverter) when the Shadow Latch is activated. AND all the upper address lines (A11-A15) are LOW, meaning the CPU is addressing the lower 2K range, which where the original TEC-1 ROMs were placed.



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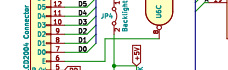
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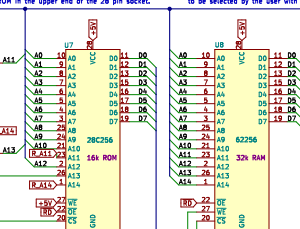
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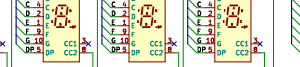
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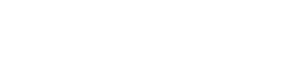
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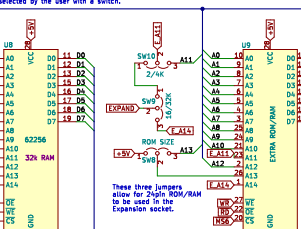


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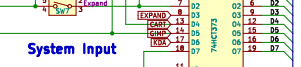
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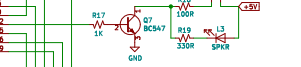
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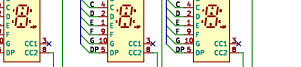
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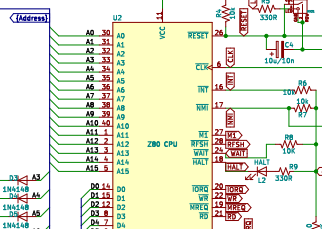


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CPU & Clock

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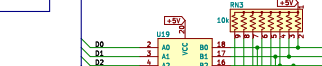
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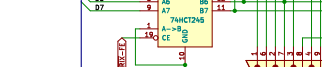
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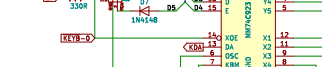
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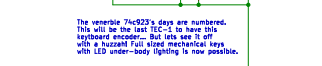
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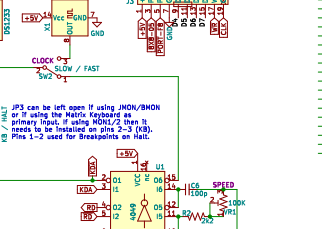


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Expansion Connectors

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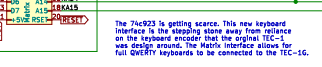
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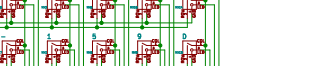
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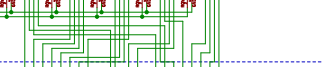
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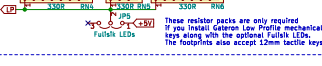
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