TEC-1G

Power Delivery

With the Shadow ROM switch ON (on Reset or OUT FF,$01), the lower 2K of the 16K ROM is mapped to the lowest 2K of the memory map. This is to provide backward compatibility to older TEC-1 machines and their Monitors.

Memory Management Unit

To remove the Shadowed ROM, an OUTput of ONE to Bit 0 of Port $FF removes the ROM from lower 2K.
(It is possible to Shadow it back in with an OUTput of 0 to Bit 0 of Port $FF)

The ROM is selected (asserted LOW)
IF
  Any address in the lower 2K is requested (with Shadow ON)
OR
  If an address is within the top 16K of 64k.
OTHERWISE
  The RAM is selected IF the address falls within the lower half (32k) of the memory map.

This line is asserted HIGH (through the inverter) when the Shadow Latch is activated, AND all the upper address lines (A11..A15) are LOW, meaning the CPU is addressing the lowest 2K range, which is where the original TEC-1 ROMs were placed.

64k Memory

The lower 32K is all RAM in a single chip.
The upper 16K of the memory map is reserved for the system ROM, although it is made up of up to a 64K EPROM to allow selection of multiple monitors, using a pair of switches.

This ROM socket can be configured to hold 2K/4K ROMs like the original TEC-1, by moving all 3 jumpers to positions 1–2, and then physically placing the 24 pin ROM in the upper end of the 28 pin socket.

These three jumpers allow for 24pin ROM/RAM to be used in the Expansion socket.

If using a 27C256 UV EPROM, jumpers required on Pins 2–3, and Pins 6–7.
For all other RAM/ROM chips, jumpers required on Pins 1–2, and Pins 4–5.

CPU & Clock

JP1 can be left open if using JMON/BMON/MON3 or if using the Matrix Keyboard as primary Input.
If using MON1/2 then it needs to be installed on pins 2–3 (KB).
Pins 1–2 used for Breakpoints on Halt.

Memory Protection

On Reset, all RAM is writeable. Under software control sending Bit 2 High of Port $FF turns ON write protect of the RAM in the second 16K memory space.

Sending to Port $FF a value with Bit 2 clear will remove write protection.

I/O Decoders

General Input/Output

System Latch

This critical latch controls a lot of important functions, and will also be the centre of huge memory expansions to come.

Status Lights showing you which output options are active.

System Input

CONFIG:
1. Keyboards 74c923 / Matrix
2. Protect OFF / ON
3. Expansion: LO / HI

Matrix Keyboard & Joystick

The 74c923 is getting scarce. This new keyboard interface is the stepping stone away from reliance on the keyboard encoder that the original TEC-1 was design around. The Matrix interface allows for full QWERTY keyboards to be connected to the TEC-1G.

HexPad Encoder

The venerable 74c923's are numbered. This will be the last TEC-1 to have this keyboard encoder... But lets see it off with a huzzah! Full sized mechanical keys with LED under-body lighting is now possible.

These resistor packs are only required if you install Gateron Low Profile mechanical keys along with the optional Fullsik LEDs. The footprints also accept 12mm tactile keys.

The TEC Deck

The new way to expand your TEC-1!
With appropriate long-legged headers, expansion boards can be stacked on top of each other, just like the original TEC-1 but now you have access to ALL the Z80 pins as well as port and memory select lines.
No more ugly fly leads or cables.
Memory Expansion of 512k with ease.
Input/Output options for days!

7 Segment Display Unit

Disco LEDs

LCD
20 Characters
x 4 Lines

Expansion Connectors

Modelled on the TEC-1 rev.D with DAT add-on
Originally designed by John Hardy, Ken Stone & Jim Robertson
published in Talking Electronics Magazine, 1983 – 1985
Thanks for assistance from: Craig Hart, Brian Chiha, Ian McLean, James Elphick

Sheets: /
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