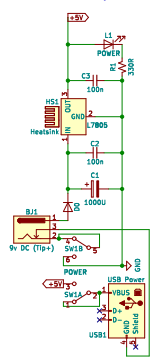


TEC-1G

Power Delivery



General Input/Output

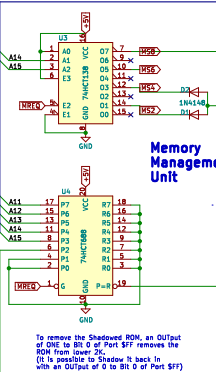


The TEC Deck

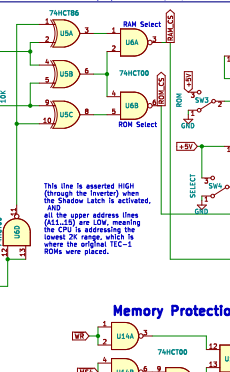
The new way to expand your TEC-1G with appropriate snap-on headers, expansion boards can be slotted on top of each other. Just the original TEC-1G and now you have access to ALL the 280 pins as well as port and memory select lines. Memory expansion of 512K with ease. Input/output options for ease.



With the Shadow ROM switch ON (on Reset or OUT FF.501), the lower 2K of the 16K ROM is mapped to the lowest 2K of the memory map. This is to provide backward compatibility to older TEC-1 machines and their numbers.



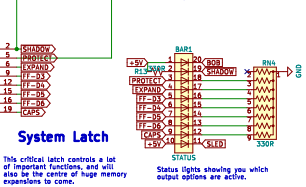
The ROM is selected (asserted LOW) if:
Any address in the lower 2K is requested (with Shadow ON).
If an address is within the top 16K of 64K. Otherwise, the ROM is selected (asserted LOW) if:
The RAM is selected if the address falls within the lower half (32K) of the memory map.



Memory Protection

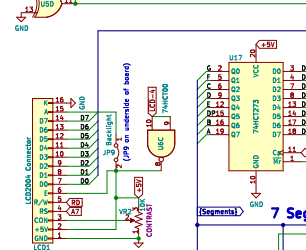
To remove the Shadowed ROM, an output of ONE to Bit 0 of Port FFF removes the ROM from lower 2K. (It is possible to Shadow it back in with an output of 0 to Bit 0 of Port FFF)

On Reset, all RAM is writable. Under software control, sending Bit 1 high of Port FFF turns ON write protect of the RAM in the second 16K memory space. Sending to Port FFF a value with Bit 2 clear will remove write protection.

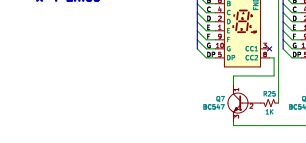


This critical latch controls a lot of important functions, and will also be the centre of huge memory expansions to come.

Status lights showing which output options are active.



LCD 20 Characters x 4 Lines



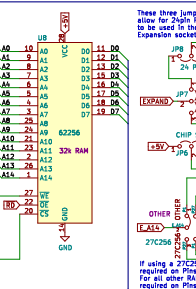
7 Segment Display Unit



Disco LEDs

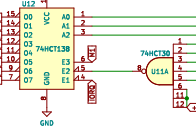
64K Memory

The lower 32K of all RAM is a single chip. The upper 16K of the memory map is reserved for the system ROM, although it is made up of up to a 64K EPROM to allow selection of multiple members, using a pair of switches.

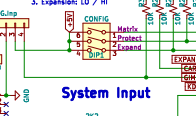


These three jumpers allow for 248K ROM/RAM to be used in the Expansion socket.

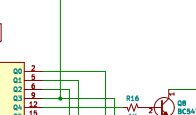
Other jumper: 27C256 EPROM jumpers required on pins 2-3, and pins 6-7. For all other ROM chips, jumpers required on pins 1-2, and pins 4-5.



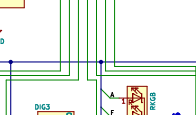
I/O Decoders



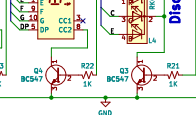
System Input



Speaker



HexPad Encoder

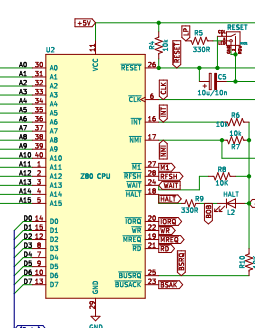


Matrix Keyboard & Joystick



CPU & Clock

CPU & Clock



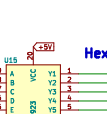
CPU & Clock



Expansion Connectors



Matrix Keyboard & Joystick



HexPad Encoder



7 Segment Display Unit



Disco LEDs



LCD 20 Characters x 4 Lines

Modelled on the TEC-1 rev.D with DAT add-on
Originally designed by John Hardy, Ken Stone & Jim Robertson
published in Talking Electronics Magazine, 1983 - 1985
Thanks for assistance from: Craig Hart, Brian Chien, Ian McLean, James Elphick
© Mark Jelle, 2023

Sheet: /
File: TEC-1G.kicad.sch
Title: TEC-1G (Board revision:)
Size: 12" x 12" Date: 2023-09-24 Rev: 1.0
Kicad: E.D.A., Kicad (6.0.10) 16:1/1