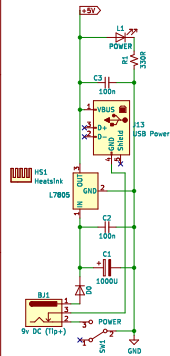


# TEC-1G

## Power Delivery

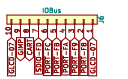


## General Input/Output

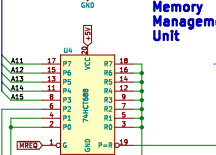


## The TEC Deck

The new way to expand your TEC-1G with appropriate long-legged headers, expansion boards can be stacked on top of each other. Just like the original TEC-1, but now you have access to all the CPU pins as well as port and memory select lines. Memory Expansion of 128k with ease. Input/output options for days!



With the Shadow ROM switch ON (on Reset or OUT FF.501), the lower 2K of the 16K ROM is mapped to the lowest 2K of the memory map. This is to provide backward compatibility to older TEC-1 machines and their ROMs.



## Memory Management Unit

To remove the Shadowed ROM, an output of ONE to Bit 0 of Port FFF removes the ROM from lower 2K. (It is possible to Shadow it back in with an output of 0 to Bit 0 of Port FFF)

The ROM is selected (asserted LOW) if:

Any address in the lower 2K is requested (with Shadow ON)

OR

If an address is within the top 16K of 64K.

OTHERWISE:

The RAM is selected if the address falls within the lower half (32K) of the memory map.

This line is asserted HIGH (through the Inverter) when the Shadow Latch is activated.

AND

All the upper address lines (A11-A15) are LOW, meaning the CPU is addressing the lower 2K range, which where the original TEC-1 ROMs were placed.

## Memory Protection

On Reset, all RAM is writable. Under software control, sending Bit 2 High of Port FFF turns ON write protect of the RAM in the second 16K memory space. Sending to Port FFF a value with Bit 2 clear will remove write protection.

Status lights showing the which output options are active.

This critical latch controls a lot of important functions, and will also be the center of huge memory expansions to come.

STATUS

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## 64k Memory

The lower 32K is all RAM in a single chip.

The upper 16K of the memory map is reserved for the system ROM, although it is made up of a 32K EPROM to allow one of two monitors to be selected by the user with a switch.

This ROM socket can be configured to hold 2K/4K ROMs like the original TEC-1, by moving all 3 jumpers to positions 1-2, and then physically placing the 2K pin ROM in the upper end of the 28 pin socket.

These three jumpers allow for High ROM/RAM to be used in the Expansion socket.

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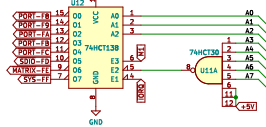
ROM SIZE

ROM SIZE

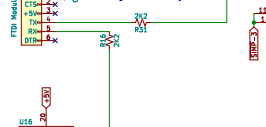
ROM SIZE

ROM SIZE

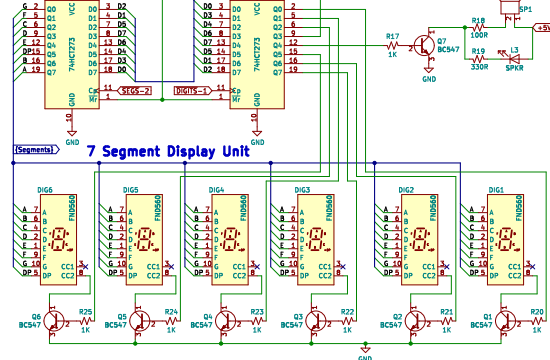
## I/O Decoders



## System Input



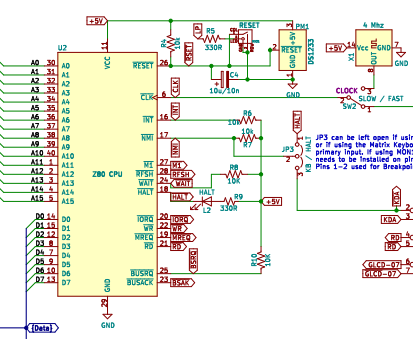
## 7 Segment Display Unit



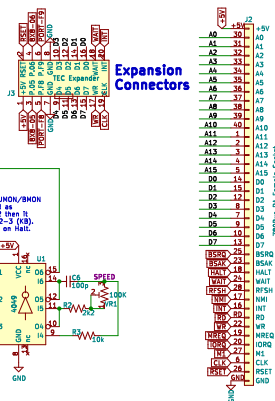
## LCD 20 Characters x 4 Lines



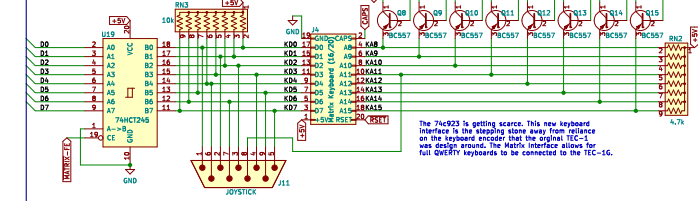
## CPU & Clock



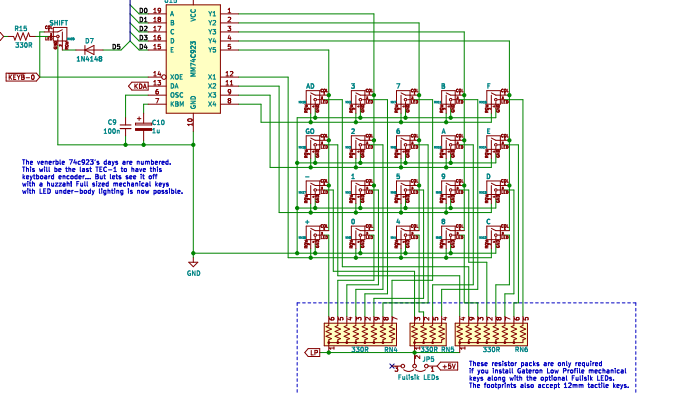
## Expansion Connectors



## Matrix Keyboard & Joystick



## HexPad Encoder



Modelled on the TEC-1 rev.D with DAT add-on  
Originally designed by John Hardy, Ken Stone & Jim Robertson  
published in Talking Electronics Magazine, 1983 - 1985  
Thanks for assistance from: Craig Hart, Brian Chien, Ian McLean  
© Mark Jelle, 2023  
Sheet: /  
File: TEC-1G.kicad.sch  
Title: TEC-1G  
Size: A2 | Date: 2023-08-19 | Rev: 1.5  
Kicad: E.D.A., kicad (6.0.10) | Id: 1/1