SSD1685

Product Proposal

168 /184 /200 /216 Source x 384 Gate

Red/Black/White
Active Matrix EPD Display Driver with Controller

Appendix: IC Revision history of SSD1685 Specification

Version	Change Items	Effective Date
0.10	Initial Release	18-Jun-2020
0.11	Removed the 0.47uF value for C8 from component list (Table 12-1)	22-Oct-2020

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FIGURES

1 GENERAL DESCRIPTION

SSD1685 is an Active Matrix EPD display driver with controller for Red/Black/White EPD displays.

It consists of selectable 168/184/200/216 number of source outputs, 384 gate outputs, 1 VCOM and 1VBD (for border), which can support displays with resolution up to 216 x 384.

In the SSD1685, data and commands are sent from MCU through hardware selectable serial peripheral interface. It has embedded booster, regulator and oscillator which is suitable for EPD display applications.

2 FEATURES

- Design for dot matrix type active matrix EPD display, support Red/Black/White color
- Selectable number of source outputs for 168/184/200/216, 384 gate outputs, 1 VCOM and 1VBD (for border)
- Power supply:
    - VCI: 2.2 to 3.7V
    - VDDIO: Connect to VCI
    - VDD: 1.8V, regulate from VCI supply
- Maximum on chip display RAM:
    - Mono B/W: 216x384 bits
    - Mono Red: 216x384 bits
- On-chip booster and regulator for generating VCOM, Gate and Source driving voltage
- Gate driving output voltage: 2-level outputs (VGH, VGL), Max 40Vp-p
    - VGH: 10V to 20V (Voltage adjustment step: 500mV)
    - VGL: -VGH (Voltage adjustment step: 500mV)
- Source driving output voltage: 4-levels outputs (VSH1, VSH2, VSS and VSL)
    - VSH1: 8.8V to 17V (Voltage adjustment step: 200mV)
    - VSH2: 2.4V to 17V (Voltage adjustment step: 100mV for 2.4V to 8.6V, 200mV for 8.8V to 17V)
    - VSL: -5V to -17V (Voltage adjustment step: 500mV)
- VCOM output voltage
    - DCVCOM: -3.0V to -0.2V in 100mV resolution
    - ACVCOM: 3-level outputs (VSH1+DCVCOM, DCVCOM, VSL+DCVCOM)
- On-chip oscillator, adjustable frame rate from 25Hz to 100Hz
- Programmable output Waveform Settings:
    - Individual setting of 4 LUT [LUTC, LUTB, LUTW, LUTR]
        - VS: 2-bit per 4 phases
    - Individual setting of 4 LUT
        - 32 phases (4 phases/group, 8 groups with repeat and state repeat function)
        - TP: Max. 63 frame/phase
        - RP: 0 to 255 times for repeat count
        - SR: 0 to 255 times for state repeat count; state repeat count for phase A,B and 1 state repeat count for phase C,D
        - XON: All Gate On Selection for each phase A,B and phase C,D
- Embedded OTP to store the waveform settings and parameters:
    - 24 sets of Waveform Settings (WS) including
        - waveform look up table (LUT)
        - Gate/Source voltage
        - VCOM value
        - Frame Rate
        - Option for LUT end
    - 24 sets of Temperature Range (TR)
    - Display mode selection
    - 4-byte waveform version
    - 10-byte User ID
- Embedded OTP to store the initial code setting
- External or internal generated voltage for burning OTP
- Built-in CRC checking method for RAM content and WS & TR in OTP
- VCI low voltage detection
- Driving voltage ready detection
- Support display partial update

- Auto write RAM command for regular patterns
- Internal Temperature Sensor of +/-2degC accuracy from -25degC to 50degC
- I2C single master interface to communicate with external temperature sensor
- MCU interface: 4-wire or 3-wire Serial peripheral interface (maximum SPI write speed 20MHz)
- Available in COG package

3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Package Form	Remark
SSD1685Z	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 12um
SSD1685Z8	Gold Bump Die	Bump Face Down On Waffle pack Die thickness: 300um Bump height: 12um

4 BLOCK DIAGRAM

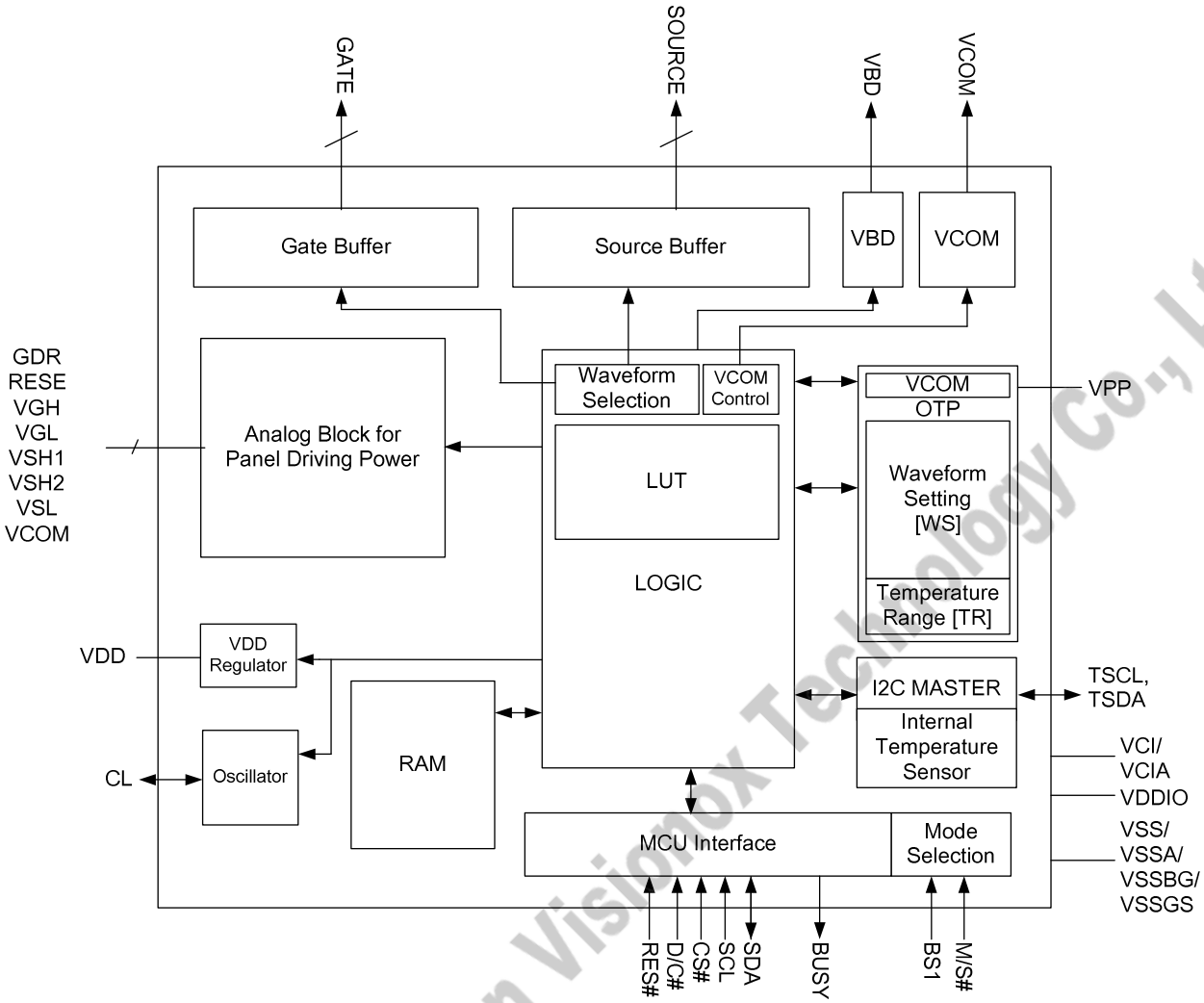


Figure 4-1 : SSD1685 Block Diagram

5 PIN DESCRIPTION

Key:

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin
C = Capacitor Pin
NC = Not Connected

Table 5-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
VCI	P	Power Supply	Power Supply	Power input pin for the chip.	-
VCIA	P	Power Supply	Power Supply	Power input pin for the chip. - Connect to VCI in the application circuit.	-
VDDIO	P	Power Supply	Power for interface logic pins	Power input pin for the Interface. - Connect to VCI in the application circuit.	-
VDD	P	Capacitor	Regulator output	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS under all circumstances.	-
VSS	P	VSS	GND	Ground (Digital).	-
VSSA	P	VSS	GND	Ground (Analog) - Connect to VSS in the application circuit.	-
VSSBG	P	VSS	GND	Ground (Reference) pin. - Connect to VSS in the application circuit.	-
VSSGS	P	VSS	GND	Ground (Output) pin. - Connect to VSS in the application circuit.	-
VPP	P	Power Supply	OTP power	Power Supply for OTP Programming.	Open

Table 5-2: Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use
SCL	I	MPU	Data Bus	This pin is serial clock pin for interface. Refer to MCU interface in Section 6.1.	-
SDA	I/O	MPU	Data Bus	This pin is serial data pin for interface. Refer to MCU interface in Section 6.1.	-
CS#	I	MPU	Logic Control	This pin is the chip select input connecting to the MCU. Refer to MCU interface in Section 6.1.	VDDIO or VSS
D/C#	I	MPU	Logic Control	This pin is Data/Command control pin connecting to the MCU. Refer to MCU interface in Section 6.1.	VDDIO or VSS
RES#	I	MPU	System Reset	This pin is reset signal input. Active Low.	-
BUSY	O	MPU	Device Busy Signal	This pin is Busy state output pin. When Busy is High, the operation of the chip should not be interrupted, and command should not be sent. For example., The chip would output Busy pin as High when - Outputting display waveform; or - Programming with OTP - Communicating with digital temperature sensor	Open
M/S#	I	VDDIO/VSS	Cascade Mode Selection	This pin is Master and Slave selection pin. - For the single chip application, the M/S# pin should be connected to VDDIO. - In the cascade mode: For Master Chip, the M/S# pin should be connected to VDDIO. For Slave Chip, the M/S# pin should be connected to VSS. The oscillator, booster and regulator circuits of the slave chip will be disabled. The corresponding pins including CL, VDD, VDDIO, VGH, VGL, VSH1, VSH2, VSL and VCOM must be connected to the master chip.	-
CL	I/O	NC	Clock signal	This pin is the clock signal pin. - For the single chip application, the CL pin should be left open. - In the cascade mode, the CL pin of the slave chip should be connected to the CL pin of the master chip.	-
BS	I	VDDIO/VSS	MCU Interface Mode Selection	This pin is for selecting 3-wire or 4-wire SPI bus. **BS1** / **MCU Interface** L / 4-wire SPI H / 3-wire SPI (9-bit SPI)	-
TSDA	I/O	Temperature sensor SDA	Interface to Digital Temp. Sensor	This pin is I^2C Interface to digital temperature sensor Data pin. External pull up resistor is required when connecting to I^2C slave.	VSS
TSCL	O	Temperature sensor SCL	Interface to Digital Temp. Sensor	This pin is I^2C Interface to digital temperature sensor Clock pin. External pull up resistor is required when connecting to I^2C slave.	VSS

Table 5-3: Analog Pins

Name	Type	Connect to	Function	Description	When not in use
GDR	O	POWER MOSFET Driver Control	VGH, VGL Generation	This pin is N-Channel MOSFET gate drive control pin.	-
RESE	I	Booster Control Input		This pin is Current sense input pin for the control Loop.	-
VGH	C	Stabilizing capacitor		This pin is Positive Gate driving voltage. Connect a stabilizing capacitor between VGH and VSS in the application circuit.	-
VGL	C	Stabilizing capacitor		This pin is Negative Gate driving voltage. Connect a stabilizing capacitor between VGL and VSS in the application circuit.	-
VSH1	C	Stabilizing capacitor	VSH1, VSH2, VSL Generation	This pin is Positive Source driving voltage, VSH1 Connect a stabilizing capacitor between VSH1 and VSS in the application circuit.	-
VSH2	C	Stabilizing capacitor		This pin is Positive Source driving voltage, VSH2 Connect a stabilizing capacitor between VSH2 and VSS in the application circuit.	
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage. Connect a stabilizing capacitor between VSL and VSS in the application circuit.	-
VCOM	C	Panel/ Stabilizing capacitor	VCOM Generation	This pins is VCOM driving voltage Connect a stabilizing capacitor between VCOM and VSS in the application circuit.	-

Table 5-4: Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
S [215:0]	O	Panel	Source driving signal	Source output pin.	Open
G [383:0]	O	Panel	Gate driving signal	Gate output pin.	Open
VBD	O	Panel	Border driving signal	Border output pin.	Open

Table 5-5: Miscellaneous Pins

Name	Type	Connect to	Function	Description	When not in use
NC	NC	NC	Not Connected	This is dummy pin. It should not be connected with other NC pins.	Open
RSV	NC	NC	Reserved	This is a reserved pin and should be kept open.	Open
TPA, TPB, TPC, TPD, TPF, FB	NC	NC	Reserved for Testing	Reserved pins. - Keep open. - Do not connect to other NC pins and test pins including TPA, TPB, TPC, TPD, TPE, TPF, TIN and FB.	Open
TIN	I	TPE	Reserved for Testing	This is a reserved pin and should be connected to TPE pin	VSS/VDDIO
TPE	O	TIN	Reserved for Testing	This is a reserved pin and should be connected to TIN pin	Open

6 Functional Block Description

6.1 MCU Interface

6.1.1 MCU Interface selection

The SSD1685 can support 3-wire/4-wire serial peripheral. MCU interface is pin selectable by BS1 shown in Table 6-1.

Table 6-1 : Interface pins assignment under different MCU interface

	Pin Name					
MCU Interface	**BS1**	**RES#**	**CS#**	**D/C#**	**SCL**	**SDA**
4-wire serial peripheral interface (SPI)	L	RES#	CS#	DC#	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	RES#	CS#	L	SCL	SDA

Note

(1) L is connected to V_{SS} and H is connected to V_{DDIO}

6.1.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 6-2 and the write procedure 4-wire SPI is shown in Table 6-2

Table 6-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:

(1) L is connected to VSS and H is connected to VDDIO
(2) ↑ stands for rising edge of signal
(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

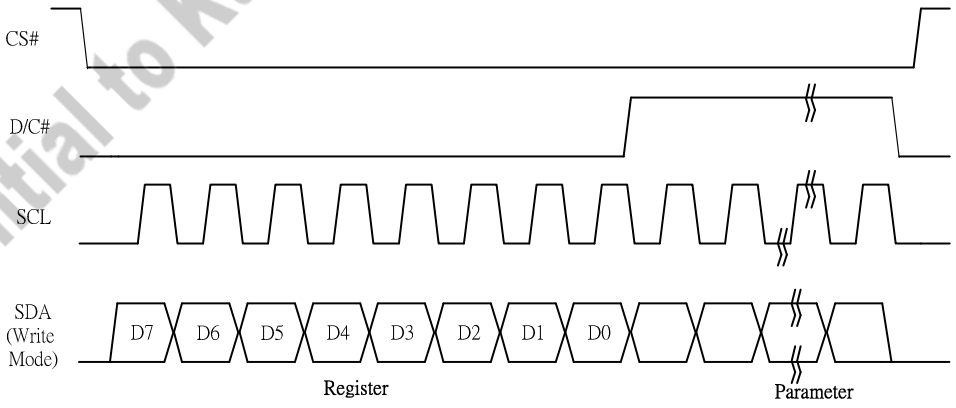


Figure 6-1 : Write procedure in 4-wire SPI mode

In the read operation (Command 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). After CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 6-2 shows the read procedure in 4-wire SPI.

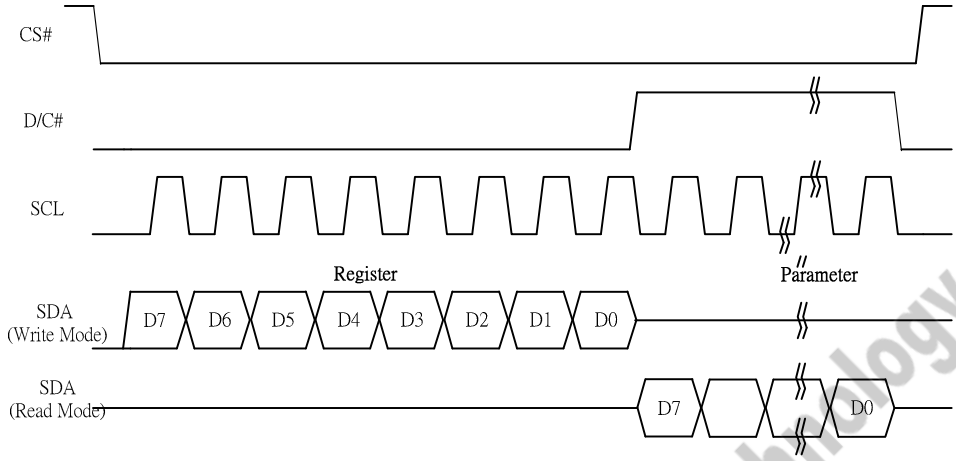


Figure 6-2 : Read procedure in 4-wire SPI mode

6.1.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 6-3 shows the write procedure in 3-wire SPI

Table 6-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to V_{SS} and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

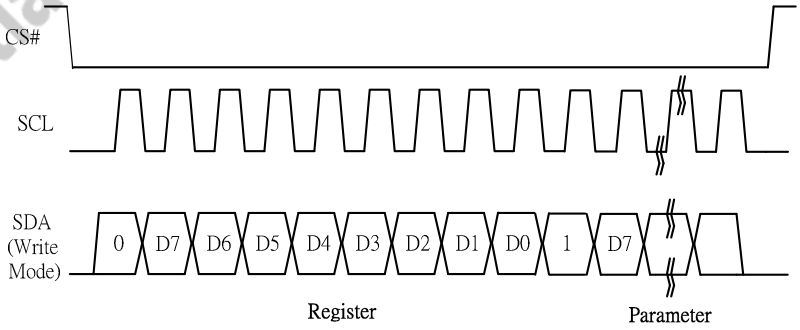


Figure 6-3 : Write procedure in 3-wire SPI

In the read operation (Register 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). SDA data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 6-4 shows the read procedure in 3-wire SPI.

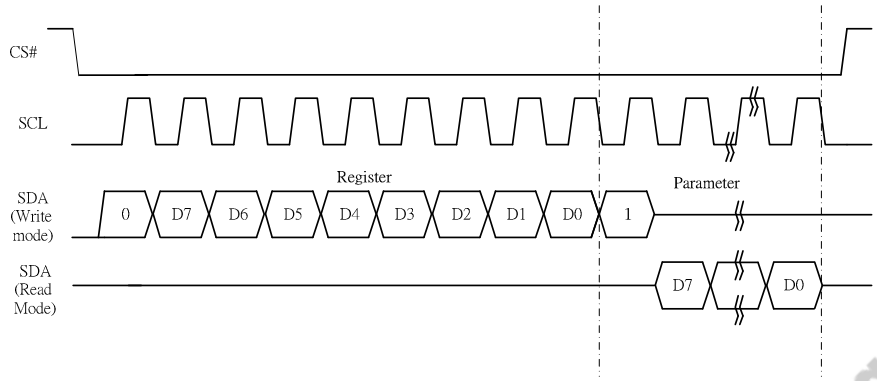


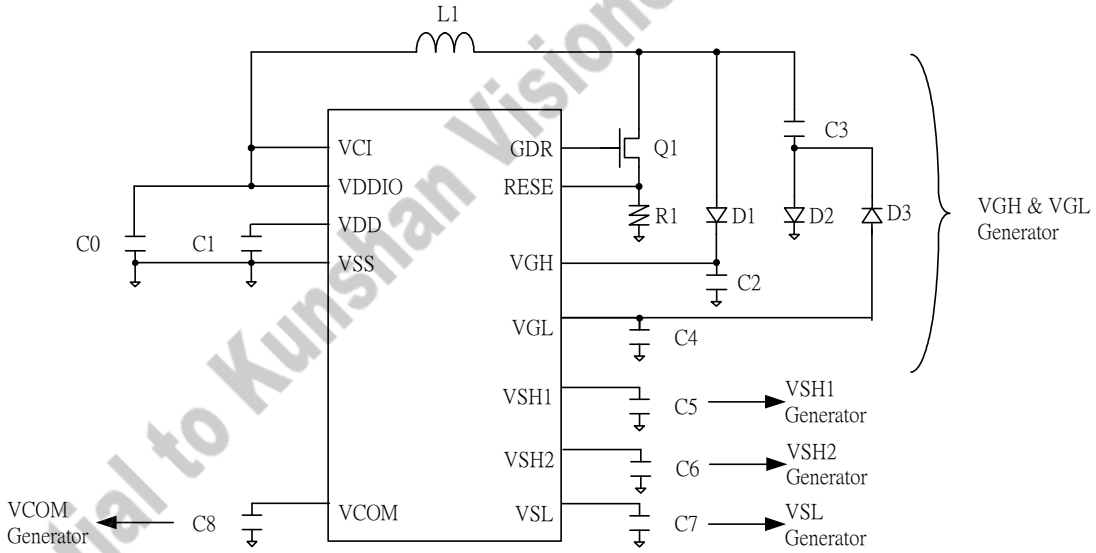
Figure 6-4 : Read procedure in 3-wire SPI mode

6.2 OSCILLATOR

The oscillator module generates the clock reference for waveform timing and analog operations.

6.3 BOOSTER & REGULATOR

A voltage generation system is included in the driver. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH1, VSH2, VSL and VCOM. External application circuit is needed to make the on-chip booster & regulator circuit work properly.



6.4 VCOM SENSING

This functional block provides the scheme to select the optimal VCOM DC level. The sensed value can be programmed into OTP.

The flow of VCOM sensing:

- Active Gate is scanning during the VCOM sense Period.
- Source are VSS.
- VCOM pin used for sensing.
- During Sensing period, BUSY is high.
- After Sensing, Active Gate return to non-select stage.

6.5 RAM

The On chip display RAM is holding the image data.
1 set of RAM is built for Mono B/W. The RAM size is 216x384 bits.
1 set of RAM is built for Mono Red. The RAM size is 216x384 bits.

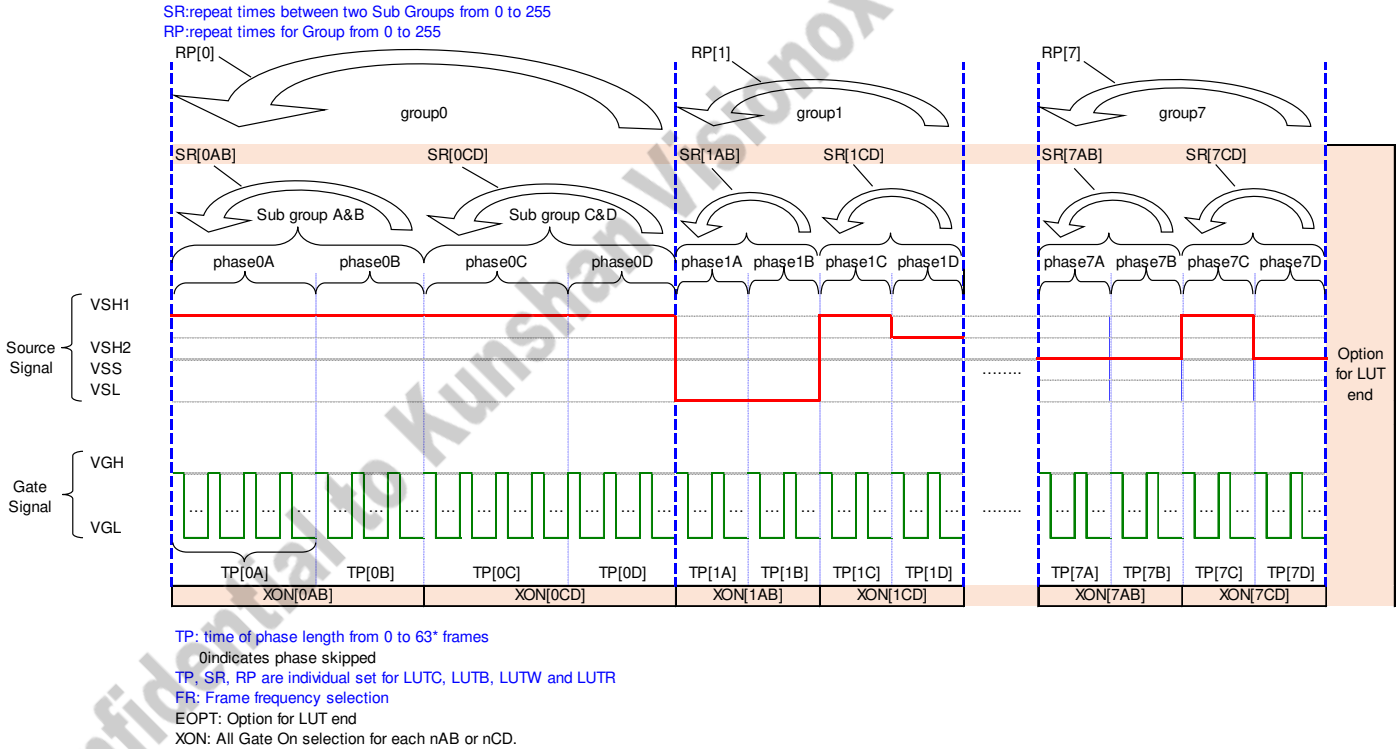
Table 6-4 : RAM bit and LUT mapping for 3-color display

Data bit in R RAM	Data bit in B/W RAM	Image Color	LUT
0	0	Black	LUTB for driving Black
0	1	White	LUTW for driving White
1	0	Red	LUTR for driving Red

Table 6-5 : RAM bit and LUT mapping for black/white display

Data bit in R RAM	Data bit in B/W RAM	Image Color	LUT
0	0	Black	LUTBB for driving Black
0	1	White	LUTWB for driving White
1	0	Black	LUTBW = LUTBB
1	1	White	LUTWW = LUTWB

6.6 Programmable Waveform for Gate, Source and VCOM



TP: time of phase length from 0 to 63* frames
0indicates phase skipped
TP, SR, RP are individual set for LUTC, LUTB, LUTW and LUTR
FR: Frame frequency selection
EOPT: Option for LUT end
XON: All Gate On selection for each nAB or nCD.

Figure 6-5 : Gate waveform and Programmable Source and VCOM waveform illustration

In the programmable waveform for Source and VCOM, there are 8 groups (Group0 to Group7) and each group has 4 phases (Phase A to Phase D) and 2 state repeats (Phase A and B, Phase C and D). Totally, there are 32 phases. In addition, in each phase, the phase length (TP[nX]) can be set by number of frame from 0 to 63 frames. Also, each group can be repeated with repeat counting number (RP[n]) from 0 to 255 times; each AB / CD phases can be repeated with state repeat counting number (SR[nAB]/SR[nCD]) from 0 to 255 times. For the voltage, there is four levels for Source voltage (VSS, VSH1, VSH2, VSL) and four levels for VCOM voltage (DCVCOM, VSH1+DCVCOM, VSL+DCVOM, Floating and VSS).

The description of each parameter is as follows.

1) TP[nX] represents the phase length set by the number of frame.
- The range of TP[nX] is from 0 to 63.
- n represents the Group number from 0 to 7; X represents the phase number from A to D.
- When TP[nX] = 0, the phase is skipped. When TP[nX] = 1, the phase is 1 frame, and so on. The maximum phase length is 63 frame.

2) RP[n] represents the repeat counting number for the Group.
- The range of RP[n] is from 0 to 255.
- n represents the Group number from 0 to 7.
- RP[n] = 0 indicates that the group is skipped, RP[n] = 1 indicates that the repeat times = 1, and so on. The maximum repeat times is 255.

3) SR[nAB] and SR[nCD] represent the state repeat counting number for Phase A & B and Phase C & D respectively.
- The range of SR[nXY] is from 0 to 255.
- n represents the Group number from 0 to 7.
- SR[nXY] = 0 indicates that the sub-group is skipped, SR[nXY] = 1 indicates that the repeat times = 1, and so on. The maximum repeat times is 255.

4) VS[nX-LUTm] represents Source and VCOM voltage level which is used in each phase. Table 6-6 shows the voltage settings for source voltage and VCOM voltage.
- n represents the Group number from 0 to 7.
- m represents the LUT number from 0-3.

Table 6-6 : VS[nX-LUTm] settings for Source voltage and VCOM voltage

VS[nX-LUTm]	Source voltage	VCOM voltage
00	VSS	DCVCOM
01	VSH1	VSH1 + DCVCOM
10	VSL	VSL + DCVCOM
11	VSH2	Floating

5) FR indicates the frame rate

FR[3:0]	Frame Rate	FR[3:0]	Frame Rate
0001	25 Hz	1001	37.5 Hz
0010	50 Hz	1010	62.5 Hz
0011	75 Hz	1011	87.5 Hz
0100	100 Hz	1100	112.5 Hz
0101	125 Hz	1101	137.5 Hz
0110	150 Hz	1110	162.5 Hz
0111	175 Hz	1111	187.5 Hz
1000	200 Hz		

6) XON[nAB] and XON[nCD], indicates the gate scan selection.
- n represents the Group number from 0 to 7.
- XON[nXY] = 0 indicates Normal gate scan in Phase[nX] & Phase[nY].
- XON[nXY] = 1 indicates All gate on, that Gate keeps High until the phase for normal gate scan, in Phase[nX] & Phase[nY].

6.7 WAVEFORM SETTING

As described in Section 6.6, parameters VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR[n] and XON[nXY] are used to define the driving waveform. In the SSD1685, there are 233 bytes in the waveform setting to store LUTB, LUTW, LUTR and LUTC, gate voltage, source voltage and frame rate. The waveform LUT of a particular temperature range can be loaded from OTP or written by MCU.

- WS byte 0~226, the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR and XON[nXY] are defined by Register 0x32
- WS byte 227, the content of Option for LUT end, is the parameter belonging to register 0x3F.
- WS byte 228, the content of gate level, is the parameter defined by Register 0x03.
- WS byte 229~231, the content of source level, is the parameter defined by Register 0x04.
- WS byte 232, the content of VCOM level，is the parameter defined by Register 0x2C.

The SSD1685 waveform setting is shown in in Figure 6-6: Waveform Setting mapping

addr.	D7	D6	D5	D4	D3	D2	D1	D0
0	RP LUTC 0							
1	VS-0A-LUTC		TP LUTC 0A					
2	VS-0B-LUTC		TP LUTC 0B					
3	VS-0C-LUTC		TP LUTC 0C					
4	VS-0D-LUTC		TP LUTC 0D					
5	SR LUTC 0AB							
6	SR LUTC 0CD							
7	RP LUTC 1							
8	VS-1A-LUTC		TP LUTC 1A					
9	VS-1B-LUTC		TP LUTC 1B					
10	VS-1C-LUTC		TP LUTC 1C					
11	VS-1D-LUTC		TP LUTC 1D					
12	SR LUTC 1AB							
13	SR LUTC 1CD							
14	RP LUTC 2							
…	…							
…	…							
…	…							
50	VS-7A-LUTC		TP LUTC 7A					
51	VS-7B-LUTC		TP LUTC 7B					
52	VS-7C-LUTC		TP LUTC 7C					
53	VS-7D-LUTC		TP LUTC 7D					
54	SR LUTC 7AB							
55	SR LUTC 7CD							
56	RP LUTR 0							
57	VS-0A-LUTR		TP LUTR 0A					
58	VS-0B-LUTR		TP LUTR 0B					
59	VS-0C-LUTR		TP LUTR 0C					
60	VS-0D-LUTR		TP LUTR 0D					
61	SR LUTR 0AB							
62	SR LUTR 0CD							
63	RP LUTR 1							
64	VS-1A-LUTR		TP LUTR 1A					
65	VS-1B-LUTR		TP LUTR 1B					
66	VS-1C-LUTR		TP LUTR 1C					
67	VS-1D-LUTR		TP LUTR 1D					
68	SR LUTR 1AB							
69	SR LUTR 1CD							
70	RP LUTR 2							
…	…							
…	…							
…	…							
106	VS-7A-LUTR		TP LUTR 7A					
107	VS-7B-LUTR		TP LUTR 7B					
108	VS-7C-LUTR		TP LUTR 7C					
109	VS-7D-LUTR		TP LUTR 7D					
110	SR LUTR 7AB							
111	SR LUTR 7CD							

addr.	D7	D6	D5	D4	D3	D2	D1	D0
112	RP LUTW 0							
113	VS-0A-LUTW		TP LUTW 0A					
114	VS-0B-LUTW		TP LUTW 0B					
115	VS-0C-LUTW		TP LUTW 0C					
116	VS-0D-LUTW		TP LUTW 0D					
117	SR LUTW 0AB							
118	SR LUTW 0CD							
119	RP LUTW 1							
120	VS-1A-LUTW		TP LUTW 1A					
121	VS-1B-LUTW		TP LUTW 1B					
122	VS-1C-LUTW		TP LUTW 1C					
123	VS-1D-LUTW		TP LUTW 1D					
124	SR LUTW 1AB							
125	SR LUTW 1CD							
126	RP LUTW 2							
…	…							
…	…							
…	…							
162	VS-7A-LUTW		TP LUTW 7A					
163	VS-7B-LUTW		TP LUTW 7B					
164	VS-7C-LUTW		TP LUTW 7C					
165	VS-7D-LUTW		TP LUTW 7D					
166	SR LUTW 7AB							
167	SR LUTW 7CD							
168	RP LUTB 0							
169	VS-0A-LUTB		TP LUTB 0A					
170	VS-0B-LUTB		TP LUTB 0B					
171	VS-0C-LUTB		TP LUTB 0C					
172	VS-0D-LUTB		TP LUTB 0D					
173	SR LUTB 0AB							
174	SR LUTB 0CD							
175	RP LUTB 1							
176	VS-1A-LUTB		TP LUTB 1A					
177	VS-1B-LUTB		TP LUTB 1B					
178	VS-1C-LUTB		TP LUTB 1C					
179	VS-1D-LUTB		TP LUTB 1D					
180	SR LUTB 1AB							
181	SR LUTB 1CD							
182	RP LUTB 2							
…	…							
…	…							
…	…							
218	VS-7A-LUTB		TP LUTB 7A					
219	VS-7B-LUTB		TP LUTB 7B					
220	VS-7C-LUTB		TP LUTB 7C					
221	VS-7D-LUTB		TP LUTB 7D					
222	SR LUTB 7AB							
223	SR LUTB 7CD							
224	FR							
225	XON3CD	XON3AB	XON2CD	XON2AB	XON1CD	XON1AB	XON0CD	XON0AB
226	XON7CD	XON7AB	XON6CD	XON6AB	XON5CD	XON5AB	XON4CD	XON4AB
227	EOPT							
228	VGH							
229	VSH1							
230	VSH2							
231	VSL							
232	VCOM							

6.8 Temperature Searching

The SSD1685 has internal temperature sensor to detect the environment temperature or can communicate with the external temperature sensor by I2C single master interface or can communicate with the external MCU to get the temperature value through SPI. In the SSD1685, there is a dedicated format for the temperature value so that the driver IC can understand it. The format of temperature value is described in Section 6.8.3.

6.8.1 Internal Temperature Sensor

The internal temperature sensor can be selected by command register. The accuracy of it is ±2degC from -25degC to 50degC.

6.8.2 External Temperature Sensor I2C Single Master Interface

The driver IC can communicate with the external temperature sensor through I2C single master interface (TSDA and TSCL). TSDA will be SDA and TSCL will be SCL. TSDA and TSCL are required to connect with external pull-up resistor. Temperature register value of external temperature sensor can be read by command register.

6.8.3 Format of temperature value

The temperature value is defined by 8-bit binary. The rules are shown as below.

- If the Temperature value MSByte bit D11 = 0, then
  the temperature is positive and value (DegC) = + (Temperature value)
- If the Temperature value MSByte bit D11 = 1, then
  the temperature is negative and value (DegC) = - (2's complement of Temperature value)

Table 6-7 shows some examples of 8-bit binary temperature value:

Table 6-7 : Example of 8-bit binary temperature settings for temperature ranges

8-bit binary (2's complement)	Hexadecimal Value	TR Value [DegC]
0111 1111	7F	12B
0110 0100	64	100
0101 0000	50	80
0100 1011	4B	75
0011 0010	32	50
0001 1001	19	25
0000 0000	00	0
1111 1111	FF	-1
1110 0111	E7	-25
1100 1001	C9	-55

6.9 Waveform Setting searching mechanism

As mentioned in Section 6.7, the SSD1685 OTP can store waveform setting and temperature range. If waveform setting and temperature range are programmed in OTP memory, corresponding waveform LUT can be selected according to the sensed temperature to drive the display. The Waveform Setting searching mechanism by driver IC is as follows.

1) Read temperature value by command register in the format of 8-bit binary.
2) According to read temperature and display mode selection, search LUT in OTP from TR0 to TR23 in sequence. The last match will be selected, then, the corresponding WS will be loaded in the LUT register to drive the display.

Remark: Waveform LUT selection criteria is "Lower temperature bound < Sensed temperature ≤ Upper temperature bound".

Table 6-8 shows an example for the waveform LUT searching from OTP:

- If the read temperature is 25degC, then, WS4 will be selected.
- If the read temperature is 34degC, then, WS7 will be selected. Although 34degC is also in the temperature range TR6, according to searching mechanism, the last match should be selected. Therefore, WS7 is selected.

Table 6-8 : Example of waveform settings selection based on temperature ranges.

Waveform LUT in OTP	Temperature Range in OTP	TR Lower Limit [Hex]	TR Upper Limit [Hex]	Temperature range in OTP
WS0	TR0	80	05	-128 DegC < Temperature ≤ 5 DegC
WS1	TR1	05	0A	5 DegC < Temperature ≤ 10DegC
WS2	TR2	0A	0F	10 DegC < Temperature ≤ 15DegC
WS3	TR3	0F	14	15 DegC < Temperature ≤ 20DegC
WS4	TR4	14	19	20 DegC < Temperature ≤ 25DegC
WS5	TR5	19	1E	25 DegC < Temperature ≤ 30DegC
WS6	TR6	1E	23	30 DegC < Temperature ≤ 35DegC
WS7	TR7	21	7F	33 DegC < Temperature ≤ 127DegC
Others	Others	00	00	

Precaution:
Please ensure the temperature range covers whole range of application temperatures, display will not be updated if no suitable temperature range matches the sensed temperature.

6.10 One Time Programmable (OTP) Memory

In the SSD1685, there is an embedded OTP memory which is designed to store the waveform settings of different temperature range and some variables/parameters. The OTP memory can store 24 sets of waveform LUT settings (WS), 24 sets of temperature range (TR), VCOM value, display mode selection, waveform version and user ID. Figure 6 7 shows the address mapping of the 24 waveform setting (WS0 to WS23) and temperature range (TR0 to TR23).

addr.	D7	D6	D5	D4	D3	D2	D1	D0
0	WS0							
…								
232								
233	WS1							
…								
465								
466	WS2							
…								
698								
699	WS3							
…								
931								
932	WS4							
…								
1164								
	…							
5126	WS22							
…								
5358								
5359	WS23							
…								
5591								
5592	TR0							
5593								
5594	TR1							
5595								
5596	TR2							
5597								
5598	TR3							
5599								
5600	TR4							
5601								
	…							
5636	TR22							
5637								
5638	TR23							
5639								

Figure 6-7 : The Waveform setting mapping in OTP for waveform setting and temperature range

6.11 The Format for Temperature Range (TR)

The format of TR Lower limit and Upper limit as shown in Figure 6-8 which temp_L[7:0] is the lower limit and temp_H[7:0] is the upper limit of the temperature range. There has 24sets of TR for waveform LUT searching.

D7	D6	D5	D4	D3	D2	D1	D0
temp_L[7:0]							
temp_H[7:0]							

Figure 6-8 : Format of Temperature Range (TR) in OTP

6.12 Cascade Mode

The SSD1685 has a cascade mode that can cascade 2 chips to achieve the display resolution up to 432 (sources) x 384 (gates). The pin M/S# is used to configure the chip. When M/S# is connected to VDDIO, the chip is configured as a master chip. When M/S# is connected to VSS, the chip is configured as a slave chip.

When the chip is configured as a master chip, it will be the same as a single chip application, ie, all circuit blocks will be worked as usual. When the chip is configured as a slave chip, its oscillator and booster & regulator circuit will be disabled. The oscillator clock and all booster voltages will be come from the master chip. Therefore, the corresponding pins including CL, VDD, VGH, VGL, VSH1, VSH2, VSL, VGL and VCOM must be connected to the master chip.

6.13 VCI Detection

The VCI detection function is used to detect the VCI level when it is lower than Vlow, threshold voltage set by register.

In SSD1685, there is a command to execute the VCI detection function. When the VCI detection command is issued, the VCI detection will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, user can issue the Status Bit Read command to check the status bit for the result of VCI, which 0 is normal, 1 is VCI<Vlow.

6.14 HV Ready Detection

The HV Ready detection function is used to detect whether the analog block is ready.

In SSD1685, there is a command to execute the HV Ready detection function. When the HV Ready detection command is issued, the HV Ready will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, user can issue the Status Bit Read command to check the status bit for the result of HV Ready, which 0 is normal, 1 indicate HV is not ready.

7 COMMAND TABLE

Table 7-1: Command Table

<table>
<tr><th colspan="12">Command Table</th></tr>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output control</td><td rowspan="4">Gate setting
A[8:0]= 17Fh [POR], 384 MUX
MUX Gate lines setting as (A[8:0] + 1).

B [2:0] = 000 [POR].
Gate scanning sequence and direction

B[2]: GD
Selects the 1st output Gate
GD=0 [POR],
G0 is the 1st gate output channel, gate output sequence is G0, G1, G2, G3, …
GD=1,
G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, …

B[1]: SM
Change scanning order of gate driver.
SM=0 [POR],
G0, G1, G2, G3…G382, G383 (left and right gate interlaced)
SM=1,
G0, G2, G4 …G382, G1, G3, …G383

B[0]: TB
TB = 0 [POR], scan from G0 to G383
TB = 1, scan from G383 to G0.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Gate Driving voltage Control</td><td rowspan="2">Set Gate driving voltage
A[4:0] = 00h [POR]
VGH setting from 10V to 20V
<table><tr><th>A[4:0]</th><th>VGH</th><th>A[4:0]</th><th>VGH</th></tr><tr><td>00h</td><td>20</td><td>0Dh</td><td>15</td></tr><tr><td>03h</td><td>10</td><td>0Eh</td><td>15.5</td></tr><tr><td>04h</td><td>10.5</td><td>0Fh</td><td>16</td></tr><tr><td>05h</td><td>11</td><td>10h</td><td>16.5</td></tr><tr><td>06h</td><td>11.5</td><td>11h</td><td>17</td></tr><tr><td>07h</td><td>12</td><td>12h</td><td>17.5</td></tr><tr><td>08h</td><td>12.5</td><td>13h</td><td>18</td></tr><tr><td>07h</td><td>12</td><td>14h</td><td>18.5</td></tr><tr><td>08h</td><td>12.5</td><td>15h</td><td>19</td></tr><tr><td>09h</td><td>13</td><td>16h</td><td>19.5</td></tr><tr><td>0Ah</td><td>13.5</td><td>17h</td><td>20</td></tr><tr><td>0Bh</td><td>14</td><td>Other</td><td>NA</td></tr><tr><td>0Ch</td><td>14.5</td><td></td><td></td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B [7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V Remark: VSH1>=VSH2
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

B[7] = 1,
VSH2 voltage setting from 2.4V to 8.6V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AEh	5.6
8Fh	2.5	AFh	5.7
90h	2.6	B0h	5.8
91h	2.7	B1h	5.9
92h	2.8	B2h	6
93h	2.9	B3h	6.1
94h	3	B4h	6.2
95h	3.1	B5h	6.3
96h	3.2	B6h	6.4
97h	3.3	B7h	6.5
98h	3.4	B8h	6.6
99h	3.5	B9h	6.7
9Ah	3.6	BAh	6.8
9Bh	3.7	BBh	6.9
9Ch	3.8	BCh	7
9Dh	3.9	BDh	7.1
9Eh	4	BEh	7.2
9Fh	4.1	BFh	7.3
A0h	4.2	C0h	7.4
A1h	4.3	C1h	7.5
A2h	4.4	C2h	7.6
A3h	4.5	C3h	7.7
A4h	4.6	C4h	7.8
A5h	4.7	C5h	7.9
A6h	4.8	C6h	8
A7h	4.9	C7h	8.1
A8h	5	C8h	8.2
A9h	5.1	C9h	8.3
AAh	5.2	CAh	8.4
ABh	5.3	CBh	8.5
ACh	5.4	CCh	8.6
ADh	5.5	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 8.8V to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
21h	8.8	37h	13
23h	9	38h	13.2
24h	9.2	39h	13.4
25h	9.4	3Ah	13.6
26h	9.6	3Bh	13.8
27h	9.8	3Ch	14
28h	10	3Dh	14.2
29h	10.2	3Eh	14.4
2Ah	10.4	3Fh	14.6
2Bh	10.6	40h	14.8
2Ch	10.8	41h	15
2Dh	11	42h	15.2
2Eh	11.2	43h	15.4
2Fh	11.4	44h	15.6
30h	11.6	45h	15.8
31h	11.8	46h	16
32h	12	47h	16.2
33h	12.2	48h	16.4
34h	12.4	49h	16.6
35h	12.6	4Ah	16.8
36h	12.8	4Bh	17
		Other	NA

C[7] = 0,
VSL setting from -5V to -17V

C[7:0]	VSL
0Ah	-5
0Ch	-5.5
0Eh	-6
10h	-6.5
12h	-7
14h	-7.5
16h	-8
18h	-8.5
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

0	0	08	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.

0	0	09	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write Register for Initial Code Setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of Initial Code Setting
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0A	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR] Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]:
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		0	0	D_5	D_4	D_3	D_2	D_1	D_0		

Bit[6:4]	Driving Strength Selection
000	1(Weakest)
001	2
010	3
011	4
100	5
101	6
110	7
111	8(Strongest)

Bit[3:0]	Min Off Time Setting of GDR [Time unit]
0000 ~ 0011	NA
0100	2.6
0101	3.2
0110	3.9
0111	4.6
1000	5.4
1001	6.3
1010	7.3
1011	8.4
1100	9.8
1101	11.5
1110	13.8
1111	16.5

D[5:0]: duration setting of phase
D[5:4]: duration setting of phase 3
D[3:2]: duration setting of phase 2
D[1:0]: duration setting of phase 1

Bit[1:0]	Duration of Phase [Approximation]
00	10ms
01	20ms
10	30ms
11	40ms

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2 After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	1		0	0	0	0	0	0	A_1	A_0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM data are unaffected by this command.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[7:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	A_6	A_5	A_4	0	A_2	A_1	A_0		A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect A[2:0] / VCI level 011 / 2.2V 100 / 2.3V 101 / 2.4V 110 / 2.5V 111 / 2.6V Other / NA The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperatrure sensor A[7:0] = 80h Internal temperature sensor
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] = 7Fh [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6] A[7:6] – Select no of byte to be sent 00 – Address + pointer 01 – Address + pointer + 1st parameter 10 – Address + pointer + 1st parameter + 2nd pointer 11 – Address A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] B[7:0] = 00h [POR] A[7:4] Red RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content A[3:0] BW RAM option 0000 – Normal 0100 – Bypass RAM content as 0 1000 – Inverse RAM content B[7:6] Resolution select 00 – Display resolution is 200x384 01 – Display resolution is 184x384 10 – Display resolution is 168x384 11 – Display resolution is 216x384
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	0	0	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Operating sequence	Parameter (in Hex)
Enable clock signal	80
Disable clock signal	01
Enable clock signal ➔ Enable Analog	C0
Disable Analog ➔ Disable clock signal	03
Enable clock signal ➔ Load LUT with DISPLAY Mode 1 ➔ Disable clock signal	91
Enable clock signal ➔ Load LUT with DISPLAY Mode 2 ➔ Disable clock signal	99
Enable clock signal ➔ Load temperature value ➔ Load LUT with DISPLAY Mode 1 ➔ Disable clock signal	B1
Enable clock signal ➔ Load temperature value ➔ Load LUT with DISPLAY Mode 2 ➔ Disable clock signal	B9
Enable clock signal ➔ Enable Analog ➔ Display with DISPLAY Mode 1 ➔ Disable Analog ➔ Disable OSC	C7
Enable clock signal ➔ Enable Analog ➔ Display with DISPLAY Mode 2 ➔ Disable Analog ➔Disable OSC	CF
Enable clock signal ➔Enable Analog ➔ Load temperature value ➔ DISPLAY with DISPLAY Mode 1 ➔ Disable Analog ➔ Disable OSC	F7
Enable clock signal ➔Enable Analog ➔ Load temperature value ➔ DISPLAY with DISPLAY Mode 2 ➔ Disable Analog ➔ Disable OSC	FF

0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[3:0] = 9h, duration = 10s. VCOM sense duration = (A[3:0]+1) sec
0	1		0	1	0	0	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[7:0]	VCOM	A[7:0]	VCOM
08h	-0.2	44h	-1.7
0Ch	-0.3	48h	-1.8
10h	-0.4	4Ch	-1.9
14h	-0.5	50h	-2
18h	-0.6	54h	-2.1
1Ch	-0.7	58h	-2.2
20h	-0.8	5Ch	-2.3
24h	-0.9	60h	-2.4
28h	-1	64h	-2.5
2Ch	-1.1	68h	-2.6
30h	-1.2	6Ch	-2.7
34h	-1.3	70h	-2.8
38h	-1.4	74h	-2.9
3Ch	-1.5	78h	-3
40h	-1.6	Other	NA

0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
1	1		K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0		
0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 30 Byte User ID stored in OTP: A[7:0]]~AD[7:0]: UserID (R38, Byte A and Byte AD) [30 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .		
1	1		Z_7	Z_6	Z_5	Z_4	Z_3	Z_2	Z_1	Z_0		
1	1		AA_7	AA_6	AA_5	AA_4	AA_3	AA_2	AA_1	AA_0		
1	1		AB_7	AB_6	AB_5	AB_4	AB_3	AB_2	AB_1	AB_0		
1	1		AC_7	AC_6	AC	AC_4	AC_3	AC_2	AC_1	AC_0		
1	1		AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01]

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
1	1		0	0	A_5	A_4	0	0	A_1	A_0		A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [227 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR and XON[nXY] Refer to Session 6.7 WAVEFORM SETTING
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		:	:	:	:	:	:	:	:		
0	1		.	..	.	.	.	.	.	.		
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command For details, please refer to SSD1685 application note. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8		
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option A[7] Spare VCOM OTP selection 0: Default [POR] 1: Spare B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] 0: Display Mode 1 1: Display Mode 2 F[6]: Ping-Pong for Display Mode 2 0: RAM Ping-Pong disable [POR] 1: RAM Ping-Pong enable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]~J[7:0] can be stored in OTP 2) RAM Ping-Pong function is not support for Display Mode 1
0	1		A_7	0	0	0	0	0	0	0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		0	F_6	0	0	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~AD[7:0]: UserID [30 bytes] Remarks: A[7:0]~AD[7:0] can be stored in OTP
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .		
0	1		Z_7	Z_6	Z_5	Z_4	Z_3	Z_2	Z_1	Z_0		
0	1		AA_7	AA_6	AA_5	AA_4	AA_3	AA_2	AA_1	AA_0		
0	1		AB_7	AB_6	AB_5	AB_4	AB_3	AB_2	AB_1	AB_0		
0	1		AC_7	AC_6	AC	AC_4	AC_3	AC_2	AC_1	AC_0		
0	1		AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	AD_1	AD_0		
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY follow the reference code sequences
0	1		0	0	0	0	0	0	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option
0	1		A_7	A_6	A_5	A_4	0	0	A_1	A_0		

A[7:6]	Select VBD as
00	GS Transition, Defined in A[2] and A[1:0]
01	Fix Level, Defined in A[5:4]
10	VCOM
11[POR]	HiZ

A [5:4] Fix Level Setting for VBD

A[5:4]	VBD level
00	VSS
01	VSH1
10	VSL
11	VSH2

A [1:0] GS Transition setting for VBD
VBD Level Selection:
00b: VCOM ; 01b: VSH1;
10b: VSL; 11b: VSH2

A[1:0]	VBD Transition
00	LUT0
01	LUT1
10	LUT2
11	LUT3

0	0	3F	0	0	1	1	1	1	1	1	End Option (EOPT)	Option for LUT end Set this byte to 22h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26
0	1		0	0	0	0	0	0	0	A_0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 18h
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	B_5	B_4	B_3	B_2	B_1	B_0		

Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="5">Set Ram Y- address Start / End position</td><td rowspan="5">Specify the start/end positions of the window address in the Y direction by an address unit for RAM

A[8:0]: YSA[8:0], YStart, POR = 000h
B[8:0]: YEA[8:0], YEnd, POR = 17Fh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_8</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>46</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Auto Write RED RAM for Regular Pattern</td><td>Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR]

A[7]: The 1st step value, POR = 0
A[6:4]: Step Height, POR= 000
Step of alter RAM in Y-direction according to Gate
<table>
<tr><th>A[6:4]</th><th>Height</th><th>A[6:4]</th><th>Height</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>384</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr>
</table>
A[2:0]: Step Width for 168x384, POR= 000
Step of alter RAM in X-direction according to Source
<table>
<tr><th>A[2:0]</th><th>Width</th><th>A[2:0]</th><th>Width</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>168</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>NA</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr>
</table></td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		A[2:0]: Step Width for 184x384, POR= 000 Step of alter RAM in X-direction according to Source A[2:0] Width A[2:0] Width 000 8 100 128 001 16 101 184 010 32 110 NA 011 64 111 NA A[2:0]: Step Width for 200x384, POR= 000 Step of alter RAM in X-direction according to Source A[2:0] Width A[2:0] Width 000 8 100 128 001 16 101 200 010 32 110 NA 011 64 111 NA A[2:0]: Step Width for 216x384, POR= 000 Step of alter RAM in X-direction according to Source A[2:0] Width A[2:0] Width 000 8 100 128 001 16 101 216 010 32 110 NA 011 64 111 NA BUSY pad will output high during operation.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	0	A_2	A_1	A_0		

A[7]: The 1st step value, POR = 0
A[6:4]: Step Height, POR= 000
Step of alter RAM in Y-direction according to Gate

A[6:4]	Height	A[6:4]	Height
000	8	100	128
001	16	101	256
010	32	110	384
011	64	111	NA

A[2:0]: Step Width for 168x384, POR= 000
Step of alter RAM in X-direction according to Source

A[2:0]	Width	A[2:0]	Width
000	8	100	128
001	16	101	168
010	32	110	NA
011	64	111	NA

A[2:0]: Step Width for 184x384, POR= 000
Step of alter RAM in X-direction according to Source

A[2:0]	Width	A[2:0]	Width
000	8	100	128
001	16	101	184
010	32	110	NA
011	64	111	NA

A[2:0]: Step Width for 200x384, POR= 000
Step of alter RAM in X-direction according to Source

A[2:0]	Width	A[2:0]	Width
000	8	100	128
001	16	101	200
010	32	110	NA
011	64	111	NA

A[2:0]: Step Width for 216x384, POR= 000
Step of alter RAM in X-direction according to Source

A[2:0]	Width	A[2:0]	Width
000	8	100	128
001	16	101	216
010	32	110	NA
011	64	111	NA

During operation, BUSY pad will output high.

Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Frame Memory Write or Read Commands.

8 COMMAND DESCRIPTION

8.1 Driver Output Control (01h)

This triple byte command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		0	0	1	0	1	0	1	1
W	1								MUX8
POR									1
W	1						GD	SM	TB
POR							0	0	0

MUX[8:0]: Specify number of lines for the driver: MUX[8:0] + 1. Multiplex ratio (MUX ratio) from 16 MUX to 384MUX.

GD: Selects the 1st output Gate
This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

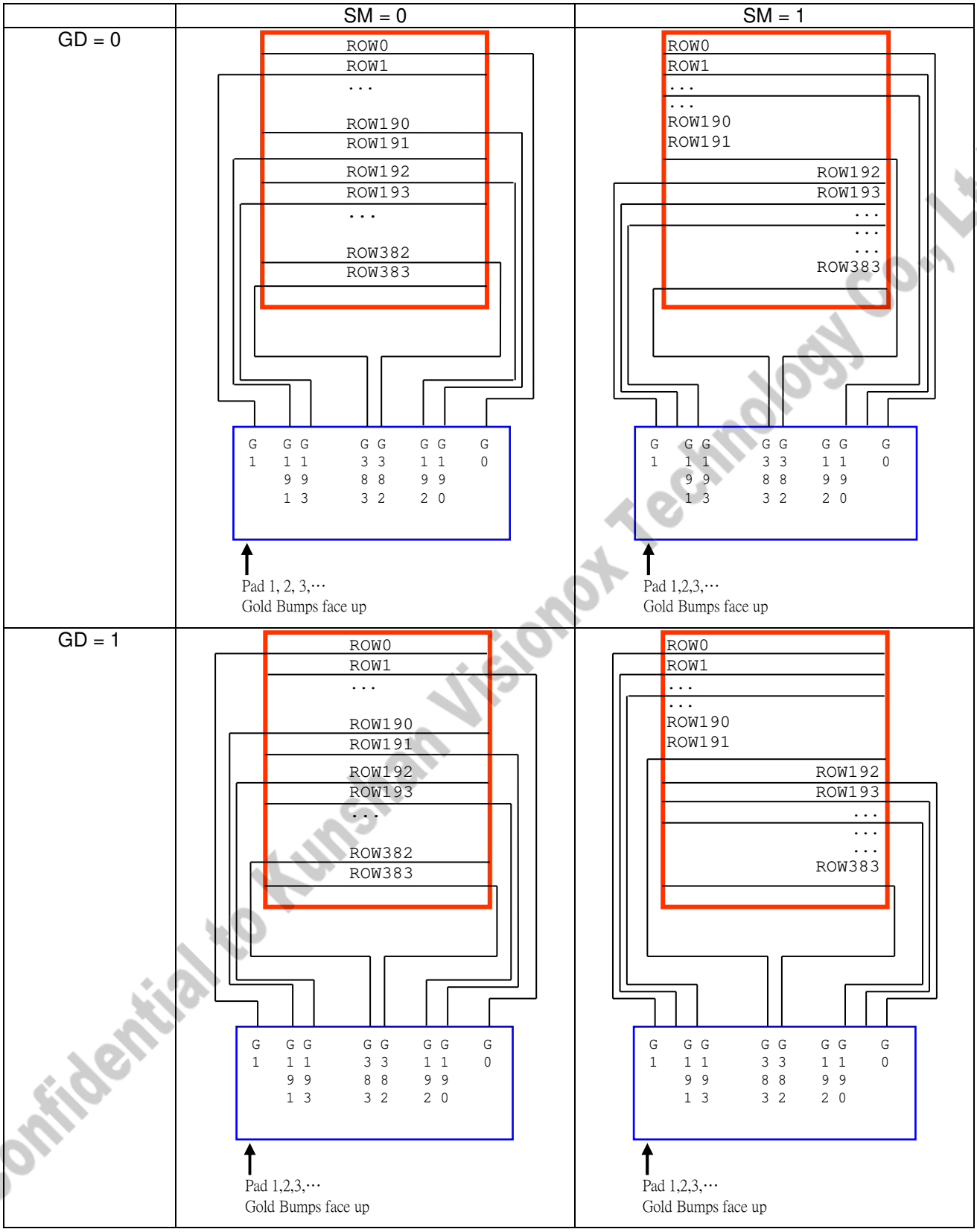
SM: Change scanning order of gate driver.
When SM is set to 0, left and right interlaced is performed.
When SM is set to 1, no splitting odd / even of the GATE signal is performed,
Output pin assignment sequence is shown as below (for 384 MUX ratio):

	SM=0	SM=0	SM=1	SM=1
Driver	GD=0	GD=1	GD=0	GD=1
G0	ROW0	ROW1	ROW0	ROW192
G1	ROW1	ROW0	ROW192	ROW0
G2	ROW2	ROW3	ROW1	ROW193
G3	ROW3	ROW2	ROW193	ROW1
:	:	:	:	:
G190	ROW190	ROW191	ROW95	ROW287
G191	ROW191	ROW190	ROW287	ROW95
G192	ROW192	ROW193	ROW96	ROW288
G193	ROW193	ROW192	ROW288	ROW96
:	:	:	:	:
G380	ROW380	ROW381	ROW190	ROW382
G381	ROW381	ROW380	ROW382	ROW190
G382	ROW382	ROW383	ROW191	ROW383
G383	ROW383	ROW382	ROW383	ROW191

See “Scan Mode Setting” on next page.

TB: Change scanning direction of gate driver.
This bit defines the scanning direction of the gate for flexible layout of signals in module either from up to down (TB = 0) or from bottom to up (TB = 1).

Figure 8-1: Output pin assignment on different Scan Mode Setting



8.2 Gate Scan Start Position (0Fh)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	SCN8
POR		0	0	0	0	0	0	0	0

This command is to set Gate Start Position for determining the starting gate of display RAM by selecting a value from 0 to 383. Figure 8-2 shows an example using this command of this command when MUX ratio= 384 and MUX ratio= 150 “ROW” means the graphic display data RAM row.

Figure 8-2: Example of Set Display Start Line with no Remapping

	MUX ratio (01h) = 17Fh	MUX ratio (01h) = 0C0h	MUX ratio (01h) = 0C0h
GATE Pin	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 05Dh
G0	ROW0	ROW0	-
G1	ROW1	ROW1	-
G2	ROW2	ROW2	-
G3	ROW3	ROW3	-
:	:	:	:
:	:	:	:
G91	:	:	-
G92	:	:	-
G93	:	:	ROW93
G94	:	:	ROW94
:	:	:	:
:	:	:	:
G190	ROW190	ROW190	:
G191	ROW191	ROW191	:
G192	ROW192	-	:
G193	ROW193	-	:
:	:	:	:
	:	:	:
G284	:	:	ROW284
G285	:	:	ROW285
G286	:	:	-
G287	:	:	-
	:	:	:
:	:	:	:
G380	ROW380	-	-
G381	ROW381	-	-
G382	ROW382	-	-
G383	ROW383	-	-
Display Example			

8.3 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	ID0
POR		0	0	0	0	0	0	1	1

ID[1:0]: The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = “01”. The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = “00”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = “0”, the address counter is updated in the X direction. When AM = “1”, the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

	ID [1:0]="00” X: decrement Y: decrement	ID [1:0]="01” X: increment Y: decrement	ID [1:0]="10” X: decrement Y: increment	ID [1:0]="11” X: increment Y: increment
AM="0” X-mode	00,00h … 31,12Bh	00,00h … 31,12Bh	00,00h … 31,12Bh	00,00h … 31,12Bh
AM="1” Y-mode	00,00h … 31,12Bh	00,00h … 31,12Bh	00,00h … 31,12Bh	00,00h … 31,12Bh

The pixel sequence is defined by the ID [0],

	ID[1:0]="00” X: decrement Y: decrement	ID[1:0]="01” X: increment Y: decrement
AM="0” X-mode	00,00h … 4, 3, 2, 1 … 31,12Bh	00,00h … 1, 2, 3, 4 … 31,12Bh

8.4 Set RAM X - Address Start / End Position (44h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1			XSA5	XSA4	XSA3	XSA2	XSA1	XSA0
POR		0	0	0	0	0	0	0	0
W	1			XEA5	XEA4	XEA3	XEA2	XEA1	XEA0
POR		0	0	1	1	0	0	0	1

XSA[5:0]/XEA[5:0]: Specify the start/end positions of the window address in the X direction by 8 times address unit. Data is written to the RAM within the area determined by the addresses specified by XSA [5:0] and XEA [5:0]. These addresses must be set before the RAM write.
It allows on XEA [5:0] ≤ XSA [5:0]. The settings follow the condition on 00h ≤ XSA [5:0], XEA [5:0] ≤ 31h. The windows is followed by the control setting of Data Entry Setting (R11h)

8.5 Set RAM Y - Address Start / End Position (45h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0
POR		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	YSA8
POR		0	0	0	0	0	0	0	0
W	1	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0
POR		0	0	1	0	1	0	1	1
W	1	0	0	0	0	0	0	0	YEA8
POR		0	0	0	0	0	0	0	1

YSA[8:0]/YEA[8:0]: Specify the start/end positions of the window address in the Y direction by an address unit. Data is written to the RAM within the area determined by the addresses specified by YSA [8:0] and YEA [8:0]. These addresses must be set before the RAM write.
It allows YEA [8:0] ≤ YSA [8:0]. The settings follow the condition on 00h ≤ YSA [8:0], YEA [8:0] ≤ 12Bh. The windows is followed by the control setting of Data Entry Setting (R11h)

8.6 Set RAM Address Counter (4Eh-4Fh)

Reg#	R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4Eh	W	1			XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0
	W	1								YAD8
	POR									0

XAD[5:0]: Make initial settings for the RAM X address in the address counter (AC).
YAD[8:0]: Make initial settings for the RAM Y address in the address counter (AC).

After RAM data is written, the address counter is automatically updated according to the settings with AM, ID bits and setting for a new RAM address is not required in the address counter. Therefore, data is written consecutively without setting an address. The address counter is not automatically updated when data is read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AM, ID[1:0]} ; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

9 Absolute Maximum Rating

Table 9-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +6.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} be constrained to the range $V_{SS} < V_{CI}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

10 Electrical Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25ºC.

Table 10-1: DC Characteristics

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V_{CI}	VCI operation voltage	VCI	-	2.2	3.0	3.7	V
V_{DD}	VDD operation voltage	VDD	-	1.7	1.8	1.9	V
V_{COM_DC}	VCOM_DC output voltage	VCOM	-	-3.0	-	-0.2	V
dV_{COM_DC}	VCOM_DC output voltage deviation	VCOM	-	-200	-	200	mV
V_{COM_AC}	VCOM_AC output voltage	VCOM	-	V_{SL} + V_{COM_DC}	V_{COM_DC}	V_{SH1}+ V_{COM_DC}	V
V_{GATE}	Gate output voltage	G0~G299	-	-20	-	+20	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage	G0~G299	-	-	-	40	V
V_{SH1}	Positive Source output voltage	VSH1	-	+8.8	+15	+17	V
dV_{SH1}	VSH1 output voltage deviation	VSH1	From 8.8V to 17V	-200	-	200	mV
V_{SH2}	Positive Source output voltage	VSH2	-	+2.4	+5	+17	V
dV_{SH2}	VSH2 output voltage deviation	VSH2	From 2.4V to 8.6V	-100	-	100	mV
			From 8.8V to 17V	-200	-	200	mV
V_{SL}	Negative Source output voltage	VSL	-	-17	-15	-8.6	V
dV_{SL}	VSL output voltage deviation	VSL	-	-200	-	200	mV
V_{IH}	High level input voltage	SDA, SCL, CS#, D/C#, RES#, BS1, M/S#, CL	-	0.8V_{DDIO}	-	-	V
V_{IL}	Low level input voltage		-	-	-	0.2V_{DDIO}	V
V_{OH}	High level output voltage	SDA, BUSY, CL	IOH = -100uA	0.9V_{DDIO}	-	-	V
V_{OL}	Low level output voltage		IOL = 100uA	-	-	0.1V_{DDIO}	V
V_{PP}	OTP Program voltage	VPP	-	7.25	7.5	7.75	V

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
Islp_VCI	Sleep mode current	VCI	- DC/DC off - No clock - No output load - MCU interface access - RAM data access	-	TBD	TBD	uA
Idslp_VCI1	Current of deep sleep mode 1	VCI	- DC/DC off - No clock - No output load - No MCU interface access - Retain RAM data but cannot access the RAM	-	TBD	TBD	uA
Idslp_VCI2	Current of deep sleep mode 2	VCI	- DC/DC off - No clock - No output load - No MCU interface access - Cannot retain RAM data	-	TBD	TBD	uA
Iopr_VCI	Operating Mode current	VCI	VCI=3.0V	-	TBD	-	uA
V_{GH}	Operating Mode Output Voltage	VGH	Enable Clock and Analog by Master Activation Command VGH=20V VGL=-VGH VSH1=15V VSH2=5V VSL=-15V VCOM = -2V No waveform transitions. No loading. No RAM read/write No OTP read /write	19.5	20	20.5	V
V_{SH1}		VSH1		14.8	15	15.2	V
V_{SH2}		VSH2		4.9	5	5.1	V
V_{SL}		VSL		-15.2	-15	-14.8	V
V_{COM}		VCOM		-2.2	-2	-1.8	V

Table 10-2: Regulators Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
IVSH	VSH1 current	VSH1 = +15V	VSH1	-	-	TBD	uA
IVSH1	VSH2 current	VSH2 = +5V	VSH2	-	-	TBD	uA
IVSL	VSL current	VSL = -15V	VSL	-	-	TBD	uA
IVCOM	VCOM current	VCOM = -2V	VCOM	-	-	TBD	uA

11 AC Characteristics

11.1 Serial Peripheral Interface

The following specifications apply for: VDDIO - VSS = 2.2V to 3.7V, T_{OPR} = 25°C, CL=20pF

Table 11-1 : Serial Peripheral Interface Timing Characteristics

Write mode

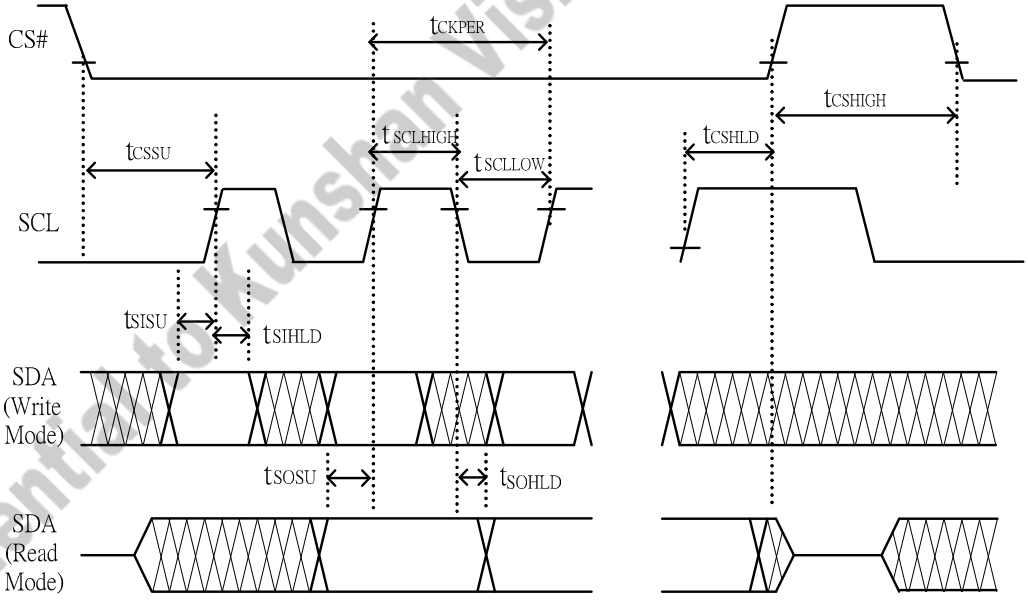
Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Write Mode)	-	-	20	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	TBD	-	-	ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	TBD	-	-	ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	TBD	-	-	ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	TBD	-	-	ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	TBD	-	-	ns
t_{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	TBD	-	-	ns
t_{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	TBD	-	-	ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Read Mode)	-	-	2.5	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	TBD	-	-	ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	TBD	-	-	ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	TBD	-	-	ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	TBD	-	-	ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	TBD	-	-	ns
t_{SOSU}	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL	TBD	TBD	-	ns
t_{SOHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL	TBD	TBD	-	ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

Figure 11-1: SPI timing diagram



12 Application Circuit

Figure 12-1: Schematic of SSD1685 application circuit

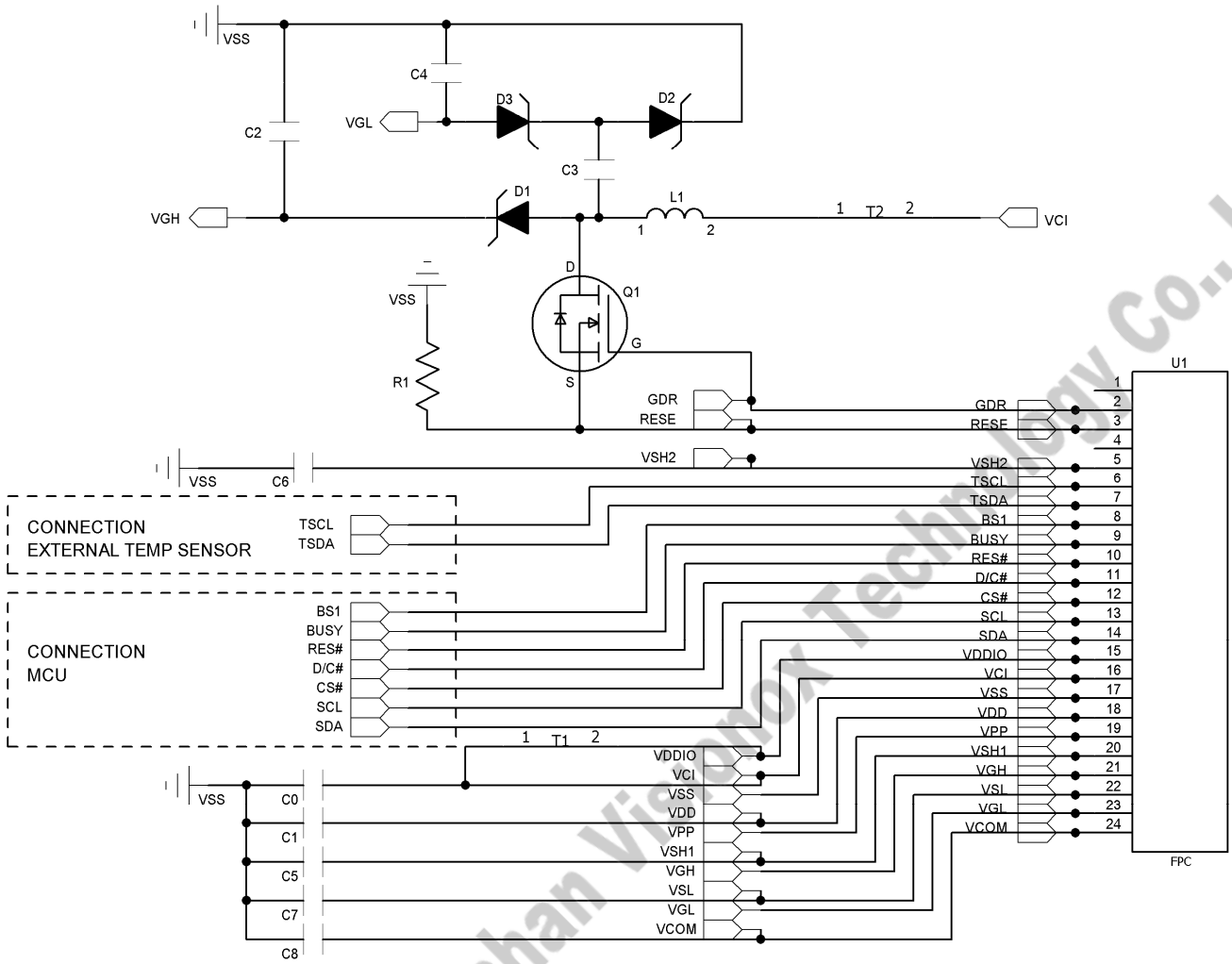


Table 12-1: Component list for SSD1685 application circuit

Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	1uF	0402/0603/0805; X7R; Voltage Rating : 25V
R1	2.2 ohm	0402/0603/0805; 1% variation, ≥ 0.05W
D1-D3	Diode	MBR0530 1) Reverse DC voltage ≥ 30V 2) Io ≥ 500mA 3) Forward voltage ≤ 430mV
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≥ 30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47uH	CDRH2D18 / LDNP-470NC Io= 500mA (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

Remarks:

1) The recommended component value and reference part in Table 14-1 is subject to change depending on panel loading.
2) Customer is required to review if the selected component value and part is suitable for their application.

The product(s) listed in this datasheet comply with Directive (EU) 2015/863 of 31 March 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

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