5T SRAM-AREA OPTIMIZATION

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ABSTRACT:

Area plays an important role in memory applications. So optimization of area needs to be done for higher packaging density, So our aim is to modify 6T SRAM(High performance) using 5T-SRAM without much effect on performance.

ORIGIN OF THE PROBLEM:

In order to perform more in-memory computations higher storage density is required, this happens through area optimization, this leads to 5T SRAM cell from 6T-SRAM cell.

RELEVANCE IN AREA OF NEUROMORPHIC/MEMORY:

SRAM cell is widely used in memory devices and applications for bit storage and they are used on integration on chip and used in cache memories(related in area of memory).

METHODOLOGY FOLLOWED OR OPERATED:

In this project we have performed operations of 6T and 5T SRAM cell.

Generally for 6T-SRAM Cell if (c and cb are 0 and 1) for read operation we precharge BL and BLbar to Vdd and give access transistors word line ON and sense amplifier is enabled. There is a differential voltage in one of the bitlines which will be detected by sense amplifier.

For write operation (c=0 and cb=1) bit line and bitline bar are precharged to Vdd and 0 respectively, word line is enabled and data is written to storage nodes.

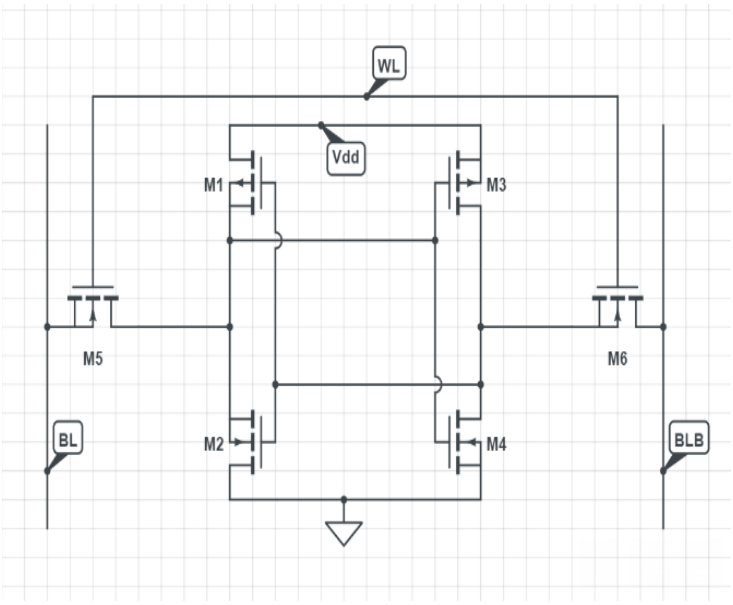


Fig: Schematic of 6T SRAM Cell

OPERATION OF 5T-SRAM:

In 5T-SRAM , Let us consider c=1 and cb=0; and for write 1, transistor M8 will be on and as c=1 and cb=0,M1 and M4 are on and as write 0 is off there is no discharge path from blr to write0;and source and drain of axs are connected at different potential so the charges flow from high to low and reaches a common voltage x; so now c and cb reaches a common voltage x and so all the transistors are on(M1,M2,M3,M4). But c has extra discharge path through bitline so it reaches 0 faster and due to butterfly regenerative cb reaches 1 so 1 is written in cb, similarly for write 0.

For read operation Only axs signal is activated and let c=0 and cb=1; then m3 and m2 are on there is path flow from one of the bitlines to ground which create a differential voltage. Here change in bit line voltage will be sensed by sense amplifier.

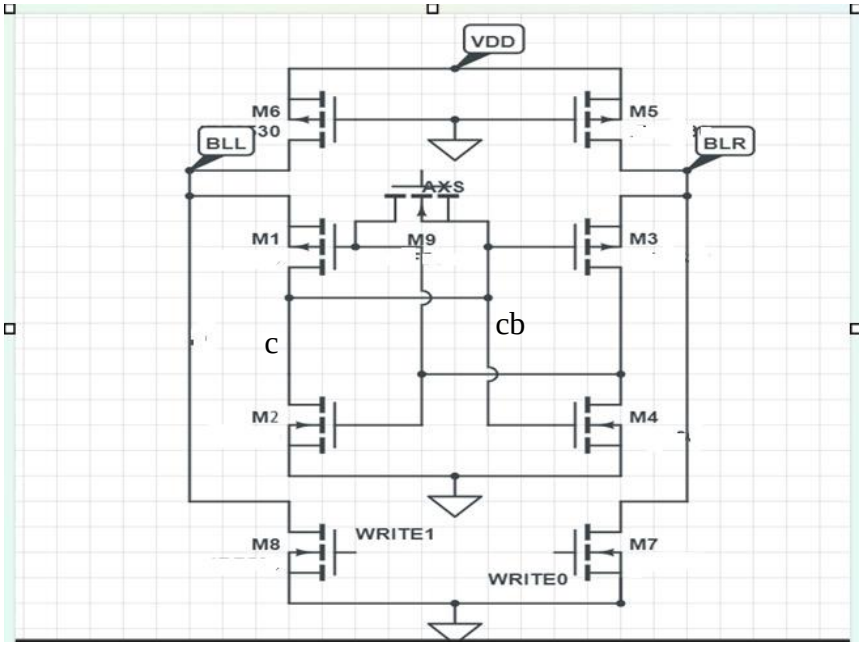
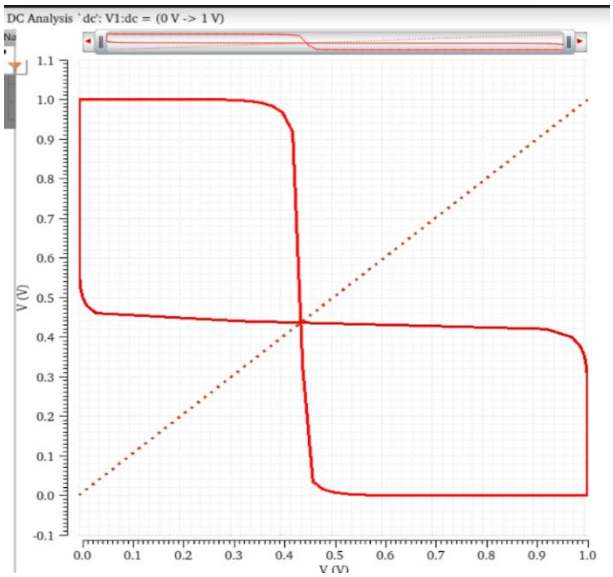
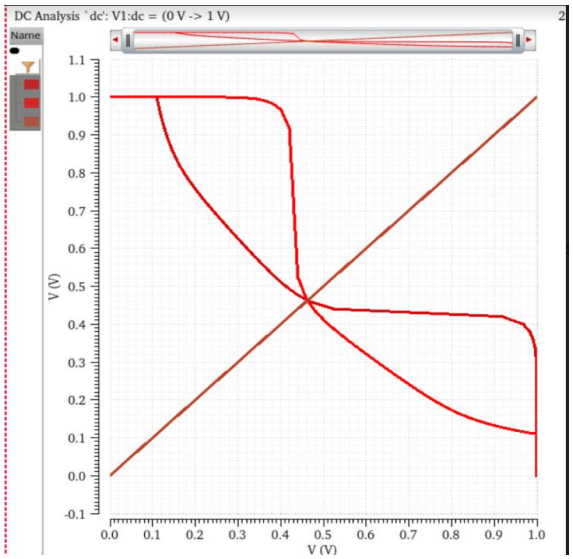


Fig: Schematic of 5T-SRAM Cell

RESULTS:

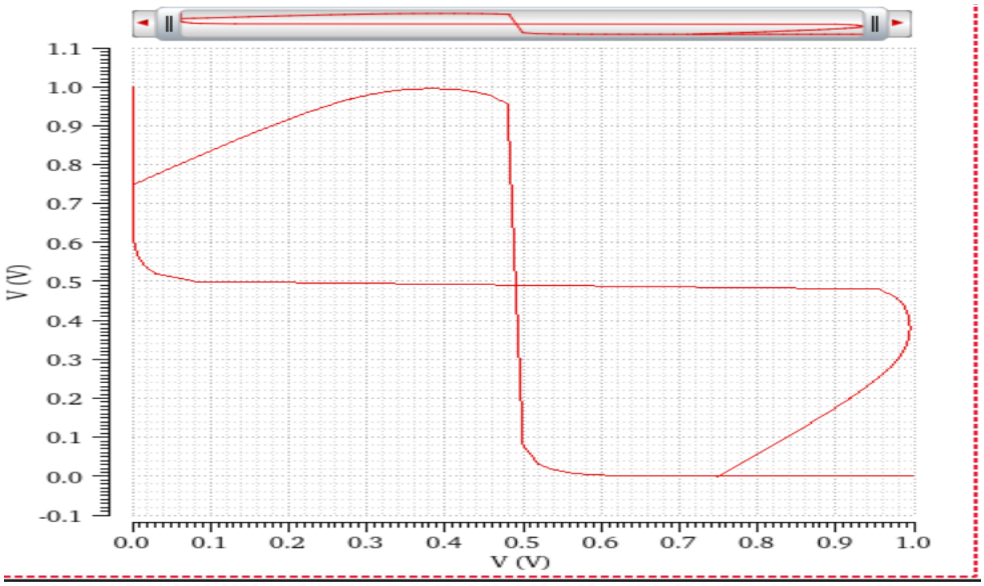
6T-SRAM HOLD AND READ SNM:



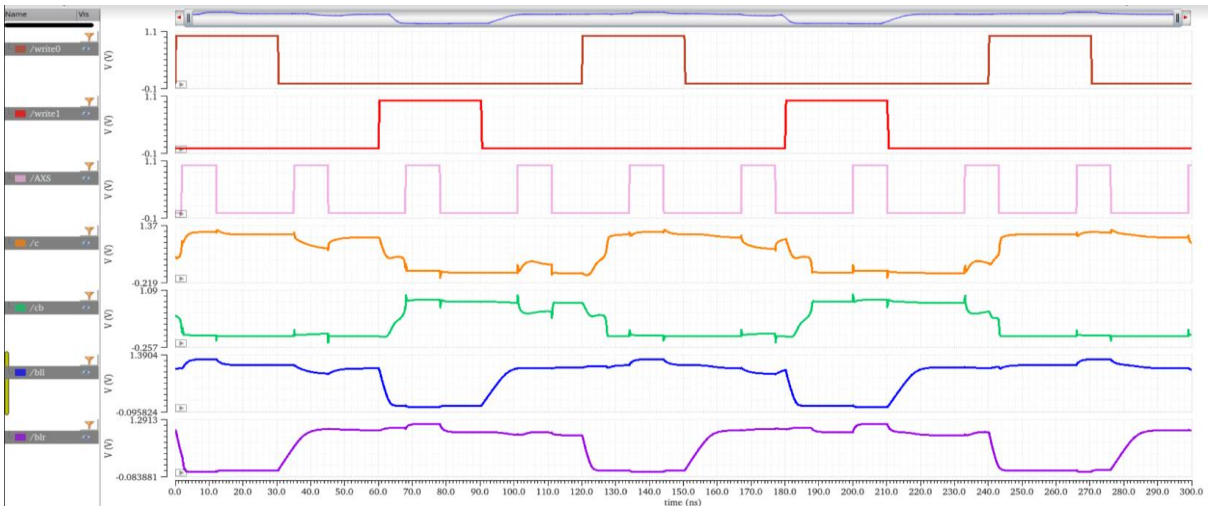


6T-SRAM HOLD 6T-SRAM READ

5T-SRAM HOLD AND READ SNM:

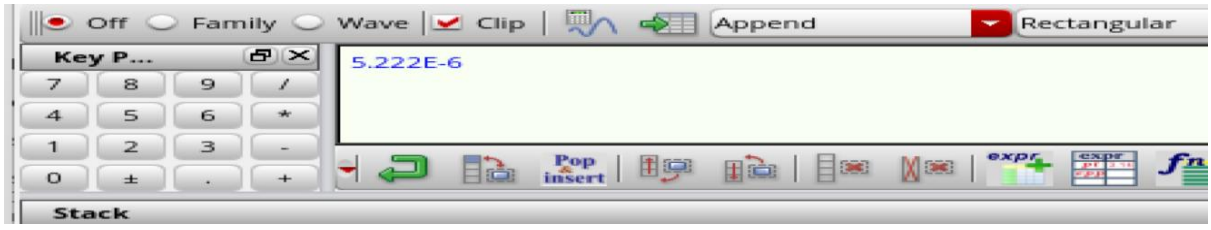


5T-READ AND WRITE:

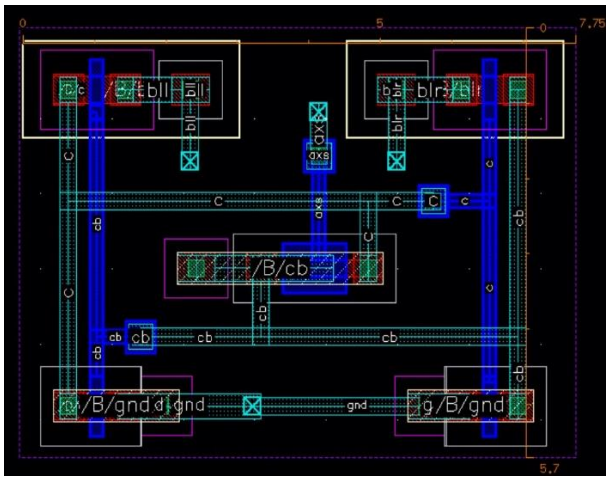


STATIC POWER DISSIPATION:5T-SRAM:

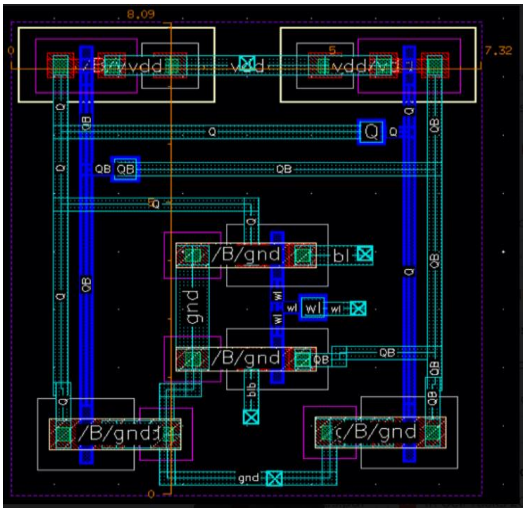
STATIC POWER DISSIPATION:6T-SRAM:



LAYOUT:



5T-SRAM



6T-SRAM

CONCLUSIONS:

	6T-SRAM	5T-SRAM
STATIC POWER	5.22 micro watts	4.11 micro watts
AREA	60.49um^2	44.46 um^2

As we can observe from above layouts,Area of 5T SRAM is decreased by 26% when compared with standard 6TSRAM.In our observation there is a slight issue in read operation

REFERENCES

1) Area Compact 5T Portless SRAM cell for High Density Cache in 65nm CMOS-Jitendra Kumar Yadav ,Pallavi Das ,Abhinav Jain , Anuj Grover
2) I. Carlson, S. Andersson, S. Natarajan, and A. Alvandpour, “A high density, low leakage, 5t sram for embedded caches,” in Solid-State Circuits Conference, 2004. ESSCIRC 2004.