# CYT62726

16-BIT CONSTANT CURRENT LED DRIVER

General Description

The CYT62726 is a 16 bits constant current LED driver with very low dropout voltage (less than 300mV at 90mA) for LED display. The constant current can be set between 4mA to 90mA by an external resistor. The CYT62726 consists of a 16-bits serial-in parallel-out shift register, a 16-bits latch, 16 low dropout constant current generators and a current setting circuits.
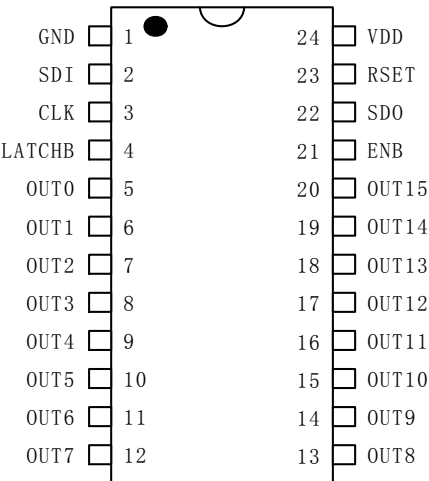
Features

- 16 constant current output channels
- Output current: 4mA-90mA
- Low dropout voltage: 300mV at 90mA
- Small propagation delay: 90ps from CLK to output current
- Adjustable output current through external resistor
- Up to 25 MHz clock frequency
- Very accurate output current:
- RoHS Compliant and 100% Lead (Pb)-Free

|	Current Accuracy
Between Bits	±3%
Between Chips	±5%

Pin Assignment

GND	1	24	VDD
SDI	2	23	RSET
CLK	3	22	SDO
LATCHB	4	21	ENB
OUT0	5	20	OUT15
OUT1	6	19	OUT14
OUT2	7	18	OUT13
OUT3	8	17	OUT12
OUT4	9	16	OUT11
OUT5	10	15	OUT10
OUT6	11	14	OUT9
OUT7	12	13	OUT8

Order Information

Part Number	Package Type
CYT62726SP	SDIP24
CYT62726SO	SOP24
CYT62726SS	SSOP24

Typical Output Current Performance

VOUT vs IOUT
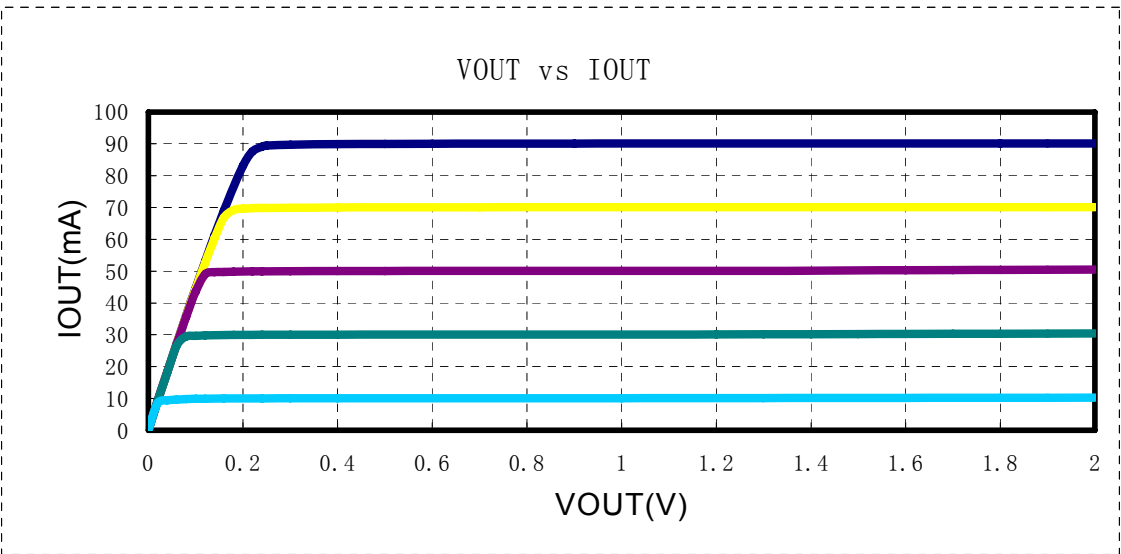
Block Diagram
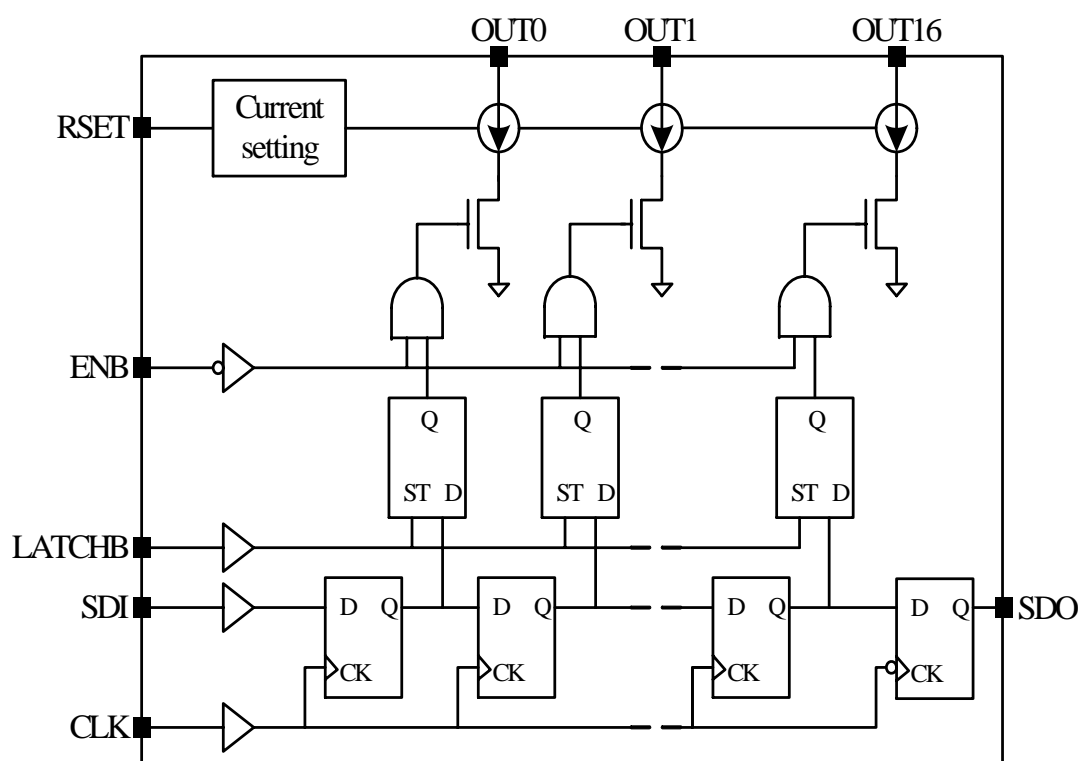
Pin Description

| Pin Number	Pin Name	Name and function
1	GND	GND terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LATCHB	Latch input terminal (active low)
5-20	OUT0-15	Constant current output terminal
21	ENB	Input terminal of output enable(active low)
22	SDO	Serial data output terminal
23	RSET	Current setting terminal, an external resistor is connected between RSET and GND to set the output current.
24	VDD	Supply voltage terminal

Equivalent Circuit of Inputs and Outputs
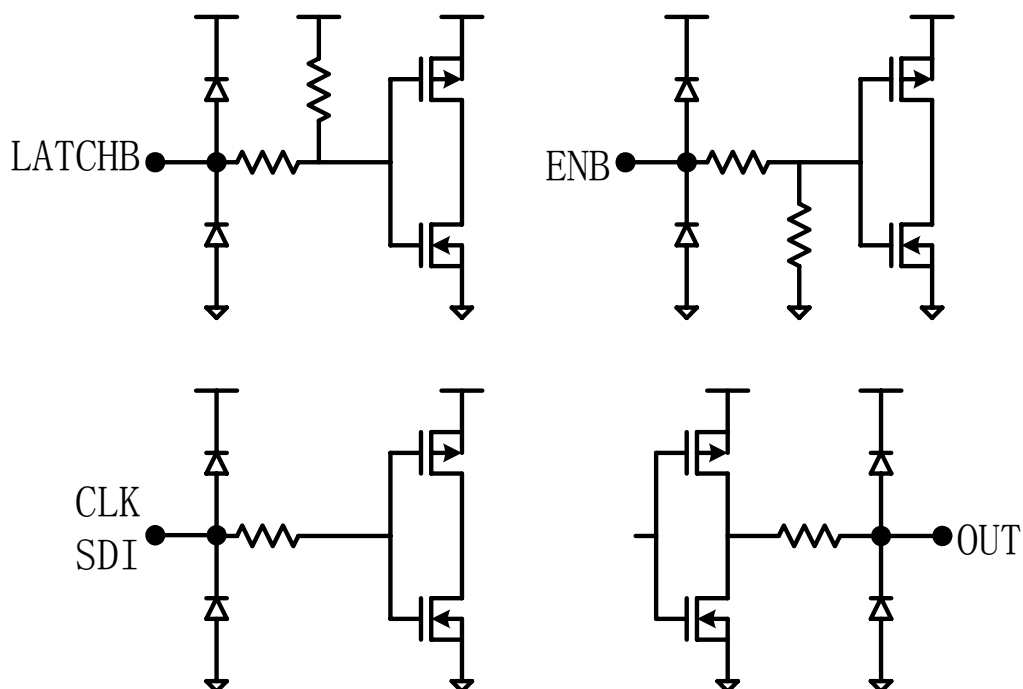
Truth Table

CLK	LATCHB	ENB	SDI	$\overline{OUT0}\ldots\overline{OUT7}\ldots\overline{OUT15}$	SDO
⌐⌐⌐	H	L	D_n	$D_n\ldots D_{n-7}\ldots D_{n-15}$	D_{n-15}
⌐⌐⌐	L	L	D_{n+1}	No change	D_{n-14}
⌐⌐⌐	H	L	D_{n+2}	$D_{n+2}\ldots D_{n-5}\ldots D_{n-13}$	D_{n-13}
⌐⌐⌐	X	L	D_{n+3}	$D_{n+2}\ldots D_{n-5}\ldots D_{n-13}$	D_{n-13}
⌐⌐⌐	X	H	D_{n+3}	off	D_{n-13}

Note: OUT0 to OUT15 = ON when Dn = H; OUT0 to OUT15 = OFF when Dn = L.

Timing Diagram
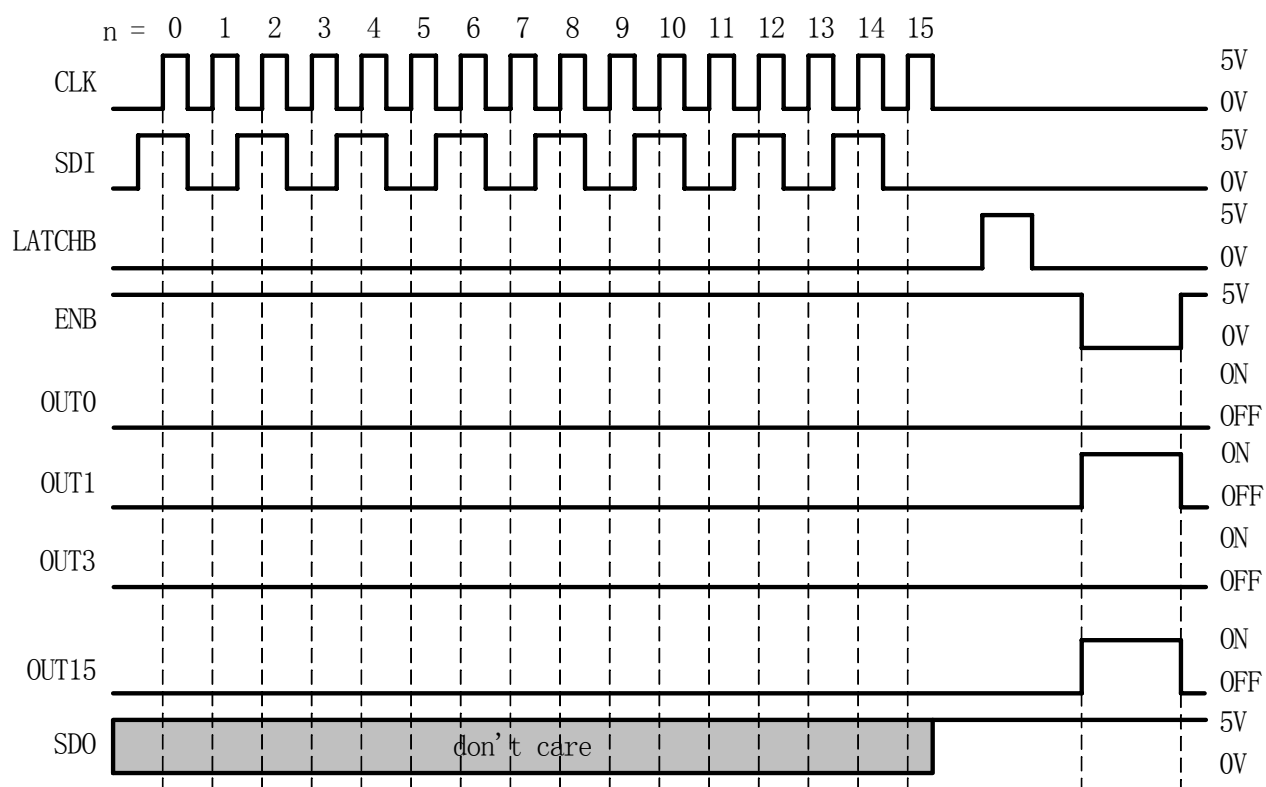
Note: The latches circuit holds data when the LATCHB terminal is Low. When the LATCHB terminal is at High level, latch circuit doesn't hold the data, it passes from the input to the output. When the ENB terminal is at Low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF. When the ENB terminal is at High level, it switches off all the data on the output terminal.

Maximum Rating

Stressing the device above the rating listed in the below table may cause permanent damage to the device.

Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Symbol	Parameter	value	unit
VDD	Supply voltage	7	V
V_O	Output voltage on OUTn	-0.5 ~ 10	V
I_O	Output current on OUTn	150	mA
VI	Input voltage	-0.4 ~VDD+0.4	V
I_{GND}	GND terminal current	1500	mA
f_{CLK}	Clock frequency	50	MHz
T_{OPR}	Operating temperature range	-40 ~ +125	℃
T_{STG}	Storage temperature range	-65 ~ +150	℃
V_{ESD}	ESD voltage for human body mode	2000	V

Recommended Operating Conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VDD	Supply voltage		4	5	5.5	V
V_O	Output voltage on OUTn				10	V
I_O	Output current on OUTn		4		90	mA
I_{OH}	Output current on SDO	SDO=VDD		10		mA
I_{OL}	Output current on SDO	SDO=0		-10		mA
V_{IH}	High level input voltage		0.7VDD		VDD+0.3	V
V_{IL}	Low level input voltage		-0.3		0.3VDD	V
tw(L)	LATCHB pulse width	VDD = 4 to 5V	20			ns
tw(CLK)	CLK pulse width		20			ns
tw(ENB)	ENB pulse width		200			ns
tsu(D)	Setup time for DATA		5			ns
th(D)	Holdtime for DATA		10			ns
tsu (L)	Setup time for LATCH		5			ns
th (L)	Hold time for LATCH		5			ns
f_{CLK}	Clock frequency	Cascade Operation (1)			25	MHz

Note: If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please consider the timings carefully.

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output leakage current	VOH = 16V				uA
V_{OL}	Output Voltage(Serial-OUT)	IOL = 1mA				V
V_{OH}	Output Voltage (Serial-OUT)	IOH= -1mA				V
I_{OL1}	Output Current	VO $\geq$0.4V REXT = 490Ω		40.11		mA
I_{OL2}		VO $\geq$0.32 V REXT = 245Ω		80.17		mA
ΔI_{OL1}	Output Current Error between bits	VO =1V REXT =490Ω.		0		%
ΔI_{OL2}		VO = 0.7V REXT = 245Ω		0		%
$R_{IN(up)}$	Pull-up Resistor	EN terminal		250		KΩ
$R_{IN(down)}$	Pull-down Resistor	LATCH terminal		250		KΩ
$IDD_{(OFF1)}$	Supply Current (OFF)	REXT=OPEN OUT 0 to 15 = OFF		1.2		mA
$IDD_{(OFF2)}$		REXT=490Ω OUT 0 to 15 = OFF		8		mA
$IDD_{(OFF3)}$		REXT=245Ω OUT 0 to 15 = OFF		15		mA

IDD$_{(ON1)}$		Supply Current (ON) REXT=490Ω OUT 0 to 15 = ON		8	mA
IDD$_{(ON2)}$		REXT=245Ω OUT 0 to 15 = ON		15	mA

Test Circuit for Electrical Characteristics

$VDD=V_{IH} =3.3V$
$V_{IL} =0V$
$t_r =t_f =10ns$
$(10\% \text{ to } 90\%)$
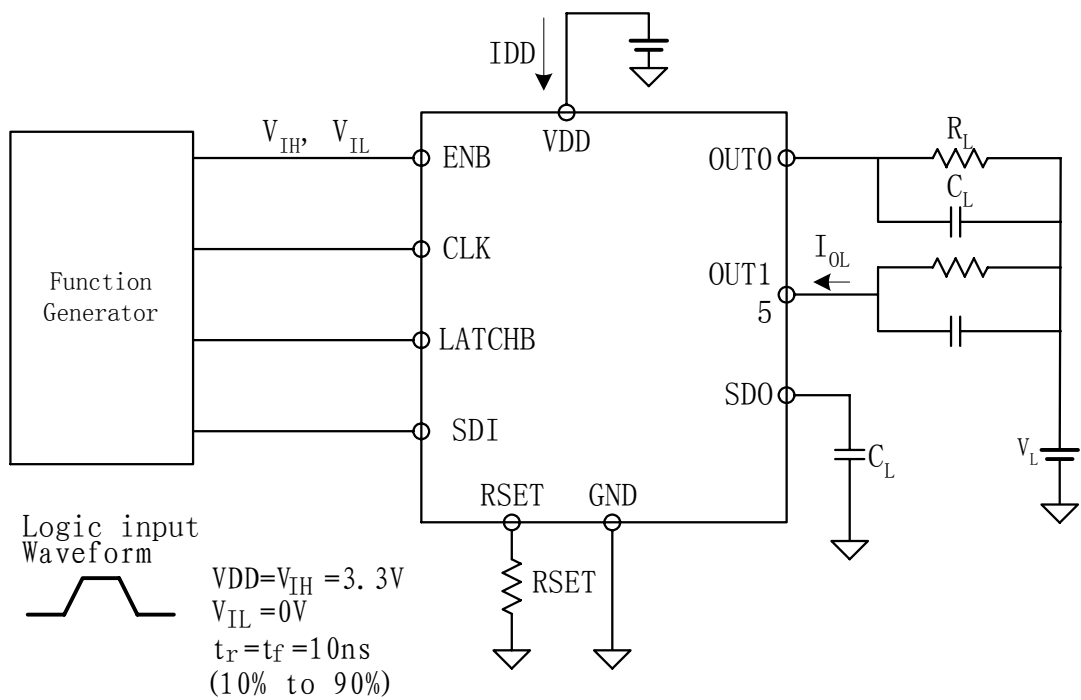
Switching Characteristics

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit
t$_{PLH1}$	OUTn current from "L" to "H" propagation delay time	CLK to OUTn	VDD =5V		67		ns
t$_{PLH2}$		LATCHB to OUTn	V$_{IH}$ = VDD		64		ns
t$_{PLH3}$		ENB to OUTn	V$_{IL}$ = GND		64		ns
t$_{PLH}$	propagation delay time	CLK to SDO	C$_L$ = 10pF I$_O$ = 40mA		5		ns

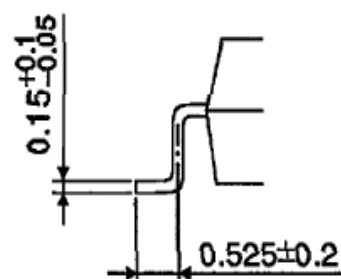|							
t_{PHL1}	OUTn current from "H" to "L" propagation delay time	CLK to OUTn	$V_L = 4V$ RSET=450 Ω $R_L = 75Ω$		5		ns
t_{PHL2}		LATCHB to OUTn			4		ns
t_{PHL3}		ENB to OUTn			4		ns
t_{PHL}	Propagation delay time	CLK to SDO			5		ns
t_{or}	Output current rise time				84		ns
t_{of}	Output current fall time				3		ns

Timing Waveform
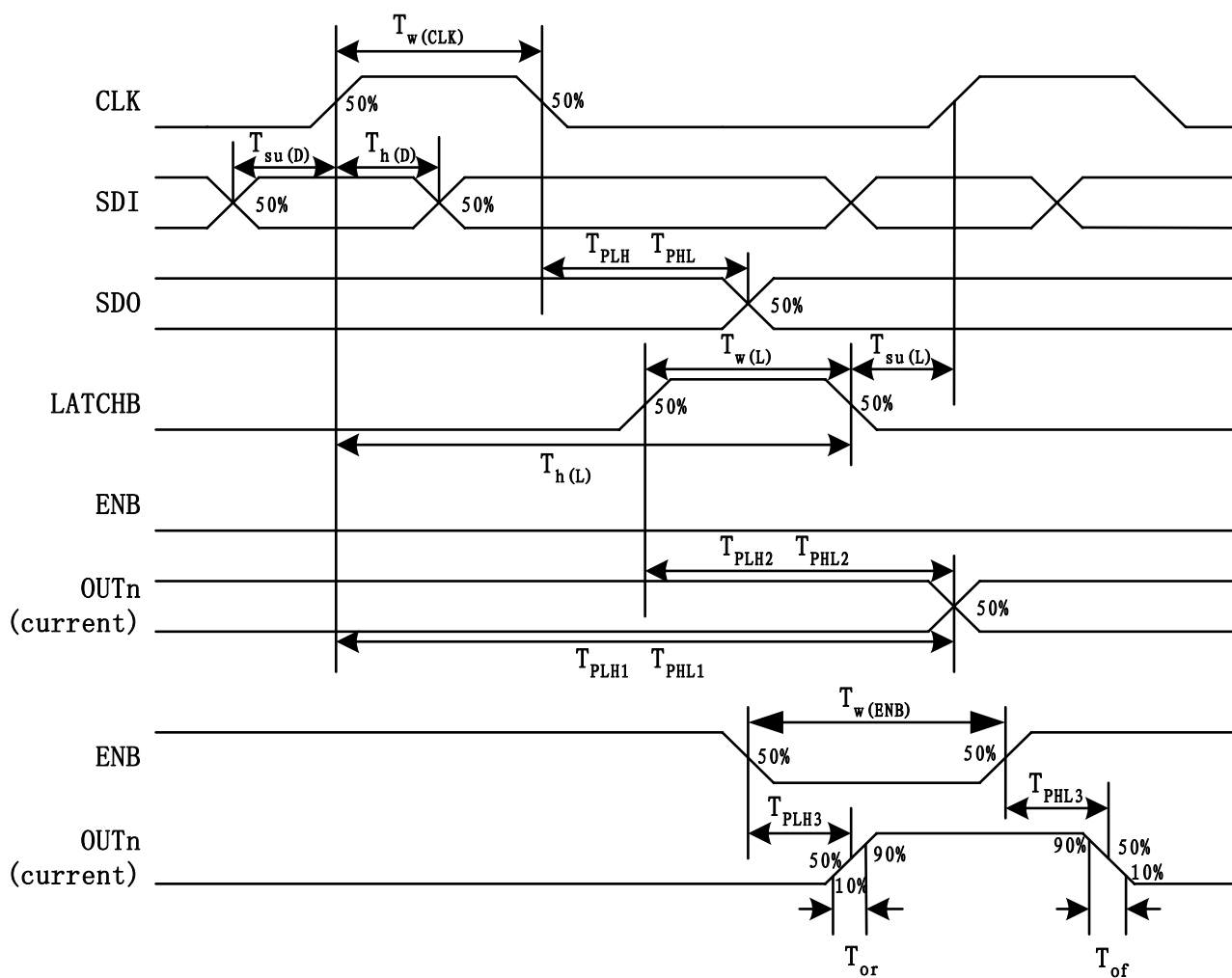
Output Current Setting

The output current is set by the external resistor RSET. The output current is 17.16/RSET.

IOUT VS. RSET (IOUT=17.16/RSET)
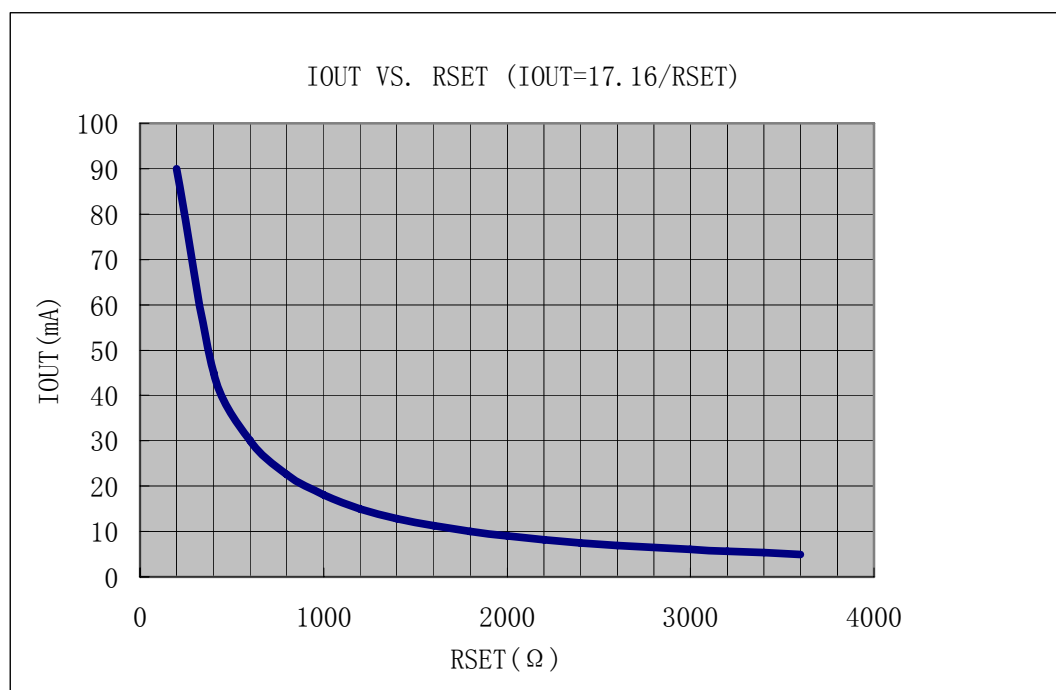
Package Information

SSOP24-P-300-1.00   Unit : mm
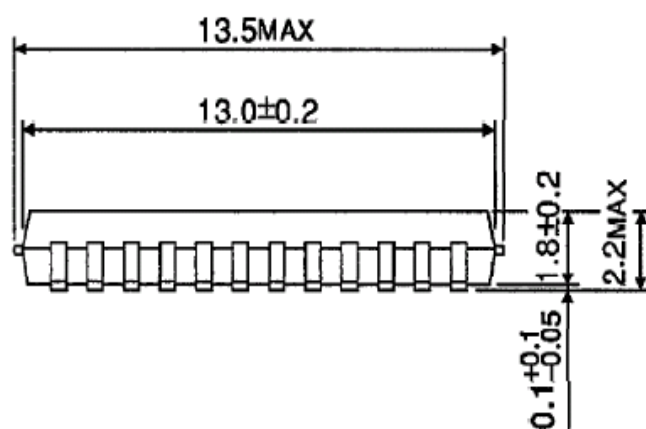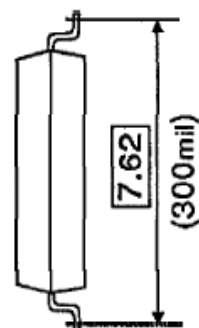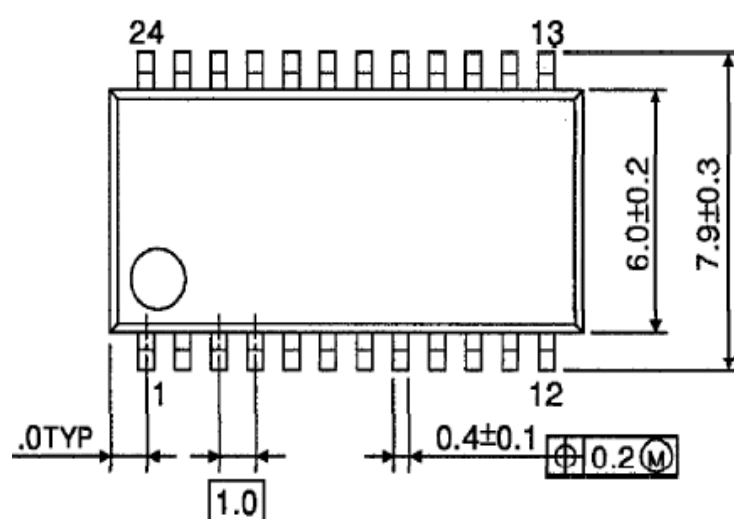
SSOP24-P-300-0.65A

Unit : mm

SOP24-P-450-1.27A   Unit : mm

24   13

8.8±0.2
11.8±0.3

11.43
(450mil)

1   12

015TYP   0.43±0.1   ⊕ 0.25 Ⓜ

1.27

16.5MAX

16.0±0.2

2.0±0.2
2.3MAX

▱ 0.1

0.1 +0.1 -0.05

0.15 +0.1 -0.05

1.0±0.2

SOP24-P-450-1.27B

Unit : mm

24   13

8.8±0.2

11.93±0.3

1   12

015TYP

0.4±0.1

1.27

11.43

(450mil)

16.5MAX

16.0±0.2

2.4±0.2

2.8MAX

0.19±0.1

0.1

0.15 +0.1 -0.05

0.8±0.2

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