

GOOGLE'S RANDOM VIBRATION TESTING METHODOLOGY, A HIGH LEVEL OVERVIEW

Part 4: COMPONENT LEVEL MEASUREMENT AND ANALYSIS REVISION A

By Ken K.H. Leung

Email: openrandomvibe@ocproject.net

What happens to critical components when it is subjected to sine and random vibration?

Factors that contribute toward localized component level stress
and failure modes in a fully populated rack

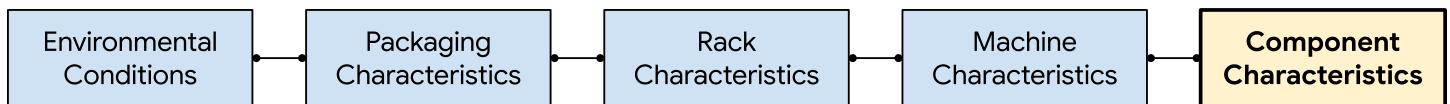


Figure 1.

As we turn our attention toward critical components inside the machines, we leave behind macro vibration behaviors (large mass moving on spring, like a machine sitting on foam packaging) and switch gears toward component specific (micro) vibration behaviors. The IPC/JEDEC and Intel guidelines are great explanation of such perspectives:

1. The IPC/JEDEC-9703 standard: MECHANICAL SHOCK TEST GUIDELINE FOR SOLDER JOINT RELIABILITY [1]
2. Intel's Strain Measurement Methodology for Circuit Board Assembly - Board Flexure Initiative (BFI) [2]

These guidelines are written for chip packages and BGA solder joints, but the methods are applicable to all electronic components. The idea is simple - subject circuit boards to high amplitude shock impacts, monitor local strain at corners of chip packages (where BGA solder joint damages are most likely to occur), and establish a correlation between strain and damage. The solder joints aren't mass/spring systems themselves. Instead, they represent stress concentration as the result of displacement of the larger mass/spring system (heatsink & circuit board, chassis & packaging, etc).

The guidelines are quite involved, and described a series of activities from start to finish:

1. Prepare test sample for shock testing (design, fabrication, and fixturing)
2. Apply rosette strain gauges around component(s) of interest
3. Monitor strain with high speed data acquisition devices (up to 100khz per channel)
4. Test sample with half sine high G shock (between 200G to 340G)

5. Measure resistance through the circuitry before, during, and after testing (if applicable)
6. Apply failure analysis techniques such as dye and pry, X-ray, or cross sectioning to assess level of mechanical damage
7. Correlate measured strain values and failure analysis results with FEA simulations.
8. Use FEA simulations and strain measurements to predict future failures

IPC/JEDEC-9703 & 9704A Guidelines

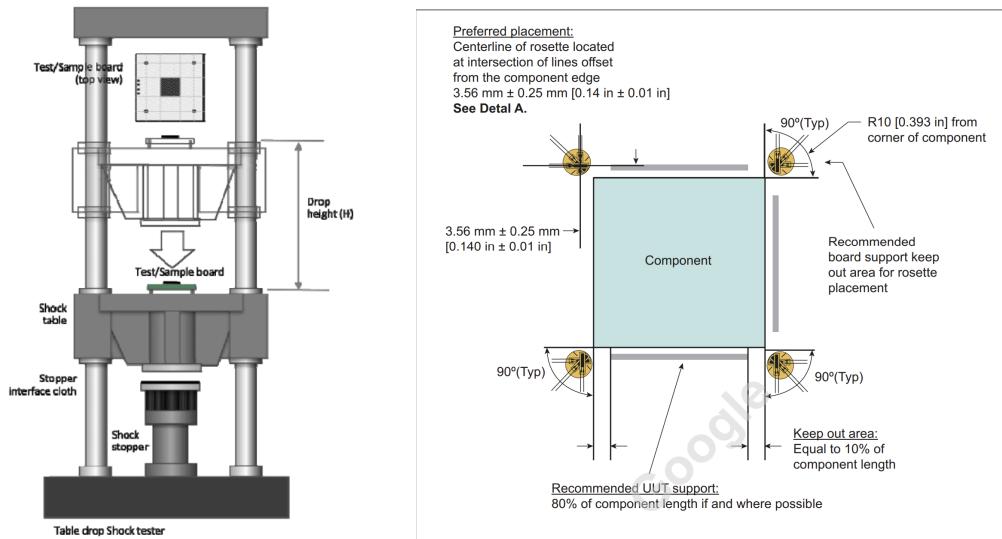


Figure 1 &2.

IPC/JEDEC-9703 & 9704A Guidelines

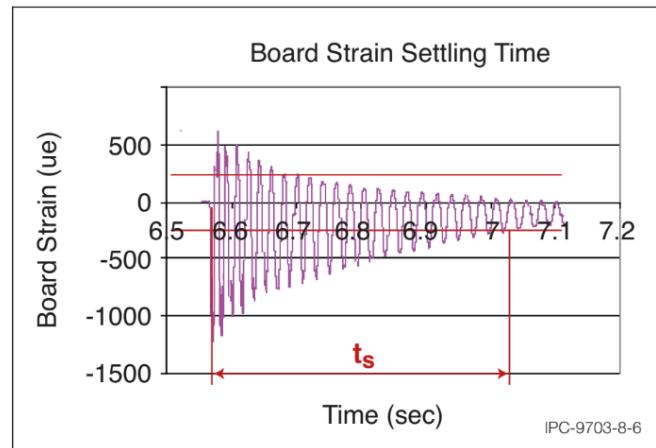
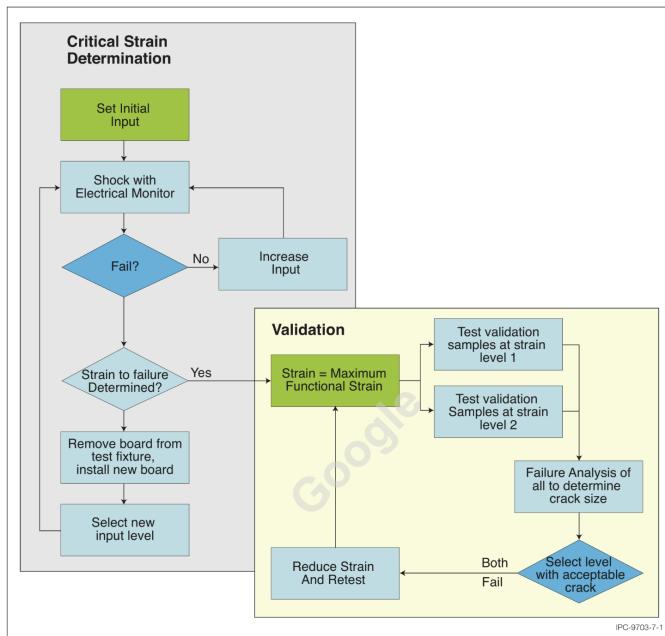


Figure 8-6 Typical Time History for a Component Board Test with Minimal Damping

Figure 3 & 4.

These methods are used by a large number of organizations and companies (many of which contributed toward the establishment of the methods in the first place) for product development, but their adoption continues to be a challenge, limited by factors such as:

1. The workflow is complex and require an investment into capital equipments and field expertise
2. 200G 2ms shock is perceived to be “harsh” (this is not necessarily true - a future paper will do a direct comparison with 30G 11ms, which is more common in packaging scenarios)
3. Different components have different failure modes, which makes the method difficult to scale across an industry full of unique critical components

Harsher conditions lead to more strain, which leads to more stress. However, no specific number can definitively predict damages across different product designs and critical components, especially when technology and materials continue to evolve. We will continue to re-examine this hypothesis as the project progresses forward. For now, we will keep it in mind as we develop more tools to help understand the big picture.

Deformation and strain monitoring during vibration testing

Let's go back to our Lenovo ThinkSystem SR650 V2 test sample. We apply a sine dwell of the first natural frequency with the unit mounted directly on the shaker table, only this time, we measure corners of the CPUs just like the IPC/JEDEC guidelines.

Equipment	Specifications
High Speed Camera: Duo Phantom v2640	4000 frames per second, 0.2 second duration, 2048 x 1536 resolution, 2.74 Gb captured
Calibration Target: Zeiss Calibration Object	CP20 Panel / CP20/350, 20.5" x 18.5"
Software: Zeiss Inspect Correlate	Profile: Sine Dwell @ 30hz, 60hz, 129hz & 2.0G
Setup Time: 3 hours	

Table 1.

There is a reason why we continue to come back to optical measurements - in addition to 3D deformation, calibrated stereo high speed video footage allows us to measure board strain over a large area. We picked a view with sufficient resolution to measure local strain at the corners of the CPUs, and large enough to see the overall board deflection. This allows us to monitor board and micro dynamic behaviors of the CPUs/Heatsinks/PCB at the same time, as well as any other components within the field of view.

Lenovo ThinkSystem SR650 V2 mounted on shaker table, zoom into the center CPU/Heatsink area

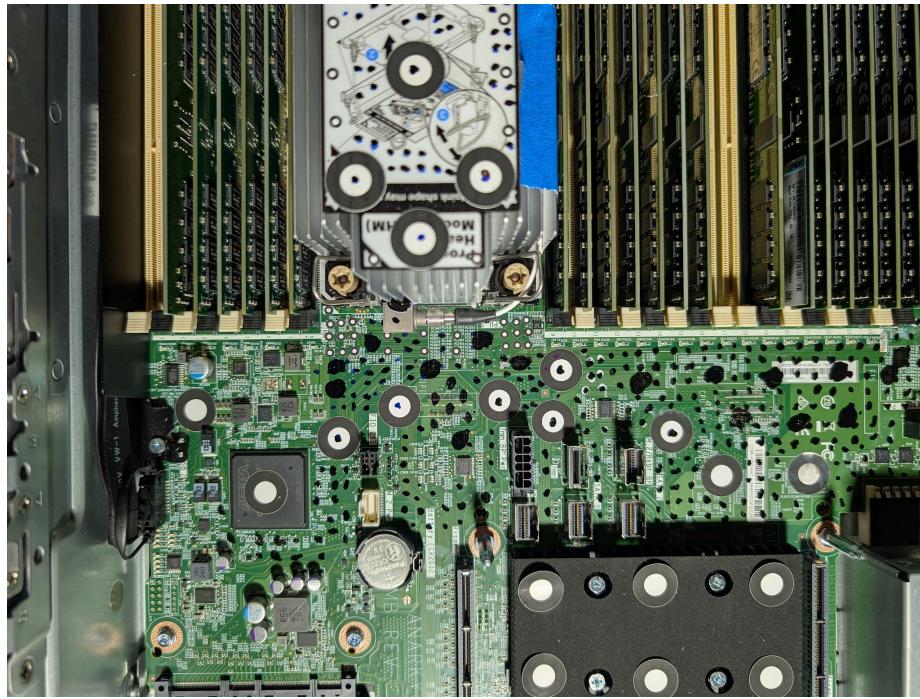


Figure 5.

We place a number of markers at the corners of the CPUs. Once absolute coordinates are calculated, they can be used to calculate microstrain (ummm/mm) at these locations. We will focus on CPU0 (left) this time.

Lenovo Lenovo SR650 V2, snapshot from Zeiss Inspect Correlate with absolute displacement measurements of CPU0, Sine Dwell, 30hz, 2.0G

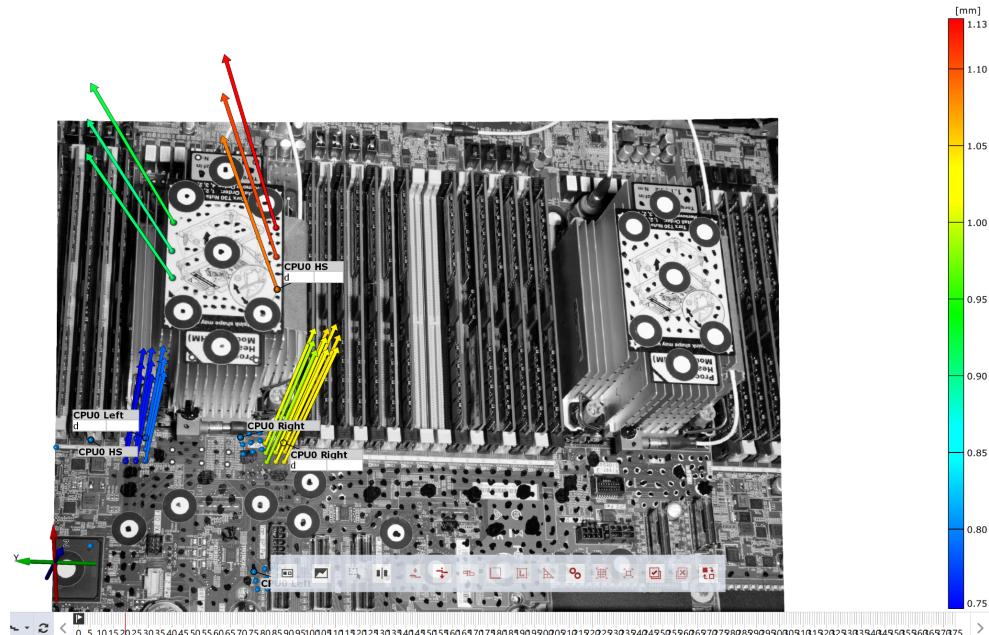


Figure 6.
Absolute displacement measurements of markers at left corner of CPU0, Sine Dwell, 30hz, 2.0G

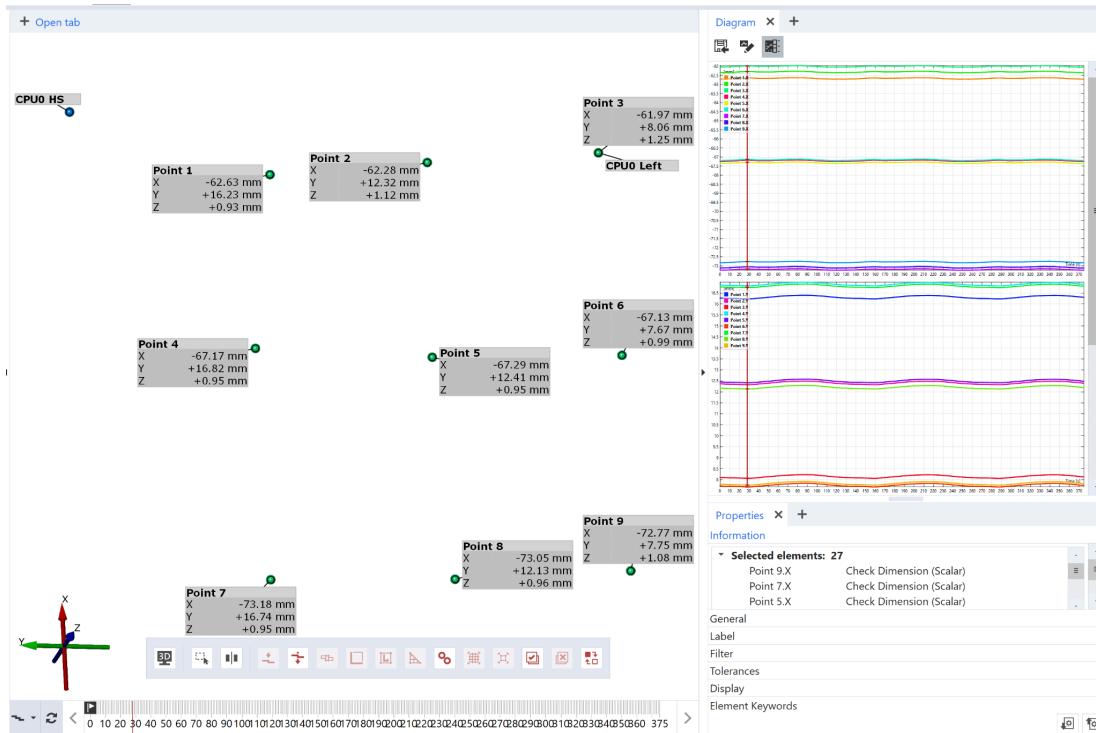


Figure 7.

Calculated microstrain (ummm/mm) between specific marker pairs, Sine Dwell, 30hz, 2.0G

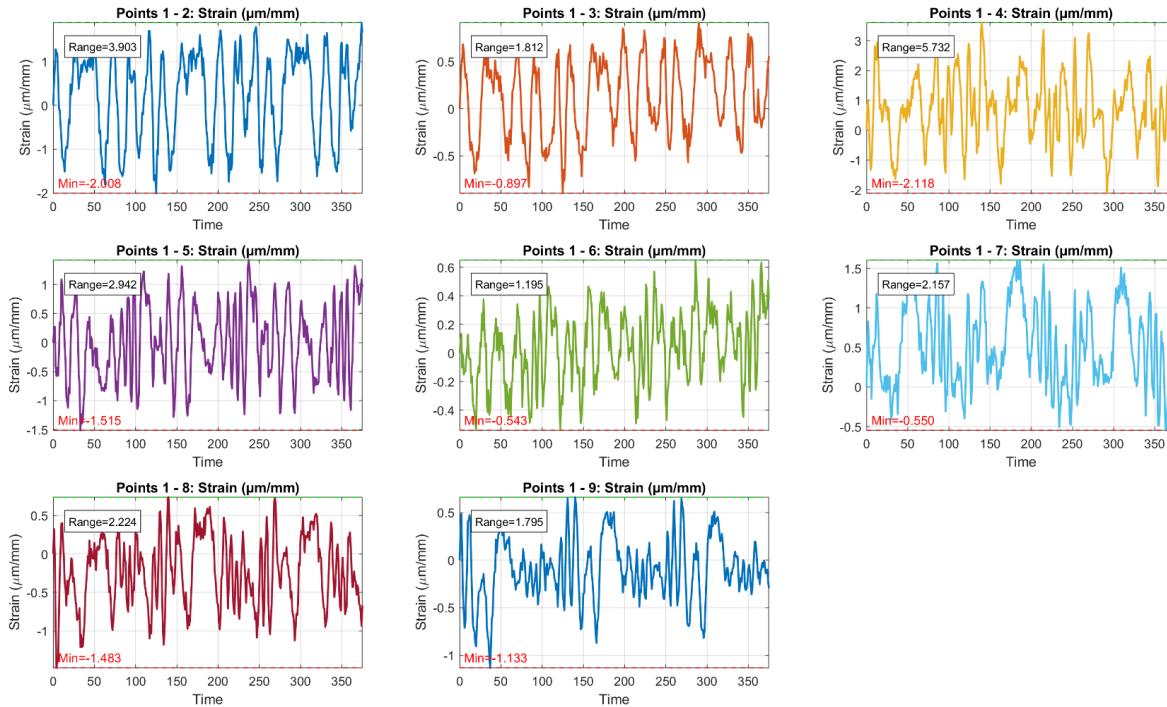


Figure 8.

Microstrain are calculated by looking at the change of relative distance between any two points with respect to values at time zero. We picked point 1 (closest to lower left corner of CPU0) as reference, and calculated microstrain relative to the 8 points near it. The calculated values are very very low, in the range of a single digit microstrain (ummm/mm) due to very similar absolute displacements values coming out of each marker. When relative movements are this small, these signals may simply be signal noise from the setup itself.

We are happy to see the values being well below what Intel and JEDEC guidelines define as threshold for damage, typically in the range of 500 to 1000 microstrain. Whether these numbers are noise is debatable - some sinusoidal behaviors are observed, but they appear to be fluctuating faster than 30hz, the drive signal, which produces slower relative displacement at the PCB that look like this (from part 1.1):

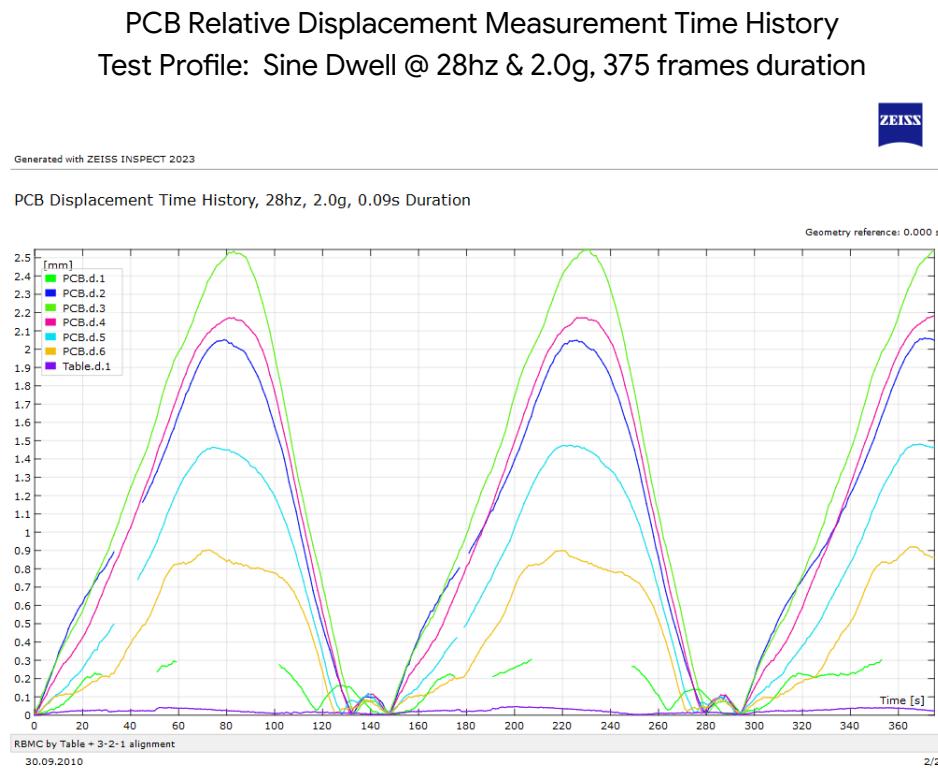


Figure 9.

Because these numbers are so low, there aren't evidence of large values of strain or relative displacements between the points. We expected that for vibration - the IPC/JEDEC guidelines themselves don't show any significant peaks until test samples are subjected to high G shock impacts.

We are going through this exercise because we want to develop the measurement capability for when the data does matter. Plus, we are still finding our way around the limit of our test setup. Let's look at a few other natural frequencies and the random vibration profile to see how the data look:

Calculated microstrain (ummm/mm) between specific marker pairs, Sine Dwell, 60hz, 2.0G

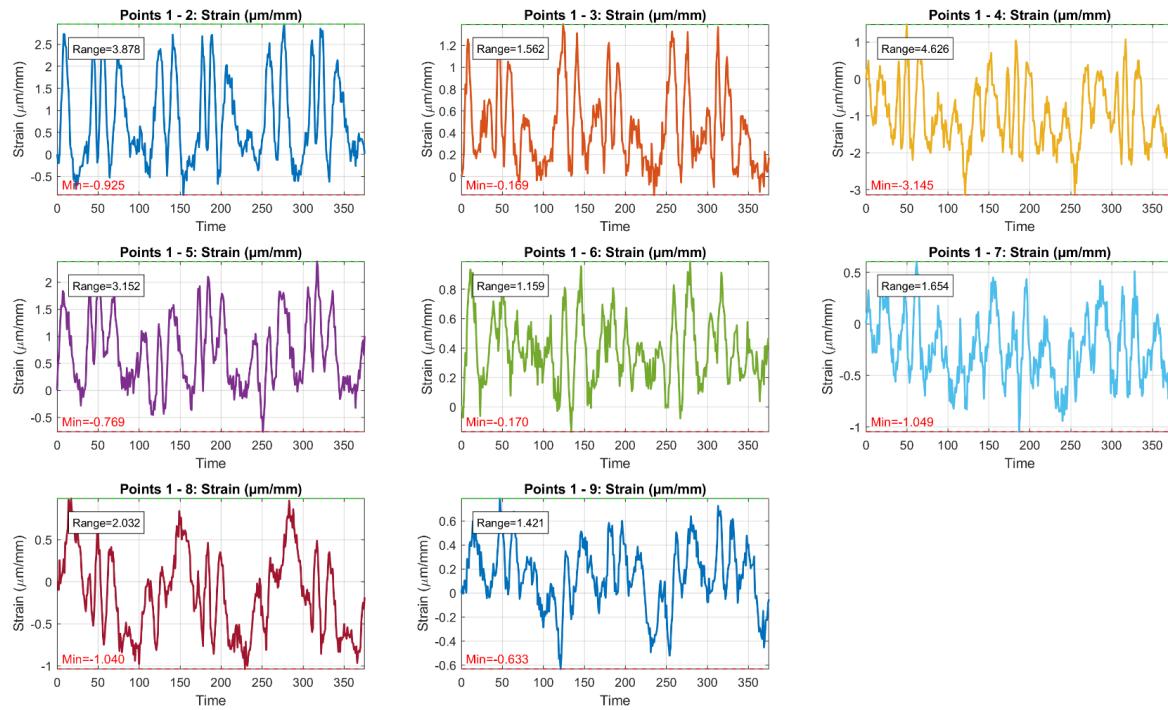


Figure 10.

Calculated microstrain (ummm/mm) between specific marker pairs, Sine Dwell, 129hz, 2.0G

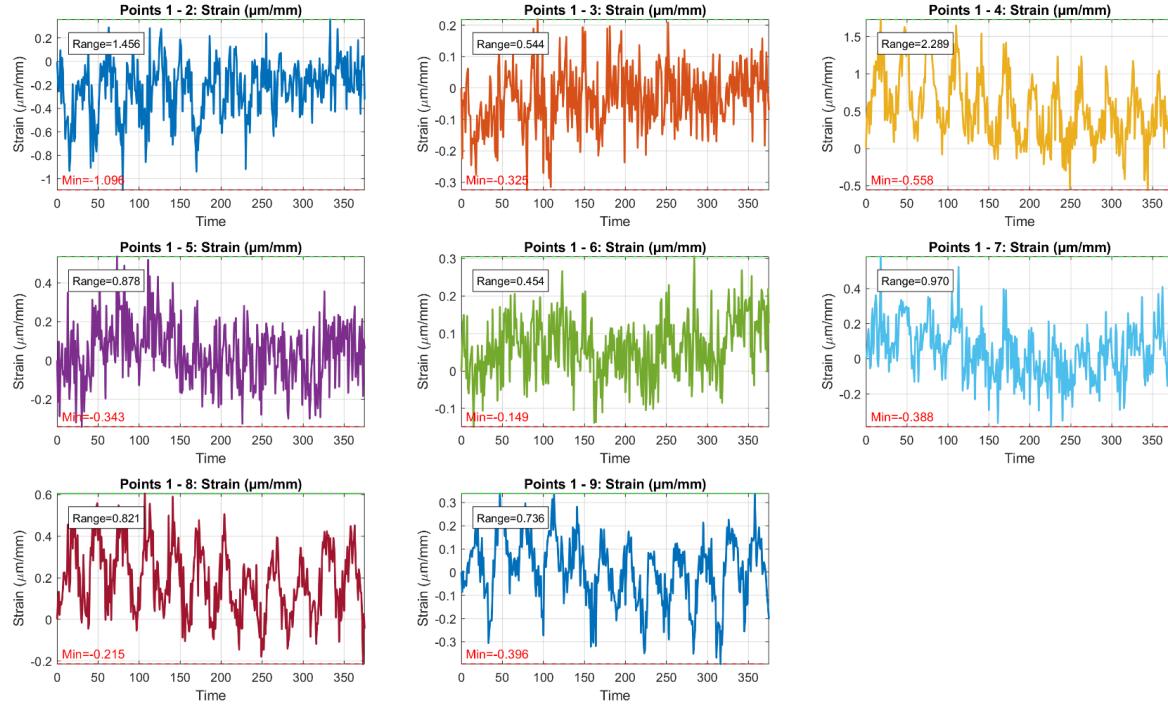


Figure 11.

Calculated microstrain (ummm/mm) between specific marker pairs, Random Vibration Profile, 1.07 Grms, 5hz to 300hz

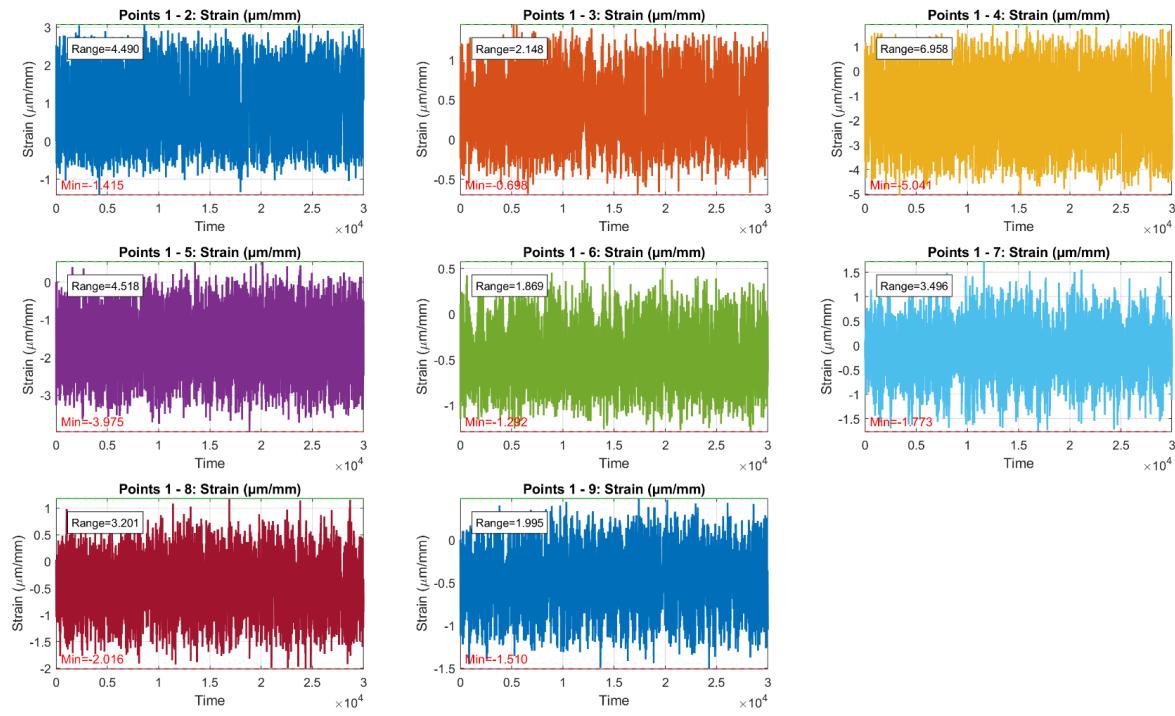


Figure 12.

If we focus on results for Points 1 - 4, the values appear to be lowered as natural frequency increases. We observed a range of 5.732 microstrain for 30hz, 4.626 microstrain for 60hz, and 2.289 microstrain for 129hz. That makes sense because higher modes are more complex and leads to smaller relative displacement and closer notes.

The range increases to 6.958 microstrain when the unit is subjected to the random vibration profile, and that's interesting because random vibration profile we used doesn't reach up to 2.0G at these frequencies. So either we are still looking at noises of the test setup, or something about random vibration is generating slightly larger absolute and relative displacements at these markers.

IPC/JEDEC 9704A Recommended Strain Limits

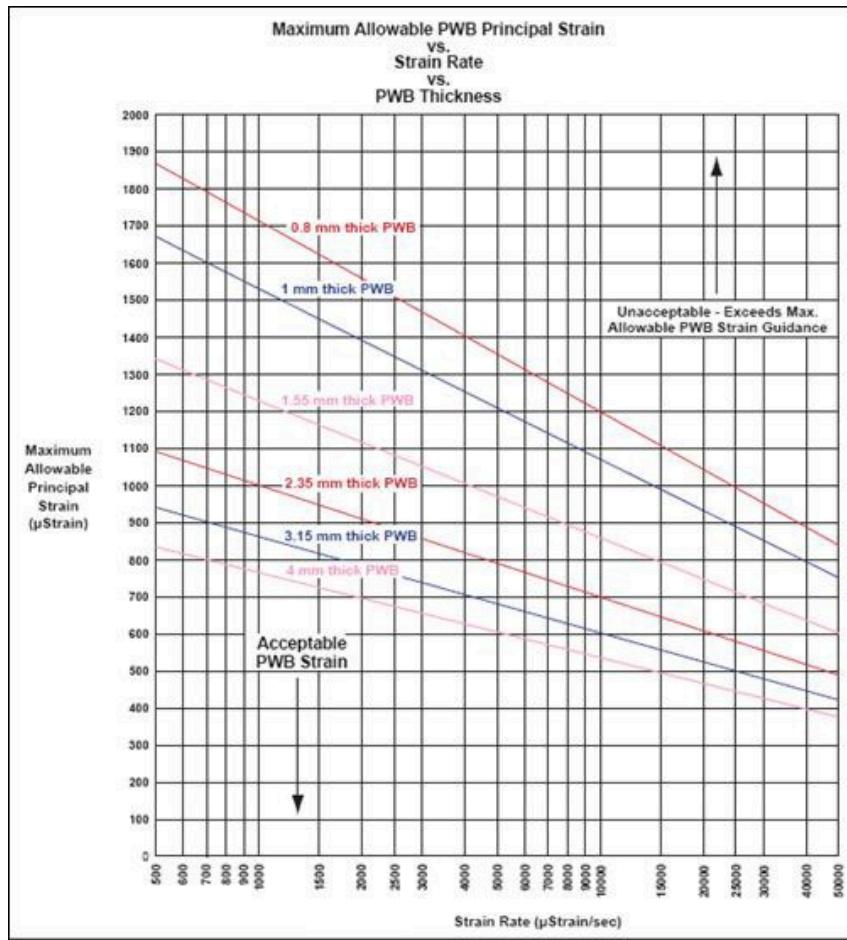


Figure 13.

One last note – while these numbers appear to be low in the context of historic IPC/JEDEC and Intel guidelines, you never know when low strain values would lead to damage in other types of components, with different geometry, material, layout, and stress concentration. Such determinations have to be made experimentally for each class of components. The location of the measurement plays a huge role, as well as the dynamic behavior of the component itself.

At the moment, such information is not widely published, leaving up to each company, supplier, and test lab to conduct their own investigation for the thousands of critical components inside the hardware. That is something I wish to fix with this project.

The Bigger Picture

Google's Chassis Level Sine Vibration Analysis

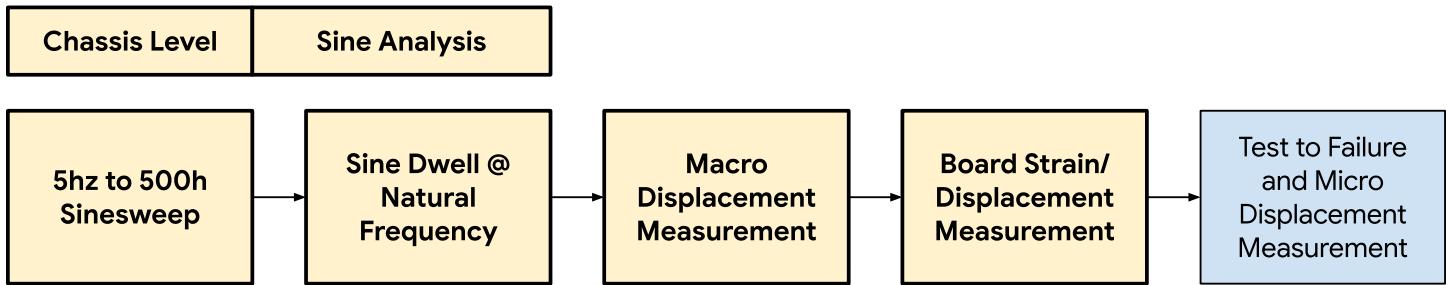


Figure 14.

Google's Chassis Level Random Vibration Analysis

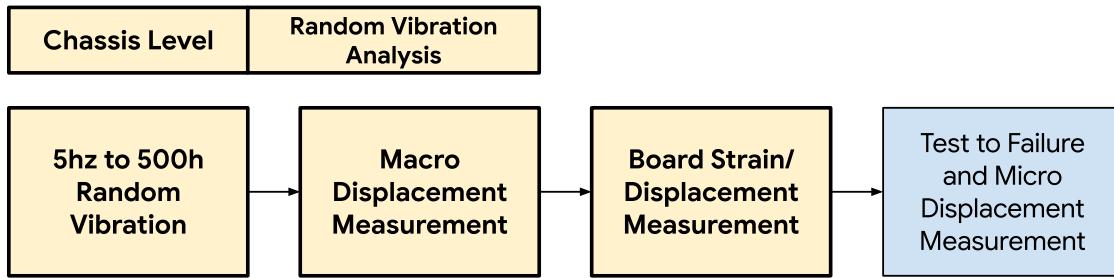


Figure 15.

We are one step closer to the full Google vibration analysis methodology. Board level measurements we made in this example are stepping into the realm of micro measurements. The noise level appears to be much lower than typical thresholds in historical IPC/JEDEC and Intel guidelines, but again, these may not be relevant in other types of microelectronics components.

The next step is to verify these measurements with actual strain gauges, which we will do in future papers concerning strain, and to zoom into an even smaller view and verify the noise level when resolutions of the area of interest is even higher.

Taking a step back, testing would be easy if we only care about a specific critical component. We would instrument strain gauges or set up high speed stereo cameras to measure strain values at pre-determined locations, and simply check to see if measured values exceed predetermined thresholds.

IPC/JEDEC 9704A Example of Strain Gauge Placements

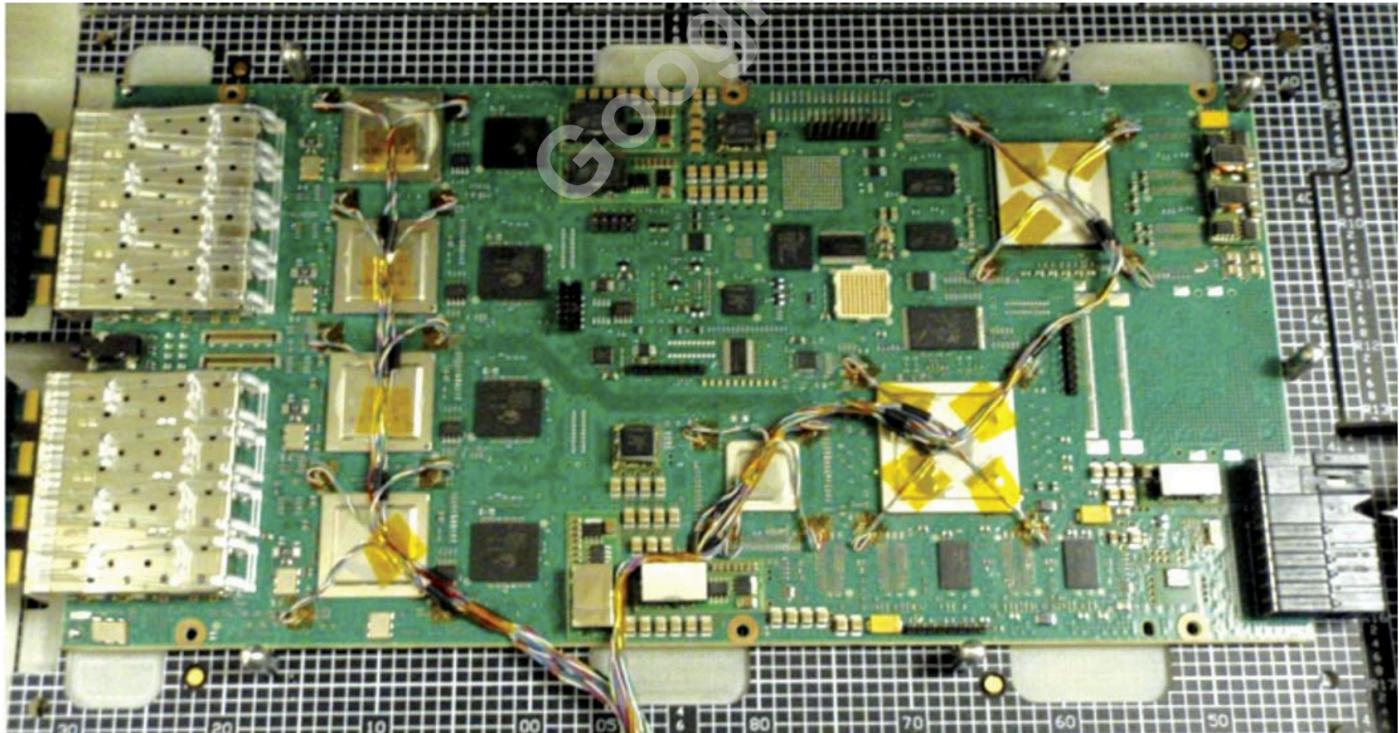


Figure 3-14 Lead Wire Routing Example

Figure 16.

Unfortunately, data center hardware is a lot more complex, and has many critical components that could lead to performance issues at product. Also, should failure occur, the component level perspective offers very little tools to mitigate such failure if the root cause ends up being machine design, shelf design, and rack design.

That's why we are always examining all layers of the stack to see where failure truly comes from. The sooner we map out all the common failure modes, and the choices and limit of mitigations available at each layer, the sooner we can focus on the optimization of each layer and how the overall stack up of damages.

References

1. IPC/JEDEC, *IPC/JEDEC-9703: Mechanical Shock Test Guideline for Solder Joint Reliability*. Bannockburn, IL, USA: IPC, 2007.
2. Intel Corporation, *Strain Measurement Methodology for Circuit Board Assembly - Board Flexure Initiative (BFI)*. Santa Clara, CA, USA: Intel, 2016.