Computer Architecture Lab 4 Report

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The prefetchers in Task 1 and 2 do not perform well on irregular memory requests because they can detect only a constant stride in an access pattern. The Markov prefetcher by ?? showed good results on irregular access patterns so for Task 3 we combine a Markov prefetcher with the stride prefetcher from Task 1 (or 2 not sure yet).

Design choices different from paper:

- Paper uses Markov prefetcher as prefetcher for LLC, we use it for L2 cache
- Paper considers only cache misses because prefetcher is off-chip, we consider all memory requests
- Paper uses a 1MB Markov table with 32-bit addresses, we have 64-bit addresses so the table size was adjusted accordingly