

# Computer Architecture HW3

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## 1 Critical Paper Reviews [500 points]

see here

## 2 Genome Analysis I [150 points]

### 2.1 Edit Distance

a) M O N - - - - T A G  
s - - i i i i - - -  
D O N N E R S T A G  
Edit Distance: 5

b) F R E I T A G  
s s s s - - -  
S A M S T A G  
Edit Distance: 4

c) D O N N E R S T A G  
d d d d d d d d d  
- - - - - - - - -  
Edit Distance: 10

### 2.2 Read Mapping

a) read1:  $6 + 3 + 3 = 12$   
read2:  $2 + 5 + 6 = 13$   
read3:  $2 + 0 + 0 = 2$   
read4:  $3 + 2 + 5 = 10$   
read5:  $6 + 5 + 3 = 14$

**51 invocations**

b) read1: 10, 15, 20  $\rightarrow$  1  
read2: 50, 55, 60 & 615, 620, 625  $\rightarrow$  2  
read3: -  $\rightarrow$  0  
read4: 610, 615, 620  $\rightarrow$  1  
read5: 710, 715, 720  $\rightarrow$  1

**5 invocations**

- c) AAAAA and GGCCT are above threshold.

read1:  $0 + 3 + 3 = 6$

read2:  $2 + 0 + 0 = 2$

read3:  $2 + 0 + 0 = 2$

read4:  $0 + 3 + 2 = 5$

read5:  $0 + 0 + 3 = 3$

**18 invocations**

### 3 Genome Analysis II [150 points]

- a)  $\{AAAA\} \rightarrow \{1\}$

$\{ATAC\} \rightarrow \{5, 17, 41\}$

$\{TGAT\} \rightarrow \{9, 43\}$

$\{CCTT\} \rightarrow \{13\}$

$\{GTTG\} \rightarrow \{21, 37\}$

$\{TAAG\} \rightarrow \{25, 45\}$

$\{GTTT\} \rightarrow \{29\}$

$\{CAAA\} \rightarrow \{33\}$

- b)  $\{AAAA\} \rightarrow \{1\}$

$\{ATAC\} \rightarrow \{5, 17, 41\}$

$\{GTTG\} \rightarrow \{21\}$

$\{CAAA\} \rightarrow \{33\}$

- c) non-overlapping 4-mers:  $2^{\log_2(8)} + 13 = 21$  bytes

non-overlapping 4-mers minimizers:  $2^{\log_2(2)} + 6 = 10$  bytes

- d) **non-overlapping 4-mers**

3 cycles for hash table query

144 cycles for edit distance calculation

total cycles:  $3 + 2 \times 144 = 291$  cycles

wasted cycles:  $0.9 \times 291 = 262$  cycles

**non-overlapping 4-mers minimizers**

2 cycles for hash table query

144 cycles for edit distance calculation

total cycles:  $2 + 144 = 146$  cycles

wasted cycles:  $0.8 \times 146 = 117$  cycles

### 4 RowClone [150 points]

- a) Step 1:

The memory controller writes back any dirty cache line from the source region.

Step 2:

The memory controller invalidates any cache line (clean or dirty) from the destination region that is cached in the on-chip caches.

- b) To perform the copy operation without RowClone, the memory controller transfers the source page (physical page 10) over the data bus to the caches. Then, the destination page (physical page 12) is written back to main memory. A page has 8KB and the memory controller moves two pages i.e. 16KB over the memory bus.

With RowClone the copy is performed inside the DRAM, so now data is transferred over the memory bus.

Amount of data eliminated: 16KB

## **5 Tiered-difficulty [150 points]**

- a) a
- b) b
- c) c
- d) d
- e) e

## **6 Low-Latency DRAM [150 points]**

- a) a
- b) b
- c) c
- d) d
- e) e
- f) f
- g) g