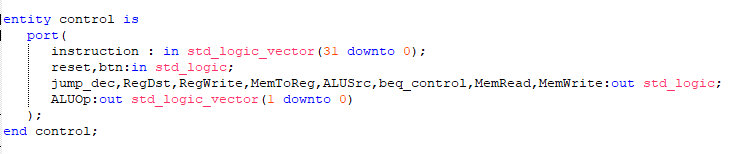
**INTRODUCTION:**

**This lab is a step forward towards the MIPS32 microprocessor. In this lab we will create the control unit, which will generate all control signal to other modules. It will convert the 32 binary bits into different value which will make sense for the processor. This control unit will detect the type of instruction and decide wich control signal should be generated.**

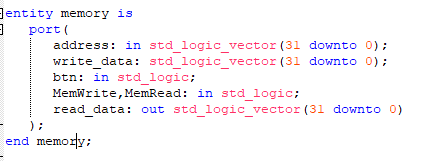
**PRE-LAB TASKS:**

**Task 1:**



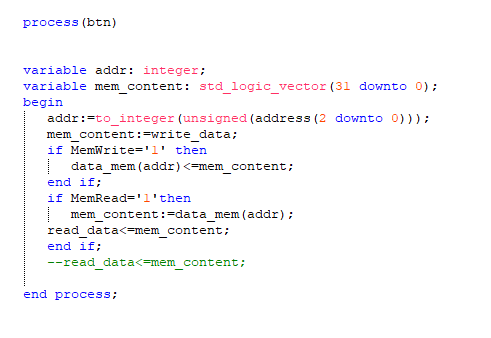
This is the entity of the control unit. These are the Input/output of this unit. **In this task we have to understand the functionality of control unit in the MIPS32 and write the pseudocode of it which will be later converted into the VHDL code.**

**Task 2:**



This is the entity of the Data Memory. These are the Input/output of this unit. **In this task we have to understand the functionality of memory module in the MIPS32 and write the pseudocode of it which will be later converted into the VHDL code.**

**LAB TASKS: Task 1:**



**LAB TASKS: Task :**



We connected the decode and fetch module and futher in coming labs we will use it.

# CONCLUSION:

In this lab we created the control module and data memory. Control generates the signal to the other units to perform there task .