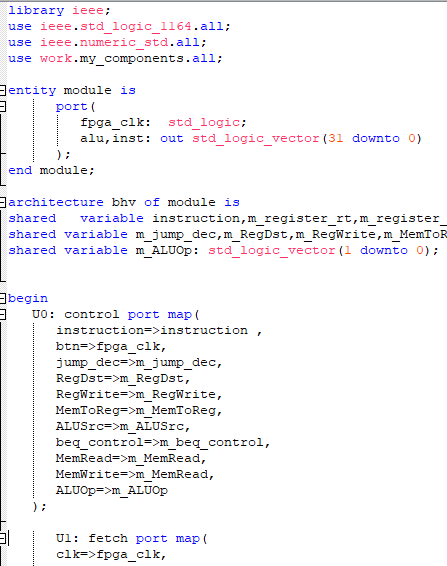
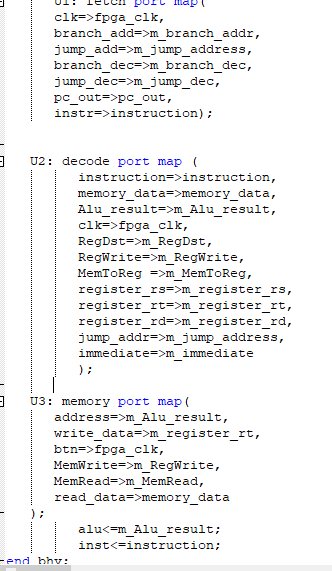
**INTRODUCTION:**

**In this lab we have created the processor and we are going to test it with know instruction set and test it that it works according to our demands. I will check it by displaying it on LCD. I will check it by ALU output of given instruction.**

**PRE-LAB TASKS:**

**Task 1:**

**LAB TASKS: Task 1:**

In this lab task I have to test some instructions on it to verify the results

**LAB TASKS: Task 2:**

Output of the lab task 1 will be shown on LCD.

# CONCLUSION:

In this lab we created the whole model of the processor. All of the outputs of the control module are connected to the specified locations.. And all the previse labs are included in this lab to complete the task. All the previse labs are tested and verified on FPGA boad so now we will run it to check its working as a whole processor