**INTRODUCTION:**

**From this lab onwards we are designing the MIPS32 processer which is divided into different parts. It is single cycle processer. First one is the Fetch module in this module according to our design it will contain an instruction set will execute in processer in single cycle.**

**And two kind of addresses**

**1. Branch address**

**2. Jump address**

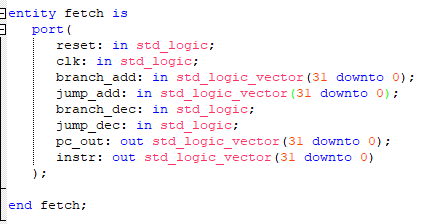
**And two signals to change address**

1. **Branch decision**
2. **Jump decision**

**When the branch decision is ON our instruction counter jump to the branch address in the instruction set and same for the Jump decision.**

**PRE-LAB TASKS:**

**Task 1:**



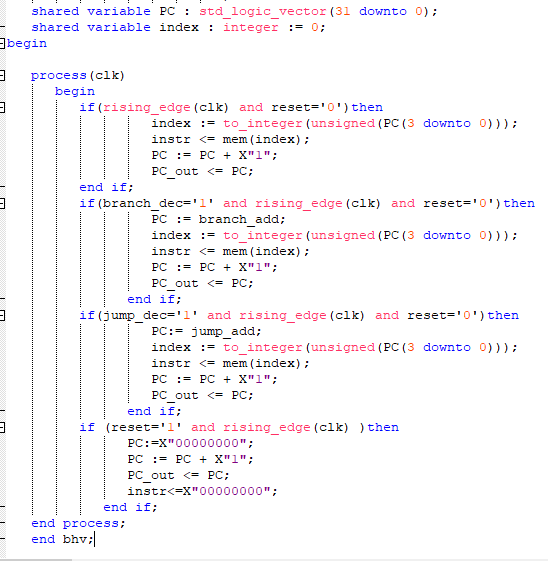
This is the entity of the fetch module. This are the Input/output of this unit.

**Task 2:**

**In this task we have to understand the functionality of fetch module in the MIPS32 and write the pseudocode of it which will be later converted into the VHDL code.**

**LAB TASKS:**

**Task 1:**



# CONCLUSION:

In this lab we created the fetch module. It deals with the instruction of the processer. All the instruction in the array of std\_logic\_verctor(31 downto 0) . instruction is fetch on the rising edge of the clock which is set to the button of the FPGA board. Some changes are made according to the conditions when branch or jump decision occurs.