# Star

eConfig is a design rule checker and device configuration tool for eAsic technology. It checks various design rules checkings(DRC) on the user design.
The main purpose of this is to find out errors in the design as early as possible.

eConfig DRCs are used at different stages of eAsic tool flow. It runs in front-end(FE): after Fit Device(Initial) and Floorplaning(Post-FP) steps, the name of executable is rdbeconfig. At these steps it uses data from RDB DB.

Also eConfig runs in back-end(BE): in Device Mapping(eConfig1), Configure Device(eConfig2) and Handoff(eConfig3) steps, the name of executable is econfig. Econfig uses data from OA DB.

| Description | Type | Initial | Post-FP | eConfig 1 | eConfig 2 | eConfig 3 |
|---|---|---|---|---|---|---|
| **Top level port connection check**<br><br>Check that each top level port from the design is connected to a PAD or MGIO. | Warning | X | X | X | X | X |
| **Top level port floating check**<br><br>Check that each top level port is not floating. | Error | X | X | X | X | X |
| **Top level port connection check for intrinsic**<br><br>Check if each top level port is not connected to intrinsic pin accept PAD or MGIO instances. | Error | X | X | X | X | X |
| **Multi-driven net and inout pin check**<br><br>Check that there are no nets with multiple drivers and unexpected inout pins. Known exceptions are handled. | Error | X | X | X | X | |
| **PLL output check**<br><br>For each PLL, check that outputs 6-7 are not used, unless all outputs 0-5 are all used. In other words, the design must use outputs 0-5 before using outputs 6-7. | Error/Warning | X | X | | | |
| **Pin check by pattern**<br><br>Special connectivity checks for pins listed in file check_pin_net.csv. For example, we check that pin eclkgate/CLKEN is not tied to ground. Various combinations of power/ground/signal checks are available. | Error | X | X | X | X | X |
| **Top level port name check**<br><br>Check that design top level port names are different from device top level port names and from shared test pin names. | Error | X | X | X | X | |
| **MGIO top level port check**<br><br>Check that top level pins of MGIO instances are connected to unique top level design ports. | Error | X | X | X | X | X |
| **Sequential cell unconnected pin check**<br><br>Check if a sequential cell (edff, bram, regfile) data pins (I_D, O_Q) are all unconnected. | Warning | X | X | X | X | X |
| **Clock gate check for BROM**<br><br>For each BROM instance (bram/regfile with defparam INIT_ON), check that there is a clock gate on the clock source path. Both clock pins I_CLKA/I_CLKB are checked. Valid clock gate cells are eclkgate, eclkgenloc, eclkmux. | Error | X | X | X | X | X |

| | | | | | | |
|---|---|---|---|---|---|---|
| **IO and MGIO placement check**<br><br>Check that all IO and MGIO instances are placed and not overlapping. General placement check for all instances happens in eConfig. | Error | | X | | | |
| **Corner block check**<br><br>Check that corner block is instantiated in the design. | Fatal/Error | X | X | | | |
| **PLL/MGIO power/ground pin check**<br><br>Check that all power/ground pins of PLL and MGIO instances are bonded out in the package. Check power/ground domains for PLL instances. | Error | | X | X | X | X |
| **Test pin check**<br><br>Check that all test pins are bonded out in the package.<br><br>Check that VREF IO is not placed on a location with input test pin.<br><br>IO configured as xxxpwrpad or xxxvsspad can not be placed on a location with output test pin. | Error | | X | X | X | X |
| **Temperature diode check**<br><br>Check that top level ports of all enabled temperature diodes are bonded out | Error | X | X | X | X | X |
| **IO port connection check**<br><br>Check that PAD, PADP, PADN pins of IO cells are connected to top level ports. VREF and UNBOUNDED IOs are allowed not to be connected. | Error | X | X | X | X | X |
| **Dedicated test pin check**<br><br>Check that no user pin is assigned to dedicated test pin locations. Dedicated locations include TEST_MODE, JTAG_MODE and other JTAG pins (if jtag option is enabled). Also, dedicated pins include IOs with valid defparam JTAG_FUNCTION ("user JTAG"). | Error | | X | X | X | X |
| **ODT configuration check**<br><br>Check that ODTEN signal value matches configuration of padng_odt instance. If padng_odt instance is offx then ODTEN must be 0. If padng_odt instance is not offx then ODTEN must be either 1 or a net. | Error | X | X | X | X | X |
| **Uided pin check**<br><br>Check that IOs with bsc type "uided" are not assigned to shared output test pin location | Error | | X | X | X | X |
| **Intrinsic net check**<br><br>Check that intrinsic nets from the design match their counterparts on the physical device. In other words, one intrinsic net from the design cannot connect pins from different device intrinsic nets. However, an intrinsic pin in the design may be connected to a valid constant as defined in the corresponding pininfo file. | Error | | X | X | X | X |
| **Mixed net check**<br><br>Check that each net connects only intrinsic or only routable pins. There are certain exceptions involving logical clock macros and test pins. | Error | X | X | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| **Placement check**<br><br>Check that all instances are placed on correct physical sites and that they do not overlap (with exception of hecell/efa cells). Check packing of hecell/efa. | Error | | | X | X | X |
| **Routable net check**<br><br>Check that routable nets do not have connections with intrinsic pins (with known exceptions) | Error | | | X | X | X |
| **Undriven pin check**<br><br>Check that each routable input pin is connected to a net with driver, and it is not connected to top level port (for non-padless designs). Check if output of edff is used. | Error | X | X | X | X | X |
| **VCCIO voltage check**<br><br>Check that all IOs in a subbank have the same VCCIO voltage | Error | | X | X | X | X |
| **VREF voltage check**<br><br>Check that all IOs in VREF subbank have the same VREF voltage | Error | | X | X | X | X |
| **Vreftune group check**<br><br>Check that all IOs that require vreftune have pin VREFT connected. Extract vreftune groups from the netlist and check that they match vreftune groups and connectivity on the device. | Error | | X | X | X | X |
| **COMP_EN/COMP_UPD check**<br><br>For each IO check that if COMP_EN != 0 then COMP_UPD != 0. Also, if COMP_EN != 0 and COMP_UPD != 0, check that all bits of CADD_I and CDAT_I are connected to a non-constant net.<br><br>Also if COMP_EN == 0 then COMP_UPD, CADD_I, CDAT_I all should be 0; this is fatal error.<br><br>If COMP_EN == 1 or COMP_EN == NET, then COMP_UPD should be connected to register. If no, this is error.<br><br>Also if COMP_UPD == 1 and COMP_EN == 0, issue a warning because of possible design problem.<br>if COMP_UPD == 1 and COMP_EN == 0 or NET then print error , because latches will be transparent all the time. | Error/Warning/Fatal | X | X | X | X | X |
| **DDR DLL check**<br><br>Check that for each active edlygenddr4s, corresponding dqsgen instance is also active. | Error | X | X | X | X | X |
| **LVDS ODTEN check**<br><br>Check that ODTEN for output LVDS IOs is not 0. | Error | X | X | X | X | X |
| **CLKDIV_PWRDN check**<br><br>Check that the bits of defparam CLKDIV_PWRDN match with the used outputs of PLL. If a bit of CLKDIV_PWRDN is 0, corresponding PLL output must be used. If the bit of CLKDIV_PWRDN is 1, corresponding PLL output must not be used. | Error/Warning | | | | X | X |
| **Bsc configuration check for differential IO**<br><br>Check that If an IO has odt configured as pdif, then corresponding bsc instance must be of "double" type pad_bscd_***d*. | Error | | | | | X |

| | | | | | | |
|---|---|---|---|---|---|---|
| **IDCODE/USERCODE/PNC check**<br>Check that IDCODE and USERCODE paramaters from the project settings match actual tie off connections on the corner block. Also check that PNC digit cells have types corresponding PNC parameter. | Error | | | | | X |
| **Instance and net name uniqueness**<br>Check that all instance and net names are unique using case insensitive comparison. Formally Verilog allows an instance and a net to have the same name, and it also allows two objects to have the same name in different letter case. However, not all 3rd party tools support these situations.<br>By default this check prints warning but if variable ETOOLS_NAME_CONFLICT_ERROR=1 then it prints errors. | Error | X | X | X | | |
| **Intrinsic pins tieoff check**<br>Unconnected intrinsic pins in design should be tieoffed constant net using pininfo information. | Error | X | X | X | | |
| **Combined pins nets check**<br>Some pins in design should be connected to the same net. Groups of such pins are defined in combined_ports.txt file | Error | | X | X | X | X |
| **MGIO IDDQ pin check**<br>If MGIO is used, IDDQ must be tied to 0. If MGIO is not used, IDDQ must be tied to 1. | Error | X | X | X | X | X |
| **MGIO AREFENABLE pin check**<br>Pin AREFENABLE should not be tieoff for used MGIO. | Error | X | X | X | X | X |
| **InOut IO check**<br>Check RX/TX configurations of IO instances and compare them with IE/OE values and top ports directions. | Error | X | X | X | X | X |
| **WKE check**<br>Check that I_WKE(P\|N) pins are connected to any net. If pin I_WKE is not connected at all then tool prints error. If pin is not connected to constant net then tool prints warning. | Error/Warning | X | X | X | X | X |
| **Check eclkgate and edff polarity**<br>Check polarity of eclkgate and edff's in clock nets. Type eclkgaten_r is only driving pins edffn*/I_CLK. Type eclkgate_r is not driving any pin edffn*/I_CLK. | Error | X | X | | | |
| **Check dcdl type upon used device**<br>If the device type is not 'e', do not allow to use dcdl3 types in design. | Fatal | X | X | X | X | X |
| **Check dcdl DFT_O pin**<br>DFT_O pin of dcdl type cell should not drive any logic cell except buffer. | Eroor/Fatal | X | X | X | X | X |
| **Check dcdl defparam FV_MODEL**<br>Print warning for every dcdl instance that has defparam FV_MODEL with value "SIMPLE". | Warning | X | X | X | X | X |

| | | | | | | |
|---|---|---|---|---|---|---|
| **Check dcdl connections mtx* and mrx* cell types**<br><br>If dcdl drives mtx*, print an error. If mrx* drives dcdl, print an error. | Error | X | X | | | |
| **Check clock inverter types**<br><br>Clock inverter types for design depend upon device version. eclkinvb_on/eclkinvb1b_on types can not be used for device version < 'f',<br><br>eclkinv_on/eclkinv1b_on ones can not be used for device version >= 'f'. | Error | | | X | | |
| **Check tx/rx/logical cell types**<br><br>TX/RX/LOGICAL clock macros types should be compatible each other. They should be configured by the same sets of virtual pins: V_IOSUPPLY, V_RXVAR and V_TXVAR. | Error | | | | X | X |