Congratulations! You passed!

Grade received 80% Latest Submission Grade 80% To pass 80% or higher

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1. In Verilog, a latch is generated from the following code, because … : 1 / 1 point

```
always @(clock or d_in or clear)
begin
if (clear == 1) q_out <= 0;
else if (clock == 1) q_out <= d_in;
end
```

- ○ Because clear is an asynchronous reset.
- ◉ Because d_in is included in the sensitivity list.
- ○ Because clock is synchronous.

Correct
Correct. Each time d_in changes the always block is evaluated.

Correct. Each time d_in changes the always block is evaluated.

2. The following verilog code has a synchronous reset, because ... : 1 / 1 point

```
always @(posedge clk)
begin
if ( ! reset ) Q <= 4'b0000;
else if (shift == 1) Q <= Q << 1;
end
```

- ○ Q output is shifted by one with the << shift operator.
- ○ reset is inverted by ! whenever reset is evaluated.
- ◉ reset is evaluated within the posedge clk block.

Correct
Correct.

- Q output is shifted by one with the << shift operator.
- reset is inverted by ! whenever reset is evaluated.
- (selected) reset is evaluated within the posedge clk block.

Correct
Correct.

3. Select the incomplete sensitivity list item for the combinatorial circuit causing indeterminate synthesis and simulation results:

1 / 1 point

- always @ (a, b, c) y = a & b & c;
- (selected) always @ (a or b) y = a & b & c;
- always @ * y = a & b & c:

Correct
Yes.

4. The following verilog code generates a:

1 / 1 point

4. The following verilog code generates a: **1 / 1 point**

```
module my_block (
 input wire clock, reset,
 input wire [15:0] d,
 output reg [15:0] q );
always @ (posedge clock, negedge reset)
 if ( ! reset ) q <= 0;
 else q <= d;
endmodule
```

- ○ Flip Flop.
- ○ Counter.
- ○ RAM Memory.
- ◉ Register.

Correct
Yes.

5. The following verilog code is important, because ... : **0 / 1 point**

```
assign z_out = ( oe == 1)? data_out: 8'bz;
```

(Select any answer that applies.)

- [x] IO power is reduced.

Correct
Yes. When tri-stated the IO is not driving.

- [ ] The z_out bus is protected, provided the output enable is timed correctly.
- [x] The IO is undriven, so other devices connected can safely drive.

Correct
Yes. When tri-stated other devices can drive the IO without power conflict.

- [ ] The bus is MUXed so other devices on the bus can safely drive.

You didn't select all the correct answers

6. Select the following verilog code signal declaration for a RAM memory: **0 / 1 point**

- ○ reg [1023:0] RAM;
- ◉ signal RAM: ram_type:= read_ram("RAM_FILE.txt");
- ○ wire [31:0] RAM [1023:0];
- ○ reg [31:0] RAM [1023:0];

Incorrect
No, this is VHDL.

7. Recall the memory constructs and select all correct statements: **1 / 1 point**

- ☐ After Synthesis, the following ROM data can be written to for future reads.

```
always @*
case(addr)
 2'b00: rom_data = 8'b1000_0000;
 2'b01: rom_data = 8'b1010_1010;
```

7. Recall the memory constructs and select all correct statements: **1 / 1 point**

- [ ] After Synthesis, the following ROM data can be written to for future reads.

```
always @*
case(addr)
 2'b00: rom_data = 8'b1000_0000;
 2'b01: rom_data = 8'b1010_1010;
 2'b10: rom_data = 8'b0101_0101;
 2'b11: rom_data = 8'b1111_0011;
endcase
```

- [x] In Verilog, the memory storage is declared by using a two-dimensional array.

Correct
Yes, this is correct.

- [x] RAM can be initialized by an external file.

Correct
Correct. Check out the example code provided in slides.

- [ ] In an FPGA, the synthesizer uses only the RAM IP block or block memory to implement RAM.

8. The following testbench verilog creates: **1 / 1 point**

```
always
begin
clock = 1'b0; #(50/2);
clock = 1'b1; #(50/2);
end
```

- ○ A single pulse 25ns wide.
- ○ Forever repeating clock at 50MHz.
- ◉ Forever repeating clock at 20MHz.
- ○ A single pulse 50ns wide.

Correct
Correct.

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Module 4 Quiz

Graded Quiz • 30 min

English

Due Sep 24, 11:59 PM IST

9. Recall the test bench structure and select all correct answers from below:

1 / 1 point

- [ ] Pound '#' delays such as the following are synthesized into delay elements in the cell library:

```
reset = 1'b0;

#100;

reset = 1'b1;
```

- [x] Model under test uses either external stimulus or test vectors to generate output vectors.

Correct
This is correct

- [ ] Output vectors alone are enough to validate a design.
- [x] There is no sensitivity list present in test bench module at the top level

Correct
Correct, this is because there are no external interfaces to the testbench.

10. Assertions are used in verilog testbenches to perform the following:

1 / 1 point

(select any that are True)

- [x] Severity level can be set to various levels: fatal, error, warning, and info.

Correct
True.

- [ ] Assertions are displayed during synthesis for debug.
- [x] Assertions can be turned on or off during simulation run.

Correct
True.

- [x] Assertions evaluate and print useful messages for design debug.

Correct
True.