

FPGA Architectures

Week 1 - PLDs and the FPGA

Week 2 - Quartus Prime and FPGA Design

Week 3 - Extending our knowledge of
FPGA capabilities

FPGA Architectures

Designing digital devices
is a creative process.

To be proficient,
know what's available.



FPGAs of many Flavors

Xilinx, Altera, Microsemi and Lattice all make PLDs

- Not for every application
- Each vendor has its specialities

Why use one instead of another?



FPGAs of many Flavors

We will determine criteria to help us decide which is best for a particular application.



Criteria for selecting FPGAs

Essential capabilities we need in an FPGA

Provide ample amounts of logic

Measured by system gates, logic elements, slices, macrocells, LABs, ALMs, etc.

Cost per gate is also important.



Criteria for selecting FPGAs

Speed - measured by maximum clock frequency.

Low power consumption - varies from microwatts to hundreds of watts.

Reprogrammability - dependent on configuration memory type, helps speed development.



Power Matters.™



Criteria for selecting FPGAs

Amount and type of I/O - thought of in terms of cost per I/O and I/O density.

Inclusion of Hard IP cores, like those for Memory, DSP Blocks, Transceivers, and even hard processors.

CPLDs and smaller FPGAs, are structured so that timing is deterministic.



Criteria for selecting FPGAs

Reliability is a major concern, measured by FIT rate or MTBF.

Endurance of the Configuration Memory - issue for long lifetime products, important parameter in FLASH based FPGAs.

Ability to protect design information held in FPGA bit pattern, and data that travels through the FPGA.



Programmable Logic Device Selection Criteria

1. Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)
2. Cost per logic gate
3. Speed (Maximum clock frequency)
4. Power Consumption (static and dynamic)
5. Reprogrammability (Configuration Memory Type)
6. Cost per I/O (I/O Density)
7. Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)
8. Deterministic timing (timing is consistent in every implementation)
9. Reliability (FIT rate)
10. Endurance (number of programming cycles and years of retention)
11. Design and Data Security

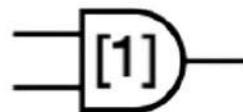
Features

- Optimized for high-performance 3.3V systems
 - 5 ns pin-to-pin logic delays, with internal system frequency up to 208 MHz
 - Small footprint packages including VQFPs, TQFPs and CSPs (Chip Scale Package)
 - Pb-free available for all packages
 - Lower power operation
 - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
 - 3.3V or 2.5V output capability
 - Advanced 0.35 micron feature size CMOS FastFLASH technology
- Advanced system features
 - In-system programmable
 - Superior pin-locking and routability with FastCONNECT II switch matrix
 - Extra wide 54-input Function Blocks
 - Up to 90 product-terms per macrocell with individual product-term allocation

- Local clock inversion with three global and one product-term clocks
- Individual output enable per output pin with local inversion
- Input hysteresis on all user and boundary-scan pin inputs
- Bus-hold circuitry on all user pin inputs
- Supports hot-plugging capability
- Full IEEE Std 1149.1 boundary-scan (JTAG) support on all devices
- Four pin-compatible device densities
 - 36 to 288 macrocells, with 800 to 6400 usable gates
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
 - 10,000 program/erase cycles endurance rating
 - 20 year data retention
- Pin-compatible with 5V core XC9500 family in common package footprints

Table 1: XC9500XL Device Family

	XC9536XL	XC9572XL	XC95144XL	XC95288XL
Macrocells	36	72	144	288
Usable Gates	800	1,600	3,200	6,400
Registers	36	72	144	288
T_{PD} (ns)	5	5	5	6
T_{SU} (ns)	3.7	3.7	3.7	4.0
T_{CO} (ns)	3.5	3.5	3.5	3.8
f_{SYSTEM} (MHz)	178	178	178	208



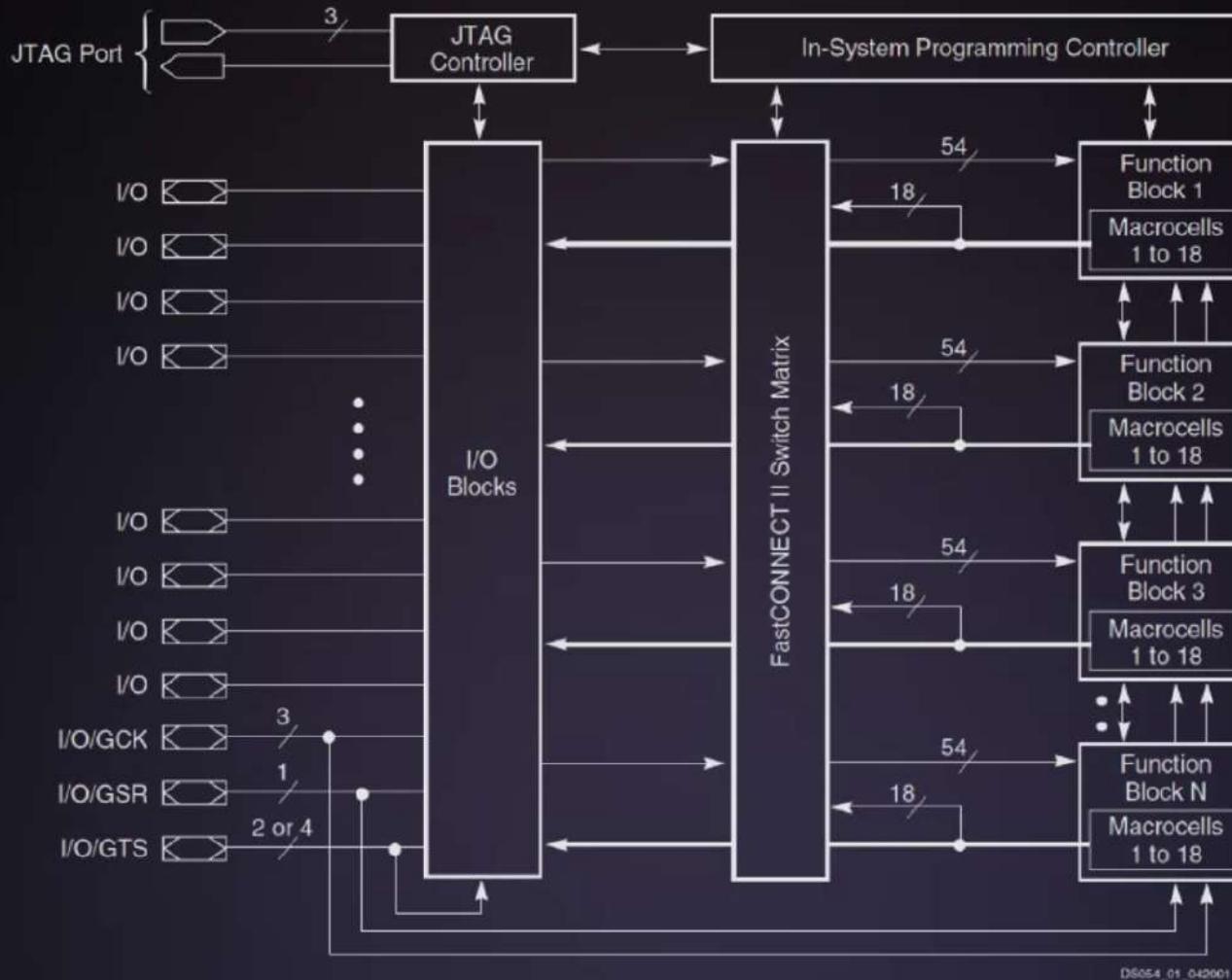
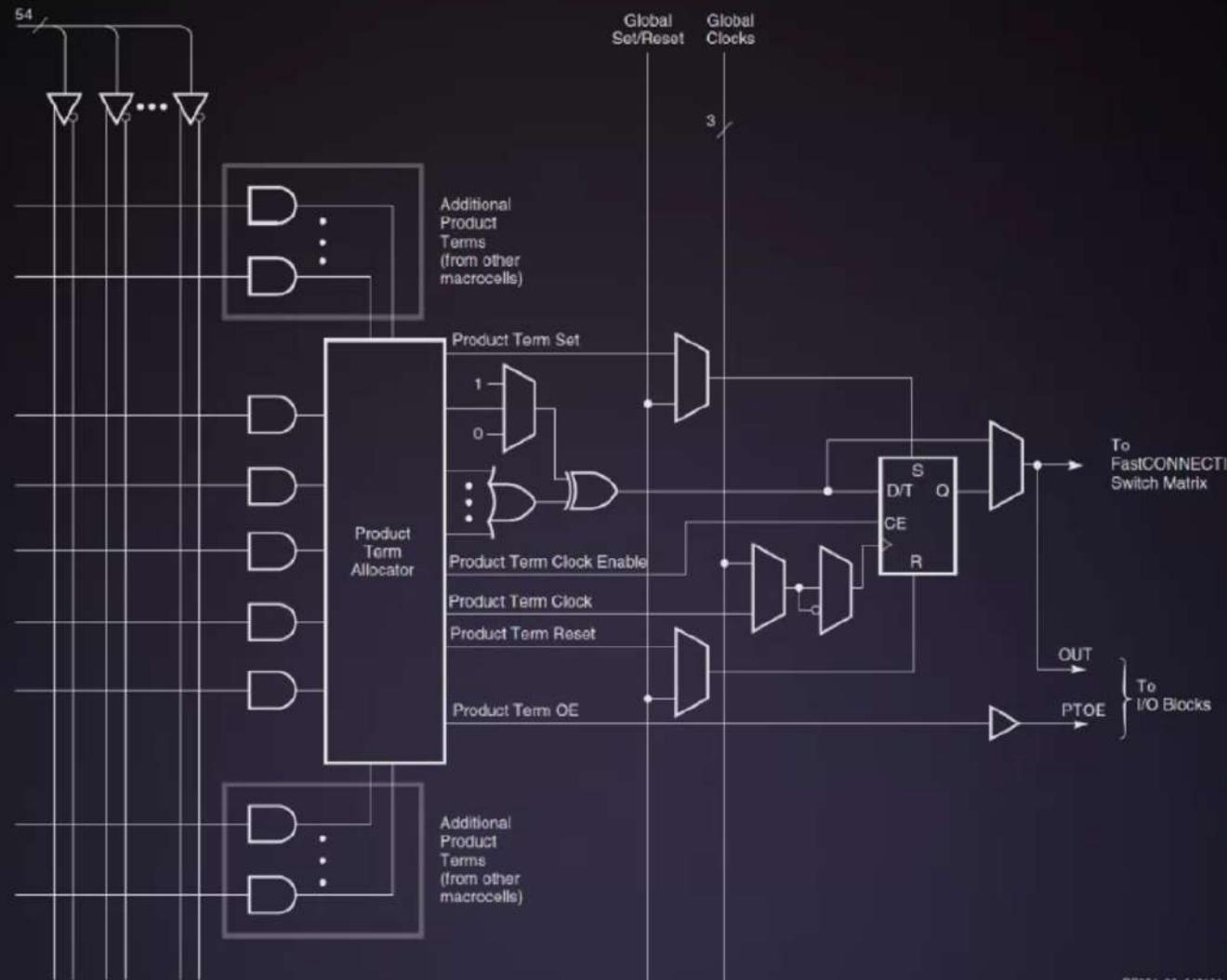


Figure 1: XC9500XL Architecture

Note: Function block outputs (indicated by the bold lines) drive the I/O blocks directly.

[2]



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Figure 3: XC9500XL Macrocell Within Function Block

[3]

Product Specification

Features

- Optimized for 1.8V systems
 - Industry's fastest low power CPLD
 - Densities from 32 to 512 macrocells
- Industry's best 0.18 micron CMOS CPLD
 - Optimized architecture for effective logic synthesis
 - Multi-voltage I/O operation — 1.5V to 3.3V
- Advanced system features
 - Fastest in system programming
 - 1.8V ISP using IEEE 1532 (JTAG) interface
 - On-The-Fly Reconfiguration (OTF)
 - IEEE1149.1 JTAG Boundary Scan Test
 - Optional Schmitt trigger input (per pin)
 - Multiple I/O banks on all devices
 - Unsurpassed low power management
 - DataGATE external signal control
 - Flexible clocking modes
 - Optional DualEDGE triggered registers
 - Clock divider (+ 2,4,6,8,10,12,14,16)
 - CoolCLOCK
 - Global signal options with macrocell control
 - Multiple global clocks with phase selection per macrocell
 - Multiple global output enables
 - Global set/reset
 - Abundant product term clocks, output enables and set/resets
 - Efficient control term clocks, output enables and set/resets for each macrocell and shared across function blocks
 - Advanced design security
 - Open-drain output option for Wired-OR and LED drive
 - Optional bus-hold, 3-state or weak pullup on select I/O pins
 - Optional configurable grounds on unused I/Os
 - Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels on all parts

- SSTL2_1, SSTL3_1, and HSTL_1 on 128 macrocell and denser devices
- Hot pluggable
- PLA architecture
 - Superior pinout retention
 - 100% product term routability across function block
- Wide package availability including fine pitch:
 - Chip Scale Package (CSP) BGA, Fine Line BGA, TQFP, PQFP, VQFP, and QFN packages
 - Pb-free available for all packages
- Design entry/verification using Xilinx and industry standard CAE tools
- Free software support for all densities using Xilinx® WebPACK™ tool
- Industry leading nonvolatile 0.18 micron CMOS process
 - Guaranteed 1,000 program/erase cycles
 - Guaranteed 20 year data retention

Family Overview

Xilinx CoolRunner™-II CPLDs deliver the high speed and ease of use associated with the XC9500/XL/XV CPLD family with the extremely low power versatility of the XPLA3 family in a single CPLD. This means that the exact same parts can be used for high-speed data communications/computing systems and leading edge portable products, with the added benefit of In System Programming. Low power consumption and high-speed operation are combined into a single family that is easy to use and cost effective. Clocking techniques and other power saving features extend the users' power budget. The design features are supported starting with Xilinx ISE® 4.1i WebPACK tool. Additional details can be found in [Further Reading](#), [page 14](#).

Table 1 shows the macrocell capacity and key timing parameters for the CoolRunner-II CPLD family.



Table 1: CoolRunner-II CPLD Family Parameters

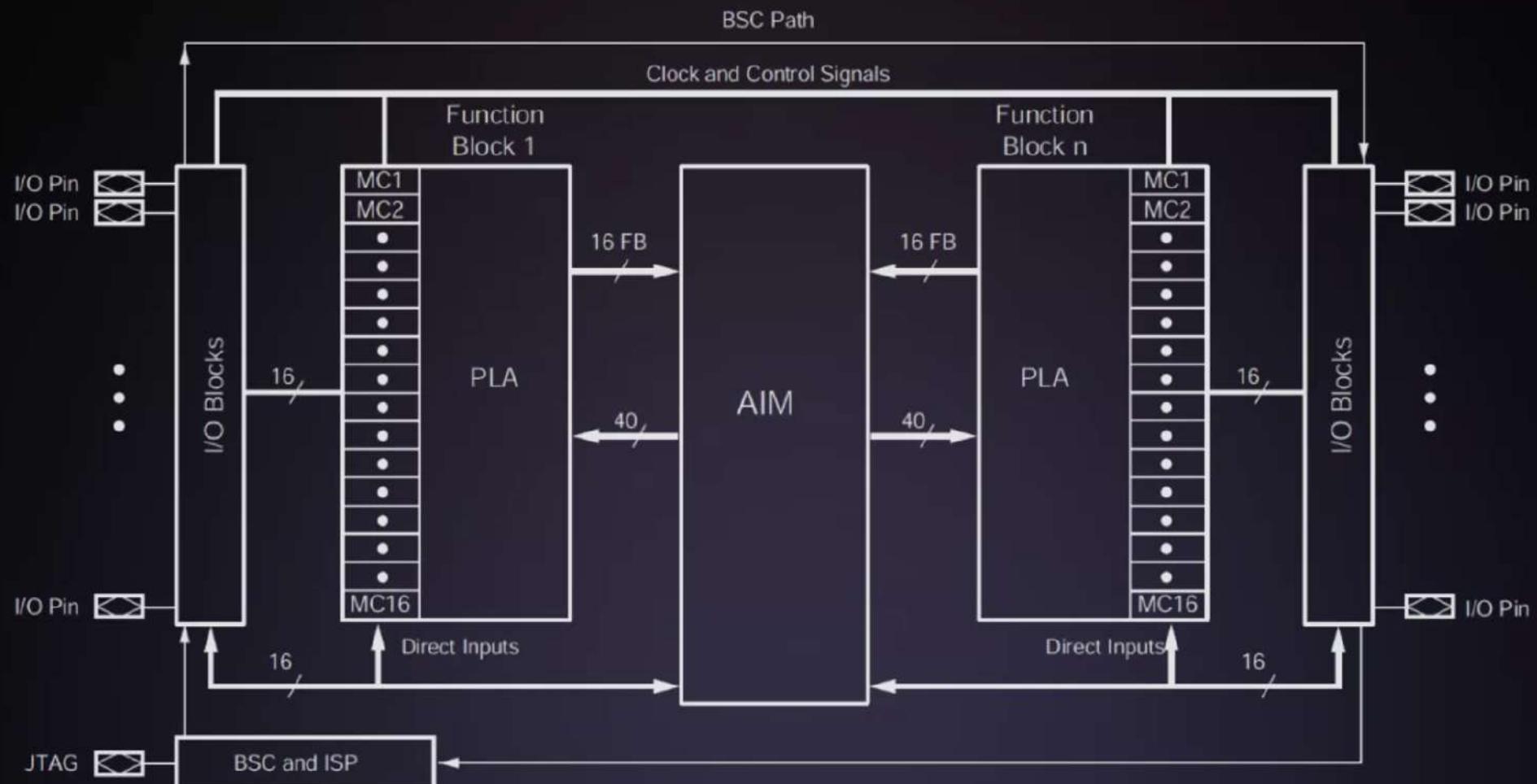
- Abundant product term clocks, output enables and set/resets
- Efficient control term clocks, output enables and set/resets for each macrocell and shared across function blocks
- Advanced design security
- Open-drain output option for Wired-OR and LED drive
- Optional bus-hold, 3-state or weak pullup on select I/O pins
- Optional configurable grounds on unused I/Os
- Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels on all parts

Table 1: CoolRunner-II CPLD Family Parameters

	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
Macrocells	32	64	128	256	384	512
Max I/O	33	64	100	184	240	270
T_{PD} (ns)	3.8	4.6	5.7	5.7	7.1	7.1
T_{SU} (ns)	1.9	2.0	2.4	2.4	2.9	2.6
T_{CO} (ns)	3.7	3.9	4.2	4.5	5.8	5.8
$F_{SYSTEM1}$ (MHz)	323	263	244	256	217	179

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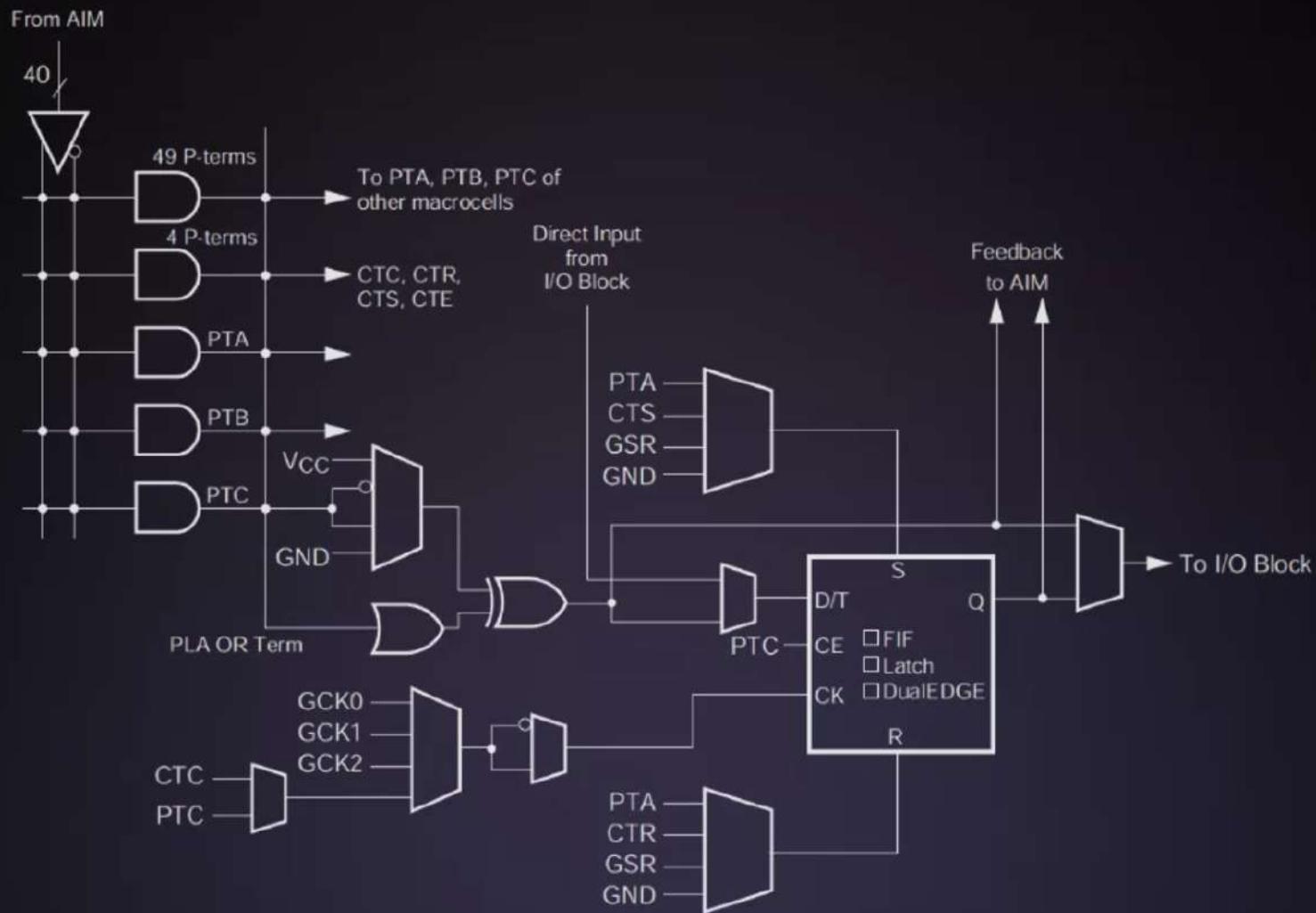




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Figure 1: CoolRunner-II CPLD Architecture

[5]

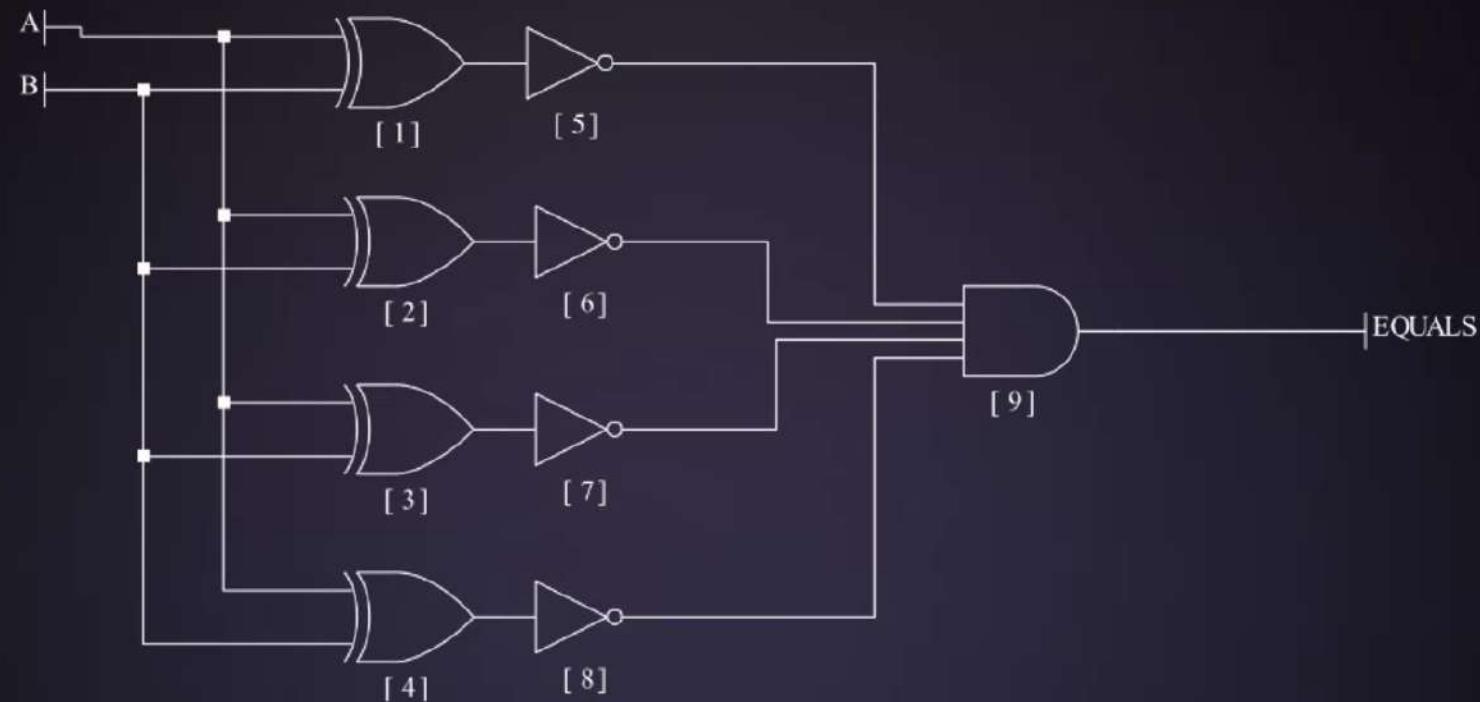


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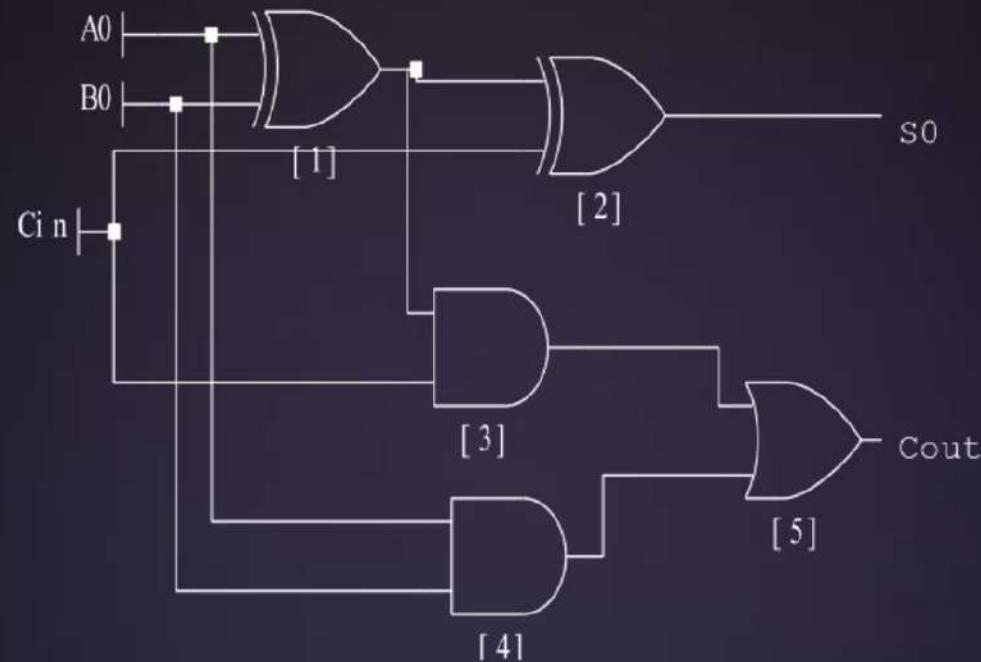
Figure 3: CoolRunner-II CPLD Macrocell

[6]

How large of a comparator in bits can be made using a XC95xx or CoolRunner II Macrocell?



How many full adders can be created in a XC9500XL or CoolRunner II Macrocell?



Xilinx CPLD Devices Summary



Xilinx offers 2 CPLD families, the XC9500XL and CoolRunner II. Both are reprogrammable, with deterministic timing and rich in I/O, but are limited in speed and logic density.

Xilinx CPLD Devices Summary



The XC9500XL family has 5 volt tolerant I/O, which can be important in industrial and automotive applications.

Xilinx CPLD Devices Summary



The CoolRunner II is a lower power CPLD family.

Xilinx CPLD Devices Summary



Xilinx CPLDs are efficient in implementation of comparators and decoders, but not efficient in implementation of adders or shift registers.

Introduction

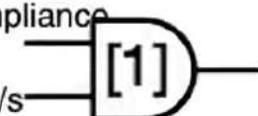
The Spartan®-3AN FPGA family combines the best attributes of a leading edge, low cost FPGA with nonvolatile technology across a broad range of densities. The family combines all the features of the Spartan-3A FPGA family plus leading technology in-system Flash memory for configuration and nonvolatile data storage.

The Spartan-3AN FPGAs are part of the Extended Spartan-3A family, which also includes the Spartan-3A FPGAs and the higher density Spartan-3A DSP FPGAs. The Spartan-3AN FPGA family is excellent for space-constrained applications such as blade servers, medical devices, automotive infotainment, telematics, GPS, and other small consumer products. Combining FPGA and Flash technology minimizes chip count, PCB traces and overall size while increasing system reliability.

The Spartan-3AN FPGA internal configuration interface is completely self-contained, increasing design security. The family maintains full support for external configuration. The Spartan-3AN FPGA is the world's first nonvolatile FPGA with MultiBoot, supporting two or more configuration files in one device, allowing alternative configurations for field upgrades, test modes, or multiple system configurations.

Features

- Buried configuration interface
- Unique Device DNA serial number in each device for design Authentication to prevent unauthorized copying
- Flash memory sector protection and lockdown
- Configuration watchdog timer automatically recovers from configuration errors
- Suspend mode reduces system power consumption
 - Retains all design state and FPGA configuration data
 - Fast response time, typically less than 100 μ s
- Full hot-swap compliance
- Multi-voltage, multi-standard SelectIO™ interface pins
 - Up to 502 I/O pins or 227 differential signal pairs
 - LVCMS, LVTTL, HSTL, and SSTL single-ended signal standards
 - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
 - Up to 24 mA output drive
 - $3.3V \pm 10\%$ compatibility and hot swap compliance
 - 622+ Mb/s data transfer rate per I/O
 - DDR/DDR2 SDRAM support up to 400 Mb/s
 - LVDS, RSDS, mini-LVDS, PPDS, and HSTL/SSTL



Features

- The new standard for low cost nonvolatile FPGA solutions
- Eliminates traditional nonvolatile FPGA limitations with the advanced 90 nm Spartan-3A device feature set
 - Memory, multipliers, DCMs, SelectIO, hot swap, power management, etc.
- Integrated robust configuration memory
 - Saves board space
 - Improves ease-of-use
 - Simplifies design
 - Reduces support issues
- Plentiful amounts of nonvolatile memory available to the user
 - Up to 11+ Mb available
 - MultiBoot support
 - Embedded processing and code shadowing
 - Scratchpad memory
- Robust 100K Flash memory program/erase cycles
- 20 years Flash memory data retention
- Security features provide bitstream anti-cloning protection

- LVDS, RSDS, mini-LVDS, PPDS, and HSTL/SSTL differential I/O
- Abundant, flexible logic resources
 - Densities up to 25,344 logic cells
 - Optional shift register or distributed RAM support
 - Enhanced 18 x 18 multipliers with optional pipeline
- Hierarchical SelectRAM™ memory architecture
 - Up to 576 Kbits of dedicated block RAM
 - Up to 176 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
- Eight global clocks and eight additional clocks per each half of device, plus abundant low-skew routing
- Complete Xilinx® [ISE®](#) and [WebPACK™](#) software development system support
- [MicroBlaze™](#) and [PicoBlaze™](#) embedded processor cores
- Fully compliant 32-/64-bit 33 MHz PCI™ technology support
- Low-cost QFP and BGA Pb-free (RoHS) packaging options
 - Pin-compatible with the same packages in the Spartan-3A FPGA family

Table 2: Summary of Spartan-3AN FPGA Attributes

Device	System Gates	Equivalent Logic Cells	CLBs	Slices	Distributed RAM Bits ⁽¹⁾	Block RAM Bits ⁽¹⁾	Dedicated Multipliers	DCMs	Maximum User I/O	Max Differential I/O Pairs	Bitstream Size ⁽¹⁾	In-System Flash Bits
XC3S50AN	50K	1,584	176	704	11K	54K	3	2	108	50	427K	1M ⁽²⁾
XC3S200AN	200K	4,032	448	1,792	28K	288K	16	4	195	90	1,168K	4M
XC3S400AN	400K	8,064	896	3,584	56K	360K	20	4	311	142	1,842K	4M
XC3S700AN	700K	13,248	1,472	5,888	92K	360K	20	8	372	165	2,669K	8M
XC3S1400AN	1400K	25,344	2,816	11,264	176K	576K	32	8	502	227	4,644K	[1]

Notes:

1. By convention, one Kb is equivalent to 1,024 bits and one Mb is equivalent to 1,024 Kb.

2. Maximum supported by Xilinx tools. See the customer notice [XCN14003: Flash Wafer Fabrication Change and Gold \(Au\) To Copper \(Cu\) Transition](#).

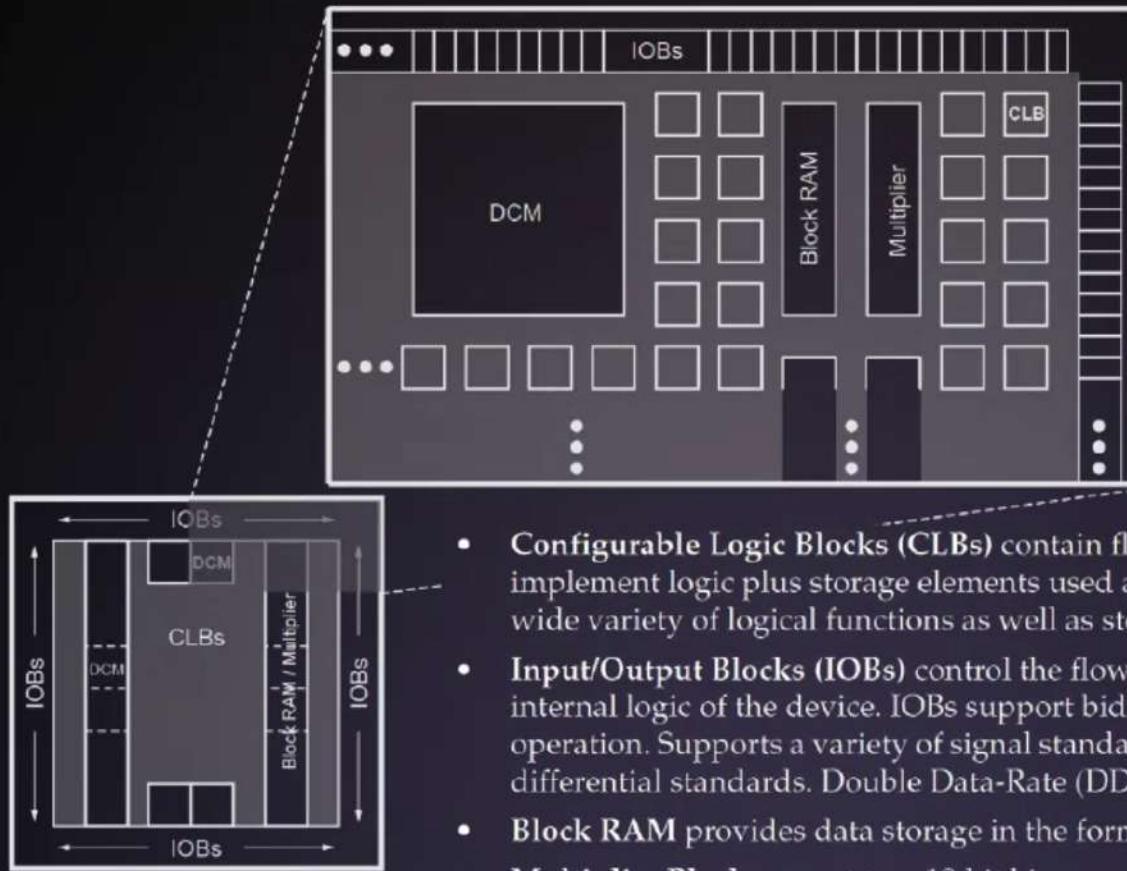
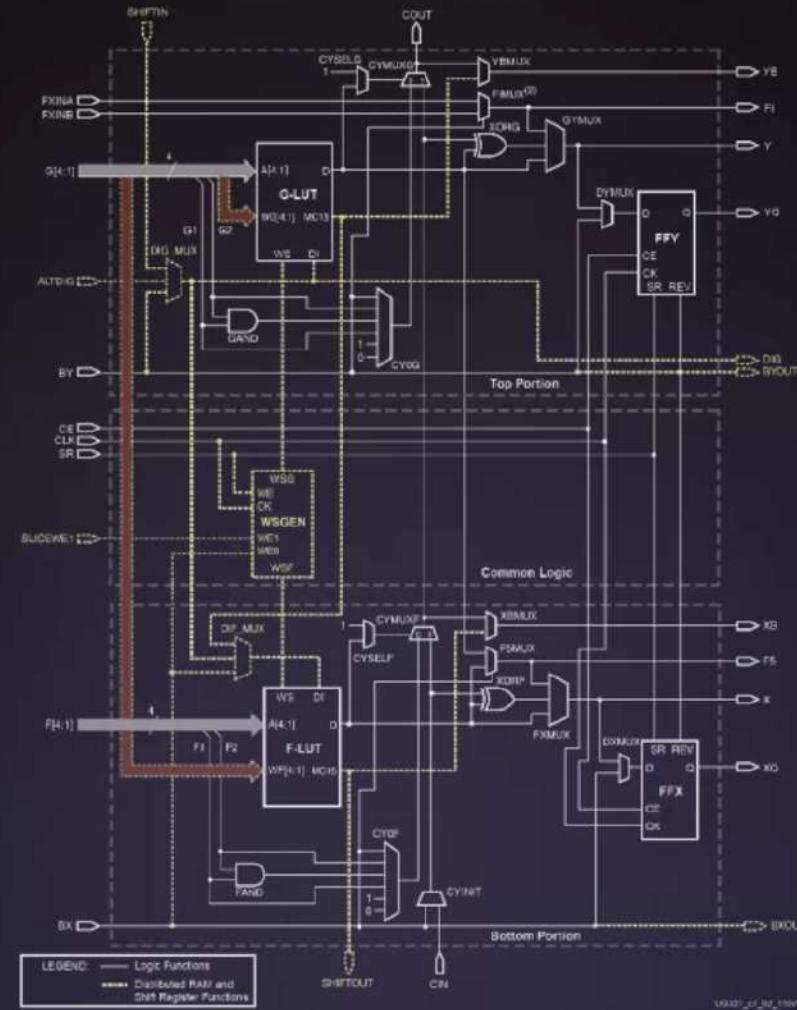


Figure 1-1:

[2]

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product. The Spartan-3A DSP platform includes special DSP multiply-accumulate blocks.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

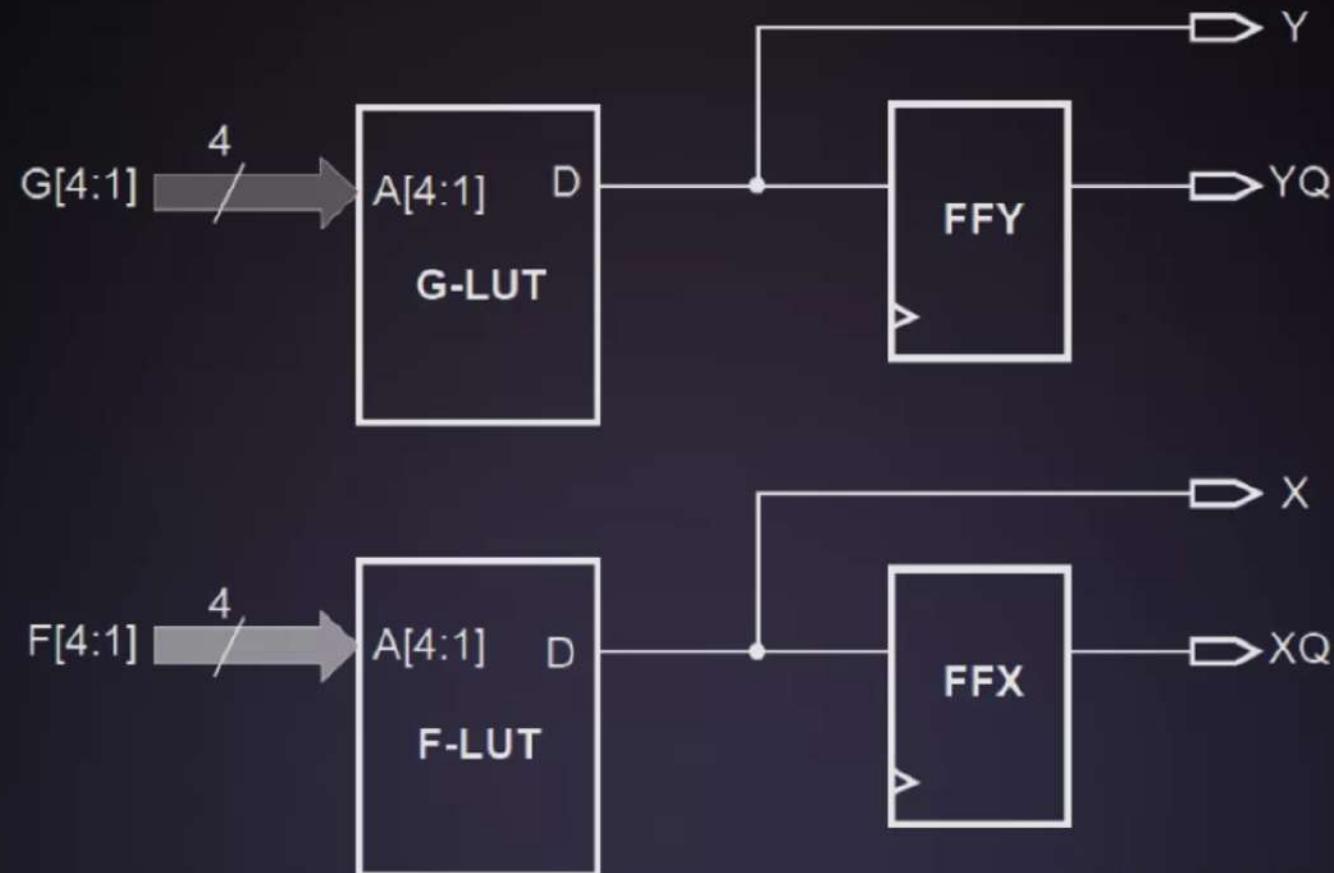


Notes:

1. Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
2. The index i can be 6, 7, or 8, depending on the slice. The upper SLICEL has an F8MUX, and the upper SLICEM has an F7MUX. The lower SLICEL and SLICEM both have an F6MUX.

Figure 5-2: Simplified Diagram of the Left-Hand SLICEM

[3]



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Figure 5-5: LUT Resources in a Slice

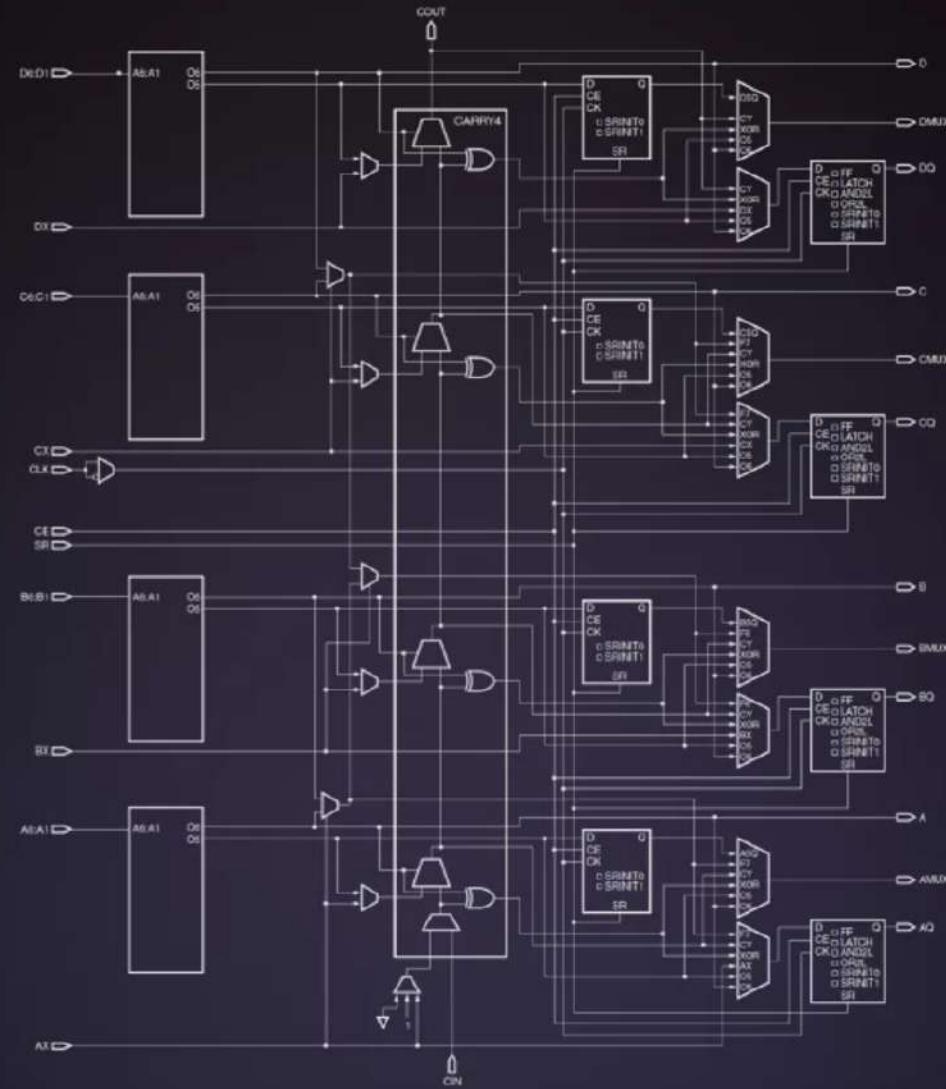
[4]

Spartan-6 FPGA Feature Summary

Table 1: Spartan-6 FPGA Feature Summary by Device

Device	Logic Cells ⁽¹⁾	Configurable Logic Blocks (CLBs)			DSP48A1 Slices ⁽³⁾	Block RAM Blocks		CMTs ⁽⁵⁾	Memory Controller Blocks (Max) ⁽⁶⁾	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices ⁽²⁾	Flip-Flops	Max Distributed RAM (Kb)		18 Kb ⁽⁴⁾	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,758	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358
XC6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	4	0	0	6	408
XC6SLX100	101,261	15,822	126,576	976	180	268	4,824	6	4	0	0	6	480
XC6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	4	0	0	6	576
XC6SLX25T	24,051	3,758	30,064	229	38	52	936	2	2	1	2	4	250
XC6SLX45T	43,661	6,822	54,576	401	58	116	2,088	4	2	1	4	4	296
XC6SLX75T	74,637	11,662	93,296	692	132	172	3,096	6	4	1	8	6	348
XC6SLX100T	101,261	15,822	126,576	976	180	268	4,824	6	4	1	8	6	498
XC6SLX150T	147,443	23,038	184,304	1,355	180	268	4,824	6	4	1	8	6	540

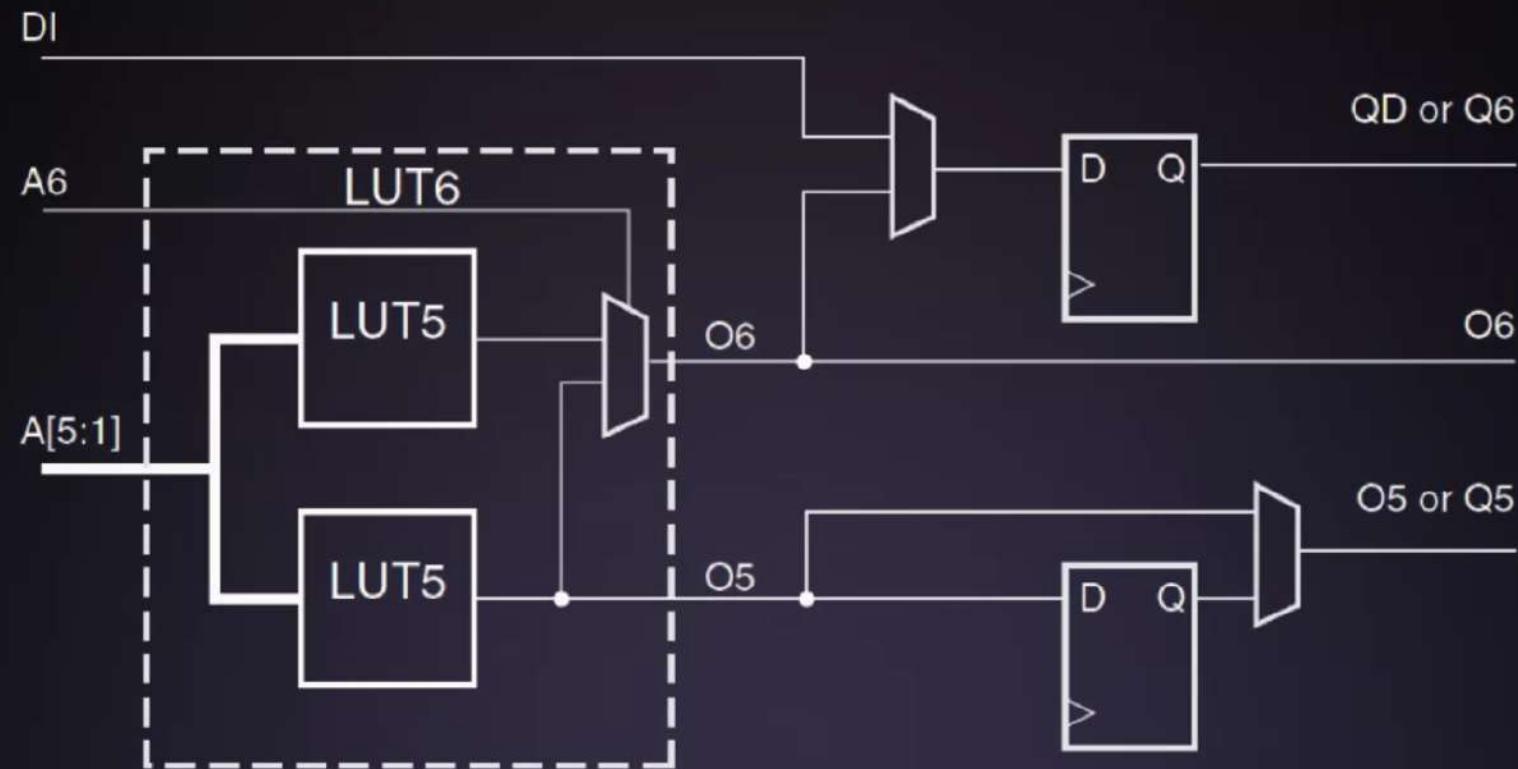




[6]

Figure 4: Diagram of SLICEL.

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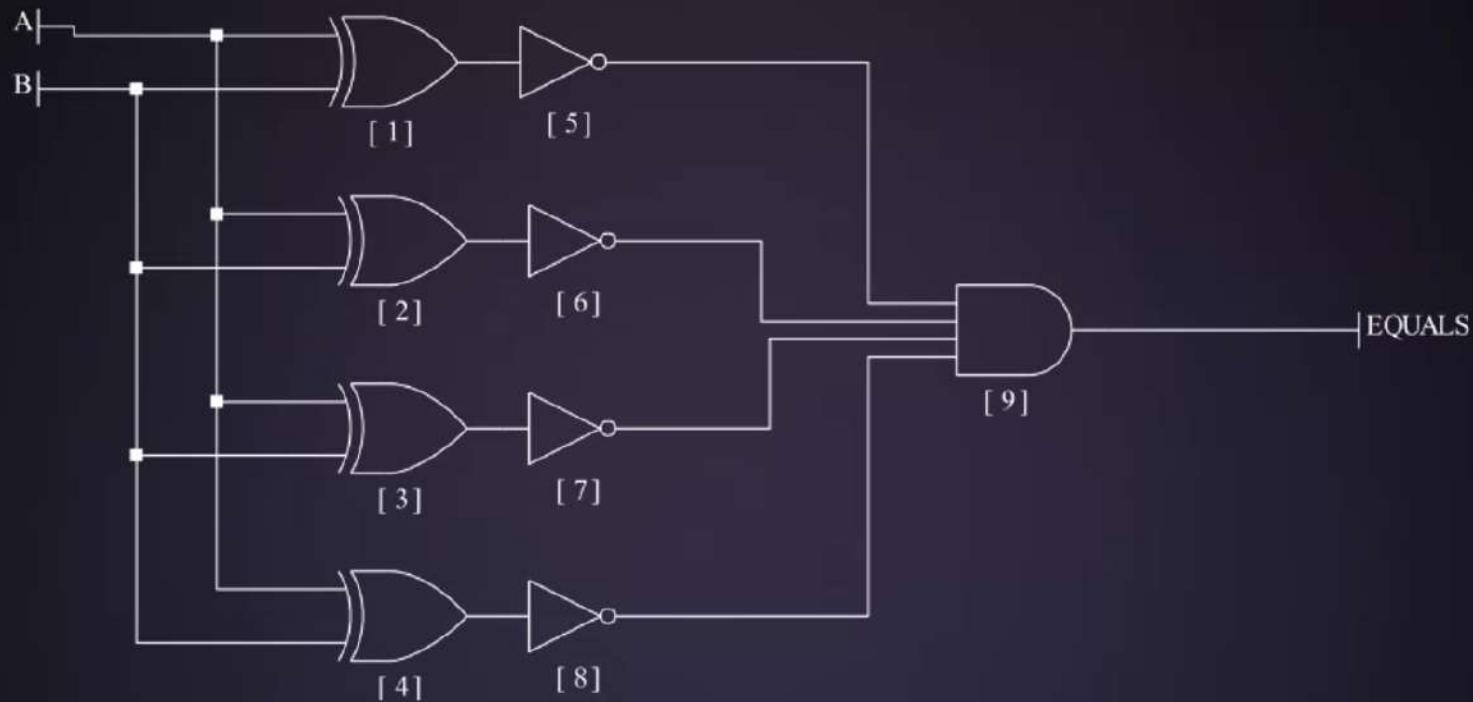


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Figure 6: LUT6

[7]

How large of a comparator in bits can be made using a Spartan Logic Cell?



How many full adders can be created in a Spartan logic cell?

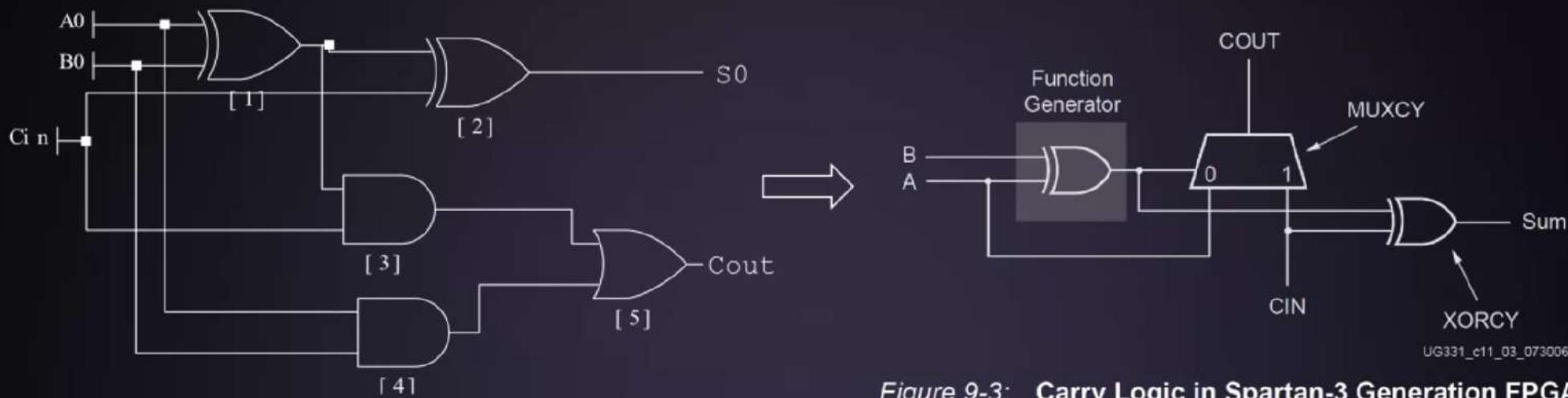


Figure 9-3: Carry Logic in Spartan-3 Generation FPGAs

[8]

Xilinx Small FPGAs Summary

Xilinx offers several smaller FPGA families, including the Spartan 3AN and Spartan 6 which are both currently available.

The Spartan 3AN uses on-chip FLASH configuration memory, so it a single-chip solution. The Spartan 6 uses SRAM configuration memory, so it needs an additional nonvolatile memory device to hold the configuration.

Xilinx Small FPGAs Summary

The Spartan 3AN has a logic cell based on a 4-input LUT and flip-flop, with additional logic to help efficiently create adders and shift registers. The Spartan 6 has a 6-input LUT with 2 flip-flops per logic cell.

Xilinx small FPGAs are more efficient in implementation of adders or shift registers than CPLDs.

Xilinx Small FPGAs Summary

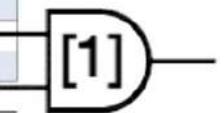
Xilinx small FPGAs include additional Hard IP blocks, including Multipliers and DSP, RAM blocks, Clock generation, and High-Speed Transceivers.

Artix-7 FPGAs

Artix®-7 FPGAs

Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth
(1.0V, 0.95V, 0.9V)

Artix®-7 FPGAs									
Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)									
	Part Number	XC7A12T	XC7A15T	XC7A25T	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280	52,160	75,520	101,440	215,360
	Slices	2,000	2,600	3,650	5,200	8,150	11,800	15,850	33,650
	CLB Flip-Flops	16,000	20,800	29,200	41,600	65,200	94,400	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400	600	892	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50	75	105	135	365
	Total Block RAM (Kb)	720	900	1,620	1,800	2,700	3,780	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5	5	6	6	10
I/O Resources	Maximum Single-Ended I/O	150	250	150	250	250	300	300	500
	Maximum Differential I/O Pairs	72	120	72	120	120	144	144	240
Embedded Hard IP Resources	DSP Slices	40	45	80	90	120	180	240	740
	PCIe® Gen2 ⁽¹⁾	1	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1
Speed Grades	GTP Transceivers (6.6 Gb/s Max Rate) ⁽²⁾	2	4	4	4	4	8	8	16
	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
Footprint Compatible	Industrial	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L
	Package ^{(3), (4)}	Dimensions (mm)	Ball Pitch (mm)	Available User I/O: 3.3V SelectIO™ HR I/O (GTP Transceivers)					
	CPG236	10 x 10	0.5	106 (2)	106 (2)	106 (2)	106 (2)	210 (0)	210 (0)
	CSG324	15 x 15	0.8		210 (0)	210 (0)	210 (0)	210 (0)	210 (0)
	CSG325	15 x 15	0.8	150 (2)	150 (4)	150 (4)	150 (4)		
Footprint Compatible	FTG256	17 x 17	1.0		170 (0)	170 (0)	170 (0)	170 (0)	170 (0)
	SBG484 / SBV484	19 x 19	0.8						285 (4)
	FGG484	23 x 23	1.0						
Footprint Compatible	FBG484 / FBV484	23 x 23	1.0						285 (4)
	FGG676	27 x 27	1.0					300 (8)	300 (8)
	FBG676 / FBV676	27 x 27	1.0						400 (8)
	FFG1156 / FFV1156	35 x 35	1.0						500 (16)



Kintex-7 FPGAs

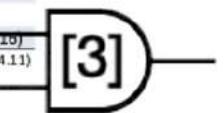
Optimized for Best Price-Performance
(1.0V, 0.95V, 0.9V)

	Part Number	XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
	EasyPath™ Cost Reduction Solutions ⁽¹⁾	—	—	XCE7K325T	XCE7K355T	XCE7K410T	XCE7K420T	XCE7K480T
Logic Resources	Slices	10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells	65,600	162,240	326,080	356,160	406,720	416,960	477,760
	CLB Flip-Flops	82,000	202,800	407,600	445,200	508,400	521,200	597,200
Memory Resources	Maximum Distributed RAM (kb)	838	2,188	4,000	5,088	5,663	5,938	6,788
	Block RAM/FIFO w/ ECC (36 Kb each)	135	325	445	715	795	835	955
	Total Block RAM (kb)	4,860	11,700	16,020	25,740	28,620	30,060	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)	6	8	10	6	10	8	8
I/O Resources	Maximum Single-Ended I/O	300	400	500	300	500	400	400
	Maximum Differential I/O Pairs	144	192	240	144	240	192	192
Integrated IP Resources	DSP48 Slices	240	600	840	1,440	1,540	1,680	1,920
	PCIe® Gen2 ⁽²⁾	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1
	GTx Transceivers (12.5 Gb/s Max Rate)	8	8	16	24	16	32	32
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial	-1, -2	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L
	Package ⁽³⁾	Available User I/O: 3.3V HR I/O, 1.8V HP I/Os (GTx)						
Footprint Compatible	FBG484 / FBV484	23 x 23	185, 100 (4)	185, 100 (4)				
	FBG676 / FBV676	27 x 27	200, 100 (8)	250, 150 (8)	250, 150 (8)	250, 150 (8)		
	FFG676 / FFV676	27 x 27		250, 150 (8)	250, 150 (8)	250, 150 (8)		
Footprint Compatible	FBG900 / FBV900	31 x 31		350, 150 (16)		350, 150 (16)		
	FFG900 / FFV900	31 x 31		350, 150 (16)		350, 150 (16)		
	FFG901 / FFV901	31 x 31			300, 0 (24)		380, 0 (28)	380, 0 (28)
	FFG1156 / FFV1156	35 x 35					400, 0 (32)	400, 0 (32)

[2]

Virtex-7 FPGAs

Optimized for Highest System Performance and Capacity (1.0V)													
		Part Number	XC7V58T	XC7V200T	XC7VX330T	XC7VX415T	XC7VX485T	XC7VX550T	XC7VX690T	XC7VX980T	XC7VX1140T	XC7VH580T	XC7VH870T
Logic Resources	EasyPath™ Cost Reduction Solutions ⁽¹⁾		XCE7V58T	—	XCE7VX330T	XCE7VX415T	XCE7VX485T	XCE7VX550T	XCE7VX690T	XCE7VX980T	—	—	—
	Slices	91,050	305,400	51,000	64,400	75,900	86,600	108,300	153,000	178,000	90,700	136,900	
	Logic Cells	582,720	1,954,560	326,400	412,160	485,760	554,240	693,120	979,200	1,139,200	580,480	876,160	
Memory Resources	CLB Flip-Flops	728,400	2,443,200	408,000	515,200	607,200	692,800	866,400	1,224,000	1,424,000	725,600	1,095,200	
	Maximum Distributed RAM (Kb)	6,938	21,550	4,388	6,525	8,175	8,725	10,888	13,838	17,700	8,850	13,275	
	Block RAM/FIFO w/ ECC (36 Kb each)	795	1,292	750	880	1,030	1,180	1,470	1,500	1,880	940	1,410	
Clocking	Total Block RAM (Kb)	28,620	46,512	27,000	31,680	37,080	42,480	52,920	54,000	67,680	33,840	50,760	
	CMTs (1 MMCM + 1 PLL)	18	24	14	12	14	20	20	18	24	12	18	
	Maximum Single-Ended I/O	850	1,200	700	600	700	600	1,000	900	1,100	600	300	
I/O Resources	Maximum Differential I/O Pairs	408	576	336	288	336	288	480	432	528	288	144	
	DSP Slices	1,260	2,160	1,120	2,160	2,800	2,880	3,600	3,600	3,360	1,680	2,520	
	PCIe® Gen2 ⁽²⁾	3	4	—	—	4	—	—	—	—	—	—	
Integrated IP Resources	PCIe Gen3	—	—	2	2	—	2	3	3	4	2	3	
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1	1	1	1	
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1	1	1	1	
Speed Grades	GTX Transceivers (12.5 Gb/s Max Rate) ⁽³⁾	36	36	—	—	56	—	—	—	—	—	—	
	GTH Transceivers (13.1 Gb/s Max Rate) ⁽⁴⁾	—	—	28	48	—	80	80	72	96	48	72	
	GTZ Transceivers (28.05 Gb/s Max Rate)	—	—	—	—	—	—	—	—	—	8	16	
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	
	Extended ⁽⁵⁾	-2L, -3	-2L, -2G	-2L, -3	-2L	-2L, -2G	-2L, -2G	-2L, -2G					
	Industrial	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1	—	—	
Package ⁽⁶⁾		Dimensions (mm)											
Available User I/O: 3.3V HR I/O, 1.8V HP I/Os (GTX, GTH)													
Footprint Compatible	FFG1157 / FFV1157 ⁽⁷⁾	35 x 35	0, 600 (20, 0)	0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (0, 20)	
	FFG1761 / FFV1761 ⁽⁷⁾	42.5 x 42.5	100, 750 (36, 0)	50, 650 (0, 28)	0, 700 (28, 0)	0, 850 (0, 36)	0, 850 (0, 36)	0, 850 (0, 36)	0, 850 (0, 36)	0, 850 (0, 36)	0, 850 (0, 36)	0, 850 (0, 36)	
	FHG1761	45 x 45	0, 850 (36, 0)	0, 850 (36, 0)	0, 850 (36, 0)	0, 850 (36, 0)	0, 850 (36, 0)	0, 850 (36, 0)	0, 850 (36, 0)	0, 850 (36, 0)	0, 850 (36, 0)	0, 850 (36, 0)	
Footprint Compatible	FLG1925	45 x 45	0, 1200 (16, 0)	0, 1200 (16, 0)	0, 1200 (16, 0)	0, 1200 (16, 0)	0, 1200 (16, 0)	0, 1200 (16, 0)	0, 1200 (16, 0)	0, 1200 (16, 0)	0, 1200 (16, 0)	0, 1200 (16, 0)	
	FFG1158 / FFV1158 ⁽⁷⁾	35 x 35	0, 350 (0, 48)	0, 350 (48, 0)	0, 350 (0, 48)	0, 350 (0, 48)	0, 350 (0, 48)	0, 350 (0, 48)	0, 350 (0, 48)	0, 350 (0, 48)	0, 350 (0, 48)	0, 350 (0, 48)	
	FFG1926	45 x 45	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	
Footprint Compatible	FLG1926	45 x 45	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	0, 720 (0, 64)	
	FFG1927 / FFV1927 ⁽⁷⁾	45 x 45	0, 600 (0, 48)	0, 600 (56, 0)	0, 600 (0, 80)	0, 600 (0, 80)	0, 600 (0, 80)	0, 600 (0, 80)	0, 600 (0, 80)	0, 600 (0, 80)	0, 600 (0, 80)	0, 600 (0, 80)	
	FLG1928	45 x 45	0, 480 (0, 72)	0, 480 (0, 72)	0, 480 (0, 72)	0, 480 (0, 72)	0, 480 (0, 72)	0, 480 (0, 72)	0, 480 (0, 72)	0, 480 (0, 72)	0, 480 (0, 72)	0, 480 (0, 72)	
Footprint Compatible	FFG1930	45 x 45	0, 700 (24, 0)	0, 1000 (0, 24)	0, 900 (0, 24)	0, 1000 (0, 24)	0, 900 (0, 24)	0, 1000 (0, 24)	0, 900 (0, 24)	0, 1000 (0, 24)	0, 1100 (0, 24)	0, 1100 (0, 24)	
	FLG1930	45 x 45	0, 1100 (0, 24)	0, 1100 (0, 24)	0, 1100 (0, 24)	0, 1100 (0, 24)	0, 1100 (0, 24)	0, 1100 (0, 24)	0, 1100 (0, 24)	0, 1100 (0, 24)	0, 1100 (0, 24)	0, 1100 (0, 24)	
	FLG1155	35 x 35	400 (24, 8)	600 (48, 8)	600 (48, 8)	600 (48, 8)	600 (48, 8)	600 (48, 8)	600 (48, 8)	600 (48, 8)	600 (48, 8)	600 (48, 8)	
Footprint Compatible	FLG1931	45 x 45	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	
	FLG1932	45 x 45	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	300 (72, 10)	



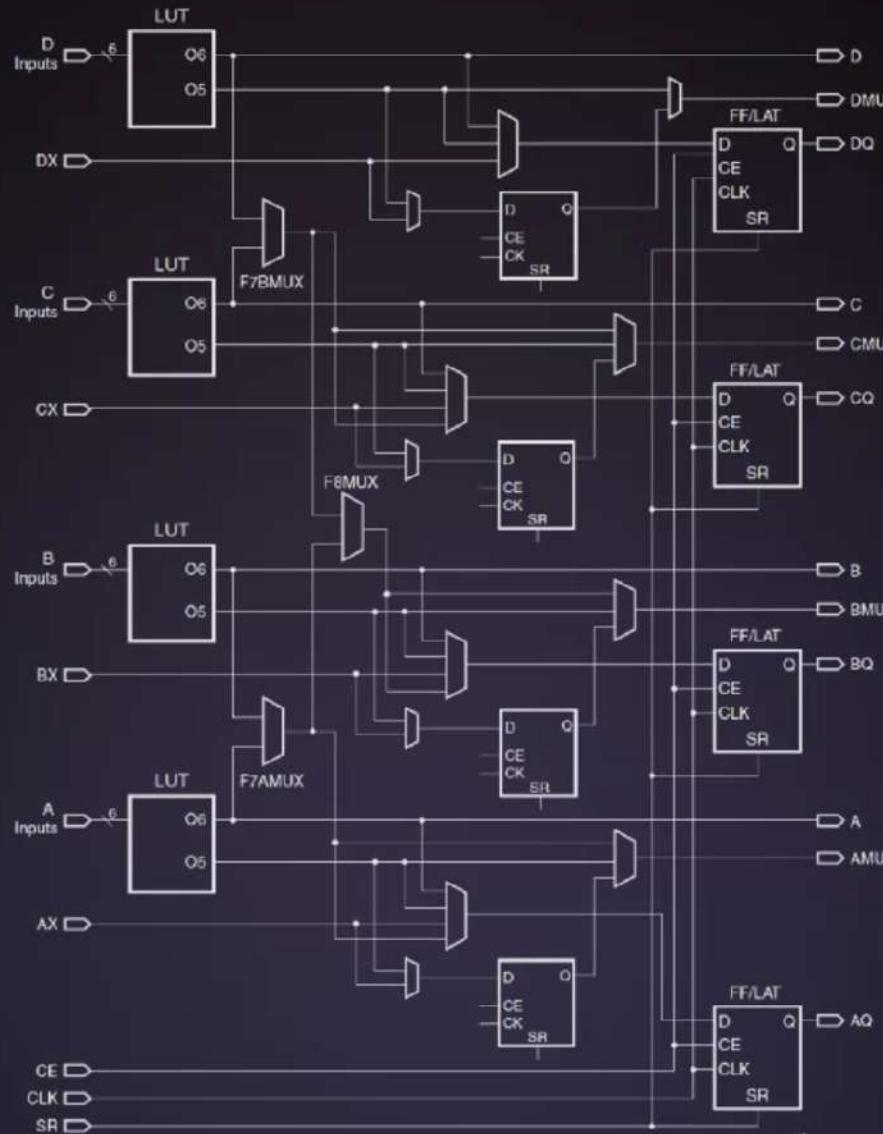


Figure 5-1: Simplified 7 Series FPGA Slice

UG74_05_01_00210

Kintex® UltraScale™ FPGAs

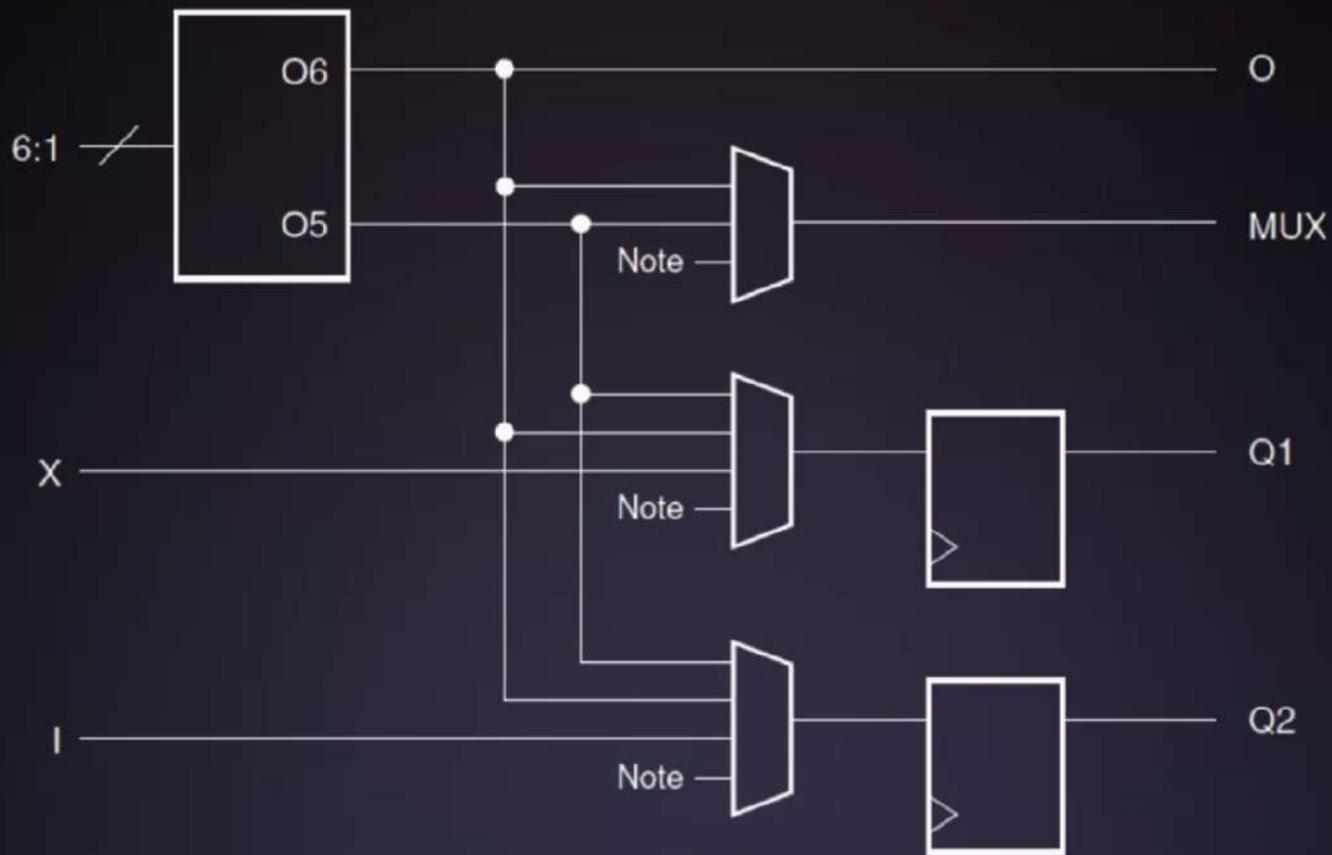
	Device Name	KU025 ⁽¹⁾	KU035	KU040	KU060	KU085	KU095	KU115
Logic Resources	System Logic Cells (K)	318	444	530	726	1,088	1,176	1,451
	CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
	CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
Memory Resources	Maximum Distributed RAM (Kb)	4,230	5,908	7,050	9,180	13,770	4,800	18,360
	Block RAM/FIFO w/ECC (36Kb each)	360	540	600	1,080	1,620	1,680	2,160
	Block RAM/FIFO (18Kb each)	720	1,080	1,200	2,160	3,240	3,360	4,320
Total Block RAM (Mb)		12.7	19.0	21.1	38.0	56.9	59.1	75.9
Clock Resources	CMT (1 MMCM, 2 PLLs)	6	10	10	12	22	16	24
	I/O DLL	24	40	40	48	56	64	64
I/O Resources	Maximum Single-Ended HP I/Os	208	416	416	520	572	650	676
	Maximum Differential HP I/O Pairs	96	192	192	240	264	288	312
	Maximum Single-Ended HR I/Os	104	104	104	104	104	52	156
	Maximum Differential HR I/O Pairs	48	48	48	48	56	24	72
Integrated IP Resources	DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520
	System Monitor	1	1	1	1	2	1	2
	PCIe® Gen1/2/3	1	2	3	3	4	4	6
	Interlaken	0	0	0	0	0	2	0
	100G Ethernet	0	0	0	0	0	2	0
Speed Grades	16.3Gb/s Transceivers (GTH/GTY)	12	16	20	32	56	64 ⁽²⁾	64
	Commercial	-1	-1	-1	-1	-1	-1	-1
	Extended	-2	-2 -3	-2 -3	-2 -3	-2 -3	-2	-2 -3
Industrial		-1 -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -2	-1 -1L -2



Virtex® UltraScale™ FPGAs

	Device Name	XCVU065	XCVU080	XCVU095	XCVU125	XCVU160	XCVU190	XCVU440
Logic Resources	System Logic Cells (K)	783	975	1,176	1,567	2,027	2,350	5,541
	CLB Flip-Flops	716,160	891,424	1,075,200	1,432,320	1,852,800	2,148,480	5,065,920
	CLB LUTs	358,080	445,712	537,600	716,160	926,400	1,074,240	2,532,960
Memory Resources	Maximum Distributed RAM (Kb)	4,830	3,980	4,800	9,660	12,690	14,490	28,710
	Block RAM/FIFO w/ECC (36Kb each)	1,260	1,421	1,728	2,520	3,276	3,780	2,520
	Block RAM/FIFO (18Kb each)	2,520	2,842	3,456	5,040	6,552	7,560	5,040
Clock Resources	Total Block RAM (Mb)	44.3	50.0	60.8	88.6	115.2	132.9	88.6
	CMT (1 MMCM, 2 PLLs)	10	16	16	20	28	30	30
	I/O DLL	40	64	64	80	120	120	120
I/O Resources	Transceiver Fractional PLL	5	8	8	10	13	15	0
	Maximum Single-Ended HP I/Os	468	780	780	780	650	650	1,404
	Maximum Differential HP I/O Pairs	216	360	360	360	300	300	648
Integrated IP Resources	Maximum Single-Ended HR I/Os	52	52	52	52	52	52	52
	Maximum Differential HR I/O Pairs	24	24	24	24	24	24	24
	DSP Slices	600	672	768	1,200	1,560	1,800	2,880
Speed Grades	System Monitor	1	1	1	2	3	3	3
	PCIe® Gen1/2/3	2	4	4	4	4	6	6
	Interlaken	3	6	6	6	8	9	0
Speed Grades	100G Ethernet	3	4	4	6	9	9	3
	GTH 16.3Gb/s Transceivers	20	32	32	40	52	60	48
	GTy 30.5Gb/s Transceivers	20	32	32	40	52	60	0
Speed Grades	Commercial	-	-	-	-	-	-	-1
	Extended	-1H-2-3	-1H-2-3	-1H-2-3	-1H-2-3	-1H-2-3	-1H-2-3	-2-3
	Industrial	-1-2	-1-2	-1-2	-1-2	-1-2	-1-2	-1-2





Note: MUX inputs include carry and wide multiplexers (not shown)

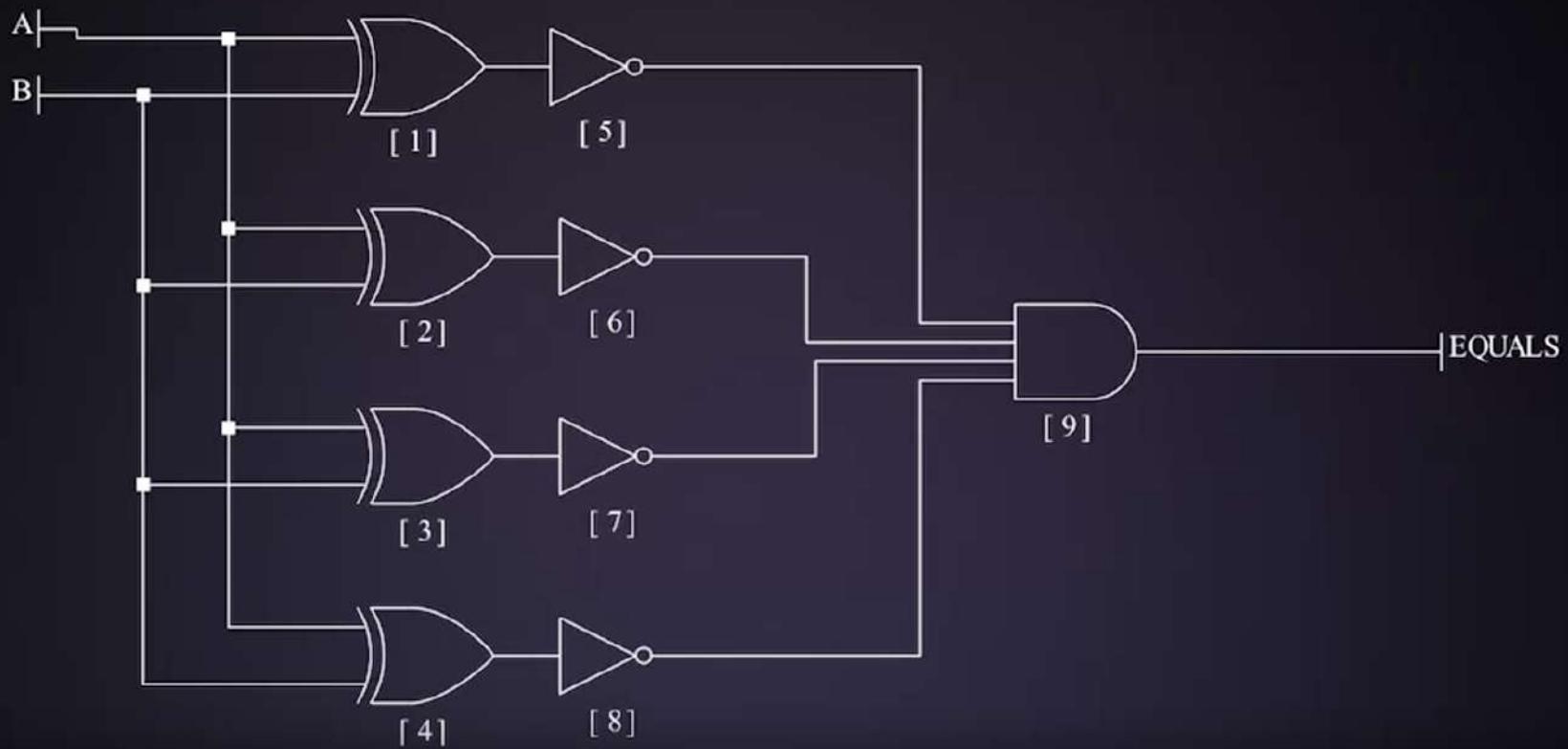
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Figure 1-2: A Simplified View of Slice I/O Connecting to a LUT and Storage Elements [7]

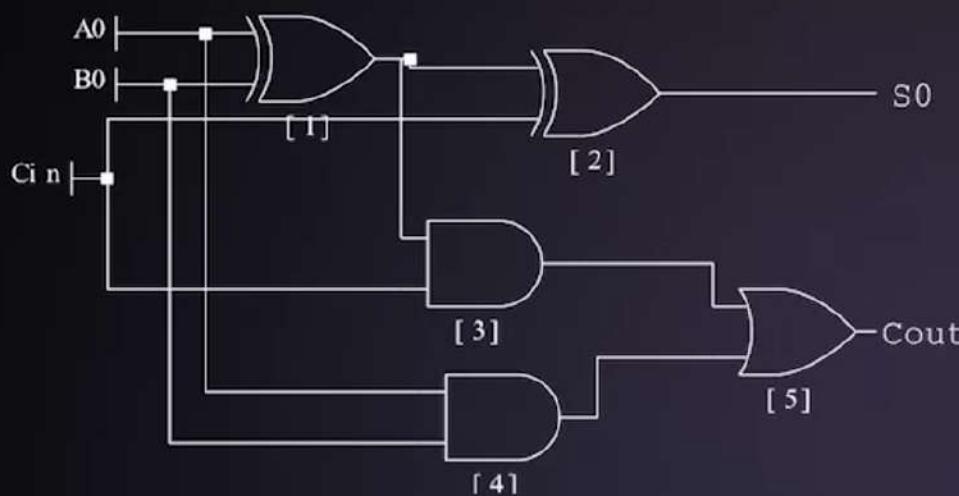
Xilinx Summary

www.xilinx.com/products/silicon-devices/fpga.html

How large of a comparator in bits can be made using a Virtex Ultrascale Logic Cell?



How many full adders can be created in a Virtex Ultrascale logic cell?



OR

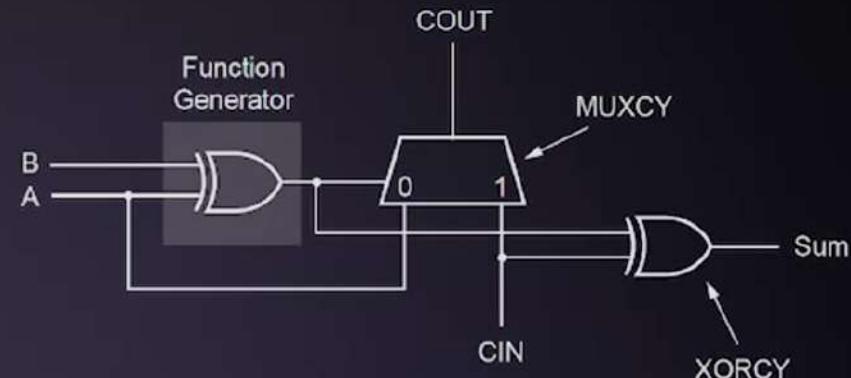


Figure 9-3: Carry Logic in Spartan-3 Generation FPGAs

[8]

Xilinx Large FPGAs Summary

Xilinx offers several large FPGA families, including the Artix-7, Kintex-7, and Virtex-7 as well as the Kintex Ultrascale and Virtex Ultrascale. These are large devices with up to 5 million logic cells.

Speed has increased greatly with these large FPGAs, with internal clock trees running up to 850 MHz and Transceivers at 30 Gbps with aggregate bandwidth of 3.66 Tbps.

Xilinx Large FPGAs Summary

Xilinx large FPGAs are rich in added hard IP blocks, which include Memory, PLLs, DSP, PCIe Gen 1/2/3 Transceivers, 100G Ethernet Interface, and even 12 bit ADCs in some cases.

Table 1-1. MAX V Family Features

Feature	5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
LEs	40	80	160	240	570	1,270	2,210
Typical Equivalent Macrocells	32	64	128	192	440	980	1,700
User Flash Memory Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192	8,192
Global Clocks	4	4	4	4	4	4	4
Internal Oscillator	1	1	1	1	1	1	1
Maximum User I/O pins	54	79	79	114	159	271	271
t_{PD1} (ns) (1)	7.5	7.5	7.5	7.5	9.0	6.2	7.0
f_{CNT} (MHz) (2)	152	152	152	152	152	304	304
t_{SU} (ns)	2.3	2.3	2.3	2.3	2.2	1.2	1.2
t_{CO} (ns)	6.5	6.5	6.5	6.5	6.7	4.6	4.6

Figure 2–6. LE for MAX V Devices

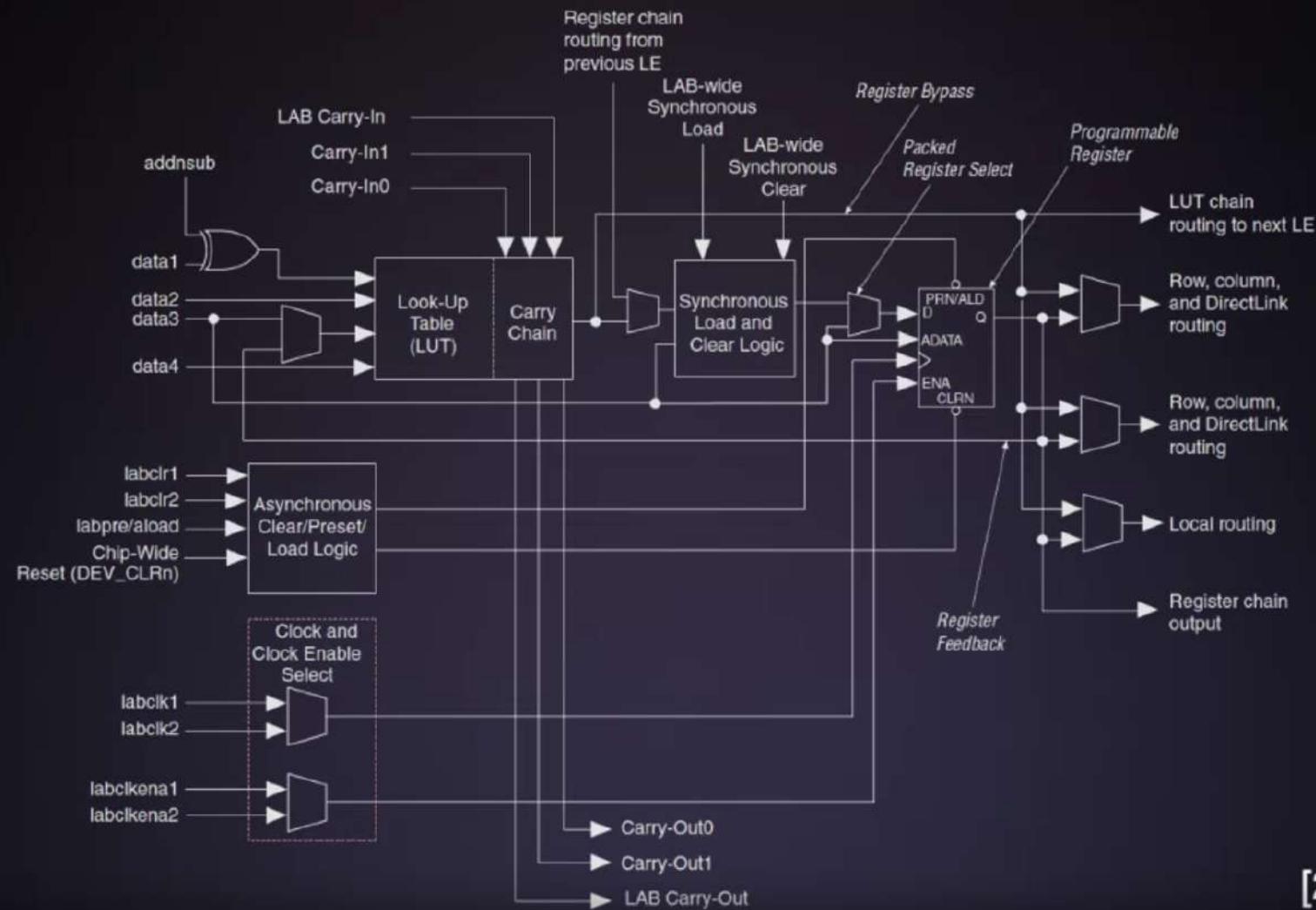
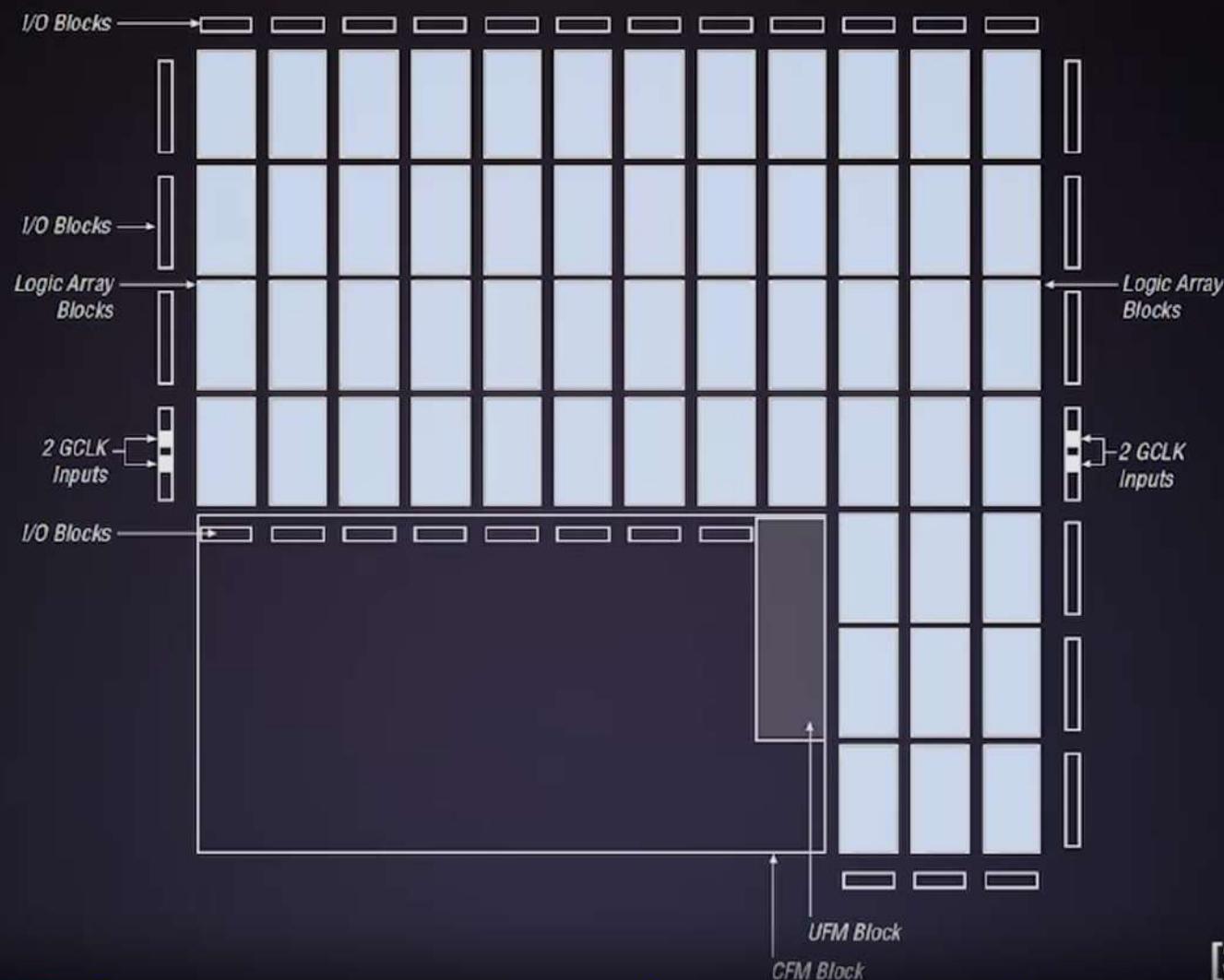


Figure 2–2. Device Floorplan for MAX V Devices



Altera Max10 Floorplan

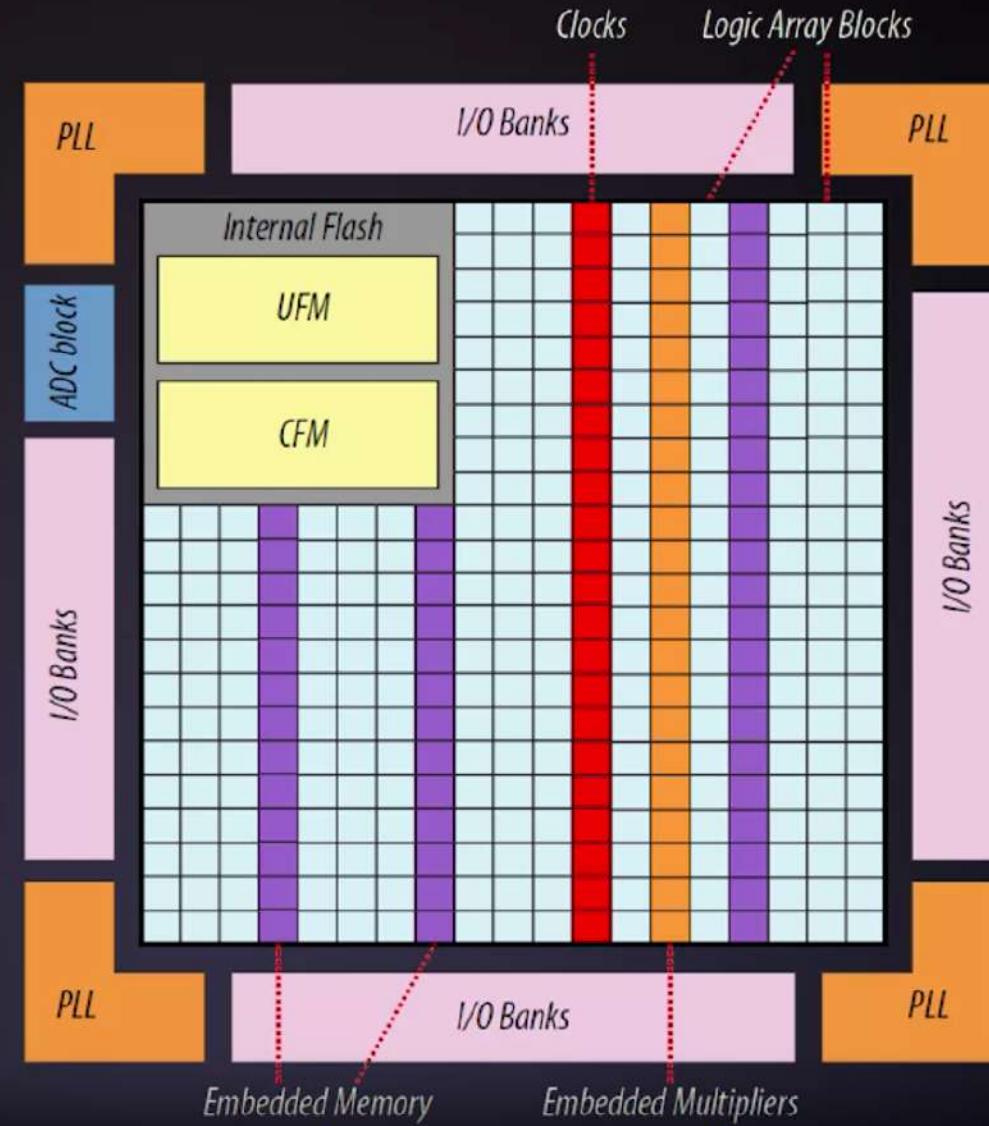
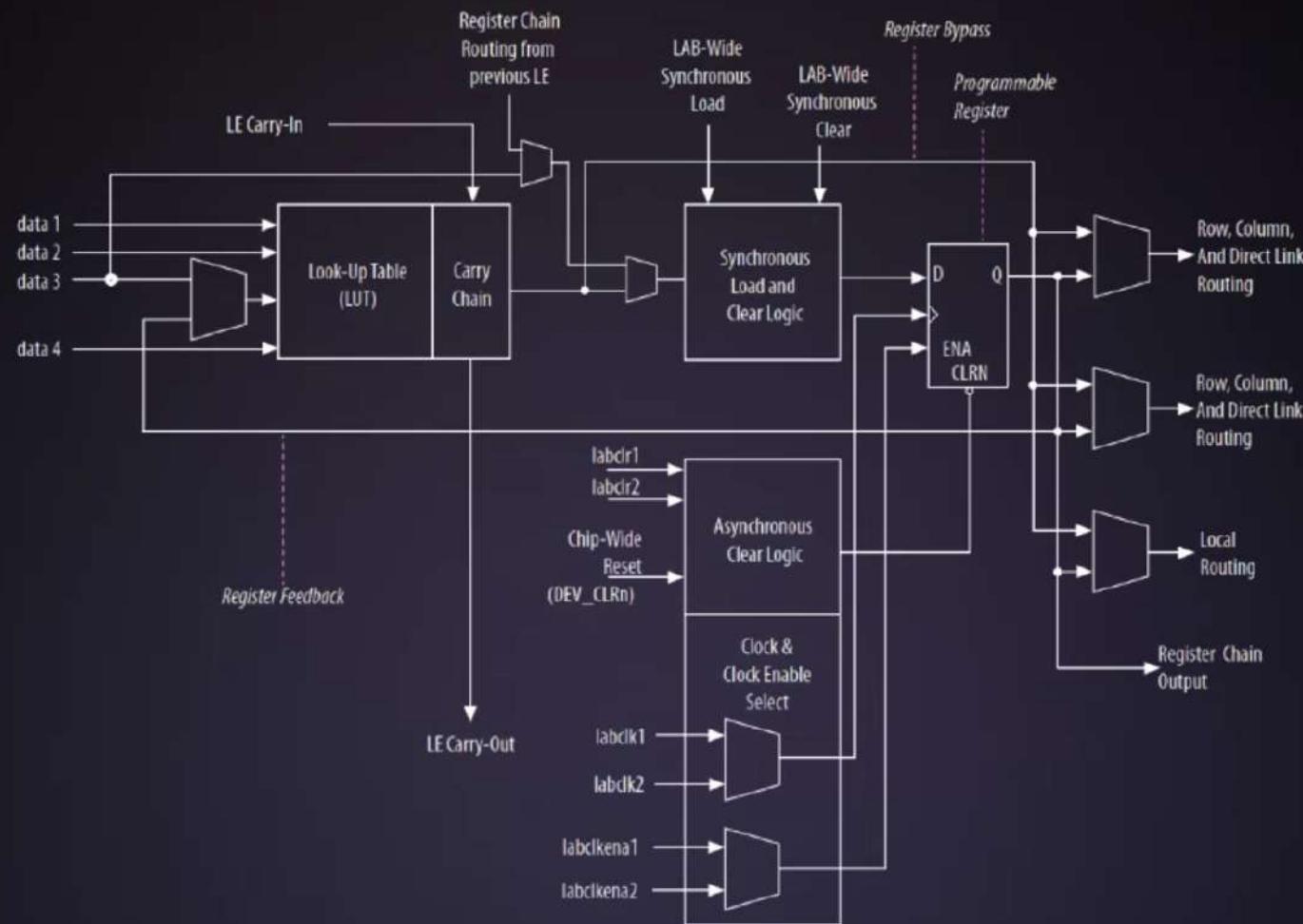


Figure 5: LE High-Level Block Diagram for MAX 10 Devices.



MAX 10 FPGAs Product Table

Product Line	10M02	10M04	10M08	10M16	10M25	10M40	10M50
LEs (K)	2	4	8	16	25	40	50
Block memory (Kb)	108	189	378	549	675	1,260	1,638
User flash memory ¹ (KB)	12	16 – 156	32 – 172	32 – 296	32 – 400	64 – 736	64 – 736
18 x 18 multipliers	16	20	24	45	55	125	144
PLLs ²	1, 2	1, 2	1, 2	1, 4	1, 4	1, 4	1, 4
Internal configuration	Single	Dual	Dual	Dual	Dual	Dual	Dual
Analog-to-digital converter (ADC), temperature sensing diode (TSD) ³	-	1, 1	1, 1	1, 1	2, 1	2, 1	2, 1
External memory interface (EMIF)	Yes ⁴	Yes ⁴	Yes ⁴	Yes ⁵	Yes ⁵	Yes ⁵	Yes ⁵

Package Options and I/O Pins: Feature Set Options, GPIO, True LVDS Transceiver/Receiver

V36 (D) ⁶	WLCSP (3 mm, 0.4 mm pitch)	C, 27, 3/7	-	-	-	-	-
V81 (D) ⁷	WLCSP (4 mm, 0.4 mm pitch)	-	-	C/F, 56, 7/17	-	-	-
F256 (D)	FBGA (17 mm, 1.0 mm pitch)	-	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54
U324 (D)	UBGA (15 mm, 0.8 mm pitch)	C, 160, 9/47	C/A, 246, 15/81	C/A, 246, 15/81	C/A, 246, 15/81	-	-
F484 (D)	FBGA (23 mm, 1.0 mm pitch)	-	-	C/A, 250, 15/83	C/A, 320, 22/116	C/A, 360, 24/136	C/A, 360, 24/136
F672 (D)	FBGA (27 mm, 1.0 mm pitch)	-	-	-	-	C/A, 500, 30/192	C/A, 500, 30/192
E144 (S) ⁶	EQFP (22 mm, 0.5 mm pitch)	C, 101, 7/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/28	C/A, 101, 10/28
M153 (S)	MBGA (8 mm, 0.5 mm pitch) ⁸	C, 112, 9/29	C/A, 112, 9/29	C/A, 112, 9/29	-	-	-
U169 (S)	UBGA (11 mm, 0.8 mm pitch)	C, 130, 9/38	C/A, 130, 9/38	C/A, 130, 9/38	C/A, 130, 9/38	-	-

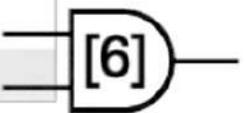
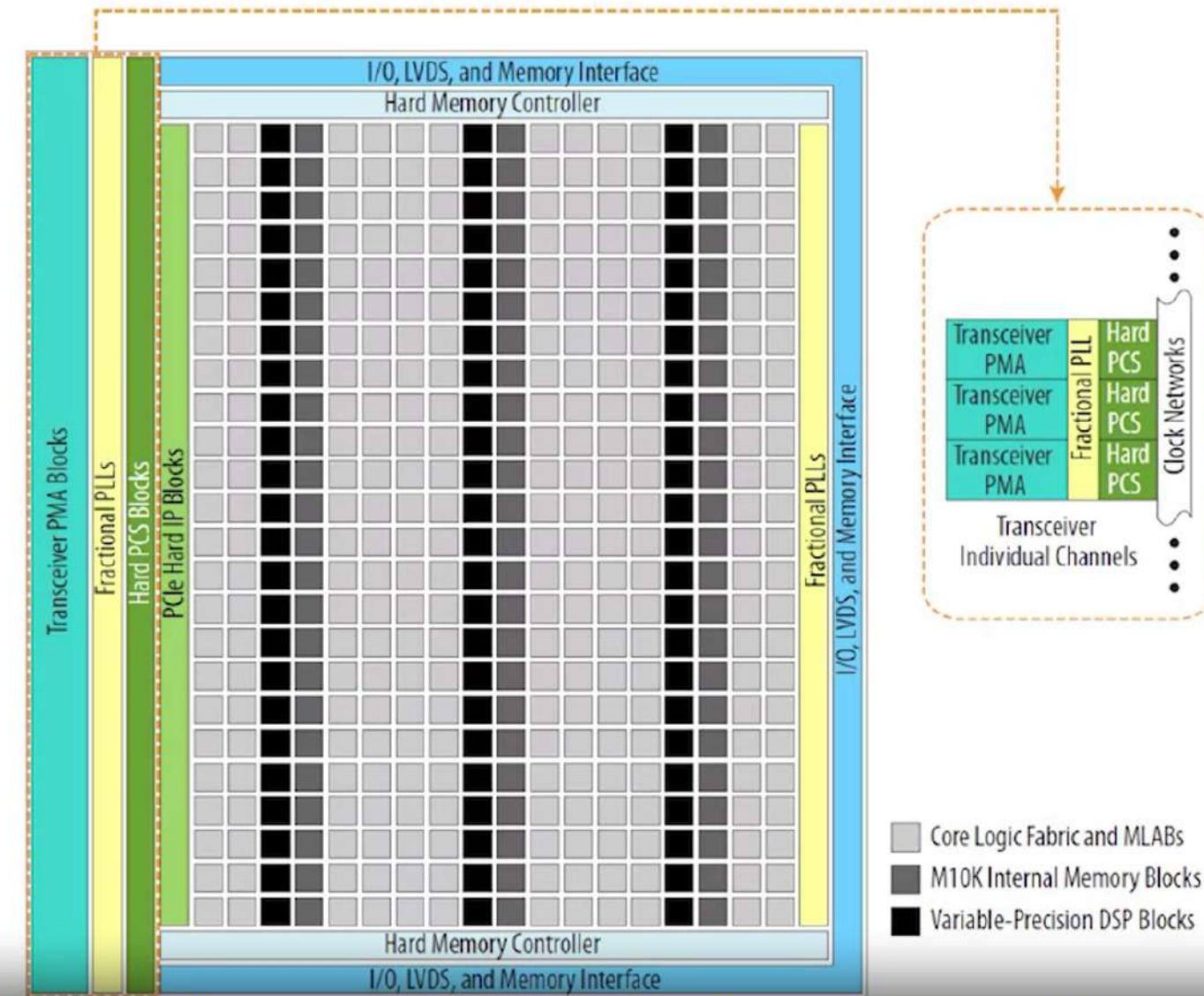


Table 4: Maximum Resource Counts for Cyclone V E Devices

Resource	Member Code				
	A2	A4	A5	A7	A9
Logic Elements (LE) (K)	25	49	77	150	301
ALM	9,434	18,480	29,080	56,480	113,560
Register	37,736	73,920	116,320	225,920	454,240
Memory (Kb)	M10K	1,760	3,080	4,460	6,860
	MLAB	196	303	424	836
Variable-precision DSP Block	25	66	150	156	342
18 x 18 Multiplier	50	132	300	312	684
PLL	4	4	6	7	8



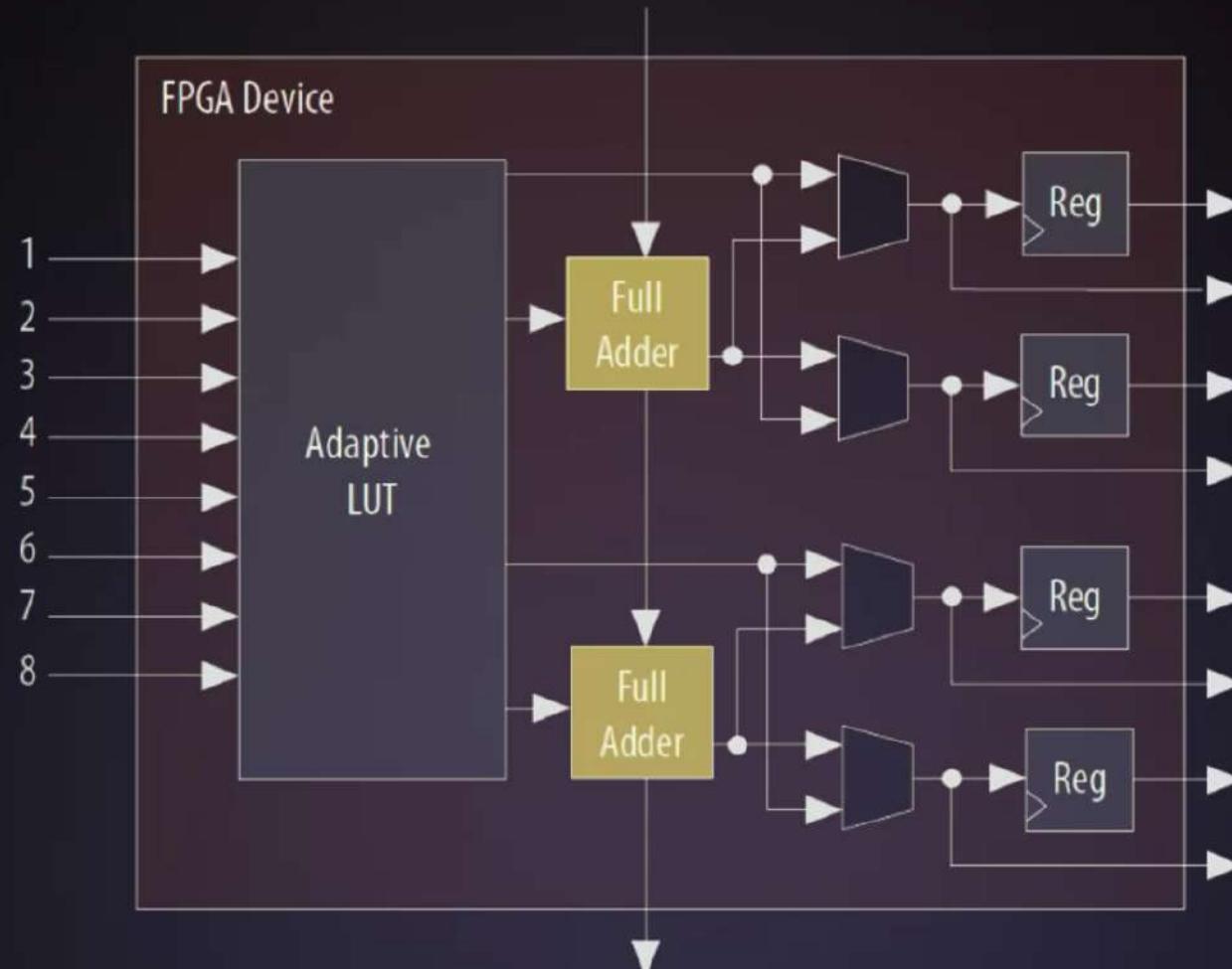
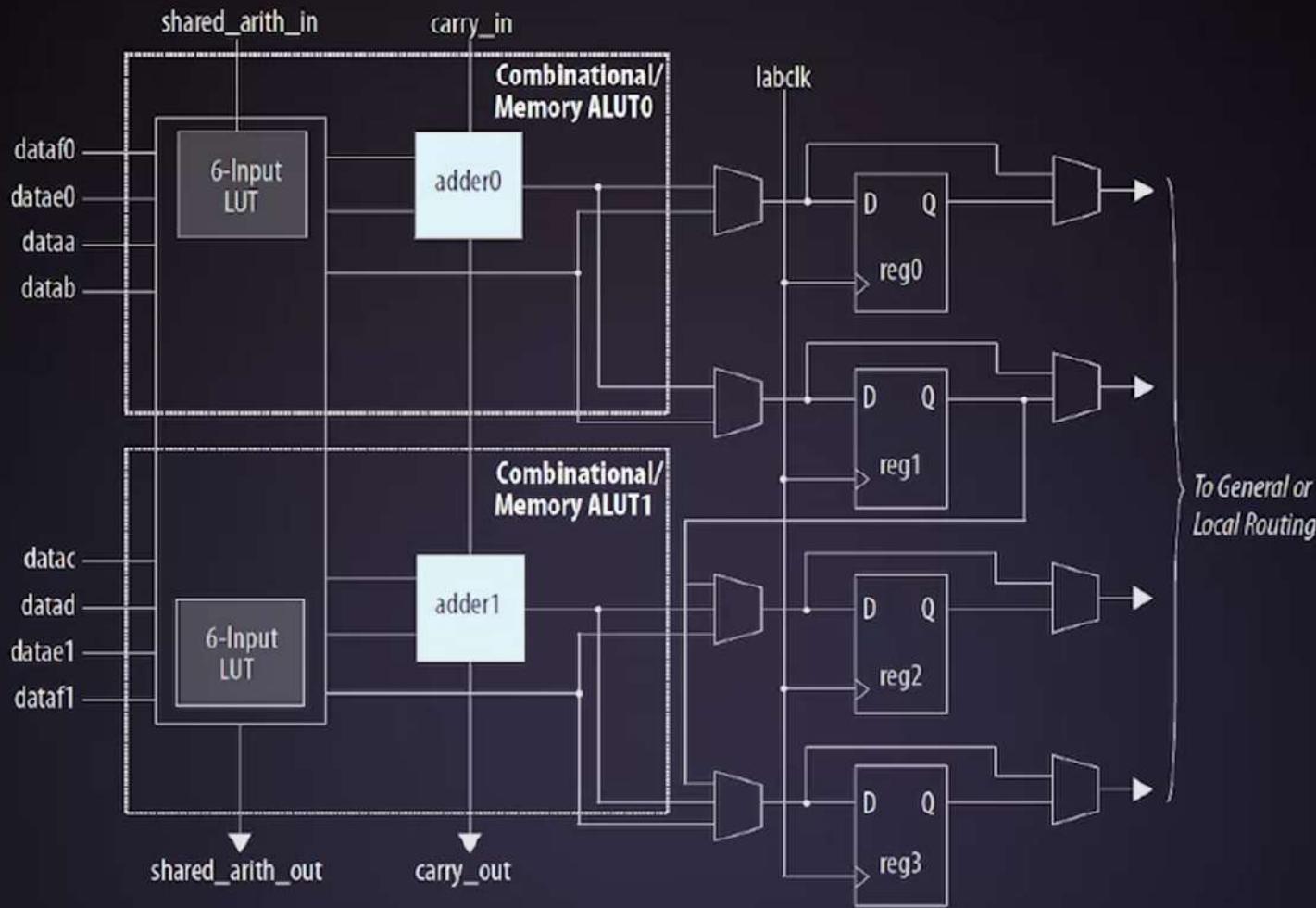
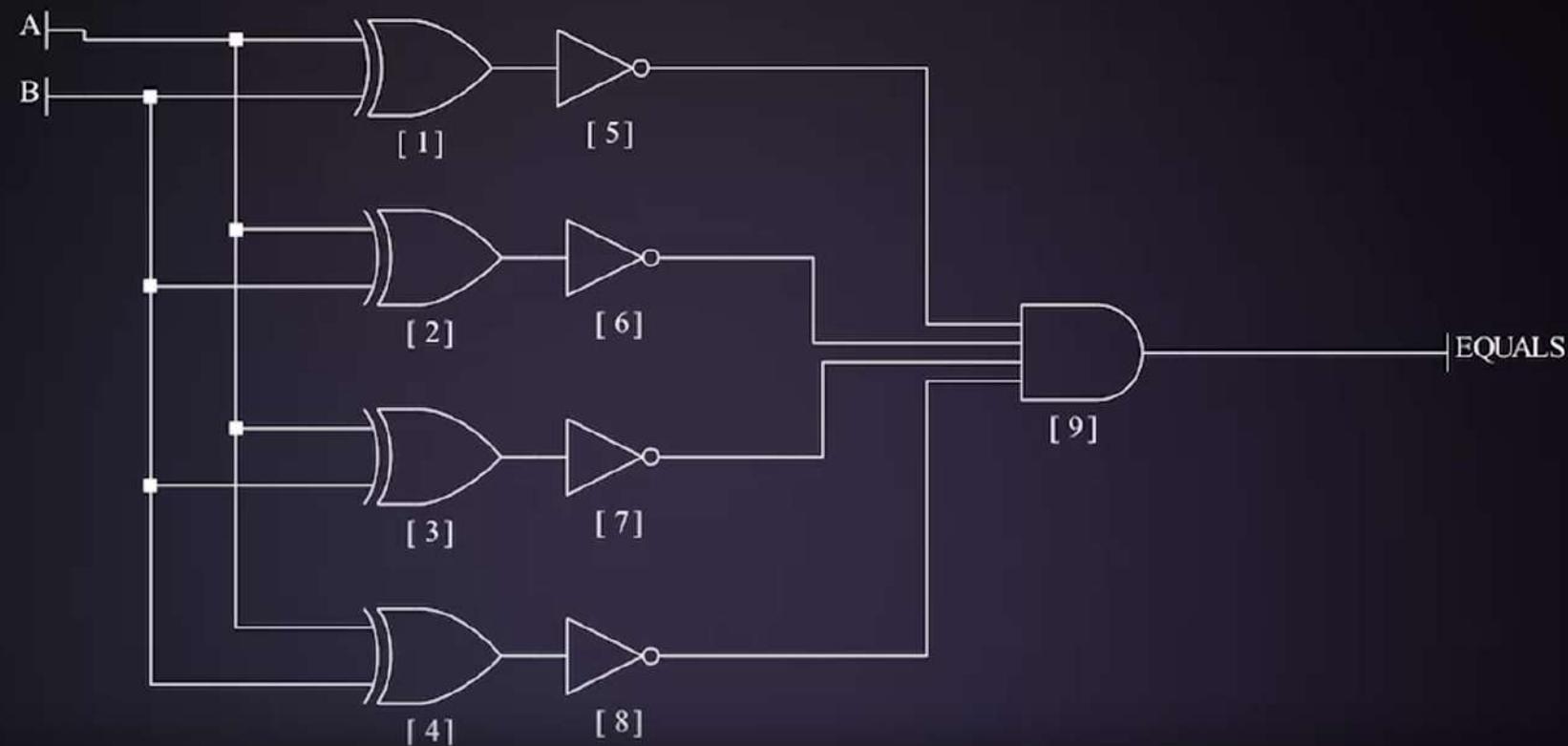


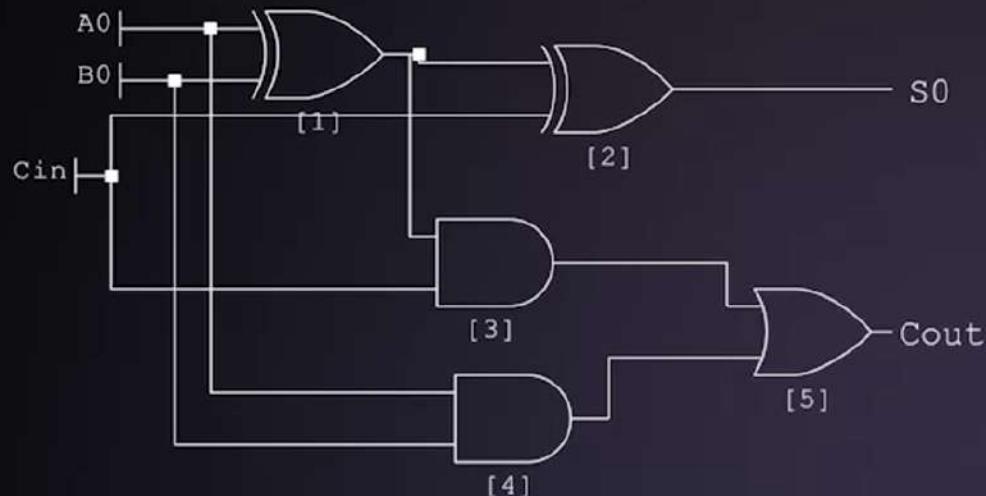
Figure 1-7: ALM High-Level Block Diagram for Arria V GX, GT, SX, and, ST Devices



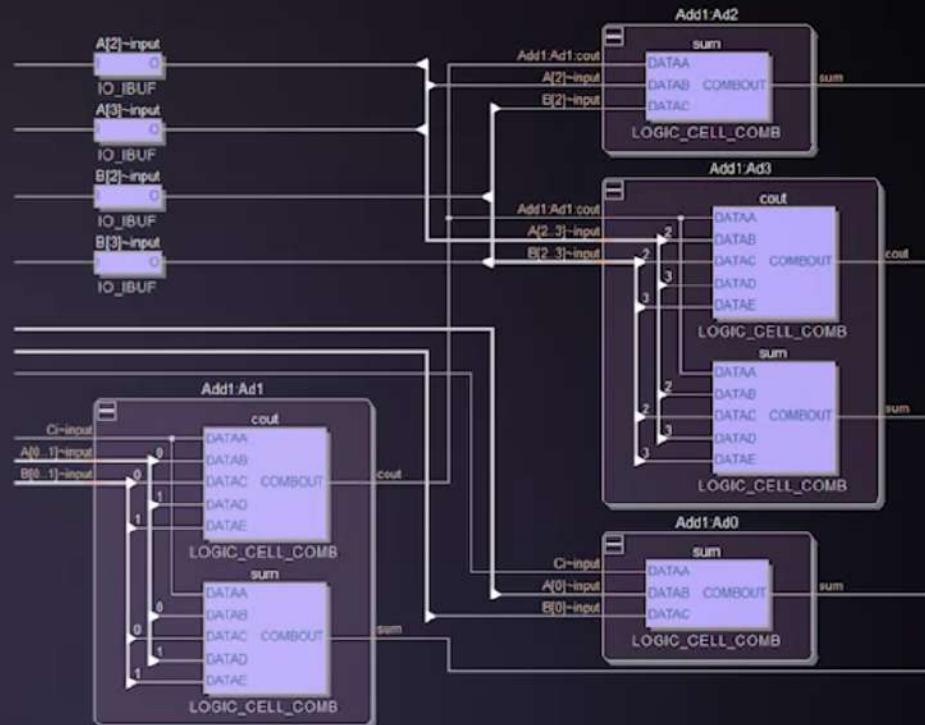
How large of a comparator can be made using a MAX 10 or Cyclone V Logic Cell?



How many full adders can be created in a MAX 10 or Cyclone V logic cell?



1 bit full adder



4 bit adder in 3 ALMs

Altera CPLDs and Small FPGAs Summary

Altera offers the MAX V CPLD and MAX 10 and Cyclone V FPGA families for smaller logic designs.

The MAX V and MAX 10 are single chip solutions with more I/O combined with reasonable logic density and efficient 4-input LUT logic cells.

The MAX 10 adds analog signal processing via an on-chip ADC.

Altera CPLDs and Small FPGAs Summary

The Cyclone V is a good entry level FPGA with good speed and logic density combined with a considerable amount of hard IP blocks, including Block memory, PLLs, Multipliers and DSP blocks, High Speed Transceivers and External Memory Interfaces.

Table 4: Maximum Resource Counts for Arria V GX Devices

Resource		Member Code						
		A1	A3	A5	A7	B1	B3	B5
Logic Elements (LE) (K)		75	156	190	242	300	362	420
ALM		28,302	58,900	71,698	91,680	113,208	136,880	158,491
Register		113,208	235,600	286,792	366,720	452,832	547,520	633,964
Memory (Kb)	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540
	MLAB	463	961	1,173	1,448	1,852	2,098	2,532
Variable-precision DSP Block		240	396	600	800	920	1,045	1,092
6 Gbps Transceiver		9	9	24	24	24	24	36
GPIO ⁽³⁾		416	416	544	544	704	704	704
LVD S	Transmitter	67	67	120	120	160	160	160
	Receiver	80	80	136	136	176	176	176
PCIe Hard IP Block		1	1	2	2	2	2	2
Hard Memory Controller		2	2	4	4	4	4	4

Figure 9: Device Chip Overview for Arria V GX and GT Devices

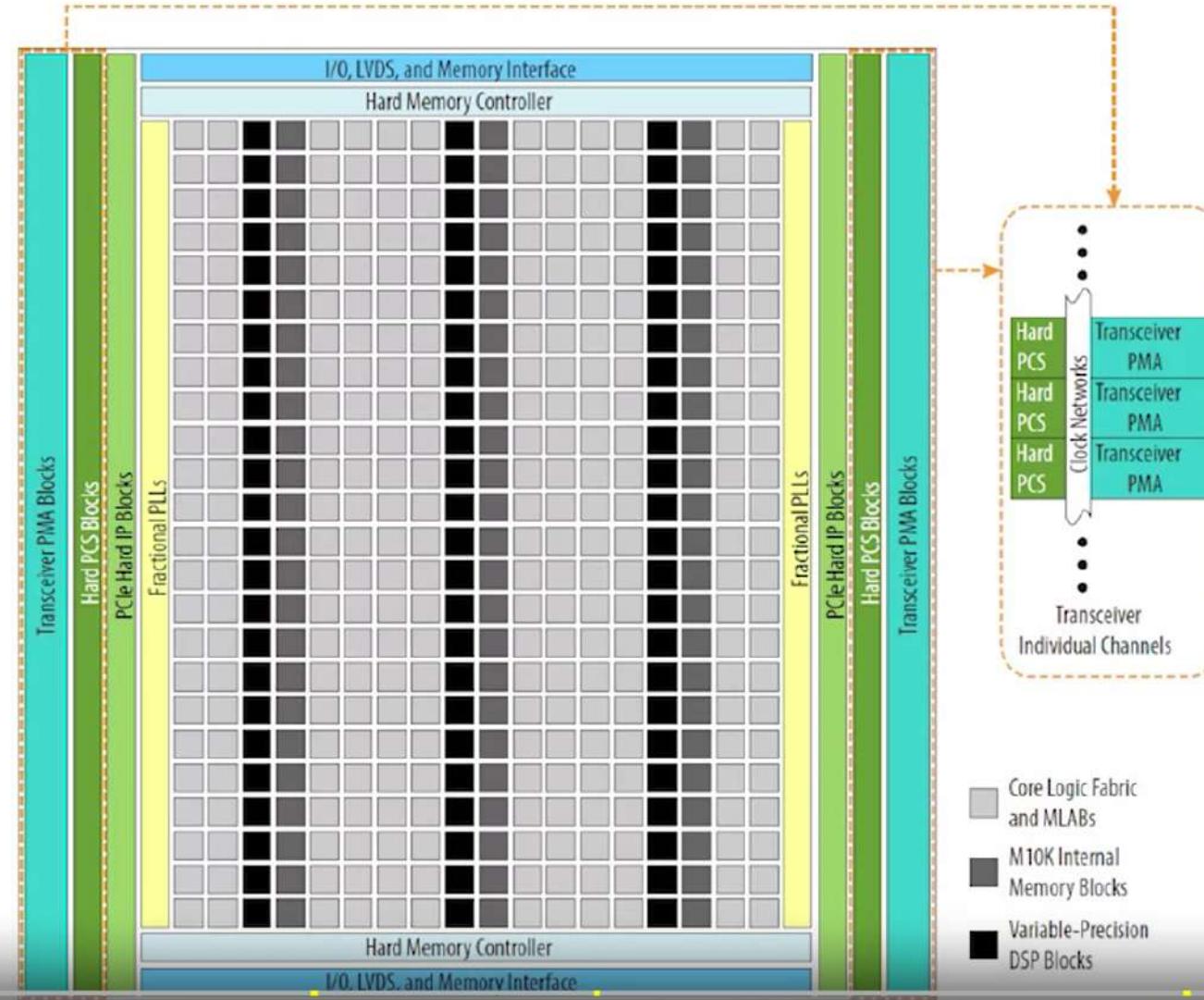


Figure 1-7: ALM High-Level Block Diagram for Arria V GX, GT, SX, and, ST Devices

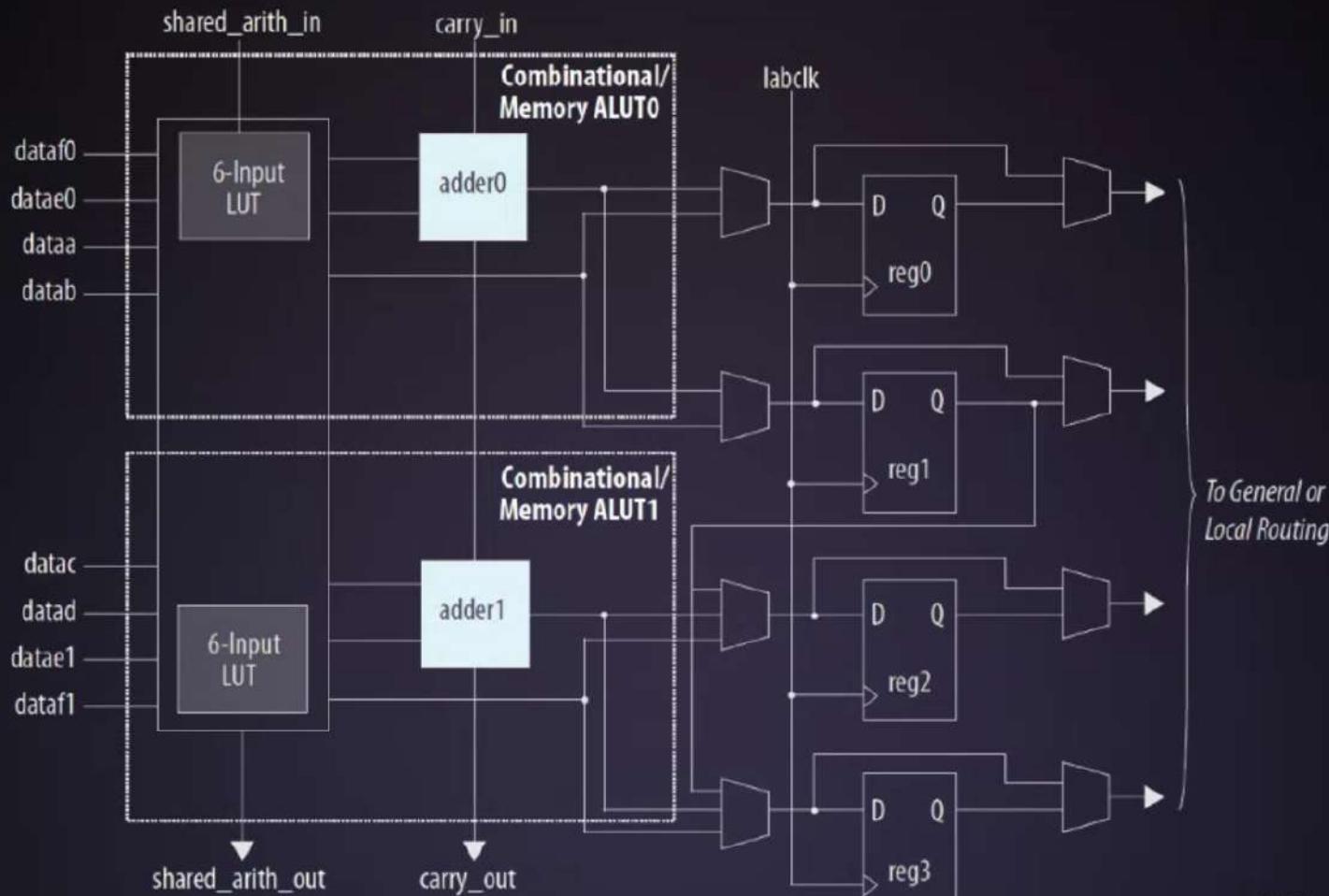


Table 3: Stratix V GX Device Features

Features	55GXA 3	55GXA 4	55GXA 5	55GXA 7	55GXA 9	55GXA B	55GXB 5	55GXB 6	55GXB 9	55GXBB
Logic Elements (K)	340	420	490	622	840	952	490	597	840	952
ALMs	128,300	158,500	185,000	234,720	317,000	359,200	185,000	225,400	317,000	359,200
Registers (K)	513	634	740	939	1,268	1,437	740	902	1,268	1,437
14.1-Gbps Transceivers	12, 24, or 36	24 or 36	24, 36, or 48	24, 36, or 48	36 or 48	36 or 48	66	66	66	66
PCIe hard IP Blocks	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4	1, 2, or 4	1, 2, or 4	1 or 4	1 or 4	1 or 4	1 or 4
Fractional PLLs	20 ⁽⁵⁾	24	28	28	28	28	24	24	32	32
M20K Memory Blocks	957	1,900	2,304	2,560	2,640	2,640	2,100	2,660	2,640	2,640
M20K Memory (MBits)	19	37	45	50	52	52	41	52	52	52
Variable Precision Multipliers (18x18)	512	512	512	512	704	704	798	798	704	704
Variable Precision Multipliers (27x27)	256	256	256	256	352	352	399	399	352	352

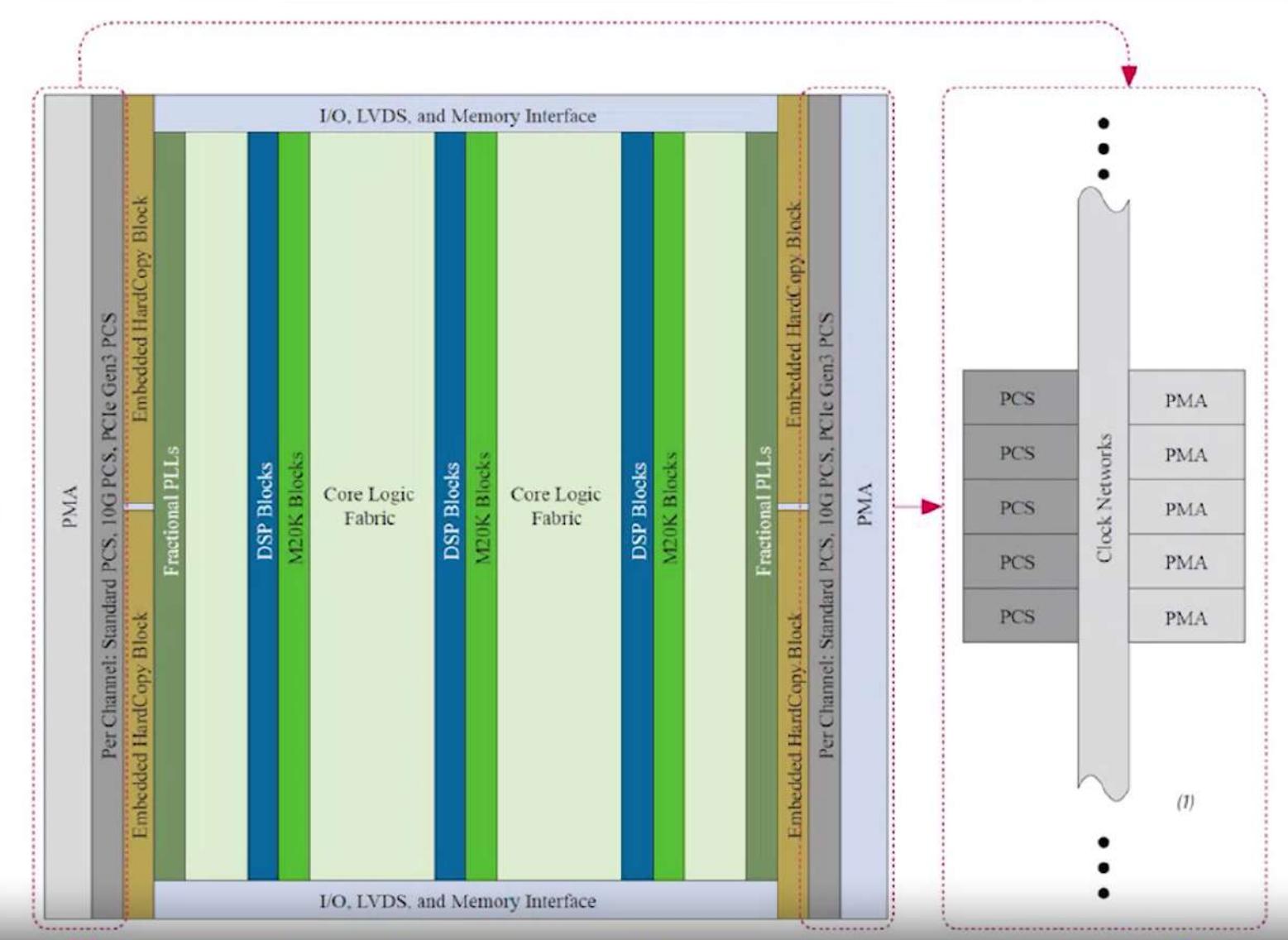


Figure 1-6: ALM High-Level Block Diagram for Stratix V Devices

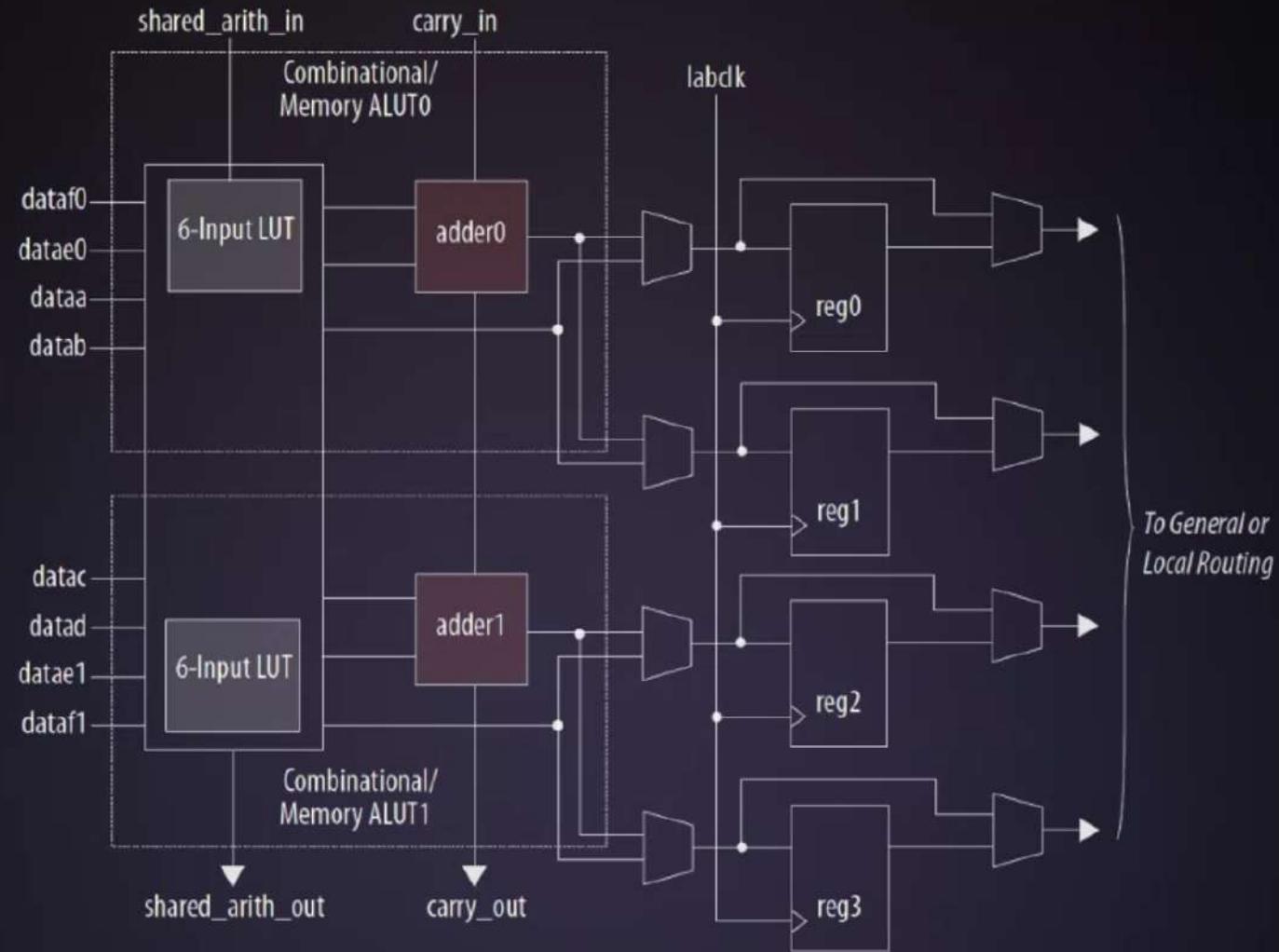
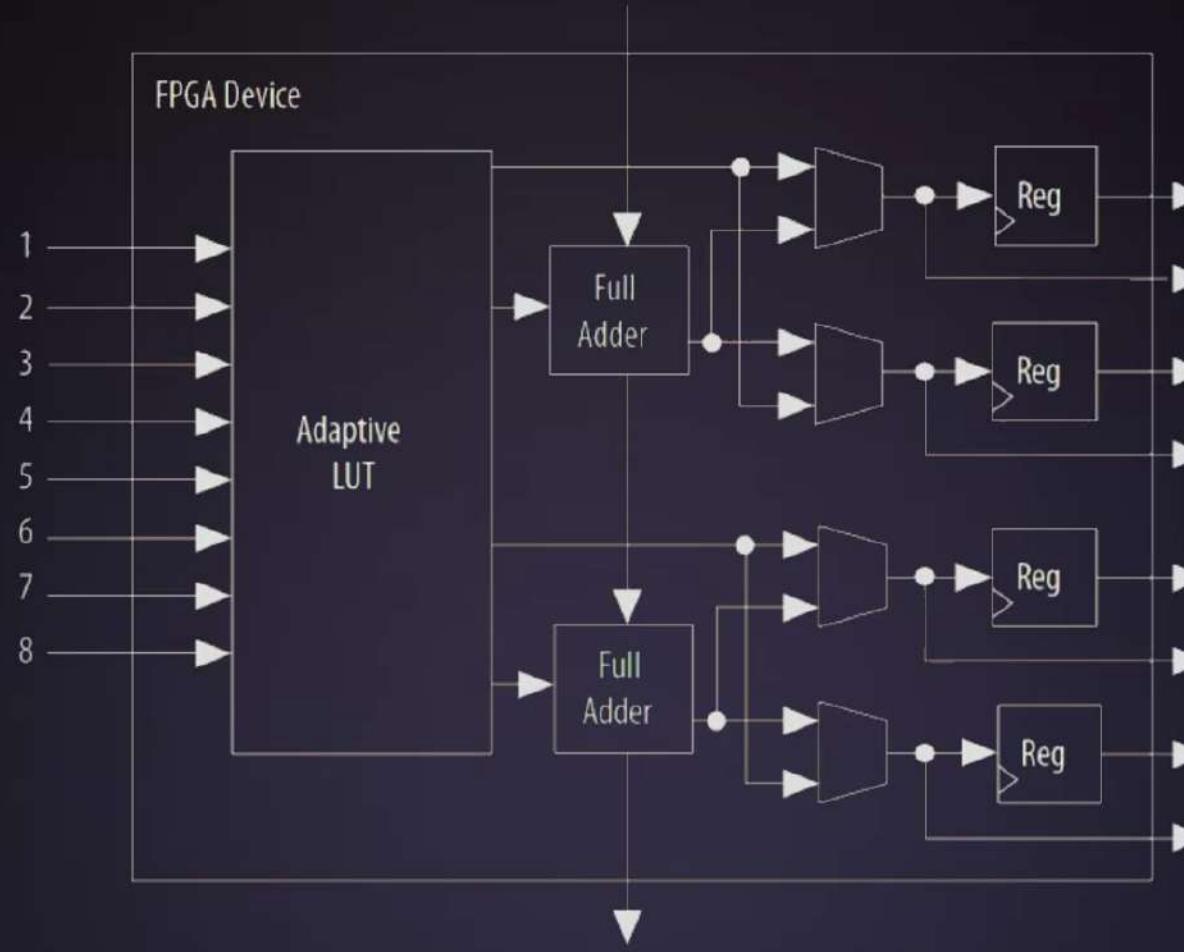


Table 6: Maximum Resource Counts for Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)—Preliminary

Resource		Product Line			
		GX 570	GX 660	GX 900	GX 1150
Logic Elements (LE) (K)		570	660	900	1,150
ALM		217,080	250,540	339,620	427,200
Register		868,320	1,002,160	1,358,480	1,708,800
Memory (Kb)	M20K	36,000	42,620	48,460	54,260
	MLAB	5,096	5,788	9,386	12,984
Variable-precision DSP Block		1,523	1,678	1,518	1,518
18 x 19 Multiplier		3,046	3,356	3,036	3,036
PLL	Fractional Synthesis	16	16	32	32
	I/O	16	16	16	16
17.4 Gbps Transceiver		48	48	96	96
GPIO ⁽²⁾		696	696	768	768

Figure 5: ALM for Arria 10 Devices



INTEL® STRATIX® 10 PRODUCT TABLE

ALTERA
now part of Intel

PRODUCT LINE	GX 400 SX 400	GX 550 SX 550	GX 850 SX 850	GX 1100 SX 1100	GX 1650 SX 1650	GX 2100 SX 2100	GX 2500 SX 2500	GX 2800 SX 2800	GX 4500 SX 4500	GX 5500 SX 5500
Logic elements (LEs) ¹	378,000	612,000	841,000	1,092,000	1,624,000	2,005,000	2,422,000	2,753,000	4,463,000	5,510,000
Adaptive logic modules (ALMs)	128,160	207,360	284,960	370,080	550,540	679,680	821,150	933,120	1,512,820	1,867,680
ALM registers	512,640	829,440	1,139,840	1,480,320	2,202,160	2,718,720	3,284,600	3,732,480	6,051,280	7,470,720
Hyper-Registers from HyperFlex™ architecture					Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric					
Programmable clock trees synthesizable					Hundreds of synthesizable clock trees					
Resources	eSRAM memory blocks	-	-	1	1	2	2	-	-	-
	eSRAM memory size (Mb)	-	-	45	45	90	90	-	-	-
	M20K memory blocks	1,537	2,489	3,477	4,401	5,851	6,501	9,963	11,721	7,033
	M20K memory size (Mb)	30	49	68	86	114	127	195	229	137
	MLAB memory size (Mb)	2	3	4	6	8	11	13	15	23
	Variable-precision digital signal processing (DSP) blocks	648	1,152	2,016	2,520	3,145	3,744	5,011	5,760	1,980
	18 x 19 multipliers	1,296	2,304	4,032	5,040	6,290	7,488	10,022	11,520	3,960
	Peak fixed-point performance (TMACS) ²	2.6	4.6	8.1	10.1	12.6	15.0	20.0	23.0	7.9
	Peak floating-point performance (TFLOPS) ³	1.0	1.8	3.2	4.0	5.0	6.0	8.0	9.2	3.2
	Secure device manager	AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection								
I/O and Architectural Features	Hard processor system ⁴	Quad-core 64 bit ARM® Cortex®-A53 up to 1.5 GHz with 32 KB I/D cache, NEON® coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I²C x5, general-purpose timers x7, watchdog timer x4								
	Maximum user I/O pins	392	400	736	736	704	704	1160	1160	1640
	Maximum LVDS pairs (1.6 Gbps (RX or TX)	192	192	360	360	336	336	576	576	816
	Total full duplex transceiver count	24	48	48	48	96	96	96	96	24
	GXT full duplex transceiver count (up to 30 Gbps)	16	32	32	32	64	64	64	64	16
	GX full duplex transceiver count (up to 17.4 Gbps)	8	16	16	16	32	32	32	32	8
	PCI Express® (PCIe®) hard intellectual property (IP) blocks (Gen3 x16)	1	2	2	2	4	4	4	1	1
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys								
	Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count ⁵									
	F1152 pin (35 mm x 35 mm, 1.0 mm pitch)	392,8,192,24	392,8,192,24	-	-	-	-	-	-	-
I/O and Architectural Features	F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)	-	400,16,192,48	-	-	-	-	-	-	-
	F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)	-	-	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	-
	F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)	-	-	736,16,360,48	736,16,360,48	-	-	-	-	-
	F2397 pin (50 mm x 50 mm, 1.0 mm pitch)	-	-	-	-	704,32,336,96	704,32,336,96	704,32,336,96	704,32,336,96	-
	F2912 pin (55 mm x 55 mm, 1.0 mm pitch)	-	-	-	-	-	-	1160,8,576,24	1160,8,576,24	1640,8,816,24



Altera Hyper-Flex Architecture

The HyperFlex Advantage



Registers Everywhere

The registers in the
interconnect routing,
called Hyper-Registers

Altera Hyper-Flex Architecture

The HyperFlex Advantage



Enhanced Core Clocking

Localized clock trees
reduce skew and timing
uncertainty

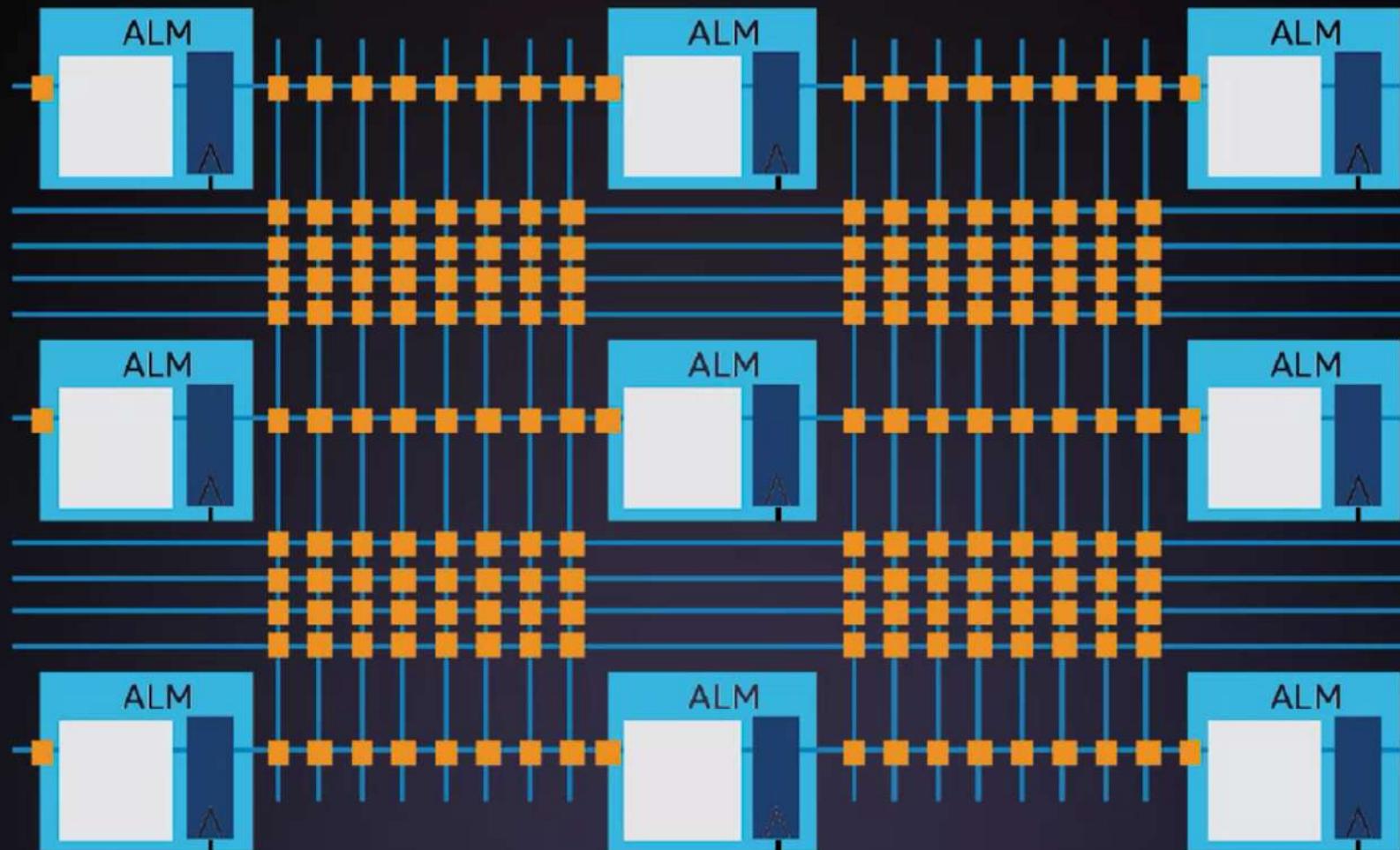
Altera Hyper-Flex Architecture

The HyperFlex Advantage



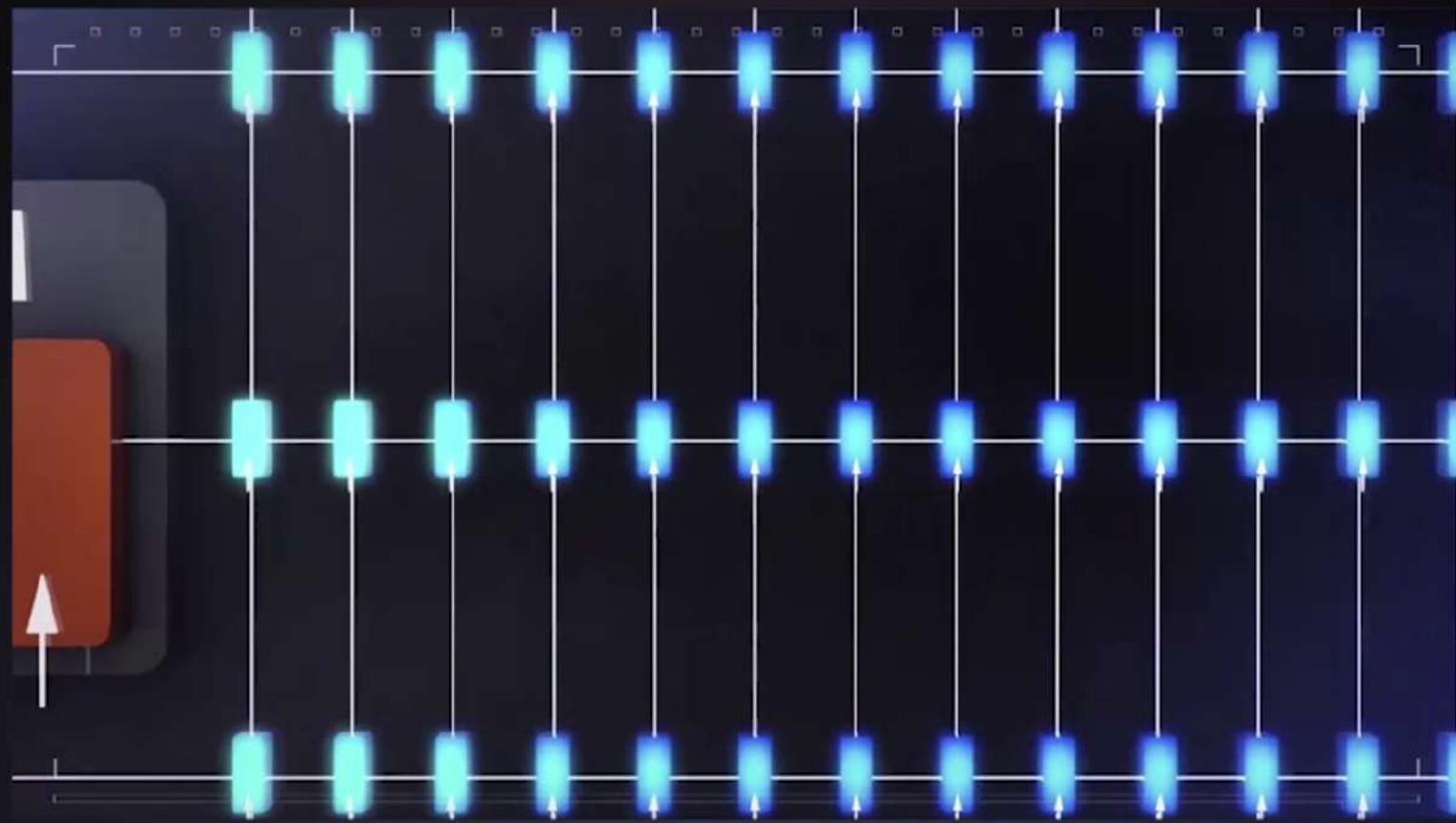
Hyper-Aware Design Flow

Includes three new improvements:
a Fast Forward Compile tool, a
Hyper-Retimer step, and enhanced
synthesis and place-and-route
algorithms that use the
Hyper-Registers.



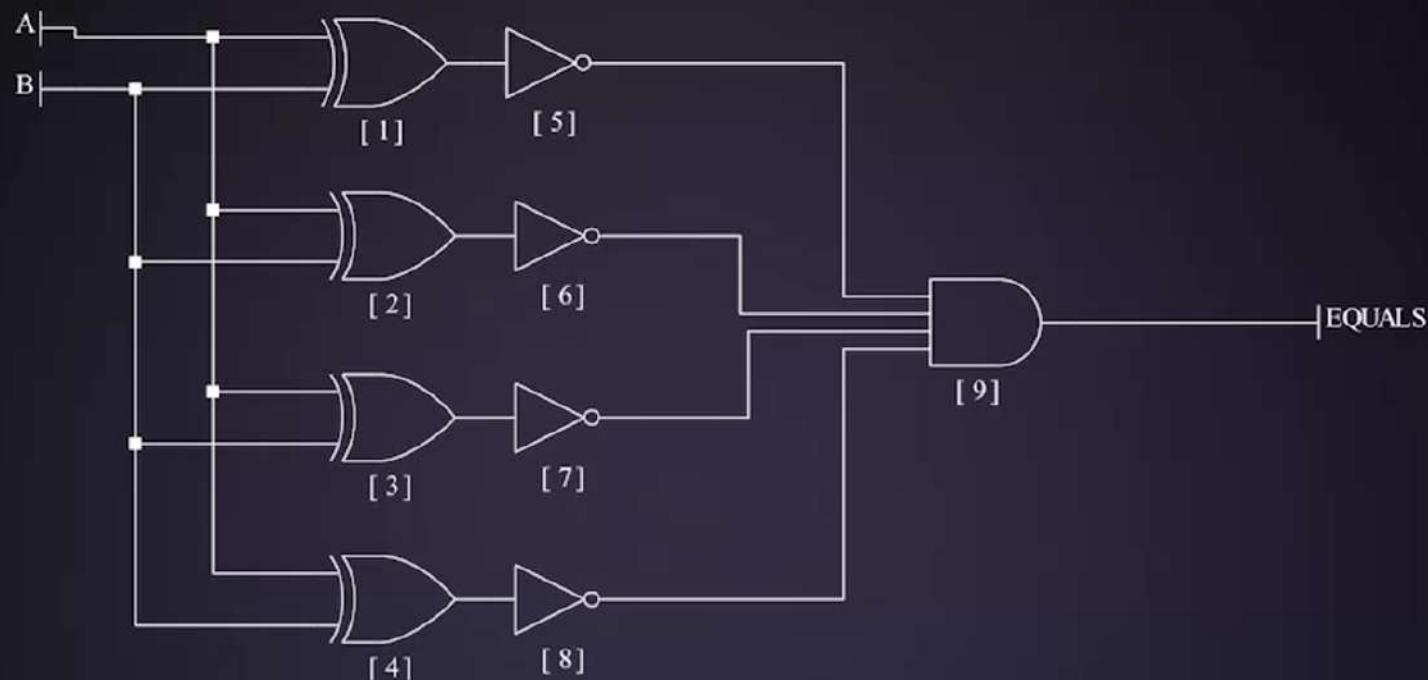
- Registers are available in every routing segment
- Registers are available on all block inputs (ALM, M20K blocks, DSP blocks, and I/O cells)

Figure 2. "Registers Everywhere" HyperFlex Architecture

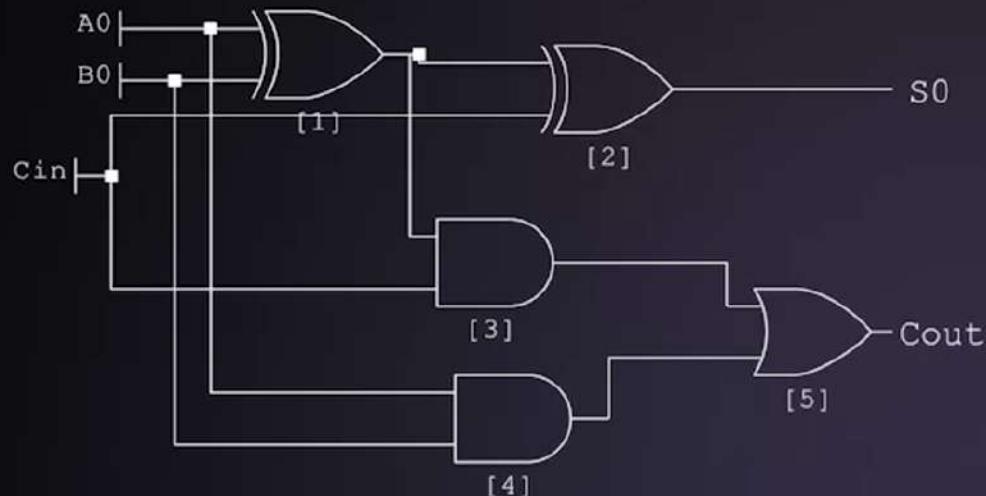


altera.com/support/training/videos/hyperflex-architecture-overview-video.tablet.html

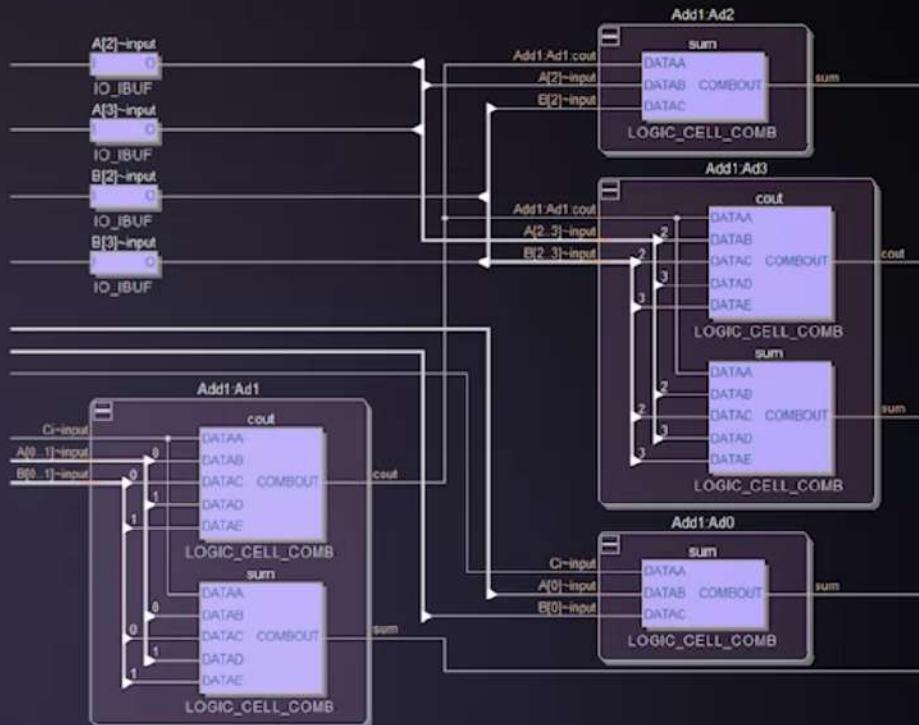
How large of a comparator can be made using a Stratix 10 Logic Cell?



How many full adders can be created in a Stratix 10?



1 bit full adder



4 bit adder in 3 ALMs

Altera Large FPGAs Summary

Altera offers the Arria V, Stratix V, Arria 10 and Stratix 10 FPGAs for large designs.

Arria V and Stratix V are large devices with up to a million logic elements and integration of many hard IP blocks to create very powerful parts with great processing power.

The Arria 10 increases the processing power further, with 28 Gbps serial transceivers and 2666 Mbps DDR4 DRAM interface.

Altera Large FPGAs Summary

The Stratix 10 is the largest and fastest FPGA currently in production, with over 5.5 million logic elements and core clock speed of 1100 MHz.

Altera's Hyperflex Architecture is a revolutionary change that will increase FPGA performance further, doubling performance at equivalent power levels.

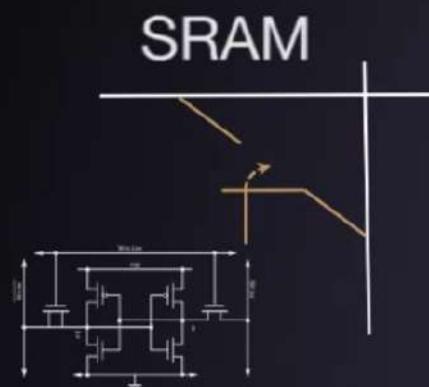
Programmable Logic Device Selection Criteria

	Selection Criteria	FLASH FPGAs	Anti-Fuse
1	Reprogrammability (Configuration Memory Type)	Yes	No
2	Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)	Moderate	Moderate
3	Cost per logic gate	Moderate to high	High
4	Speed (Maximum clock frequency)	400 MHz	870 MHz
5	Power Consumption (static and dynamic)	Very Low	Moderate
6	Cost per I/O (I/O Density) and extent of supported I/O standards	Low, Good	Low, Good
7	Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)	Extensive	Good
8	Deterministic timing (timing is consistent in every implementation)	No	Yes
9	Reliability (FIT rate)	Excellent	Best Available
10	Endurance (number of programming cycles and years of retention)	10K/ 20 year	1/ 20 year
11	Design and Data Security	Best Available	Excellent

FLASH Interconnection Technologies

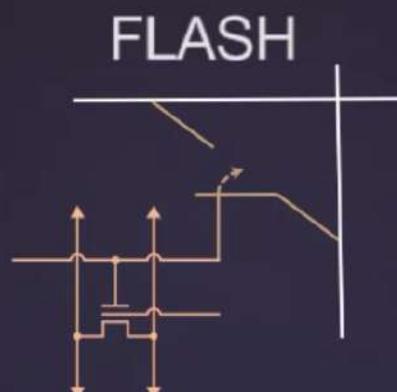
FPGA Interconnect Technologies are SRAM, FLASH, and Antifuse

Microsemi manufactures FLASH and Antifuse FPGAs



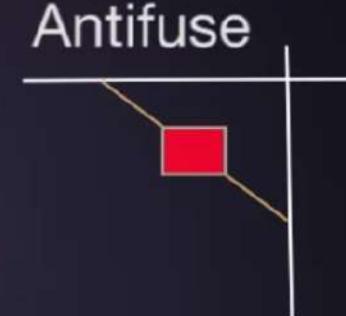
SRAM

Reprogrammable
And Volatile



FLASH

Reprogrammable
and Non-Volatile

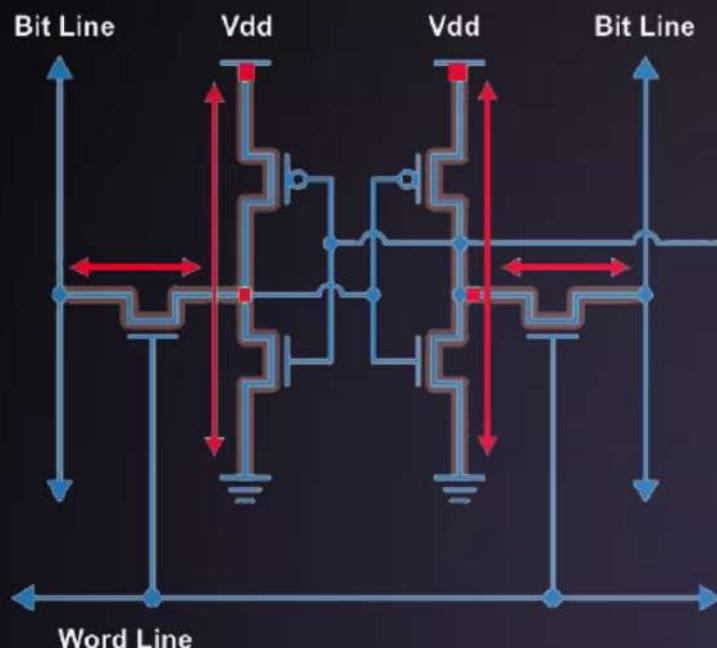


Antifuse

One-time Programmable
and Non-Volatile

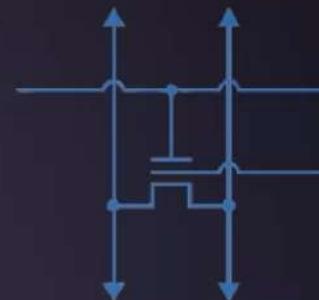
Microsemi FLASH Technology Advantages

FPGA SRAM routing Cell



Substantial Leakage per Cell
High Static Current

FLASH routing cell



1000x Lower Leakage
Very low static current

Microsemi FLASH Technology Advantages

True FLASH-Based Technology

Live at Power-up

Integration provides lower total system cost

Low power across the board

Best Design Security

Superior Reliability

Microsemi IGLOO nano

IGLOO nano Devices	AGLN010	AGLN015 ¹	AGLN020		AGLN060	AGLN125	AGLN250
IGLOO nano-Z Devices ¹				AGLN030Z ¹	AGLN060Z ¹	AGLN125Z ¹	AGLN250Z ¹
System Gates	10,000	15,000	20,000	30,000	60,000	125,000	250,000
Typical Equivalent Macrocells	86	128	172	256	512	1,024	2,048
VersaTiles (D-flip-flops)	260	384	520	768	1,536	3,072	6,144
Flash*Freeze Mode (typical, μ W)	2	4	4	5	10	16	24
RAM Kbits (1,024 bits) ²	–	–	–	–	18	36	36
4,608-Bit Blocks ²	–	–	–	–	4	8	8
FlashROM Kbits (1,024 bits)	1	1	1	1	1	1	1
Secure (AES) ISP ²	–	–	–	–	Yes	Yes	Yes
Integrated PLL in CCCs ^{2,3}	–	–	–	–	1	1	1
VersaNet Globals	4	4	4	6	18	18	18
I/O Banks	2	3	3	2	2	2	4
Maximum User I/Os (packaged device)	34	49	52	77	71	71	68
Maximum User I/Os (Known Good Die)	34	–	52	83	71	71	68

Microsemi IGLOO nano

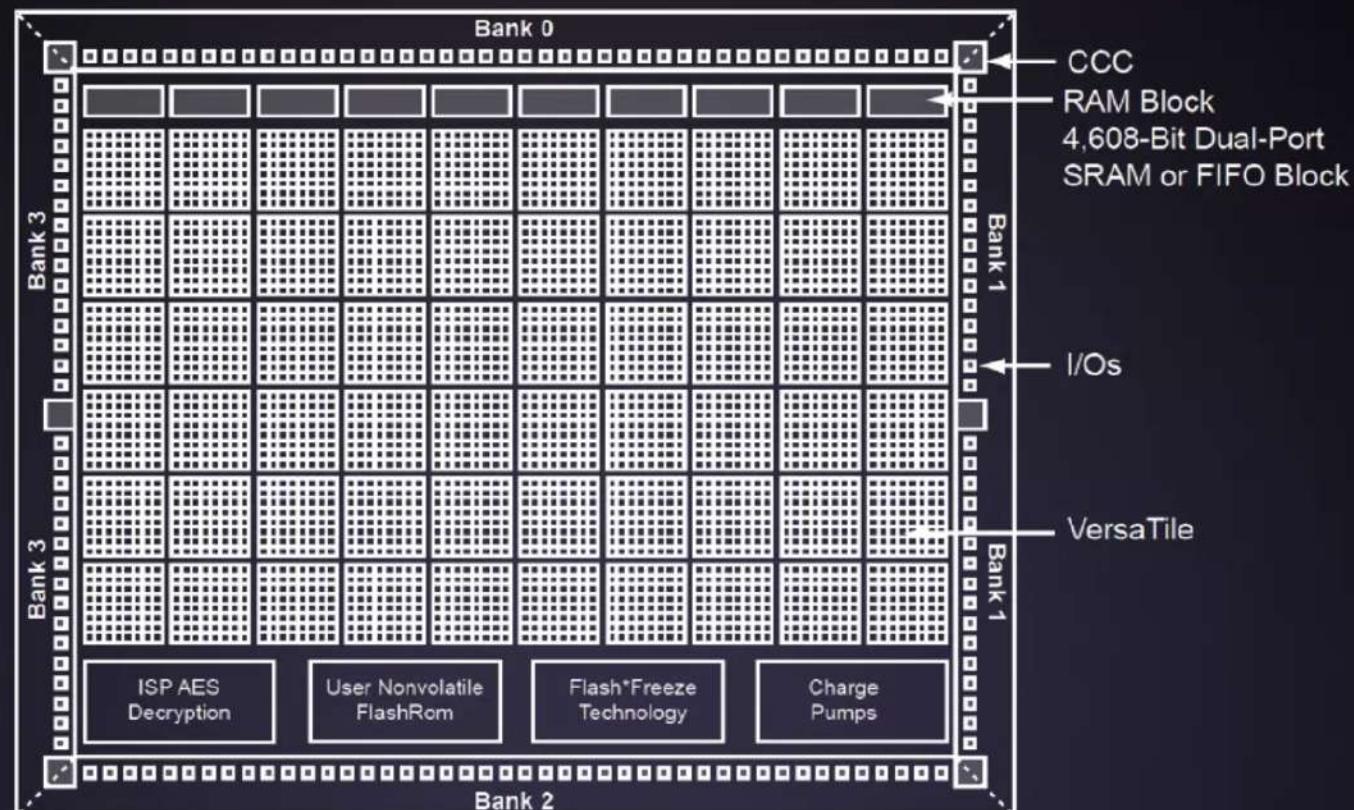


Figure 1-4 • IGLOO Device Architecture Overview with Four I/O Banks (AGLN250)

Microsemi IGLOO nano

LUT-3 Equivalent



D-Flip-Flop with Clear or Set



Enable D-Flip-Flop with Clear or Set



Figure 1-6 • VersaTile Configurations

Microsemi SmartFusion

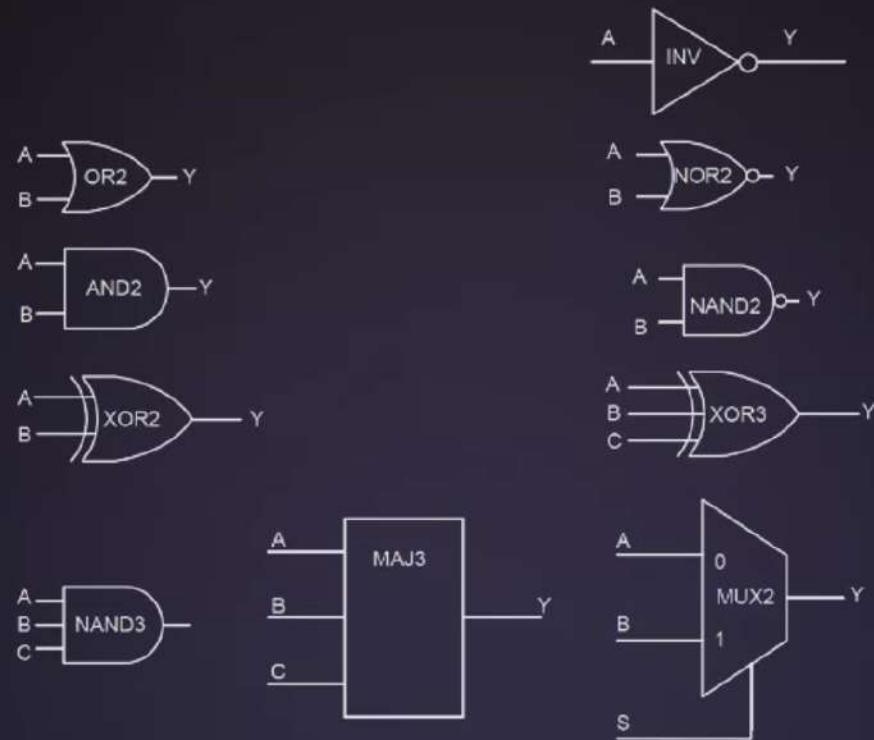


Figure 2-21 • Sample of Combinatorial Cells

[4]

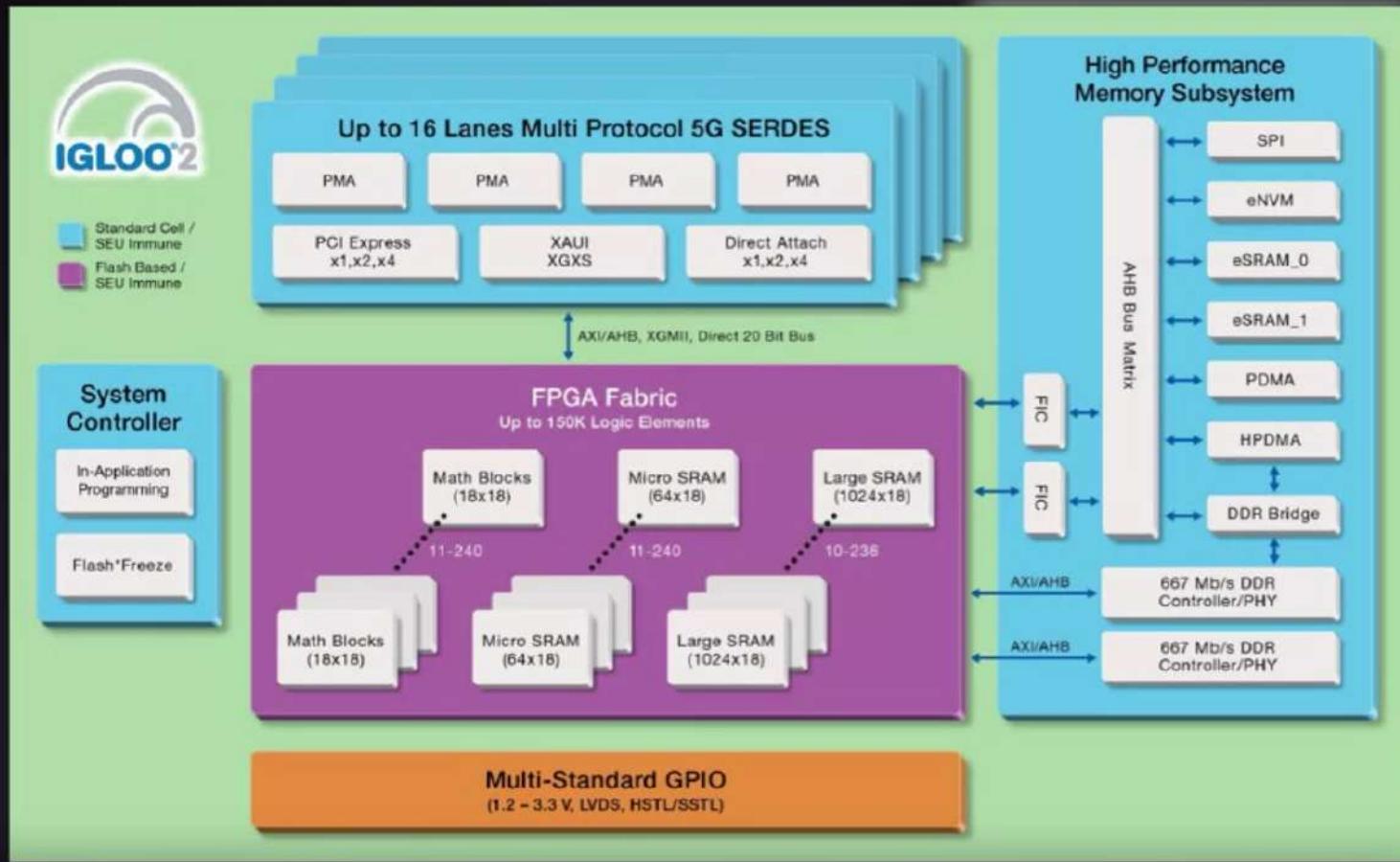
Microsemi IGLOO2

Table 1 • IGLOO2 FPGA Product Family

	Features ^{2,3}	M2GL005 (S)	M2GL010 (S/T/TS)	M2GL025 (T/TS)	M2GL050 (T/TS)	M2GL060 (T/TS)	M2GL090 (T/TS)	M2GL150 (T/TS)
Logic/DSP	Maximum Logic Elements (4LUT + DFF) ¹	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Math Blocks (18x18)	11	22	34	72	72	84	240
	PLLs and CCCs		2		6		6	
	SPI/HPDMA/PDMA			1 each				
	Fabric Interface Controllers (FICs)		1		2		1	2
	Data Security			AES256, SHA256, RNG			AES256, SHA256, RNG, ECC, PUF	
Memory	eNVM (K Bytes)	128		256			512	
	LSRAM 16K Blocks	10	21	31	69	69	109	236
	uSRAM 1K Blocks	11	22	34	72	72	112	240
	eSRAM (K Bytes)			64				
	Total RAM (K bits)	703	912	1104	1826	1826	2586	5000
High Speed	DDR Controllers		1x18		2x36	1x18	1x18	2x36
	SERDES Lanes (T)	0		4		4	4	16
	PCIe End Points	0		1		2		4
User I/Os	MSIO (3.3 V)	119	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40	40	62	40	40	106
	DDRIO (2.5 V)	66	70	70	176	76	76	176
	Total User I/O	209	233	267	377	387	425	574
Grades	Commercial (C), Industrial (I), Military (M), Automotive (T1/T2)	C, I, T1, T2		C, I, M, T1, T2			C, I, M	



Microsemi IGLOO2



Microsemi IGLOO2

Security

- Design Security Features (available on all devices)
 - Intellectual Property (IP) Protection through Unique Security Features and Use Models New to the PLD Industry
 - Encrypted User Key and Bitstream Loading, Enabling Programming in Less-Trusted Locations
 - Supply-Chain Assurance Device Certificate
 - Enhanced Anti-Tamper Features
 - Zeroization
- Data Security Features (available on premium devices)
 - Non-Deterministic Random Bit Generator (NRBG)
 - User Cryptographic Services (AES-256, SHA-256, Elliptical Curve Cryptographic (ECC) Engine)
 - User Physically Unclonable Function (PUF) Key Enrollment and Regeneration
 - CRI Pass-Through DPA Patent Portfolio License
 - Hardware Firewalls Protecting Microcontroller Subsystem (HPMS) Memories

Reliability

[7]

- Single Event Upset (SEU) Immune
 - Zero FIT FPGA Configuration Cells
- Junction Temperature: 125°C – Military Temperature, 100°C – Industrial Temperature, 85°C – Commercial Temperature
- Single Error Correct Double Error Detect (SECDED) Protection on the Following:
 - Embedded Memory (eSRAMs)
 - PCIe Buffer
 - DDR Memory Controllers with Optional SECDED Modes
 - Buffers Implemented with SEU Resistant Latches on the Following:
 - DDR Bridges (HPMS, MDDR, FDDR)
 - SPI FIFO
 - NVM Integrity Check at Power-Up and On-Demand
 - No External Configuration Memory Required—Instant-On, Retains Configuration When Powered Off

Microsemi IGLOO2

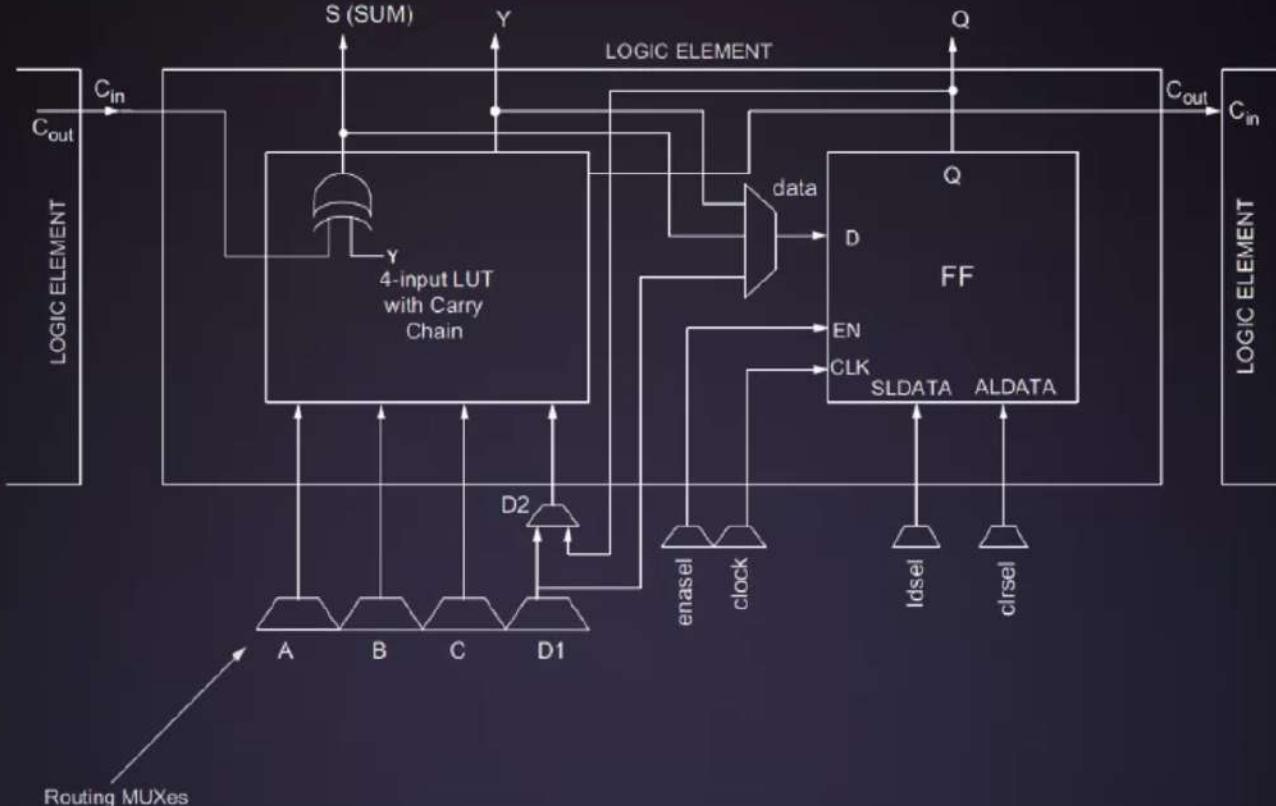


Figure 2 • Functional Block Diagram of Logic Element

Microsemi Axcelerator FPGA Family

Table 1 • Axcelerator Family Product Profile

Device	AX125	AX250	AX500	AX1000	AX2000
Capacity (in Equivalent System Gates)	125,000	250,000	500,000	1,000,000	2,000,000
Typical Gates	82,000	154,000	286,000	612,000	1,060,000
Modules					
Register (R-cells)	672	1,408	2,688	6,048	10,752
Combinatorial (C-cells)	1,344	2,816	5,376	12,096	21,504
Maximum Flip-Flops	1,344	2,816	5,376	12,096	21,504
Embedded RAM/FIFO					
Number of Core RAM Blocks	4	12	16	36	64
Total Bits of Core RAM	18,432	55,296	73,728	165,888	294,912
Clocks (Segmentable)					
Hardwired	4	4	4	4	4
Routed	4	4	4	4	4
PLLs	8	8	8	8	8
I/Os					
I/O Banks	8	8	8	8	8
Maximum User I/Os	168	248	336	516	684
Maximum LVDS Channels	84	124	168	258	342
Total I/O Registers	504	744	1,008	1,548	2,052
Package					
PQ		208	208		
BG				729	
FG	256, 324	256, 484	484, 676	484, 676, 896	896, 1152
CQ		208, 352	208, 352	352	256, 352
CG				624	624

[9]

Microsemi Axcelerator Layout

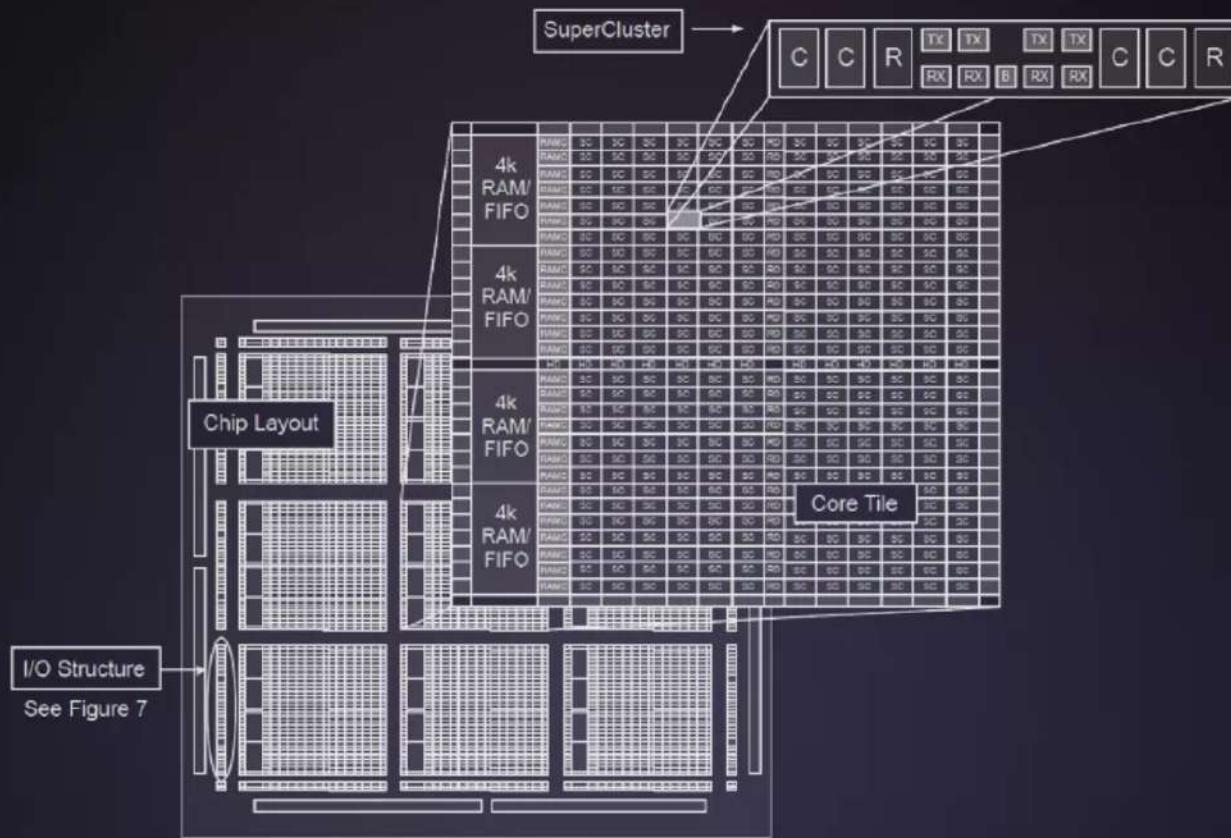


Figure 1-6 • AX Device Architecture (AX1000 shown)

Microsemi Axcelerator Logic

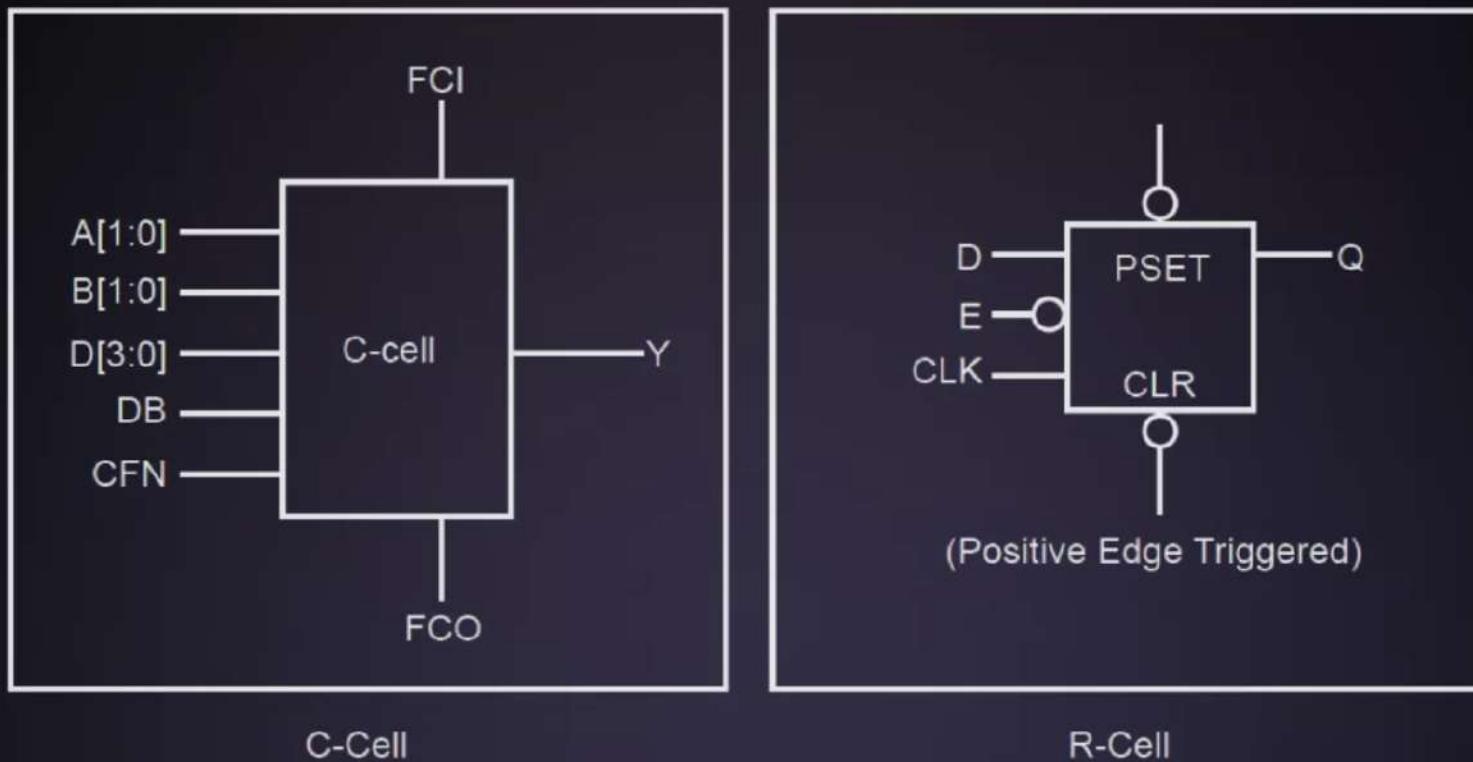


Figure 1-3 • AX C-Cell and R-Cell

Microsemi RTAX Rad-Hard FPGA Family

Table 1 • RTAX Family Product Profile

Device	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL	RTAX2000D/DL	RTAX4000D/DL
Capacity						
Equivalent System Gates	250,000	1,000,000	2,000,000	4,000,000	2,000,000	4,000,000
ASIC Gates	30,000	125,000	250,000	500,000	250,000	500,000
Modules						
Register (R-cells)	1,408	6,048	10,752	20,160	9,856	18,480
Combinatorial (C-cells)	2,816	12,096	21,504	40,320	19,712	36,960
Embedded RAM/FIFO (w/o EDAC)						
Core RAM Blocks	12	36	64	120	64	120
Core RAM Bits (K = 1,024)	54 k	162 k	288 k	540 k	288 k	540 k
Embedded Multiply/Accumulate Blocks	-	-	-	-	64	120
Clocks (segmentable)						
Hardwired	4	4	4	4	4	4
Routed	4	4	4	4	4	4
I/Os						
I/O Banks	8	8	8	8	8	8
User I/Os (maximum)	198	418	684	840	684	840
I/O Registers	744	1,548	2,052	2,520	2,052	2,520
Package						
CG/LG*	624	624	624, 1152	1272	1272	1272
CQ	208, 352	352	256, 352	352	352	352

Microsemi RTAX Logic

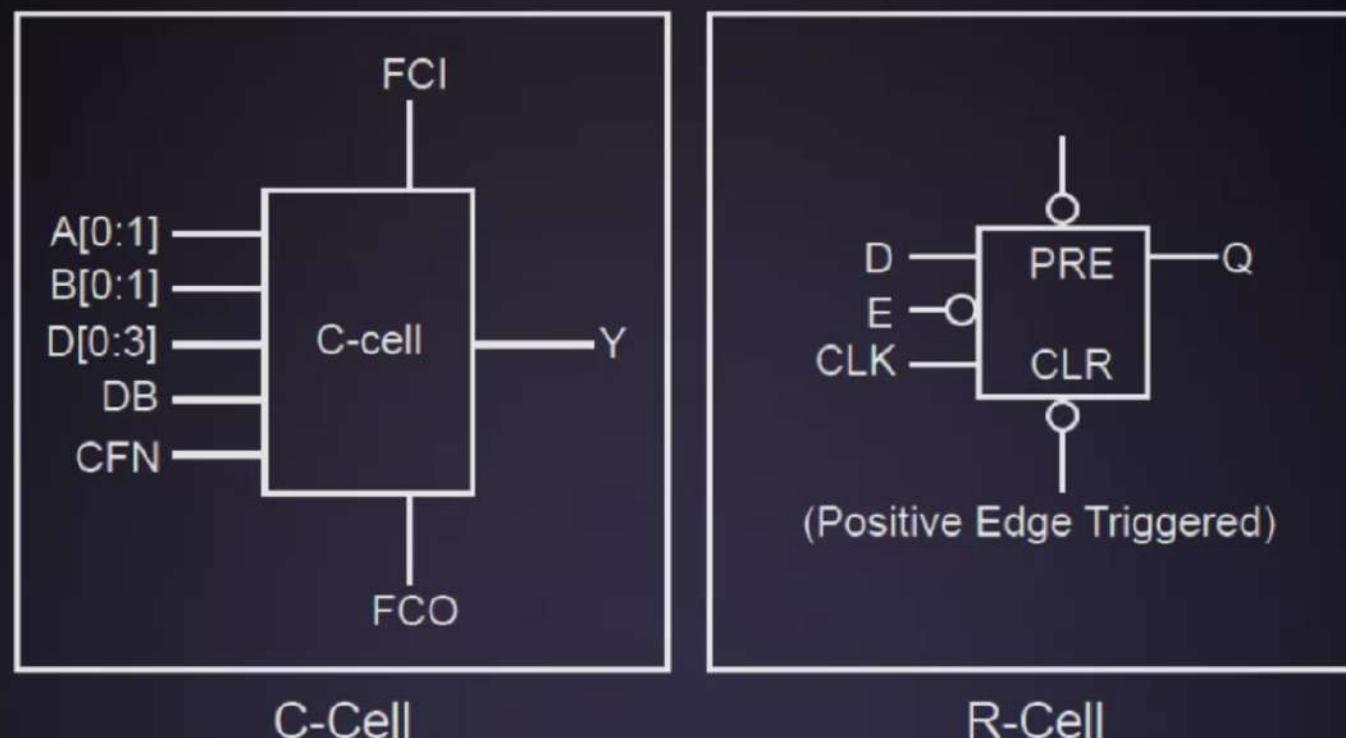
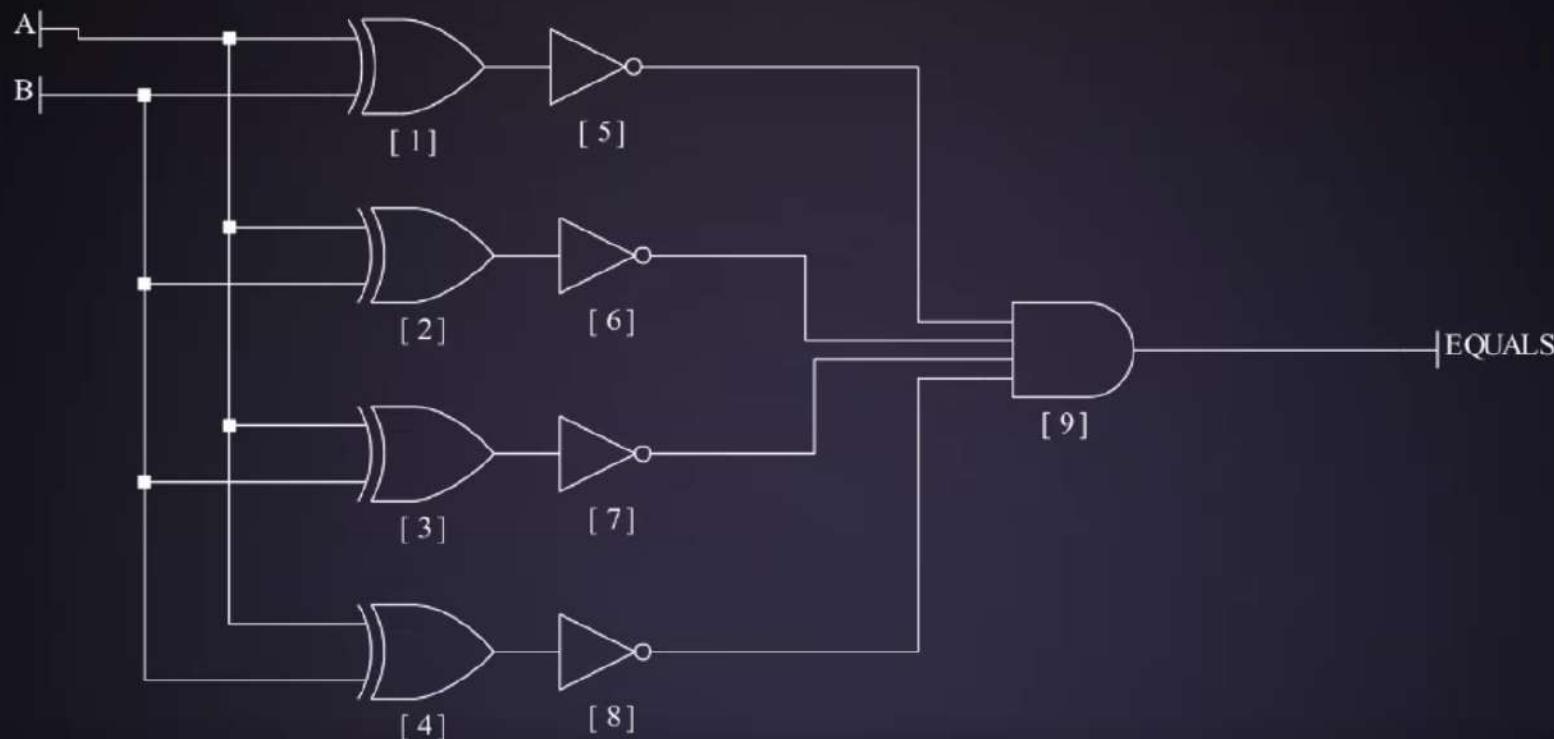
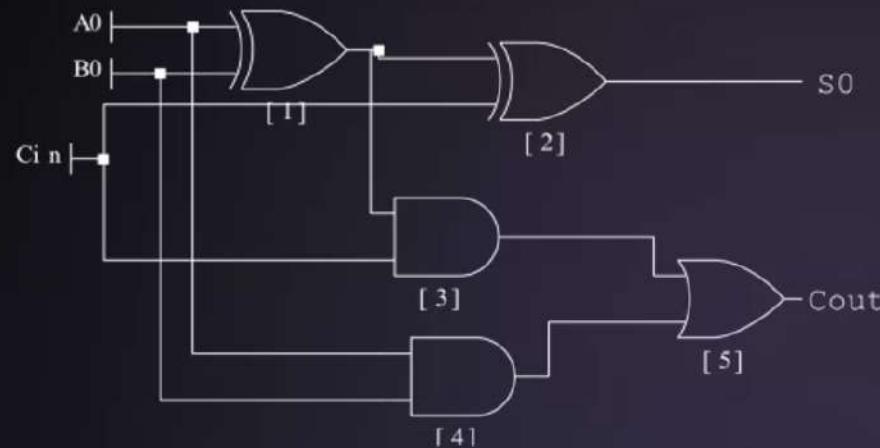


Figure 1-3 • RTAX C-Cell and R-Cell

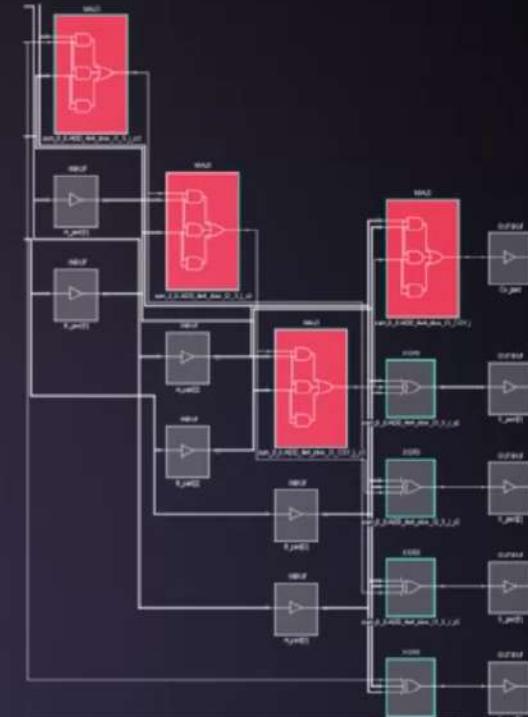
How large of a comparator can be made using an IGLOO Logic Cell?



How many full adders can be created in a IGLOO?



1 bit full adder



4 bit adder in 8 Versatiles

Microsemi FPGAs Summary

Microsemi offers both FLASH and Antifuse FPGAs. Each type has different capabilities and limitations.

The current Microsemi FLASH FPGA offering, the IGLOO and IGLOO2, are instant-on single chip solutions that are reprogrammable, with very good low power performance and high reliability and security.

Microsemi Antifuse FPGAs are designed for rugged environments and high reliability, including the Axcelerator family and the RTAX radiation tolerant family.

Microsemi FPGAs Summary

The Microsemi IGLOO2 has a wealth of hard IP cores included, including memory controllers, high-speed transceivers, RAMs, DSP blocks, and many security enhancements.

If security or reliability or low power are design requirements, Microsemi FPGAs are worth consideration.

Programmable Logic Device Selection Criteria

	Selection Criteria	SRAM CPLDs	SRAM FPGAs
1	Reprogrammability (Configuration Memory Type)	Yes	Yes
2	Size or Logic Density (amount of logic in systems gates, LEs, Slices, ALMs, etc.)	Small	Moderate
3	Cost per logic gate	Low	Low
4	Speed (Maximum clock frequency)	388 MHz	400 MHz
5	Power Consumption (static and dynamic)	Very Low	Moderate
6	Cost per I/O (I/O Density) and extent of supported I/O standards	Low, Good	Low, Good
7	Hard IP available on chip (Memory, DSP Blocks, Transceivers, etc.)	Very Good	Good
8	Deterministic timing (timing is consistent in every implementation)	No	No
9	Reliability (FIT rate)	Fair	OK
10	Endurance (number of programming cycles and years of retention)	100K/ 20 year	NA
11	Design and Data Security	Fair	Fair

Lattice ECP5

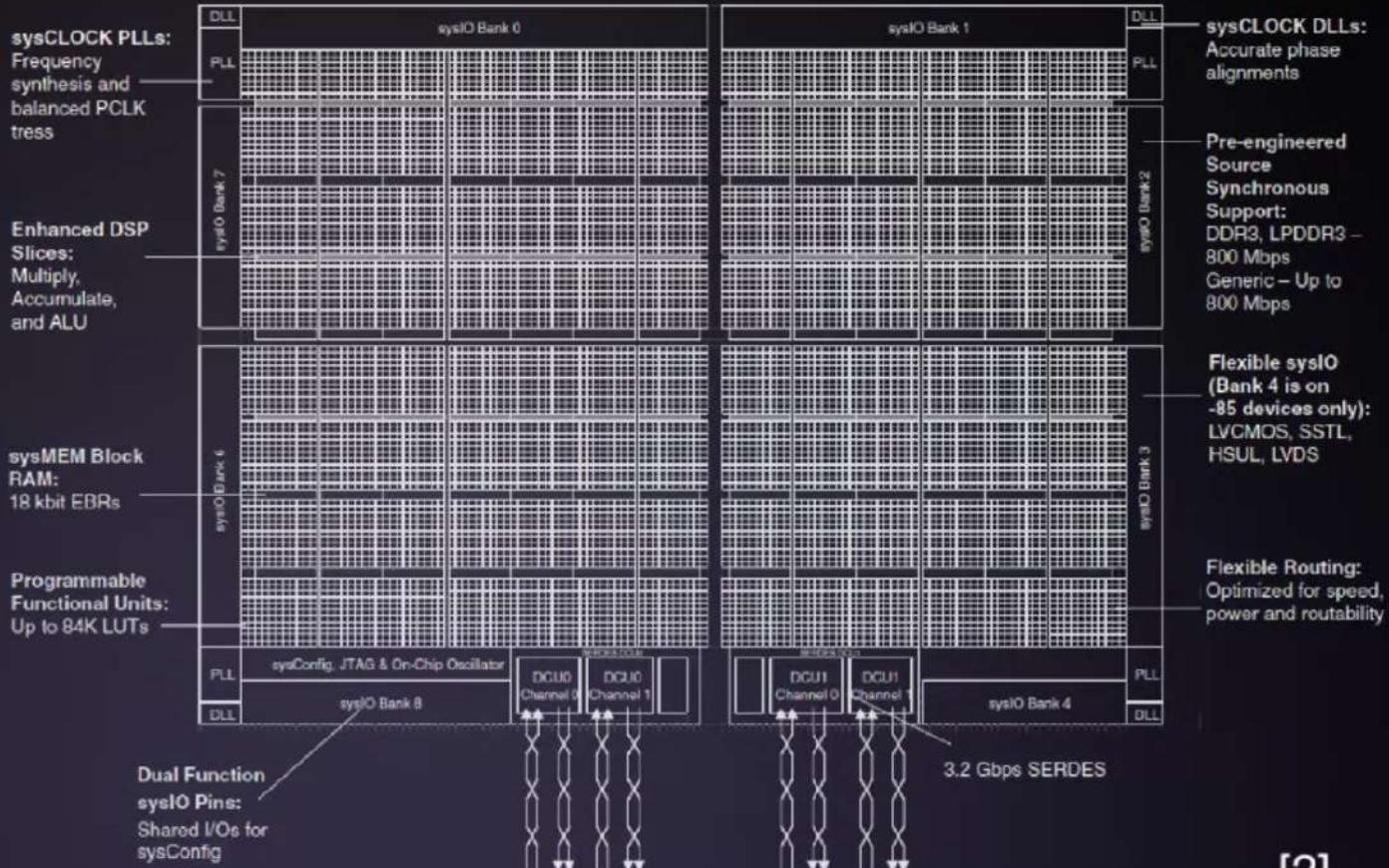
Table 1.1. ECP5 and ECP5-5G Family Selection Guide

Device	LFE5UM-25 LFE5UM5G-25	LFE5UM-45 LFE5UM5G-45	LFE5UM-85 LFE5UM5G-85	LFE5U-12	LFE5U-25	LFE5U-45	LFE5U-85
LUTs (K)	24	44	84	12	24	44	84
sysMEM Blocks (18 Kb)	56	108	208	32	56	108	208
Embedded Memory (Kb)	1,008	1944	3744	576	1,008	1944	3744
Distributed RAM Bits (Kb)	194	351	669	97	194	351	669
18 X 18 Multipliers	28	72	156	28	28	72	156
SERDES (Dual/Channels)	1/2	2/4	2/4	0	0	0	0
PLLs/DLLs	2/2	4/4	4/4	2/2	2/2	4/4	4/4
Packages and SERDES Channels / I/O Combinations							
285 csfBGA (10 x 10 mm ² , 0.5 mm)	2/118	2/118	2/118	0/118	0/118	0/118	0/118
381 caBGA (17 x 17 mm ²)	2/197	4/203	4/205	0/197	0/197	0/203	0/205
554 caBGA (23 x 23 mm ²)	—	4/245	4/259	—	—	0/245	0/259
756 caBGA (27 x 27 mm ²)	—	—	4/365	—	—	—	0/365

ECP5 Architecture

Contains an array of logic blocks surrounded by Programmable I/O Cells (PIC)

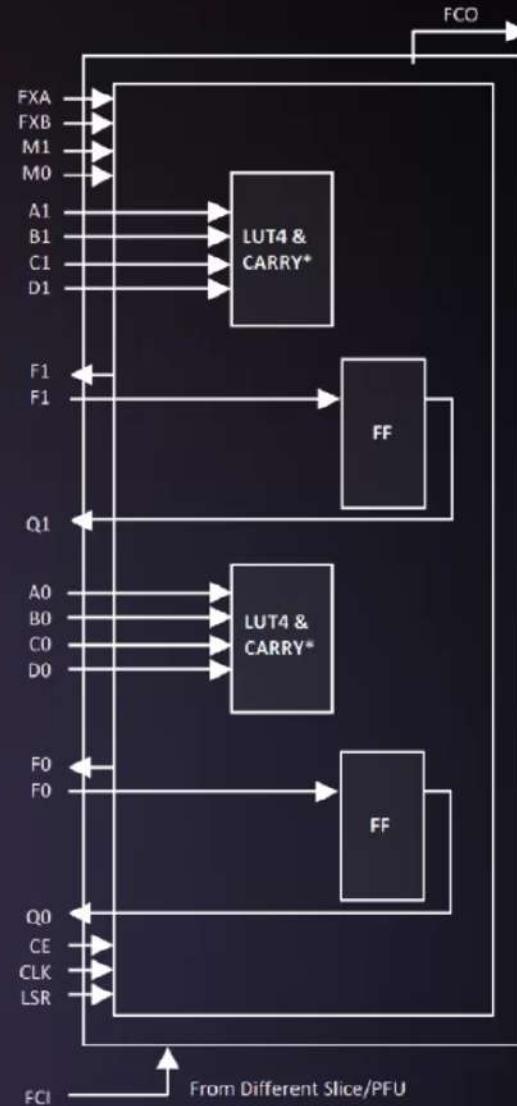
sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices



ECP5 Slice (Logic Element)

Each slice contains two LUT4s feeding two registers.

Distributed SRAM mode:
Slice 0 through Slice 2 are
configured as distributed
memory, and Slice 3 is used as
Logic or ROM.



ECP5 DSP Slice

The ECP5 sysDSP Slice supports many functions:

Full double data rate support -
Higher operation frequency
(throughput of up to 370 Mbps)

Dual-multiplier architecture.

Fully cascadable DSP across slices

- Symmetrical, assymetrical & non-symmetrical filters

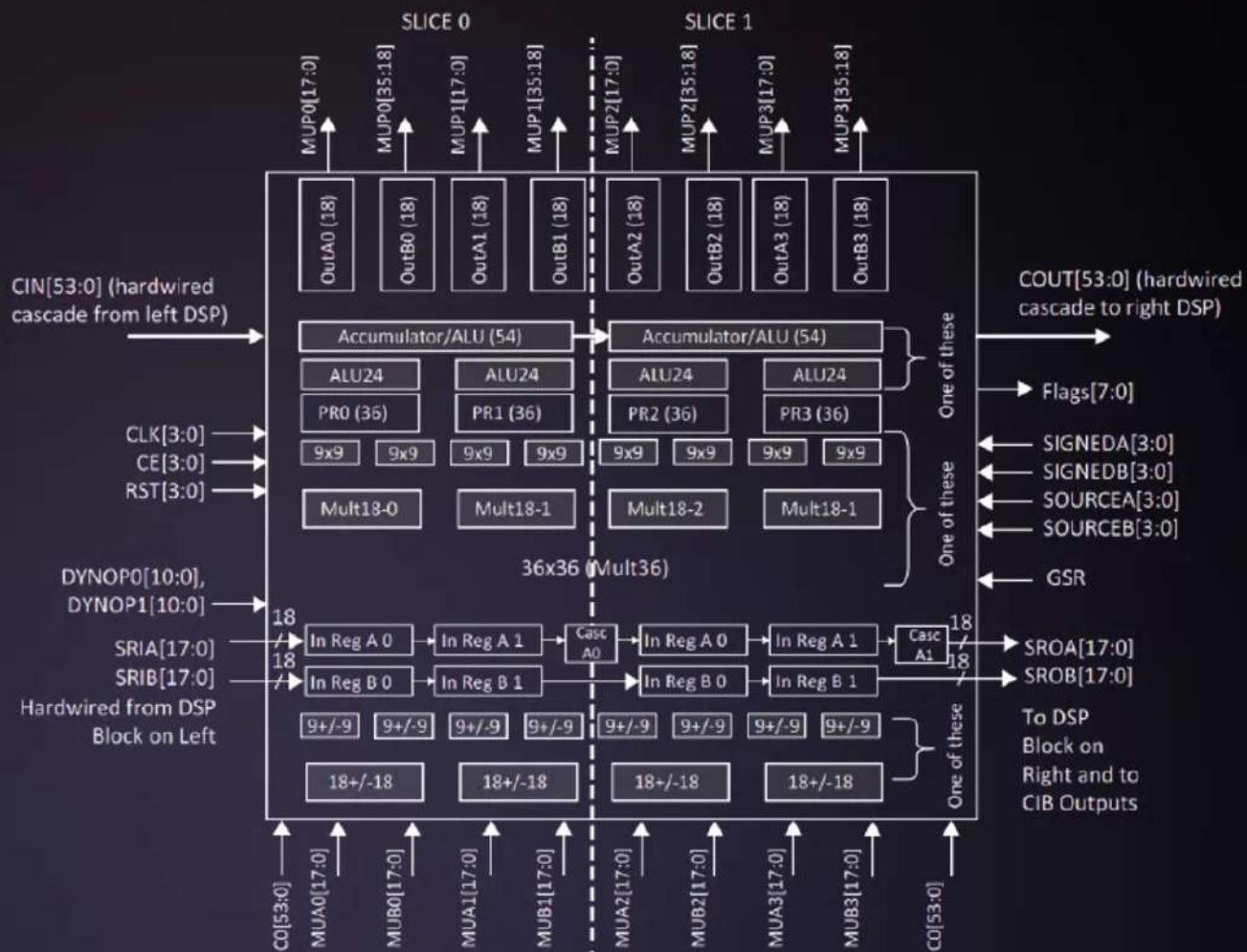


Figure 2.14. Simplified sysDSP Slice Block Diagram

ECP5 DSP Slice

The ECP5 sysDSP Slice supports many functions:

Multiply (one 18x36, two 18x18 or four 9x9 Multiplies per Slice)

Multiply (36x36 by cascading across two sysDSP slices)

Multiply Accumulate - one 18x36 or two 18x18

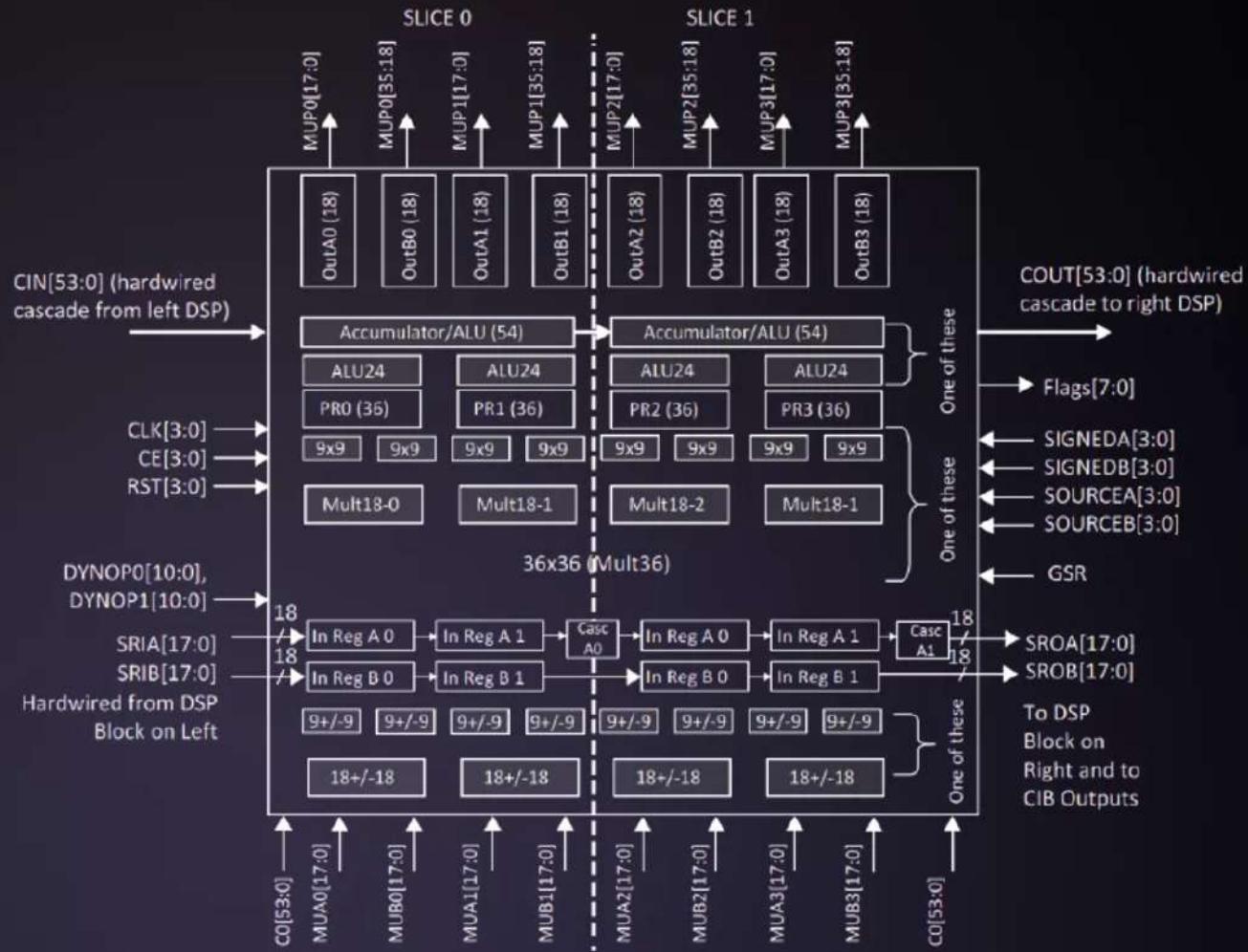


Figure 2.14. Simplified sysDSP Slice Block Diagram

Lattice ECP3

Table 1-1. LatticeECP3™ Family Selection Guide

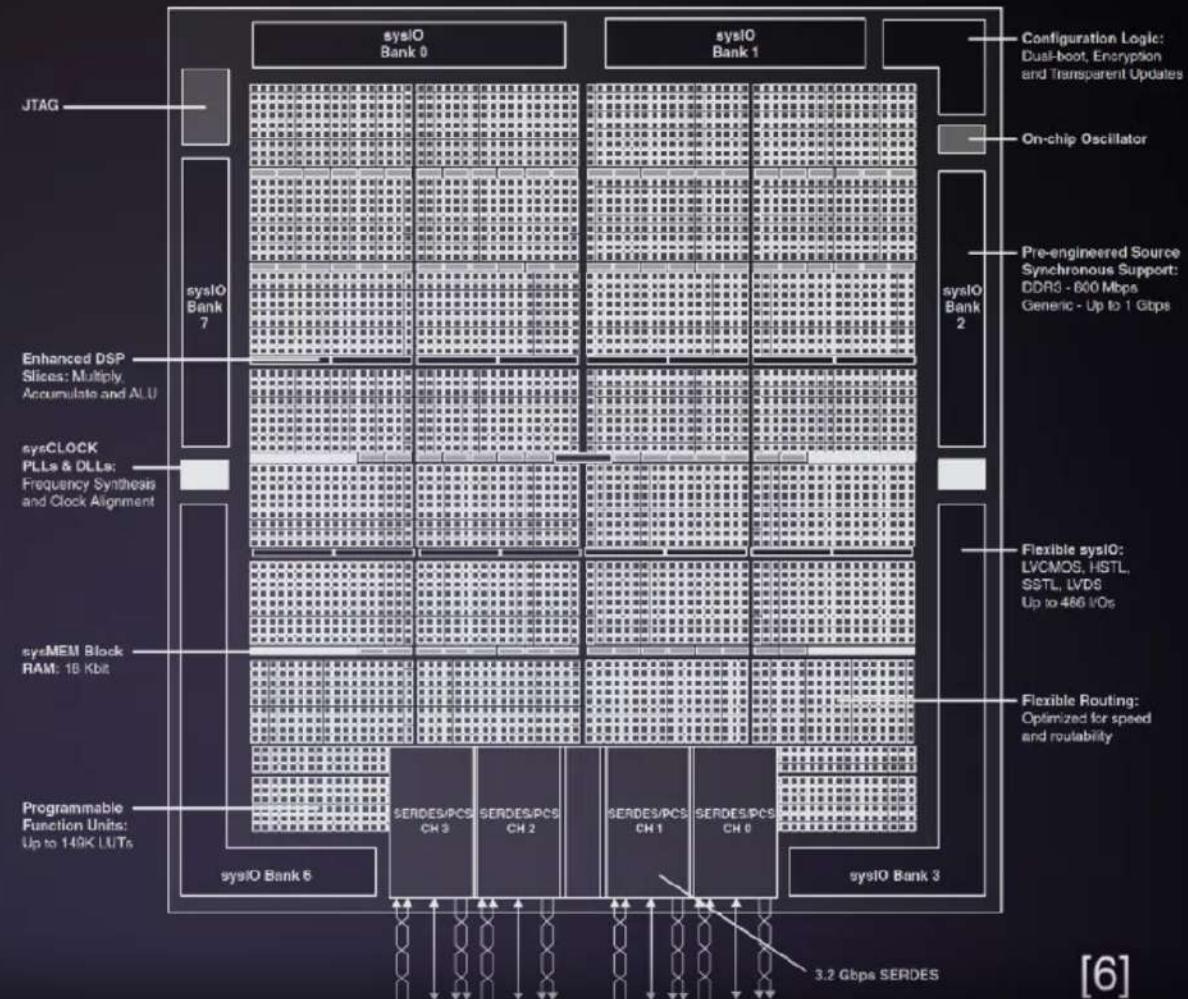
Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2 / 2	4 / 2	10 / 2	10 / 2	10 / 2
Packages and SERDES Channels/ I/O Combinations					
328 csBGA (10 x 10 mm)	2 / 116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586

ECP3 Architecture

Each contains an array of logic blocks surrounded by Programmable I/O Cells (PIC)

sysMEM™ Embedded Block RAM (EBR) and rows of sys-DSP™ Digital Signal Processing slices

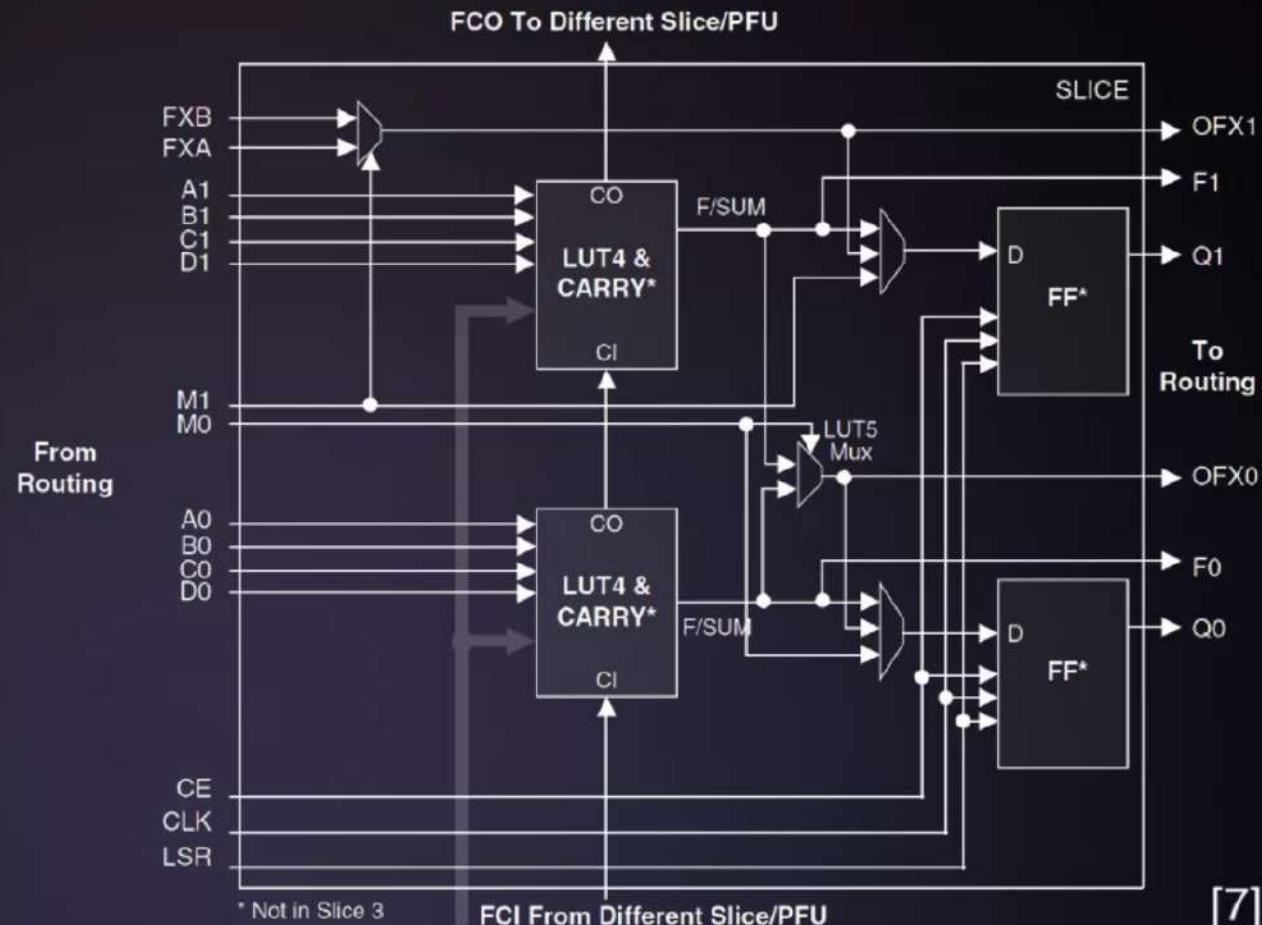
Figure 2-1. Simplified Block Diagram, LatticeECP3-35 Device (Top Level)



ECP3 Slice (Logic Element)

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only

Slice 0 through Slice 2 can be configured as distributed memory.



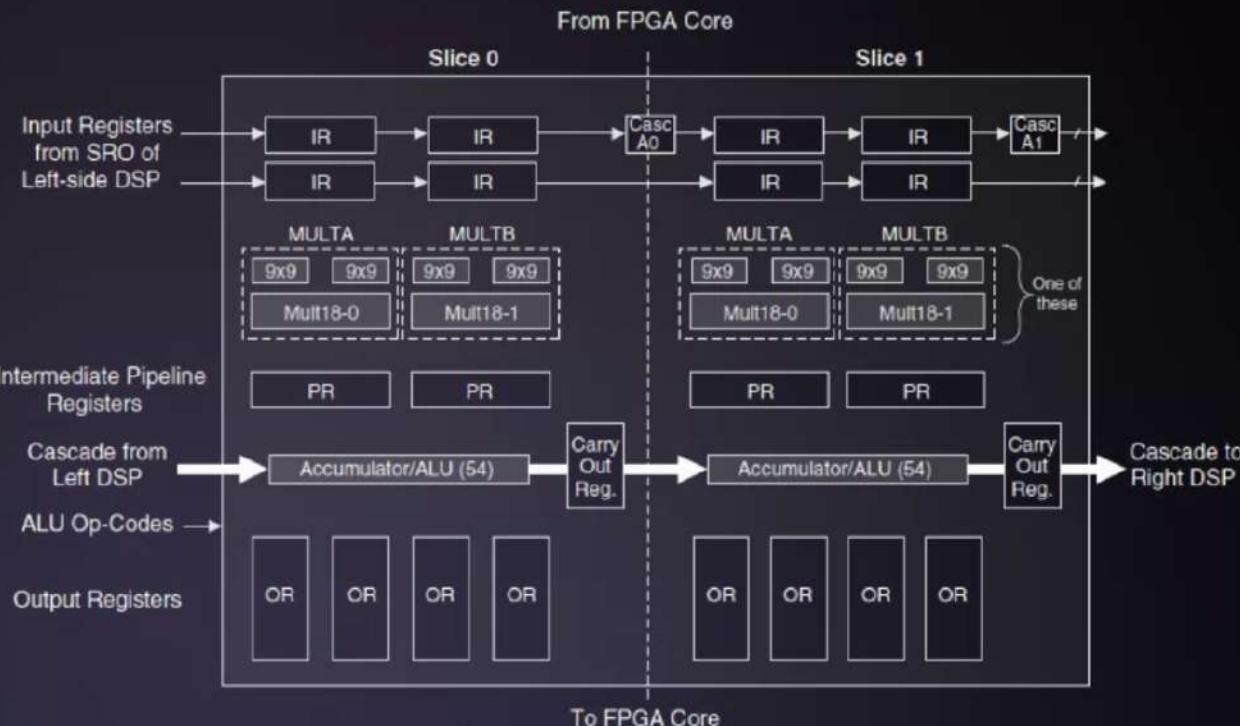
ECP3 DSP Slice

The LatticeECP3 sysDSP Slice supports many functions:

Multiply (one 18x36, two 18x18 or four 9x9 Multiplies)

Multiply (36x36 by cascading across two sysDSP slices)

Multiply Accumulate (up to 18x36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)

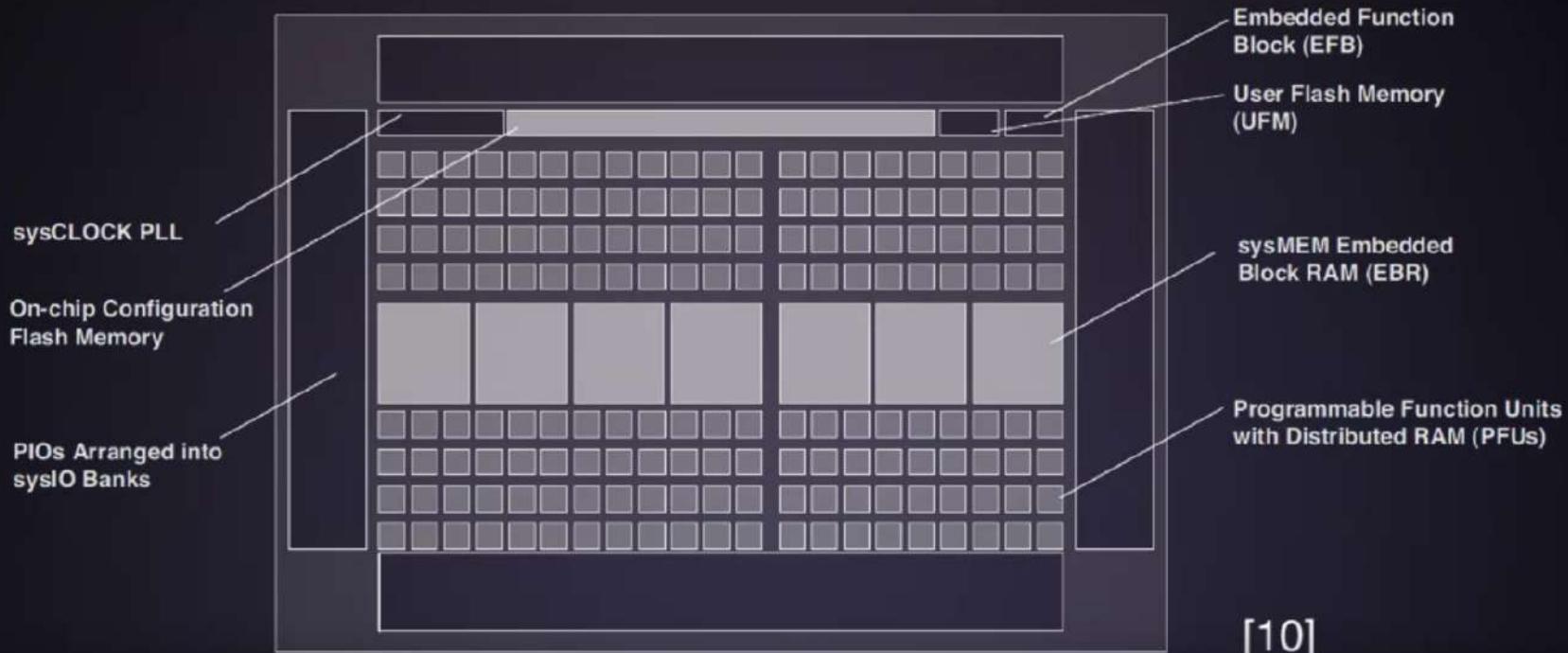


Lattice MACHX02

		XO2-256	XO2-640	XO2-640U ¹	XO2-1200	XO2-1200U ¹	XO2-2000	XO2-2000U ¹	XO2-4000	XO2-7000
LUTs		256	640	640	1280	1280	2112	2112	4320	6864
Distributed RAM (kbits)		2	5	5	10	10	16	16	34	54
EBR SRAM (kbits)		0	18	64	64	74	74	92	92	240
Number of EBR SRAM Blocks (9 kbits/block)		0	2	7	7	8	8	10	10	26
UFM (kbits)		0	24	64	64	80	80	96	96	256
Device Options:	HC ²	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	HE ³						Yes	Yes	Yes	Yes
	ZE ⁴	Yes	Yes		Yes		Yes		Yes	Yes
Number of PLLs		0	0	1	1	1	1	2	2	2
Hardened Functions:	I2C	2	2	2	2	2	2	2	2	2
	SPI	1	1	1	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1	1	1	1

Lattice MACHX02

The MachXO2 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have PLLs and blocks of Embedded Block RAM (EBRs).



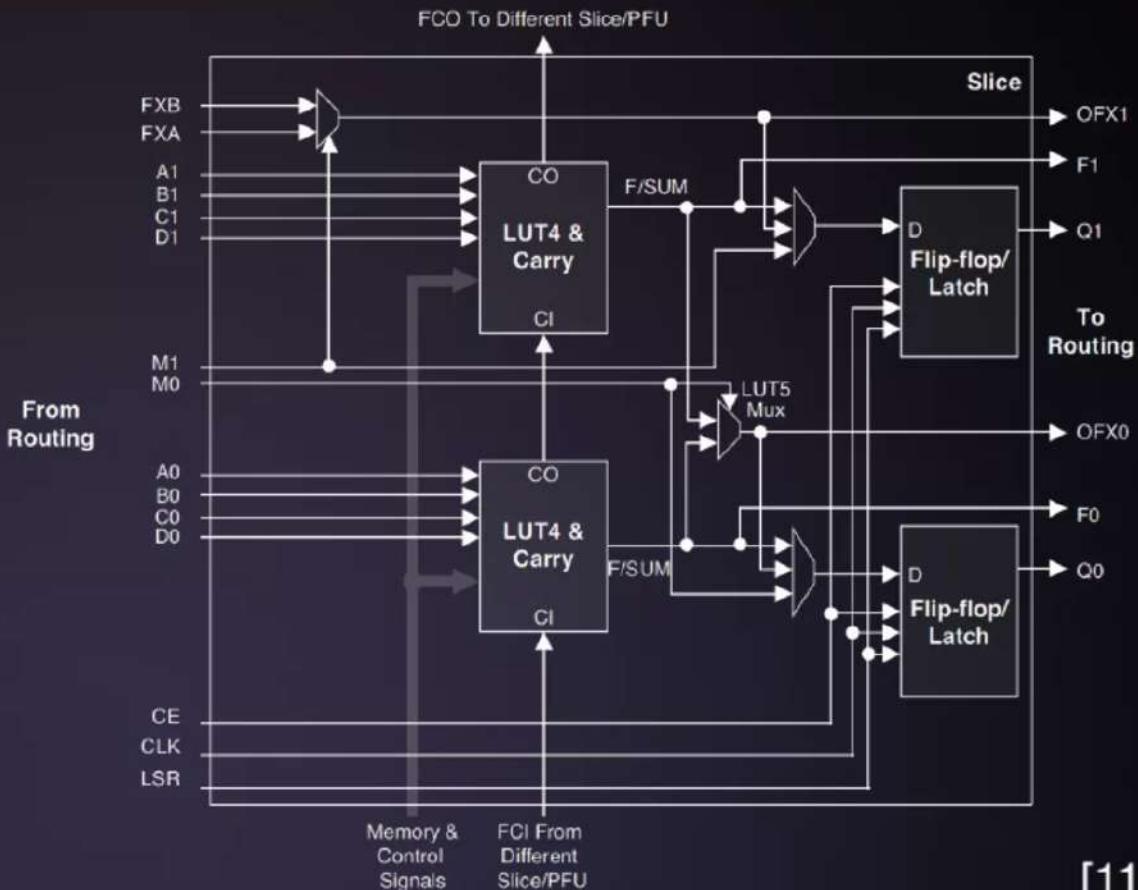
[10]

MACHXO2 Slice (Logic Element)

The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU).

There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU).



[11]

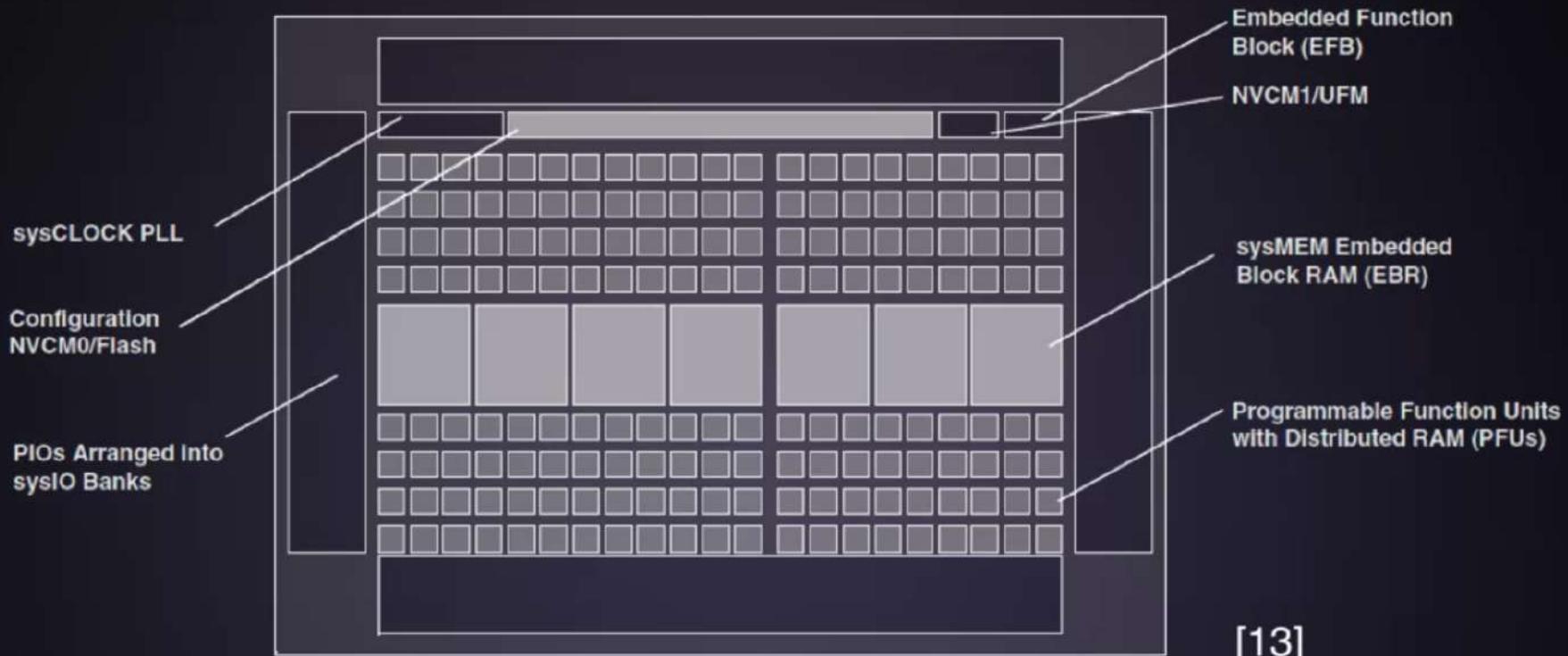
Lattice MACHX03

Features	MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400
LUTs	640	1300	2100	4300	6900	9400
Distributed RAM (kbits)	5	10	16	34	54	73
EBR SRAM (kbits)	64	64	74	92	240	432
Number of PLLs	1	1	1	2	2	2
Hardened Functions:	I ² C	2	2	2	2	2
	SPI	1	1	1	1	1
	Timer/Counter	1	1	1	1	1
	Oscillator	1	1	1	1	1
MIPI D-PHY Support	Yes	Yes	Yes	Yes	Yes	Yes
Multi Time Programmable NVCM	MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400
Programmable Flash	MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400

[12]

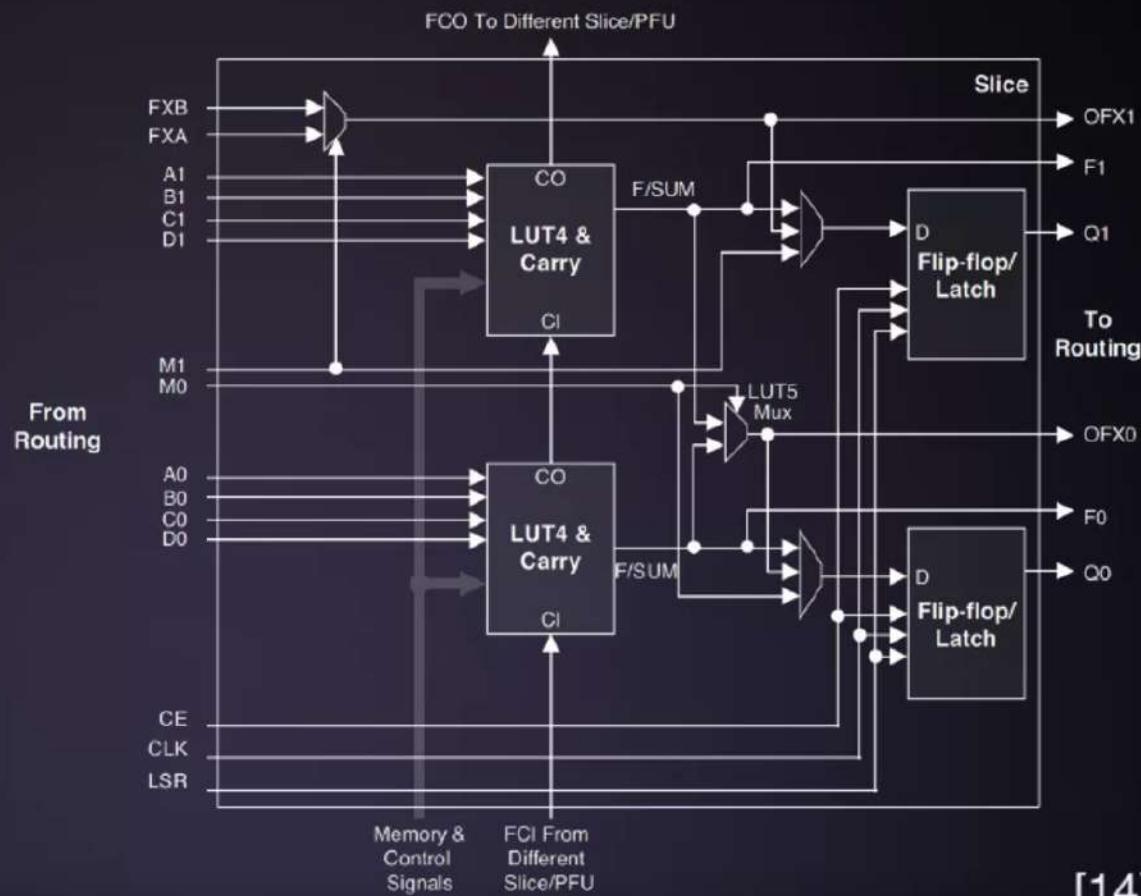
MACHXO3L Architecture

The MachXO3L/LF family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). The larger logic density devices in this family have PLLs and Embedded Block RAM (EBRs).



MACHXO3L Slice (Logic Element)

The MACHXO3 logic element is a slice with 2 LUT4s and 2 flip-flops, identical to the slice in the MACHXO2.



Lattice ICE40 Ultra

Part Number	iCE5LP1K	iCE5LP2K	iCE5LP4K
Logic Cells (LUT + Flip-Flop)	1100	2048	3520
EBR Memory Blocks	16	20	20
EBR Memory Bits	64 k	80 k	80 k
PLL Block	1	1	1
NVCM	Yes	Yes	Yes
DSP Blocks (MULT16 with 32-bit Accumulator)	2	4	4
Hardened I2C, SPI	1,1	2,2	2,2
HF Oscillator (48 MHz)	1	1	1
LF Oscillator (10 kHz)	1	1	1
24 mA LED Sink	3	3	3
500 mA LED Sink	1	1	1
Embedded PWM IP	Yes	Yes	No
Packages, ball pitch, dimension	Total User I/O Count		
36-ball WLCSP, 0.35 mm, 2.078 mm x 2.078 mm	26	26	26
36-ball ucfBGA, 0.40 mm, 2.5 mm x 2.5 mm	26	26	26
48-ball QFN Package, 0.5 mm, 7.0 mm x 7.0 mm	39	39	39

ICE40 Architecture

Array of Programmable Logic Blocks (PLB)

2 Oscillator Generators

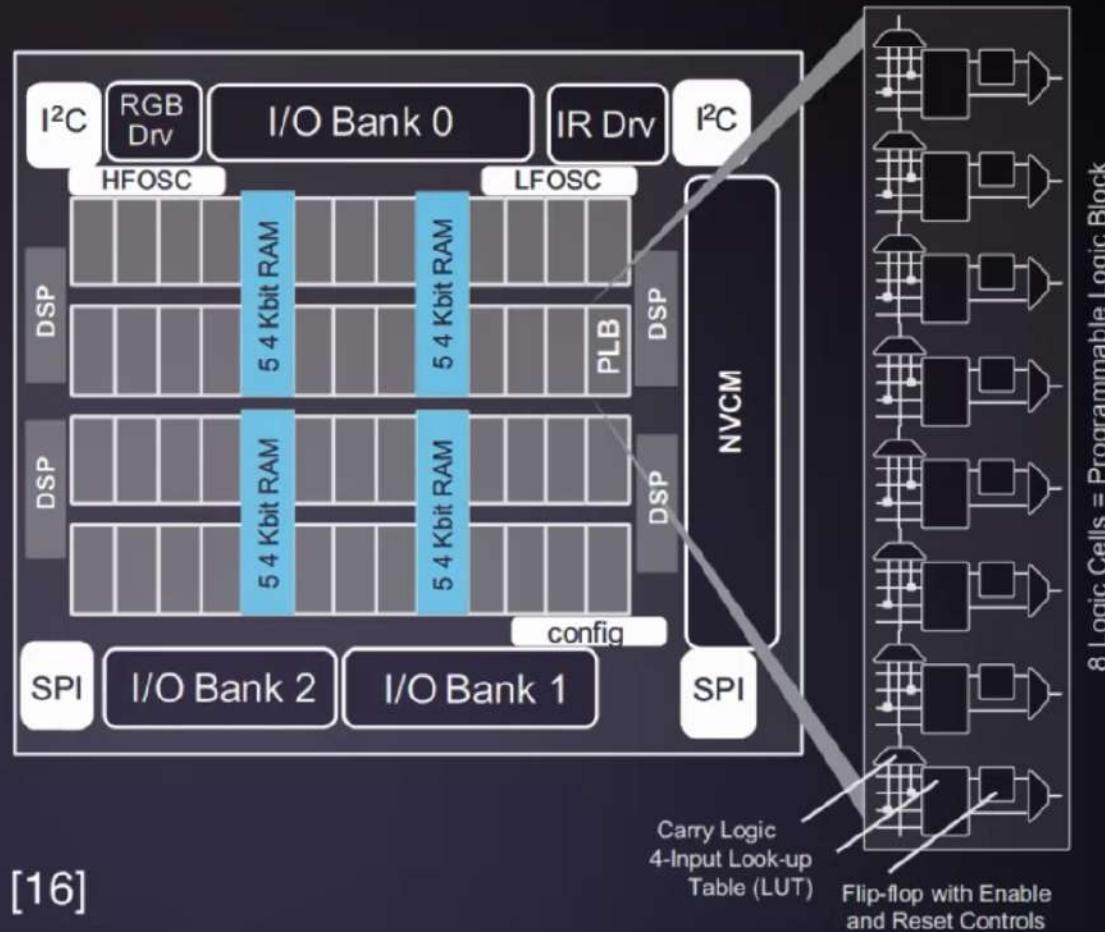
2 user configurable I²C controllers

2 user configurable SPI controllers

DSP Blocks

LED Drivers

Block RAM (EBR) surrounded by Programmable I/O (PIO)



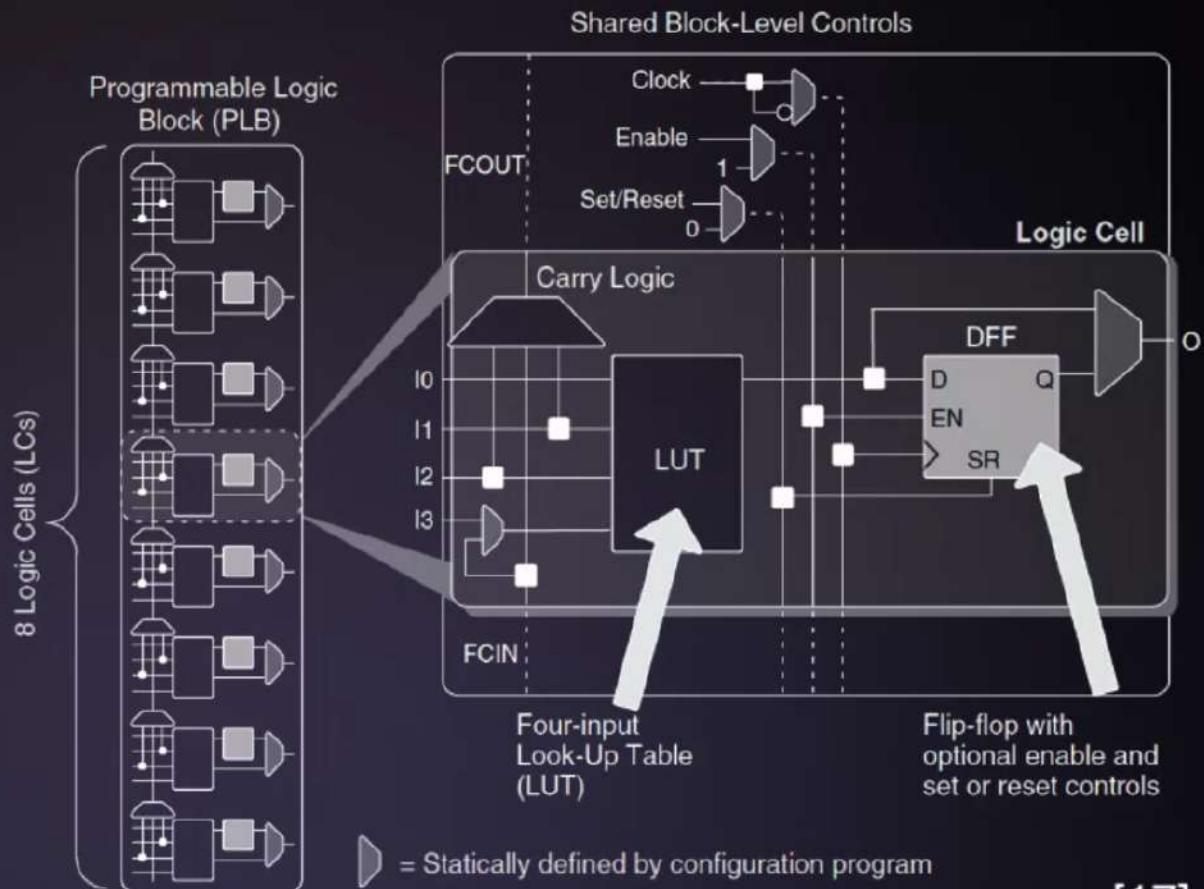
ICE40 Slice (Logic Element)

Core consists of Programmable Logic Blocks (PLB)

Can be programmed to perform logic and arithmetic functions.

Each PLB consists of eight interconnected Logic Cells (LC) as shown.

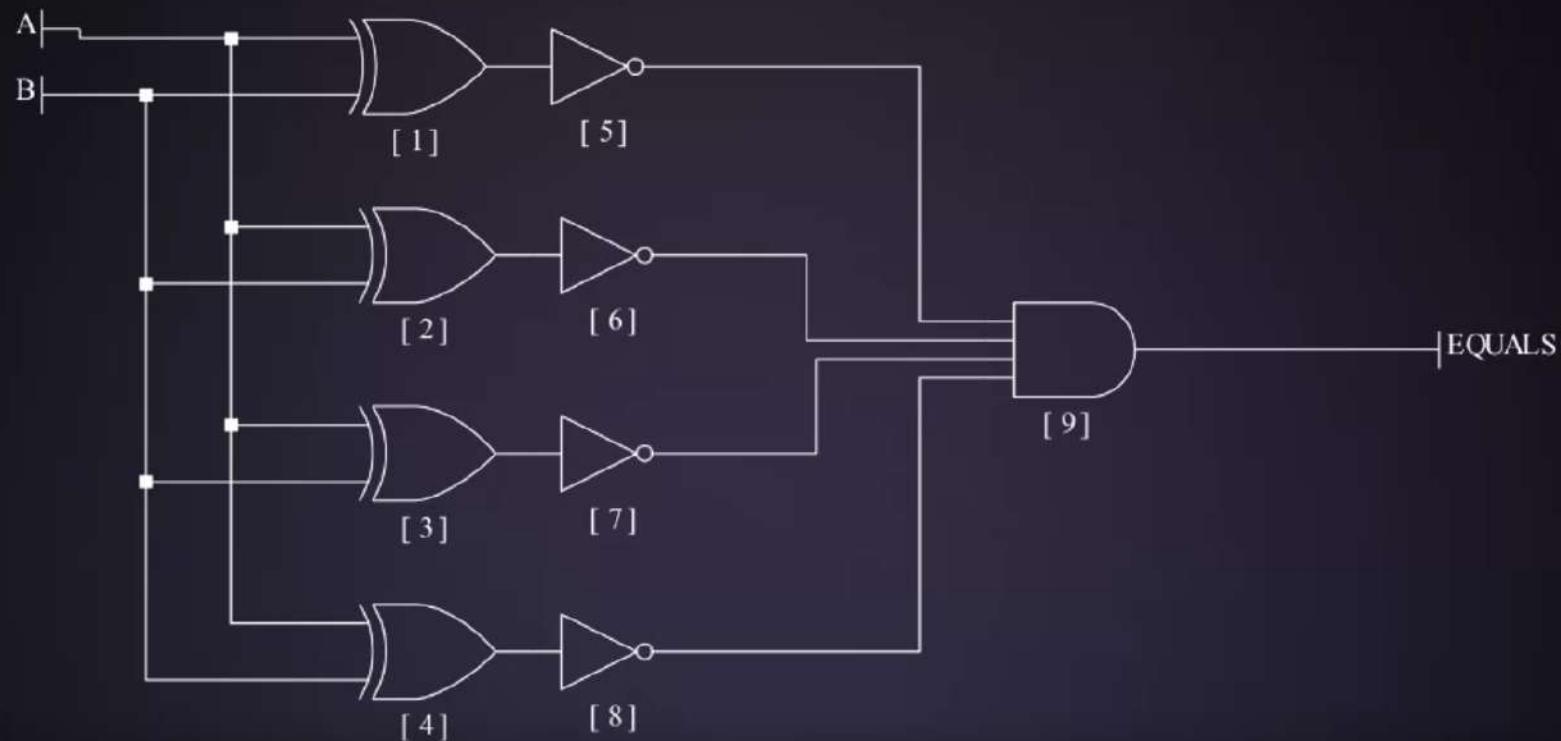
Each LC contains one LUT and one register.



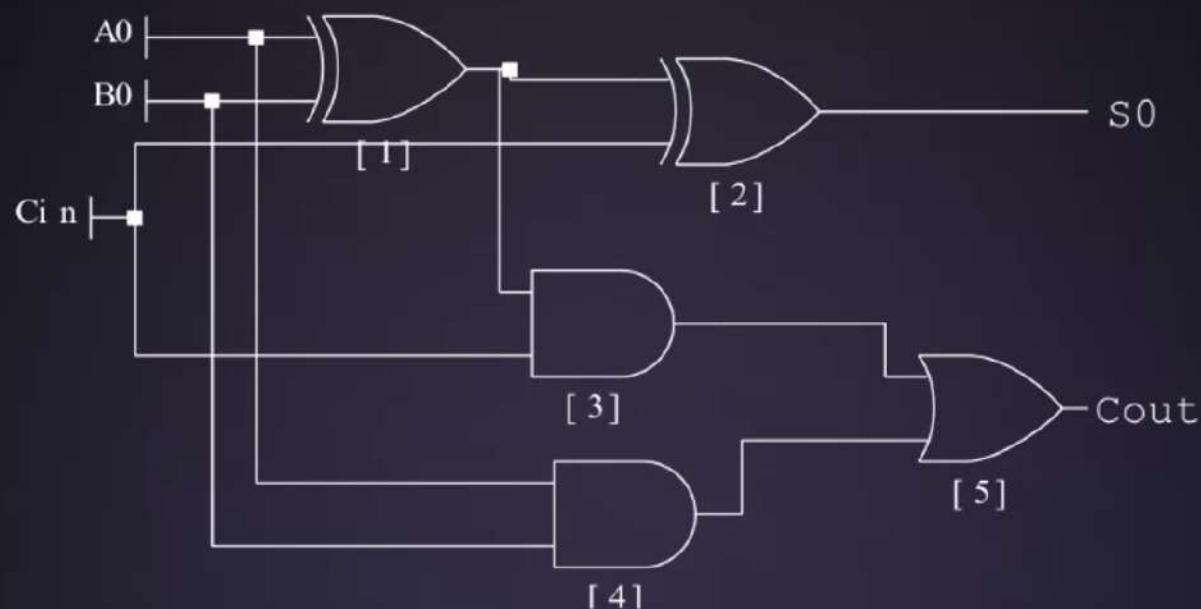
□ = Statically defined by configuration program

[17]

How large of a comparator can be made using a Lattice logic Cell?



How many full adders can be created in a Lattice logic element?



1 bit full adder

Lattice FPGAs Summary

Lattice specializes in low cost high value small to medium size programmable logic parts, including the iCE40, MACHXO2, MACHXO3, ECP3 and ECP5 families.

The MACHXO2 and MACHXO3 devices are single chip solutions with on-chip nonvolatile configuration memory storage, but routing controlled by SRAM cells that must be loaded on power up. These devices feature low power, very small size down to 2.5 x 2.5 mm, and several hard IP blocks.

Lattice FPGAs Summary

The iCE40 family includes an abundance of hard IP functions for such a small part, and very low power consumption.

Lattice devices all have logic elements based on a 4 input LUT and register, adequate but somewhat less capable than other offerings.