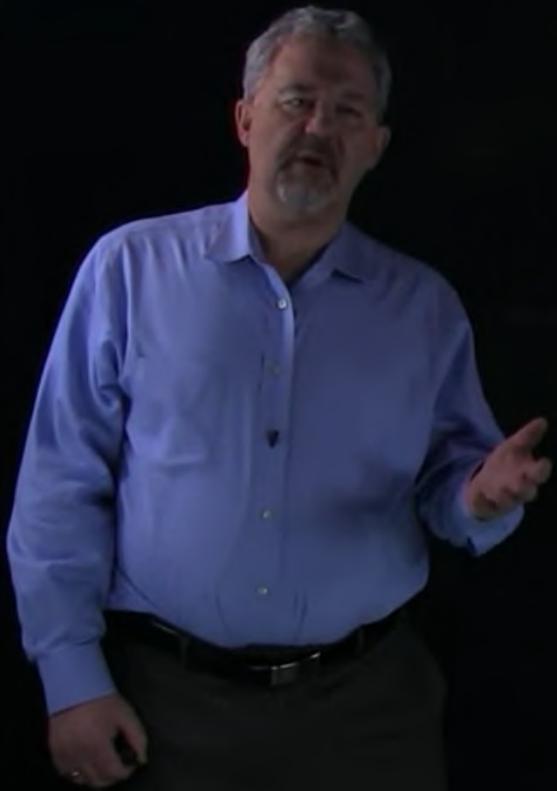


FPGA Design for Embedded Systems

FPGA Softcore Processors and IP Acquisition

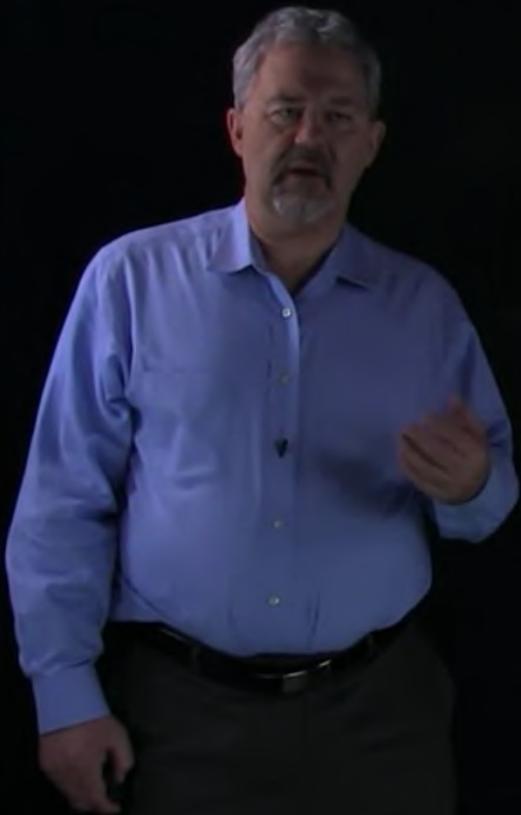
An Introduction to IP Cores



Modern FPGA design is no longer centered on HDL module design as it is on acquisition and use of IP Cores

In this Module we will introduce IP cores including offerings from all the major vendors, Intel Altera, Xilinx, Microchip Microsemi, and Lattice. You will learn how to find, acquire, and use these cores.

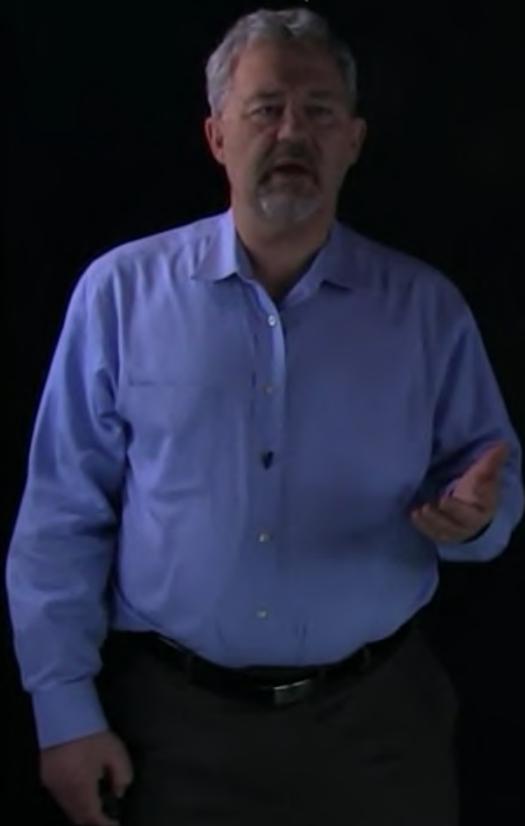
An Introduction to IP Cores



IP Core Acquisition

The breadth of IP Core offerings is astounding. It includes Processors, DSP, Communications, Interface, Memory, Audio/Video, Controls and Security IP in a range from simple devices, such as counters all the way to complex devices like 32-bit customized soft processors.

An Introduction to IP Cores

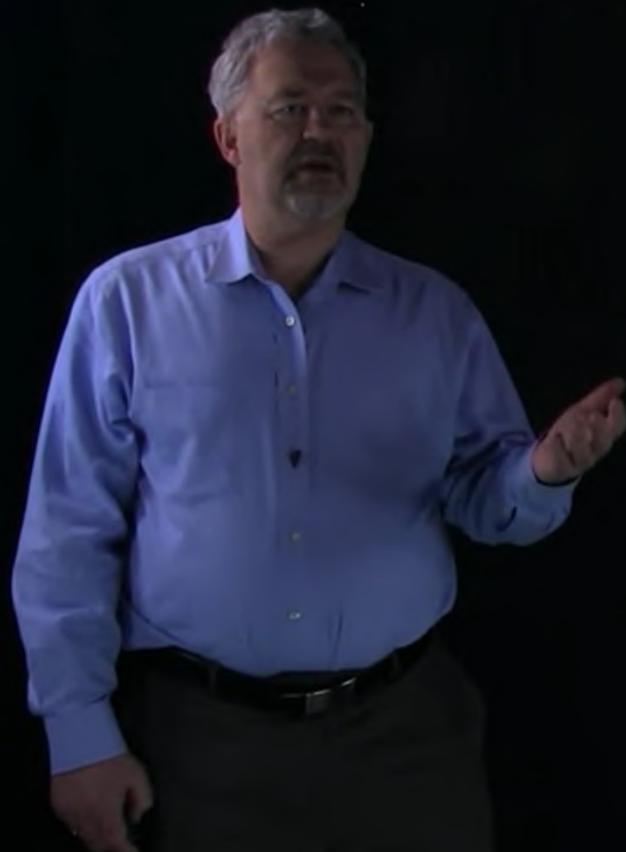


IP Core Utilization

IP cores can be included in your design in a number of ways:

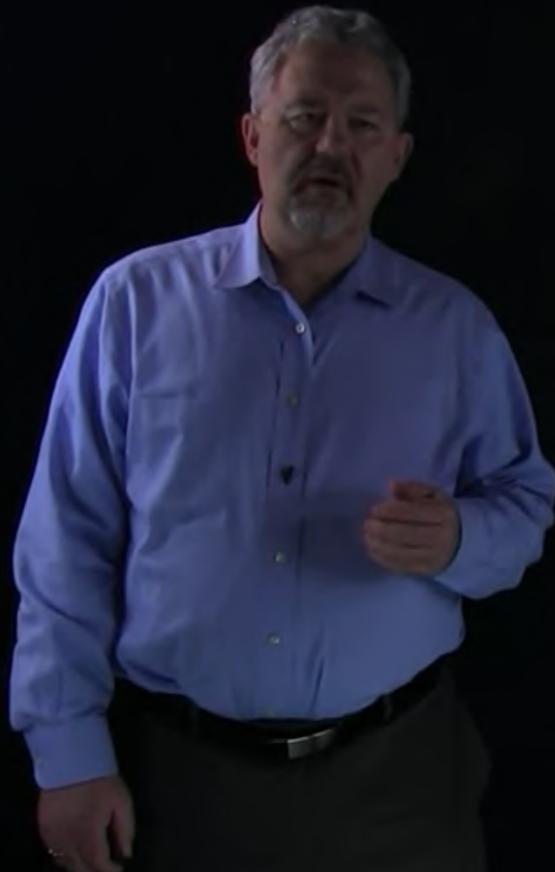
- You can **instantiate the cores in your HDL** design using the top-level port definitions.
- In some cases, IP can be added as a block diagram element in a high-level system diagram with **wired connections added graphically**.
- Yet another way is to use a **system level design tool** like Qsys which allows you to incorporate the IP into the design directly.

Videos in this Module



1. Introduction to IP Cores
2. Microsemi IP Cores
3. Intel Altera IP Cores
4. Xilinx IP Cores
5. Lattice IP Cores
6. Use of IP cores with Qsys

Microsemi IP Cores



In this video, you will learn:

- What is available from Microsemi as IP Cores, including Processors, DSP, Communications, Interface, Memory, Audio/Video, Controls and Security
- How to integrate the IP in a Microsemi Design
- How to find 3rd party IP for Microsemi FPGA Devices

Microsemi IP Cores



Microsemi develops and supports DirectCore IP Cores for applications with the widest possible interest. Most DirectCores are available for free within our Libero tool suite. Common communications interfaces, peripherals and processing elements are all available as DirectCores.



Microsemi CompanionCore Partners use their detailed system knowledge of common applications to craft optimized solutions targeted for Microsemi SoC FPGAs and FPGAs. CompanionCores are available for purchase from our partners and are easily integrated into your design using our Libero tool suite.

Connectivity	Ethernet	Connectivity	Processor
DSP	Security	DSP	Security
Memory Controller	Error Correction	Memory Controller	Error Correction
Processor	Imaging and Video	Imaging and Video	Machine Learning



Microsemi Direct IP Cores

Core10/100	Communications	CoreAPB	Interface	CoreFROM	Memory	CoreRMII	Interface
Core10/100_AHBAPB	Communications	CoreAPB3	Interface	CoreGPIO	Interface	CoreRSDEC	DSP
Core10GMAC	Communications	CoreAPBLSRAM	Memory	CoreHPDMACtrl	Memory	CoreRSENC	DSP
Core1553BRM*	Interface	CoreApbNvm	Memory	CoreI2C	Interface	CoreSDLC	Communications
Core1553BRT_		CoreAPBSRAM	Memory	CoreInterrupt	Embedded	CoreSDR	Memory
Core1553BRT_APB*	Interface	CoreAXI	Interface	CoreJESD204BRX	Interface	CoreSDR_AHB	Memory
Core1588	Communications	CoreAXItoAHBL	Interface	CoreJESD204BTX	Interface	CoreSDR_AXI	Memory
Core16550	Communications	CoreCFI	Memory	CoreLPC	DSP	CoreSF2Config	Embedded
Core3DES	Security	CoreCIC*	DSP	CoreMACFilter	DSP	CoreSF2Reset	Embedded
Core429*, Core429_APB*	Interface	CoreConfigMaster	Embedded	CoreMBX	Interface	CoreSGMII	Communications
Core8051s	Embedded	CoreConfigP	Embedded	CoreMDIO_APB	Interface	CoreSMIP	Security
CoreABC	Embedded	CoreCORDIC	DSP	CoreMemCtrl	Memory	CoreSPI	Interface
CoreAES128	Security	CoreDDR	Memory	CoreMMC	Memory	CoreSysServices	Embedded
CoreAHB	Interface	CoreDDS	Embedded	CorePCIF		CoreTBitoEPCS	Interface
CoreAHB2APB	Interface	CoreDES	Security	CorePCIF_AHB	Interface	CoreTimer	Embedded
CoreAHBLite	Interface	CoreEDAC	Error Correction	CorePCS	Interface	CoreTSE_AHB , CoreTSE	Communications
CoreAHBLSRAM	Memory	CoreFFT	DSP	CorePWM	Controls	CoreUART	Communications
CoreAHBLtoAXI	Interface	CoreFFT*	DSP	CoreQDR	Memory	CoreUART_APB	Communications
CoreAhbNvm	Memory	CoreFIFO	Memory	CoreQDR	Memory	CoreWatchdog	Embedded
CoreAhbSram	Memory	CoreFIR	DSP	CoreQEI	Controls	Cortex-M1	Embedded
CoreAHBtoAPB3	Interface	CoreFME	Memory	CoreRemap	Interface	MiV_RV32IMAF_L1_AHB	Embedded
CoreAI	Interface			CoreResetP	Embedded	RISC-V_AXI4	Embedded
				CoreRGMI	Communications		



Microsemi Companion IP Cores

80186EC	Embedded
80188XL Processor	Embedded
8237 DMA Controller	Embedded
8251 Serial Controller	Communications
8254 Programmable Timer	Embedded
8259A Interrupt Controller	Embedded
AES Key Wrap and Unwrap cores	Security
Alma AES-GCM128	Security
Alma H264-MP-E	Audio/Video
Alma JPEG-D-X	Audio/Video
Alma LJPEG-E	Audio/Video
Alma MD5	Security
Alma SHA1	Security
Alma SHA256	Security
Alma SPI	Communications
Alma UHT-JPEG-E	Audio/Video
Alpha Blender	Audio/Video
ARINC-818 IP Core	Communications
ATAPI Host Controller	Memory
Athena Advanced True Random Number	Security
Athena AES-A500	Security
Athena BFFT-M	DSP
Athena EC Ultra	Security

Athena F5200 Public Key	Security
Microprocessor	
Athena Fast AES-GCM	Security
Athena PPFFT-M	DSP
Athena RNG-A200	Security
Athena SHA2-A300	Security
Athena SNOW-A100	Security
Audio Video (AV) IP Core	Video
Bitec DisplayPort 1.4a	Audio/Video
Bitec HDMI 2.0b	Audio/Video
Camera Interface	Audio/Video
CAN	Communications
CANmodule-IIIx	Communications
CE-ATA 1.1	Storage
Chroma down Resampler	Audio/Video
Chroma Up Resampler	Audio/Video
Color Space Converter	Audio/Video
Common Scrambling Algorithm (DVB-CSA) cores	Security
Crest Factor Reduction	Communications
D16550	Communications
D68HC11K	Embedded
Digital Predistortion	Communications
DLIN	Communications
DUARTmodule	Communications
ECC1	Security

EP550	Memory SD
EP553	Memory e.MMC
Fast AES Encryptor and Decryptor	Security
Fast SHA-256 hashing core	Security
GPIOmodule	Bus Interfaces
GRFPU	Embedded
H.264-15 Encoder	Audio/Video
H16550S	Communications
Image Rotation	Audio/Video
iniADPLL	Embedded
iniCAN	Communications
iniCPU	Embedded
iniG704-E1	Communications
iniHDLC	Communications
iniSCI master	Bus Interfaces
iniSCI slave	Bus Interfaces
iniUART	Communications
INTCmodule	Embedded
Integrated SD/SDIO/MMC/CE-ATA	Storage
iW-Multibus II	Bus Interfaces
iW-NAND Flash Controller	Storage
iW-VME	Bus Interfaces
LCD HDMI Video Output Interface	Audio/Video
LCD Interface	Audio/Video

LEON3	Embedded
LIN	Bus Interfaces
Multiplexed Keypad	Bus Interfaces
Interface Core (PERDYN11088)	
PCI Express	Bus Interfaces
PCI Express	Bus Interfaces
Expresso DMA Bridge	
PCI-M32	Bus Interfaces
Remote Direct Memory Access (RDMA) IP Core	Communications
RTCmodule	Embedded
SCR-APB	Embedded
SD 2.0 Controller	Storage
SD/SDIO/MMC Controller	Storage
SecureRF AEcore	Security
Serial Front Panel	Communications
Data Port (sFPDP) IP Core	
Spacewire	Communications
SPIModule	Bus Interfaces
Standard AES Encryptor and Decryptor	Security
TIMERmodule	Embedded
TinyPlus AES Encryptor and Decryptor	Security
UARTmodule	Communications
Video Decoder Interface	Audio/Video
Video DeInterlacer	Audio/Video
Video Encoder Interface	Audio/Video
Video Scaler	Audio/Video
VME64s	Bus Interfaces

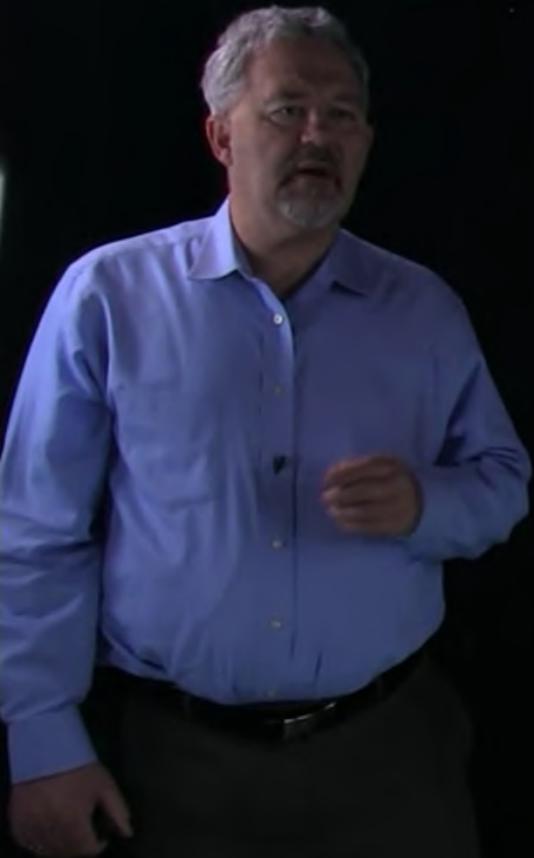


Microsemi IP Core Use

You searched for: Device: DirectCores					101 results found.
Still can't find what you are looking for? Please send a request to soc_marketing@microsemi.com					
	Name	Function	Devices	Try It Now	Resources
▶ Website Migration ▶ SoC Customer Portal ▶ My Cases ▶ Licensing ▶ IP Search ▶ Knowledge Base Search	ARM Cortex M1 DirectCore	ARM 32-bit FPGA Optimized Processor	Processors & Peripherals	ProASIC3 Fusion IGLOO	<ul style="list-style-type: none">• Register your Design• Cortex M1 Webcast - Small, Fast, and Free• Cortex-M1 Cortex M1 Web Page• Cortex-M1 Release Notes• Cortex-M1 Handbook • Cortex-M1 Product Brief• Cortex-M1 Technical Reference Manual• DirectCore IP Cores
	ARM Cortex-M1 DirectCore	ARM Cortex-M1 processor	Processors & Peripherals	RTG4 PolarFire	<ul style="list-style-type: none">• Register your Design• Hand Book for PolarFire • Hand Book for RTG4• Release Notes for PolarFire• Release Notes for RTG4
	Core10100 DirectCore	10/100 Mbps Ethernet MAC with Host Controller	Communications Ethernet	IGLOO2 IGLOO nano ProASIC3 ProASIC3L Fusion	<ul style="list-style-type: none">• Register your Design• Core10/100 Conformance Test Report• Core10/100 Brochure• Core10/100 Release Notes• Core10/100 Handbook 



Microsemi IP Core Use



Libero - C:\Microsemiprj\SC_standalone\polled_uart\UART\UART.prj*

Project File Edit View Design Tools SmartDesign Help

Catalog Simulation Mode

Name / Version

Basic Blocks

Bus Interfaces

- CoreAHB 1.3.101
- CoreAHB2APB 1.1.101
- CoreAHBLite 5.4.102
- CoreAHtoAPB3 3.1.100
- CoreAPB 1.1.101
- CoreAPB3 4.1.100
- CoreAXI4Interconnect 2.1.100
- CoreAXITOAHBL 3.4.100
- CorePCIF 4.2.100
- CorePCIF_AHB 4.2.100

Clock & Management

- Clock - Delayed 2.1

DSP

- CoreCordic 4.0.102
- CoreRSDEC 3.6.104
- CoreRENC 3.5.102

Macro Library

- AND2 1.0
- AND2A 1.0
- AND2B 1.0
- AND3 1.0

Documentation:

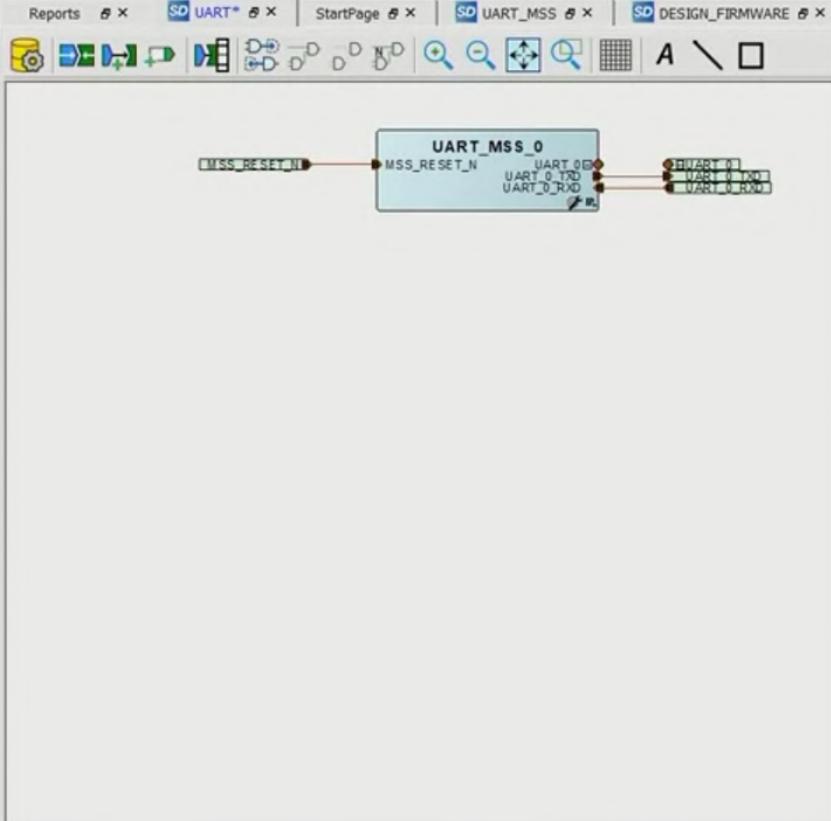
- [CoreAPB3_HB.pdf](#)
- [CoreAPB3_RN.pdf](#)

Description:

The CoreAPB3 component implements an APB3 (AMBA3 APB) fabric, which is backwards compatible with APB2 slave peripherals.

There is one APB3 Master Interface.

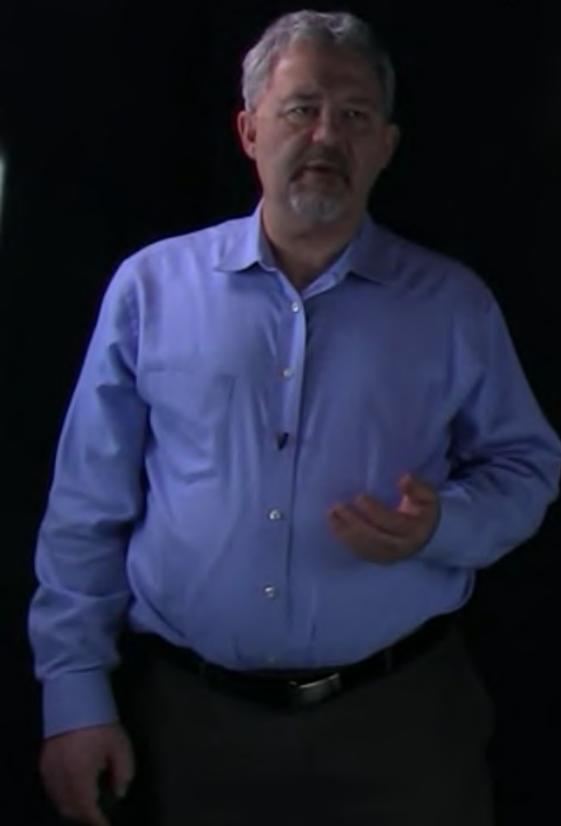
Design Flow Design Hierarchy Catalog Files



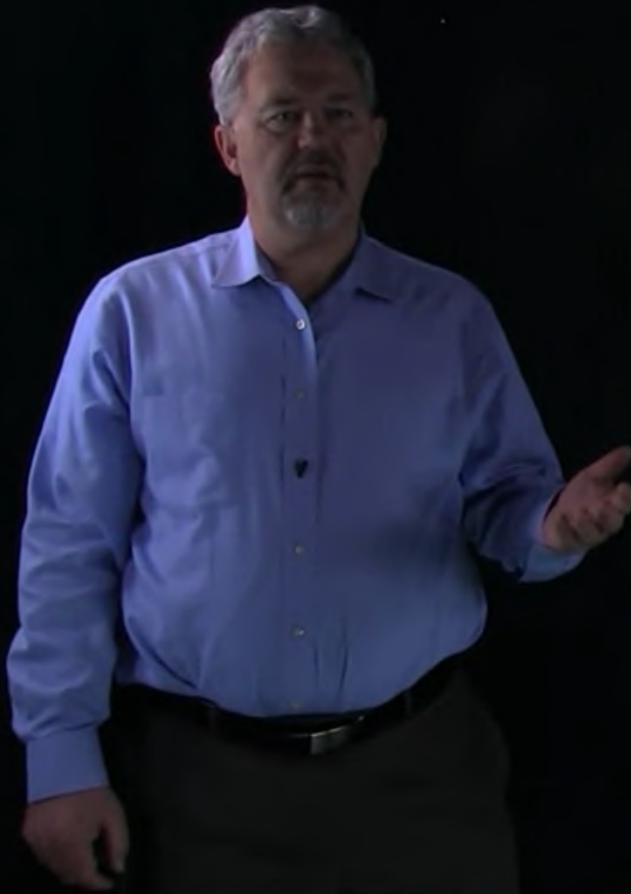
Summary

In this video, you have learned:

- What is available from Microsemi as IP Cores, including Processors, DSP, Communications, Interface, Memory, Audio/Video, Controls and Security
- How to integrate the IP in a Microsemi Design
- How to find 3rd party IP for Microsemi FPGA Devices



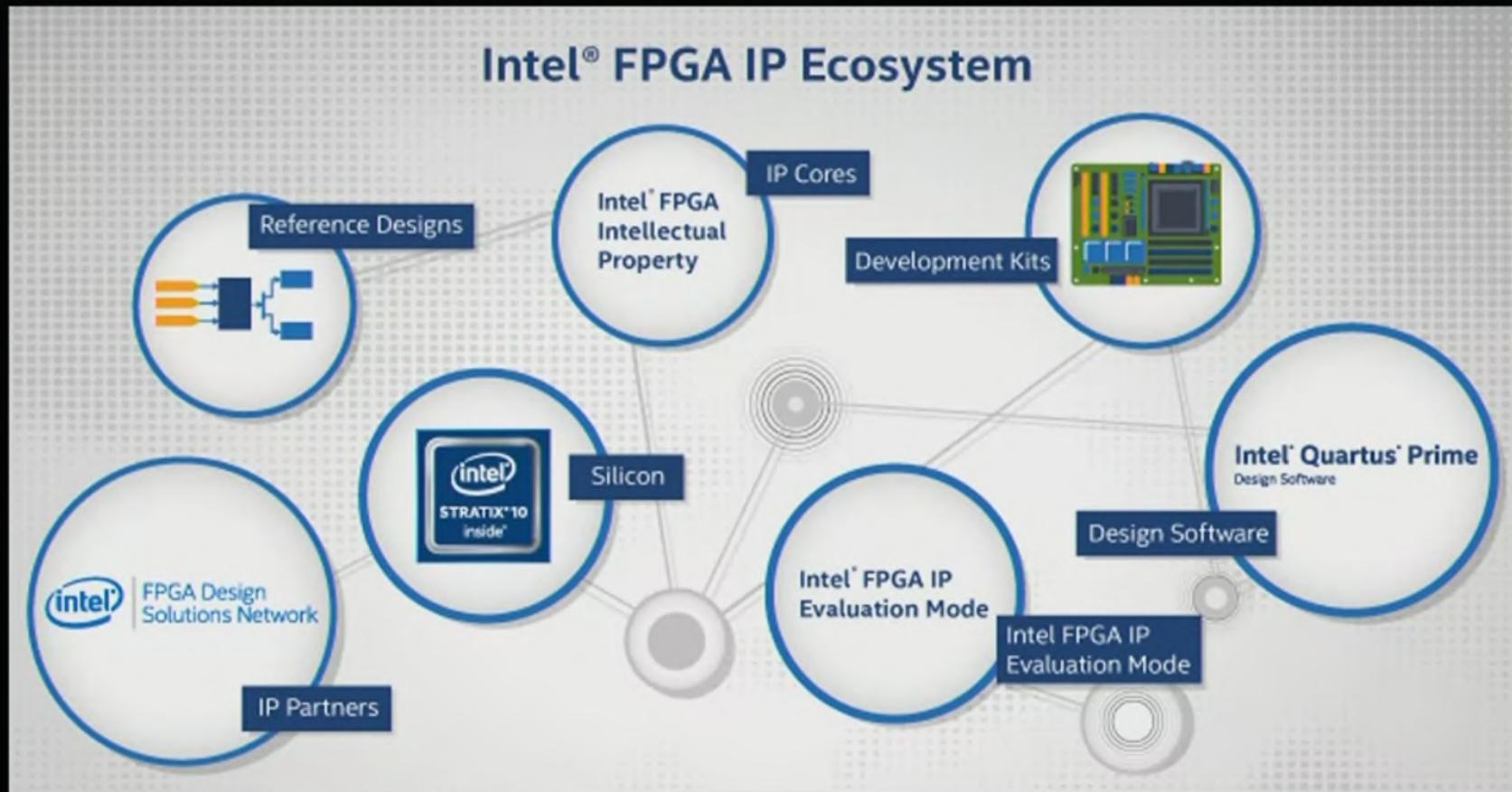
Intel Altera IP Cores



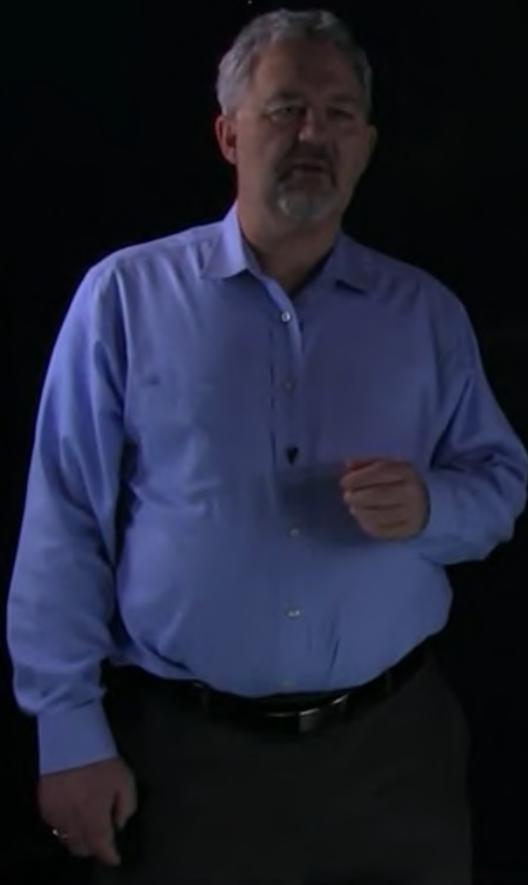
In this video, you will learn:

- What is available from Altera as IP Cores, including Processors, DSP, Communications, Interface, Memory, Audio/Video, Controls and Security
- How to integrate the IP in an Altera Design
- How to find 3rd party IP for Altera FPGA Devices

Intel Altera IP Cores



Intel Altera IP Cores



- IP Included In Quartus

Intel delivers intellectual property (IP) as part of the IP catalog, which is built into the Intel® Quartus® Prime and Quartus II software.

- Broad Portfolio

The portfolio includes IP for protocol and memory interfaces, digital signal processing (DSP), embedded processors, and related peripherals.

- Tested

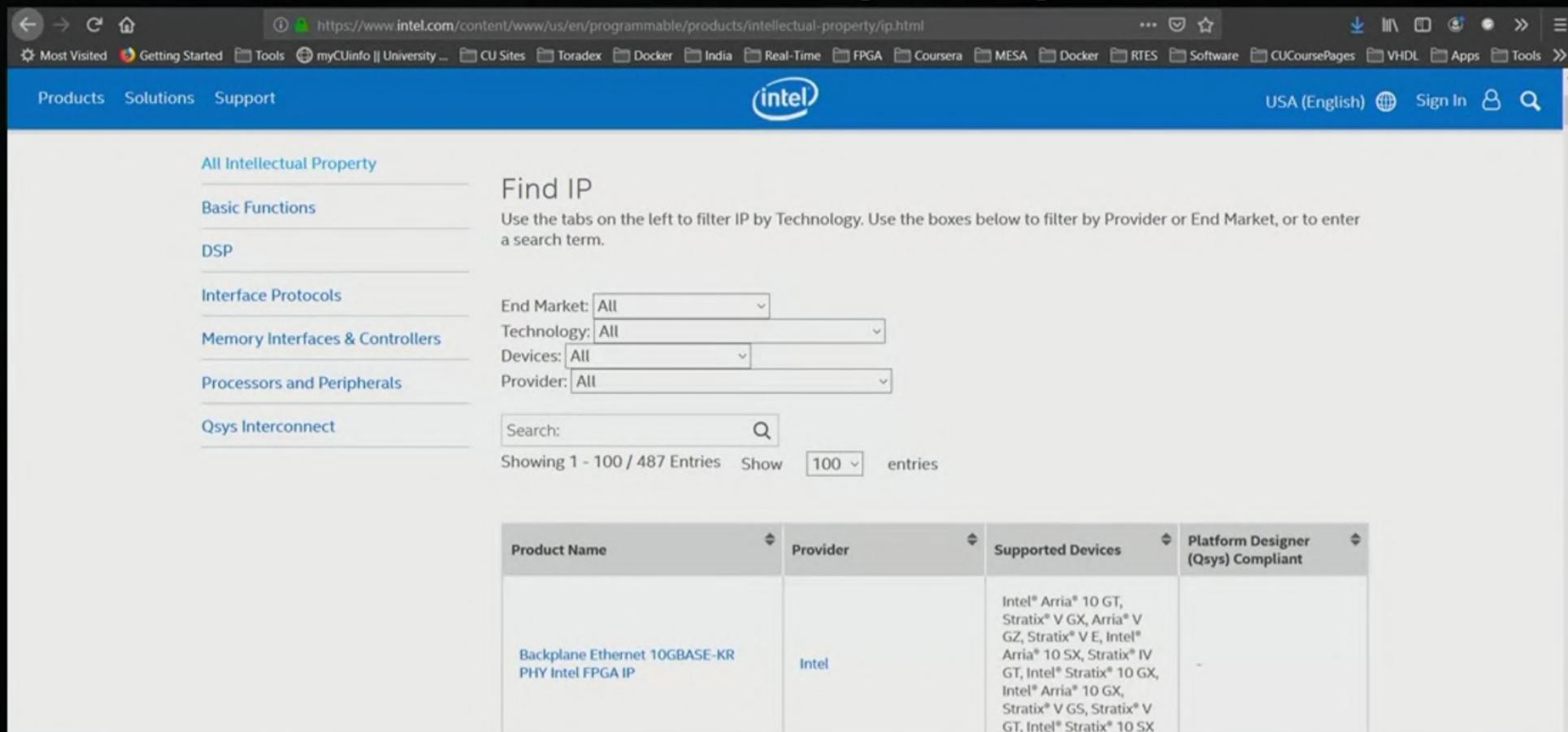
All the IP cores have been thoroughly tested and verified on hardware to provide you the assurance that they will work well together in your system.

Intel Altera IP Cores

ALTERA_CORDIC	DSP	ROM: 1-PORT	Memory	Clocked Audio Input	Audio/Video	NIOS II Bitswap	Processors
ALTERA_MULT_ADD	DSP	ROM: 2-PORT	Memory	Clocked Audio Output	Audio/Video	NIOS II Floating Point Hardware	Processors
ALTFP_ADD_SUB	DSP	Altera SignalTap II Logic Analyzer	Utility	DisplayPort	Audio/Video	Altera I2C Slave To Avalon MM	Processors
ALFPT_ATAN	DSP	Altera In-System Sources and Probes	Utility	SDI II	Audio/Video	Master Bridge	Processors
ALTFP_DIV	DSP	USB Debug Link	Utility	Ethernet 10G MAC	Communications	Lauterbach Trace Interface IP	Processors
ALTFP_EXP	DSP	Altera Avalon Interrupt Sink	Processor	XAUI PHY	Interface	Vectored Interrupt Controller	Processors
ALTFP_LOG	DSP	Altera Avalon Interrupt Source	Processor	TSE	Communications	16x2 Character Display	Audio/Video
ALTFP_MULT	DSP	Altera Avalon-MM Monitor	Interface	Ethernet IEEE 1588 TOD Synchronizer	Communications	Audio and Video Config	Audio/Video
ALTFP_SINCOS	DSP	Altera Avalon-ST Monitor	Interface	Ethernet IEEE 1588 Time of Day Clock	Communications	IrDA UART	Communications
ALTFP_SQRT	DSP	Altera Clock Source BFM	Utility	Ethernet Packet Classifier	Communications	RS232 UART	Communications
LPM_ADD_SUB	DSP	Altera External Memory BFM	Interface	JESD204B	Interface	PS/2 Controller	Interface
LPM_COUNTER	DSP	Altera Avalon Data Pattern Checker	Interface	PHY IP Core for PCI Express (PIPE) v16.1	Interface	USB Controller	Communications
LPM_DIVIDE	DSP	Altera Avalon Data Pattern Generator	Interface	RapidIO II (IDLE2 up to 6.25 Gbaud)	Interface	Altera UP Flash Memory IP Core	Memory
LPM_MULT	DSP	Avalon-MM Traffic Generator and BIST	Engine	Utility		SD Card Interface	Memory
JTAG to Avalon Master Bridge	Utility	BCH	Security	Avalon-ST Serial Peripheral Interface (SPI)	Interface	SRAM/SSRAM Controller	Memory
ALTCLKCTRL	Utility	High-Speed Reed-Solomon	Security	SerialLite II v16.1	Interface	100G Ethernet Intel® FPGA IP Core	Communications
Altera PLL	Utility	LDPC	Security	Transceiver PHY Reset Controller	Interface	1G/2.5G/5G/10G Multi-Rate	Communications
Altera Config Debug Agent	Utility	Random Number Generator	Security	Transceiver Reconfiguration Controller	Interface	Ethernet PHY Intel FPGA IP	Communications
Altera Remote Update	Utility	Turbo	Security	Custom PHY v16.1	Interface	10G PDH/SONET/SDH Packet	Communications
Altera Serial Flash Loader	Utility		Communications	Cyclone V Transceiver PLL v16.1	Interface	Mapper (TPW192-S)	Communications
Internal Oscillator	Utility	Viterbi		Hybrid Memory Cube (HMC) MegaCore	Memory	40 Gbps Ethernet MAC and PHY	Communications
Altera Advanced SEU Detection	Security	CIC	DSP	DDR2 SDRAM Controller with UniPHY	Memory	Intel FPGA HDMI IP Core	Audio/Video
ALTDDIO_BIDIR	Controls	FIR II	DSP	DDR3 SDRAM Controller with UniPHY	Memory	Intel® FPGA IP for PCI Express*	Communications
LPM_SHIFTREG	Utility	Floating Point Hardware 2		LPDDR2 SDRAM Controller with UniPHY	Memory	Low Latency Ethernet 100G MAC	Communications
FIFO	Memory	Combinatorial	DSP			and PHY Intel FPGA IP	Communications
RAM: 1-PORT	Memory	Floating Point Hardware 2 Multi-cycle	DSP			PCI Express	Interface
RAM: 2-PORT	Memory	NCO	Utility			QDR II SRAM Controller Intel®	
		FFT	DSP			FPGA IP	
						SerialLite IV Streaming Intel FPGA IP	Memory
						Video and Image Processing Suite	Communications
						Intel® FPGA IP	Audio/Video



Intel Altera 3rd party IP Cores



The screenshot shows a web browser displaying the Intel IP Core search page. The URL is <https://www.intel.com/content/www/us/en/programmable/products/intellectual-property/ip.html>. The page features a sidebar with categories like All Intellectual Property, Basic Functions, DSP, Interface Protocols, Memory Interfaces & Controllers, Processors and Peripherals, and Qsys Interconnect. The main content area is titled "Find IP" and includes filters for End Market, Technology, Devices, and Provider, as well as a search bar and pagination. A table lists IP cores, including the "Backplane Ethernet 10GBASE-KR PHY Intel FPGA IP" which is provided by Intel and supports various Intel devices.

All Intellectual Property

Basic Functions

DSP

Interface Protocols

Memory Interfaces & Controllers

Processors and Peripherals

Qsys Interconnect

Find IP

Use the tabs on the left to filter IP by Technology. Use the boxes below to filter by Provider or End Market, or to enter a search term.

End Market: All

Technology: All

Devices: All

Provider: All

Search:

Showing 1 - 100 / 487 Entries Show 100 entries

Product Name	Provider	Supported Devices	Platform Designer (Qsys) Compliant
Backplane Ethernet 10GBASE-KR PHY Intel FPGA IP	Intel	Intel® Arria® 10 GT, Stratix® V GX, Arria® V GZ, Stratix® V E, Intel® Arria® 10 SX, Stratix® IV GT, Intel® Stratix® 10 GX, Intel® Arria® 10 GX, Stratix® V GS, Stratix® V GT, Intel® Stratix® 10 SX	-



Intel Altera 3rd party IP Cores

1 Gbps to 400 Gbps Ethernet MAC	Communication	
100Gb/s Gigabit Ethernet IP Solution	Communication	
1553-BC/RT/MT: MIL-STD-1553 Core	Communication	
32 E1/DS1 CES CodeChip	Communication	
40G MAC + PCS (40GBASE-R4)	Communication	
40GbE TCP Offloading EngineIP core	Communication	
80186EC 80186XL Processor	Processor	
8251 Serial Controller	Processor	
8530 Multi-Protocol Controller	Processor	
A429-RxTx: Multichannel ARINC 429	Communication	
AC'97 Controller	Audio/Video	
AES-CCM: Advanced Encryption Standard	Security	
AES-GCM: Advanced Encryption Standard	Security	
AES-P: Programmable Advanced Encryption	Security	
AHB Master	Interface	
AHB Slave	Interface	
AHB to PCI Host Bridge	Interface	
ARINC 818-2 IP Core	Communication	
Aurora 8b10b IP Core	Communication	
AXI DMA Back-End Core	Interface	
Bitec HDMI 2.0a IP Core	Audio/Video	
CAMFE: Camera Front-End Processor Core	Audio/Video	
CAN-CTRL: CAN 2.0 & CAN FD Bus Controller	Communication	
Color Space Conversion	Audio/Video	
CompactFlash Controller	Memory	
CSI-2 (MIPI) Controller Core V2	Interface	
D2692 - Dual UART	Communication	
D6840 - Programmable Timer Module	Processor	
D8254 - Programmable Interval Timer	Processor	
D8255 - Programmable Peripheral Interface	Processor	
	D8259 - Programmable Interrupt Controller	Processor
	DBLCD32 - LCD/TFT Display Controller	Audio/Video
	DF6811E 8-bit Fast Microcontroller	Processor
	DFPIC1655X - RISC Microcontroller	Processor
	DFPMU - Floating Point Coprocessor	Processor
	DI2CM I2C Bus Interface-Master	Interface
	DI2CS - I2C Bus Interface - Slave	Interface
	DisplayPort Receiver IP Core	Audio/Video
	DMA Core for PCIe Hard IP	Interface
	DMAC-RMII - 10/100 Mb	Communication
	DP8051XP Pipelined 8-Bit Microcontroller	Processor
	DSI-2 (MIPI) Controller Core	Audio/Video
	DSMART - ISO 7816 based smart card reader	Interface
	DSPI - Serial Peripheral Interface Master/Slave	Interface
	Embedded USB 3.0/3.1 Gen 1 Host Controller	Communication
	Embedded USB 3.1 Gen 2 Device Controller	Communication
	Enhanced ClearNAND Controller	Memory
	EtherCAT MASTER IP	Communication
	Ethernet MAC 10/100	Communication
	EXP-E5200 - Security Processor	Security
	EXP-F5200 - Suite B Crypto Microprocessor	Security
	Gen4 PCI Express EndPont Controller	Interface
	Gen4 PCI Express Root Complex Controller	Interface
	GiGE / Triple-speed Ethernet MAC	Communication
	Graphics Accelerator for Android	Audio/Video
	H.264/AVC 4k Decoder IP Core	Audio/Video
	H.264/AVC 4k Encoder IP Core	Audio/Video
	H.264/AVC 8k Encoder IP Core	Audio/Video
	H16550S: Synchronous 16550 UART with FIFO	Audio/Video
	H265-MP-D: HEVC/H.265 Main Profile Decoder	Audio/Video

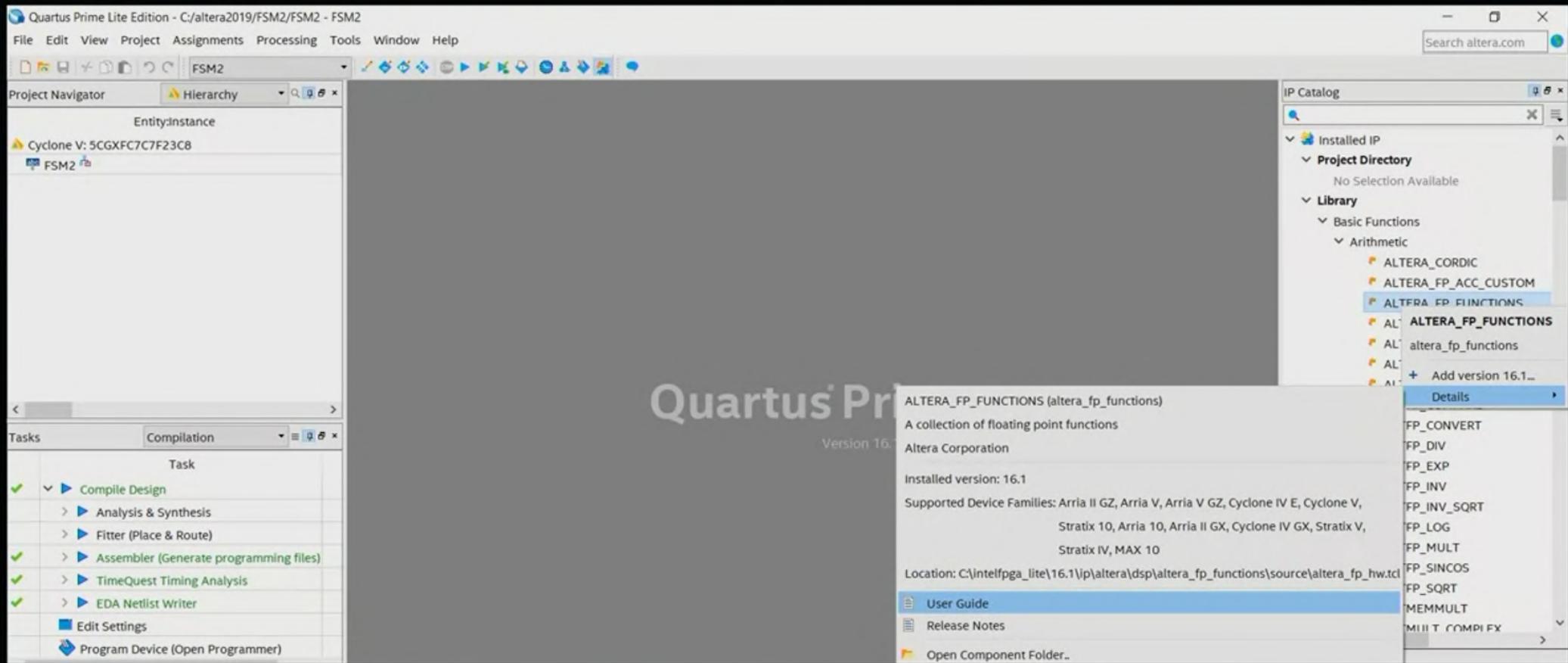


Intel Altera 3rd party IP Cores

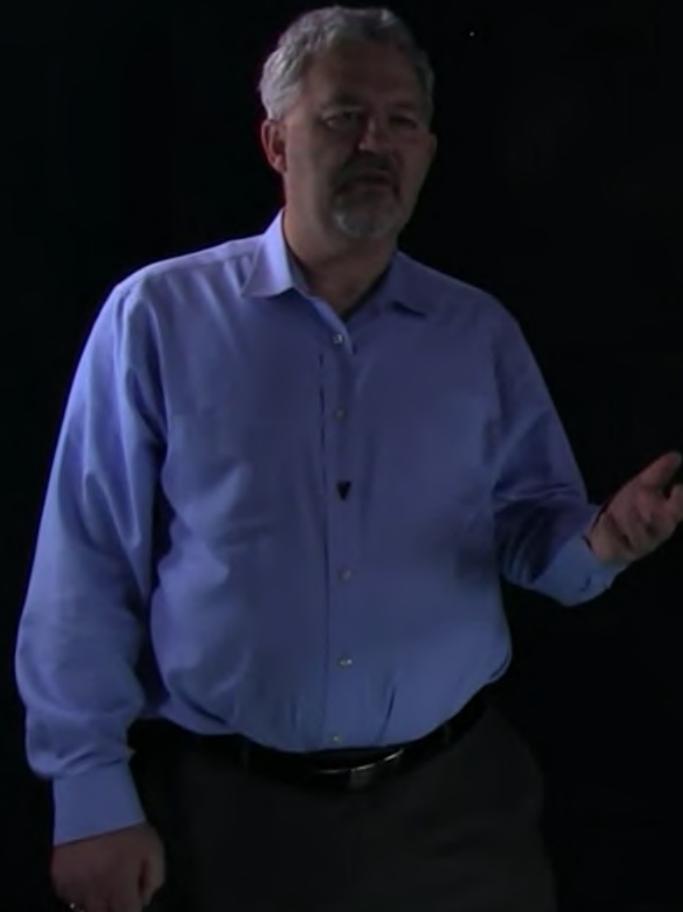
HSDLC: HDLC & SDLC Protocol Controller Core	Communication	
HyperRAM controller	Memory	
I2S Controller	Interface	
IEEE1588 Protocol Stack Package	Communication	
IntelliProp SAS Initiator IP Core	Interface	
IntelliProp SATA AHCI Host Core	Interface	
IntelliProp SATA RAID IP Core(IPC-BL109A-RD)	Interface	
Interlaken from 1Gbps to 1,000Gbps	Communication	
ION 64b/66b High Speed Serial Interface IP	Communication	
IP SD / SDIO / MMC Slave Controller (EP560)	Memory	
IPLock IPcore Protection System	Security	
JPEG streamin Decoder	Audio/Video	
JPEG2000 Decoder (HD/4K/8K)	Audio/Video	
JPEG2000 Encoder (HD/4K/8K)	Audio/Video	
JPEG-EX-F: 4K/8K, Baseline/Extended Encoder	Audio/Video	
JPEG-LS-D: Lossless & Near-Lossless Decoder	Audio/Video	
L8051XC1: 8051-Compatible Microcontroller	Processor	
Lancero - Scatter-Gather DMA Engine PCIe	Interface	
LIN Bus Master/Slave Controller Core	Communication	
MD5: MD5 Processor Core	Processor	
MECHATROLINK-III Master/Slave IP	Interface	
Mentor Graphics AXI3 Inline Monitor BFM	Interface	
Mentor Graphics AXI4STREAM Master BFM	Interface	
Mentor Graphics AXI4STREAM Slave BFM	Interface	
MIPI CSI2 Receive Core	Audio/Video	
MIPI-CSI2 Transmit Core	Audio/Video	
MPEG-2 Decoder IP Core	Audio/Video	
MPEG-2 Encoder IP Core	Audio/Video	
NAND Flash Controller (EP501)	Memory	
Nios II Advanced CAN	Processor	
	NVMe IP core	Memory
	ONFI Controller	Memory
	PCI-M32: 32-bit, 33 MHz PCI Master/Target Interface	Interface
	PCI-M64: 64-bit, 66 MHz PCI Master/Target Interface	Interface
	Pipeline SDRAM Controller	Memory
	PSRAM Memory Controller	Memory
	QDR Infiniband Target Channel Adapter	Memory
	Quad SPI serial FLASH Memory Controller	Memory
	SCR: Smart Card Reader Controller	Interface
	SD / SDIO / MMC Host Controller	Memory
	SD 3.0/eMMC 4.5 Host Controller (EP553)	Memory
	SD/ SDIO/ SDXC 3.0 Host Controller	Memory
	SHA-256: 256-bit SHA Cryptoprocessor Core	Security
	SHA2-A300 Secure Hash Algorithm IP Core	Security
	Streaming Multi-port SDRAM Memory Controller	Memory
	TICO Lightweight Decoder (HD/4K/8K)	Audio/Video
	TICO Lightweight Encoder (HD/4K/8K)	Audio/Video
	True Random Number Generator (TRNG)	Security
	UDP/IP Hardware Protocol Stack Core	Communication
	UDPIP-40G: 40G UDP/IP Hardware Protocol Stack	Communication
	Ultra-Low Latency 25Gb/s Ethernet IP Solution	Communication
	USB 1.1 Device, RAM Interface (USB11SR)	Communication
	USB 3.0/3.1 Gen 1 Device, FIFO Interface	Communication
	USB3.0 Host IP core	Communication



Intel Altera IP Core Use



3rd Party IP Core Use - VHDL

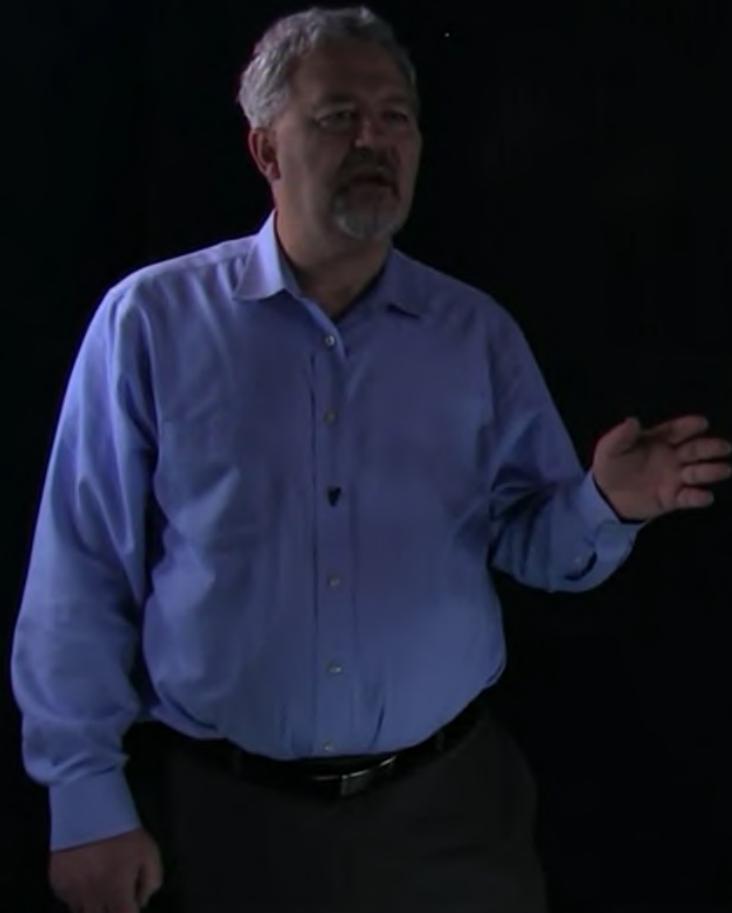


```
-- This file shows an example of using the FPGACore package in VHDL
-- This saves time since core component declarations are made in the package
-- As an alternative to a Package, you can also cut & paste just these
-- component definitions in a new design and use the components as needed.
-- NOTE: The core function's *.vhd files must be in the project
-- directory or search path.

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.all;
USE IEEE.NUMERIC_STD.all;
USE IEEE.STD_LOGIC_UNSIGNED.all;
PACKAGE FPGACore IS
    COMPONENT debounce
        PORT(pb, clock_100Hz      : IN  STD_LOGIC;
              pb_debounced    : OUT STD_LOGIC);
    END COMPONENT;
    COMPONENT dec_7seg
        PORT(hex_digit      : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
              segment_a, segment_b, segment_c, segment_d,
              segment_e, segment_f, segment_g : OUT STD_LOGIC);
    END COMPONENT;
END FPGACore;
```



3rd Party IP Core Use - VHDL



```
-- Example showing use of FPGACore
-- modify Lines below for your design
-- Do not just add this code to a new design
-- Note the use of Port Maps using Components above
LIBRARY work;
USE work.FPGACore.ALL;
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.NUMERIC_STD.all;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

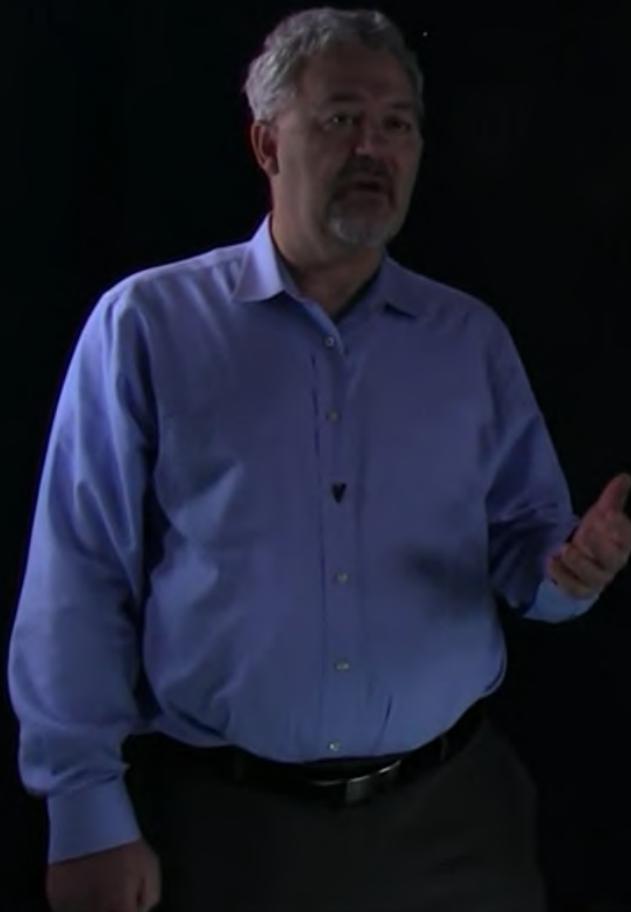
ENTITY FPGApack IS
    PORT (clock_100Hz, pb1 : IN STD_LOGIC;
          pb1_debounced : OUT STD_LOGIC);
END FPGApack;

ARCHITECTURE a OF FPGApack IS
SIGNAL clock_100Hz : STD_LOGIC;
BEGIN
    debounce1 : debounce PORT MAP (pb => pb1,
                                     clock_100Hz => clock_100Hz,
                                     pb_debounced => pb1_debounced);

END a;
```



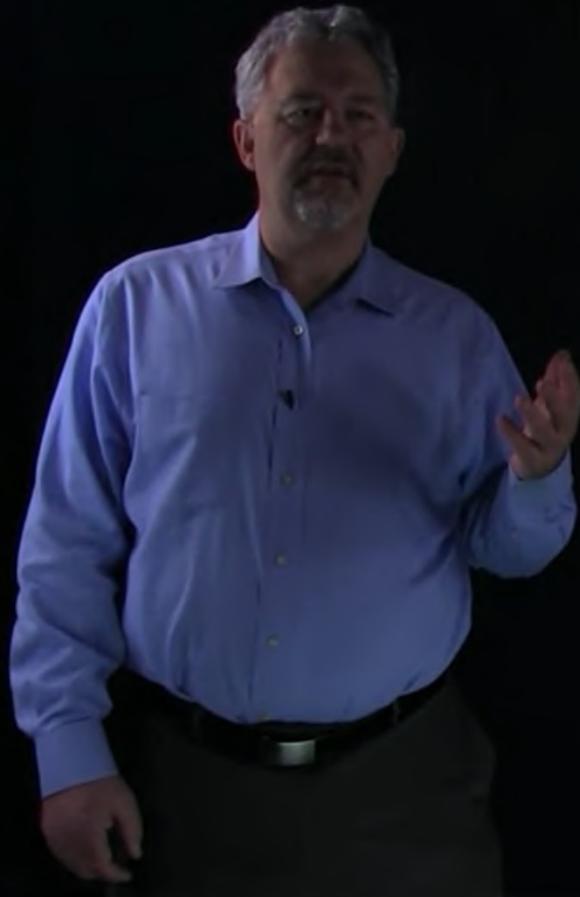
Summary



In this video, you have learned:

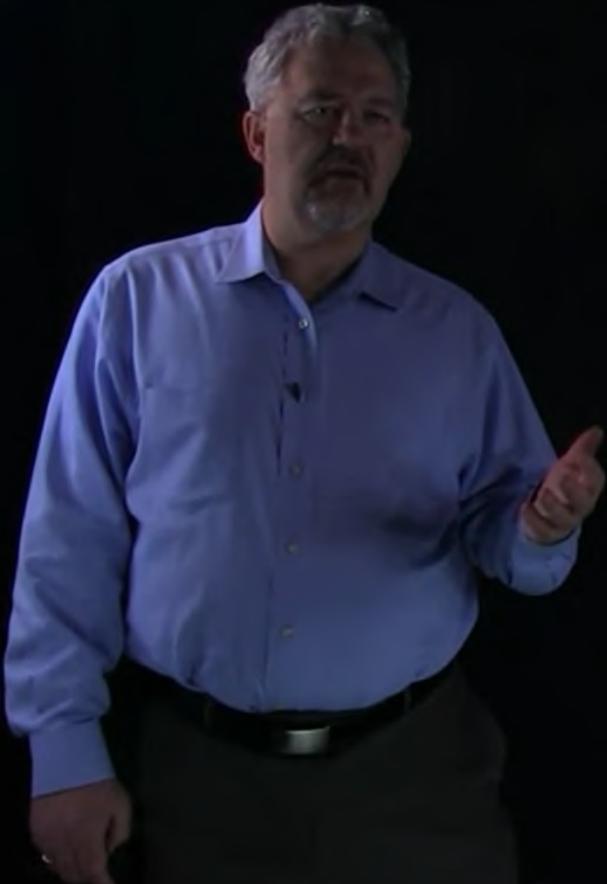
- What is available from Altera as IP Cores, including Processors, DSP, Communications, Interface, Memory, Audio/Video, Controls and Security
- How to integrate the IP in a Altera Design
- How to find 3rd party IP for Altera FPGA Devices

Xilinx IP Cores



In this video, you will learn:

- What is available from Xilinx as IP Cores, including Processors, DSP, Communications, Interface, Memory, Audio/Video, Controls and Security
- How to integrate the IP in an Xilinx Design
- How to find 3rd party IP for Xilinx FPGA Devices



Xilinx IP Cores

- IP Included In Vivado

Vivado IP Integrator provides a graphical and Tcl-based, correct-by-construction design development flow. It provides a device and platform aware, interactive environment that supports intelligent auto-connection of key IP interfaces, one-click IP subsystem generation, real-time DRCs, and interface change propagation, combined with a powerful debug capability.

- Leveraging IP to save cost

By leveraging the combination of Vivado IPI and HLS customers are saving up to 15X in development costs versus an RTL approach.

- Tested

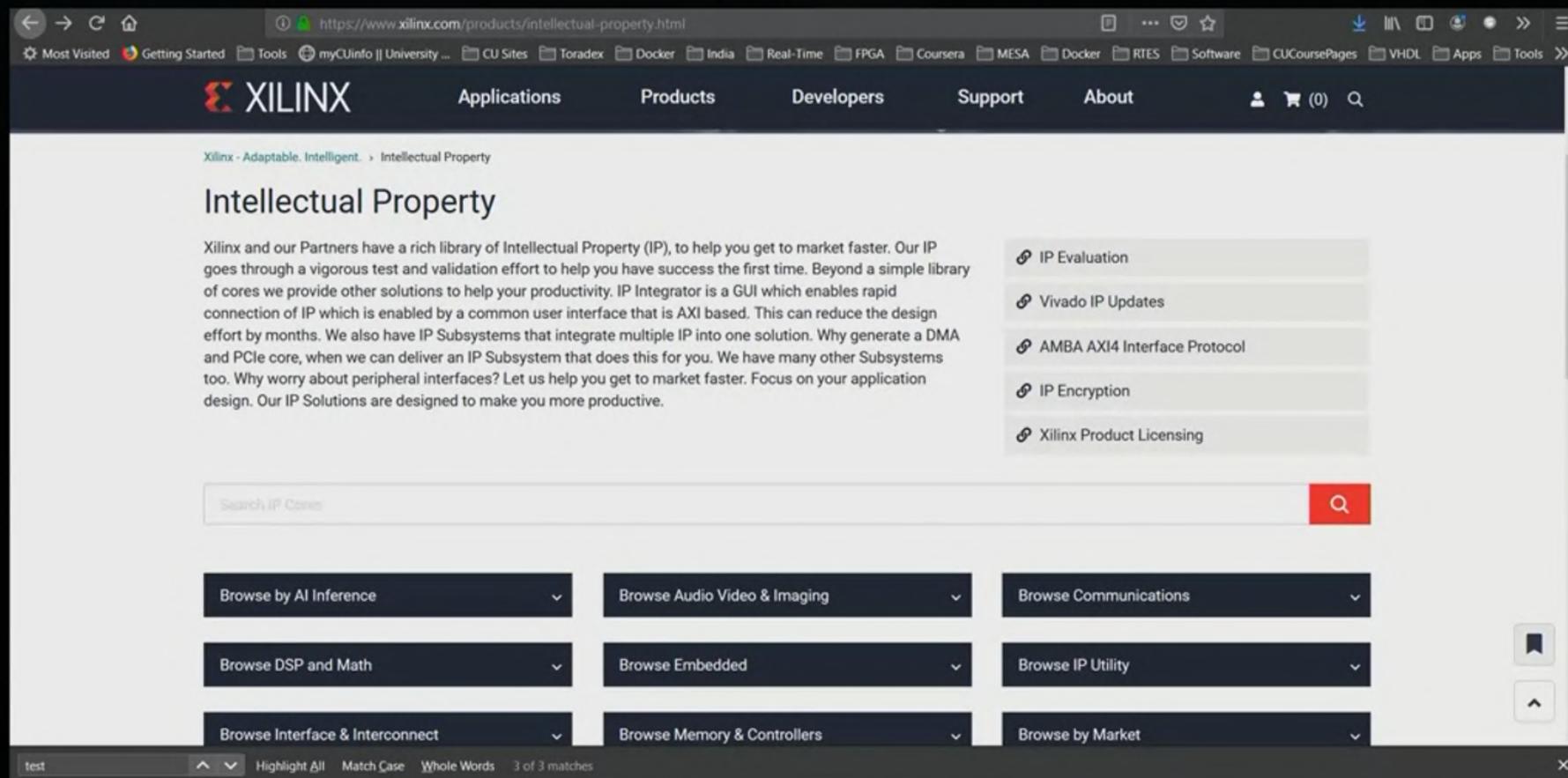
Xilinx IP goes through a vigorous test and validation effort to help you have success the first time.

Xilinx IP Cores

MicroBlaze		AXI USB 2.0 Device Controller		Communications	LDPC Encoder / Decoder	DSP	Communications
ze	Embedded	XAU/DXAUI		Interface	Multiplier Accumulator	DSP	Hard-core Tri-mode Ethernet MAC
n	Embedded	QSGMII		Interface	Polar Encoder / Decoder	DSP	ions
e to AXI Bridge	Interface	CPRI		Communications	AXI External Memory Controller	Memory	Audio I2S
General Purpose IO	Interface	JESD204		Interface	AXI System Cache	Memory	Audio/Video
Central DMA Controller	Interface	Serial RapidIO LogiCORE IP		Interface	AXI Video DMA (AXI VDMA)	Audio/Video	Audio Clock Recovery Unit
Streaming FIFO	Interface	Zynq UltraScale+ RFSoC RF Data Converter		Communications	Block Memory Generator	Memory	AXI4-Stream to Video Out
APB Bridge	Interface	3GPP LTE Channel Estimator	DSP	Core	DDR4 Controller	Memory	Chroma Resampler
Video DMA (AXI VDMA)	Interface	3GPP LTE Fast Fourier Transform (LTE-FFT)	DSP	Core	DDR3 Controller	Memory	Color Correction Matrix
DC Core	Interface	Accumulator	DSP	Core	Error Correction Checking (ECC)	Memory	DisplayPort Subsystem
AXI4-Stream Interconnect	Interface	Adder/Subtractor	DSP	Core	FIFO Generator	Memory	Gamma Correction
JTAG to AXI Master	Interface	Binary Counter	DSP	Core	LPDDR3 Controller	Memory	H.264/H.265 Video Codec Unit
600G Interlaken Core	Interface	Cascaded Integrator Comb (CIC) Compiler	DSP	Core	Memory Interface	Memory	HDMI
Aurora 64B/66B	Interface	Complex Multiplier	DSP	Core	QDRIV SRAM Core	Memory	MIPI CSI Controller Subsystems
SPI-4 Phase 2 Interface Solutions	Interface	Convolutional Encoder	DSP	Core	RLD3 Controller	Memory	RGB to YCrCb Color-Space
QDMA Subsystem for PCI Express	Interface	CORDIC	DSP	Core	10 Gigabit Ethernet Media Access	Controller	Converter
XPS UART Lite	Communications	DDS Compiler	DSP	Core	Controller	Communications	SDI
AXI Quad SPI	Interface	Discrete Fourier Transform (DFT)	DSP	Core	10 Gigabit Ethernet PCS/PMA	Communications	SPDIF
AXI UART Lite	Communications	Divider	DSP	Core	(10GBASE-R)	Communications	Test Pattern Generator
AXI UART16550	Communications	Fast Fourier Transform (FFT)	DSP	Core	100M/1G TSN Subsystem	Communications	UHD Serial Digital Interface (UHD-SDI)
IBERT for 7 Series GTZ Transceivers	Interface	FIR Compiler	DSP	Core	10G Ethernet with 1588 Subsystem	Communications	Audio/Video
LogiCORE IP Serial RapidIO Gen 2	Interface	Floating-Point Operator	DSP	Core	32G Fibre Channel (32GFC) Reed-Solomon FEC	Communications	ChipScope AXI Monitor
NVMe Host Accelerator (NVMeHA)	Memory	Interleaver / De-interleaver	DSP	Core	3GPP LTE Turbo Encoder	Communications	ChipScope Integrated Controller (ICON)
					40G/100G Ethernet Core	Communications	ChipScope Integrated Logic Analyzer (ILA)
					DUC/DDC Compiler	Communications	Utility
						Fixed Interval Timer (FIT)	Utility



Xilinx 3rd party IP Cores



The screenshot shows the Xilinx website's Intellectual Property page. The header includes the Xilinx logo, navigation links for Applications, Products, Developers, Support, and About, and a search bar. The main content area is titled "Intellectual Property" and discusses Xilinx's IP solutions. To the right, there is a sidebar with links to IP Evaluation, Vivado IP Updates, AMBA AXI4 Interface Protocol, IP Encryption, and Xilinx Product Licensing. Below the main content are several dropdown menus for browsing IP cores by category: AI Inference, Audio Video & Imaging, Communications, DSP and Math, Embedded, IP Utility, Interface & Interconnect, Memory & Controllers, and Market. A search bar is located at the top of the page, and a "test" watermark is visible at the bottom.

Intellectual Property

Xilinx and our Partners have a rich library of Intellectual Property (IP), to help you get to market faster. Our IP goes through a vigorous test and validation effort to help you have success the first time. Beyond a simple library of cores we provide other solutions to help your productivity. IP Integrator is a GUI which enables rapid connection of IP which is enabled by a common user interface that is AXI based. This can reduce the design effort by months. We also have IP Subsystems that integrate multiple IP into one solution. Why generate a DMA and PCIe core, when we can deliver an IP Subsystem that does this for you. We have many other Subsystems too. Why worry about peripheral interfaces? Let us help you get to market faster. Focus on your application design. Our IP Solutions are designed to make you more productive.

IP Evaluation

Vivado IP Updates

AMBA AXI4 Interface Protocol

IP Encryption

Xilinx Product Licensing

Search IP Cores

Browse by AI Inference

Browse Audio Video & Imaging

Browse Communications

Browse DSP and Math

Browse Embedded

Browse IP Utility

Browse Interface & Interconnect

Browse Memory & Controllers

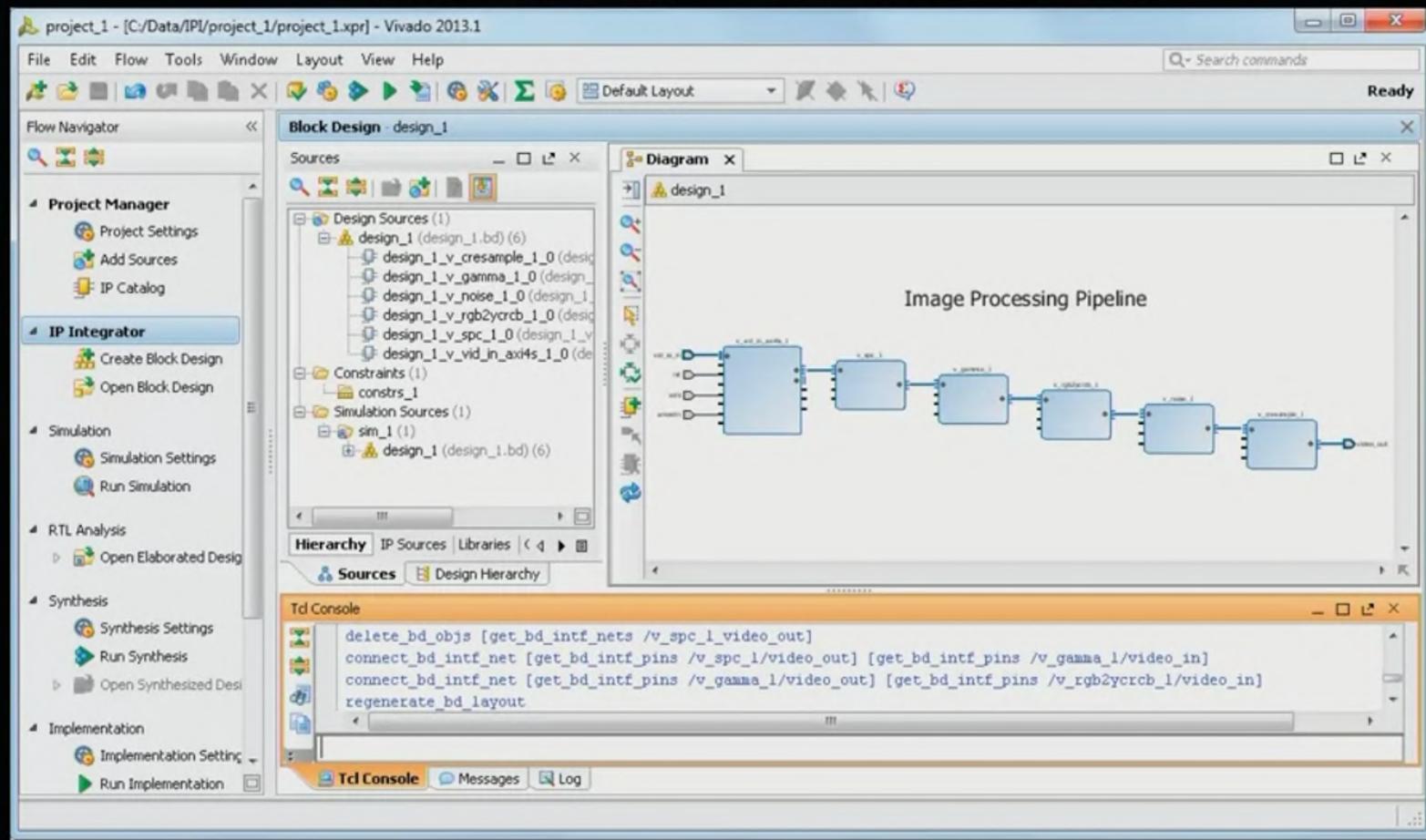
Browse by Market

test

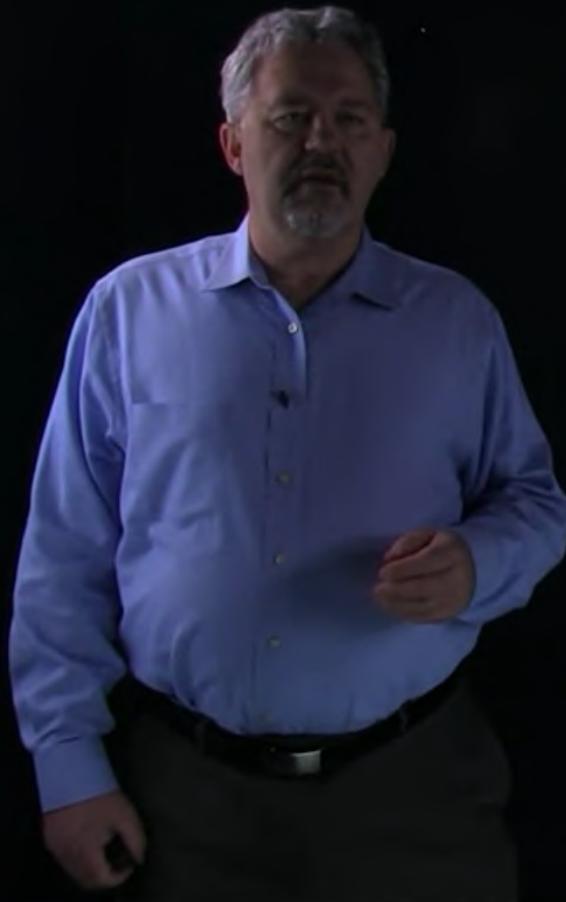
Highlight All Match Case Whole Words 3 of 3 matches



Xilinx IP Core Use



Summary



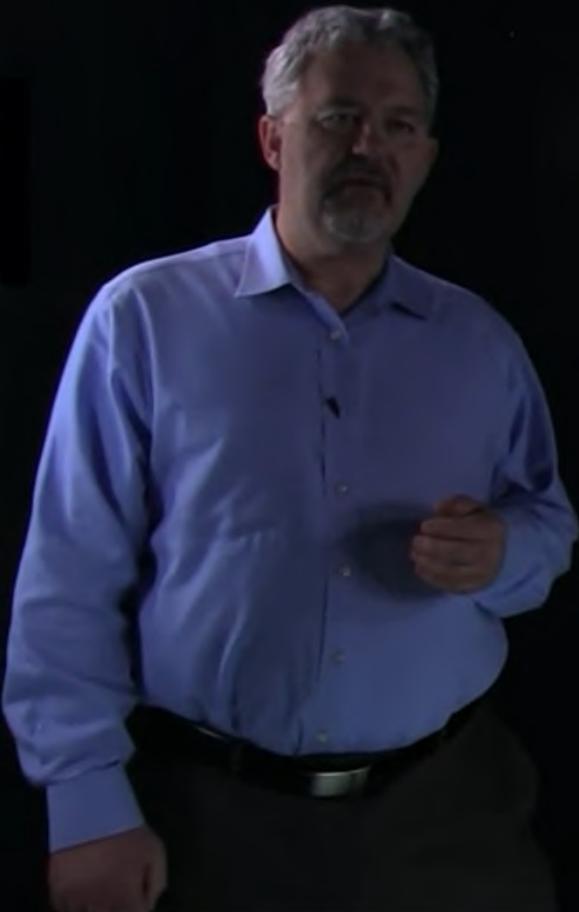
In this video, you have learned:

- What is available from Xilinx as IP Cores, including Processors, DSP, Communications, Interface, Memory, Audio/Video, Controls and Security
- How to integrate the IP in a Xilinx Design
- How to find 3rd party IP for Xilinx FPGA Devices

References

- [1] Xilinx Staff. (2019/Nov/30), *Intellectual Property* [Online]. Available: <https://www.xilinx.com/products/intellectual-property.html>
- [2] Xilinx Staff. (2019/Nov/30), *Vivado IP Integrator Backgrounder* [Online]. Available: https://www.xilinx.com/publications/prod_mktg/vivado/Vivado_IP_Integrator_Bac_kgrounder.pdf

Lattice IP Cores

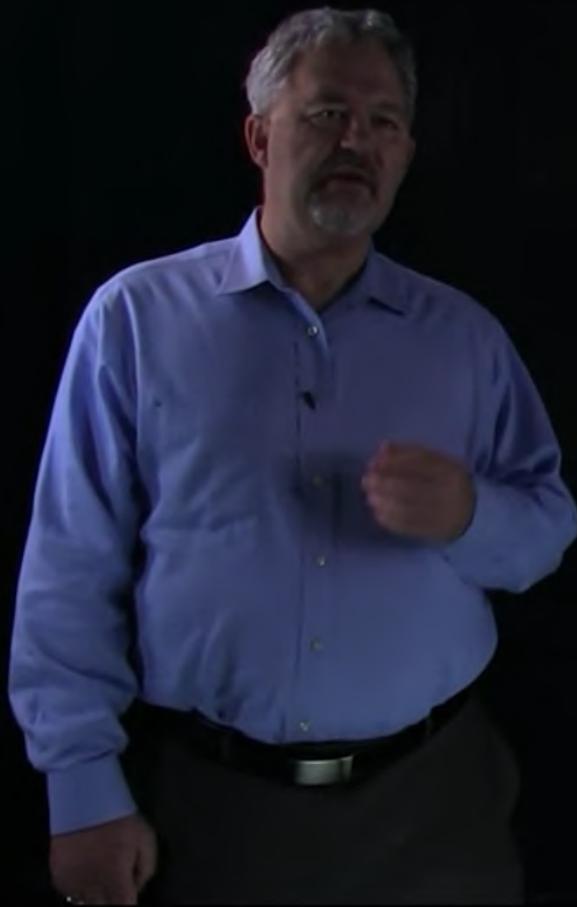


In this video, you will learn:

- What is available from Lattice as IP Cores, including Processors, DSP, Communications, Interface, Memory, Audio/Video, Controls and Security
- How to integrate the IP in an Lattice Design
- How to find 3rd party IP for Lattice FPGA Devices



Lattice IP Cores

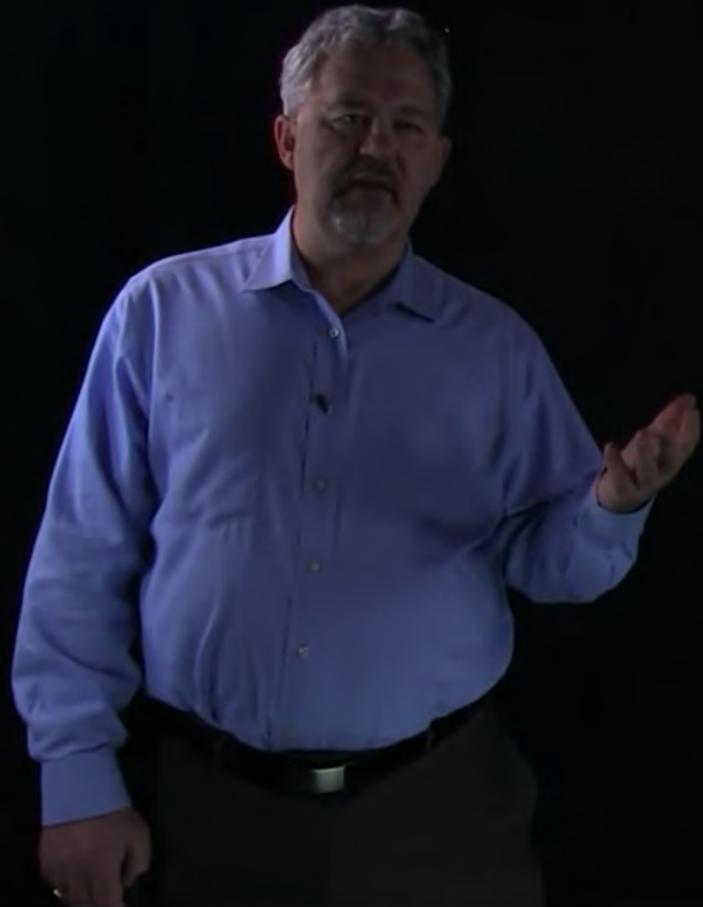


IP Included In Diamond

- **Diamond IPexpress** is an easy way to use a collection of functional blocks from Lattice Semiconductor. There are two types of functional blocks available through IPexpress: modules and IP. IPexpress enables you to extensively customize these blocks.
- **Modules**: These basic, configurable blocks come with IPexpress. They provide a variety of functions including I/O, arithmetic, memory, and more.
- **IP**: Intellectual property (IP) are more complex, configurable blocks. They are accessible through IPexpress, but they do not come with the tool. They must first be downloaded and installed as a separate step before they can be accessed from IPexpress. To see all that's available and to learn about licensing and other vendors of IP, go to the Lattice Web site: www.latticesemi.com/ip.



Lattice IP Cores



IP Core Integration

- **Instantiation:** IPexpress modules and IP are instantiated the same way other modules are in your HDL. When you generate modules and IP in IPexpress, the tool also produces a Verilog or VHDL file with the necessary instantiation commands. You can copy and paste the contents of this file into one of your source files.
- **Device Specific:** Before you instantiate any IPexpress module, check that it is compatible with your design project's device. When they were created, the modules were optimized for a specific device and may depend on that device's architecture.

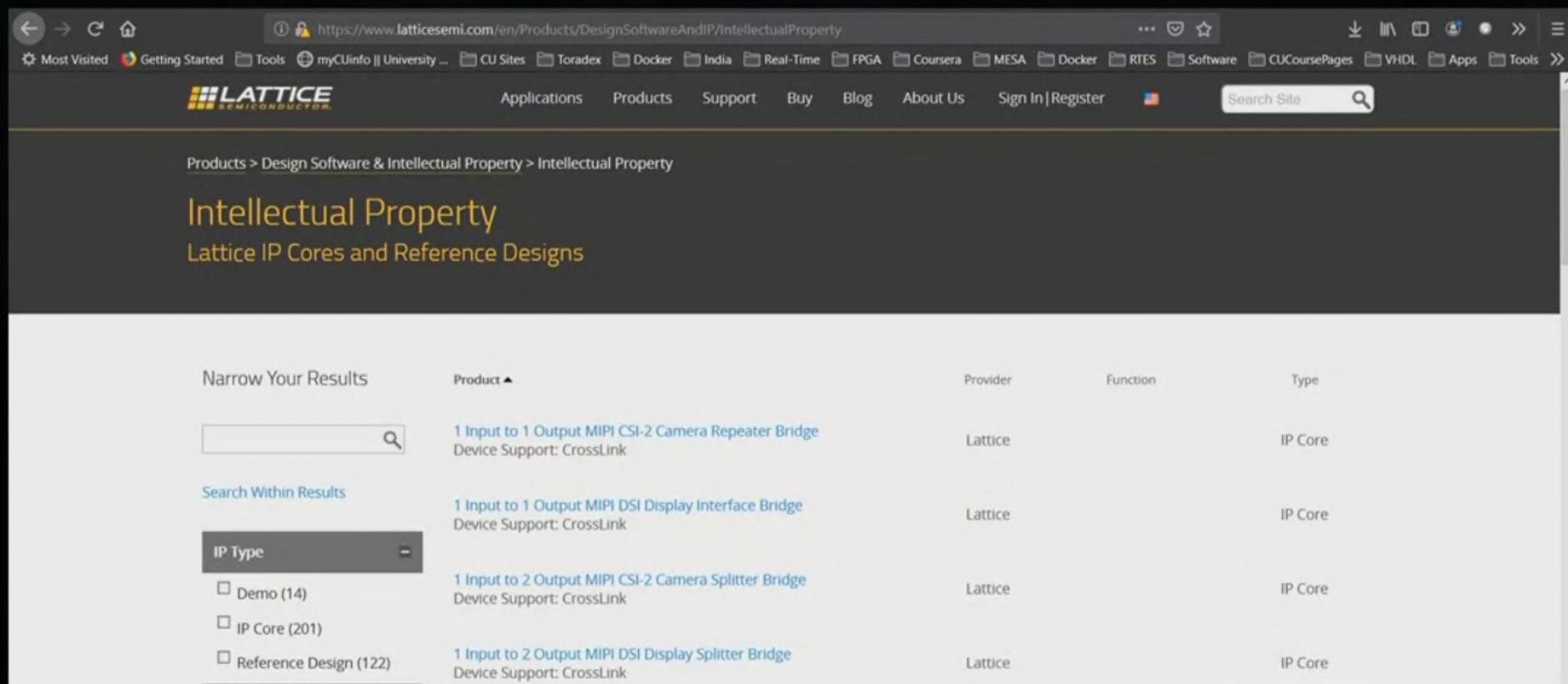


Lattice IP Cores

			LPDDR3 SDRAM				
MICO32	Embedded		Controller	Memory			
MICO8	Embedded		SG-DMA	Memory			
DDR Generic	Memory		10G Ethernet MAC	Communications	PCS PIPE IP		
MIPI_DPHY	Audio/Video	RAM_DP	Memory	10Gb+ Ethernet MAC	Communications	SRIO	Interface
SDR	Memory	ROM	Memory	2.5G Ethernet MAC	Communications	Tri-Rate SDI PHY	Interface
I2C	Interface	FIFO	Memory	2.5G Ethernet PCS	Communications	4:1 CSI-2 to CSI-2	Audio/Video
DLL	Utility	2D Edge Detector	DSP	CPRI 5G	Communications	CMOS to D-PHY	Audio/Video
PLL	Utility	2D FIR Filter	DSP	CPRI	Communications	CSI-2 to CSI-2	Audio/Video
PMU	Utility	2D Scaler	DSP	SGMII Gb Ethernet PCS	Communications	CSI-2/DSI D-PHY	Audio/Video
Power Controller	Utility	Block Convolutional Encoder	DSP	SPI4	Communications	Receiver	Audio/Video
Adder	DSP	Block Viterbi Decoder	DSP	Tri-Speed Ethernet		CSI-2/DSI D-PHY	
Adder_Subtractor	DSP	CIC Filter	DSP	MAC	Communications	Transmitter	Audio/Video
Comparator	DSP	CORDIC	DSP	XAUI	Communications	D-PHY to CMOS	Audio/Video
Complex Multiplier	DSP	Color Space Converter	DSP	DVB-ASI	Interface	DSI to DSI	Audio/Video
Counter	Utility	FFT Compiler	DSP	JESD204A	Interface	FPD-LINK Receiver	Audio/Video
FFT_Butterfly	DSP	FIR Filter	DSP	JESD204B 5G	Interface	FPD-LINK Transmitter	Audio/Video
LFSR	DSP	Gamma Corrector	DSP	JESD204B	Interface	FPD-LINK to DSI	Audio/Video
Mult_Add_Sub_Sum	DSP	Interleaver Deinterleaver	DSP	JSED207	Interface	Pixel to Byte Converter	Audio/Video
Multiplier	DSP	Numerically Controller	DSP	PCI Express 5G		SubLVDS Image Sensor	
Multiply_accumulate	DSP	Oscillator	DSP	Endpoint	Interface	Receiver	Audio/Video
Sin-Cos-Table	DSP	Video Frame Buffer	DSP	PCI Express Endpoint	Interface	SubLVDS to CSI-2	Audio/Video
Barrel_Shifter	DSP	DDR SDRAM Controller	Memory	PCI Master/Target 33	Interface		
MAC	DSP	DDR2 SDRAM Controller	Memory	PCI Master/Target 66	Interface		
Distributed_DPRAM	Memory	DDR3 SDRAM Controller	Memory	PCI TARGET 66	Interface		
Distributed_ROM	Memory	DDR3 SDRAM PHY	Memory	PCI TARGET 33	Interface		
		LPDDR SDRAM Controller	Memory				
		LPDDR2 SDRAM Controller	Memory				



Finding Lattice IP Cores



The screenshot shows a web browser displaying the Lattice Semiconductor website. The URL in the address bar is <https://www.latticesemi.com/en/Products/DesignSoftwareAndIP/IntellectualProperty>. The page title is "Intellectual Property". The main content area displays a table of Lattice IP cores, with the first four rows shown:

Narrow Your Results	Product ▲	Provider	Function	Type
<input type="text"/> 	1 Input to 1 Output MIPI CSI-2 Camera Repeater Bridge Device Support: CrossLink	Lattice		IP Core
Search Within Results	1 Input to 1 Output MIPI DSI Display Interface Bridge Device Support: CrossLink	Lattice		IP Core
IP Type ▾	1 Input to 2 Output MIPI CSI-2 Camera Splitter Bridge Device Support: CrossLink	Lattice		IP Core

On the left side, there is a sidebar with a "Search Within Results" section and a "IP Type" dropdown menu. The "IP Type" menu contains the following options:

- Demo (14)
- IP Core (201)
- Reference Design (122)



Lattice 3rd party IP Cores

AES-CCM Core	Security	EP501: NAND Flash Controller	Embedded
AES-GCM Core	Security	EP510: CompactFlash/PCMCIA Host Adapter	Embedded
CANmodule-III	Communications	EP550: SD / SDIO / MMC Host Controller	Connectivity
CLP-02 DES/3DES	Security	EP560: SD / SDIO / MMC Slave Controller	Connectivity
CLP-11 Tiny AES	Security	Fast AES Core	Security
CLP-17 Elliptic Curve Point Multiplier Core	Security	Fast Hash Core	Security
D16450: Configurable UART	Communications	Floating Point To Integer Pipelined Converter	DSP
D8259: Programmable Interrupt Controller	Embedded	High Performance 8-bit RISC Microcontroller	Embedded
DF6805: 8-bit FAST Microcontrollers Family	Embedded	High Performance Configurable 8-bit RISC MCU	Embedded
DF6808: 8-bit FAST Microcontrollers Family	Embedded	High Performance DES and Triple-DES Cores	Security
DF6811: 8-bit FAST Microcontrollers Family	Embedded	IEEE 1588 Syn1588®Clock_M Core	Communications
DFPADD: Floating Point Pipelined Adder Unit	DSP	IEEE 1588 Syn1588®Clock_S Core	Communications
DFPAU: Floating Point Arithmetic Unit	DSP	iniCAN	Connectivity
DFPCOMP: Floating Point Comparator Unit	DSP	Integer to Floating Point Pipelined Convert	DSP
DFPDIV: Floating Point Pipelined Divider Unit	DSP	LZRW3 Data Compression Core	Communications, DSP
DFPMU: Floating Point Mathematics Unit	DSP	Modular Exponentiation Core	Communications, DSP
DFPMUL: Floating Point Pipelined Multiplier Unit	DSP	Payload Compression System	Communications, DSP
DFPSQRT: Floating Point Pipelined Square Root Unit	DSP	Serial Peripheral Interface - Master/Slave with FIFO	Connectivity
DI2CM: I2C Bus Interface - Master	Connectivity	Standard AES Core	Security
DI2CS: I2C Bus Interface - Slave	Connectivity	syn1588® Versatile IP Dual HP	Communications
DP8051: Pipelined High Performance 8-bit MCU	Embedded	syn1588®Versatile IP	Communications
DP8051XP: Pipelined High Performance 8-bit MCU	Embedded	TC1000-WiMAX: 802.16 d/e CTC	Communications
DSPI: Serial Peripheral Interface - Master/Slave	Connectivity	TC1700: Turbo decoder Core for HSPA+, LTE & WiMAX	Communications
DSPIIS: Serial Peripheral Interface - Slave	Connectivity	TC4400: ITU-Ghn LDPC Encoder/Decoder Cores	Communications
EP100: PowerPC Bus Slave	Connectivity	TC7000-LTE: 3GPP-Long Term Evolution CTC Decoder	Communications
EP201: PowerPC Bus Master	Connectivity	Tiny AES Core	Security
EP300: PowerPC Bus Arbiter	Connectivity	Tiny Hash Core	Security



Lattice IP Core Use

Lattice Diamond - IPExpress

File List

XO2_Pico

- LCMXO2-1200ZE-1MG132C
- Strategies
 - Area
 - I/O Assistant
 - Quick
 - Timing
 - Strategy1
- XO2_Pico
 - Input Files
 - ./Source/PicoLCDDriver/lcd4digit.v
 - ./Source/PicoLCDDriver/LCDCharMapLUTs.ipx
 - ./Source/PicoLCDDriver/LCDEncoding4to1.v
 - ./Source/PicoLCDDriver/PicoLCDdrive.v
 - ./Source/PicoLCDDriver/pwm.v
 - ./Source/PicoLCDDriver/lcdencoding4to1com.v
 - ./mico8/soc/mico8.v
 - ./Source/wb2lcd.v
 - ./Source/XO2_top.v
 - ./IPCore/myEFB/myEFB.ipx
 - Synthesis Constraint Files
 - LPF Constraint Files
 - XO2_Pico/XO2_Pico.lpf
 - Debug Files
 - Script Files
 - Analysis Files
 - Programming Files
 - XO2_Pico/XO2_Pico.xcf

Start Page Reports IPExpress

Name Version

- Arithmetic_Modules
 - Adder 3.5
 - Adder_Subtractor 3.5
 - Comparator 3.6
 - Complex_Multiplier 1.8
 - Convert 1.3
 - Counter 4.6
 - FFT_Butterfly 1.5
 - LFSR 3.7
 - Mult_Add_Sub 2.8
 - Mult_Add_Sub_Sum 2.7
 - Multiplier 4.9
 - Multiply_Accumulate 2.8
 - Sin-Cos_Table 1.6
 - Subtractor 3.5
- DSP_Modules
 - 1D_FILTER 1.2
 - ADDER_TREE 1.4
 - BARREL_SHIFTER 1.3
 - MAC 4.2
 - MMAC 2.2
 - MULT 4.2
 - MULTADDSUB 4.2
 - MULTADDSUBSUM 4.2
 - SLICE 1.6
 - WIDE_MUX 1.4
- Memory_Modules
 - Distributed_RAM

Module/IP Name

Macro Type: Version:

IP Name:

Project Path:

File Name:

Module Output:

Device Family:

Part Name:

Synthesis: SimplifyPro

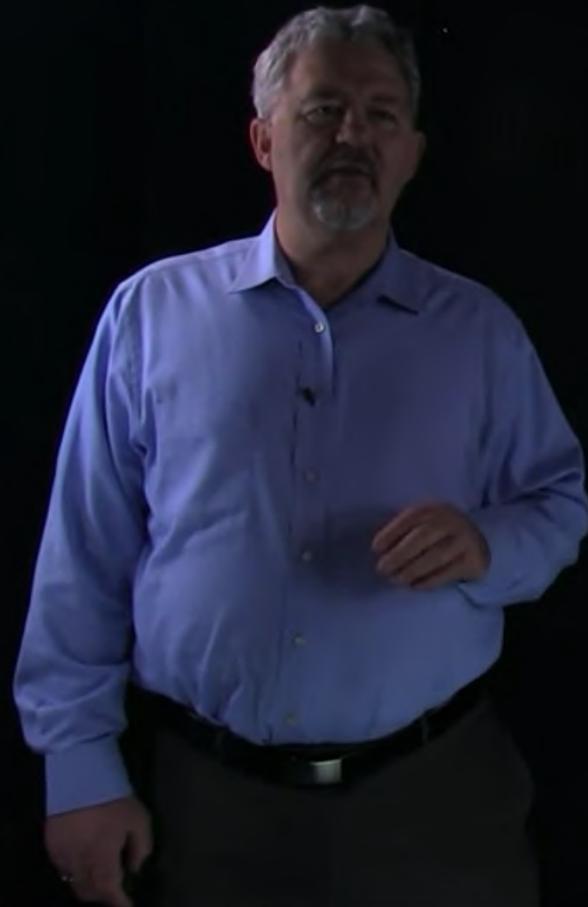
Please enter a project directory!

Customize

File List Process Hierarchy Configuration About



Summary



In this video, you have learned:

- What is available from Lattice as IP Cores, including Processors, DSP, Communications, Interface, Memory, Audio/Video, Controls and Security
- How to find 3rd party IP for Lattice FPGA Devices
- How to integrate the IP in a Lattice Design

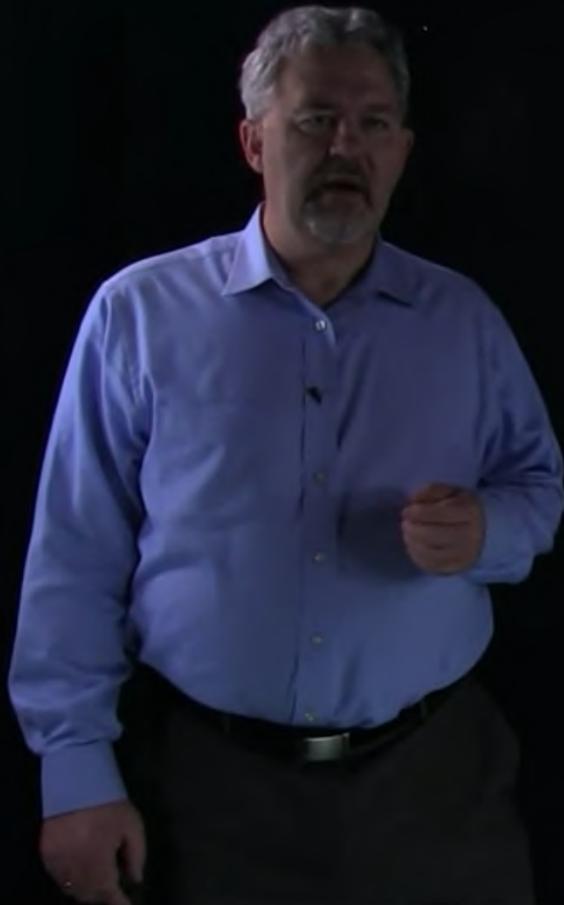


References

- [1] Lattice Staff. (2020/Feb/07), *Lattice IPexpress Quick Start Guide* [Online]. Available:
<https://www.latticesemi.com/Search.aspx?&lcid=9&q=IPexpress&t=-420>
- [2] Lattice Staff. (2020/Feb/07), *Lattice Synthesis Engine for Diamond User Guide* [Online]. Available:
<http://www.latticesemi.com/en/Products/DesignSoftwareAndIP/FPGAandLDS/LatticeDiamond>



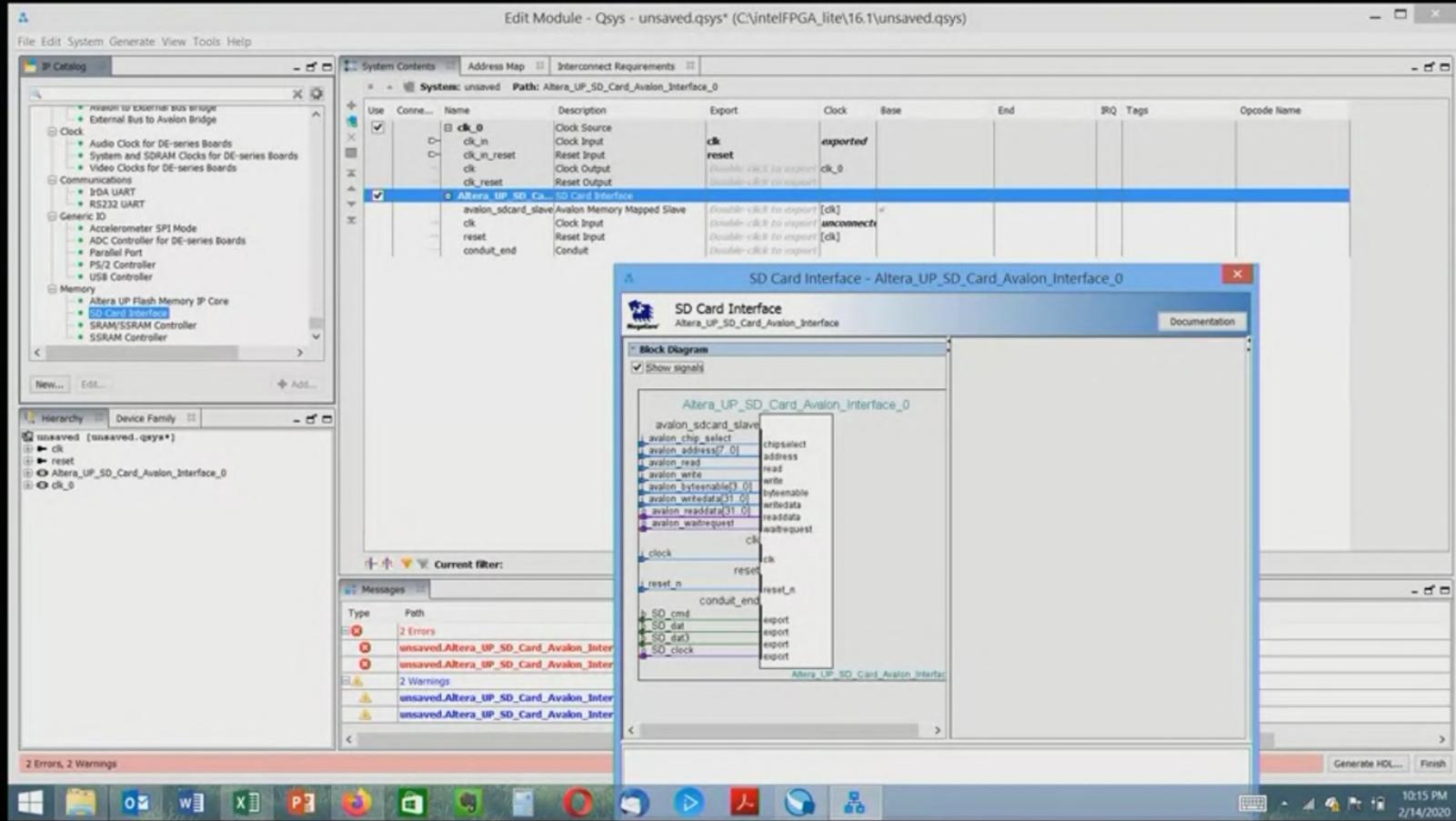
Intel Altera IP Cores for Qsys



In this video, you will learn:

- How to integrate IP from Intel Altera into a Qsys Design, perhaps one of the easiest ways to incorporate IP blocks in your design.
- The remarkable range Altera provides as IP Cores, including soft processors, interfaces to hard processors, DSP, Serial ports, AXI and APB buses, Transceiver interfaces, Memory, Audio/Video, and Control.

Qsys IP Access

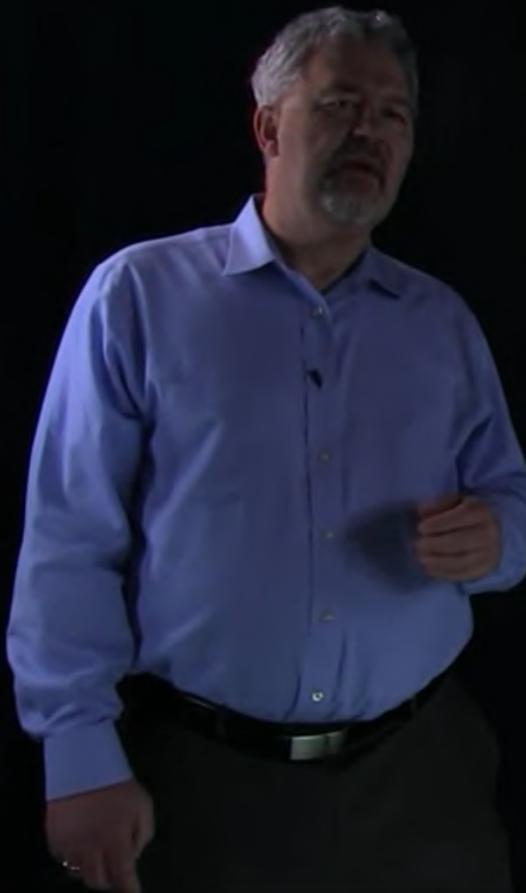


Intel Altera IP Cores available for Qsys

Video Sync Generator	Audio/Video	Altera Avalon LCD	Embedded	Altera Avalon Data Pattern Gen.	Interface	Altera SDRAM Tri-State Controller	Memory
DisplayPort	Audio/Video	PIO	Embedded	PS/2 Controller	Interface	DDR3 SDRAM Cont. with UniPHY	Memory
SDI II	Audio/Video	SPI Slave to Avalon Master Bridge	Embedded	Parallel Port	Interface	LPDDR2 SDRAM Cont. with UniPHY	Memory
2D-FIR II (4k ready)	Audio/Video	Vectorized Interrupt Controller	Embedded	ADC Controller for DE-series	Interface	Altera Avalon Compact FLASH	Memory
Avalon-ST Video Monitor	Audio/Video	Altera Avalon Mutex	Embedded	Accelerometer SPI Mode	Interface	Altera Generic QUAD SPI Controller	Memory
Color Space Convert. II (4k ok)	Audio/Video	Altera Avalon Mailbox	Embedded	Avalon to External Bus Bridge	Interface	Altera Parallel Flash Loader	Memory
Interlacer II (4K passthru)	Audio/Video	Series V Hard Processor Sys.	Embedded	Eternal Bus to Avalon Bridge	Interface	Altera Advanced SEU Detection	Security
Frame Buffer II (4K Ready)	Audio/Video	Altera HPS Trace IP	Embedded	Generic Tri-State Controller	Interface	High-Speed Reed-Solomon	Security
Gamma Corrector II (4K Ready)	Audio/Video	Nios II Processor	Embedded	AHB Slave Agent	Interface	Random Number Generator	Security
Interlacer II (4K Ready)	Audio/Video	Nios II Custom Instr. Master Trans.	Embedded	APB Master Agent	Interface	Turbo CODEC	Security
Mixer II (4K Ready)	Audio/Video	Nios II Custom Instr. Slave Trans.	Embedded	APB Slave Agent	Interface	JTAG to Avalon Master Bridge	Utility
Test Pattern Gen. II (4K Ready)	Audio/Video	Nios II Floating Point Hardware	Embedded	Avalon-MM Master Agent	Interface	Altera Remote Update	Utility
Viterbi	Communications	Nios II Custom Instr. Xconnect	Embedded	Avalon-MM Slave Agent	Interface	Altera PLL	Utility
USB Controller	Communications	Altera Avalon Interrupt Sink	Embedded	AXI Master Agent	Interface	Altera Serial Flash Loader	Utility
IrDA UART	Communications	Altera Avalon Interrupt Source	Embedded	AXI Slave Agent	Interface	Internal Oscillator	Utility
Altera 16550 Compatible UART	Communications	Avalon-MM Clock Crossing Bridge	Interface	Memory Mapped Arbiter	Interface	Scatter-Gather DMA Controller	Utility
Ethernet 1588 Time of Day Clk	Communications	Avalon-MM Pipeline Bridge	Interface	Transceiver PHY Reconfig Cont.	Interface	Altera SignalTap II Logic Analyzer	Utility
Ethernet 1588 TOD Sync	Communications	Avalon-ST Bytes to Packets Conv.	Interface	Altera Avalon I2C Master	Interface	Altera In-Sys. Sources and Probes	Utility
Triple-Speed Ethernet	Communications	Avalon-ST Packets to Bytes Conv.	Interface	Rapid IO II (up to 6.25 Gbaud)	Interface	System ID Peripheral	Utility
Ethernet 10G MAC	Communications	Avalon-ST Channel Adapter	Interface	V-Series Avalon-MM DMA for PCIe	Interface	Trace System	Utility
ALTERA_FP_MATRIX_MULT	DSP	Avalon-ST Data Format Adapter	Interface	JESD204B	Interface	USB Debug Master	Utility
FFT	DSP	Avalon-ST Pipeline Stage	Interface	Altera Serial Flash Controller	Memory	Altera Avalon-MM Master BFM	Utility
AXI Bridge	Embedded	Altera Avalon-MM Monitor	Interface	Avalon-ST Dual Clock FIFO	Memory	Avalon-MM Traffic Gen. and BIST	Utility
AXI Timeout Bridge	Embedded	Altera Avalon-ST Monitor	Interface			Engine	Utility
IRQ Clock Crosser	Embedded	Altera External Memory BFM	Interface			Avalon-ST Test Pattern Generator	Utility
IRQ Fanout	Embedded	Altera Avalon-ST Sink BFM	Interface			Avalon-ST Test Pattern Checker	Utility
Interval Timer	Embedded						



Summary



In this video, you have learned:

- How to integrate IP from Intel Altera into a Qsys Design, perhaps one of the easiest ways to incorporate IP blocks in your design.
- The remarkable range Altera provides as IP Cores, including soft processors, interfaces to hard processors, DSP, Serial ports, AXI and APB buses, Transceiver interfaces, Memory, Audio/Video, and Control.

References

- [1] Intel/Altera Staff. (2019/Nov/29), *Introduction to Intel FPGA IP Cores*. [Online]. Available:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_intro_to_megafuctions.pdf
- [2] Intel/Altera Staff. (2020/Feb/17), *Nios II Gen2 Hardware Development Tutorial*. [Online]. Available:
<https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an717.pdf>