1. Determine which lines have syntax errors in the accompanying VHDL code: 8.5 / 10 points

```
library ieee;                                   -- line 1
use ieee.std_logic_1164.all;                    -- line 2
                                                -- line 3
entity find_errors is (                         -- line 4
    a: bit_vector(0 to 3);                      -- line 5
    b: out std_logic_vector(3 to 0);            -- line 6
    c: in bit_vector(5 downto 0))               -- line 7
end find_errors;                                -- line 8
                                                -- line 9
architecture not_good of find_errors            -- line 10
  begin                                         -- line 11
  my_label: process                             -- line 12
    begin                                       -- line 13
    if c = x"F" then                            -- line 14
      b <= a;                                   -- line 15
    else                                        -- line 16
     b <= '0101';                               -- line 17
    end if                                      -- line 18
  end process;                                  -- line 19
end not_good                                    -- line 20
```

Select only the line numbers in which errors occur. You should find about 8-10 errors.

- [ ] Error in Line 1
- [ ] Error in Line 2

- [ ] Error in Line 1
- [ ] Error in Line 2
- [ ] Error in Line 3
- [x] Error in Line 4

Correct
missing keyword port after is

- [x] Error in Line 5

This should not be selected
No error

- [x] Error in Line 6

Correct
should be 3 downto 0

- [x] Error in Line 7

Correct
missing semicolon at end.

- [ ] Error in Line 8
- [ ] Error in Line 9
- [x] Error in Line 10

Correct
missing keyword is at the end

missing keyword is at the end

- [ ] Error in Line 11
- [x] Error in LIne 12

Correct
process sensitivity list is missing

- [ ] Error in Line 13
- [x] Error in Line 14

Correct
comparison will always be false because of vector length mismatch

- [ ] Error in Line 15
- [ ] Error in Line 16
- [ ] Error in Line 17
- [x] Error in Line 18

Correct
missing semicolon

- [ ] Error in Line 19
- [x] Error in Line 20

Correct
missing semilcolon

1. Name the parts of a VHDL file? **1 / 1 point**

- ○ Entity and Architecture pair
- ◉ Library, Entity, and Architecture
- ○ Entity input, output, and Architecture process
- ○ Module, Sensitivity list, and Signals

Correct
Correct.

2. The V in VHDL stands for? **1 / 1 point**

- ○ Very
- ○ Verilog
- ◉ Very High Speed IC
- ○ Version 5 (V) of Hardware Description Language

Correct
Yes.

3. The VHDL variable assignment operator := has: **1 / 1 point**

- (●) Current value
- ( ) Future value
- ( ) Previous value
- ( ) All of the above

Correct
Correct.

4. The following VHDL signals are equivalent: **1 / 1 point**

- ( ) D(1), d(2)
- (●) DATA_in : std_logic, data_IN : std_logic
- ( ) string "abc", string "123"
- ( ) X : INTEGER, Y : REAL

Correct

5. The library for VHDL std_logic type includes the values of: **1 / 1 point**

U X 0 1 Z W L H - If the function truth table for "not" function is : not '1' = '0',

please provide : not 'X' = ?

- ○ '0'
- ○ '1'
- ○ 'Z'
- ◉ 'X'

Correct
Yes, it is X Unknown.

6. In the FPGA design flow, Timing based simulation occurs: **1 / 1 point**

- ○ Before synthesis and placement of logic
- ◉ After synthesis and placement of logic

Correct
Yes, timing is based on the location of the placed cells.

7. If A = "1010", using the shift left logical, Provide ? <= A SLL 2

1 / 1 point

- ○ "1011"
- ◉ "1000"
- ○ "1010"
- ○ "0010"

Correct
Correct.

8. Which one of the following statements is correct about VHDL signals? (**Mark all that apply**)

1 / 1 point

- ☐ Signals can be defined within entity block.
- ☐ Signals connected to ports must have the same “mode specifier”. (i.e. in, out, inout, …)
- ☑ Signals can be used in both concurrent assignments and in sequential blocks.

Correct
This is correct.

- ☑ A signal changes its value at the “same time" at the next scheduled event after the signal assignment expression is evaluated.

Correct

9. VHDL can be implemented into the following devices: **1 / 1 point**

- ○ FPGA
- ○ ASIC
- ○ CPLD
- ◉ All of the above

Correct
Yes.

10. Types of VHDL port Declarations in the Entity: **1 / 1 point**

- ○ generics
- ○ signals
- ○ input, output, inout
- ◉ in, out, inout

Correct
Correct, this is the VHDL port declaration type.