Introduction to FPGA Design for Embedded Systems

Week 1 Assignment

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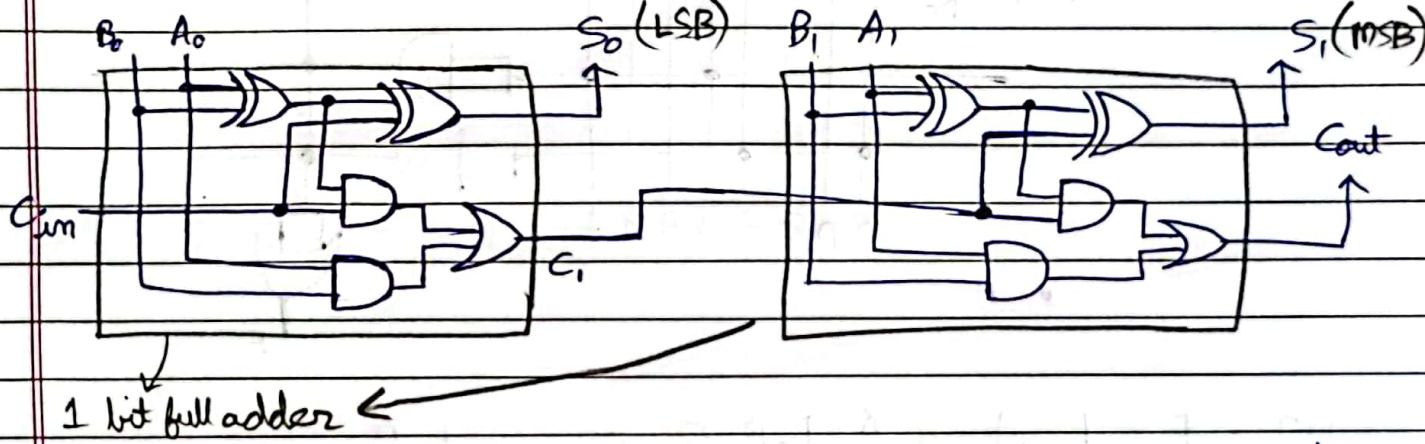
Q1) Let $A = (A_1, A_0)$ and $B = (B_1, B_0)$ be the 2 numbers added, along with C_{in} as the input carry.
Correspondingly, $S = (S_1, S_0)$ will be the sum and C_{out} the carry.
The schematic can be hierarchially implemented by cascading 2 one-bit full adders, as shown.



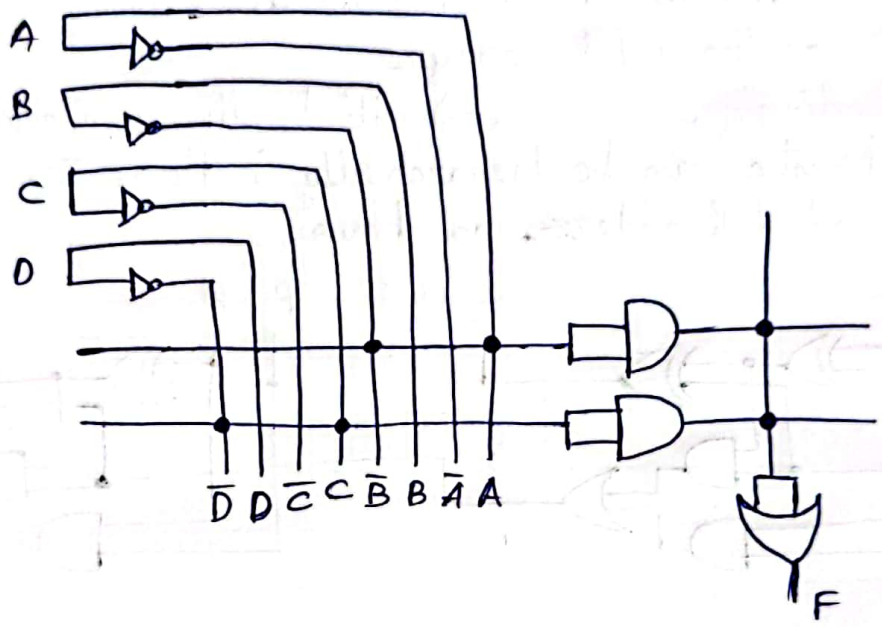
The cascading is done by giving the output carry of LSB to the input carry of the MSB (as the carry done in basic addition).

Here,
$$S_0 = A_0 \oplus B_0 \oplus C_{in} = A_0 \text{ XOR } B_0 \text{ XOR } C_{in}$$
$$C_1 = (A_0 \oplus B_0) \cdot C_{in} + A_0 \cdot B_0$$
$$S_1 = A_1 \oplus B_1 \oplus C_1$$
$$C_{out} = (A \oplus B_1) \cdot C_1 + A_1 \cdot B_1$$

2) Let $F = A\bar{B} + C\bar{D}$

We have 2 AND arrays and 1 OR array.
So the AND arrays can be used to generate $A\bar{B}$ and $C\bar{D}$ respectively, and then these two can be added using the OR array.

Schematic:



LUT: F = 1 when A=1, B=0 or C=1, D=0

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0