1. Which of the following characteristics are used for selection of a Programmable Logic Device? (**Mark all that apply**) **1 / 1 point**

- [x] Power Consumption

  Correct
  Excellent!

- [x] Size or Logic Density

  Correct
  Excellent!

- [ ] Sustainability
- [ ] Manufacturer
- [x] Speed

  Correct
  Excellent!

- [x] Reliability

  Correct
  Excellent!

2. The CoolRunner II CPLD has the following features: (**Mark all that apply**) **1 / 1 point**

- [x] Deterministic timing

  Correct
  It has deterministic timing, 5 ns pin to pin delay.

- [ ] More than 2000 flip flops
- [x] I/O rich device

  Correct
  This device has up to 270 I/O pins, so lots of I/O per register, almost one to two.

- [x] Low power

  Correct
  The CoolRunner II CPLD part was designed with low power in mind, hence the name, and includes several low power features.

3. Which of the following characteristics are advantages for the selection of Anti-Fuse FPGAs over Flash FPGAs? (**Mark all that apply**) **0.5714285714285714 / 1 point**

- [ ] Reprogrammability

3. Which of the following characteristics are advantages for the selection of Anti-Fuse FPGAs over Flash FPGAs? (**Mark all that apply**)

0.5714285714285714 / 1 point

- [ ] Reprogrammability
- [ ] Power Consumption
- [ ] Deterministic Timing
- [ ] Hard IP
- [x] Speed

Correct
Excellent!

- [x] Reliability (FIT Rate)

This should not be selected
Reliability is not a significant advantage for Anti-fuse FPGAs

- [x] Data Security

This should not be selected
Data Security is not an advantage for Anti-fuse FPGAs

4. Which of these are advantages of Microsemi Flash Technology? (**Mark all that apply**)

0.8571428571428571 / 1 point

- [x] True FLASH based technology for routing

  Correct
  Excellent!

- [ ] Higher total system cost
- [x] Reprogrammability

  This should not be selected
  FLASH FPGAs are reprogrammable, but so are SRAM FPGAs.

- [x] Low Power

  Correct
  Excellent!

- [ ] Speed
- [x] Design Security

  Correct
  Excellent!

- [x] Superior Reliability

  Correct
  Excellent!

5. Which of the following statements are correct? (**Mark all that apply**) **1 / 1 point**

- [ ] Microsemi Accelerator and RTAX family are Flash based FPGAs.
- [x] Microsemi Accelerator and RTAX family are antifuse based FPGAs.

Correct
Excellent!

- [ ] Microsemi Accelerator and RTAX family are reprogrammable and nonvolatile.
- [x] Microsemi Accelerator and RTAX family are designed for high reliability.

Correct
Excellent!

6. Which of the following statements are correct? (**Mark all that apply**) **1 / 1 point**

- [ ] ECP3 and ECP5 are Flash based FPGAs.
- [x] ECP3 and ECP5 are SRAM based FPGAs.

Correct
Excellent!

- [x] MACHX02 and MACHX03 are single chip solutions with an NVCM.

6. Which of the following statements are correct? (**Mark all that apply**) **1 / 1 point**

- [ ] ECP3 and ECP5 are Flash based FPGAs.
- [x] ECP3 and ECP5 are SRAM based FPGAs.

Correct
Excellent!

- [x] MACHX02 and MACHX03 are single chip solutions with an NVCM.

Correct
Excellent!

- [ ] MACHX02 and MACHX03 are Flash based CPLDs.
- [x] ECP3 and ECP5 support several specialized multiplier functionality such as Multiply Accumulate

Correct
Excellent!

7. Which of the following statements are correct? (**Mark all that apply**) **1 / 1 point**

- [ ] The use of Xilinx CPLDs are efficient in the implementation of adders or shift registers as the available

7. Which of the following statements are correct? (**Mark all that apply**) **1 / 1 point**

- [ ] The use of Xilinx CPLDs are efficient in the implementation of adders or shift registers as the available macrocell is used optimally .
- [x] The use of Xilinx CPLDs are efficient in the implementation of comparators and decoders as the available macrocell is used optimally.

Correct
Excellent!

- [x] Xilinx small FPGAs are more efficient in the implementation of adders or shift registers than CPLDs.

Correct
Excellent!

8. Which of the characteristics are available from the families of Xilinx CPLDs and FPGAs? (**Mark all that apply**) **0.6666666666666666 / 1 point**

- [ ] ***Spartan 6:*** FPGA , SRAM-based , 4-input LUT
- [x] ***7 series*** : FPGA , SRAM-based , 6-input LUT

8. Which of the characteristics are available from the families of Xilinx CPLDs and FPGAs? (**Mark all that apply**) 0.6666666666666666 / 1 point

- [ ] ***Spartan 6:*** FPGA , SRAM-based , 4-input LUT
- [x] ***7 series*** : FPGA , SRAM-based , 6-input LUT

Correct
Excellent!

- [ ] ***XC9500XL*** : CPLD
- [x] ***Spartan 6*** : FPGA , SRAM-based , 6-input LUT

Correct
Excellent!

- [ ] ***7 series*** : FPGA , SRAM-based , 4-input LUT
- [x] ***XC9500XL*** : CPLD , Low power

This should not be selected
the XC9500XL is not a low power device.

9. What kind of device should best be used in a design that requires expansion of I/O? 1 / 1 point

- (•) CPLD

9. What kind of device should best be used in a design that requires expansion of I/O? **1 / 1 point**

- (●) CPLD
- ( ) FPGA
- ( ) ASSP
- ( ) Op-Amp

Correct
CPLDs have many I/O relative to the amount of logic so are ideal for I/O Expansion.

10. Which of the characteristics best match the families of Altera CPLDs and FPGAs? (**Mark all that apply**) **1 / 1 point**

- [ ] ***MAX V***: CPLD , 4-input LUT , SRAM
- [x] ***Cyclone V***: FPGA , 8-input Adaptive LUT , SRAM

Correct
Excellent!

- [ ] ***Arria 10***: FPGA , 6-input LUT

10. Which of the characteristics best match the families of Altera CPLDs and FPGAs? (**Mark all that apply**) **1 / 1 point**

- [ ] ***MAX V***: CPLD , 4-input LUT , SRAM
- [x] ***Cyclone V***: FPGA , 8-input Adaptive LUT , SRAM

Correct
Excellent!

- [ ] ***Arria 10***: FPGA , 6-input LUT
- [x] ***Stratix V***: FPGA , SRAM , 6-input LUT

Correct
Excellent!

- [ ] ***MAX 10***: FPGA , 6-input LUT , FLASH
- [ ] ***Cyclone V***: FPGA , 6-input LUT , FLASH

11. Consider an application that requires 5V I/O. What might be an appropriate family to use to implement a programmable logic solution? **1 / 1 point**

- ( ) Altera MAX10
- (•) Xilinx XC9500XL

11. Consider an application that requires 5V I/O. What might be an appropriate family to use to implement a programmable logic solution? **1 / 1 point**

- ○ Altera MAX10
- ◉ Xilinx XC9500XL
- ○ Microsemi SmartFusion
- ○ Lattice ICE40

Correct
Correct. The Xilinx XC9500XL has 5V I/O.

12. Assuming the same process geometry, when designing adder circuits, what advantages accrue from using an architecture with 8-input LUTs versus 4-input LUTs? (**Mark all that apply**) **0.5 / 1 point**

- ☑ Higher speed calculation

This should not be selected
If pipelined, the speed of calculation will not be significantly different.

- ☐ Lower latency
- ☑ Fewer LUTs

Correct
Excellent!

- ☐ Bigger Outputs

13. What are the essential capabilities that we need in an FPGA? (**Mark all that apply**) **0.6 / 1 point**

- [x] Low Latency

  This should not be selected
  Low latency is not a characteristic used to select FPGAs.

- [x] Low power consumption

  Correct
  Excellent!

- [x] Drive Strength

  This should not be selected
  Drive strength of outputs may vary some, but is not usually an essential driver in FPGA selection.

- [x] Reprogrammability

  Correct
  Excellent!

- [ ] Fitness

14. Xilinx CPLD Macrocells include: (**Mark all that apply**) **1 / 1 point**

- [ ] Multiple LUTS
- [x] Wide-input AND-OR Array

Correct
Excellent!

- [x] Flip-Flop with global set/reset

Correct
Excellent!

- [ ] Analog inputs

15. In Xilinx SPARTAN 3AN FPGAs, the Logic Slice consists of: **1 / 1 point**

- ( ) A LUT and a Flip-flop
- ( ) 2 LUTs and a Flip-Flop
- (•) 2 LUTs and 2 Flip-Flops
- ( ) A LUT and 2 Flip-Flops

Correct
Correct.

- [ ] Analog Inputs

15. In Xilinx SPARTAN 3AN FPGAs, the Logic Slice consists of: **1 / 1 point**

- ○ A LUT and a Flip-flop
- ○ 2 LUTs and a Flip-Flop
- ◉ 2 LUTs and 2 Flip-Flops
- ○ A LUT and 2 Flip-Flops

✓ **Correct**
Correct.

16. Xilinx Ultrascale Transceivers have aggregate bandwidth in excess of: **1 / 1 point**

- ○ 1 Gbps
- ○ 10 Gbps
- ◉ 1 Tbps
- ○ 100 Mbps

✓ **Correct**