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Module 1 Quiz
Graded Quiz • 30 min

English

Due Nov 12, 11:59 PM IST

1. Select the true statements regarding Soft Processors:

1 / 1 point

- [x] Soft Processors provide flexibility with Hardware vs. Software tradeoff.

Correct
This is correct!

- [ ] Soft Processors cannot be pre-compiled before selecting FPGA for size and frequency.
- [x] Soft Processors can be migrated into future FPGA devices.

Correct
Yes, the big advantage of soft processors is that they are migratable.

- [ ] Soft Processors do not allow cache size selection.

2. NIOS II soft processor has a ___-bit RISC architecture.

1 / 1 point

32

Correct

3. The NIOS II (E) Economy soft core processor operates at a _____ frequency than the NIOS II (F) Fast soft core. **0 / 1 point**

195 MHz

Incorrect
The operating frequency comparison between the two variants.

4. The NIOS II (E) Economy soft core processor operates at a _____ MIPS rate than the NIOS II (F) Fast soft core. **0 / 1 point**

18

Incorrect
The MIPS comparison between the two variants.

5. The Xilinx Microblaze soft core processor uses the following bus structure: **1 / 1 point**

5. The Xilinx Microblaze soft core processor uses the following bus structure: **1 / 1 point**

- ○ Avalon
- ○ Custom 32 bit
- ○ AHB
- ◉ AXI

Correct
Correct!

6. The .___ file is loaded to the configuration flash which loads the SRAM at each power ON. **1 / 1 point**

pof

Correct

7. **1 / 1 point**

The NIOS II Soft processor uses the following files for software configuration: (**Mark all that apply**)

- [x] .sopcinfo

  Correct
  Yes, needed to establish the processor architecture

- [x] .elf

  Correct
  Yes, the output of the software compilation

- [x] .hex

  Correct
  Yes, used for programming software images

- [x] system.h

  Correct
  Yes, an output from Qsys used to define the parameters of the processor

- [ ] .config

- [ ] .config

8. The ARM Cortex M1 Soft processor can be compiled into the following FPGA devices: **0 / 1 point**

- ( ) Xilinx
- ( ) Altera
- (•) Microsemi
- ( ) All of the above

Incorrect
Correct but it can also be compiled into the other FPGA devices.

9. For the NIOS II, both the instruction and data buses are implemented as _____ ports. **1 / 1 point**

master

Correct
Correct!

10. The NIOS II soft core processor has ___ IRQ interrupt(s). **1 / 1 point**

- ○ 10
- ○ 16
- ◉ 32
- ○ 1

Correct
This is correct.

11. In the NIOS II core, MMU and MPU: **1 / 1 point**

- ○ Can be used together
- ◉ Are exclusive
- ○ Are not available
- ○ Are necessary

Correct
MMU and MPU are exclusive in NIOS II core.