Congratulations! You passed!

Grade received 83.57%

Latest Submission Grade 83.58%

To pass 70% or higher

Go to next item

1. What was missing in CPLDs that created a need for devices like FPGAs ?

1 / 1 point

- ○ Designs that required many flip-flops
- ○ Designs that contained large amounts of sequential circuits
- ◉ All of the above

✓ **Correct**
Completely correct.

2. Which of the following characterize CPLDs ? (**Select all that apply**)

0.8333333333333334 / 1 point

- ☑ LUTs

✗ **This should not be selected**
Use of LUTs for logic characterizes FPGAs, not CPLDs

2. Which of the following characterize CPLDs ? (**Select all that apply**) **0.8333333333333334 / 1 point**

- [x] LUTs

  This should not be selected
  Use of LUTs for logic characterizes FPGAs, not CPLDs

- [ ] Scales easily to larger devices
- [x] Predictable

  Correct
  Correct. CPLDs have predictable timing because of the fixed routing structure

- [ ] Rich with FFs/registers
- [x] Easy to design with

  Correct
  Correct. CPLDs have a clear structure and good software tools that make them easy to design with.

- [x] Deterministic

  Correct
  Correct. CPLDs have deterministic timing.

3. Fill in the table so that the LUT implements: **1 / 1 point**

F = (~A & B) | (~C & ~D)

RAM CONTENTS				
Address				Output Data
A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	a
0	0	1	1	0
0	1	0	0	1
0	1	0	1	b
0	1	1	0	1
0	1	1	1	c
1	0	0	0	1
1	0	0	1	0
1	0	1	0	d
1	0	1	1	0
1	1	0	0	1
1	1	0	1	e
1	1	1	0	0
1	1	1	1	0

1	1	1	1	0

a = __

b = __

c = __

d = __

e = __

Enter your numerical answers separated by a comma

(example: ***x,x,x,x,x*** or **1,1,1,1,1**)

0,1,1,0,0

Correct

4. Which of the following characteristics best match a **CPLD** and which best match an **FPGA**? **1 / 1 point**

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- ***CPLD :***PLDs that are an integrated circuit designed to be configured by the designer after manufacturing and made up of memory elements (LUTs) and registers.

  FPGA :A PLD with multiple PALs in the same package with registered outputs and an interconnecting programmable fabric.

- ***CPLD :***PLDs that are an integrated circuit designed to be configured by the designer after manufacturing and made up of memory elements (LUTs) and registers.

  FPGA :A PLD with a fixed AND plane and a programmable OR plane.

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- ***CPLD :***A PLD with a fixed AND plane and a programmable OR plane.

  FPGA :PLDs that are an integrated circuit designed to be configured by the designer after manufacturing and made up of memory elements (LUTs) and registers.

Correct
Correct for both!

5. Which of the following characteristics best matches **PROM** and which of the following best match a **PAL** ? **1 / 1 point**

- ***PAL :***PLD with a fixed AND plane and a programmable OR plane

  PROM :is a semiconductor device integrated circuit (IC) product that is dedicated to a specific application market and sold to more than one user

- ***PAL :***PLD with a fixed OR plane and a programmable AND plane

  PROM :PLDs with multiple PALs in the same package with registered outputs and an interconnecting programmable fabric

- ***PAL :***PLD with a fixed AND plane and a programmable OR plane

  PROM :PLD with a fixed OR plane and a programmable AND plane

- ***PAL :***PLD with a fixed OR plane and a programmable AND plane

  PROM :PLD with a fixed AND plane and a programmable OR plane

Correct
Correct for both!

6. Which of the following is the best definition for a **CPLD ?** **1 / 1 point**

- A device with multiple PALs in same package with registered outputs and interconnecting programmable

6. Which of the following is the best definition for a **CPLD ?** **1 / 1 point**

- (●) A device with multiple PALs in same package with registered outputs and interconnecting programmable fabric
- ( ) A device with a combination of fully re-programmable AND/OR array and a bank of macrocells that perform combinational and sequential logic
- ( ) An array of programmable logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together", like many logic gates that can be inter-wired in different configurations

Correct
Correct, this is a good description of a CPLD.

7. Which of the following characteristics are associated with **Flash FPGAs** ? **1 / 1 point**

(**Select all that apply**)

- [x] High Reliability

Correct
Correct, FLASH FPGAs are highly reliable and immune to Single Event Upsets (SEU)

- [ ] Highest Density

7. Which of the following characteristics are associated with **Flash FPGAs** ? **1 / 1 point**

(**Select all that apply**)

- [x] High Reliability

  Correct
  Correct, FLASH FPGAs are highly reliable and immune to Single Event Upsets (SEU)

- [ ] Highest Density
- [x] Reprogrammable

  Correct
  Correct, FLASH FPGAs can be reprogrammed in circuit many times.

- [x] Expensive

  Correct
  FLASH FPGAs tend to be somewhat expensive

- [ ] One time Programmable (OTP)
- [ ] Lowest Cost

8. How many **4-input LUTs** with single outputs will be required to implement a **2-bit full adder** with carry? **1 / 1 point**

- ○ 2
- ◉ 4
- ○ 1
- ○ 3

Correct
Correct, 4 LUTs are required to make a 2-bit adder.

9. Does the usage of LUTS for implementation of adders with respect to gates improve delay or performance? Select all that apply.. **0.75 / 1 point**

- ☑ decreases delay

Correct
True, as the number of gate delays will be larger than the number of LUT delays. The result of the implementation of the 4-bit ripple-carry adder in the Altera MAX10 FPGA is made of a cascade of 4 pairs of 3-input LUTs. The delay through this circuit will be only 4 LUT delays, not 11 gate delays as based on the delay equation of Carry Look ahead adder.

- ☐ increases delay

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- [ ] increases delay
- [ ] increases performance
- [ ] decreases performance

You didn't select all the correct answers

10. Which of the characteristics match the implementation of a multiplier in an FPGA using Combinational Circuits versus Sequential Shift algorithms ? (**Mark all that apply**) **1 / 1 point**

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- [x] **Combinational circuits**: Fast , Big

  Correct
  Multipliers made with Combinational circuits are fast as they are limited only by the propagation delay through the gates, but many gates are required so it is large.

- [x] **Sequential Shift:** Small , Slow , State Machine

  Correct
  Multipliers made with sequential shifters are slow due to clock delays, but smaller in size than Combinational multipliers.

- [ ] **Combinational circuits**: Small , Big
- [ ] **Sequential Shift**: Fast , Slow , State Machine

11. Which of the characteristics match the implementation of a multiplier in an FPGA using Speciality Circuits, such as the Booth Algorithm ? (**Mark all that apply**) **0.875 / 1 point**

- [x] Fast

11. Which of the characteristics match the implementation of a multiplier in an FPGA using Speciality Circuits, such as the Booth Algorithm ? (**Mark all that apply**) **0.875 / 1 point**

- [x] Fast

  Correct
  Correct, Booth Algorithm multipliers are fairly fast in execution time

- [ ] Big
- [x] Small

  Correct
  Correct. Booth algorithm multipliers are fairly small in area especially for larger multiplicands

- [ ] Slow
- [x] Complex

  Correct
  Correct. Booth algorithm multipliers are more complex than shifter or memory types

- [ ] Do not scale easily
- [ ] Lookup Tables
- [ ] State Machine

You didn't select all the correct answers

You didn't select all the correct answers

12. Which one of the following is **not** a programmable logic device? **1 / 1 point**

- EPROM
- PLA
- CPLD
- ROM (selected)
- FPGA

Correct
Correct. A ROM's bit pattern is set during manufacturing of IC and can't be changed.

13. What is true for ASICs relative to FPGAs? (Select all that may apply) **0.5 / 1 point**

- [x] High cost per unit

This should not be selected
This is incorrect

- [ ] Lower speed

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- [x] High cost per unit

This should not be selected
This is incorrect

- [ ] Lower speed
- [ ] ASICs have lower cost per unit.
- [x] Higher speeds

Correct
Correct. ASICs generally have higher speed than FPGAs

14. What are the principal advantages of FLASH based FPGAs over SRAM based FPGAs ? (**Mark all that apply**) **0.25 / 1 point**

- [x] Faster Speed

This should not be selected
FLASH FPGAs are generally slower than SRAM FPGAs

Correct
Correct. ASICs generally have higher speed than FPGAs

14. What are the principal advantages of FLASH based FPGAs over SRAM based FPGAs ? (**Mark all that apply**) **0.25 / 1 point**

- [x] Faster Speed

This should not be selected
FLASH FPGAs are generally slower than SRAM FPGAs

- [ ] Lower Power
- [x] Higher Reliability

Correct
Correct. FLASH FPGAs are more reliable, with SEU immunity

- [ ] Better Security

15. Which of the following is the best implementation for a 2-bit full adder. Hint: make sure to pay attention to signal names as well as circuit diagram. **0 / 1 point**

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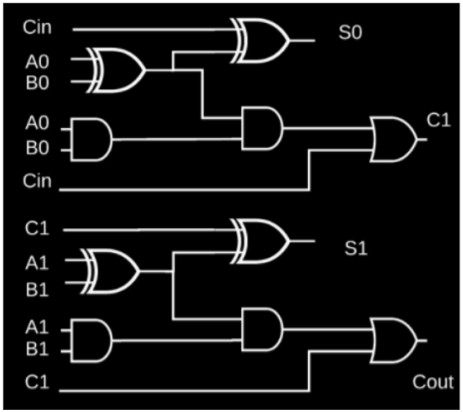


C1
Cout

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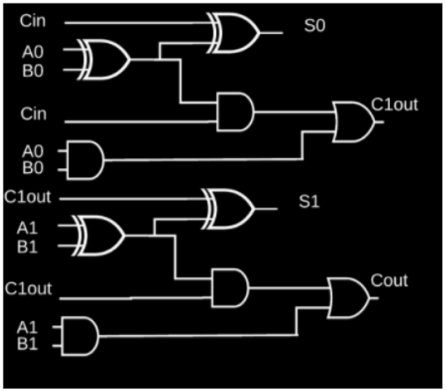
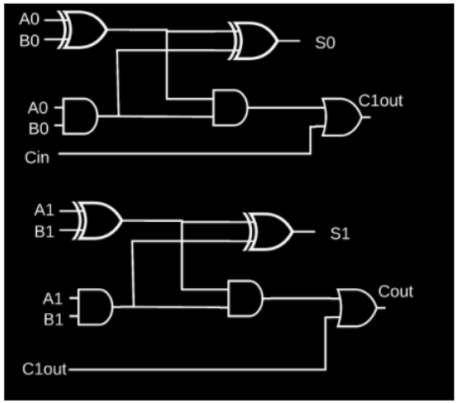

Cin
A0
B0
S0
Cin
A0
B0
C1out
C1out
A1
B1
S1
C1out
A1
B1
Cout

.


A0



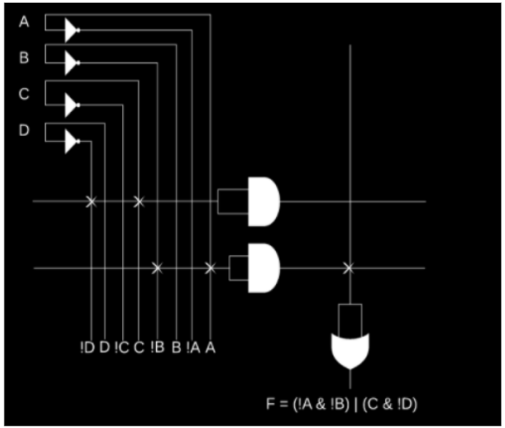
Incorrect
If you missed this, you might want to review Video 6

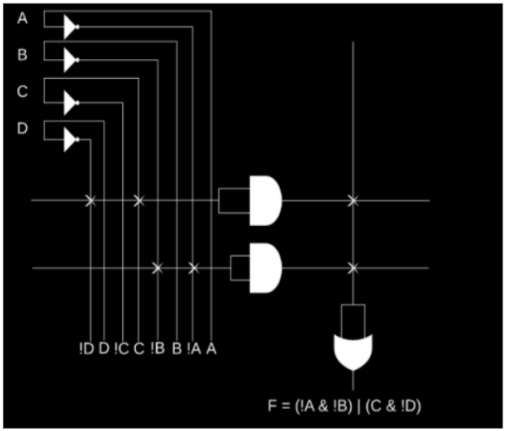
16. Choose the best implementation of the logic equation

1 / 1 point

(NOT(A) AND NOT(B)) OR (C AND NOT(D))

using PLA options:



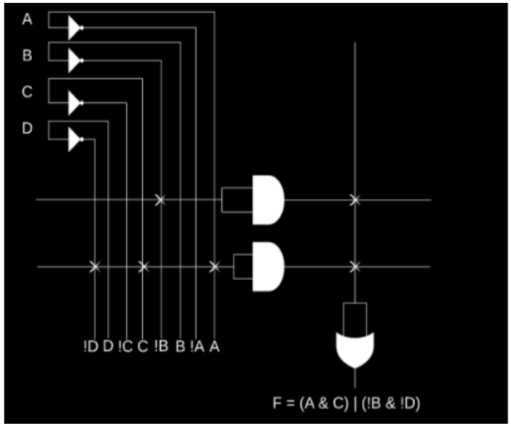

A
B
C
D
!D D !C C !B B !A A
F = (!A & !B) | (C & !D)

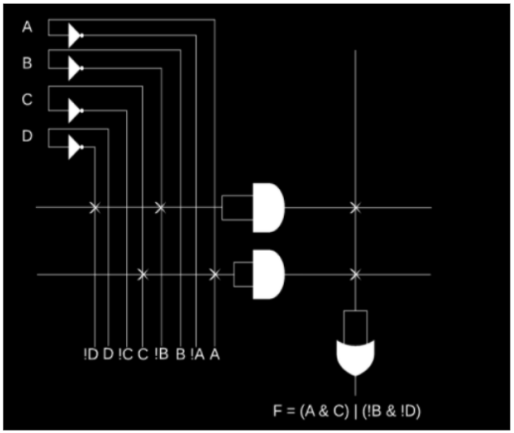
17. Choose the correct implementation of logic equation

1 / 1 point

((A) AND (C)) OR (NOT(B) AND NOT(D))

using PLA options:





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Correct