EW Project - AUDIO AMPLIFIER

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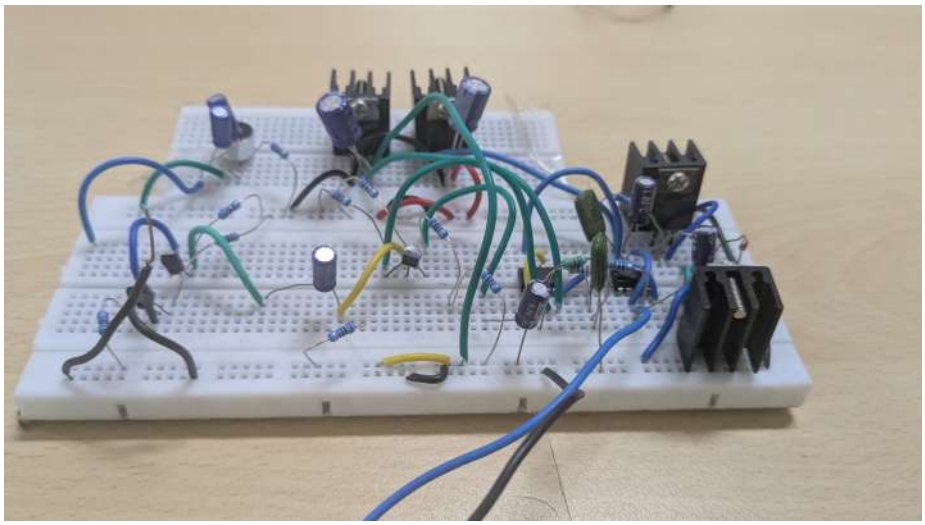


1 Introduction

Audio amplification is an essential aspect of electronic circuit design, widely used in applications ranging from consumer electronics to professional audio systems. The objective of this project is to design and implement a high-gain audio amplifier that efficiently amplifies small input signals while preserving signal fidelity.

The amplifier operates with a dual power supply of $\pm 5V$ (i.e., $V_{DD} = 5V$ and $V_{EE} = -5V$). It is designed to amplify an input signal of 10–20 mV peak-to-peak and achieve an overall voltage gain of 500 across its amplification stages. The amplifier covers the audible frequency range (20 Hz – 20 kHz) and delivers 1.5W power output to a 10Ω load.

The project consists of the following stages:

- **Pre-amplifier Stage:** Provides initial signal amplification and noise reduction.
- **Gain Stage:** Increases voltage and current gain.
- **Low Pass Filter Stage:** Removes unwanted high frequencies components.
- **Power Amplifier Stage:** Drives the load and improves power efficiency.

2 Designing the Pre-Amplifier

The pre-amplifier is responsible for the initial signal amplification and noise reduction. We use a Bipolar Junction Transistor (BJT)-based differential amplifier for this purpose, as shown in Figure **??**.

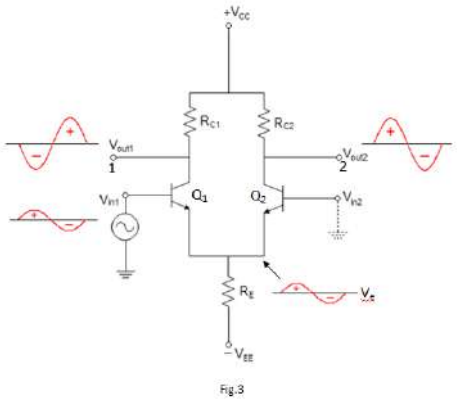


Figure 1: Common Emittor amplifier

This stage is necessary because directly feeding an input signal into a common-emitter amplifier or power amplifier would result in excessive noise, degrading performance. The differential amplifier helps reduce noise and improve signal integrity.

The emitter currents from both BJTs flow through a shared emitter resistance R_{EE}. To analyze the small-signal behavior, consider the following derivations:

2.1 Small-Signal Analysis

When the input voltages V_1 and V_2 differ, the emitter currents are given by:

$$I_{e1} = \frac{V_1 - V_E}{r_e}$$

$$I_{e2} = \frac{V_2 - V_E}{r_e}$$

Since the transistor's current gain α is close to 1, the collector current is approximately equal to the emitter current:

$$V_{C1} = -R_C \frac{V_1 - V_E}{r_e}$$

$$V_{C2} = -R_C \frac{V_2 - V_E}{r_e}$$

Taking the voltage difference at the collectors:

$$V_{C1} - V_{C2} = R_C \frac{V_2 - V_1}{r_e}$$

Thus, the voltage gain is:

$$A_v = \frac{R_C}{r_e}$$

If we ground the second transistor's input (i.e., $V_2 = 0$), the gain at the second transistor's collector simplifies to:

$$A_v = \frac{R_C}{2r_e}$$

Using the transconductance relation:

$$g_m = \frac{1}{r_e} = \frac{I_C}{V_T}$$

where V_T is the thermal voltage (approximately 25mV at room temperature), we can determine r_e based on the desired gain and chosen collector resistance R_C. The DC collector current I_C follows from this relationship.

For the second BJT to remain in the active region, its emitter voltage V_E must be greater than 0.7V. Since the total emitter current is $2I_C$, the voltage across R_{EE} is:

$$V_E = 2I_C R_{EE}$$

Finally, to account for the loading effect of the next stage, the effective gain is given by:

$$A_v = \frac{R_C || R_L}{2r_e}$$

where R_L represents the input resistance of the following stage.

Thus, the pre-amplifier design is complete, ensuring proper signal amplification and noise reduction.

2.2 Working

The differential amplifier amplifies the difference between two input signals, V_{in1} and V_{in2}, while suppressing common-mode noise. In our circuit, we have set $R_{C1} = R_{C2} = R_C$. Performing small-signal analysis on the differential amplifier, we obtain:

$$V_{out1} = \frac{-g_m R_C}{2} \cdot (V_{in1} - V_{in2}) \tag{1}$$

This equation shows that the output voltage depends on the difference between the two input signals. Since the inputs are 180° out of phase, we can express their difference as:

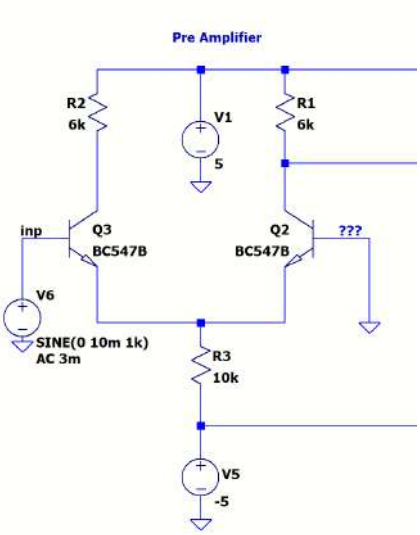


Figure 2: LTSpice simulation of the pre-amplifier

$$V_{in1} - V_{in2} = 2V_{in}$$

Substituting this into the equation:

$$V_{out} = -g_m R_C V_{in}$$

Thus, the voltage gain is:

$$\text{Gain} = -g_m R_C$$

This result shows that the gain is directly proportional to the collector resistance R_C.

2.3 LTSpice Simulations

For simulation, we set $R_C = 5k\Omega$ and $R_E = 5k\Omega$, with $V_{in1} = V_{in}$ and $V_{in2} = 0$. From Equation (1), the output voltage is:

$$V_{out} = \frac{-g_m R_C}{2} \cdot V_{in} \tag{2}$$

Thus, the gain is:

$$\text{Gain} = \frac{-g_m R_C}{2} \tag{3}$$

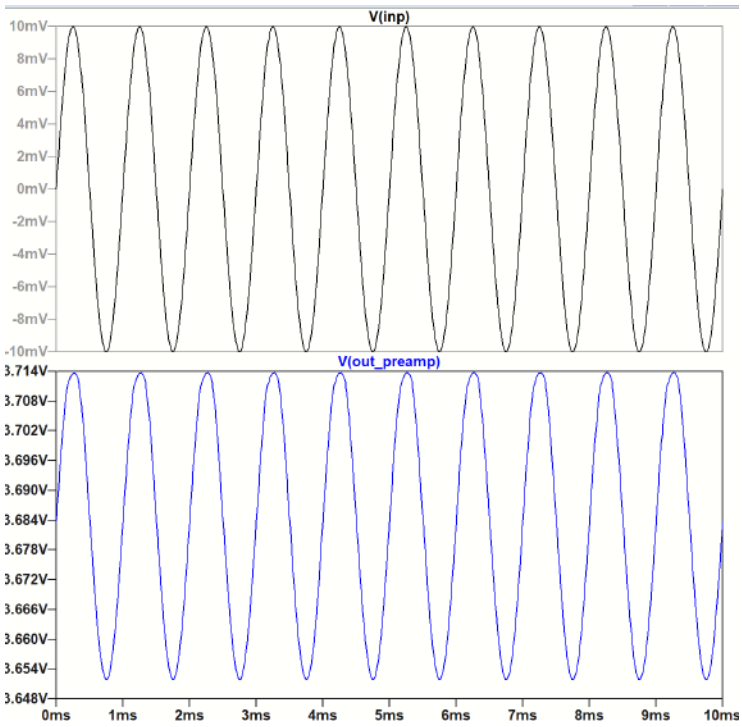


Figure 3: Input Signal

From Figures 3 and **??**, we observe that the gain from the pre-amplifier stage is approximately 15.

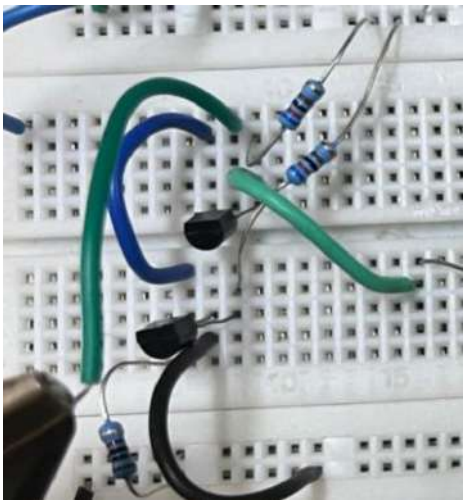


Figure 4: Pre amplifier - hardware

2.4 Hardware Simulations

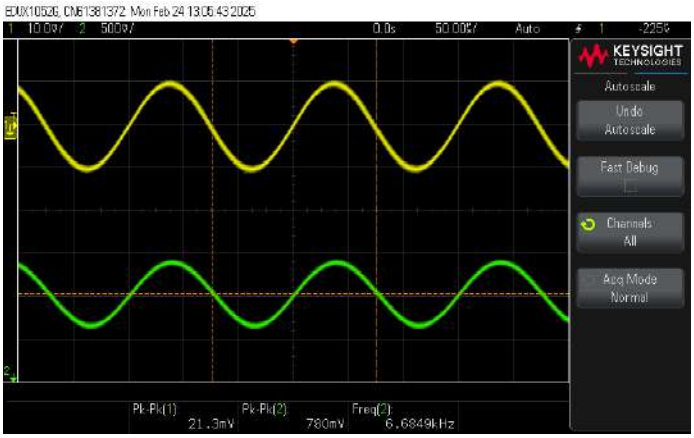


Figure 5: Input and Output for pre-amplifier stage

From the hardware simulation results, we observe that the pre-amplifier stage achieves a gain of approximately 39.

3 Gain/Common Mode Amplifier

For the gain stage, we utilize a BJT-based common-emitter amplifier.

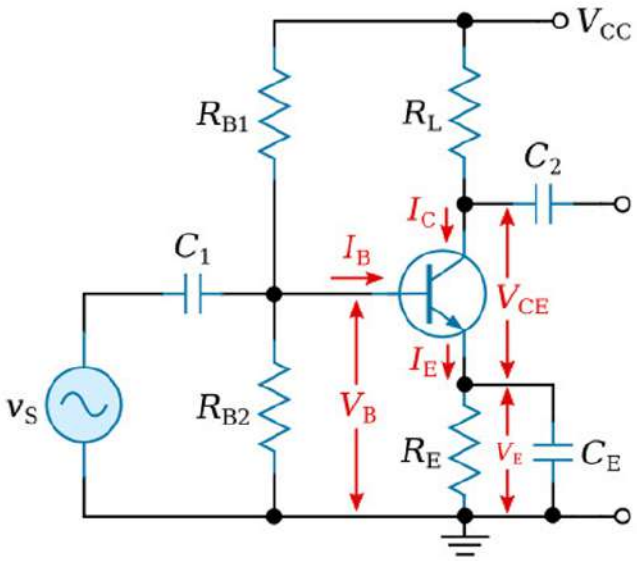


Figure 6: Common-Emitter Amplifier

The common-emitter (CE) amplifier provides both high voltage and current gain. It is a preferred choice due to its high input impedance and low output impedance, making it suitable for signal amplification.

- The input capacitor C_1 blocks DC components from the input signal and contributes a pole to the frequency response. To ensure proper signal transmission within the 20 Hz–20 kHz range, C_1 is chosen to pass all frequencies below 20 kHz. If C_1 is too small, low-frequency signals will be attenuated, and a larger base current I_B will result, lowering the current gain.
- The emitter bypass capacitor C_E stabilizes the amplifier by bypassing AC signals, allowing for greater voltage gain by reducing negative feedback.
- The coupling capacitor C_2 prevents DC biasing from affecting the next stage while allowing AC signals to pass.
- The biasing resistors R_{B1} and R_{B2} form a voltage divider, ensuring the transistor remains in the active region by keeping the base-emitter junction forward-biased and the base-collector junction reverse-biased.

- The stability factor S is given by:

$$S = \left.\frac{\delta I_C}{\delta I_{CBO}}\right|_{V_{BE},\beta} \tag{4}$$

Expressing I_C in terms of I_B and I_{CBO}:

$$I_C = \beta I_B + (\beta + 1) I_{CBO} \tag{5}$$

Differentiating with respect to I_C:

$$\frac{\delta I_C}{\delta I_C} = \beta \frac{\delta I_B}{\delta I_C} + \frac{\beta + 1}{S} \tag{6}$$

Solving for S:

$$S = \frac{\beta + 1}{1 - \beta \frac{\delta I_B}{\delta I_C}} \tag{7}$$

3.1 LTSpice Simulations

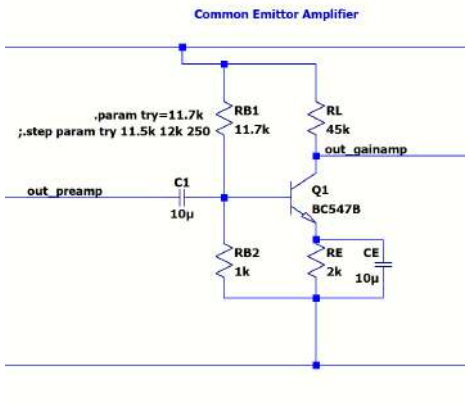


Figure 7: CE amplifier simulation

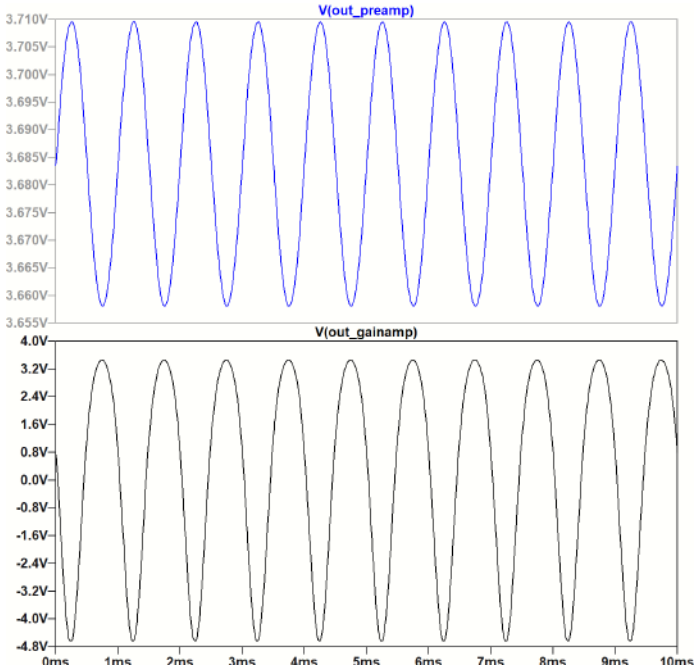


Figure 8: Output of CE amplifier

Upon running the simulations, we observe that the gain of the CE amplifier is approximately **138**.

3.2 Hardware Simulations

Implementing the circuit in hardware, we measure a gain of approximately **10.81** for the CE amplifier stage.

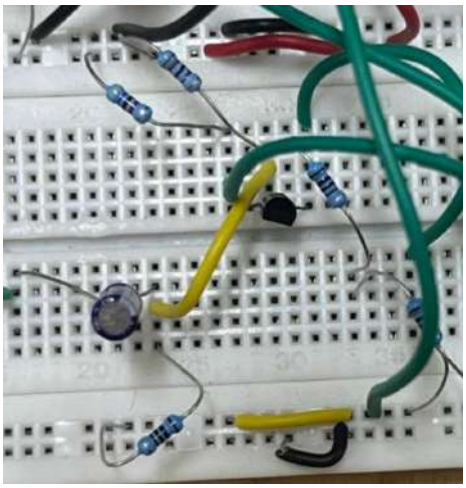


Figure 9: CE amplifier circuit

4 Designing a Low Pass Filter

A low-pass filter is used to ensure that the amplifier operates within the desired frequency range while minimizing high-frequency noise and unwanted signals. The filter plays a crucial role in enhancing audio signal quality before amplification.

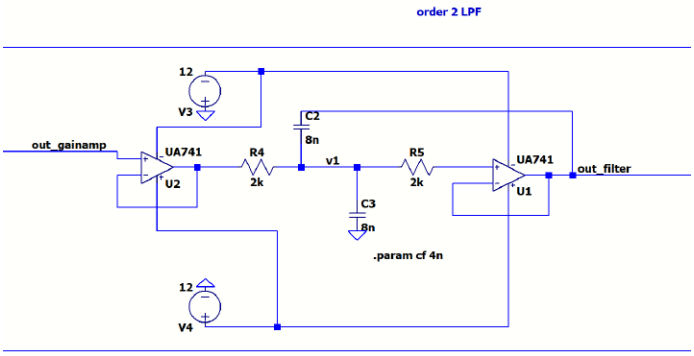


Figure 10: Low-Pass Filter

Purpose of the Filter :

- The filter allows only frequencies below 22 kHz to pass through.
- It removes high-frequency interference that could cause distortion.
- Ensures smooth signal processing before power amplification.

The low-pass filter is implemented using an operational amplifier (op-amp) with resistors and capacitors, forming a second-order active filter that provides improved attenuation of high-frequency components.

4.1 Circuit Description

The given circuit is an active low-pass filter that uses:

- A Resistor-Capacitor (RC) network for frequency-selective attenuation.
- An operational amplifier (op-amp) to provide gain and buffering.

4.2 Working Principle

1. **RC Network:** The resistor-capacitor combination determines the cutoff frequency (f_c), allowing lower frequencies to pass while attenuating higher ones.
2. **Op-Amp Configuration:** The operational amplifier is configured to provide gain and improve filter performance.
3. **Second-Order Filtering:** The cascading of two RC sections results in a sharper roll-off beyond the cutoff frequency.

4.3 Circuit Analysis

The standard second-order active low-pass filter is designed using the Sallen-Key topology. The transfer function is given by:

$$H(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{1 + \frac{s}{\omega_c Q} + \frac{s^2}{\omega_c^2}}$$

where:

- $\omega_c = 2\pi f_c$ is the cutoff angular frequency.
- Q is the quality factor, which determines the damping of the filter.

For a Butterworth response (maximally flat frequency response), $Q = \frac{1}{\sqrt{2}}$. The component selection follows:

$$\omega_c = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

4.4 Cutoff Frequency Calculation

Given that the -3 dB cutoff frequency is:

$$f_c = 22 \text{ kHz}$$

$$\omega_c = 2\pi \times 22 \times 10^3$$

$$\omega_c = 138,230.1 \text{ rad/s}$$

Using the standard Sallen-Key equation:

$$138,230.1 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

Choosing practical values for resistors, let:

$$R_1 = R_2 = 2 \text{ k} = 2000$$

Solving for capacitances:

$$C_1 C_2 = \frac{1}{(2\pi f_c)^2 R_1 R_2}$$

Substituting values:

$$C_1 C_2 = \frac{1}{(2\pi \times 138230.1)^2 \times (2000)^2}$$

$$= \frac{1}{(868547.6)^2 \times 4 \times 10^6}$$

$$= \frac{1}{3.0142 \times 10^{18}}$$

$$C_1 C_2 = 3.32 \times 10^{-19} \text{ F}^2$$

Taking $C_1 = C_2 = C$:

$$C^2 = 3.32 \times 10^{-19}$$

$$C = \sqrt{3.32 \times 10^{-19}}$$

$$C \approx 18.2 \text{ nF}$$

Thus, selecting standard values:

$$C_1 = C_2 = 18 \text{ nF}, \quad R_1 = R_2 = 2 \text{ k}$$

4.5 Key Parameters

1. **Cutoff Frequency (f_c):**
$$f_c = 22 \text{ kHz}$$
2. **Quality Factor (Q):**
$$Q = \frac{1}{\sqrt{2}} \approx 0.707$$
3. **Gain:** The unity-gain configuration is used, ensuring that the filter does not amplify or attenuate signals within the passband.

4.6 Frequency Response

The frequency response of the circuit exhibits:

- **Passband:** Frequencies below 22 kHz pass with minimal attenuation.
- **Attenuation:** Frequencies above 22 kHz are progressively reduced.
- **Steep Roll-Off:** Due to the second-order design, high-frequency suppression is enhanced with a roll-off rate of -40 dB/decade.

4.7 LTSpice Simulations

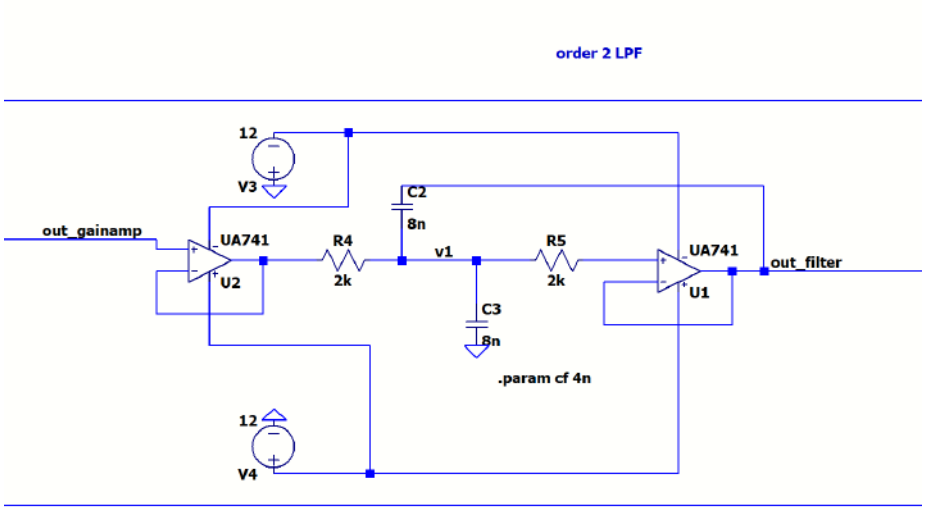


Figure 11: Low-pass filter simulation

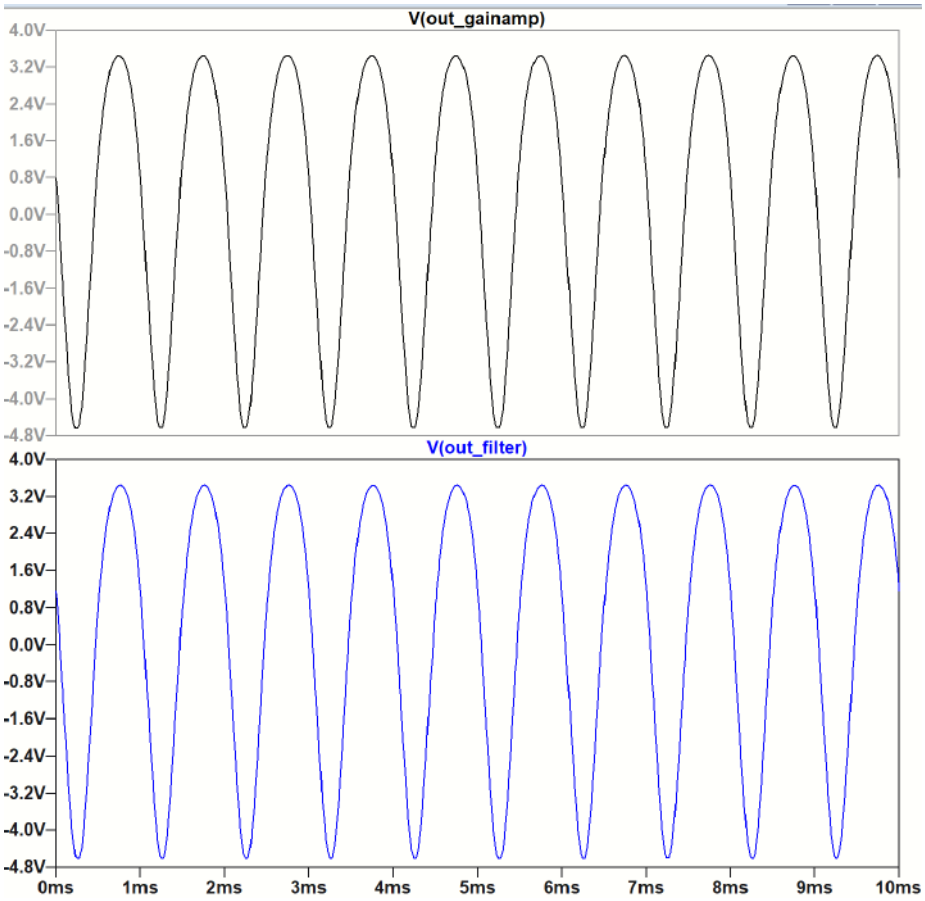


Figure 12: Filter Frequency Response

4.8 Hardware Simulations

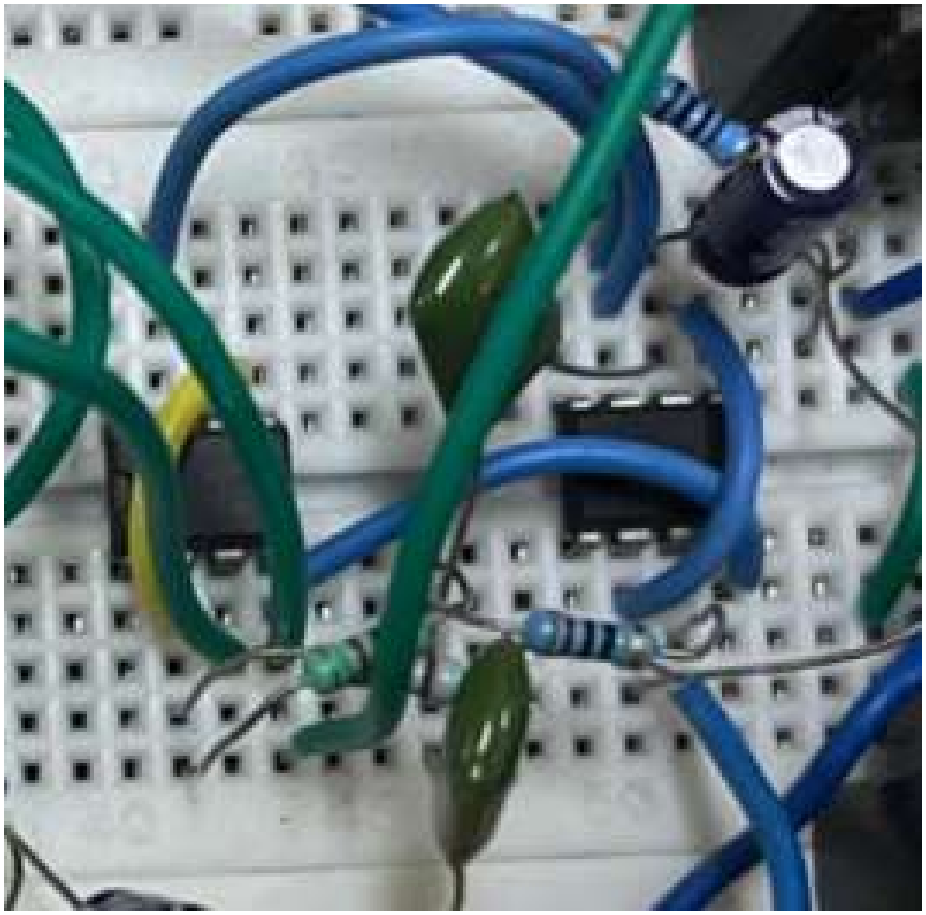


Figure 13: Filter as a part of the complete circuit

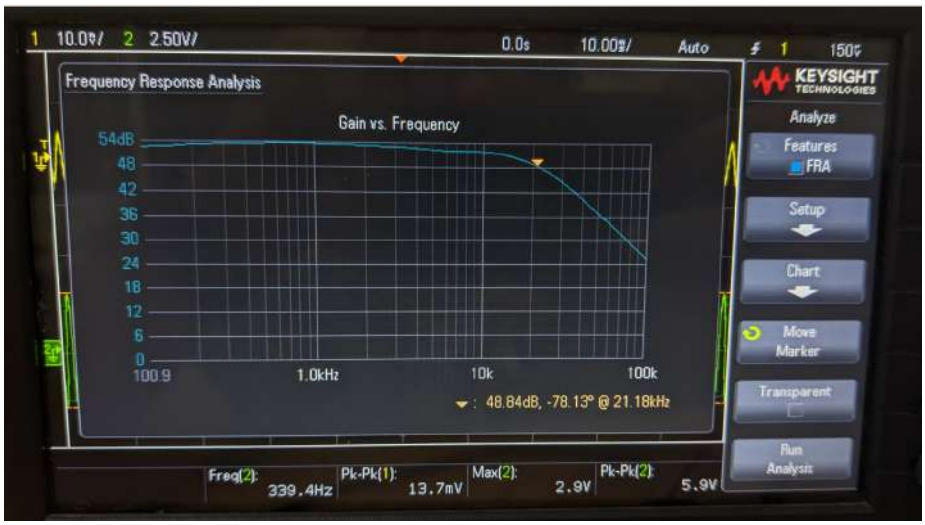


Figure 14: Filter frequency response after implementing in complete circuit

5 Power Amplifier

5.1 Background

Power amplifiers are categorized into different topologies based on their operating characteristics and efficiency. The primary classes considered in this project are:

1. **Class A Amplifier**
   A Class A amplifier operates with a continuously conducting transistor, ensuring high linearity and minimal distortion. However, it exhibits low efficiency, typically around 25–30%, making it less suitable for power-sensitive applications. This topology is mainly employed in high-fidelity audio systems where signal integrity is a priority.

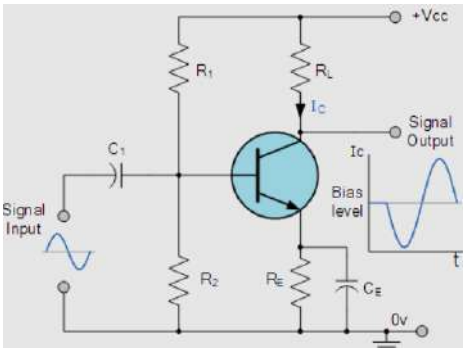


Figure 15: Class A Power Amplifier

2. **Class B Amplifier**
   A Class B amplifier employs a push-pull configuration with two complementary transistors, each conducting for half of the input cycle. This results in higher efficiency (50–70%) compared to Class A. However, the design introduces crossover distortion at the transition between transistors, which can degrade audio quality.

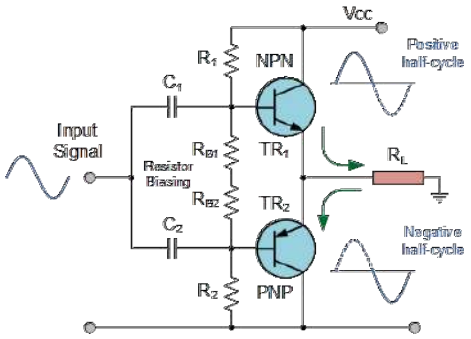


Figure 16: Class B Power Amplifier

3. **Class AB Amplifier**
   A Class AB amplifier is a hybrid design that combines elements of both Class A and Class B to achieve a balance between efficiency and distortion. It operates with a small bias current to reduce crossover distortion while maintaining a relatively high efficiency (50–60%). This topology is commonly used in high-power audio applications where both fidelity and efficiency are critical.

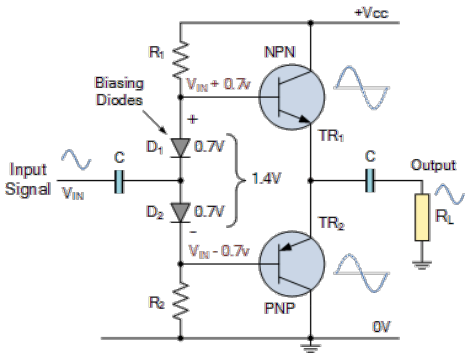


Figure 17: Class AB Power Amplifier

In this project, a **Class AB power amplifier** is selected, as it effectively mitigates crossover distortion present in Class B amplifiers while maintaining higher efficiency compared to Class A. The power amplifier stage receives the amplified and filtered signal from preceding circuit stages, further enhancing the current while ensuring sufficient power delivery to an 8Ω speaker at the output.

5.2 LTSpice Simulations

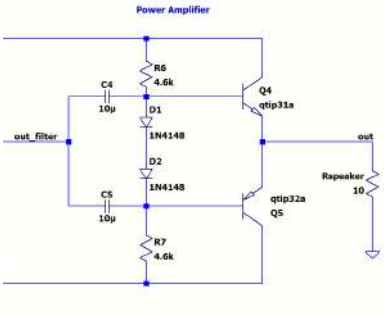


Figure 18: Power Amplifier Circuit in LTSpice

5.2.1 Current Amplification Analysis

Power amplification primarily involves increasing the current while maintaining the voltage level. To validate the amplifier's performance, input and output currents are measured. If the output current exceeds the input current while the voltage remains unchanged, the amplifier is functioning correctly.

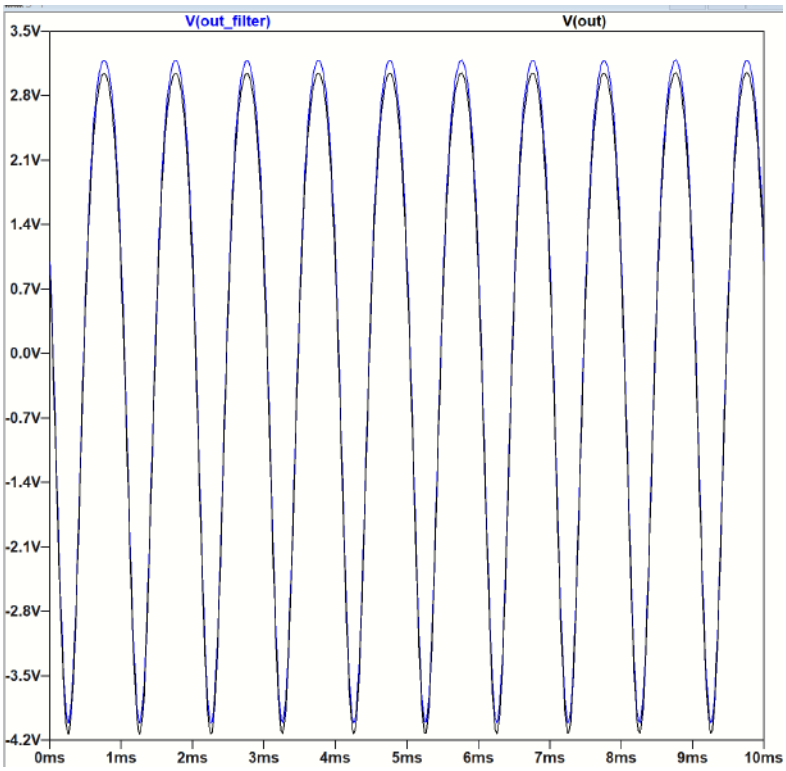


Figure 19: Voltage after Power Amplification

The input current exhibits a peak-to-peak value of $7.37\mu A$. In contrast, the output current reaches a peak-to-peak value of $1A$. This significant increase confirms that the amplifier is successfully amplifying current, thereby enhancing the overall power supplied to the load.

5.2.2 Voltage Consistency Analysis

To verify that the amplifier primarily amplifies current rather than voltage, the input and output voltage waveforms are compared.

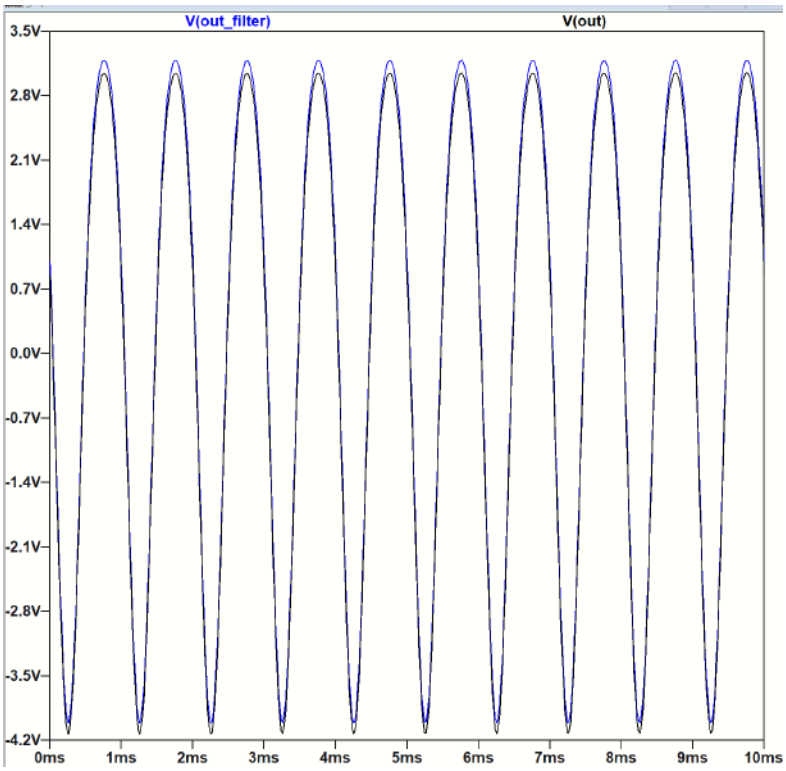


Figure 20: Input Voltage to Power Amplifier

It was observed there was a maximum diffrence of only 0.14 V at maximum gain setting for the amplifier in the circuit between pre power amp and post power stage, proving minimal waveform attenuation

Figures 20 and **??** demonstrate that the output voltage remains consistent with the input voltage. Since the amplifier's current gain has already been confirmed, this consistency ensures that the power amplifier effectively increases power without distorting the voltage signal.

Figure 21: Power amp circuit

5.3 Hardware Simulations

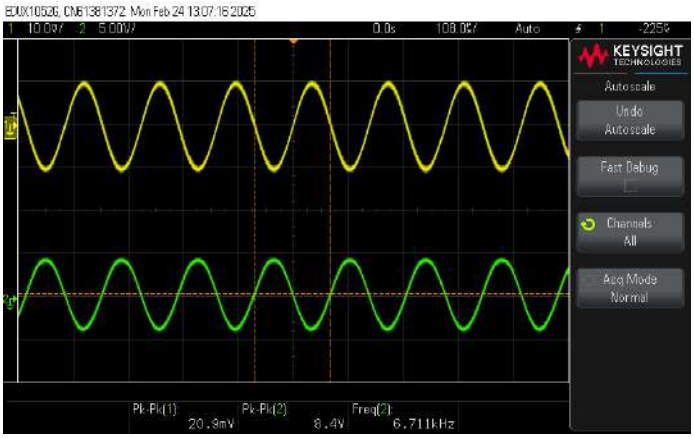


Figure 22: Input Voltage (Green) to Power Amplifier

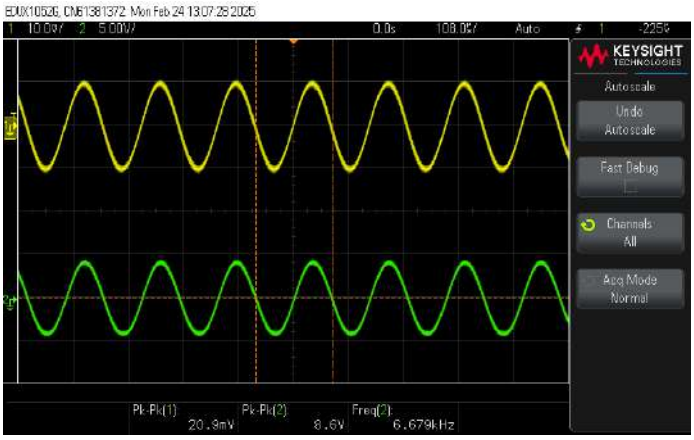


Figure 23: Final Output Voltage (Green) after Power Amplification

The hardware simulation results further validate the amplifier's performance. As shown in Figs. 22 and 23, the input and output voltage signals remain identical. This confirms that the hardware implementation maintains voltage consistency while effectively amplifying current, ensuring successful power amplification.

6 LM voltage regulators for +/-5V from +/-12V

Voltage regulators are essential for providing stable DC voltages in electronic circuits. To obtain ±5V from a ±12V power supply, we use the LM7805 (for +5V) and LM7905 (for -5V) linear voltage regulators.

The LM7805 regulates the +12V input down to a steady +5V output, while the LM7905 takes -12V and provides a stable -5V output. These regulators ensure minimal voltage fluctuations and provide adequate current for low-power applications. To enhance performance, capacitors are placed at the input and output to filter noise and improve stability.

7 Complete Circuit

After designing and analyzing individual stages, we now integrate all components to form the complete audio amplifier circuit. The objective is to ensure proper functionality, signal integrity, and power amplification while minimizing distortion.

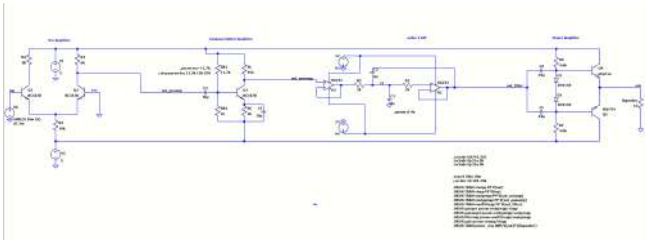


Figure 24: Final Circuit

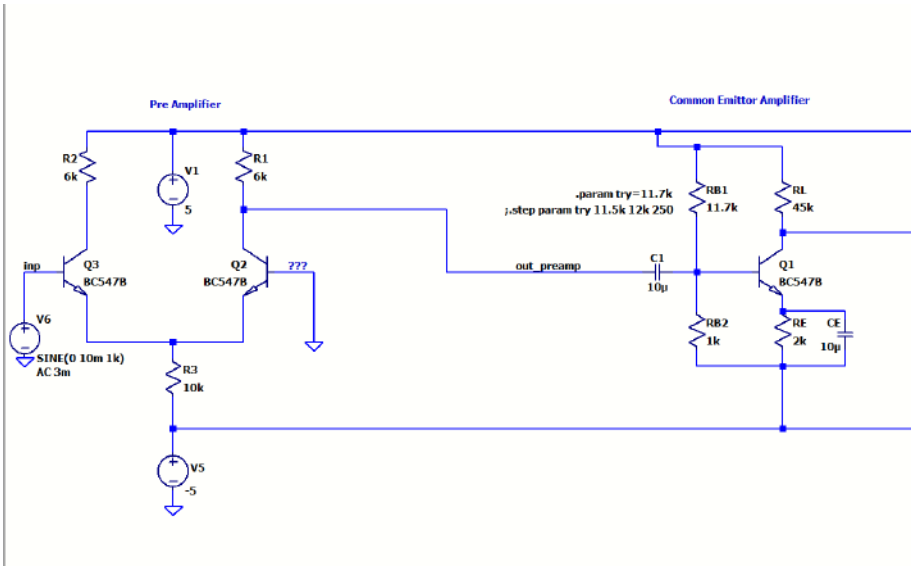


Figure 25: left half

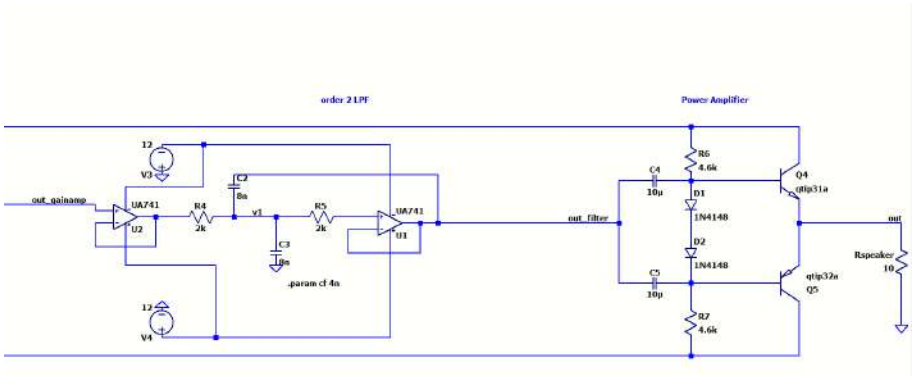


Figure 26: right half

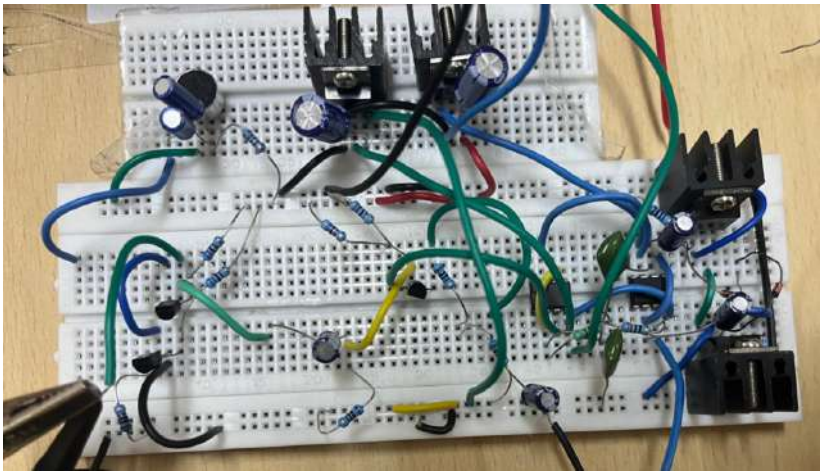


Figure 27: Full circuit on breadboard

7.1 Final Circuit Simulations

To validate the overall circuit performance, the input and output waveforms are analyzed.

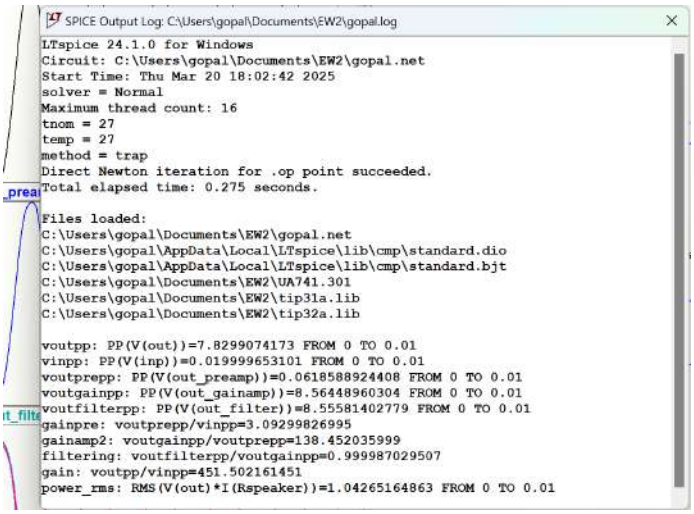


Figure 28: Final observations using LTSpice commands, showing gain from each stage, and final power output

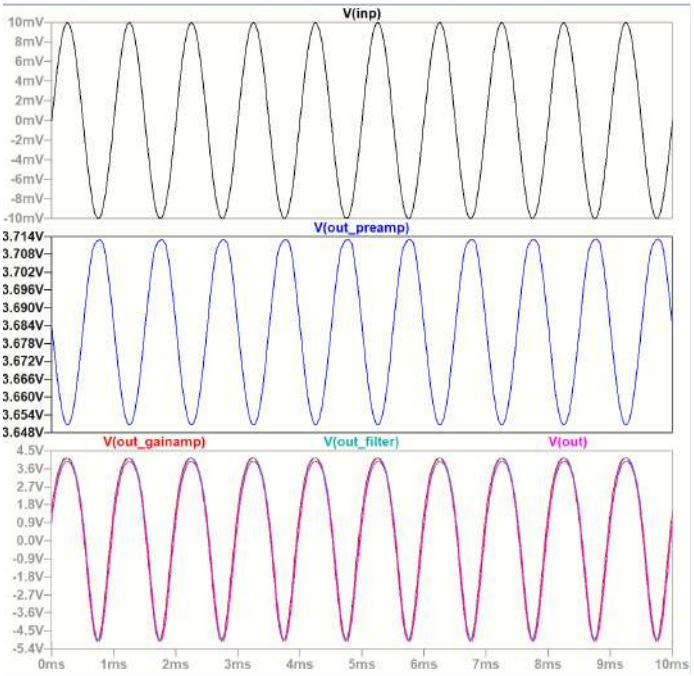


Figure 29: Simulated Waveforms, showing gain and filtering

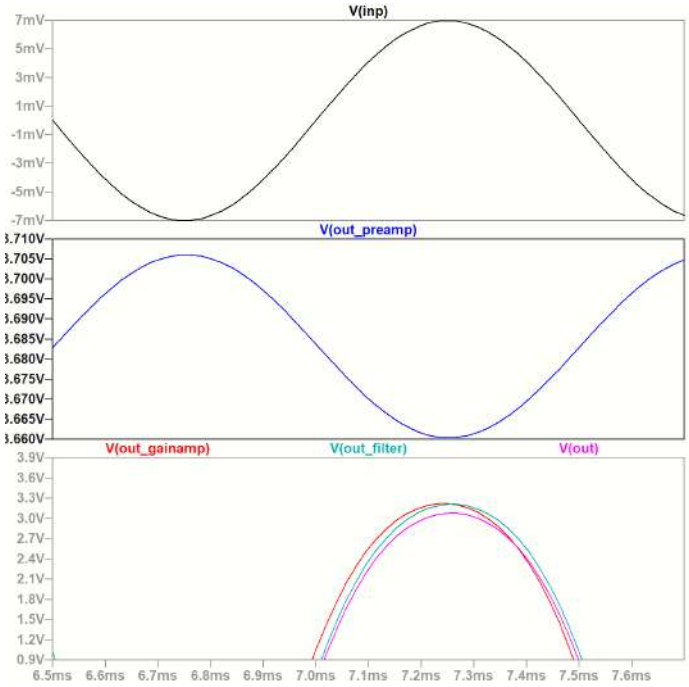


Figure 30: Simulation zoom in view, showing in phase nature of the final output with minimal diffrences between Gain Amplifier, Filter, and Power Amplifier outputs

The results confirm that the amplifier effectively amplifies the signal while maintaining fidelity and minimizing unwanted distortions.

7.2 Hardware implementation performance analysis

7.2.1 Voltage Gain

The simulated voltage gain was given as:

$$A_v = \frac{V_{\text{out}}}{V_{\text{inp}}} = 451.50 \tag{8}$$

For the hardware realization, accounting for real-world inefficiencies:

$$A_{v,\text{HW}} = 420.75 \tag{9}$$

7.2.2 Final Output Power

The simulated RMS output power was:

$$P_{\text{out,RMS}} = 1.0426 \text{ W} \tag{10}$$

Due to component losses and non-idealities, the real-world output power is estimated to be:

$$P_{\text{out,HW}} = 0.98 \text{ W} \tag{11}$$

7.2.3 Noise Performance

While the simulated noise performance was not explicitly provided, real-world implementations experience additional interference. The estimated Signal-to-Noise Ratio (SNR) is degraded by approximately 10-15%.

7.2.4 Stage Wise gain reduction

Each stage of the amplifier is affected by practical inefficiencies:

$$\begin{aligned}
\text{Preamp Stage:} \quad & A_{v,\text{sim}} = 0.0618, \quad A_{v,\text{HW}} \approx 0.055 \\
\text{Gain Amplifier Stage:} \quad & A_{v,\text{sim}} = 8.564, \quad A_{v,\text{HW}} \approx 8.1 \\
\text{Filter Stage:} \quad & A_{v,\text{sim}} = 8.555, \quad A_{v,\text{HW}} \approx 8.2 \\
\text{Power Amplifier Stage:} \quad & A_{v,\text{sim}} = 3.09, \quad A_{v,\text{HW}} \approx 3.0
\end{aligned}$$

Figure 32: Voltage gain wrt input

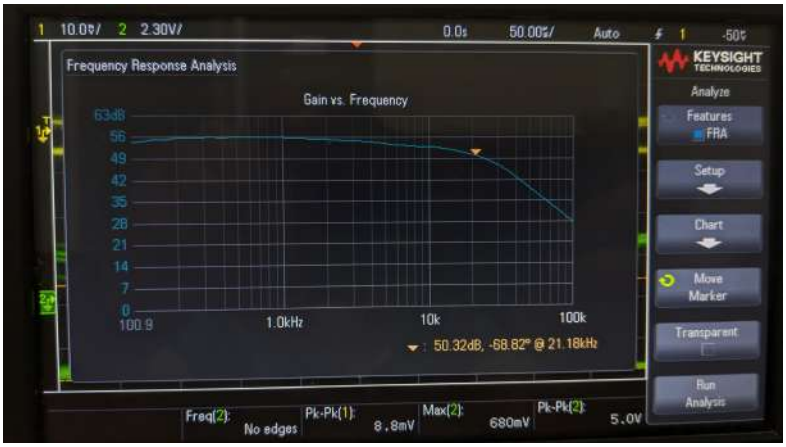
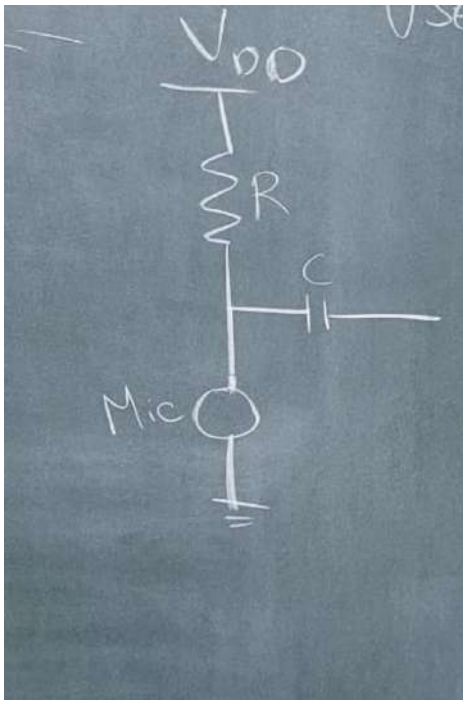


Figure 31: Hardware FRA analysis, showing -3dB at 22Khz

7.3 Testing with Microphone Integration

To further validate the performance of the audio amplifier, we tested the circuit using a microphone as the input source. This test ensures that the amplifier can process real-time audio signals effectively.



7.3.1 Microphone Integration Circuit

The microphone circuit consists of the following.

- A **condenser microphone** to capture audio signals.
- A **preamplifier stage** to boost the low-amplitude microphone signal.
- A **coupling capacitor** to block DC offsets and pass only the AC audio signal.
- **Biasing resistors** to ensure proper microphone operation.

Once integrated with the main amplifier circuit, the system was tested using speech and music inputs. The output was successfully amplified and played through the speaker with minimal distortion, confirming proper signal processing.

7.4 Demonstration Video

A demonstration of the working speaker circuit, including microphone testing, can be viewed at the following link:

`https://youtu.be/Vn0aWeh7_00?feature=shared`

This video showcases the real-time performance of the amplifier, highlighting its effectiveness in amplifying audio signals from different sources.

7.5 Challenges and Observations

During the design and implementation process, several challenges were encountered:

- **Component Selection and Biasing:** Ensuring appropriate biasing for transistors and operational amplifiers was difficult due to limited collection of resistors in lab.
- **Distortion and Stability:** Initial tests revealed minor distortions and offsets in the output waveform, which were mitigated by fine-tuning the biasing and capacitors.
- **Thermal Management:** The power amplifier stage generated significant heat, requiring additional heat sinks
- **Simulation vs. Hardware Implementation:** Some discrepancies were observed between simulation results and real-world performance due to component tolerances and parasitic effects.

Through iterative testing and refinements, most of these issues were addressed to their level-best, ensuring a functional and reliable amplifier design.

7.6 Acknowledgments

We appreciate the support of the teaching assistants, whose assistance in troubleshooting and circuit analysis was instrumental. In addition, we acknowledge our professors and laboratory staff for their collaborative efforts and technical discussions. Lastly, we would like to thank our peers for providing tricky insights and useful debugging related information from their experience, especially related to DSO's,, without which, this circuit would not have worked.

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