AN57821

PSoC® 3, PSoC 4, and PSoC 5LP Mixed-Signal Circuit Board Layout Considerations

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Associated Part Family: All PSoC 3, PSoC 4, and PSoC 5LP parts

Related Application Notes: None

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AN57821 introduces basic PCB layout practices to achieve 12- to 20-bit performance for the PSoC® 3, PSoC 4, and PSoC 5LP families of devices. The design practices covered in this application note are good rules to use in any mixed-signal design for any accuracy.

Contents

1 Introduction

To better understand the problems that may arise when using ADCs with a resolution of 12 bits or above, it is helpful to know how small a voltage an ADC can resolve. An 8-bit ADC with a range of 2 V detects a minimum value of 2 V/256 = 0.008 V or about 8 mV. Although 8 mV seems small, compare it to ADCs with higher resolutions. Table 1 compares ADCs with an input range of ±1 V and resolutions between 8 and 20 bits.

Table 1. ADC Resolution

Range ± 1.024 Volts		
Bits	**Resolution**	**Units**
8	8.000	mV
9	4.000	mV
10	2.000	mV
11	1.000	mV
12	500	µV
13	250	µV

Range ± 1.024 Volts		
Bits	**Resolution**	**Units**
14	125.0	µV
15	62.5	µV
16	31.3	µV
17	15.6	µV
18	7.8	µV
19	3.9	µV
20	2.0	µV

When the resolution is 20 bits, an ADC resolves down to 2 µV. Add a little gain and you can resolve voltages less than a single microvolt. Also, do not forget that a system with a low-resolution ADC and a narrow input range (high ADC gain) may resolve voltages in the microvolt range as well.

Offsets and noise sources below 1 mV, which were insignificant with a low-resolution ADC, are now significant when using a 12- to 20-bit ADC. These errors can easily be overlooked by designers who are not used to sensitive analog circuits. Today's electronics are smaller than ever, and the small circuit board geometries alone are enough to cause many problems.

2 Trace Resistance Does Matter

As PCBs get smaller, trace widths continue to get narrower and closer. Six-mil (0.006-inch) or less trace widths and spaces between traces are common in today's electronics. Even if you specify 6-mil traces, they can easily be over-etched down to 4 or 5 mils.

So, why do you care about traces getting smaller? One problem is that as traces get narrower the trace resistance increases. The standard equation for trace resistance is provided in Equation 1.

$$\text{Resistance} = \text{Resistivity} \times \frac{Length}{(Width \times Thickness)}$$

Equation 1

Where,

Resistivity for copper is about 6.787×10^{-7} Ω/inch.

Thickness of copper for a 1-oz copper PCB equals 1.378 mils.

A one-inch trace 8 mils wide, on a 1-oz copper PCB is about 0.062 Ω. Table 2 shows the calculated resistance values for several combinations of trace lengths and widths.

Table 2. Trace Resistance

Trace Resistance in Ω				
Width (mils)	**Trace Length (inches)**			
	0.1”	**0.5”**	**1”**	**2”**
15	0.0033	0.0164	0.0328	0.0657
10	0.0049	0.0246	0.0493	0.0985
8	0.0062	0.0308	0.0616	0.1231
6	0.0082	0.0410	0.0821	0.1642
4	0.0123	0.0616	0.1231	0.2463

As shown in Table 2, all combinations are well under an ohm. That does not sound too bad, but it all depends on where it is with respect to the circuit. If it is the trace to the input of a high-impedance amplifier, it may not matter, but in other cases, you may not be so lucky. Now take this same table and pass a 5-mA current through each trace combination. Although 5 mA is not much current and trace resistances less than an ohm seem small, the combined offsets are significant when using a high-resolution ADC, as shown in Table 3.

Table 3. Trace Voltage Offset

Offset Due to 5 mA Current (microvolts)				
Width (mils)	Trace Length (inches)			
	0.1”	0.5”	1”	2”
15	16.42	82.10	164.20	328.40
10	24.63	123.13	246.25	492.50
8	30.79	153.93	307.85	615.70
6	41.05	205.23	410.45	820.90
4	61.57	307.83	615.65	1231.30

In this table, if 5 mA flows through a 2-inch-long trace that is 6 mils wide, the voltage drop is about 820 µV or 0.82 mV. In Table 1, note that this voltage drop does not become significant until your system is using a 12-bit or higher resolution ADC. The cells shaded in green are conditions that affect a 16-bit ADC by at least half of the least significant bit or more. The cells shaded in yellow are conditions that can cause the same error in a 12-bit or higher ADC. This assumes that both the 12- and 16-bit ADC have an input range of 2 volts (+/– 1 volt).

An example application where this magnitude of offset causes significant error is measuring temperature with a thermocouple. With a K-type thermocouple, the output is about 40 µV per degree centigrade. The 410-µV offset equates to an error in excess of 10 °C. If the same trace is over-etched to 4 mils, the error is 50 percent higher. From this example, you can see how important it is to evaluate every PCB trace in your signal path. Although at first this does not sound too bad for a 12-bit ADC, if you add a gain of 16 in front of the ADC, you have the equivalent voltage resolution of a 16-bit ADC.

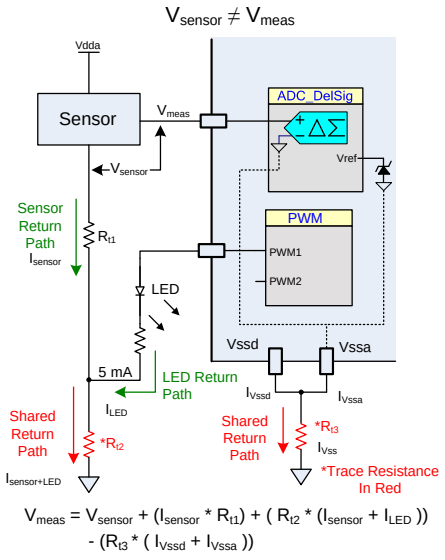
3 Shared Return Paths

When designing a circuit board with mixed signals or high-precision ADCs, you should know where current is flowing in the PCB. Trace currents of just a few milliamperes can be enough to cause significant problems.

Trace resistance usually causes a problem when a sensitive analog signal's return path is shared by a digital or high-current analog device. In these cases, high current does not mean amperes, but instead milliamperes. In the previous example, the thermocouple shared the same return path as a 5-mA load. If you reduce that load to 0.5 mA, the error remains 1 °C. Therefore, even currents in the hundreds of microamperes are significant.

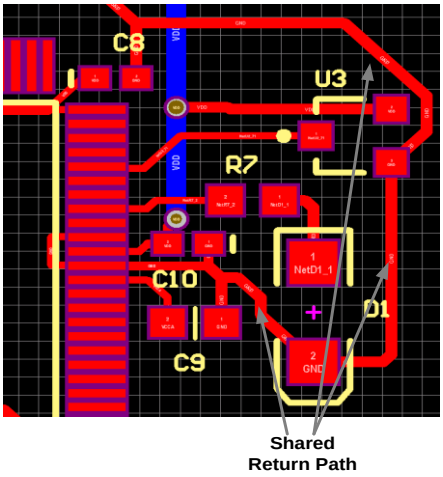
Figure 1 shows an example where return current paths are shared between the analog and digital grounds, and between a sensor and an LED. Both these shared paths can cause problems that may appear as system offsets or gain errors.

Figure 1. Resistance in Signal Return Path



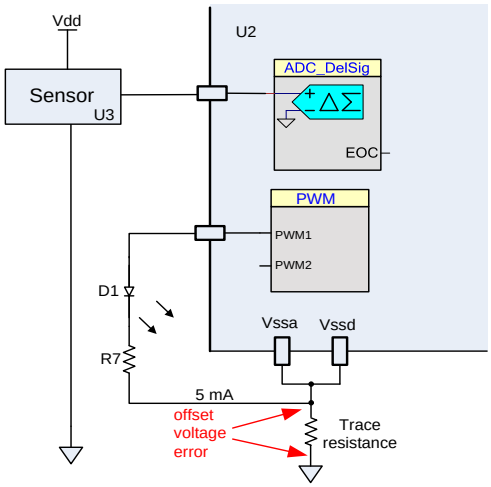
When the ADC in this example measures the output of the sensor, it also measures the voltage across the trace resistance. Depending on the length of the trace between the common ground point and the place where the sensor and LED currents combine, a significant voltage offset error may occur. How significant depends on the desired accuracy of the system, the voltage gain of the sensor, and the magnitude of the offset error voltage. An example of the PCB layout is shown in Figure 2.

Figure 2. Example Layout with Shared Return Paths



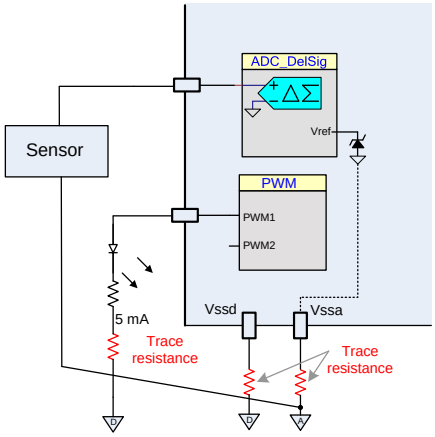
The analog ground (V_{SSA}) is as important as any of the signals you are measuring. The trace between the PSoC V_{SSA} pin and the system ground must be as short and low impedance as possible. Sharing this path with any component that uses even a few hundred microamperes can cause problems when measuring sub-millivolt signals. An offset can translate into a measurement offset when using single-ended measurements. In Figure 3, the LED's current flows in the same path back to the supply, but the sensor has its own path. The internal bandgap reference is also connected to V_{SSA}. Any voltage induced by sharing the return path with the LED causes the ADC's reference to fluctuate by the I*R drop. This offset between the reference and V_{SSA} causes an ADC gain error.

Figure 3. Current in Analog Ground Path



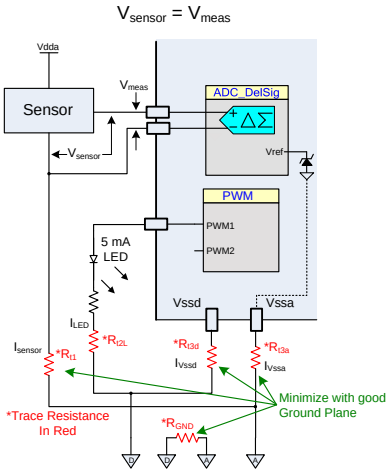
By providing separate ground paths for the digital ground (V_{SSD}), analog ground (V_{SSA}), sensor, and LED, there are no shared return paths (Figure 4). The sensor, ADC, and reference are at the same analog ground reference, so changing current in the LED has little or no effect on the sensor's output. Also note in the figure that the sensor and V_{SSA} connect to the analog ground at the same location. This can physically be the same point or to a very low impedance plane.

Figure 4. Good Ground Connections



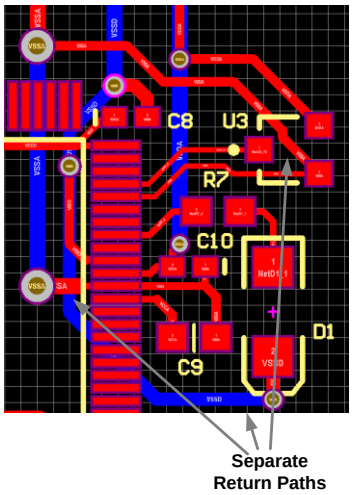
Using a differential ADC connection to the sensor helps eliminate common mode voltage offsets caused by sharing a sensor return with a high current path (see Figure 1). A common voltage is an offset common to both the sensor V_{SS} and the sensor output. However, a differential connection to the sensor does not help errors caused by shared ground paths with V_{SSA} (Figure 3). See Figure 5.

Figure 5. Differential ADC and Separate Return Paths



An example of an improved routing that maintains separate return paths, separate analog and digital supplies, and a differential connection to the sensor is shown in Figure 6.

Figure 6. Example Layout with Separate Return Paths



3.1 Beware of the Hidden Killer

When sharing return paths with sensors or the V_{SSA} pin with a modulated load, such as a LED driven by a PWM, errors may not always be apparent at first. If the load is modulated in perfect sync with the ADC, the errors induced may be large or insignificant. If synchronization does not cause measurable errors on the bench, then no problem may be seen in the initial development and testing. The problem is that with a change in either the ADC sample rate or the PWM frequency in this case, the error or noise can change significantly. This can be hard to test because in many applications, the change in the load modulation can vary due to environmental or software changes. So a board design that appears to be working at one time may fail at others. This is why it is imperative to follow good design rules even if a design appears to be working properly.

4 Routing Analog and Digital Signals

Ideally, analog and digital signals should be kept on opposite sides of the board, but this is usually impractical. Many designs require both analog and digital signals in the same area. Unfortunately, running relatively high-impedance analog signals in the same area as digital signals can cause unwanted crosstalk, which can add excessive noise to the analog signal.

4.1 What is Crosstalk?

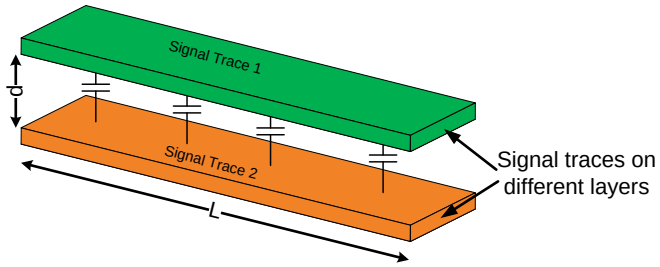
Crosstalk occurs when one signal affects another signal without being directly connected. This is most common when a digital signal with fast rise and fall times affects an analog signal with much high impedance. Digital signals are not immune to crosstalk either. High-speed digital signals can easily affect other digital signals. Crosstalk between signals is usually one of three types: conductive, capacitive, or inductive. In all cases, increasing the distance between signals and decreasing the parallel length between signals will help to reduce the problem.

Conductive crosstalk is usually not a problem and is an issue only when signals have very high impedance, such as more than 10 MΩ. It usually occurs when foreign materials such as dirt, oil, salt, or other liquids contaminate a PCB and cause the PCB material between traces to become more conductive. This decrease in resistance may cause enough crosstalk to adversely affect circuit operation. A solder mask can protect the PCB in some cases, but there are always areas, such as where components are attached to the PCB, that are exposed. Measures should be taken to isolate the PCB from these materials if they are found in the environment where the product is used. If it is impossible to insulate the PCB from foreign materials, a conformal coating can be applied to the PCB, but with added cost.

Capacitive coupling may occur when one trace is directly above the other on a different layer. A capacitor is formed between the copper traces. The more the overlap of the copper between these traces, the higher the capacitance. Decreasing the overlapping area between the signals will decrease the capacitance and therefore decrease the coupling. In some situations, especially with only two-layer boards, it may be impossible to eliminate instances where a sensitive analog signal crosses over a fast digital signal. In these cases, the signals should cross at 90° angles to minimize the capacitance formed between these signals.

If you are using multilayer boards with more than two layers, make sure a power plane is between the two signals where they intersect to minimize coupling. Notice in Figure 7 that a capacitor is formed between the two traces, which is directly proportional to the overlapping area.

Figure 7. Capacitive Coupling of Parallel Traces



If a multilayer board is used, make sure the analog and digital traces intersect at a 90° angle. This way, the overlapping area is much less and therefore creates less capacitive coupling between the signals. See Figure 8 for an example.

Figure 8. Capacitive Coupling of Traces Running Perpendicular

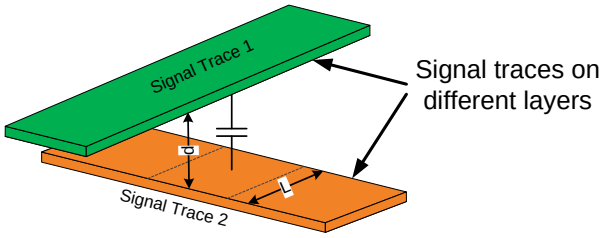
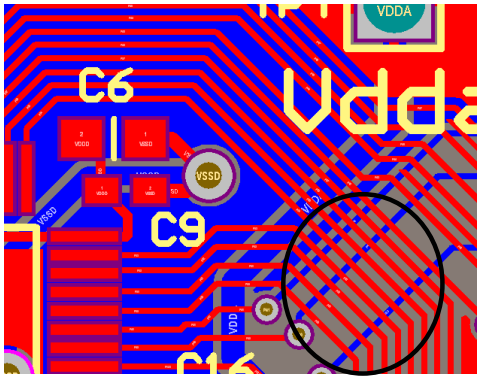


Figure 9 shows an example PCB layout where the analog traces (red) must cross over the digital (blue) traces. Notice the 90° angles between the analog and digital traces.

Figure 9. Digital Traces Cross Analog Traces at 90°

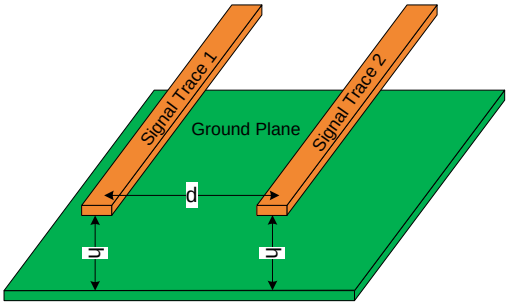


Traces that run next to each other on the same or a near layer may be coupled magnetically. This is referred to as inductive coupling. Inductive coupling is a function of three mechanical features: the separation between traces, the distance that the two traces are parallel, and the distance between the trace and the nearest power plane. The distance between the signals and between the signals and the ground plane are the biggest contributors, as shown in the simplified Equation 2 and Figure 10.

Equation 2

$$Crosstalk \cong \frac{1}{1+(\frac{d}{h^2})}$$

Figure 10. Spacing for Inductive Coupling

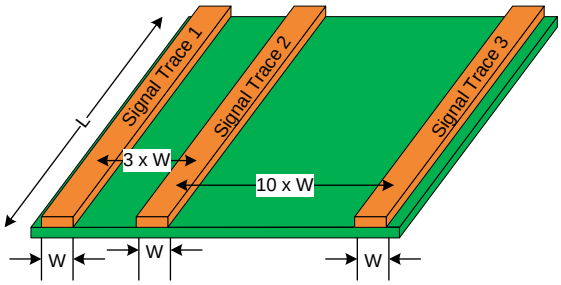


As you can see, the height the trace is above the ground plane is a huge factor. By reducing this distance, the crosstalk is reduced by the square of the height. If you need to run digital and analog traces near each other, keeping them close to the ground plane may be the best option to reduce crosstalk.

4.2 3-W Rule

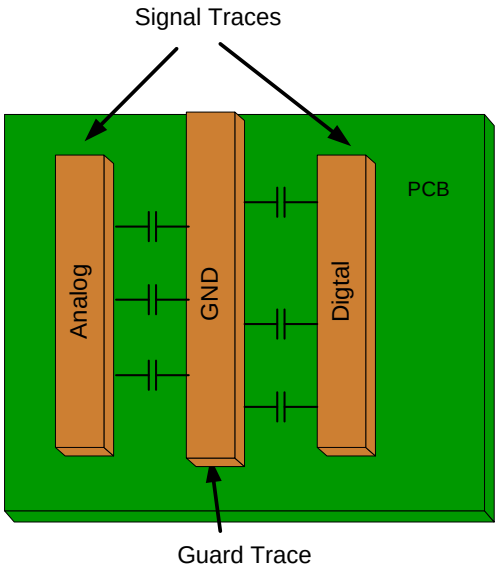
The 3-W rule states that the separation between logic traces (center to center) should be three times the width of the traces. For example, if the traces on a PCB are 0.008 inches wide, the distance between the trace's centers would be 0.024 inches (0.008 inches x 3), and the distance between trace edges would be 0.016 inches (0.008 inches x 2). This puts each trace outside the 70 percent magnetic flux boundary of the other trace. To be outside the 98 percent flux boundary, the spacing between the traces needs to be 10 times the width of the traces. Of course, all of this is dependent on the impedance of the traces and the rise time of the signals. See Figure 11.

Figure 11. Example of 3-W Rule



Another option to reduce coupling between signals that must run near each other and on the same side of the board is to use a guard trace connected to ground between the signals. This helps to reduce the capacitive coupling between the signals. See Figure 12.

Figure 12. Using Guard Traces



In multilayer boards, some layers are closer to some layers than others. For example, with a common 4-layer 0.062-inch-thick board, layers 1 and 2 are closer together than layers 2 and 3. When routing analog and digital signals in the same area, separate the traces on non-adjacent layers to ensure maximum separation.

5 Multiple Power Domains

Sensitive analog systems make it desirable to maintain separate analog and digital power supplies. The PSoC 3, PSoC 4, and PSoC 5LP families provide separate power and ground pins for the analog and digital blocks. The PSoC 3 and PSoC 5LP GPIOs are also divided into four groups, but this is mainly to provide multiple logic levels to external components. A summary of the power supply connections follows.

- V_{SSD} – Ground for all digital logic and I/O pins.
- V_{DDD} – Supply for all digital peripherals and digital core regulator. V_{DDD} must be less than or equal to V_{DDA}.
- V_{SSA} – Ground for all analog peripherals.
- V_{DDA} – Supply for all analog peripherals and analog core regulator. V_{DDA} must be the highest voltage present on the device. All other supply pins must be less than or equal to V_{DDA}.
- V_{CCD} – Output of digital core regulator and input to digital core. Requires a 1-µF cap to V_{SSD}. Regulator output not for external use.
- V_{CCA} – (PSoC 3 and 5LP only) Output of analog core regulator and input to analog core. Requires a 1-µF cap to V_{SSA}. Regulator output not for external use.
- V_{DDIO} – Supplies for I/O pins. For PSoC 3 and 5LP, there are four V_{DDIO} pins. The GPIOs are grouped into four groups, each with its own power pin. V_{DDIO} must be less than or equal to V_{DDA}.

Depending on the product family and part number, a PSoC device may have all or a subset of these pins. For details, refer to the datasheet of the part you are using.

The use of separate external analog and digital regulators is always a good idea. If the cost of an additional regulator is prohibitive and the digital section of your design does not contain high-speed or high-current switching, it is possible to use a single regulator. One important note is always to wire your design as if you have separate regulators. Separate both power and ground signals for the analog (V_{DDA}, V_{SSA}) and digital supplies (V_{DDD}, V_{SSD}). Make the connection between these two supplies (analog and digital) as close to the power supply source as possible. Usually the output impedance of the power supply is low, and with such a connection, the digital supply has less of an effect on the analog supply.

The PSoC 4 parts that are available in the 28-pin SSOP package have the V_{SSD} and V_{SSA} supply pins combined into a single V_{SS} pin to save pins. Also, the V_{DDA} and V_{DDD} pins are combined into a single V_{DD} pin. This 28-pin SSOP package should be avoided when the maximum analog performance is required when several GPIO pins are used to drive fast low-impedance loads.

6 Ground Planes

Ground planes are always beneficial in a mixed-signal design, but additional layers may be expensive for a given design. Even with two-layer boards, it is possible to provide partial planes under sensitive analog sections of the design. Whether you use ground planes or not, make sure the return paths are as direct to the power supply as possible. Remember, ground planes may not improve your design if the path to the supply is not low impedance, or the plane is too fragmented. On two-sided boards, do not rely only on using fill; it can lead to narrow, high-resistance paths that are not obvious without careful inspection. Route the ground with traces and supplement with fill.

If care is taken when selecting pins, the board layout can be much easier and enable partial analog and digital power planes. Figure 13 shows how the analog and digital sections of the chip are placed in the PSoC 3 and PSoC 5LP device with respect to the I/O ports.

Figure 13. PSoC 3/PSoC 5LP Analog/Digital Layout

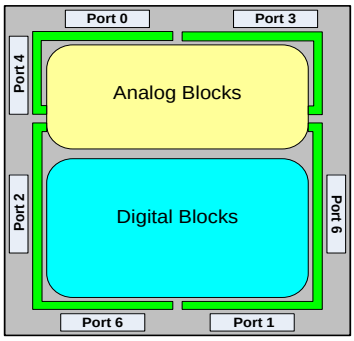
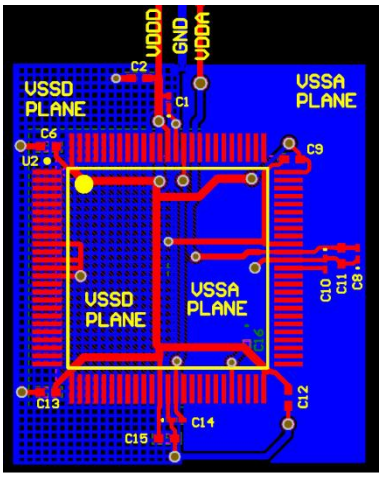


Figure 14 is an example of a two-layer board layout. The PSoC device is rotated 90° clockwise with respect to the image in Figure 13. The blue is the bottom layer, and the red is the top layer. Notice that there is adequate room to route the signals away from the PSoC device on the top layer even with all power supply pins connected and good power grounds on the bottom layer. The V_{SSD} plan was hatched intentionally so that it is easy to distinguish between the V_{SSD} and V_{SSA} power planes. Normally, it is recommended to make your power planes solid, unless there is a special case, such as CapSense® buttons and controls.

If separate analog and digital ground planes can be used in your design, they should be connected at a single point in most cases. This single point should be between the power supply source and the PSoC device itself.

With a single regulator, it is possible to use a single ground plane, but only if the analog and digital components are well isolated from one another.

Figure 14. Example PSoC 3 and PSoC 5LP Two-Layer Board Layout



See Appendix A for example layouts for QFN, and SSOP packages.

7 Bypass Capacitors

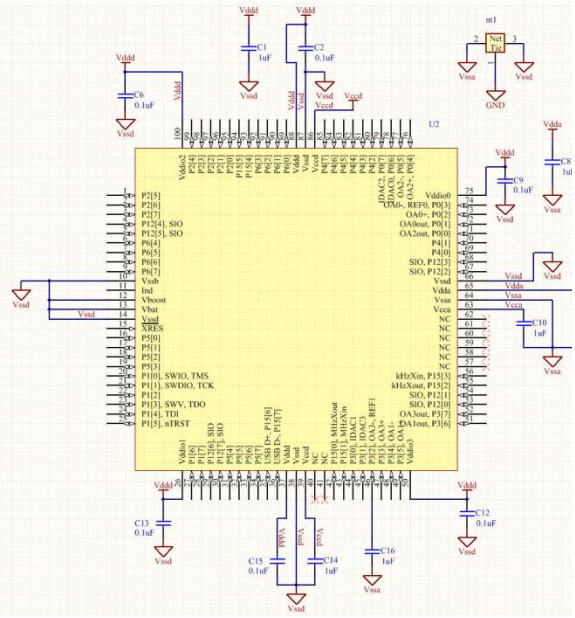
7.1 PSoC 3 and PSoC 5LP

As mentioned previously, there are several power domains with the PSoC 3 and PSoC 5LP parts. Each of these domains has individual bypass capacitor requirements. Table 4 summarizes these requirements, and Figure 15 shows an example schematic with the capacitors in place.

Table 4. PSoC 3 and PSoC 5LP Bypass Capacitor Connection Summary

Power Supply	Bypass Capacitors
$V_{DDD} – V_{SSD}$	0.1-µF ceramic capacitor at each pin plus a 4.7-µF to 10-µF bulk capacitor (C1, C2, C15).
$V_{DDA} – V_{SSA}$	0.1-µF ceramic capacitor at pin (C11). Additional 1-µF to 10-µF bulk capacitor (C8) if more than an inch from power supply.
V_{DDIO} 0,1,2,3 – V_{SSD}	0.1-µF ceramic capacitor at each V_{DDIO} pin. Additional 1-µF bulk capacitor if several pins are switching 5 to 10 mA. (C9, C13, C6, C12)
$V_{CCA} – V_{SSA}$	1-µF capacitor (C9) at the V_{SSA} pin.
$V_{CCD} – V_{SSD}$	1-µF ceramic capacitor (C14) at one of the two V_{CCD} pins. The V_{CCD} pins should be connected together.
$V_{REF} – V_{SSA}$ (optional)	The internal bandgap may be bypassed at pin P3[2] or P0[3] with a 1-µF to 10-µF capacitor (C16). For PSoC 5LP, reference bypass capacitors should be used for each of the SAR ADCs if operating above 100 ksps. A 1-µF to 10-µF capacitor should be placed on pins P0[2] and/or P0[4], depending on which SAR ADCs are being used.

Figure 15. Example PSoC 3 and PSoC 5LP Schematic of Power Connections



7.2 PSoC 4

Since the PSoC 4 family is not intended to achieve the accuracy and resolution possible with both PSoC 3 and PSoC 5, board layout is not as critical either. That said, it is still always important to adhere to good board layout practices. In the example PSoC 4200 series device shown in Figure 16, notice that there are two analog sensitive areas near Port 1 and Port 2. Port 2 is the preferred port to route signals directly to the SAR ADC, although an AMUXBUS can be used to route all signals to the SAR ADC, but with a higher resistive path. Port 1 contains two general-purpose opamps, which can be used to buffer input signals to the ADC or to operate totally independent of the SAR ADC. If these two ports are used for analog signaling, it is a good practice to keep digital signals routed away from this area.

Figure 16. PSoC 4200 Block Layout Diagram

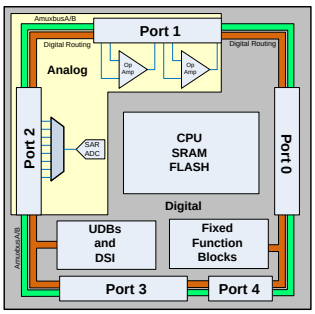


Figure 17 shows an example schematic for the PSoC 4200 series TQFP 44-pin package. Notice that there are much fewer power supply pins than are used for PSoC 3 and PSoC 5LP. There are several reasons for this, including that it is a Table 5 summarizes the PSoC 4 power connections and the bypass capacitors for each pin.

Figure 18 shows an example layout for PSoC 4 in the 44-pin TQFP package. The V_{SSD} digital ground plane is shown hatched so it is easy to tell the difference between the two analog and digital ground planes. This is just one example of the many ways in which to lay out a two-layer PCB. Appendix A: Layout Examples gives sample schematics and PCB layouts for the QFN and SSOP packages as well.

significantly smaller device and it does not contain a high-performance 16- to 20-bit Delta-Sigma ADC as do the PSoC 3 and PSoC 5LP devices.

Figure 17. PSoC 4 TQFP 44 Example Schematic

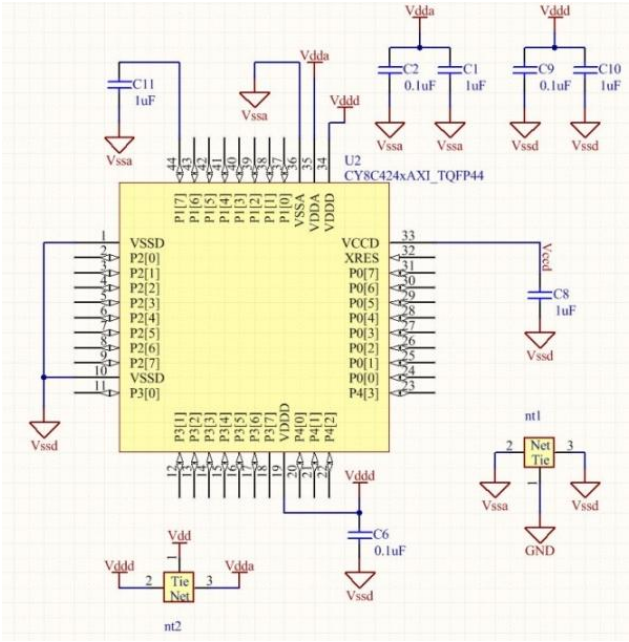
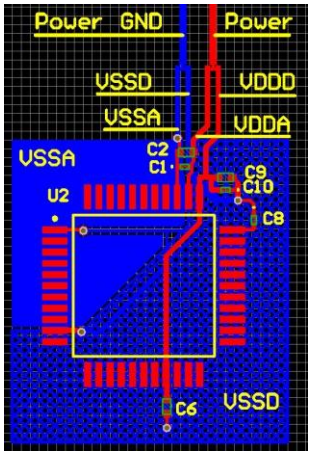


Table 5. PSoC 4 Bypass Capacitor Connection Summary

Power Supply	Bypass Capacitors
$V_{DDD} – V_{SSD}$	0.1-µF ceramic capacitor at each pin plus a 1-µF to 10-µF bulk capacitor (C9, C10).
$V_{DDA} – V_{SSA}$	0.1-µF ceramic capacitor at pin (C2). Additional 1-µF to 10-µF bulk capacitor (C1).
$V_{CCD} – V_{SSD}$	1-µF ceramic capacitor at the V_{CCD} pin (C8)
$V_{REF} – V_{SSA}$ (optional)	The internal bandgap may be bypassed with a 1-µF to 10-µF capacitor at P1[7]. (C11)
$V_{DDIO} – V_{SSA}$ (V_{DDIO} is not present in all PSoC 4 devices)	0.1-µF ceramic capacitor and an additional 1-µF to 10-µF bulk capacitor (not shown in the image).
$V_{DD} – V_{SS}$ (these pins are not present in all PSoC 4 devices)	0.1-µF ceramic capacitor and an additional 1-µF to 10-µF bulk capacitor (not shown in the image).

Figure 18. PSoC 4 TQFP 44-Pin Layout



7.3 Capacitor Selection

There are two types of capacitors used for power supply stability: bypass and bulk. Bulk capacitors are sometimes referred to as reservoir capacitors as well. The bypass capacitors must be placed near the power supply pins of the component. Bypass capacitors help to eliminate high-frequency noise and supply current for short transients. These capacitors are usually between 0.001 µF and 0.1 µF. Capacitors with a dielectric of NPO, X5R, and X7R make excellent bypass capacitors and are available in values from hundreds of picofarads to several microfarads.

The reservoir capacitors are usually placed near the regulators. They are also spread around the board if it is more than a few square inches in size and contains several active components. The capacitors are used to supply power for longer periods and filter low-frequency noise. Reservoir capacitors range in size between 1 µF and 100 µF or even larger for boards with high current signals or power supplies. X5R, tantalum, and some surface mount electrolytic capacitors work well for this purpose.

Often the 0.01-µF or 0.1-µF capacitor is sufficient for a bypass capacitor. For reservoir capacitors, it is recommended to do some simple calculations to make sure you have the optimum value. Too big and you are spending more than you need. Too little and your power supply ripple may be excessive and cause noise. Start with the equation:

$$I = C * \frac{dV}{dT}$$

Solving for C:

$$C = I * \frac{dt}{dV}$$

dt = Clock or highest frequency component (fclk * π)
I = Average current
dV = Acceptable ripple voltage

$$C = \frac{I_{ave}}{(f_{clk} * \pi * dV)}$$

8 All Capacitors Are Not Equal

When selecting a capacitor for any application, even a simple bypass cap, it is very important to look at its specifications. The voltage and temperature coefficients are two of the most ignored capacitor specifications, but they can greatly affect the device capacitance under normal operating conditions.

As devices become increasingly smaller, tradeoffs are made between performance and size. A capacitor that is rated at 1 µF and a max voltage of 6.3 may be less than 0.1 µF at 5 volts. So you really do need to pay attention to the voltage coefficient. Also, do not assume that the coefficient is the same for an entire family of parts. The voltage and temperature coefficient can vary greatly between packages. A 0805 package may have a better voltage coefficient than a 0603 package, or the other way around. So read the datasheet. If you cannot get temperature and voltage coefficients for a capacitor, consider using a capacitor from a different manufacturer.

9 Mixed-Signal PCB Rules Summary

The following is a list of rules to keep in mind when designing mixed-signal boards:

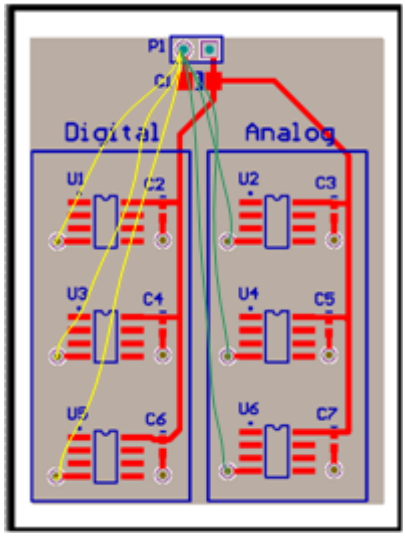
1. Consider separate analog and digital supplies.
2. Understand all return paths.
3. Use four-layer boards with power planes if possible, although they are not always affordable.
4. Do not run analog signals parallel to clocks or fast digital signals.
5. If analog and digital signals must cross, make the intersection at 90^{o} to keep the coupling capacitance to a minimum.
6. Use power planes in similar areas. For example, only run analog signals over analog power planes.
7. Keep bypass capacitors as close to ICs as possible. Also make sure bypass connections to power signals are low impedance.
8. Separate analog and digital signals and components on the board, if possible. Designate “analog” and “digital” areas of the PCB.
9. Avoid long traces into a high-impedance input. These act as antennas.
10. Keep power traces as wide (low impedance) as possible.
11. Keep analog signals close to the ground plane to minimize inductive crosstalk.
12. Use large or multiple vias when connecting power signals between planes to reduce impedance.
13. Minimize the digital rise and fall times of digital signals.
14. Use guard traces to isolate analog and digital signals.

10 PCB Layout and Auto Routing Tools

PCB layout tools have come a long way in the last 20 years. Many of these tools allow signals to be grouped and create different rules for trace widths and distance between traces. These rules keep you from inadvertently making mistakes. Auto routers have also become more powerful, and many common tools follow the same rules as when you route by hand. A skilled PCB layout designer can use these rules to enhance the quality of the auto router. Although these tools are very powerful, be careful how they route analog and digital signals. You may find it worthwhile to hand route the sensitive part of your board and then let the auto router complete the least critical section of the board. Either way, make sure you review the final routing.

Placing the parts in optimal locations can also greatly aid in either hand routing or auto routing. After the parts placement and board layout is complete, a simple test can be used to validate if shared return paths could cause a problem. Print out your board layout and draw the most direct path between your power supply and each of the components. Use one color for analog parts and another for digital parts. If the different colors cross, you may want to re-evaluate your design. See Figure 19.

Figure 19. Draw Return Paths on PCB Layout



11 Summary

The design tips discussed in this application note help you grasp the following concepts:

- Understand your signal return path and do not share analog and digital return paths, if possible.
- Trace resistance does matter, and it is as simple as Ohms law to determine just how much.
- There is always coupling between any two adjacent traces, so keep digital signals away from analog signals.

About the Author

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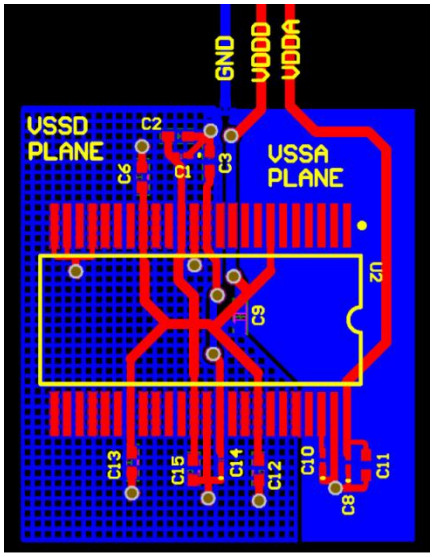
Background:	Mark Hastings graduated from Washington State University in 1984. For most of the last 25 years, he has been involved in embedded and mixed-signal designs. Most of his free time is spent hiking and climbing in the North Cascades of Washington.

A Appendix A: Layout Examples

A.1 PSoC 3 and PSoC 5LP SSOP, QFN, and TFQP Packages

Figure 20. Example Layout for 48-Pin SSOP Package



For more examples including schematic, layout and gerber files, see CY8CKIT-030 and CY8CKIT-050 development kit web pages. Also refer to PSoC 3 and PSoC 5LP CAD resources web pages.

Figure 21. PSoC 3/5 Schematic for 48-Pin SSOP Package

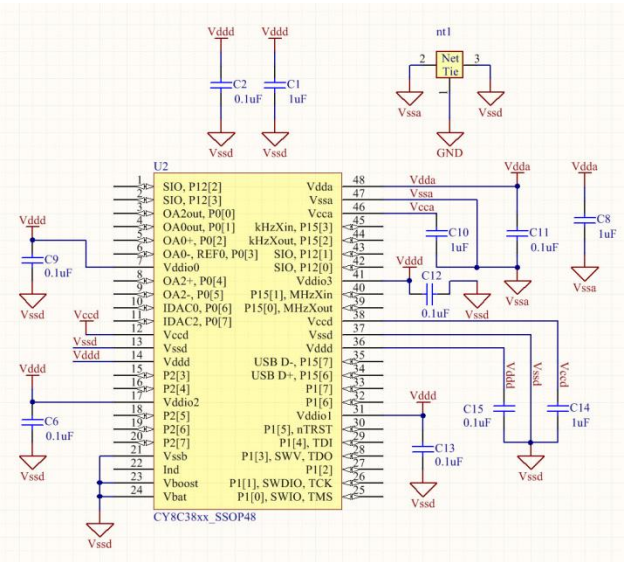


Figure 22. Example PSoC 3/5 Layout for 68-Pin QFN Package

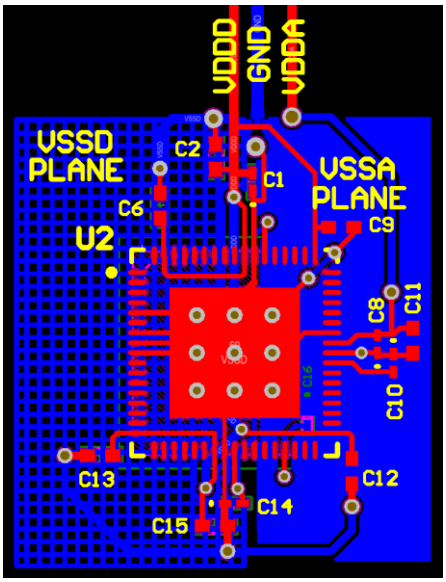
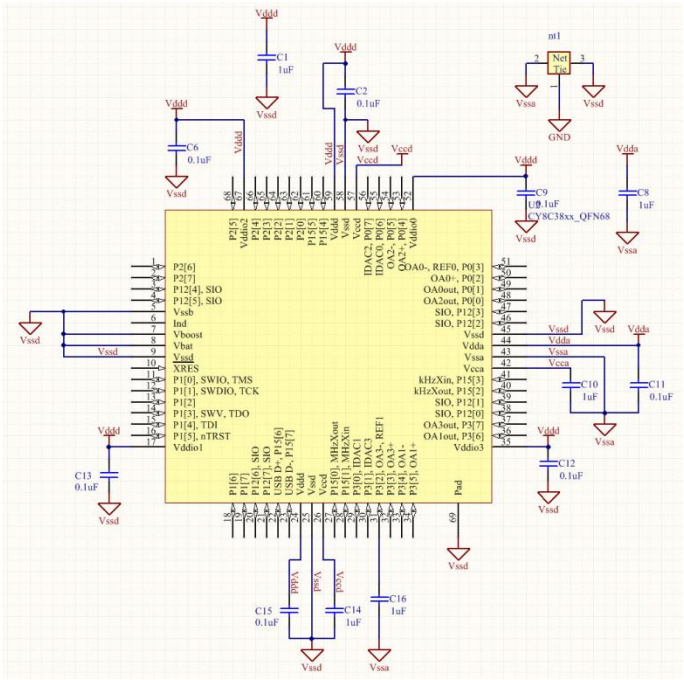


Figure 23. Schematic for 68-Pin QFN Package



A.2 PSoC 4 QFN and SSOP Packages

Figure 24. Example Layout for PSoC 4 QFN 40-Pin Package

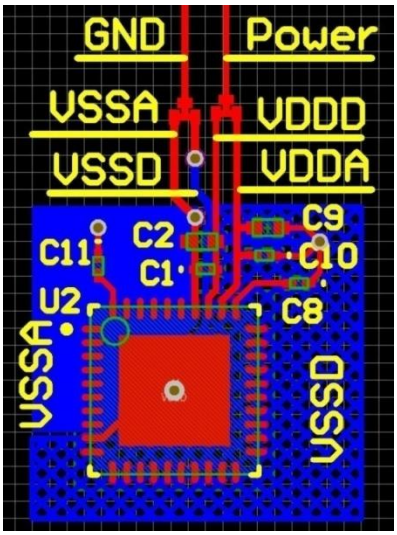


Figure 25. Example Schematic for PSoC 4 QFN 40-Pin Package

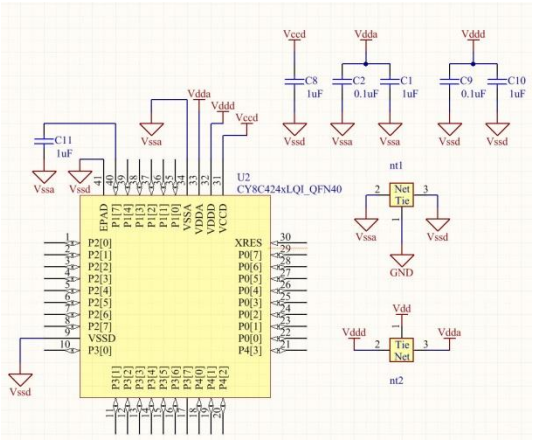


Figure 26. Example Layout for PSoC 4 SSOP 28-Pin Package

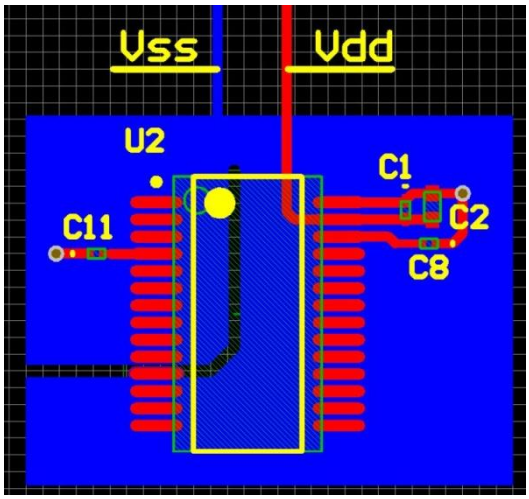
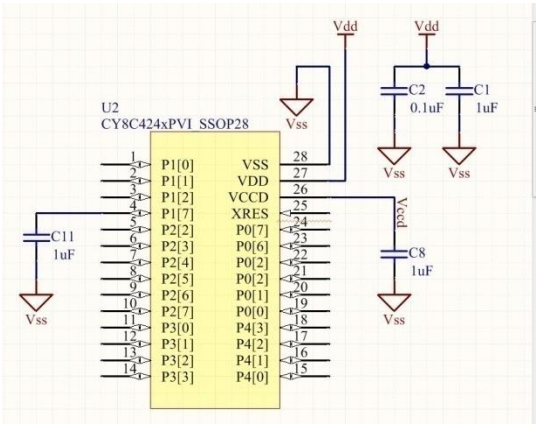


Figure 27. Example Schematic for PSoC 4 SSOP 28-Pin Package



For more examples including schematic, layout and gerber files, see CY8CKIT-044, CY8CKIT-042, and CY8CKIT-040 development kit web pages. Also, refer to PSoC 4 CAD resources web page.

Document History

Document Title: AN57821 - PSoC® 3, PSoC 4, and PSoC 5LP Mixed-Signal Circuit Board Layout Considerations

Document Number: 001-57821

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2818833	MEH	12/01/2009	New application note
*A	2896385	MEH	03/19/2010	Changed connection to Vboost from V_{DDD} to V_{SSD}
*B	2991511	SRIH	07/22/2010	Fixed branding discrepancies
*C	3095205	MEH	11/25/2010	Changed the title, updated abstract, and fixed a few minor typos.
*D	3460049	MEH	12/09/2011	Changed Title Updated Figures 1, 3, 4, and 5, and Tables 2 and 3 Several minor changes throughout document Changed abstract Updated template
*E	3656888	MEH	6/26/2012	Updated **Error! Not a valid result for table.**. Updated Ground Planes**Error! Not a valid result for table.**. Added Appendix A. Updated in new template.
*F	3719890	MEH	8/23/2012	Updated capacitor designators to match the schematic changes in rev *E.
*G	3811577	MEH	11/15/2012	Updated Associated Part Family as “All PSoC 3 and PSoC 5LP parts”. Replaced PSoC 5 with PSoC 5LP in all instances across the document.
*H	3940231	MEH	4/08/2013	Fixed wiring error with SSOP 48-pin package. Added PSoC 4 information.
*I	4494203	MEH	9/05/2014	Added the section "All Capacitors Are Not Equal”.**Error! Not a valid result for table.**
*J	4573117	MEH	11/18/2014	Sunset Update
*K	4776263	NIDH	06/03/2015	Updated the following for PSoC 4-M series: Updated Multiple Power Domains. Updated Table 5. Added links to kit web pages for additional schematic/layout details. Updated the document as per new template.
*L	5687787	AESATMP7	04/18/2017	Updated Cypress Logo and Copyright.

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