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```
1   ## SRIDHAR (212223060271)
2   # Ex No: 01 - Design & Implementation of CMOS Inverter Design Using Cadence EDA Tools
3
4   ## Aim
5   The aim is to create and simulate a CMOS inverter circuit with Cadence EDA tools, assess
    its key electrical properties, and explore foundational CMOS principles, including the
    design workflow and simulation approaches.
6
7   ## Tools Required
8
9   ### Cadence EDA Suite
10  - **Virtuoso Schematic Editor** (for circuit design)
11  - **Spectre Simulator** (for circuit simulation)
12
13  ### Process Design Kit (PDK)
14  - CMOS technology library (e.g., 180nm, 45nm node)
15
16  ### Computer System
```

Use `Control + Shift + m` to toggle the `tab` key moving focus. Alternatively, use `esc` then `tab` to move to the next interactive element on the page.

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```
21          Open the Cadence Virtuoso tool and set up the working library.
22          Create a new schematic cell view for the CMOS Inverter design.
23  ### 2. Schematic Design:
24      Select the NMOS and PMOS transistors from the library.
25
```

    Connect the NMOS transistor with its source terminal to GND and its drain terminal to the output node.
    Connect the PMOS transistor with its source terminal to VDD and its drain terminal to the same output node as NMOS.
    Join the gate terminals of both transistors to form the input node.
    Connect input voltage sources Vdc and Vpulse

3. Simulation:

    Check the Design for Errors and proceed for Simulation
    Launch the Analog Design Environment (ADE).
    Configure transient analysis for time-domain response.
    Set the simulation parameters such as voltage sweep range and step size.
    Use Spectre simulator to perform transient and DC analyses.

4. Waveform Analysis:

    Observe the output voltage waveform concerning the input voltage.