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School of Electronics Engineering (SENSE)

VIT CHENNAI

BECE303P

VLSI SYSTEMS DESIGN

Hackathon Report

WINTER 2024 – 25

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INTRODUCTION

In the realm of Very Large Scale Integration (VLSI) design, optimizing the performance of fundamental arithmetic circuits is crucial for developing high-speed and energy-efficient digital systems. Among these fundamental circuits, the full adder plays a vital role, serving as a core component in arithmetic units such as multipliers and Arithmetic Logic Units (ALUs). The propagation delay of a full adder directly influences the overall speed and efficiency of these larger systems, making its design and optimization a key area of interest.

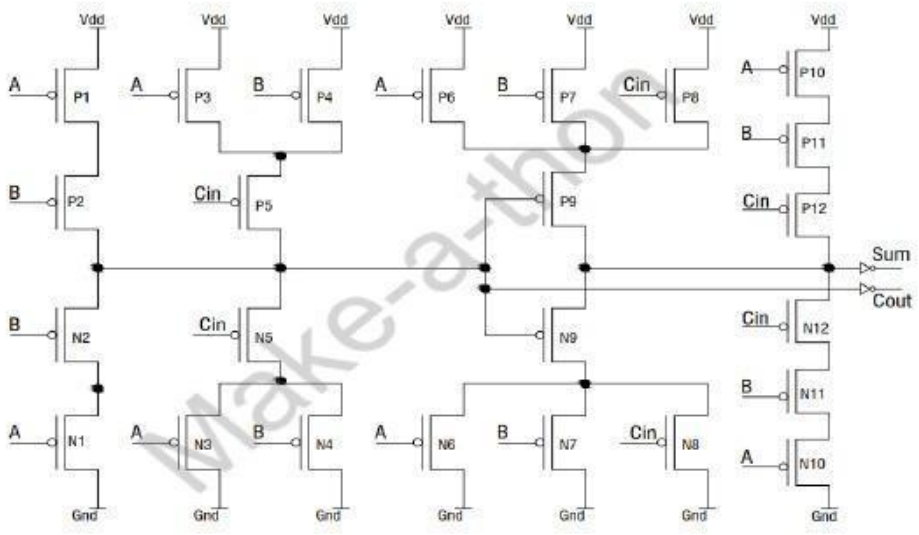
This report presents the transistor-level design and simulation of six different full adder architectures using the Cadence design tool. The primary objective of this work is to analyze and compare the propagation delays of each design under two scenarios: without transistor sizing (default W/L ratios) and with optimized transistor sizing. Transistor sizing, a common technique in VLSI, involves adjusting the width-to-length ratios of transistors to improve circuit performance in terms of speed, power consumption, and area.

By evaluating the delay characteristics of each design, the most efficient full adder implementation was identified. This optimized full adder was then employed as a building block in the construction of a 4-bit binary multiplier, demonstrating how low-level optimizations can enhance the performance of more complex digital systems.

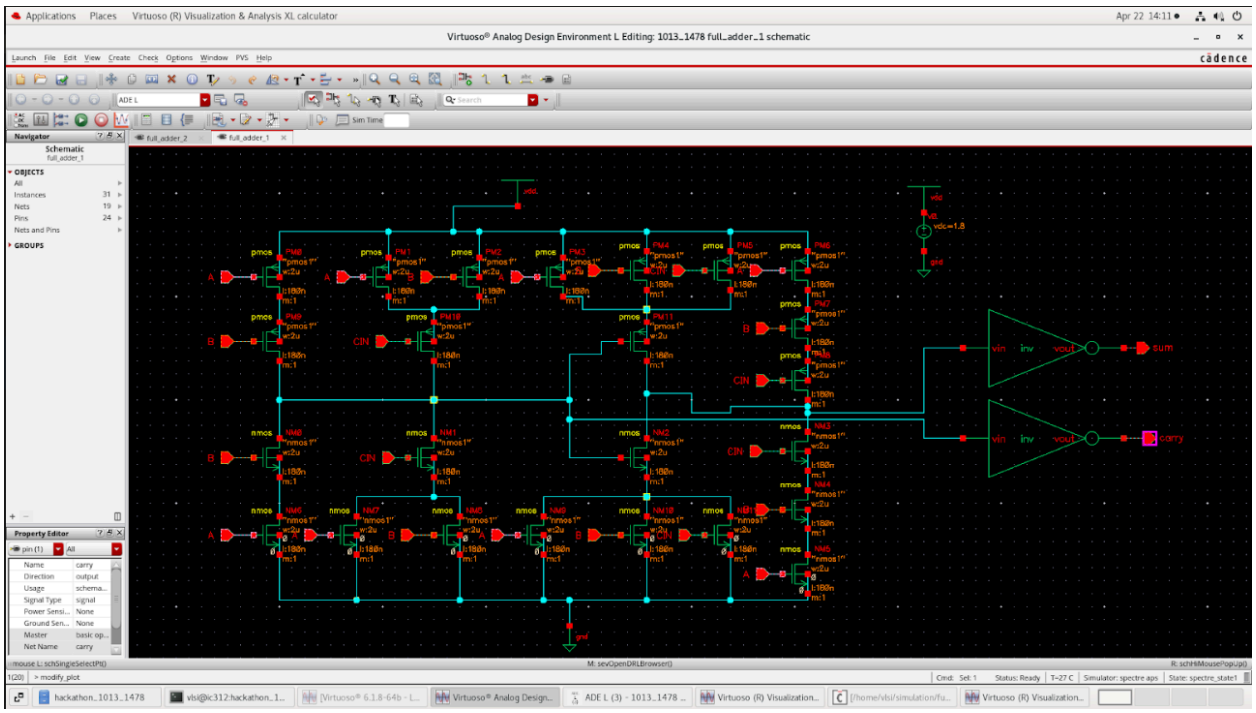
The simulations and results presented in this study highlight the impact of transistor-level optimization on circuit performance and underscore the practical application of tools like Cadence in modern VLSI design. This work contributes to the ongoing effort to develop high-speed, low-power arithmetic circuits for contemporary computing and embedded systems.

FULL ADDER ONE

CIRCUIT DIAGRAM:



SCHEMATIC:



OUTPUT:


Applications Places Virtuoso (R) Visualization & Analysis XL
Apr 22 14:12
Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Transient Response
Tue Apr 22 14:07:40
/carry
/pwr
/sum
/A
/B
/CIN
V (V)
W (uW)
time (ns)

DELAYS AND POWER:

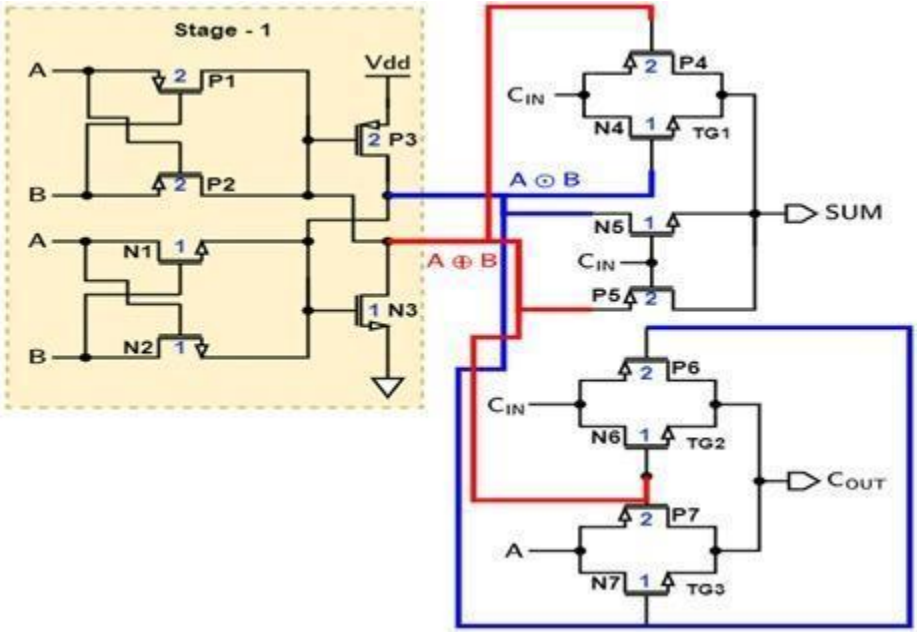
Output edge	Input signal	Input edge	Delay	
			Before sizing	**After sizing**
Cout:				
R1	Cin	R2	109.14ps	136.1ps
F1	A	R1	214 ps	183.4ps
R2	Cin	R3	111.6 ps	160ps
Sum:				
R1	Cin	R1	85.87 ps	117.9ps
F1	Cin	R2	198 ps	249.9ps
R2	Cin	F2	294.5 ps	301.9ps
F2	Cin	R3	189.3 ps	250.3ps
R3	Cin	R4	122.8 ps	158.1ps
Power:			6.632 uW	24.36 uW

INFERENCE:

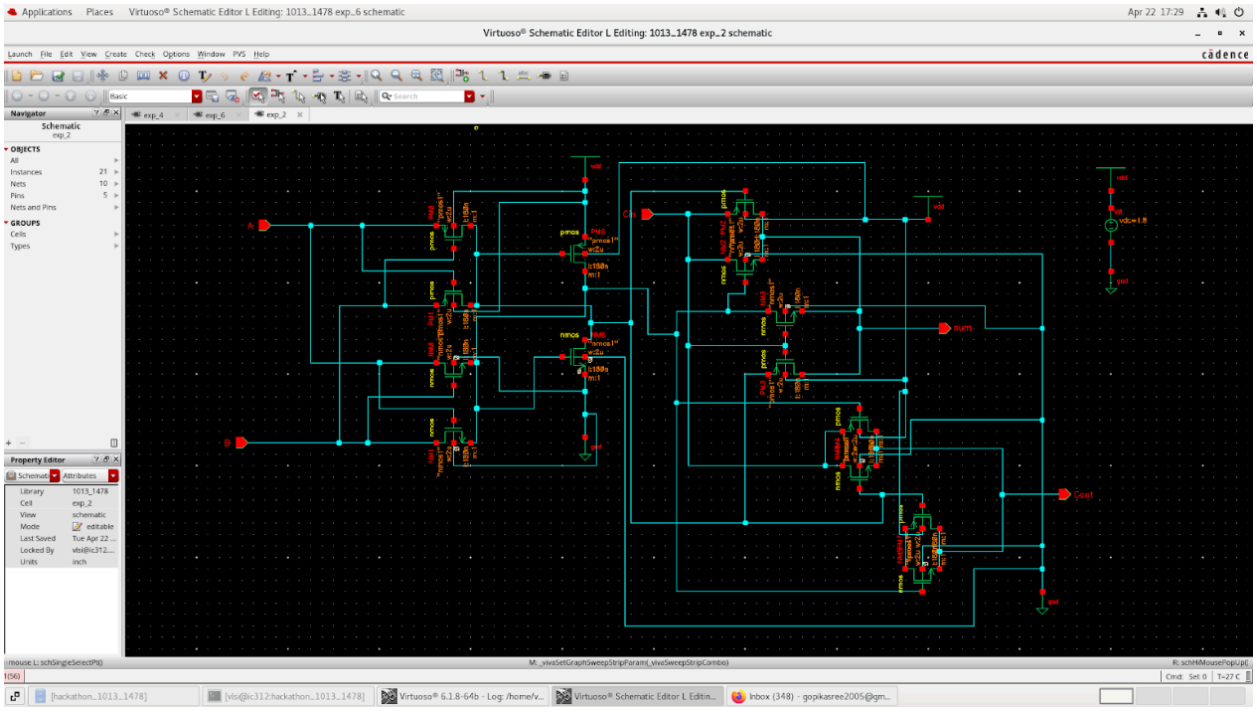
The maximum delay in this circuit is 294.5 ps.

FULL ADDER TWO

CIRCUIT DIAGRAM:



SCHEMATIC:



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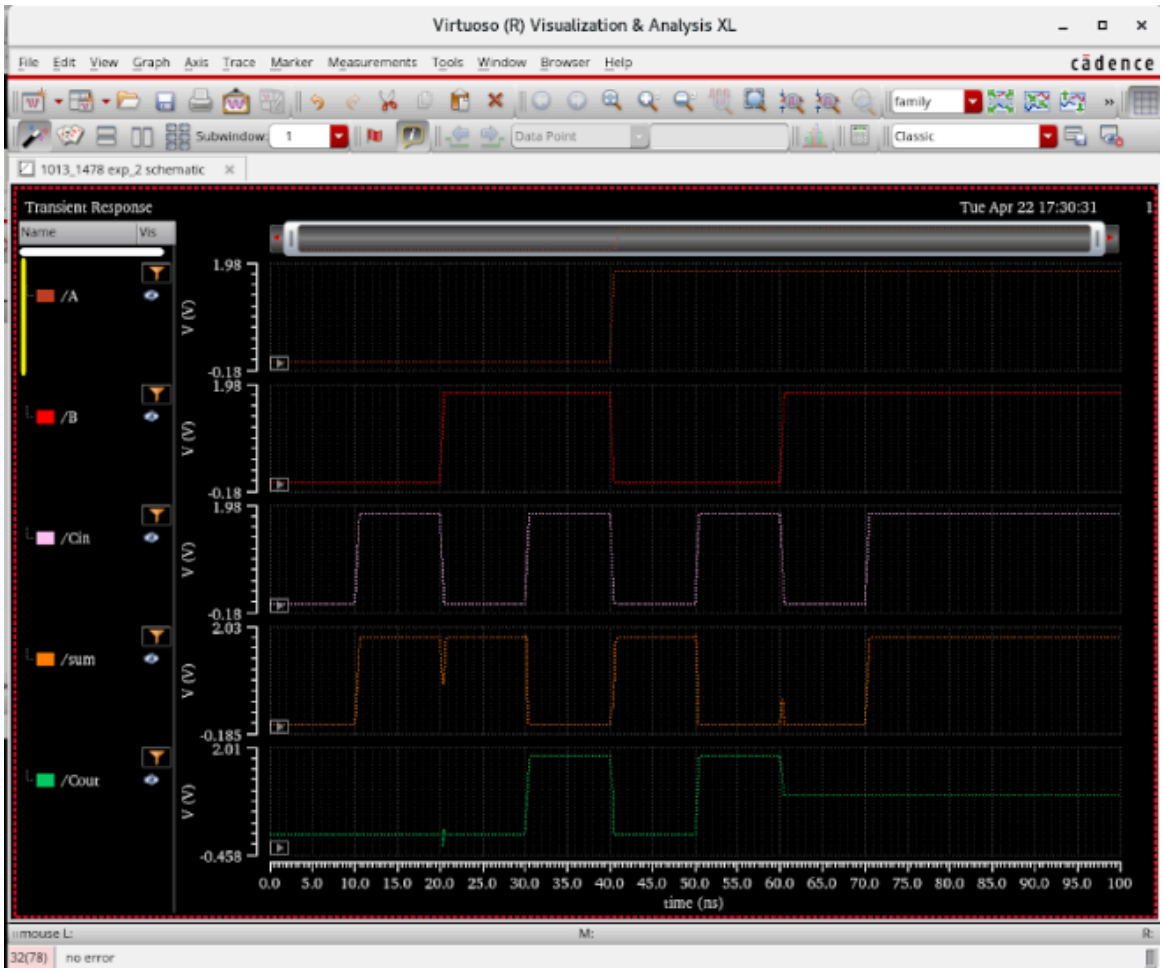

Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
1013_1478 exp_2 schematic
Transient Response
Tue Apr 22 17:30:31
Name
Vis
/A
/B
/Cin
/sum
/Cout
1.98
-0.18
2.03
-0.185
2.01
-0.458
0.0 5.0 10.0 15.0 20.0 25.0 30.0 35.0 40.0 45.0 50.0 55.0 60.0 65.0 70.0 75.0 80.0 85.0 90.0 95.0 100
time (ns)
no error

DELAYS AND POWER:

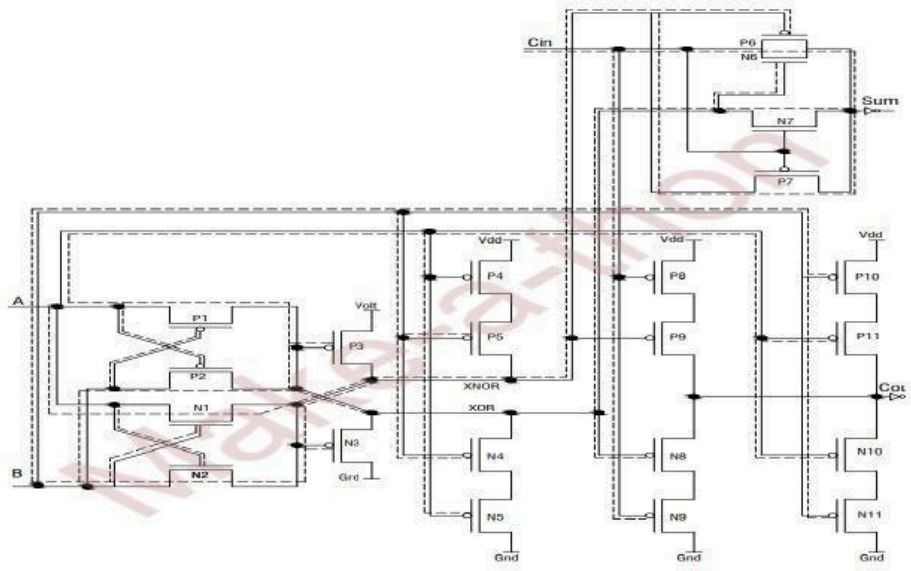
Output edge	Input signal	Input edge	Delay	
			Before sizing	**After sizing**
Cout:				
R1	Cin	R2	19.2 ps	23.57ps
F1	A	R1	130.4 ps	136.7ps
R2	Cin	R3	19.19 ps	23.35ps
Sum:				
R1	Cin	R1	13.5 ps	16.91ps
F1	Cin	R2	30.25ps	61.03ps
R2	Cin	F2	234.1ps	216.2ps
F2	Cin	R3	30.19ps	60.9ps
R3	Cin	R4	13.64ps	17.18ps
Power:			6.687 uW	7.353uW

INFERENCE:

The maximum delay in this circuit is 234.1 ps.

FULL ADDER THREE

CIRCUIT DIAGRAM:



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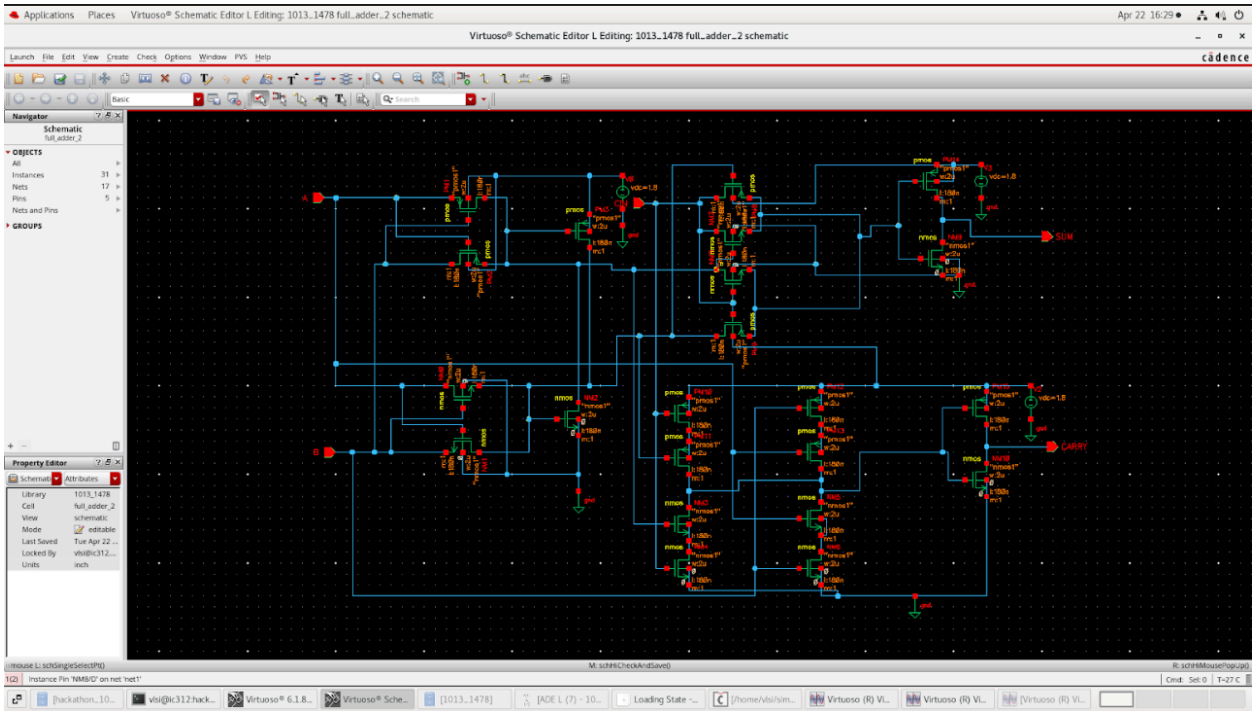

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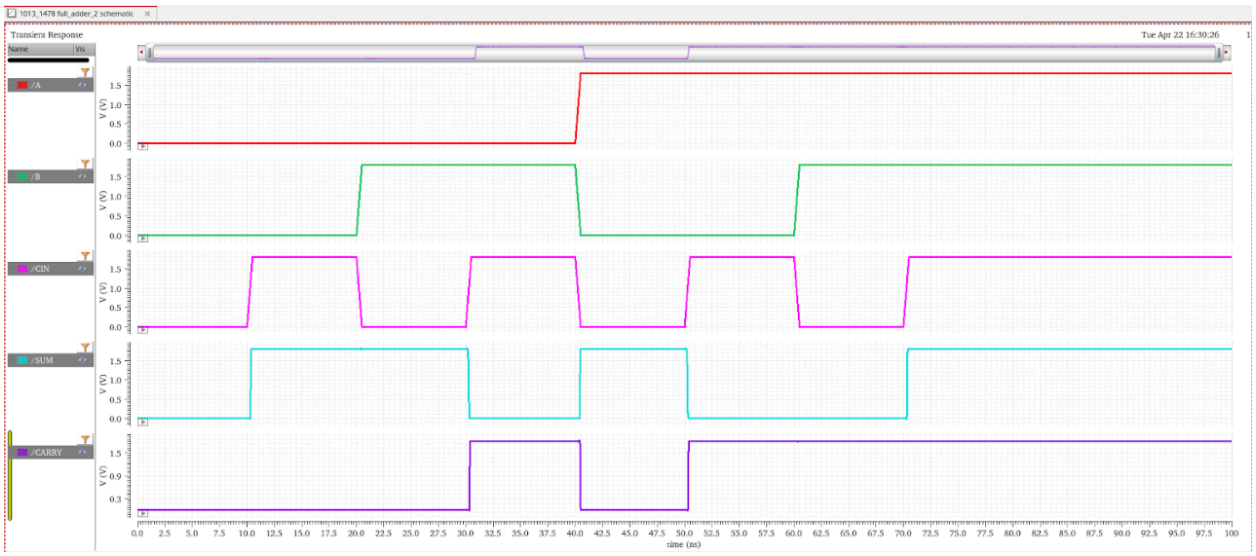

1013_1478 full_adder_2 schematic
Transient Response
Tue Apr 22 16:30:26
Name
Vis
/A
/B
/CIN
/SUM
/CARRY
V (V)
time (ns)

DELAYS AND POWER:

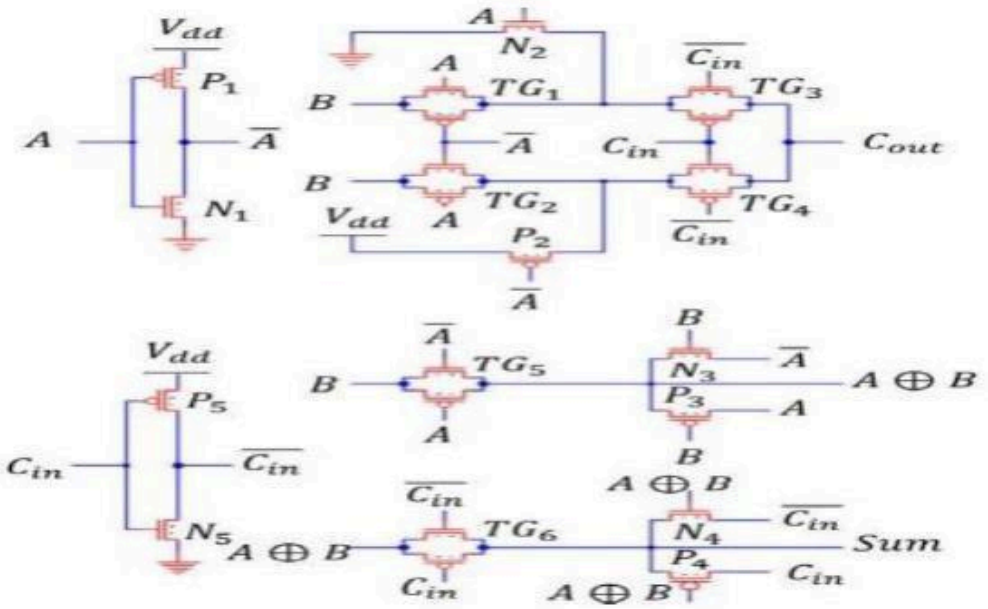
Output edge	Input signal	Input edge	Delay	
			Before sizing	**After sizing**
Cout:				
R1	Cin	R2	92.13ps	158ps
F1	A	R1	227.5 ps	265.6ps
R2	Cin	R3	90.83ps	138.7ps
Sum:				
R1	Cin	R1	88.04 ps	115.5ps
F1	Cin	R2	16.63 ps	18.66ps
R2	Cin	F2	186.52ps	276.6ps
F2	Cin	R3	16.71ps	19.97ps
R3	Cin	R4	87.88ps	107.3ps
Power:			6.87 uW	16.19uW

INFERENCE:

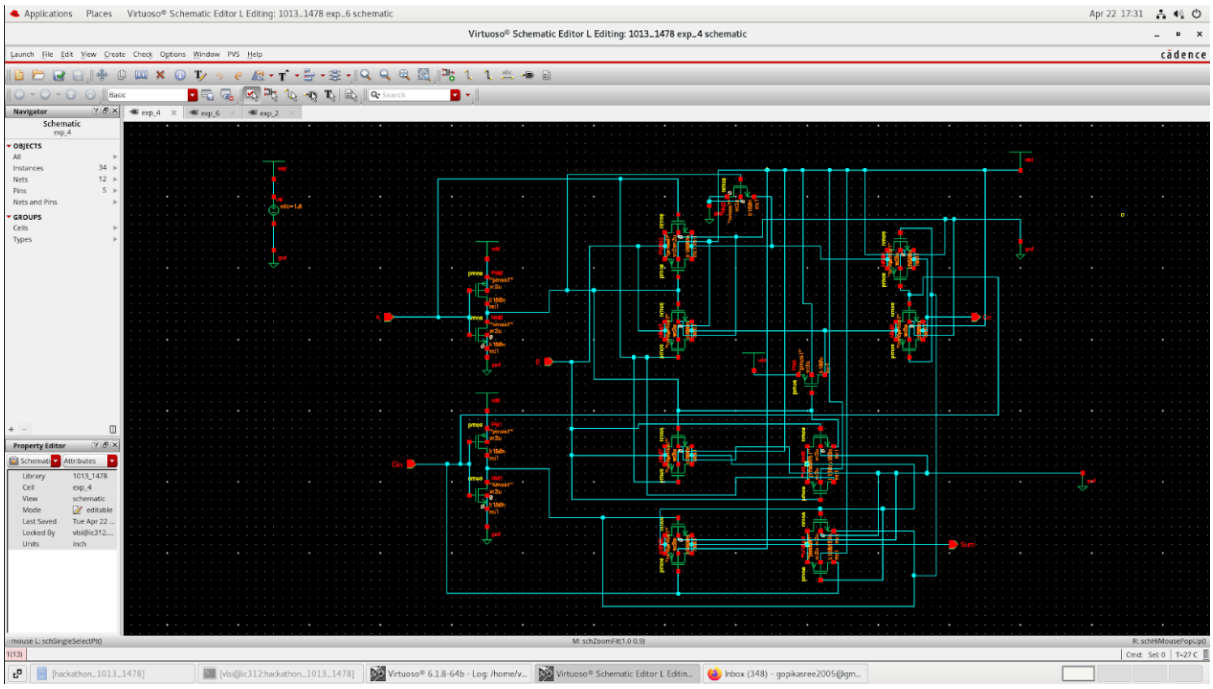
The maximum delay is 227.5 ps.

FULL ADDER FOUR

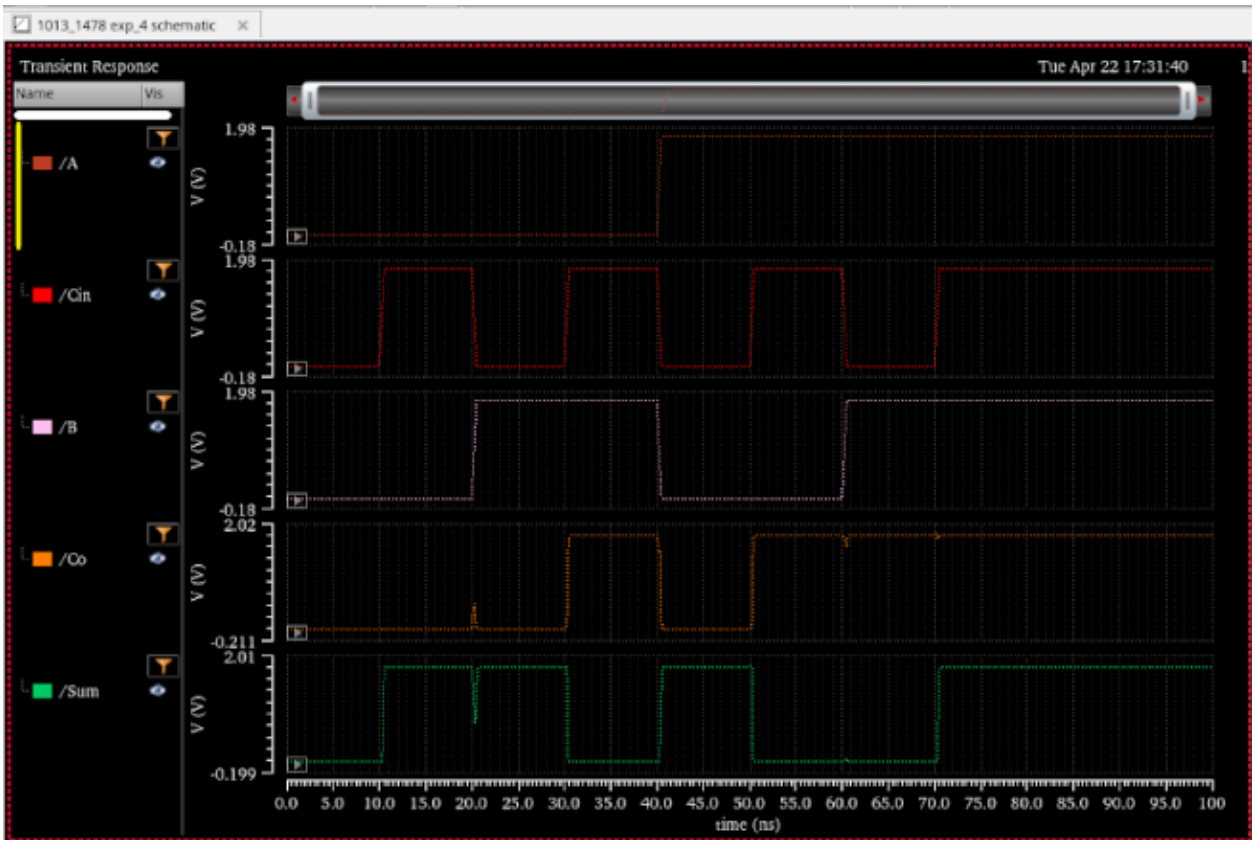
CIRCUIT DIAGRAM:



SCHEMATIC:



OUTPUT:


1013_1478 exp_4 schematic
Transient Response
Tue Apr 22 17:31:40
Name
Vis
/A
/Cin
/B
/Co
/Sum
1.98
-0.18
1.98
-0.18
1.98
-0.18
2.02
-0.211
2.01
-0.199
V (V)
0.0 5.0 10.0 15.0 20.0 25.0 30.0 35.0 40.0 45.0 50.0 55.0 60.0 65.0 70.0 75.0 80.0 85.0 90.0 95.0 100
time (ns)

DELAY AND POWER:

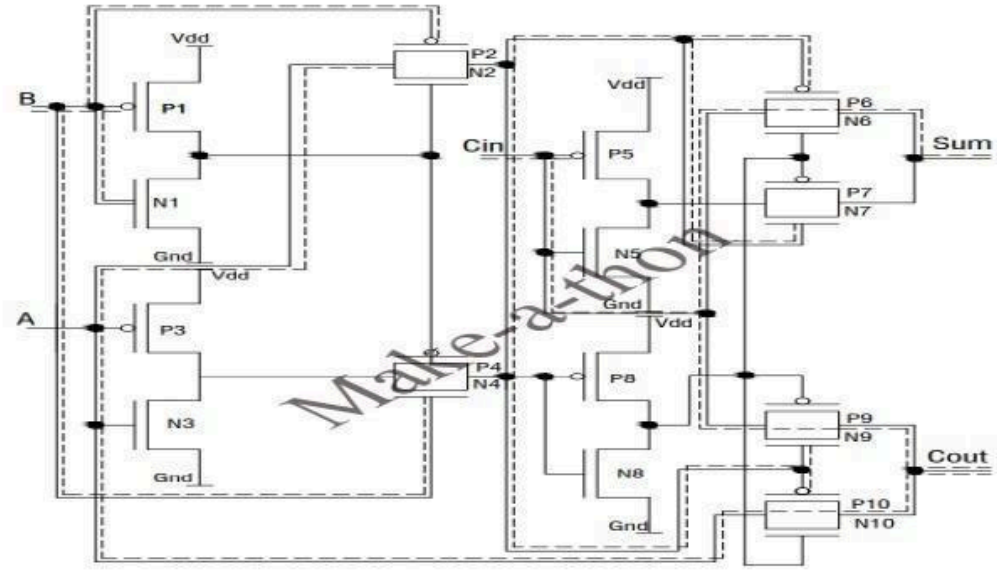
Output edge	Input signal	Input edge	Delay	
			Before sizing	**After sizing**
Cout:				
R1	Cin	R2	112.2 ps	121.3ps
F1	A	R1	197.4ps	178.5ps
R2	Cin	R3	112.2ps	121.3ps
Sum:				
R1	Cin	R1	137ps	126.1ps
F1	Cin	R2	70.76ps	111.2ps
R2	Cin	F2	186.6ps	175.3ps
F2	Cin	R3	76.61ps	111.2ps
R3	Cin	R4	136.8ps	127ps
Power:			6.606 uW	11.75 uW

INFERENCE:

The maximum delay here is 197.4 ps.

FULL ADDER FIVE

CIRCUIT DIAGRAM:



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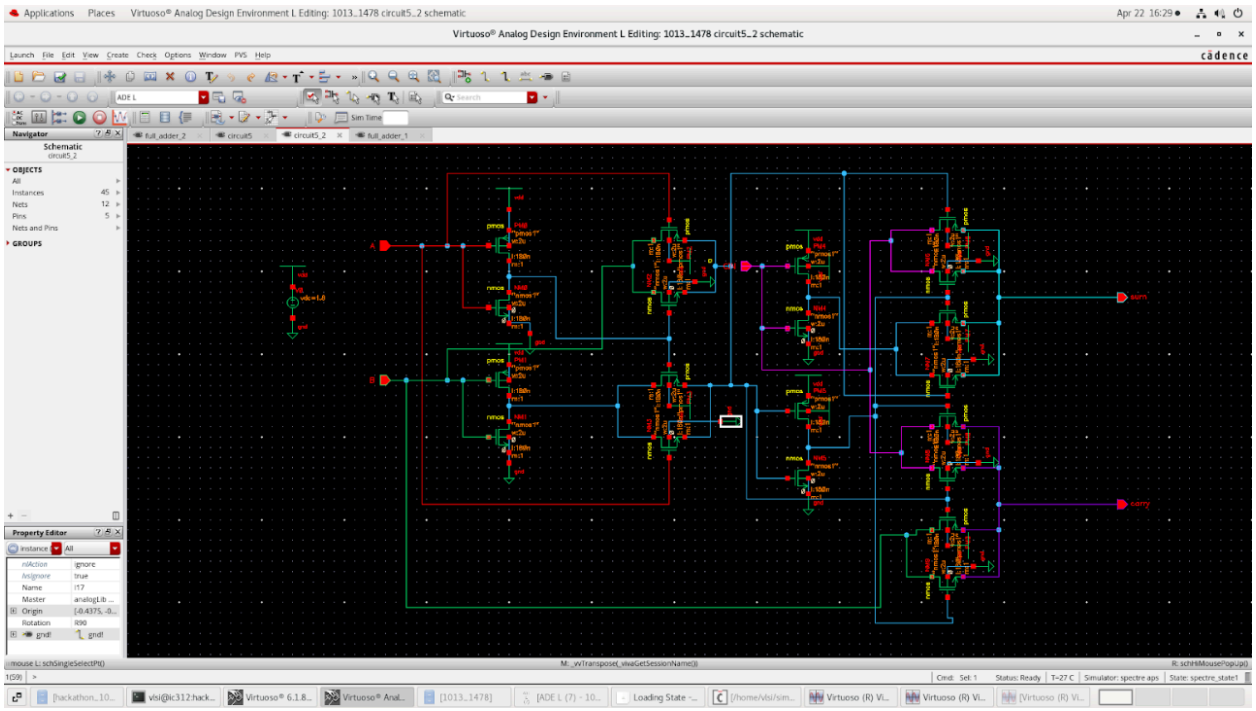
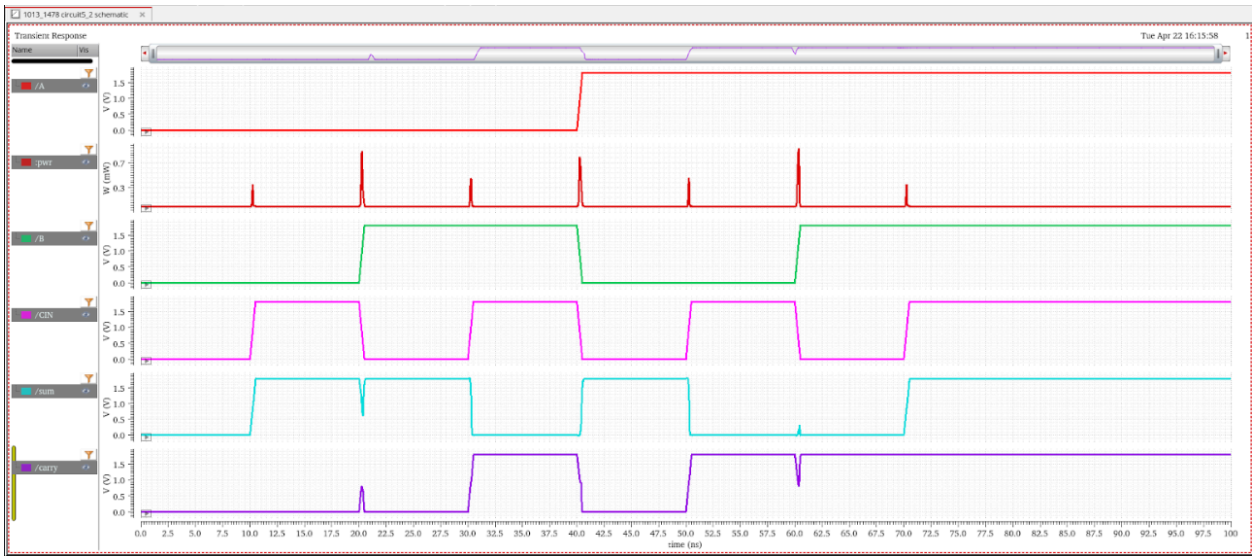


OUTPUT:


1013_1478 circuit5_2 schematic
Transient Response
Tue Apr 22 16:15:58
Name
/A
:pwr
/B
/CIN
/sum
/carry
V (V)
W (mW)
time (ns)

DELAY AND POWER:

Circuit 5:

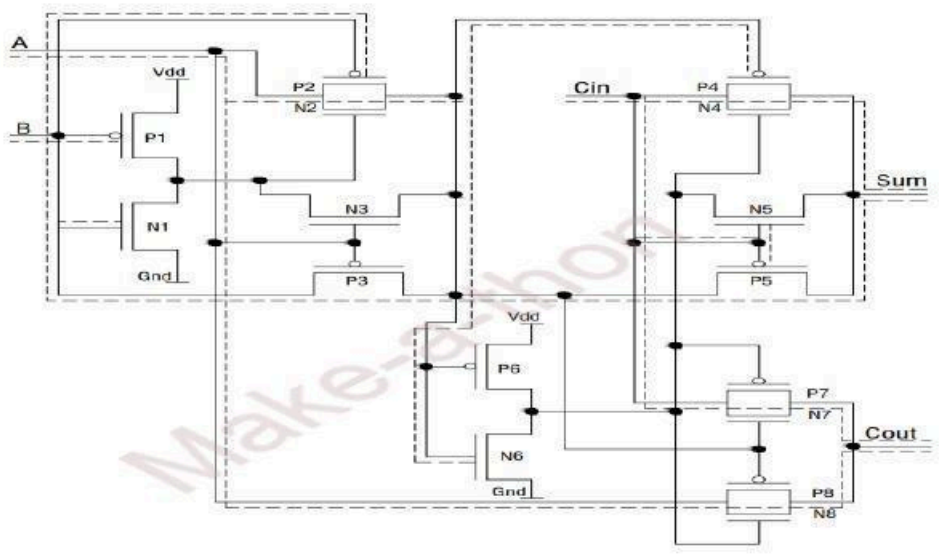
Output edge	Input signal	Input edge	Delay	
			Before sizing	**After sizing**
Cout:				
R1	Cin	R2	15.09ps	19.68ps
F1	A	R1	73.84ps	52.54ps
R2	Cin	R3	15.89ps	20.51ps
Sum:				
R1	Cin	R1	15.75ps	20.5ps
F1	Cin	R2	61.52ps	97.01ps
R2	Cin	F2	183.2ps	148.3ps
F2	Cin	R3	61.79ps	97.12ps
R3	Cin	R4	15.88ps	20.56ps
Power:			6.423 uW	13.17uW

INFERENCE:

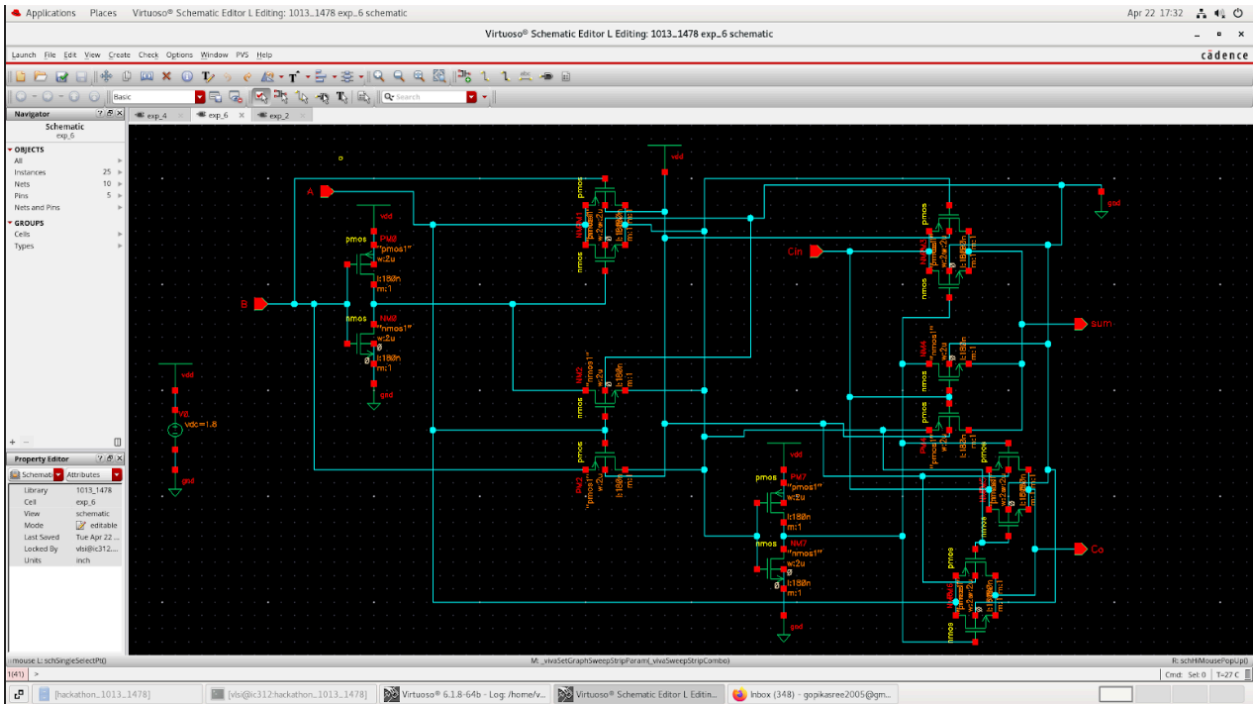
The maximum delay is 183.2 ps.

FULL ADDER SIX

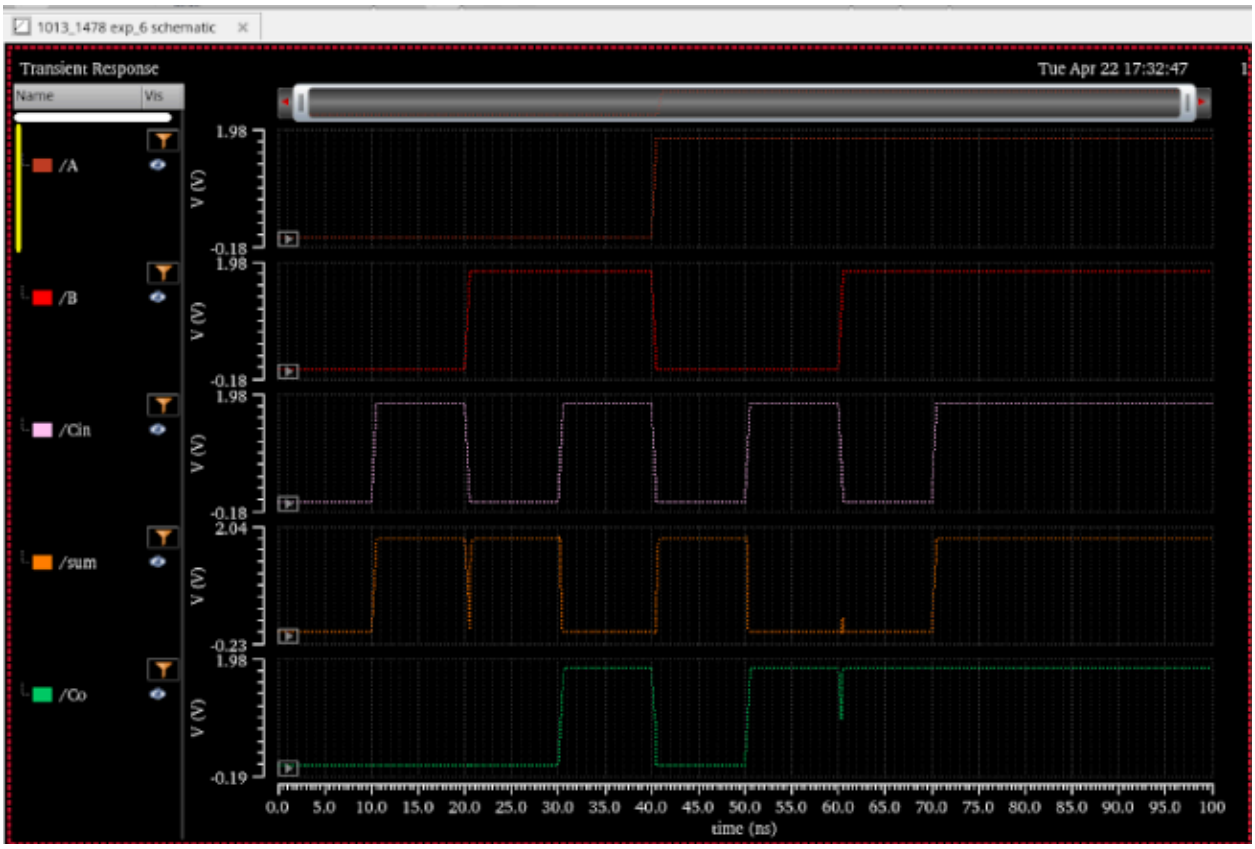
CIRCUIT DIAGRAM:



SCHEMATIC:



OUTPUT:


1013_1478 exp_6 schematic
Transient Response
Tue Apr 22 17:32:47
Name
Vis
/A
/B
/Cin
/sum
/Co
1.98
-0.18
1.98
-0.18
1.98
-0.18
2.04
-0.23
1.98
-0.19
V (V)
0.0 5.0 10.0 15.0 20.0 25.0 30.0 35.0 40.0 45.0 50.0 55.0 60.0 65.0 70.0 75.0 80.0 85.0 90.0 95.0 100
time (ns)

DELAY AND POWER:

Output edge	Input signal	Input edge	Delay	
			Before sizing	After sizing
Cout:				
R1	Cin	R2	19.04ps	19.46ps
F1	A	R1	20.09ps	74.23ps
R2	Cin	R3	17.50ps	17.27ps
Sum:				
R1	Cin	R1	9.947ps	12.20ps
F1	Cin	R2	20.06ps	44.81ps
R2	Cin	F2	272.3ps	241.1ps
F2	Cin	R3	12.35ps	43.25ps
R3	Cin	R4	6.291ps	9.985ps
Power:			4.11 uW	7.218uW

INFERENCE:

The maximum delay is 272.3 ps.

FINAL RESULT AND CONCLUSION:

By comparing all the maximum delays of the six circuits, we can see that circuit five has the least maximum delay. This demonstrates how well its architecture reduces critical path delays and increases switching performance.

The fifth full adder design was chosen as the best option in light of this outcome, and it was then utilized as the basic component of a 4-bit binary multiplier. This optimized full adder was used to synthesize the multiplier circuit, which was then evaluated for performance and functionality to ensure accuracy and efficiency.

This experiment demonstrates how crucial low-level circuit optimization is for improving the functionality of intricate digital systems, particularly transistor sizing. Modern VLSI and embedded systems depend on faster, smaller, and more power-efficient arithmetic units, which are developed in part by the results.

32 bit multiplier using 5th circuit: