

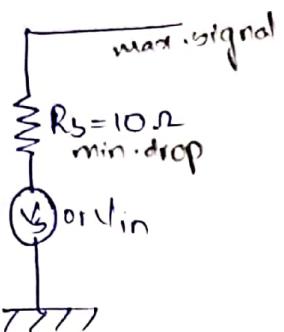
UNIT - II

9/12/19

MULTISTAGE AMPLIFIERS

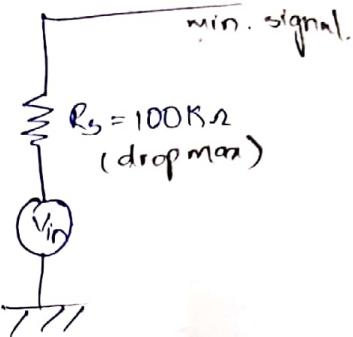
introduction.

(i) Voltage Sources (Types)



strong source

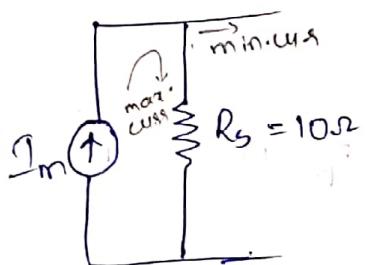
→ Weak & strong depends
of source.



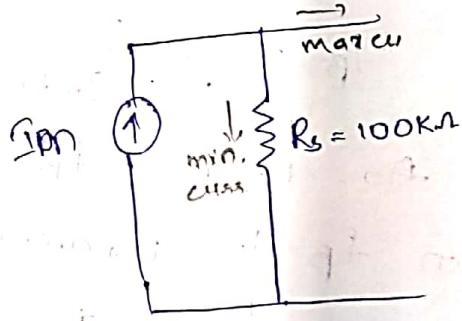
weak source.

on internal resistance

(ii) Current Source



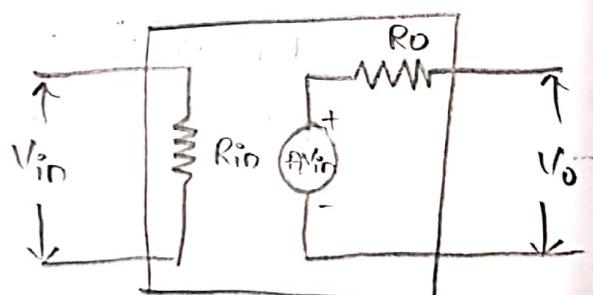
weak source



Strong current source

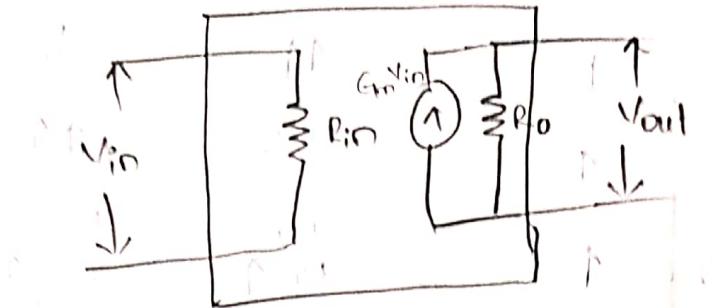
* AMPLIFIERS (Types)

1. Voltage Amplifier



Let Gain be 'f' then the i/p voltage is amplified to (fV_{in}) but we cannot get it across R_o so there is a drop due to which it across R_o

2. Trans conductance - Amplifier



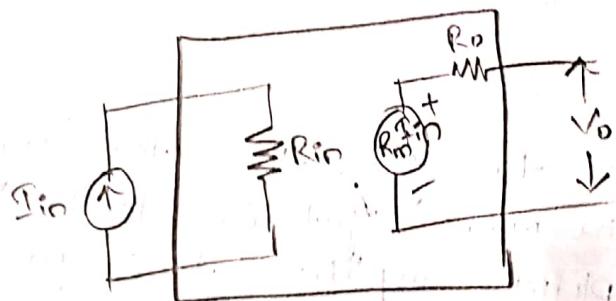
Trans conductance = G_m

3. Current - Amplifier



Current Gain = A_f

4. Trans Resistance - Amplifier

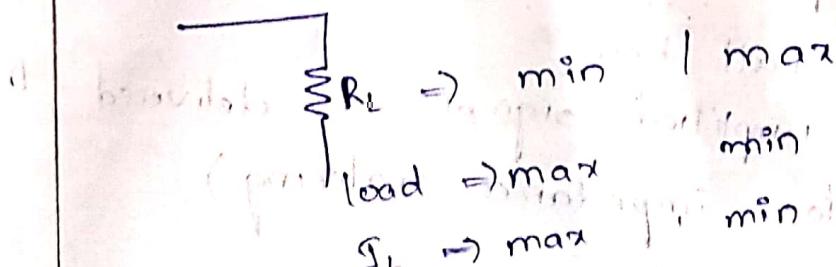


R_m - Transresistance.

* Load (how much current it takes)

There are 2 types of loads

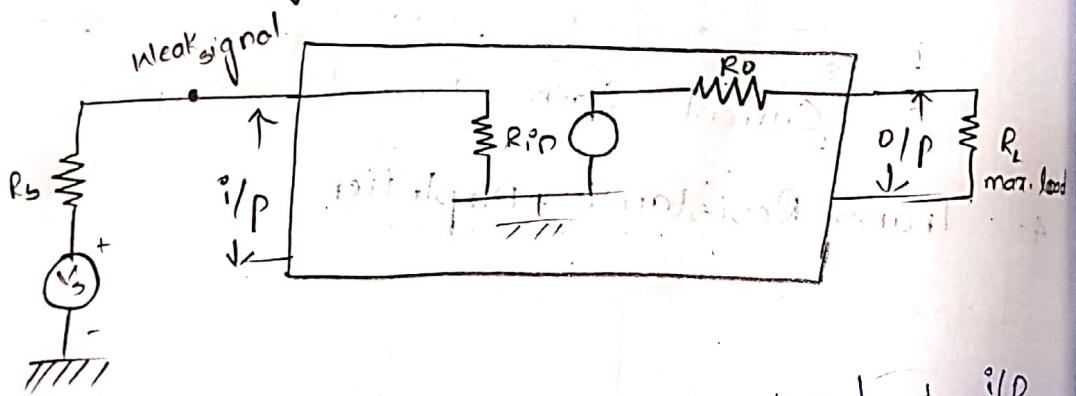
1. analog (which is connected to analog circuit) (R_L)
2. digital (connected to digital circuit or some digital display) (C_L)



	CE	CC Voltage buffer	CB current buffer
R_m	↑	↑↑	↓
R_{out}	↑	↓↓	↑↑
A (Gain)	↑	$A_v = 1$ $A_i \uparrow$	$A_i = 1$ $A_v = 1 \uparrow$
BW	↑	↑↑	\downarrow $I_e = \beta I_B$ Voltage source.

* MULTISTAGE AMPLIFIER.

Case(i)- Voltage source



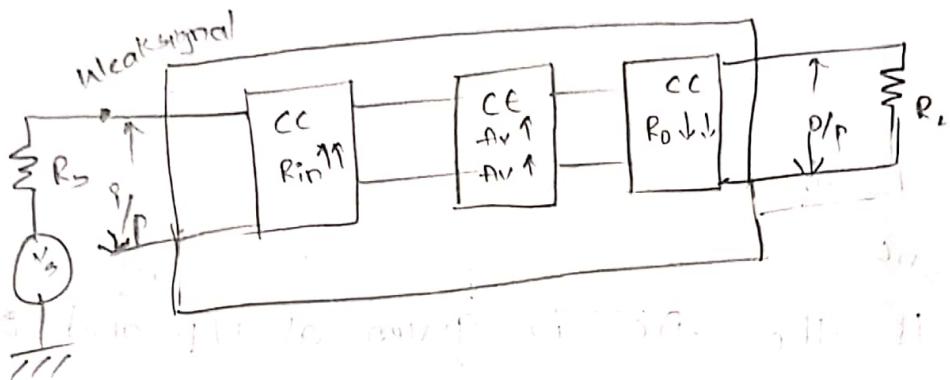
→ We have to give the weak signal at i/p side, the weak signal is feed to the amplifier side, the amplifier amplifies it & gives it to load.

Requirements:

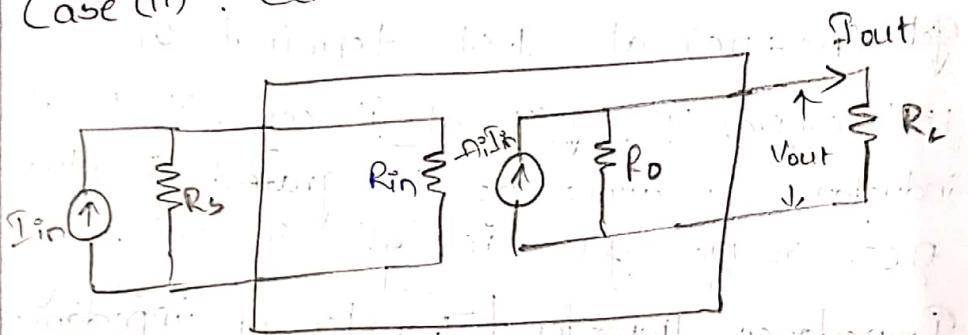
1. $R_{in} \rightarrow$ high (becoz to entire i/p signal is feeded into amplifier (i.e. impedance matching to be done))
2. Gain \rightarrow be high (''to amplify i/p signal)
 $A_v, A_i \uparrow$
3. $R_o \rightarrow$ small 'becoz entire amplified signal is delivered to load (for impedance matching).

So No -Amplifier can satisfy all 3 above requirements so we construct a multistage amplifiers to satisfy all requirements

$\Rightarrow R_{in}, R_{out} \rightarrow cc, -A_{v1}, A_{v2} \Rightarrow CE$



Case (ii) : current source as load

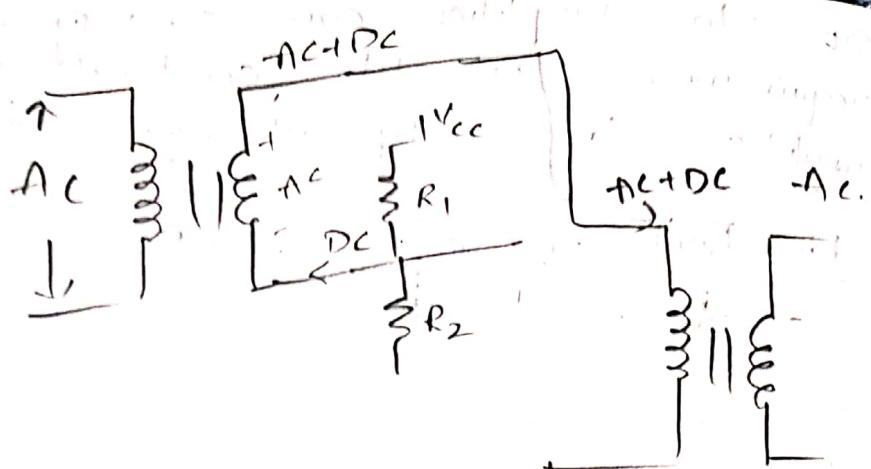


Requirements

1. R_{in} - low. (To allow whole current to amplifier)
 2. Gain - high
 3. R_o - high (becoz to allow max. current to load)
- \Rightarrow To meet these requirements will use CB and CC amplifier to design multistage amplifier with current source

METHODS OF INTERSTAGE COUPLING.

- \rightarrow ABOUT TRANSFORMER:
- 1. Inductor as adder and subtractor
 - 2. Transformer - used to add AC & DC used to separate AC & DC



\rightarrow Add \rightarrow AC & DC

If the AC is given at 1st and 2nd terminal is connected to DC (some source) we get $(AC+DC)$ at 1st terminal on 2nd side.

separate AC & DC
If $(AC+DC)$ is given at 1st coil, it allows inductor to ground & allows AC. so we get AC at 2nd coil.

2. * Impedance Transfer | Transfer of impedance

10 : 1



By adjusting coils we are changing resistance so that to match load

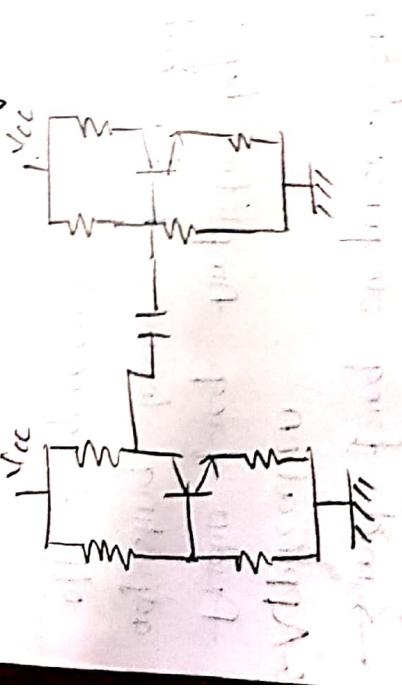
$$\frac{Z_1}{Z_2} = \left(\frac{n_1}{n_2}\right)^2$$

$$Z_1 \left(\frac{n_2}{n_1}\right)^2 = Z_2$$

$$1 \text{ k}\Omega (R_0 \text{ for } CE)$$

$$\therefore Z_2 = 10 \Omega$$

RC Coupled multistage



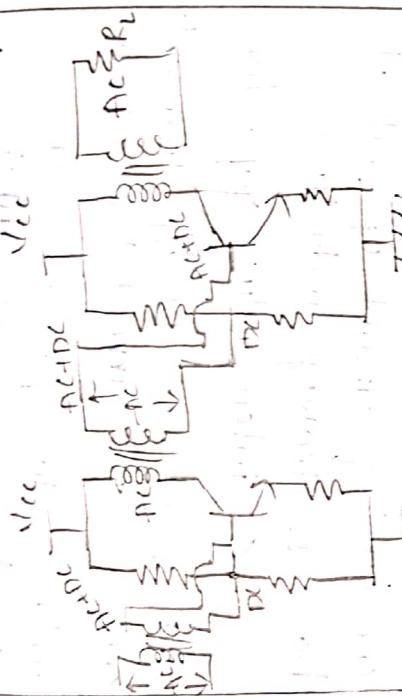
1. It has DC isolation

2. Drift : unwanted changes in the o/p due to temp variation (PVT changes w.r.t temp)
No drift

3. We need to use CC at IP & O/P for impedance matching. So impedance matching is not done in RC coupled circuit

4. Hardware complexity is less.

Transformer coupled multistage Direct coupled multistage



1. It has DC isolation

2. It has no drift

3. Impedance matching is done by transformer.

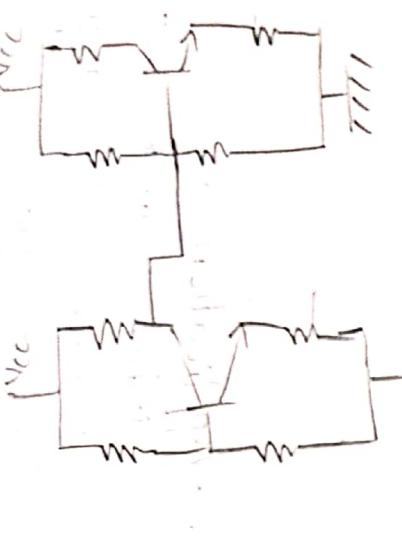
4. Hardware complexity (Bulky)

5. No impedance matching is done

6. Hardware complexity is less

7. Hardware needs more area.

Transformer coupled multistage Direct coupled multistage



1. It has no DC isolation because

on direct coupling ac voltage at next stage which affects Q-point of and stage

2. It has drift.

3. No impedance matching

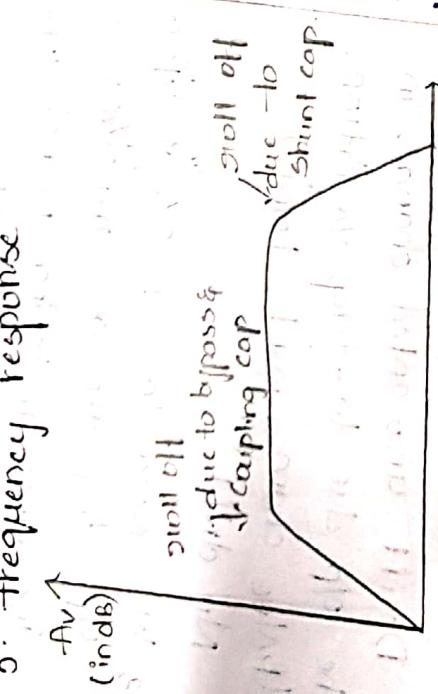
4. Hardware complexity is less

5. Hardware needs more area.

6. Hardware needs more area.

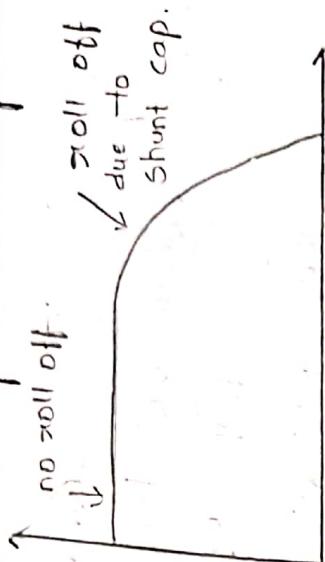
Rc coupled Multistage

5. frequency response



Transformer coupled multistage

Transformer coupled multistage



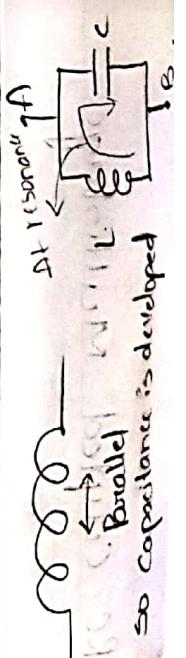
It amplifies both AC & DC signal
so if we want to amplify both
then we can go for this

In place of R_c we have shunt impedance of matching transformer. So when we consider e.g. circuit of coil it has L - leakage inductance C - interwinding capacitance

\rightarrow mid freq. response is const.

Application

Audio freq. amplifier by adjusting lower & higher cut off frequencies.



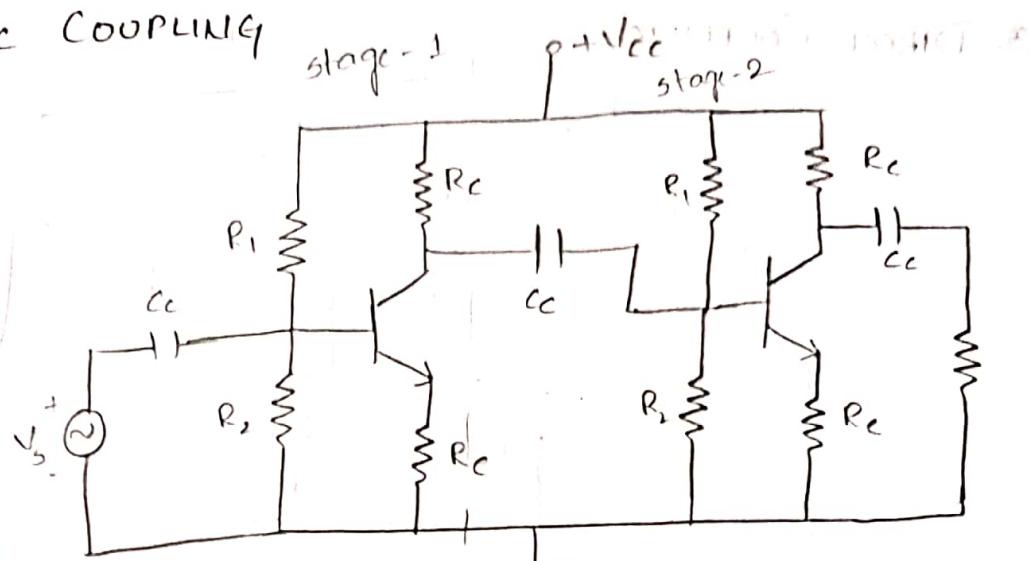
Application:
In Radio, TV receivers we have to tune a particular freq. so those freq. signals are amplified by this

inductor to cap. & vice versa so as there is no current the tank circuit offers high impedance. So Gain (R_o/R_e) \uparrow as $R_{\text{imp}} \uparrow$

At resonance no I/p from external source so current flows from

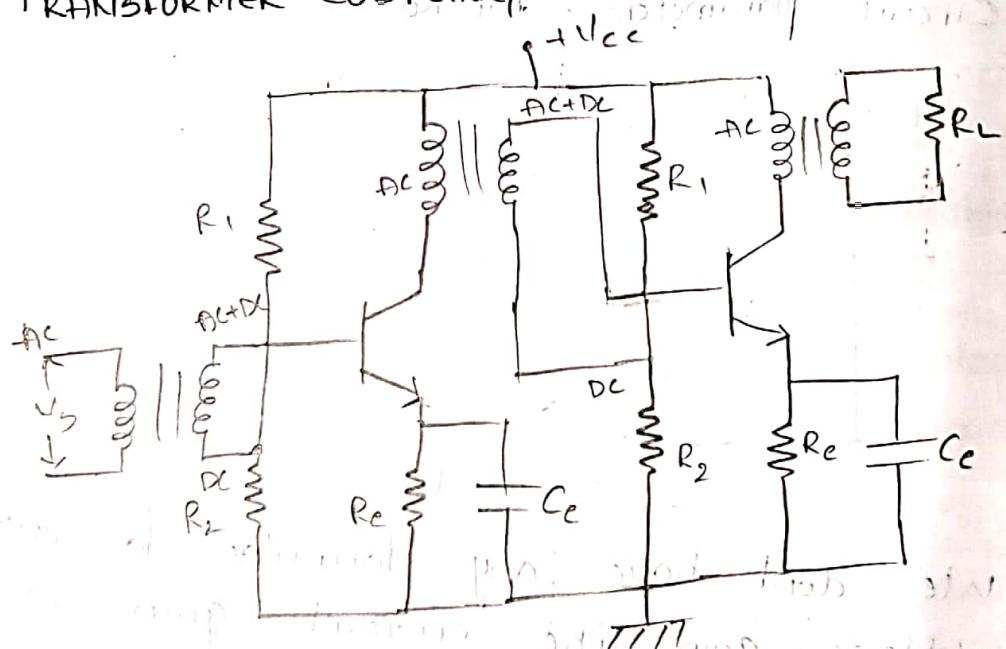
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1. RC COUPLING



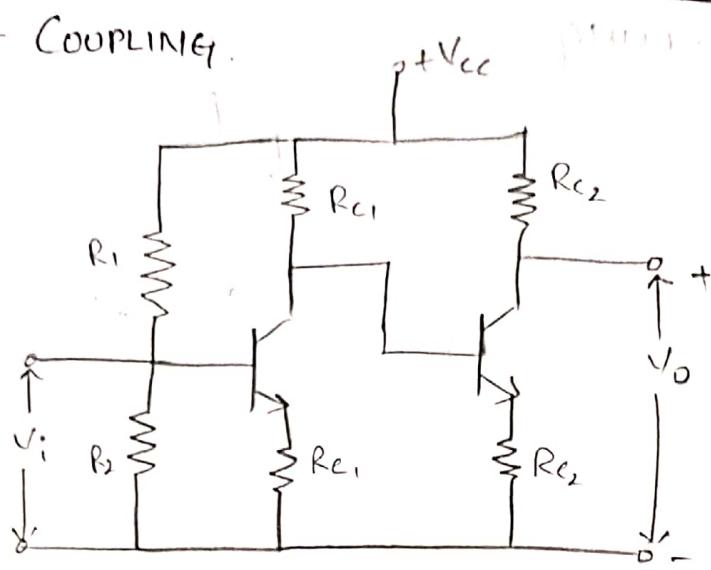
- Here 1st stage is coupled with a coupling cap. and resistive load at the o/p of 1st stage.
- Here the coupling capacitor allows AC and blocks DC so no DC from 1st stage is given to 2nd stage so there will be no affect on quiescent (Q)-point of next stage. So there will be no affect on operating point.

2. TRANSFORMER COUPLING



- It is coupled through an impedance matching transformer.
- As transformer blocks d.c, so there will be no affect on Q -point of next stage.

3. DIRECT COUPLING



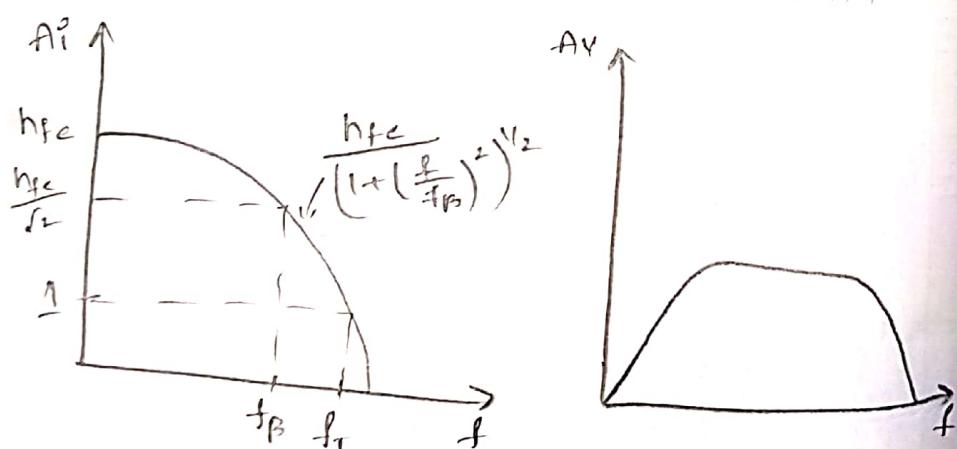
- O/P of 1st stage is directly connected to the i/p of the next stage.
- direct coupling allows the quiescent d.c. collector current of 1st stage to pass through base of the next stage, affecting its biasing conditions.

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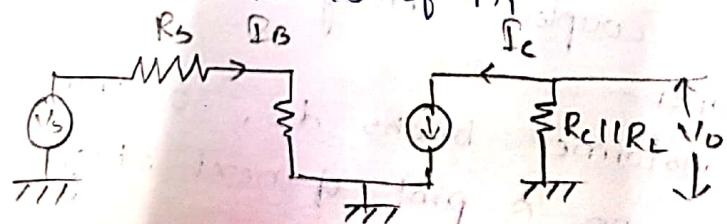
* N stage Cascading Amplifier

ANALYSIS

Circuit parameters - $R_{in}, R_o, A_i, A_v, B_W$



We don't have any formulae for current voltage gain like current gain so we write A_v in terms of A_f .



$$-A_V = \frac{V_o}{V_i} = \frac{R_o \times I_o}{R_{in} \times I_i} = \frac{R_o \times A_f}{R_{in}}$$

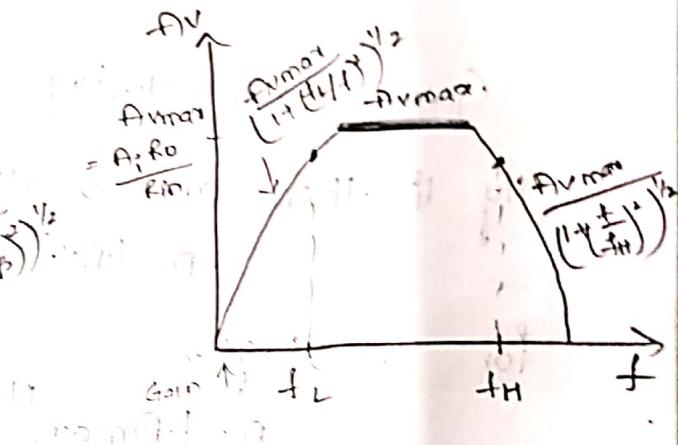
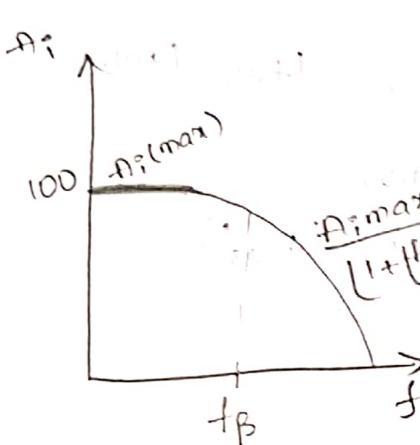
$$-A_V = \left(\frac{R_o / R_L}{R_{in} + R_S} \right) A_f$$

at low freq
at mid freq
at high freq

for CE amplifier,

$$(A_f)_{max} = h_{FE} = 100 \text{ dB}$$

$$(A_{fV})_{max} = A_f \times \frac{R_o}{R_{in}} = 100 \times \frac{1.5k}{1.2k} = 12.5 \text{ dB}$$



$\frac{f}{f_B}$ → freq. scaling factor. Scaling factor to be included in the eqn. There is a scaling factor which decides the gain.

→ for freq. response with current gain, at low freq's we have max. current gain (A_{fmax}) upto certain freq. f_B but after that roll off occurs. So there will be a scaling factor f/f_B (which is to be included in the eqn) decides the gain.

→ Similarly for freq. response with voltage gain, we have max. gain (A_{fVmax}) at mid frequency level. But at high freq's there is roll off i.e. Gain \downarrow so we have to include scaling factor f/f_H in the eqn so at high frequencies the

curve eqn is $\frac{A_{fVmax}}{\sqrt{1+(f/f_H)^2}}$. At low freq's gain

\uparrow so scaling factor to be reversed i.e. f_L/f so the curve eqn becomes, $A_{fVmax}/\sqrt{1+(f/f_L)^2}$

* Analysis of multistage amplifier.

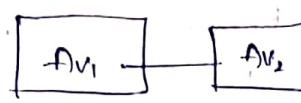
Case 1: $N = 1$



Gain of single stage (Av)

Gain of loaded single stage (Av')

Case 2: $N = 2$



1st stage loaded with 2nd one

Gain of multistage (A) = $(Av'_1)(Av'_2)$

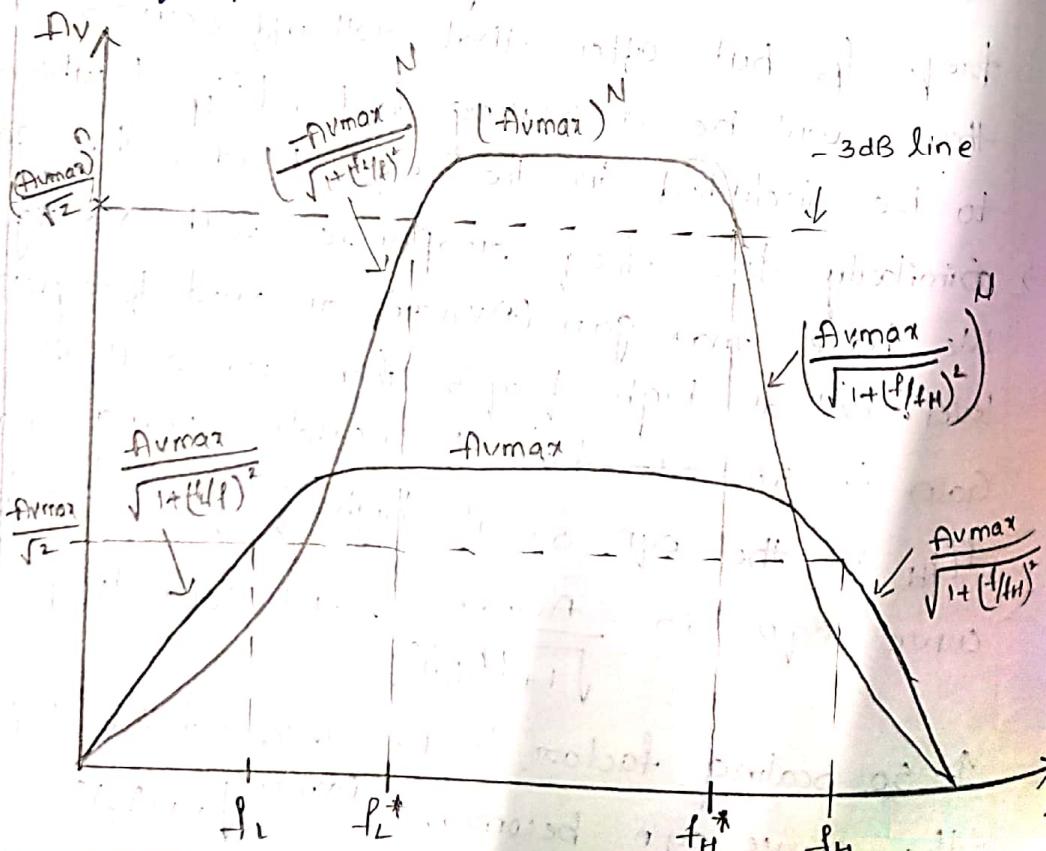
My If there are 3 stages,

$$A = (Av'_1)(Av'_2)(Av'_3)$$

for N stages,

$$A = (Av_{max})^N$$

→ When we plot graph for multistage amplifier of N stages, gain becomes $A = (Av_{max})^N$ at mid frequencies



* CALCULATION

f_L^*

$$\text{When } f = f_L^*, \quad A = \frac{(\text{Avmax})^N}{\sqrt{2}}$$

$$A = \left(\frac{\text{Avmax}}{\sqrt{1 + (\frac{f_L}{f_L^*})^2}} \right)^N \text{ at high frequencies}$$

$$\text{At } f = f_L^* \quad A = \frac{(\text{Avmax})^N}{\sqrt{2}}$$

$$\frac{(\text{Avmax})^N}{\sqrt{2}} = \left(\frac{\text{Avmax}}{\sqrt{1 + (\frac{f_L}{f_L^*})^2}} \right)^N$$

$$2 = \left(1 + \left(\frac{f_L}{f_L^*} \right)^2 \right)^N$$

$$\frac{f_L}{f_L^*} = \sqrt{2^{1/N} - 1}$$

$$\boxed{f_L^* = \frac{f_L}{\sqrt{2^{1/N} - 1}}} \quad \text{at high frequencies}$$

As $N \uparrow f_L^* \text{ also } \uparrow$ so lower cut off freq. of multistage amplifier (f_L^*) \uparrow as we \uparrow the no. of stages.

2. f_H^*

$$\text{When } f = f_H^*, \quad A = \frac{(\text{Avmax})^N}{\sqrt{2}} \cdot f_{H0}$$

$$A = \left(\frac{\text{Avmax}}{\sqrt{1 + (\frac{f_H}{f_H^*})^2}} \right)^N \text{ at high frequencies}$$

$$\text{At } f = f_H^*, \quad A = \frac{(\text{Avmax})^N}{\sqrt{2}}$$

$$\frac{(\text{Avmax})^N}{\sqrt{2}} = \left(\frac{\text{Avmax}}{\sqrt{1 + (\frac{f_H}{f_H^*})^2}} \right)^N$$

$$\alpha = \left(1 + \left(\frac{f_H^*}{f_H}\right)^2\right)^N$$

$$f_H^* = f_H \sqrt{2^{1/N} - 1}$$

As $N \uparrow$, $f_H^* \downarrow$ so higher cut off freq. of multistage amplifier \downarrow , as the no. of stages \uparrow
 → Analysis is done by compounding bandwidth & voltage gain.

Effect of Cascading

1. On Gain.

Gain becomes $(A_V)^N$ so Gain \uparrow for a multistage Amplifier

2. f_L^*

$$f_L^* = \frac{f_L}{(2^{1/N} - 1)^{1/2}}$$

$f_L^* \uparrow$ as stages \uparrow

3. f_H^*

$$f_H^* = f_H (2^{1/N} - 1)^{1/2}$$

$f_H^* \downarrow$ as stages \uparrow

4. Band width.

Band width of multistage amplifier \downarrow as the no. of stages \uparrow

In the Gain in decibels?
for a multistage amplifier with N stages,

$$G = G_1 \times G_2 \times G_3 \times \dots \times G_N$$

So Gain is multiplied on linear scale but on logarithmic scale,

$$G = 20 \log(G_1 \times G_2 \times G_3 \times \dots \times G_N)$$

$$G = 20 \{ \log G_1 + \log G_2 + \dots + \log G_N \}$$

Gain is added on log-scale so we can easily plot that & can compare.

$$\rightarrow f_L = 100 \text{ Hz} \quad f_H = 1 \text{ MHz} \quad f_L^*, f_H^* = ?$$

$$f_L^* = \frac{f_L}{\sqrt{2^{N-1}}} = \frac{100}{\sqrt{\sqrt{2}-1}} = 155.38 \text{ Hz}$$

$$f_H^* = f_H \sqrt{2^{N-1}} = 1 \text{ MHz} \sqrt{\sqrt{2}-1} = 643.59 \text{ kHz}$$

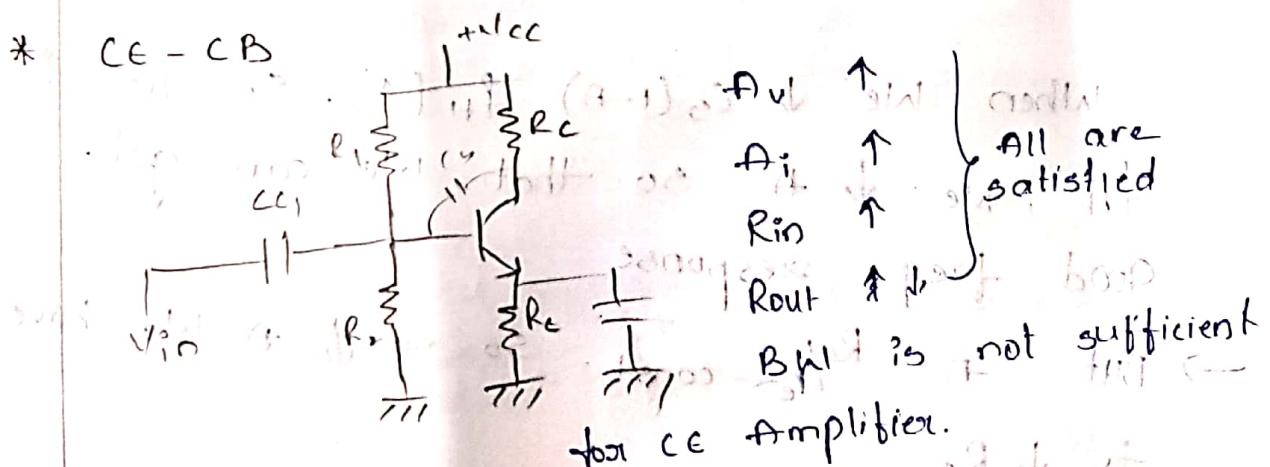
$$= 1 \text{ MHz} \sqrt{\sqrt{2}-1} = 643.59 \text{ kHz}$$

2/2/19

CASCADING STAGES

1. CE - CE
2. CE - CB (cascode amplifier) * for CB all are not satisfied except A_v
3. CC - CC (Darlington / Bootstrap)

- * CE - CB



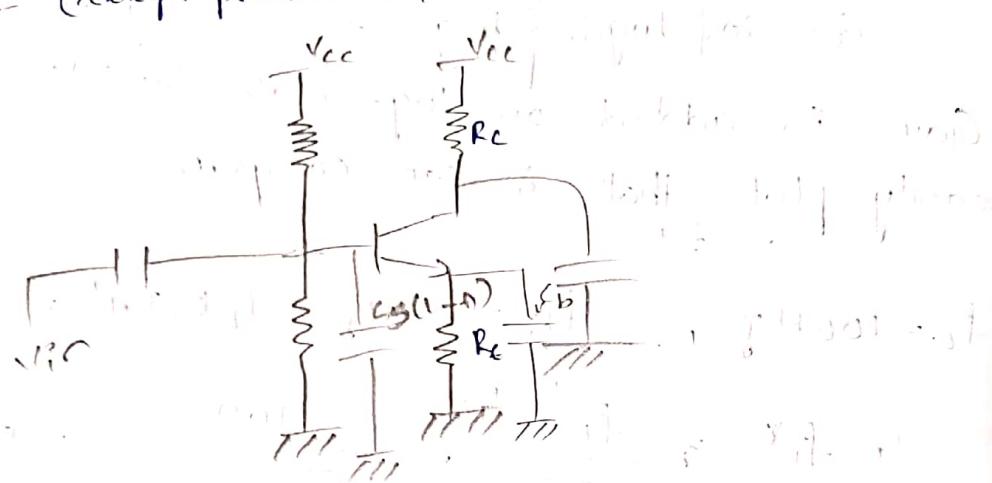
$$BW = f_H - f_L$$

↓
we can adjust
we cannot control

f_H (due to parasitic / shunt capacitors / stray)

$$f = \frac{1}{2\pi RC} \quad \text{so we } \uparrow f_H \rightarrow \uparrow BW \text{ by } 1.$$

c (coupled parasitic / shunt / stray)



To \downarrow the capacitive value $C_s(1-A)$ we have to $\downarrow A$ i.e. we can $\downarrow R_c$.

*



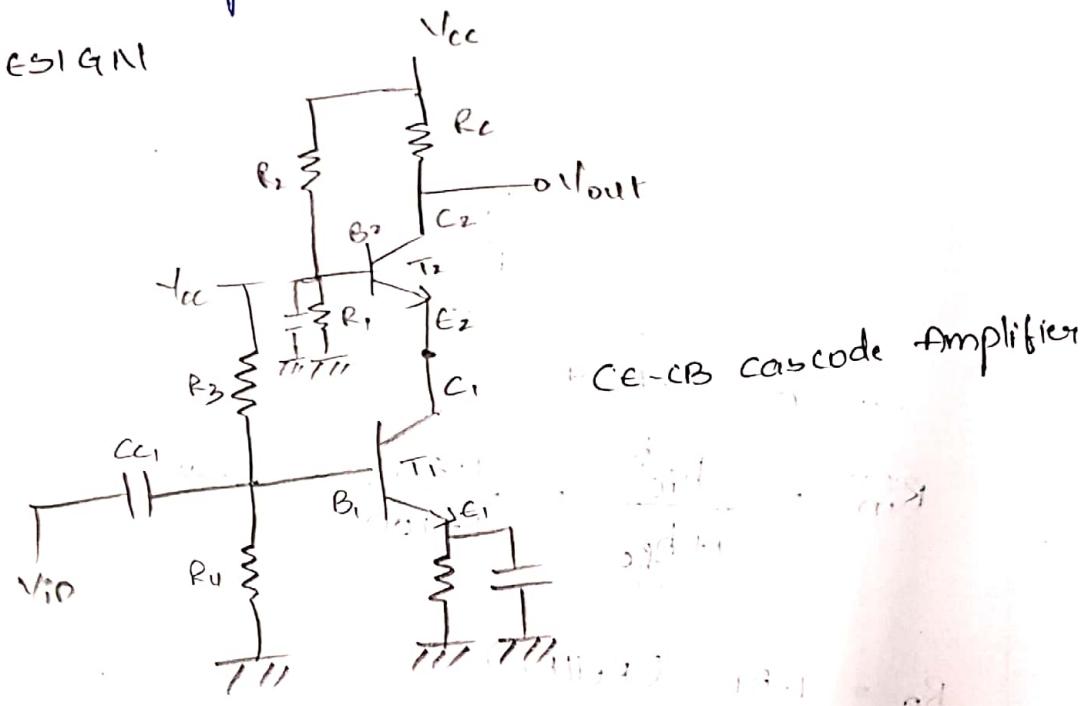
$$f_H = \frac{1}{2\pi R C_s(1-A)}$$

When we $\downarrow C_s(1-A)$ $f_H (\uparrow)$. So To $\uparrow f_H$, we $\downarrow A$ so that we can get good freq. response

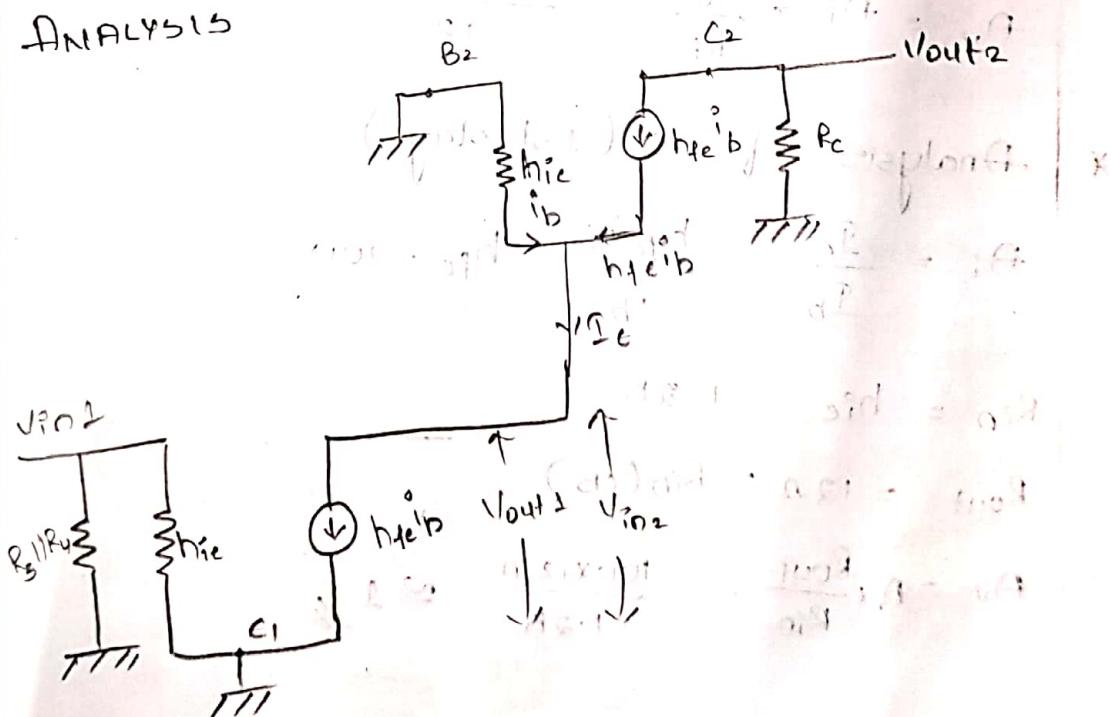
→ But $A = R_c/R_e \leftarrow \text{const.}$ so to $\downarrow A$ we have to $\downarrow R_c$

→ I_{ce} can replace I_{ce} with a circuit, which has low i/p resistance, so that I_{ce} can gain from the given configurations. I_{ce} have low i/p resistance for CB. So we construct CE followed by CB.

* DESIGN



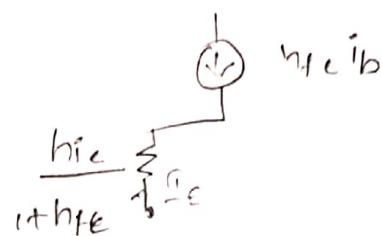
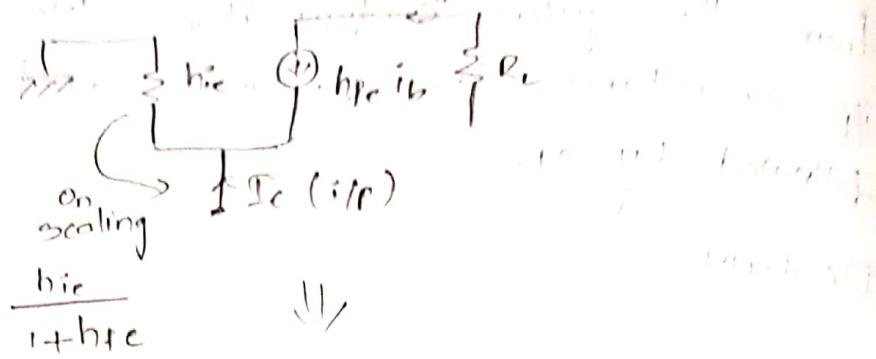
* ANALYSIS



→ Analysis of CB

$$A_i = \frac{I_c}{I_e} = \frac{(h_{fe})^m}{(1+h_{fe}) I_b} = \frac{h_{fe}}{1+h_{fe}} \approx 0.98$$

At R_{in} we have to see the resistance of the branch & ground. (h_{fe} & ground)



$$R_{in} = \frac{h_{ie}}{1+h_{fe}} = \frac{1.2K}{1+100} \approx 12\Omega$$

$$R_o = 1.5K \quad (R_L || R_C)$$

$$A_V = A_i \times \frac{R_o}{R_i} = \frac{0.98 \times 1.5K}{12} \approx 12.2$$

* Analysis of CE (1st stage)

$$A_i = \frac{I_c}{I_b} = \frac{h_{fe} i_b}{i_b} = h_{fe} = 100$$

$$R_{in} = h_{ie} = 1.2K$$

$$R_{out} = 12.2 = R_{in}(CB)$$

$$A_V = A_i \times \frac{R_{out}}{R_{in}} = \frac{100 \times 12.2}{1.2K} \approx 1$$

* Miller effect

At higher cut frequencies roll off occurs due to shunt capacitances. This is called miller effect.

Overall effect

$$\Delta V = \Delta V_1 \times \Delta V_2 = 1 \times 122 = 122$$

$$A_i = A_{i1} \times A_{i2} = (100)(0.78) = 78 \approx 100$$

$$R_{in} = R_{in}(ce) (\because i/p is ce) = 1.2K$$

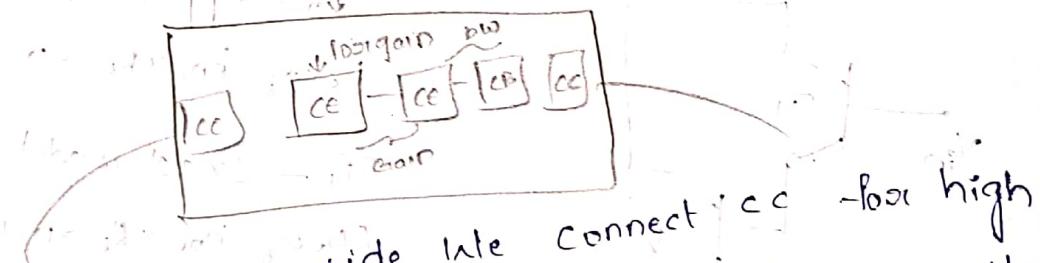
$$R_{out} = R_{out}(CB) (\because o/p is CB) = 1.5K (\text{or } R_L)$$

\therefore All the parameters are good for ce-CB amplifiers

* for approx. h-parameter model

$$\text{if, } h_{oe} \times R_L < 0.1$$

\rightarrow for CC-CC $h_{oe}R_L$ is not less than 1 so we use exact h-parameter model. esp. in public addressing stages

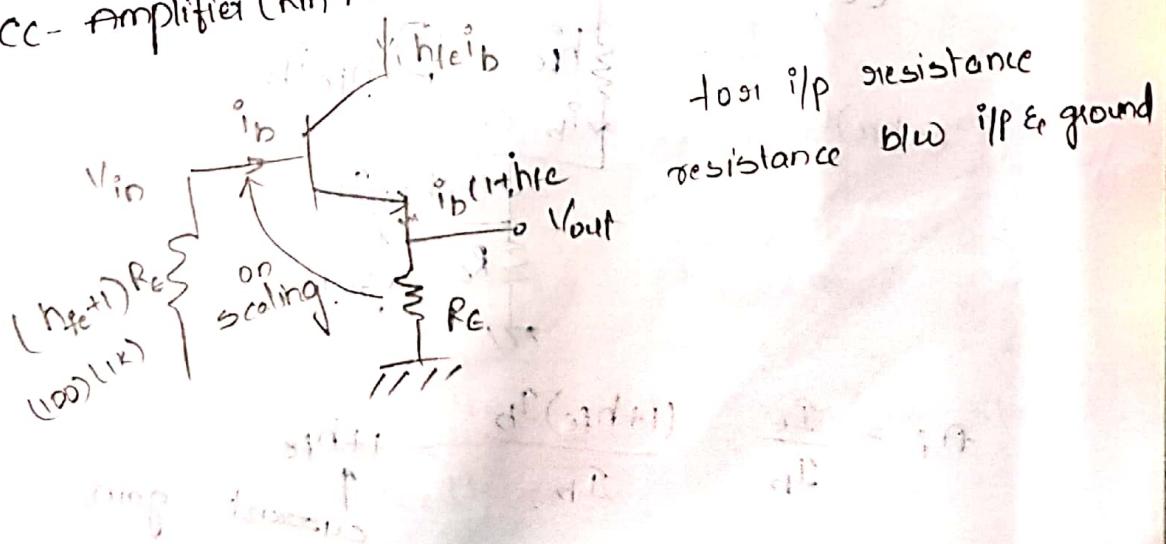


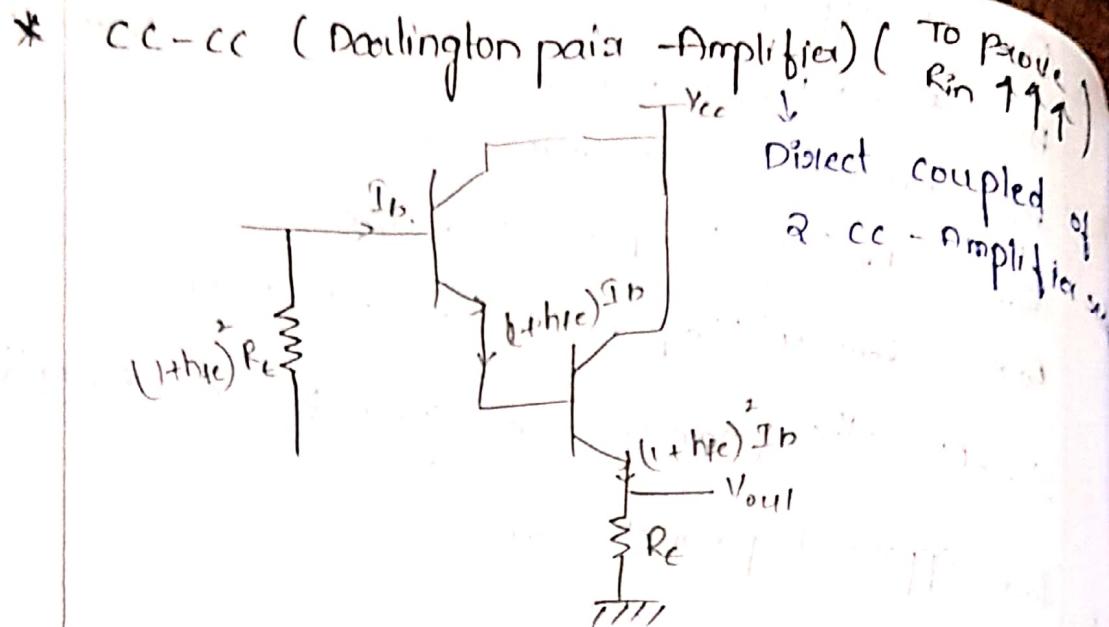
\rightarrow i/p side & o/p side late connect cc -> high i/p resistance & low o/p resistance for an voltage amplifier.

\rightarrow late add cc-cc to get high i/p resistance.

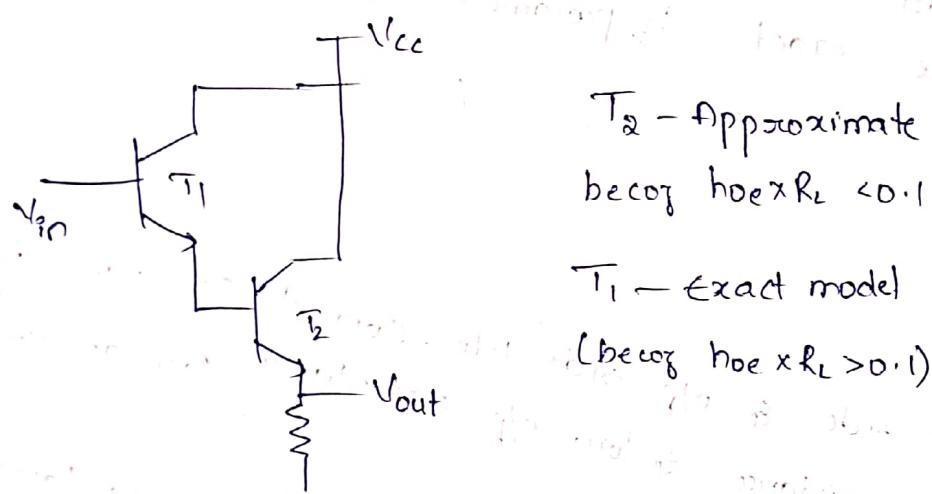
* High i/p resistance Amplifier.

CC-Amplifier ($R_{in} \uparrow$)

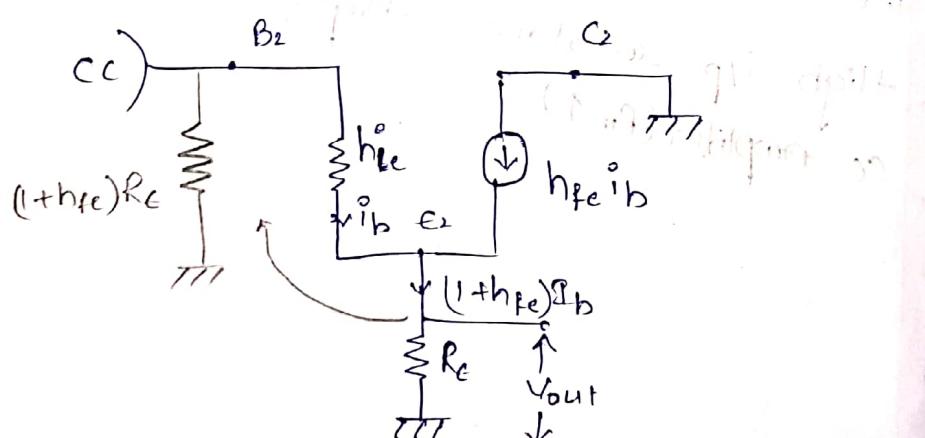




For maintaining the current const (I_b)
 the resistance are scaled by the factor of $(1+h_{fe})$
 at the i/p side.



* Approximate h-parameter for T₂ (2nd stage)



$$A_i = \frac{I_e}{I_b} = \frac{(1+h_{fe})I_b}{I_b} = 1+h_{fe}$$

↑ current gain

$$R_{in} = h_{ie} + (1+h_{fe}) R_c \approx (1+h_{fe}) R_c \quad (\text{Current gain factor})$$

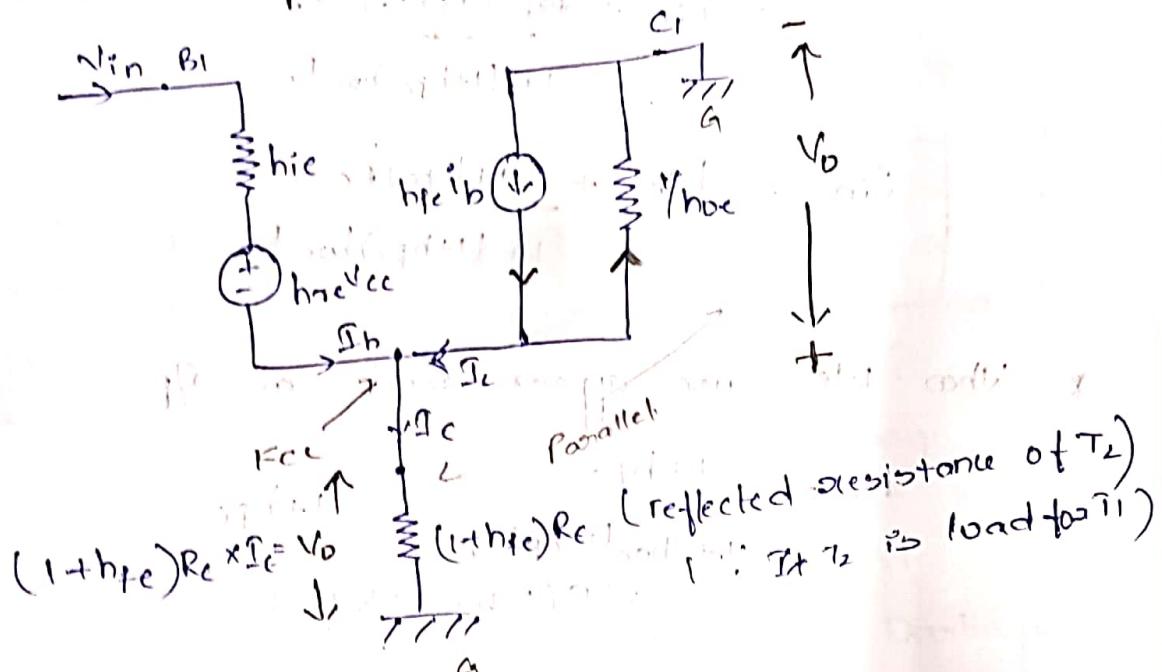
Reflected resistance at $i/p = A_i R_c$

Because of current gain pull in reflected
gain pull side.

if Current gain to increase

R_{in}

* Exact h-parameter form



A_i (current gain)

$$I_e = I_b + I_c$$

$I_e = I_b + (h_{fe} i_b + \text{current through } 'h_{oe})$

$$I_c = I_b + (h_{fe} i_b + \text{current through } 'h_{oe})$$

(V_{out} is V_{hoe})

$$R = (1+h_{fe}) I_c R_{hoe}$$

$$I_c = I_b + h_{fe} I_b - (1+h_{fe}) I_c R_{hoe}$$

$$I_b + h_{fe} I_b = (1+h_{fe}) I_c R_{hoe} + I_e$$

$$I_b (1+h_{fe}) = I_c (1 + (1+h_{fe}) R_{hoe})$$

$$\left\{ \frac{I_c}{I_b} = \frac{1+h_{fe}}{1 + h_{oe}(1+h_{fe}) R_c} \right\} = A_i \text{ (for stage 1)}$$

* R_{in} (for stage - 1) \rightarrow I_B flows.

$I_B \rightarrow T_B$ flows.
Voltage source \rightarrow neglected.

$$R_{in} = h_{ie} + A_i R_e$$

$$= h_{ie} + A_i (1+h_{fe}) R_e \quad (\because A_i \propto I_B \propto (1+h_{fe}) e)$$

$$= h_{ie} + \frac{A_i (1+h_{fe})^2 R_e}{1+(1+h_{fe}) h_{oe} R_e}$$

$$R_{in} = h_{ie} + \frac{(1+h_{fe})^2 R_e}{1+(1+h_{fe}) h_{oe} R_e}$$

* When we use appox. mode at i/p,

$$A_i = \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe}) R_e} = 1+h_{fe} \\ \approx 0 \quad (\because h_{oe} = \frac{25 \mu A}{V})$$

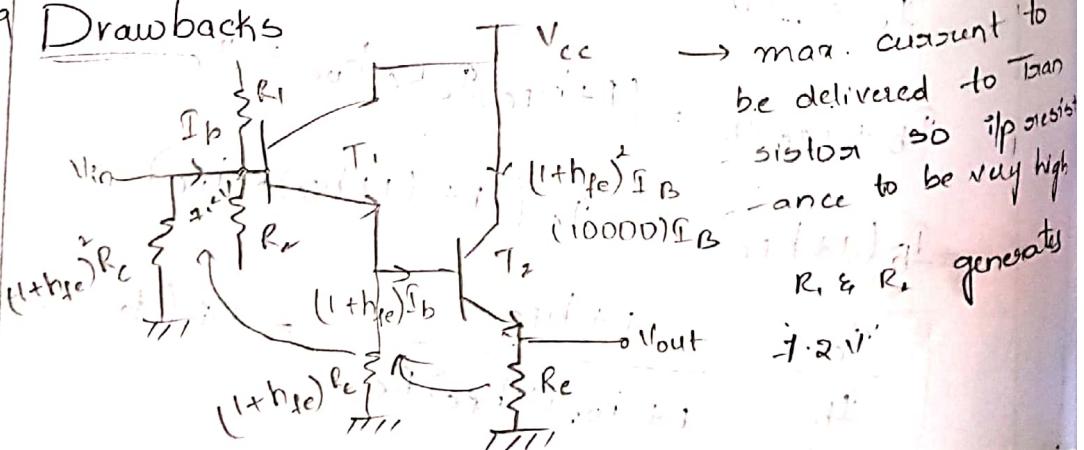
$$R_{in} = \frac{(h_{fe}+1)^2 R_e}{1+h_{oe}(1+h_{ie}) R_e} + h_{ie} \quad \text{neglected w.r.t } (1+h_{fe}) R_e$$

$$R_{in} = (1+h_{fe})^2 R_e \quad \text{(i/p resistance fed by darlington)}$$

$$\rightarrow A_i = A_1 \times A_2$$

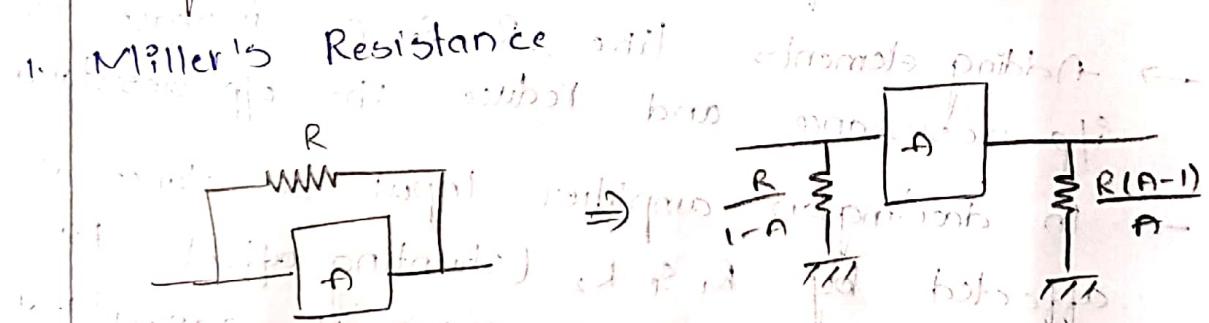
$$= (1+h_{fe})(1+h_{fe}) = (1+h_{fe})^2$$

30/12/19 Drawbacks



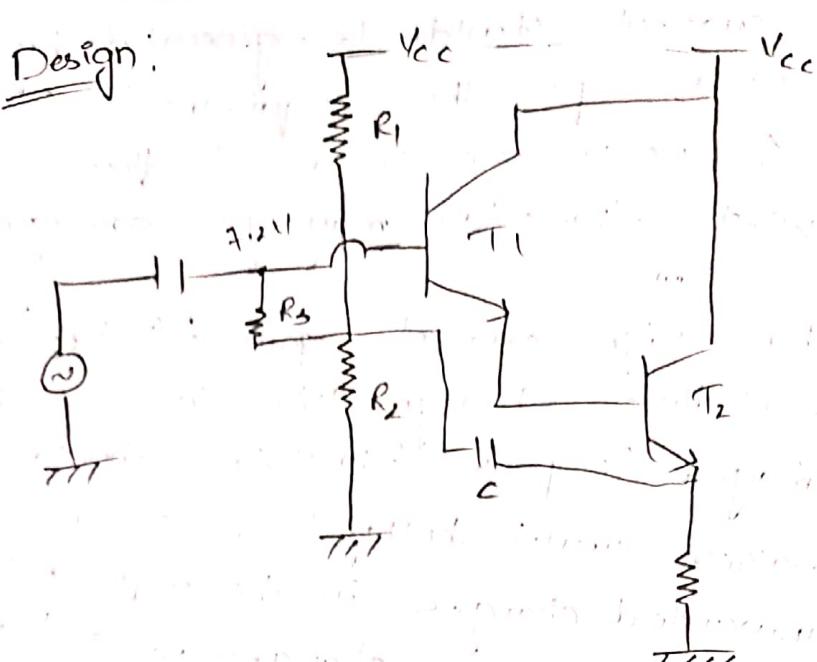
- Maximum current should be generated by the transistor (as per the requirements) so as current \uparrow (i.e. if excess current flows) temp \uparrow due to which transistor may get damaged
(or)
Circuit has high current gain ($(1+h_{fe})^2$) so max. current flows through transistor & it may get damaged. So power transistors should be used which makes circuit bulky.
- drift = unwanted changes in the opamp due to temp. variation (B, V_{BE} changes w.r.t temp)
due to direct coupling drift occurs here.
- There will be problem called shunting due to R_1 & R_2 resistors which are used for biasing. When R_1 & R_2 parallel with large input resistance, the total resistance will be reduced. This effect is called shunting effect.
To reduce the drawbacks due to Darlington we design another circuit Darlington + Bootstrap

Prerequisites for Miller's Bootstrap

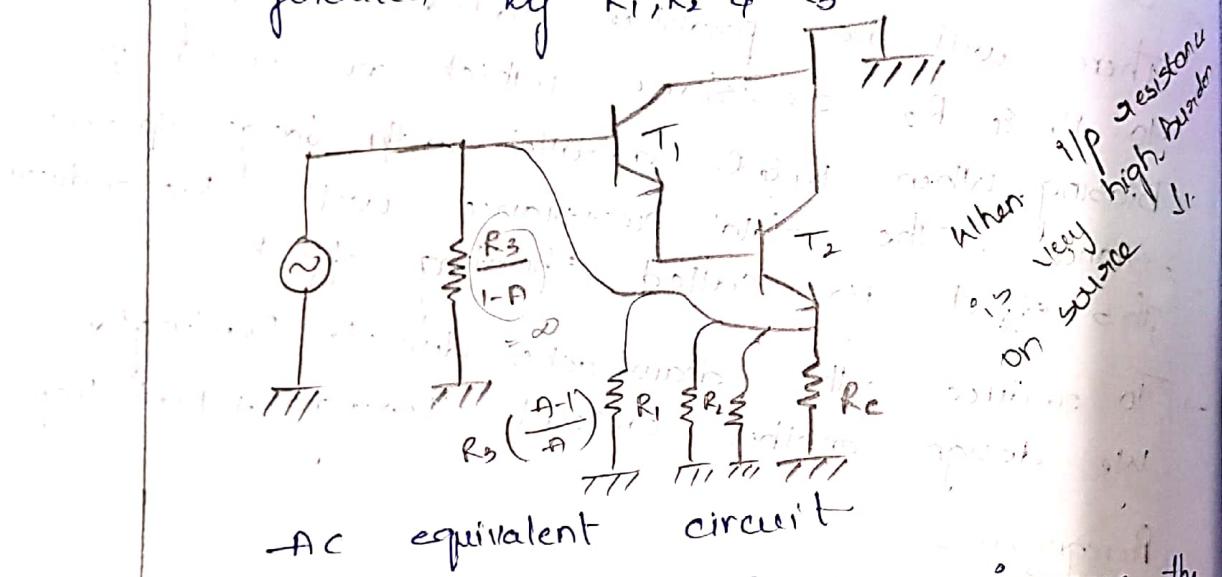


* Boot strap + Darlington
In darlington, we have shunting effect due to R_1 & R_2 . To eliminate that, we connect a resistor & a capacitor to the darlington amplifier so that it will not have shunting effect.

Design:



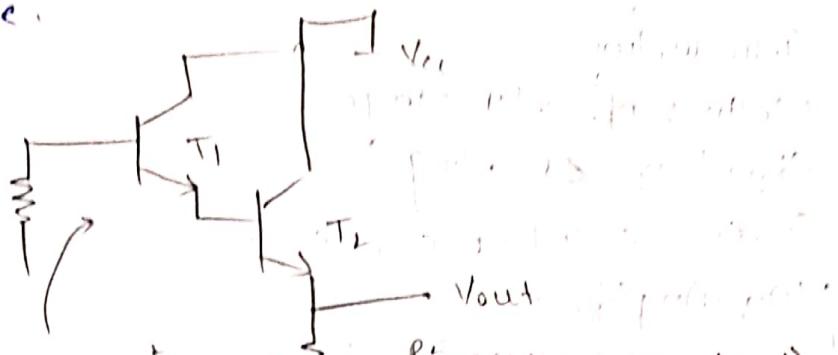
R_3 & C are connected here so that V_{o2} is generated by R_1, R_2 & R_3



AC equivalent circuit

- Adding elements like R_3 & C increase the i/p resistance and reduce the o/p resistance.
- In darlington amplifier Input resistance is affected by R_1 & R_2 (shunting effect) But when we add R_3 & C (branch capacitor) that effect is reduced & i/p resistance is not affected due to R_1 & R_2 (As $R_3/(A-1) \approx \infty$ ($A \approx 1$) The i/p resistance is not affected by R_1 & R_2 as R_1 & R_2 appear at o/p side as the capacitor is shunt circuit)

→ As R_o is branch resistance, By using Miller's theorem, we split it at i/p side.



$$R_{in} = \frac{h_{ie} + (1+h_{fe})R_c}{1+h_{oe}(1+h_{fe})R_c} \quad R_o = \frac{R_c || R_1 || R_2 || R_3 \left(\frac{n-1}{n}\right)}{A} + R_{out}$$

similar to darlington

- As $\frac{R_3}{1-n} \rightarrow \infty$ → the i/p resistance becomes very high as it is not affected by R_1 & R_2
- R_1 & R_2 appears at o/p side so the o/p resistance decreases further.

$$\begin{aligned} R_{in} &= h_{ie} + \frac{(1+h_{fe})^2 R_c}{1+h_{oe}(1+h_{fe})R_c} \\ &\approx (1+h_{fe})^2 R_c = (1+100)^2 \cdot 2.2K \\ &= 22000 \Omega \\ &\approx 22M\Omega \end{aligned}$$

$$R_o = R_c || R_1 || R_2 || R_3 \left(\frac{n-1}{n} \right)$$

$$= 2.2K || 1M\Omega || 600K || 1M \left(\frac{0.98-1}{0.98} \right)$$

$$R_o = \frac{1}{0.5 + 1/10M} = 218K \approx 1.975K\Omega$$

if bypass capacitors are present in series

then feedback is negative w.r.t. only emitters which forms positive feedback, so it increases the gain & reduces the output.

8/1/20

Unit - II

Multistage Amplifiers

Introduction

Methods of inter stage

Effect of cascading

CC-CC / CC-CB / CC-CE / CC-CC

MOS Amplifiers

Small signal model

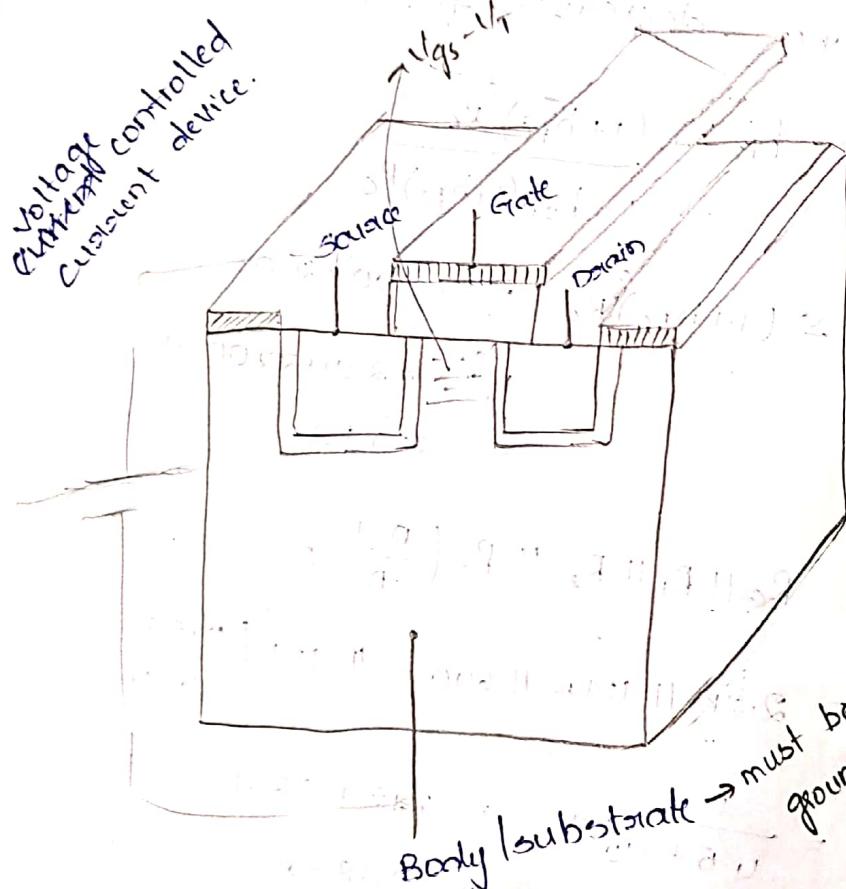
CG-3

CD-1

CG-1

* MOS small signal Model

Design of small signal model / linear model for MOS



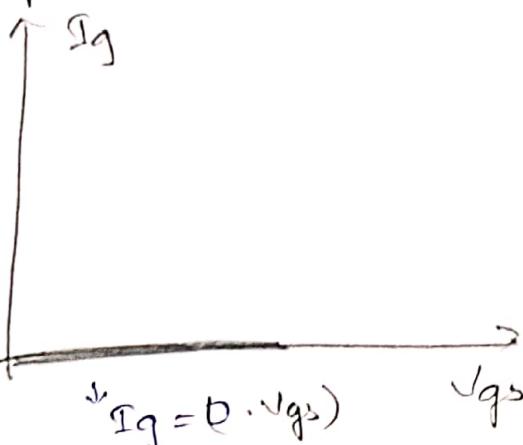
Source & drain are interchangeable

→ When we give voltage at Gate terminal ($> V_t$)
 V_t - Threshold Voltage, current starts flowing from drain to source. & channel is created.

→ When we apply voltage at drain & source, current flow starts increasing in the channel.

MOSFET

Input characteristics



$$g_m = \frac{\partial I_d}{\partial V_{gs}}$$

$$\boxed{I_d = g_m(V_{gs})}$$

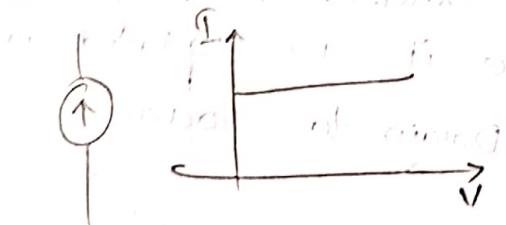


g_m - Transconductance. How much current should flow with respect to applied gate voltage of MOSFET.

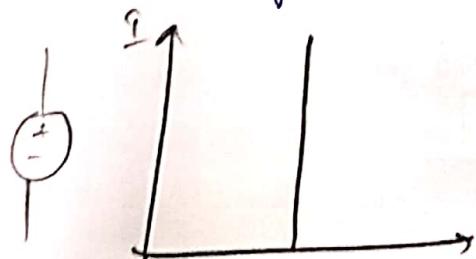
Very useful to applied input voltage of MOSFET make output current.

Characteristic Curves. (Pre-requisites)

1. Ideal current source

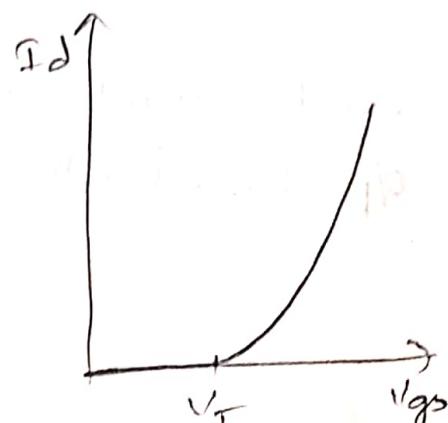


3. Ideal voltage source



(Const. voltage irrespective of current) for voltage source

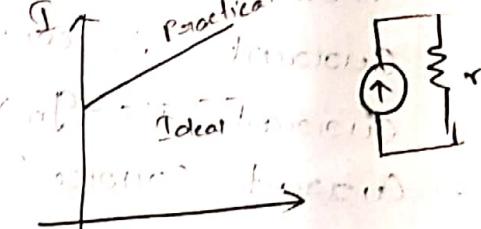
Transfer characteristics



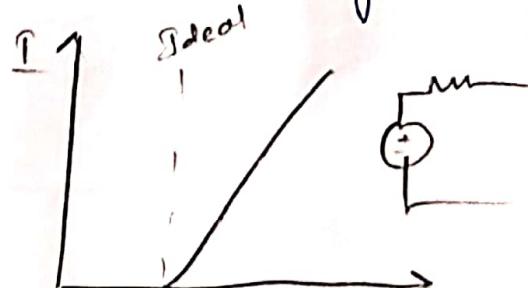
$$(\because y = m(x - x_0)^2)$$

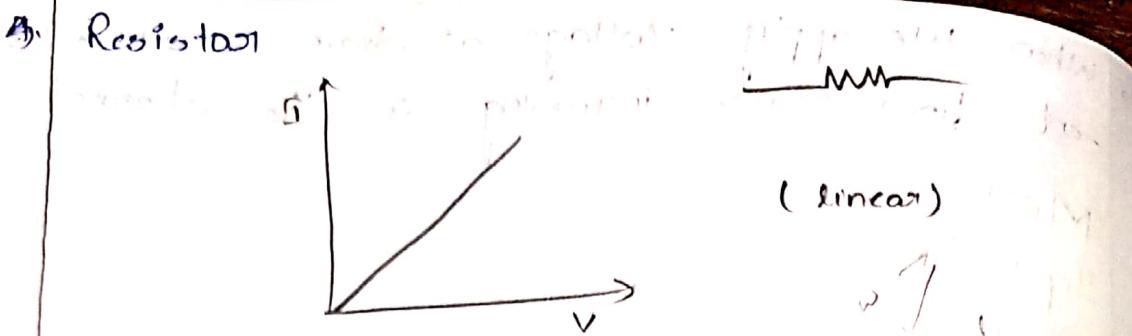
$$I_d = \frac{C_{ox} N}{2} (V_{gs} - V_T)^2$$

2. Practical current source



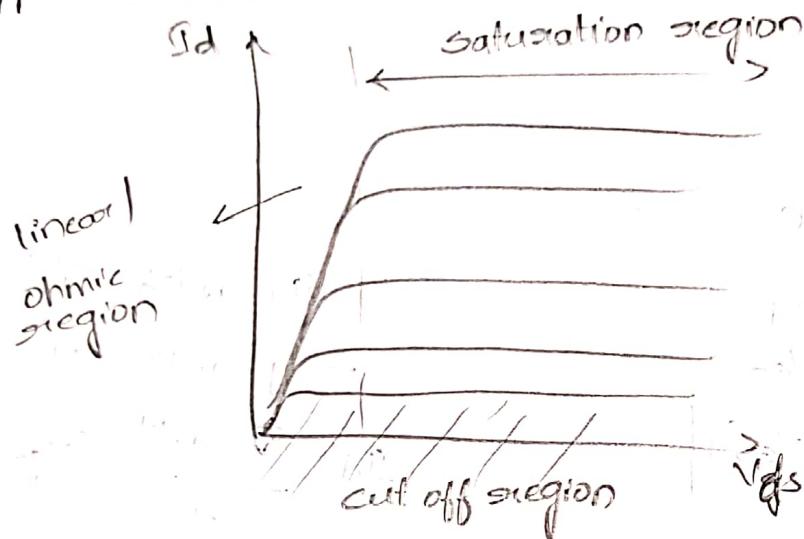
4. Practical voltage source





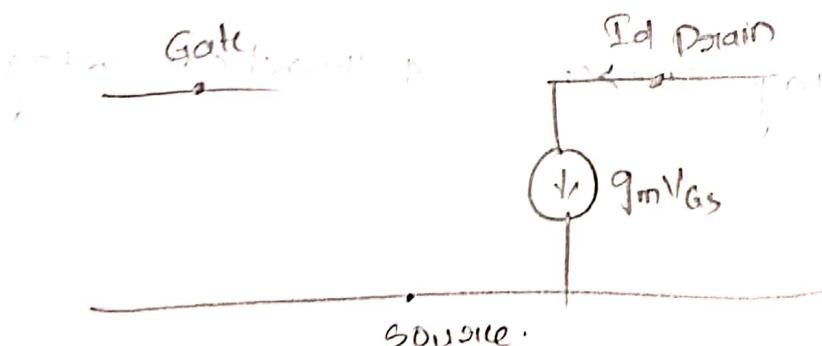
* Small signal model.

O/P characteristics



$$\text{WKT, } Id = g_m V_{GS}$$

- from Gate to Source terminal there is no flow of Gate current so infinite resistance is there at i/p so open circuit (from i/p char)
- from drain to source (from O/P characteristics) Current is const. in saturation region There current is $g_m V_{GS}$ so it is replaced with current source (from Drain to source)



Body

Cutoff - $(V_{GS} < V_T) \leq 0$ - no channel is formed
 \uparrow
 $(V_{GS} - V_T) > 0$ channel is formed

Saturation - $(V_{GS} - V_T) \leq V_{DS}$

When, $V_{DS} > (V_{GS} - V_T)$ channel length gets modulation which is called as channel length modulation

With the increase of drain voltage, drain current increases. This happens because with the increase of drain voltage, drain current increases. When the drain voltage is higher than the threshold voltage, then the drain current increases with the increase of drain voltage. This is called as channel length modulation. It is opposite to channel length modulation.

channel length modulation

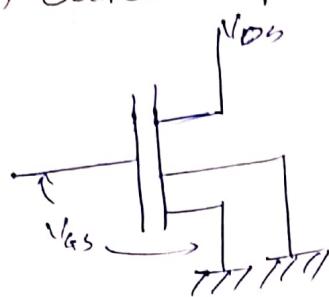
channel length modulation

61120

CS:

1. Resistive load
2. Current source load
3. Diode connected load

Common Source Amplifier

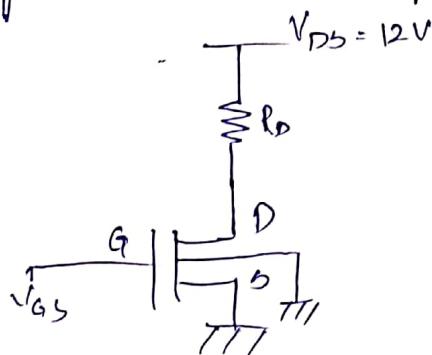


- Mosfet always expect $g_m V_{GS}$ current. If supply is strong enough to generate more than that current it has to operate in saturation region & it has to do amplification as per requirements.
- When more current flows near drain terminal more charge is accumulated near drain terminal which ↑ the drain voltage so V_{DS} is more than V_{GS} .

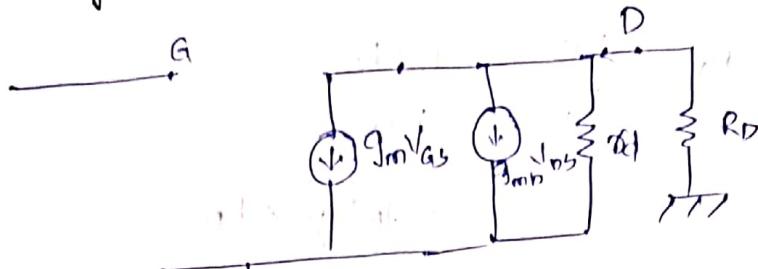
$$\therefore \text{When } (V_{GS} - V_T) < V_{DS}$$

↑
operates, saturation region

- When we ↑ V_{DS} , ↑ V_{GS} then it enters into linear region
- As $R_D = 0$, the output voltage = $R_D \times I = 0$ i.e no o/p voltage is generated at o/p. To get o/p voltage we have to place R_D



AC Analysis



Here, r_d is max ($r_d \gg R_D$) so current flows through R_D and also Body terminal is connected to ground so source & body are at same potential so we can neglect body effect.

WKT,

$$I_d = \frac{1}{2} \mu C_{ox} \left(\frac{w}{L} \right) (V_{GS} - V_T)^2 \quad (1)$$

$$g_m = \frac{\partial I_d}{\partial V_{GS}} = 2 \cdot \frac{1}{2} \mu C_{ox} \left(\frac{w}{L} \right) (V_{GS} - V_T) \quad (2)$$

$$(V_{GS} - V_T) = \sqrt{\frac{2 I_d}{\mu C_{ox} \frac{w}{L}}} \quad (3)$$

from (1) and (3)

$$(V_{GS} - V_T) = \sqrt{\frac{2 I_d}{\mu C_{ox} \frac{w}{L}}} \quad (3)$$

Replace (3) in (2) we get

$$g_m = \mu C_{ox} \frac{w}{L} \left(\sqrt{\frac{2 I_d}{\mu C_{ox} \frac{w}{L}}} \right)$$

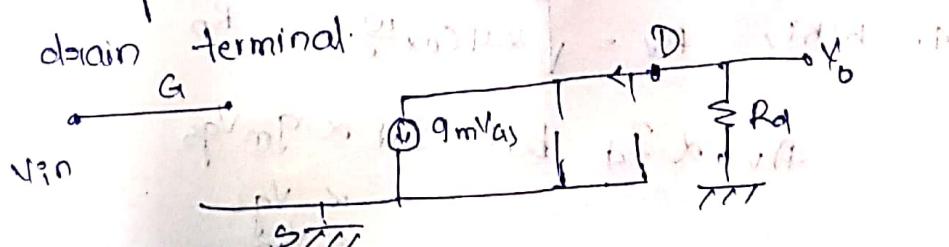
$$g_m = \sqrt{2 I_d \mu C_{ox} \frac{w}{L}}$$

From above equation we can say

$$\mu C_{ox} \left(\frac{w}{L} \right) = K_n$$

modulation is neglected when channel length is large.

We keep a resistive load with low resistance at drain terminal.



Voltage Gain: (A_V)

$$-A_V = \frac{V_O}{V_I} = \frac{g \times R_D}{V_{GS}}$$

$$= -\frac{g_m V_{GS} \times R_D}{V_{GS}}$$

$$\boxed{-A_V = -g_m R_D}$$

$$\boxed{-A_V = \sqrt{2 \mu C_{ox} \frac{W}{L} I_D \cdot R_D}}$$

if output gain depends
on drain voltage

Drawbacks: Process variable which changes w.r.t.
process

1. For Amplifier Gain to be max., To I_{GD} we have to $\uparrow R_D$ (or load resistance). When we $\uparrow R_D$ it will be comparable with R_D so we cannot neglect channel length modulation i.e. channel length modulation comes into picture when R_D is \uparrow .
2. When we $\uparrow R_D$, we cannot construct a circuit with more R_D i.e. we cannot fabricate it easily so circuit becomes bulky.
3. When $R_D \uparrow$, voltage drop across it \uparrow which \uparrow power dissipation $\rightarrow \uparrow$ heat
4. When $R_D \uparrow$, current that flows through drain terminal \downarrow than expected current ($g_m V_{GS}$) so the MOSFET enters into linear region from saturation region.

WKT, $A_V = \sqrt{2 \mu C_{ox} \frac{W}{L} I_D \cdot R_D}$

$A_V \propto I_D$ but $I_D \propto g_m V_{GS}$
 $\propto V_{GS}$

i.e. A_V is a process variable (i.e. which changes w.r.t. Process), Here overall gain depends on I/P voltage.

$$\text{Gain} \propto R_D^{-1}$$

for max. Gain - R_D to be ↑

Heat \downarrow Linearity \downarrow Channel length
Linearity \downarrow 2D rotation \downarrow modulation

Gain $\propto I_d$

$$I_d \propto g_m V_{GS}$$

$$\propto V_{GS}$$

\rightarrow $\propto V_{IN}$