四川大学期末考试试题（闭卷）

（2019~2020 学年第 2 学期）　　A 卷

课程号：311039030　课程名称：数字逻辑应用与设计　任课教师：李辉，应三丛，王艳

适用专业年级：软件工程 2019 级　学号：＿＿＿＿＿＿　姓名：＿＿＿＿＿＿

考生承诺

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

1、已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；

2、不带手机进入考场；

3、考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

考生签名：

题　号	一(10%)	二(50%)	三(40%)	四(0%)	五(0%)	六(0%)	七(0%)	八(0%)
得　分								
卷面总分			阅卷时间					

注意事项： 1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上；

2. **请将答案全部填写在本试题纸上；**

3. 考试结束，请将试题纸、添卷纸和草稿纸一并交给监考老师。

评阅教师	得分

一、填空题（本大题共 5 空，每空 2 分，共 10 分）。

a. $(100101)_2$=(　　)$_{10}$　b. $(59)_{10}$=(　　)$_2$　c. $(31.5)_{10}$=(　　)$_2$

d. $(1100111010000011)_2$=(　　)$_{16}$　e. $(35.9)_{10}$=(　　)$_{BCD}$

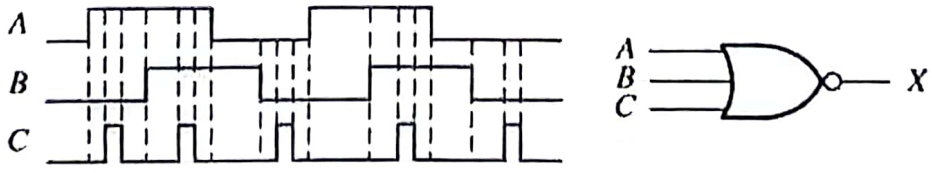
评阅教师	得分

二、计算题（本大题共 7 小题，共 50 分）。

1. Perform the indicated operations. Convert each decimal number into its corresponding 2s complement code prior to performing the indicated operation.(12 pts)

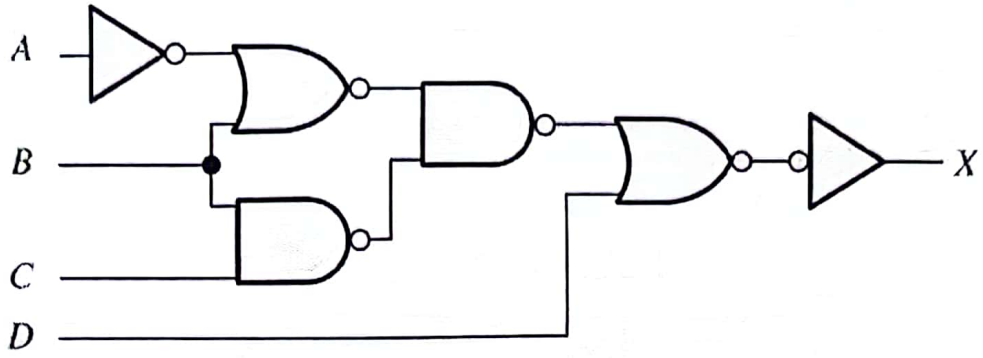
   a. (–10) + (–4)　b. (+15) + (–3)　c. (5) + (7)　d. (–19) + (–23)

2. Determine the output waveform in the following figure and draw the timing diagram.(3 pts)



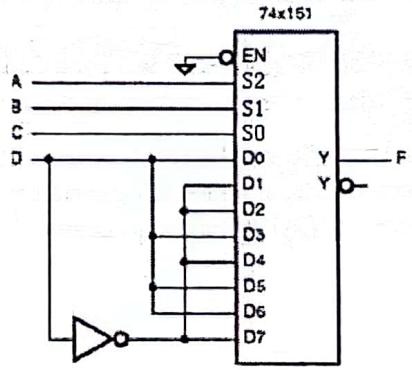
3. Simplify the following expressions using Karnaugh maps. (15 pts)
   a) f(A, B, C, D) = A'B'C'D'+A'B'C'D+ABCD+ABCD'
   b) f(X, Y, Z, W) = (X'+Y)(X'+Y'+Z')(Y+Z'+W)(X+Y'+Z+W')
   c) f(a, b, c, d) = $\sum m(5,6,7,8,9) + \sum d(10,11,12,13,14,15)$

4. Write the switching expressions for the following logic circuits and Simplify it. (5 pts)

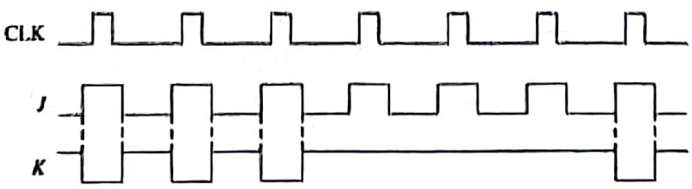


5. Realize the function shown below using a 3-8 decoder and the appropriate logic gates. (5pts)
   F(A, B, C) = AB'C'+AB'C+A'B'C

6. The circuit of the below realizes a combinational function F of four variable by the multiplexer-based circuit. Fill in the Karnaugh map and Write out the simplified SOP expression of the logic function F (5 pts)



7. Complete the negative edge-triggered J-K flip-flop timing diagram. Assume that Q is initially LOW(5 pts)

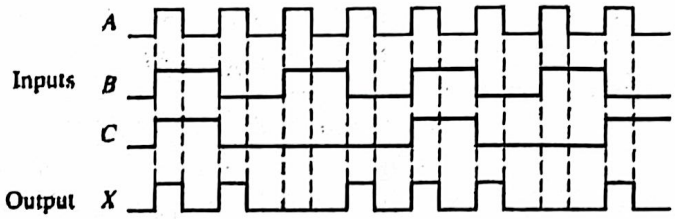


评阅教师	得分

三、分析设计题（本大题共4小题，共40分）。

1. (8 pts) Design a voting circuit in which three people vote (only approve and against), and when the majority (>=2) approves, the vote passes. (approve = 1, pass = 1). Design the circuit
   a) With NAND gates.
   b) With 3-to-8 decoder.
   c) With 4-1 multiplexer.

2. (8 pts)Given the input and output waveforms below, determine the logical circuit and implement it by using only NAND gates. Requires:(1)Write the logical expression in minimum SOP form.(2)Draw the logic diagram.



3. (12 pts)There are three indicator lights of red, yellow and blue, which are used to indicate the working states of three devices. When all three devices are working normally, the green light is on; when one device is faulty, the yellow light is on; when two devices are faulty, the red light is on; When the three devices fail at the same time, the yellow and red lights are on at the same time.
   a) Draw the truth table;
   b) Write the logic function expression that realizes the red, yellow and green lights
   c) Implement this circuit with 3-8 decoder and draw the logic circuit diagram.

4. (12 pts)Design a counter to produce the following binary sequence. Use J-K flip-flops. Requirements: (1) Draw the next state table, transition table, excitation table (2) Simplify the excitation equations with Karnaugh map (3) Draw the logic circuit diagram.

   1,4,3,5,7,6,2,1,...