四川大学期末考试试题（闭卷）

（2019~2020 学年第 1 学期）　　A 卷

课程号：311077030 课程名称：计算机组成和体系结构 任课教师：_____

适用专业年级：软件工程 2018 级 学号：_____ 姓名：_____

考生承诺

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

1、 已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；

2、 不带手机进入考场；

3、 考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

考生签名：

题　　号	一 (15%)	二 (15%)	三 (10%)	四 (10%)	五 (30%)	六 (20%)
得　　分						
卷面总分			阅卷时间			

注意事项： 1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上；

2. **请将答案全部填写在本试题纸上；**

3. 考试结束，请将试题纸、添卷纸和草稿纸一并交给监考老师。

评阅教师	得分

一、单项选择题.（本大题共 15 小题，每小题 1 分，共 15 分）

提示：在每小题列出的四个备选项中只有一个是符合题目要求的，请将其代码填写在下表中。错选、多选或未选均无分。

1	2	3	4	5	6	7	8	9	10
11	**12**	**13**	**14**	**15**					

1. （ ）There are _____ megabytes in a terabyte.

（A） 2^{10}

（B） 2^{20}

（C） 2^{30}

（D） 2^{40}

2. （ ）Suppose a system has a byte-addressable memory size of 256MB. How many bits are required for each address?

（A） 8

（B） 28

（C） 32

（D） 48

3. （ ）The equation below relates seconds to instruction cycles. What goes in the ???? space?

$$\text{CPU time} = \frac{\text{seconds}}{\text{program}} = \frac{\text{instructions}}{\text{program}} \times \frac{\text{????}}{\text{instruction}} \times \frac{\text{seconds}}{\text{cycle}}$$

（A） maximum bytes

（B） average bytes

（C） maximum cycles

（D） average cycles

4. （ ）Consider the postfix expression: A-B+C*(D*E-F)/(G+H*K). The equivalent postfix (reverse Polish notation) expression is:

（A） AB-C+DE*F-GH+K**/

（B） AB-CDE*F-*+GHK*+/

（C） ABC+-E*F-*+GHK*+/

（D） None of these

5. （ ）Examples of secondary memory include:

（A） ROM, PROM, and EROM

（B） main memory and cache

（C） magnetic disk drives and solid state memory

（D） optical jukeboxes and tape libraries

6. （ ）The average time required to reach a memory storage location and retrieve its contents is called:

（A） latency

（B） response time

（C） hit time

（D） effective access time

7. （ ）Cache mapping is necessary because:

（A） the address generated by the CPU must be converted to a cache location

（B） cache is so small that its use requires a map

（C） cache is larger than main memory and mapping allows us to store multiple copies of each piece of data from main memory

（D） none of the above

8. （ ）Disk and tape are forms of _____ storage.
   （A） durable
   （B） sequential
   （C） random
   （D） direct

9. （ ）A _____ is the smallest schedulable unit in a system.
   （A） thread
   （B） packet
   （C） segment
   （D） sector

10. （ ）The purpose of a TLB is:
   （A） to cache page table entries
   （B） to cache frequently used data from memory
   （C） to hold the starting address of the page table
   （D） to hold the length of the page table

11. （ ）The first general-purpose programmable electronic computer was the _____ .
   （A） ENIAC
   （B） IBM 650
   （C） Atanasoff-Berry computer
   （D） DEC PDP-1

12. （ ）The level of the computer hierarchy that is composed of gates and wires is the _____ .
   （A） control level
   （B） machine level
   （C） system software level
   （D） digital logic level

13. （ ）The _____ is the agreed-upon interface between all the software that runs on the machine and the hardware that executes it. It allows you to talk to the machine.
   （A） hardware protocol
   （B） software protocol
   （C） machine control architecture
   （D） instruction set architecture

14. （ ）Public-resource computing is also known as _____ computing.
   （A） global

（B） local

（C） static

（D） dynamic

15. （ ）The embedded systems programmer typically writes programs exclusively in _____ and does not have the luxury of after-the-fact performance tuning.

（A） assembly language

（B） machine language

（C） code language

（D） binary language

评阅教师	得分

二、判断题（本大题共 15 小题，每小题 1 分，共 15 分）

提示：正确打 T，错误打 F，将其结果填写在下表中。

1	2	3	4	5	6	7	8	9	10
11	**12**	**13**	**14**	**15**					

1. （ ）At its most basic level, a computer consists of only two parts: A processor and an I/O device.
2. （ ）MARIE has a common bus scheme, which means a number of entities share the bus.
3. （ ）One disadvantage to big endian representation is that most computers require words to be written on word address boundaries.
4. （ ）All cache mapping schemes require a main memory address to have an offset field.
5. （ ）The simplest way for a CPU to communicate with an I/O device is through polled I/O.
6. （ ）Fixed-length instructions always have the same number of operands.
7. （ ）Cylinders describe circular areas on each disk in Rigid Disk Drives.
8. （ ）Program instructions act on the data, unlike data-driven, or dataflow, architectures.
9. （ ）The disadvantage of RAID-1 is that it is costly and requires large memory space.
10. （ ）A branch instruction changes the flow of information by changing the PC.
11. （ ）The control level is above the machine level in the computer level hierarchy.

12. （ ）Cognitive computing can make inferences within a problem's context using hard facts and incomplete information.
13. （ ）Computer architecture encompasses all physical aspects of computer systems.
14. （ ）Channel I/O is a type of non-isolated I/O because the systems are equipped with separate I/O buses.
15. （ ）Embedded systems rarely use virtual memory.

评阅教师	得分

三、名词解释题（本大题共 5 小题，每小题 2 分，共 10 分）。

提示：解释每小题所给名词的含义，若解释正确则给分，若解释错误则无分，若解释不准确或不全面，则酌情扣分。

1. the three basic components of every computer

2. Indirect Addressing

3. Interrupts

4. Pipelining

5. the two types of cache write policies

评阅教师	得分

四、填空题（本大题共 10 空，每空 1 分，共 10 分）。

1. In the von Neumann architecture, the central processing unit (CPU) consists of registers, an arithmetic-logic unit (ALU), and a(n) _____.
2. List 3 addressing mode _____, _____, _____.
3. Name the four types of I/O architectures： _____, _____, _____, _____.
4. Flynn's taxonomy classifies computer architectures based on two properties. They are _____, _____.

评阅教师	得分

五、问答题（本大题共 6 小题，每小题 5 分，共 30 分）。

1. How does register addressing differ from direct addressing?

2. Assume a computer has 32-bit integers. Show how the value 0xCAFEBABE would be stored sequentially in memory, starting at address 0x100, on both a big endian machine and a little endian machine, assuming that each address holds one byte.

Address	Big Endian	Little Endian
0x100		
0x101		
0x102		
0x103		

3. Suppose we have a byte-addressable computer using fully associative mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 16 bytes, determine:

   a. the size of the offset field.

   b. the size of the tag field.

4. Consider a byte-addressable computer with 24-bit addresses, a cache capable of storing a total of 64K bytes of data, and blocks of 32 bytes. Show the format of a 24-bit memory address:

   a. if the computer uses direct mapping.

Tag	Block	Offset

   b. if the computer uses 4-way set associative mapping.

Tag	Set	Offset

5. Suppose we have the instruction LDA 800. Given memory as follows:

	Memory
800	900
…	
900	1000
…	
1000	500
…	
1100	600
…	
1200	800

What would be loaded into the AC if the addressing mode for the operand is:

   a. immediate_____

   b. direct _____

   c. indirect _____

6. Suppose we have a byte-addressable computer with a cache that holds 8 blocks of 4 bytes each. Assuming that each memory address has 8 bits,
   a. which cache block would the hexadecimal address 0x09 map if the computer uses direct mapping?
   b. which cache set would the hexadecimal address 0x1F map if the computer uses direct mapping?
   c. which cache set would the hexadecimal address 0x1F map if the computer uses 2-way set associative mapping?

评阅教师	得分

六、 计算题（本大题共 2 小题，每小题 10 分，共 20 分）。

1. Suppose we wish to evaluate the following expression:

   Z = (A * B) - (C / D)

   a. Convert the expression in postfix notation.
   b. Write a program to evaluate the above arithmetic statement using a stack organized computer with zero-address instructions (eg. add, subt, mult, devision instructions, and only pop and push can access memory).

2. Given a byte-addressable memory with 256 bytes, suppose a memory dump yields the results shown below. The address of each memory cell is determined by its row and column. For example, memory address 0x97 is in the 9th row, 7th column, and contains the hexadecimal value 43. Memory location 0xA3 contains the hexadecimal value 58.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	DC	D5	9C	77	C1	99	90	AC	33	D1	37	74	B5	82	38	E0
1	49	E2	23	FD	D0	A6	98	BB	DE	9A	9E	EB	04	AA	86	E5
2	3A	14	F3	59	5C	41	B2	6D	18	3C	9D	1F	2F	78	44	1E
3	4E	B7	29	E7	87	3D	B8	E1	EF	C5	CE	BF	93	CB	39	7F
4	6B	69	02	56	7E	DA	2A	76	89	20	85	88	72	92	E9	5B
5	B9	16	A8	FA	AE	68	21	25	34	24	B6	48	17	83	75	0A
6	40	2B	C4	1D	08	03	0E	0B	B4	C2	53	FB	E3	8C	0C	9B
7	31	AF	30	9F	A4	FE	09	60	4F	D7	D9	97	2E	6C	94	BC
8	CD	80	64	B3	8D	81	A7	DB	F1	BA	66	BE	11	1A	A1	D2
9	61	28	5D	D4	4A	10	A2	43	CC	07	7D	5A	C0	D3	CF	67
A	52	57	A3	58	55	0F	E8	F6	91	F0	C3	19	F9	BD	8B	47
B	26	51	1C	C6	3B	ED	7B	EE	95	12	7C	DF	B1	4D	EC	42
C	22	0D	F5	2C	62	B0	5E	DD	8E	96	A0	C8	27	3E	EA	01
D	50	35	A9	4C	6A	00	8A	D6	5F	7A	FF	71	13	F4	F8	46
E	1B	4B	70	84	6E	F7	63	3F	CA	45	65	73	79	C9	FC	A5
F	AB	E6	2D	54	E4	8F	36	6F	C7	05	D8	F2	AD	15	32	06

The system from which this memory dump was produced contains 4 blocks of cache, where each block consists of 8 bytes. Assume that the following sequence of memory addresses takes place: 0x2C, 0x6D, 0x86, 0x29, 0xA5, 0x82, 0xA7, 0x68, 0x80, and 0x2B.

a. How many blocks of main memory are there?

b. Assuming a direct mapped cache:

   i. Show the format for a main memory address assuming that the system uses direct mapped cache. Specify field names and sizes.

   ii. What does cache look like after the 10 memory accesses have taken place? Draw the cache and show contents and tags.

   iii. What is the hit rate for this cache on the given sequence of memory accesses?

c. Assuming a fully associative cache:

   i. Show the format for a main memory address. Specify field names and sizes.

   ii. Assuming that all cache blocks are initially empty, blocks are loaded into the first available empty cache location, and cache uses a first-in, first-out replacement policy, what does cache look like after the 10 memory accesses have taken place?

   iii. What is the hit rate for this cache on the given sequences of memory accesses?