

四川大学期中考试试题（闭卷）

Sichuan University Mid-term Test (Closed Book)

(2024 - 2025 学年 第 1 学期)

课程号: 311077030

课程名称: Computer Organization and Architecture

任课教师 Lecturer: Xuedong Yuan

考试时间 Time Period: 2 hours

适用专业年级: Software Engineering

姓名(Student Name):

Student Commitment

I have read and comprehended the "Regulations of Sichuan University on Examinations". I give my commitments as follows:

1. I have put prohibited stationary and exam-related items at designated area as required.
 2. I have not brought cell phone to the examination room.
 3. During the examination, I will comply with the above two provisions. If there is any violation, I agree to accept the punishments in accordance with the relevant provisions.

Signature:

题号	一(15%)	二(10%)	三(10%)	四(10%)	五(30%)	六(20%)
得分						
卷面总分		教师签名		阅卷时间		

注意事项: 1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上;

2. 请将答案全部填写在本试题纸上;
 3. 考试结束, 请将试题纸、添卷纸和草稿纸一并交给监考老师。

Notice: 1. Please write your student ID and your name in both exam papers and added answer papers precisely;

- 2. Please write all your answers on this exam paper;**

3. After the exam, please hand in exam paper, added answer sheet and scratch papers to examiners all together.

评阅教师	得分

一、单项选择题 Multiple choice, every question only has one right answer. (本大题共 15 小题, 每小题 1 分, 共 15 分)

提示: 在每小题列出的四个备选项中只有一个是符合题目要求的,请将其代码填写在下表中。错选、多选或未选均无分。

1. The computer component that makes sure that instructions are decoded and executed properly is the _____.

- A) arithmetic-logic unit
- B) control unit
- C) floating-point unit
- D) graphics processing unit

2. Software as a Service (SaaS) replaces the _____ of the computer hierarchy with an Internet-based application.

- A) digital logic level through user levels
- B) digital logic level through high-level language levels
- C) system software level through high-level language levels
- D) digital logic level through machine levels

3. If, after fetching a value from memory, we discover that the system has returned only half of the bits that we expected; it is likely that we have a problem with:

- A) the I/O bus
- B) the system bus
- C) byte alignment
- D) the control unit

4. Suppose that a 32MB system memory is built from 321MB RAM chips. How many address lines are needed to select one of the memory chips?

- A) 4
- B) 5
- C) 8
- D) 32

5. Consider the postfix expression: A-B+C*(D*E-F)/(G+H*K). The equivalent postfix (reverse Polish notation) expression is:

- A) AB-C+DE*F-GH+K**/
- B) AB-CDE*F-*+GHK*+/- C) ABC+-E*F-*+GHK*+/- D) None of these

6. The term endian refers to a computer architecture's:

- A) ability to complete arithmetic operations
- B) ability to find the end of variable length instructions
- C) byte order
- D) address modes

7. “Locality of reference” refers to:

- A) data always being in cache
- B) programs always referencing data in RAM
- C) clustering of memory references
- D) the requirement that forces us to use a large amount of expensive memory

8. Cache memory improves performance by improving memory _____ while virtual memory improves performance by increasing memory _____.

- A) execution time/access time
- B) locality/access time
- C) access time/address space
- D) organization/paging

9. The approach of using a combination of memory types to provide the best performance at the best cost is called:

- A) caching
- B) hierarchical memory
- C) solid state memory
- D) off-line memory

10. If a cache access requires one clock cycle and dealing with cache misses requires an additional five clock cycles, which of the following cache hit rates results in an effective access time of 2 clock cycles?

- A) 70%
- B) 80%
- C) 85%
- D) 90%

11. All of the following are cache replacement algorithms except:

- A) LRU
- B) FIFO
- C) random
- D) thrashing

12. A major advantage of direct mapped cache is its simplicity and ease of implementation.

The main disadvantage of direct mapped cache is:

- A) it is more expensive than fully associative and set associative mapping
- B) it has a greater access time than any other method
- C) its performance is degraded if two or more blocks that map to the same location are used alternately

- D) it does not allow the cache to store the tag that corresponds to the block currently residing in that cache location
13. Assuming an 8-bit virtual address with pages of 32 bytes, the virtual address format is:

- A) 5 bits for the page and 3 bits for the offset
 - B) 3 bits for the page and 5 bits for the offset
 - C) 8 bits for the page and 32 bits for the offset
 - D) 32 bits for the page and 8 bits for the offset
14. Engineers describe bus operation through clearer and precise pictures known as _____.

- A. timing diagrams
 - B. sequential diagrams
 - C. direct diagrams
 - D. circuit diagrams
15. If a system's instruction set consists of an 8-bit opcode, what is the maximum number of output signal lines required for the control unit?
- A) 8
 - B) 64
 - C) 128
 - D) 256

评阅教师	得分	二、判断题 True or False (本大题共 10 小题，每小题 1 分，共 10 分)									
		提示：正确打 T，错误打 F，将其结果填写在下表中。									
1	2	3	4	5	6	7	8	9	10		

1. () Peripheral Component Interconnect (PCI) is the recommended replacement for SATA (serial ATA).
2. () A program counter points to the memory address of the instruction that the CPU is currently executing.
3. () Little endian computers store a two-byte integer with the least significant byte at the lower address.
4. () Caching breaks down when programs exhibit good locality.
5. () When a computer uses paging, there must be a page table for every process.
6. () All cache mapping schemes require a main memory address to have an offset

field.

7. () A fixed-length instruction must have fixed-length opcodes.
8. () A Very Long Instruction Word (VLIW) is an architectural characteristic in which each instruction can specify multiple scalar operations.
9. () An assembler "assembles" assembly language into register transfer language (RTL).
10. () The control store for a hardwired control unit is implemented using ROM, EPROM, or PROM.

评阅教师	得分

三、判断改错题（本大题共 5 小题，每小题 2 分，共 10 分）。

提示：正确打√，错误打×，将其结果填写在下表中，并改正。

1	2	3	4	5

Identify the following register transfer statements (1-3) as legal or not legal for the datapath used in MARIE. If it is not legal, rewrite it as a sequence of microoperations to perform the indicated task.

1. $IR \leftarrow MAR$

改正：

2. $MBR \leftarrow AC$

改正：

3. $AC \leftarrow AC + MBR$

改正：

4. Not all cache mapping schemes require a main memory address to have an offset field.

改正：

5. One disadvantage to big endian representation is that most computers require words to be written on word address boundaries.

改正：

评阅教师	得分

四、填空题 Fill in the blanks（本大题共 15 空，每空 1 分，共 15 分）。

1. In the von Neumann architecture, the central processing unit(CPU) consists of _____, _____, _____ and a program counter.

2. List three main cache mapping schemes: _____, _____, _____.

Notice: Please write clearly and legibly. In total 09 pages, This is page

3. Memory segmentation can result in _____ fragmentation, while paging can result in _____ fragmentation.
4. Examples of secondary memory include: _____ and _____.
5. Clock skew is a problem for _____.
6. Computers designed using the _____ architecture have two buses: one for data and one for instructions.
7. There are three basic ISA architectures for internal storage in the CPU: _____, _____ and _____.

评阅教师	得分

五、简答题（本大题共 6 小题，每小题 5 分，共 30 分）。

1. Given the instruction set for MARIE:

Instruction Opcode	Instruction	Instruction Opcode	Instruction
0	JnS X	7	Halt
1	Load X	8	Skipcond (00 for AC<0, 01 for AC=0, 10 for AC>0)
2	Store X	9	Jump X
3	Add X	A	Clear
4	Subt X	B	Addl X
5	Input	C	Jumpl X
6	Output		

Write the assembly language equivalent for the machine instruction: 0011 000000000101

2. Assume a computer has 32-bit integers. Show how the value 0x0001122 would be stored sequentially in memory, starting at address 0x000, on both a big endian machine and a little endian machine, assuming that each address holds one byte.

Address	Big Endian	Little Endian
0x000		
0x001		
0x002		
0x003		

3. A nonpipelined system takes 300ns to process a task. The same task can be processed in a 5-segment pipeline with a clock cycle of 60ns. Determine the speedup ratio of the pipeline for 100 tasks.
 4. Consider a byte-addressable computer with 24-bit addresses, a cache capable of storing a total of 64K bytes of data, and blocks of 32 bytes. Show the format of a 24-bit memory address if the computer uses 4-way set associative mapping.
 5. Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.
 6. Suppose the cache access time is 10ns, main memory access time is 200ns, and the cache hit rate is 90%. Assuming parallel (overlapped) access, what is the average access time for the processor to access an item?

评阅教师	得分

六、设计、分析及非标准答案题 Design, analysis, and Open-answer questions (本大题共 3 小题, 1 题 4 分, 2 题 10 分, 3 题 6 分; 共 20 分)。

1. Convert the following expressions from infix to reverse Polish (postfix) notation. (8 points)

- a) $(5 \times (4 + 3)) \times 2 - 6$
- b) $X * Y + W * Z + V * U$
- c) $W * X + W * (U * V + Z)$
- c) $(W * (X + Y * (U * V))) / (U * (X + Y))$

2. **Cache design:** Assume the following cache/memory design: 16-bit addresses, byte-addressable, cache size is 256 bytes, block size is 8 bytes, tag size is 11 bits.

- a) What is the associativity of the cache? (Or answer the following two questions instead:
What type of mapping schemes should be used for this cache? please explain; If the N-way set associative cache mapping way is used, How many blocks are there in one set?)
- b) How many sets are in the cache?

Cache access time: Assume you have two cache designs, as described below:

<u>Cache A</u>	<u>Cache B</u>
1 MB L1 Cache	256 KB L1 Cache 768 KB L2 Cache
92% Hit Rate in L1	70% Hit Rate in L1 85% Hit Rate in L2
4 ns L1 access time	2 ns L1 Access Time 8 ns L2 Access Time
100 ns main memory access time	100 ns main memory access time

c) Calculate the average access time for Cache A.

d) Calculate the average access time for Cache B.

e) Which cache is faster?

3. Cache simulation

Assume a cache with the following configuration: total size is 1024 bytes, block size is 16 bytes, 4-way associative. The memory address size is 12 bits and is byte-addressable. Thus the partition of the address into tag, set index and offset is:

Tag	Set	Offset

What is the format of a memory address as seen by the cache? Fill in the blank.

For this problem we want to consider a MRU (most recently used) replacement policy, since we believe that LRU is overrated, particularly with iterations over large arrays.

Consider the stream of load instructions with the memory addresses shown in the table below. For each address, **indicate** the set number, whether the reference is a hit or miss, and the type of a miss (compulsory, conflict, capacity):

Address	Set Number	Hit or Miss	Compulsory	Conflict	Capacity
0x2AF					
0x224					
0x235					
0x531					
0x83C					
0x8A1					
0x93A					
0x2A2					
0x33A					
0x220					
0x23A					
0x23B					
0x33C					
0x931					

Tips: Three types of Missing in cache

'Compulsive': occurs during system startup. After resetting, the cache is empty.

'Capacity': The occurrence of 'Capacity' is due to the limited size of the cache.

'Conflict': is because different data blocks may share the same cache location.