四川大学期末考试试题（闭卷）

（2020~2021 学年第 1 学期）　　A 卷

课程号：311077030　课程名称：计算机组成和体系结构　任课教师：

适用专业年级：软件工程 2019 级　学号：　姓名：

考生承诺

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

1、 已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；

2、 不带手机进入考场；

3、 考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

考生签名：

题　　号	一 (15%)	二 (15%)	三 (10%)	四 (10%)	五 (30%)	六 (20%)
得　　分						
卷面总分			阅卷时间			

注意事项： 1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上；

2. **请将答案全部填写在本试题纸上；**

3. 考试结束，请将试题纸、添卷纸和草稿纸一并交给监考老师。

评阅教师	得分

一、单项选择题（本大题共 15 小题，每小题 1 分，共 15 分）

提示：在每小题列出的四个备选项中只有一个是符合题目要求的，请将其代码填写在下表中。错选、多选或未选均无分。

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

1. There are _____ kilobytes in an exabyte.

（A） 2^{10}

（B） 2^{30}

（C） 2^{50}

（D） 2^{70}

2. Which of the following is a computer that used second-generation (transistor) technology?

（A） IBM 360

（B） Atanasoff-Berry computer

（C） PDP-1

（D） Cray-1

3. Suppose that a 64MB system memory is built from 64 1MB RAM chips. How many address lines are needed to select one of the memory chips?
   （A） 6
   （B） 8
   （C） 32
   （D） 64

4. This bus arbitration method can cause throughput delays owing to bottlenecks in the selection process
   （A） distributed arbitration using self-selection
   （B） centralized parallel arbitration
   （C） daisy chain arbitration
   （D） distributed arbitration using collision detection

5. Which MARIE instruction is being carried out by the RTN that follows?

```
MAR ← X
MBR ← M[MAR]
MAR ← MBR
MBR ← AC
M[MAR] ← MBR
```

   （A） Store X
   （B） JnS X
   （C） Load X
   （D） StoreI X

6. Consider the postfix expression: A-B+C*(D*E-F)/(G+H*K). The equivalent postfix (reverse Polish notation) expression is:
   （A） AB-C+DE*F-GH+K**/
   （B） AB-CDE*F-*+GHK*+/
   （C） ABC+-E*F-*+GHK*+/
   （D） AB-CDE*F-GH+K**/

7. General-purpose architectures are divided into three groups:
   （A） memory-memory, register-memory, and load-store
   （B） stack addressing, accumulator addressing, and register addressing
   （C） Von Neumann, parallel, and quantum
   （D） Windows, Mac, and Linux

8. Consider the postfix (reverse Polish notation) 10 5 + 6 3 - /. The equivalent infix expression is:

（A） (10+5)/(6-3)

（B） (10+5)-(6/3)

（C） 10/5+(6-3)

（D） (10+5)-(6/3)

9. If the opcodes field for an instruction has *k* bits, that means there are _____ potential distinct operations

（A） 2*k*

（B） *k*/2

（C） 2^k

（D） k^2

10. Cache memory improves performance by improving memory _____ while virtual memory improves performance by increasing memory _____.

（A） execution time/access time

（B） locality/access time

（C） access time/address space

（D） organization/paging

11. Assuming an 8-bit virtual address with pages of 32 bytes, the virtual address format is:

（A） 5 bits for the page and 3 bits for the offset

（B） 3 bits for the page and 5 bits for the offset

（C） 8 bits for the page and 32 bits for the offset

（D） 32 bits for the page and 8 bits for the offset

12. Cache replacement policies are necessary:

（A） to determine which cache mapping policy to use

（B） to determine which block in cache should be the victim block

（C） to decide where to put blocks when cache is empty

（D） all of the above

13. The large computer systems use an intelligent type of DMA interface known as ___.

（A） memory I/O

（B） interrupt-driven I/O

（C） memory-mapped I/O

（D） I/O channel

14. There are two major parallel architectural paradigms, _____ and _____.

（A） Single multiprocessors (SMPs), massively parallel processors (MPPs)

（B） Symmetric multiprocessors (SMPs), multiple parallel processors (MPPs)

（C） Single multiprocessors (SMPs), multiple parallel processors (MPPs)

（D） Symmetric multiprocessors (SMPs), massively parallel processors (MPPs)

15. delays binding process; still, the process is actually running.

（A） Run-time binding

（B） Time binding

（C） Late binding

（D） Book binding

评阅教师	得分

二、判断题（本大题共 15 小题，每小题 1 分，共 15 分）

提示：正确打 T，错误打 F，将其结果填写在下表中。

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

1. Computer architecture encompasses all physical aspects of computer systems.
2. We can be certain that a megabyte always consists of 220 bytes.
3. In a pure load/store architecture, no instructions other than the load and store instructions are allowed to directly access memory.
4. A Very Long Instruction Word (VLIW) is an architectural characteristic in which each instruction can specify multiple scalar operations.
5. Accumulator architectures use sets of general purpose registers to store operands.
6. A unified cache is a cache that holds both data and instructions.
7. Caching breaks down when programs exhibit good locality.
8. I/O channels are driven by small CPUs called I/O processors (IOPs).
9. Cache memory has the shortest (fastest) access time.
10. Channel I/O is a type of non-isolated I/O because the systems are equipped with separate I/O buses.
11. When a computer uses paging, there must be a page table for every process.
12. If a system has a byte-addressable memory size of 256MB, 32bits are required for each address.
13. Labels is placed into the symbol table during the first pass.
14. A stack-organized computer uses indirect addressing.
15. To carry out a binary arithmetic operation, an accumulator architectures uses one operand.

评阅教师	得分

三、名词解释题（本大题共 5 小题，每小题 2 分，共 10 分）。

提示：解释每小题所给名词的含义，若解释正确则给分，若解释错误则无分，若解释不准确或不全面，则酌情扣分。

1. Register

2. ALU

3. RAID

4. Virtual address

5. Flynn's Taxonomy

评阅教师	得分

四、填空题（本大题共 10 空，每空 1 分，共 10 分）。

1. A terabyte represents what power of two?_____. A kilobyte represents what power of two? _____. A gigabyte represents what power of two? _____.
2. Computer chips having multiple processing units on a single chip are _____architectures.
3. List 3 addressing mode _____, _____, _____.
4. There are three basic forms of locality in memory access, they are_____, _____ and _____.

评阅教师	得分

五、问答题（本大题共 6 小题，每小题 5 分，共 30 分）。

1. What is the purpose of having various address modes?

2. Assume a computer has 32-bit integers. Show how the value 0x0001122 would be stored sequentially in memory, starting at address 0x000, on both a big endian machine and a little endian machine, assuming that each address holds one byte.

Address	Big Endian	Little Endian
0x000		
0x001		
0x002		
0x003		

3. Match the following:

_____ Holds data the CPU needs to process
_____ Holds next instruction to be executed
_____ Holds address of next instruction to be executed
_____ Holds memory address of data being referenced
_____ Holds data written from the keyboard
_____ Holds interrupt signals
_____ Holds data just read from memory

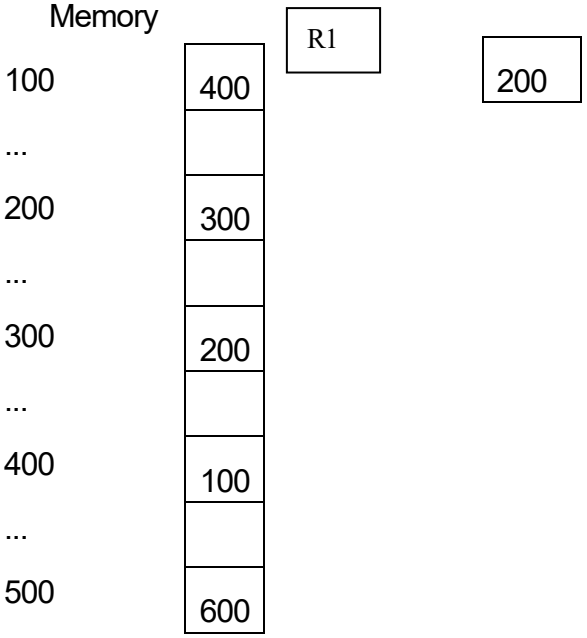
A. Instruction Register
B. Program Counter
C. Accumulator
D. Memory Address Register
E. Input Register
F. Memory Buffer Register
G. Flag Register

4. Suppose we have a byte-addressable computer with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes:

   a. Show the format of memory address if the computer uses direct mapping.

   b. Show the format of memory address if the computer uses 2-way set associative mapping.

5. Suppose we have the instruction Load 100. Given that memory and register R1 contain the values below:



Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	
Direct	
Indirect	
Indexed	

6. Suppose the cache access time is 10ns, main memory access time is 200ns, and the cache hit rate is 90%. Assuming parallel (overlapped) access, what is the average access time for the processor to access an item?

评阅教师	得分

六、计算题（本大题共 3 小题，1 题 8 分，2 题 10 分，3 题 2 分；共 20 分）。

1. Suppose we have 1Gx16 RAM chips that make up a 32Gx64 memory that uses high interleaving. (Note: This means that each word is 64 bits in size and there are 32G of these words.) (8 points)
   a) How many RAM chips are necessary?
   b) Assuming 4 chips per bank, how many banks are required?
   c) How many lines must go to each chip?
   d) How many bits are needed for a memory address, assuming it is word addressable?
   e) For the bits in part d), draw a diagram indicating how many and which bits are used for chip select, and how many and which bits are used for the address on the chip.
   f) Redo this problem assuming low order interleaving is being used instead.
   g) Where would address 11 (which is B in hex) be located(Which bank)?
   h) If low-order interleaving is used, where would address 11 (which is B in hex) be located(Which bank)?

2. Suppose we have a computer that uses a memory address word size of 8 bits. This computer has a 16-byte cache with 4 bytes per block.

The computer accesses a number of memory locations throughout the course of running a program. The system accesses memory addresses in this exact order: 0x6E, 0xB9, 0x17, 0xE0, 0x4E,0x4F, 0x50, 0x91, 0xA8, 0xA9, 0xAB, 0xAD, 0x93, and 0x94.

The memory addresses of the first **four accesses** have been loaded into the cache blocks as shown below. (The contents of the tag are shown in binary and the cache "contents" are simply the address stored at that cache location.) (10 points)

	Tag Contents	Cache Contents (represented by address)
Block 0	1110	0xE0
		0xE1
		0xE2
		0xE3

	Tag Contents	Cache Contents (represented by address)
Block 1	0001	0x14
		0x15
		0x16
		0x17

Block 2	1011	0xB8
		0xB9
		0xBA
		0xBB

Block 3	0110	0x6C
		0x6D
		0x6E
		0x6F

Suppose this computer uses direct-mapped cache.

a. Draw a diagram indicating the format for a main memory address. Specify field names and sizes.
b. What is the hit ratio for the entire memory reference sequence given above, assuming we count the first four accesses as misses?
c. What memory blocks will be in the cache after the last address has been accessed?

3. The average memory access time for a microprocessor with 1 level of cache is 2.4 clock cycles

- If data is present and valid in the cache, it can be found in 1 clock cycle
- If data is not found in the cache, 80 clock cycles are needed to get it from off-chip memory

Designers are trying to improve the average memory access time to obtain a 65% improvement in average memory access time, and are considering adding a 2nd level of cache on-chip.

- This second level of cache could be accessed in 6 clock cycles
- The addition of this cache does not affect the first level cache's access patterns or hit times
- Off-chip accesses would still require 80 additional clock cycles.

To obtain the desired speedup, how often must data be found in the 2nd level cache（the L2 hit rate）? (2 points)