

# 四川大学期末考试试题（闭卷）

(2018–2019 学年第 1 学期)

A 卷

课程号: 311077030、314056030 课程名称: 计算机组成和体系结构 任课教师: \_\_\_\_\_

适用专业年级: 软件工程 2017 级、网络安全 2017 级 学号: \_\_\_\_\_ 姓名: \_\_\_\_\_

## 考生承诺

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

- 1、已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；
- 2、不带手机进入考场；
- 3、考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

考生签名:

题号	一(30%)	二(10%)	三(36%)	四(24%)
得分				
卷面总分		阅卷时间		

注意事项: 1. 请务必将本人所在学院、姓名、学号、任课教师姓名等信息准确填写在试题纸和添卷纸上；  
2. 请将答案全部填写在本试题纸上；  
3. 考试结束，请将试题纸、添卷纸和草稿纸一并交给监考老师。

评阅教师	得分

## 一、填空题（本大题共 15 空，每空 2 分，共 30 分）。

1. The main functions of the CPU is \_\_\_\_\_.
2. (共 4 分) For a memory space which has  $4M \times 32$  bits, \_\_\_\_\_ bits of the address should be if the memory is byte-addressable, \_\_\_\_\_ bits of the address if it is word-addressable.
3. (共 6 分) There are three basic forms of locality in memory access, they are \_\_\_\_\_, \_\_\_\_\_ and \_\_\_\_\_.
4. (共 4 分) Given a memory of 8M bytes consisting of several  $128K \times 8$  RAM chips, and assuming byte-addressable memory, the correct way is using \_\_\_\_\_ bits for chip select and \_\_\_\_\_ bits for address on chip.
5. What unit is typically used to measure the speed of a computer clock \_\_\_\_\_.
6. Virtual memory can be implemented with different techniques, including: \_\_\_\_\_, \_\_\_\_\_, \_\_\_\_\_.
7. List the three fields in a set associative cache address \_\_\_\_\_, \_\_\_\_\_, \_\_\_\_\_.



评阅教师	得分

## 二、判断题（本大题共 5 小题，每小题 2 分，共 10 分）

提示：正确打√，错误打×，将其结果填写在下表中。

1	2	3	4	5

- (共 2 分) The Principle of Equivalence of Hardware and Software says that hardware and software are basically equivalent, and implementations done via either method will run at the same speeds.
- (共 2 分) Amdahl's Law states that the performance enhancement possible with a given improvement is limited by the amount that the improved feature is used.
- (共 2 分) A branch instruction changes the flow of information by changing the PC.
- (共 2 分) MARIE has a common bus scheme, which means a number of entities share the bus..
- (共 2 分) A fixed length instruction must have a fixed length opcode.

评阅教师	得分

## 三、问答题（本大题共 6 小题，共 46 分）。

- (共 4 分) Write down the characteristics present in a von Neumann architecture.

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- (共 4 分) What is an address mode? List five types of address mode.



3. (共 4 分) What are the advantages and disadvantages of fixed-length and variable-length instructions? Which is currently more popular?

4. (1) (4 分) Explain how programmed I/O is different from interrupt-driven I/O.

(2) (2 分) How does direct memory access (DMA) work?

5. (共 4 分) Discuss the advantages and disadvantages of dynamic linking.



## 6. (共 4 分) Explain the functions of the following codes . (4 分)

Address	Instruction	Comments
100	Load Addr	
101	Store Next	
102	Load Num	
103	Subt One	
104	Store Ctr	
105	Clear	
Loop,	106 Load Sum	
107	AddI Next	
108	Store Sum	
109	Load Next	
10A	Add One	
10B	Store Next	
10C	Load Ctr	
10D	Subt One	
10E	Store Ctr	
10F	Skipcond 00 /If control variable < 0, skip next instruction	
110	Jump Loop	
111	Halt	
Addr,	112 Hex 118	
Next,	113 Hex 0	
Num,	114 Dec 7	
Sum,	115 Dec 0	
Ctr,	116 Hex 0	
One,	117 Dec 1	
	118 Dec 12	
	119 Dec 15	
	11A Dec 10	
	11B Dec 18	
	11C Dec 25	
	11D Dec 13	
	11E Dec 20	



7. (共 6 分) Convert the following expressions from infix to reverse Polish (postfix) notation.

- a)  $X \times Y + W \times Z + V \times U$
- b)  $W \times X + W \times (U \times V + Z)$
- c)  $(W \times (X + Y \times (U \times V))) / (U \times (X + Y))$

8. (共4分) Suppose we have the instruction Load 500. Given that memory and register R1 contain the values below:

Memory

500	700	R1	400
700			
900	1200		
1100			
1300	1300		
500			
900			

Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	/
Direct	
Indirect	
Indexed	



评阅教师	得分

**四、计算题（本大题共 2 小题，共 24 分）。**

1. (共14分) Suppose that a  $4M * 16$  main memory is built using  $256KB * 8$  RAM chips and memory is word-addressable.
  - a) How many RAM chips are necessary?
  - b) How many RAM chips are there per memory word?
  - c) How many address bits are needed for each RAM chip?
  - d) How many banks will this memory have?
  - e) How many address bits are needed for all of memory?
  - f) If high-order interleaving is used, where would address  $63_{10}$  be located?
  - g) Repeat Exercise for low-order interleaving.
2. (共10分) A 2-way set associative cache consists of four sets. Main memory contains  $4K$  blocks of eight words each.
  - a) Show the main memory address format that allows us to map addresses from main memory to cache. Be sure to include the fields as well as their sizes.
  - b) Compute the hit ratio for a program that loops 4 times from locations 11 to 69 in main memory.

