Exam Bank Chapter 1 – Null & Lobur 4th ed.

Multiple Choice

1. Suppose someone writes a program to find the perfect solution to a problem, but it will take 150 years to run. We say that this particular solution is:
A) computationally infeasible
B) an infinite loop
C) computationally tenable
D) NP complete

Answer: A
Topic: Overview
Difficulty: Easy
Page: 1

2. We study computer _____ to become familiar with how circuits and signals collaborate to create working computer systems.
A) architecture
B) organization
C) layers
D) programming

Answer: B
Topic: Overview
Difficulty: Easy
Page: 2

3. Computer _____ concerns itself with instruction sets and formats, operation codes, data types, the number and types of registers, addressing modes, main memory access methods, and various I/O mechanisms.
A) layers
B) architecture
C) organization
D) programming

Answer: B
Topic: Overview
Difficulty: Easy
Page: 2

4. The _____ is the agreed-upon interface between all the software that runs on the machine and the hardware that executes it. It allows you to talk to the machine.
A) hardware protocol
B) software protocol
C) machine control architecture
D) instruction set architecture

Answer: D
Topic: Overview
Difficulty: Easy
Page: 2

5. There are _____ megabytes in a terabyte.
A) 2^{10}
B) 2^{20}
C) 2^{30}
D) 2^{40}

Answer: B
Topic: An Example System
Difficulty: Medium
Page: 5

6. There are _____ kilobytes in an exabyte.
A) 2^{20}
B) 2^{30}
C) 2^{40}
D) 2^{50}

Answer: D
Topic: An Example System
Difficulty: Medium
Page: 5

7. Clock speeds in today's microprocessors are measured in _____ .

A) kilohertz
B) megahertz
C) gigahertz
D) terahertz

Answer: C
Topic: An Example System
Difficulty: Easy
Page: 8

8. Many desktop computers utilize the _____ bus standard in which the system augments its main bus with dedicated I/O buses using expansion slots.
A) enhanced integrated bus
B) serial advanced technology attachment
C) universal serial bus
D) peripheral component interconnect

Answer: D
Topic: An Example System
Difficulty: Medium
Page: 12

9. _____ allow movement of data to and from devices external to the computer.
A) ports
B) system buses
C) monitors
D) scanners

Answer: A
Topic: An Example System
Difficulty: Easy
Page: 12

10. The organization that sets standards for computer components, signaling protocols, and data representation is the:
A) ISO
B) IEEE
C) CCITT

D) ANSI

Answer: B
Topic: Standards Organizations
Difficulty: Easy
Page: 18

11. The organization that sets standards for photographic film and the pitch of screw threads, in addition to matters concerning computers, is the:
A) ISO
B) IEEE
C) CCITT
D) ANSI

Answer: A
Topic: Standards Organizations
Difficulty: Easy
Page: 18

12. The mechanical computer that included mechanisms that provided memory and an arithmetic processing unit was the:

A) Pascaline
B) Difference Engine
C) Atanasoff-Berry Computer
D) von Neumann calculator

Answer: B
Topic: Historical Development
Difficulty: Medium
Page: 20

13. The first completely electronic computer was the _____ .
A) ENIAC
B) Analytical Engine
C) Atanasoff-Berry Computer
D) DEC PDP-1

Answer: C

Topic: Historical Development
Difficulty: Easy
Page: 23

13. The first general-purpose programmable electronic computer was the _____ .
A) ENIAC
B) IBM 650
C) Atanasoff-Berry computer
D) DEC PDP-1

Answer: A
Topic: Historical Development
Difficulty: Easy
Page: 23

14. The ENIAC was originally built in order to speed up calculations for _____ .
A) systems of linear equations
B) weather forecasting
C) ballistics tables
D) chess playing

Answer: C
Topic: Historical Development
Difficulty: Easy
Page: 25

15. In 1948 John Bardeen, Walter Brattain, and William Shockley invented the _____.
A) ENIAC
B) vacuum tube
C) electronic valve
D) transistor

Answer: D
Topic: Historical Development
Difficulty: Easy
Page: 27

16. The first supercomputer, the CDC 6600, had a memory size of _____.
A) 128 kilowords
B) 256 megawords
C) 128 gigawords
D) 256 terawords

Answer: A
Topic: Historical Development
Difficulty: Easy
Page: 27

17. Which of the following is a computer that used second-generation (transistor) technology?
A) IBM 360
B) Atanasoff-Berry computer
C) PDP-1
D) Cray-1

Answer: C
Topic: Historical Development
Difficulty: Medium
Page: 27

18. Which of the following is a computer that used third-generation (integrated circuit) technology?
A) IBM 360
B) Atanasoff-Berry computer
C) PDP-1
D) CDC 6600

Answer: A
Topic: Historical Development
Difficulty: Medium
Page: 29

19. Which of the following is a computer that used fourth-generation (VLSI) technology?

A) IBM 360
B) Cray-1
C) PDP-11
D) IBM PC

Answer: D
Topic: Historical Development
Difficulty: Easy
Page: 31

20. In 1965, one of the founders of Intel predicted "The density of transistors in an integrated circuit will double every year." This is now known as:
A) Rock's Law
B) Amdahl's Law
C) Moore's Law
D) Cray's Law

Answer: C
Topic: Moore's Law
Difficulty: Easy
Page: 33

21. The approximate cost of building a chip fabrication plant today is:
A) just under $1 billion
B) between $1 billion and $15 billion
C) between $15 billion and $100 billion
D) over $100 billion

Answer: B
Topic: Moore's Law
Difficulty: Easy
Page: 34

22. The difference in expressive power between the physical components of a computer and a high-level language such as C++ is called a _____.
A) cognitive limitation
B) expressive constraint
C) semantic gap
D) von Neumann bottleneck

Answer: C
Topic: The Computer Level Hierarchy
Difficulty: Easy
Page: 34

23. The level of the computer hierarchy that is composed of gates and wires is the _____.
A) control level
B) machine level
C) system software level
D) digital logic level

Answer: D
Topic: The Computer Level Hierarchy
Difficulty: Easy
Page: 36

24. The level of the computer hierarchy where an operating system functions is the _____.
A) control level
B) machine level
C) system software level
D) digital logic level

Answer: C
Topic: The Computer Level Hierarchy
Difficulty: Easy
Page: 36

25. The computer component that makes sure that instructions are decoded and executed properly is the _____.
A) arithmetic-logic unit
B) control unit
C) floating-point unit
D) graphics processing unit

Answer: B
Topic: The Computer Level Hierarchy
Difficulty: Medium

Page: 36

26. Software as a Service (SaaS) replaces the _____ of the computer hierarchy with an Internet-based application.
A) digital logic level through user levels
B) digital logic level through high-level language levels
C) system software level through high-level language levels
D) digital logic level through machine levels

Answer: A
Topic: Cloud Computing
Difficulty: Medium
Page: 38

27. Platform as a Service (PaaS) replaces the _____ of the computer hierarchy with an Internet-based platform.
A) digital logic level through user levels
B) digital logic level through high-level language levels
C) system software level through high-level language levels
D) digital logic level through machine levels

Answer: B
Topic: Cloud Computing
Difficulty: Medium
Page: 38

28. Infrastructure as a Service (IaaS) replaces the _____ of the computer hierarchy with an Internet-based infrastructure.
A) digital logic level through user levels
B) digital logic level through high-level language levels
C) system software level through high-level language levels
D) digital logic level through machine levels

Answer: D
Topic: Cloud Computing
Difficulty: Medium
Page: 38

29. Cloud storage is a limited form of _____.
A) Software as a Service (SaaS)
B) Platform as a Service (PaaS)
C) Infrastructure as a Service (IaaS)
D) Data as a Service (DaaS)

Answer: C
Topic: Cloud Computing
Difficulty: Medium
Page: 39

30. The von Neumann bottleneck _____.
A) creates collisions on an I/O bus
B) describes the single processor-memory path
C) is eliminated when multiple processors/cores are used
D) was first invented by John Atanasoff

Answer: B
Topic: von Neumann Model
Difficulty: Easy
Page: 40

31. Deep Blue beat a human chess Grandmaster using _____ methods.
A) cognitive
B) numerical
C) hardwired
D) brute force

Answer: D
Topic: Parallelism: Enabler Of Machine Intelligence
Difficulty: Easy
Page: 47

32. Watson defeated human Jeopardy! champions using _____ methods.
A) cognitive
B) numerical

C) hardwired
D) brute force

Answer: A
Topic: Parallelism: Enabler Of Machine Intelligence
Difficulty: Easy
Page: 48

Short Answer

33. At the most basic level, a computer is a device consisting of three pieces: A processor; an I/O mechanism and a(n)_____.

Answer: Memory
Topic: Introduction
Difficulty: Easy
Page: 3

34. Expressed as a power of two, there are _____ kilobytes in a megabyte.

Answer: 2^{10}
Topic: Overview
Difficulty: Medium
Page: 5

35. Expressed as a power of two, there are _____ megabytes in a terabyte.

Answer: 2^{20}
Topic: An Example System
Difficulty: Medium
Page: 5

36. A terabyte represents what power of two?

Answer: 40
Topic: An Example System
Difficulty: Medium
Page: 5

37. There are _____ nanoseconds in a millisecond.

Answer: 1,000,000
Topic: An Example System
Difficulty: Medium
Page: 5

38. A kilobyte represents what power of two?

Answer: 10
Topic: An Example System
Difficulty: Easy
Page: 5

39. A gigabyte represents what power of two?

Answer: 30
Topic: An Example System
Difficulty: Medium
Page: 5

40. The ratio of horizontal pixels to vertical pixels that a monitor can display is its _____ ratio.

Answer: aspect ratio
Topic: An Example System
Difficulty: Medium
Page: 13

41. The statement “The cost of capital equipment to build semiconductors will double every four years.” is known as: _____.

Answer: Rock’s Law
Topic: Moore's Law
Difficulty: Easy
Page: 33

42. In the von Neumann architecture, the central processing unit (CPU) consists of registers, an arithmetic-logic unit (ALU), and a(n) _____.

Answer: control unit
Topic: von Neumann Model
Difficulty: Medium
Page: 40

43. Computers designed using the _____ architecture have two buses: one for data and one for instructions.

Answer: Harvard
Topic: Non-von Neumann Architectures
Difficulty: Medium
Page: 44

44. Computer chips having multiple processing units on a single chip are _____ architectures.

Answer: Multicore
Topic: Parallel Processors and Parallel Computing
Difficulty: Easy
Page: 45

True/False

45. Computer architecture encompasses all physical aspects of computer systems.

Answer: False
Topic: Introduction
Difficulty: Medium
Page: 2

46. Any task done by software can also be done using computer hardware, and any operation performed directly by hardware can be done using software.

Answer: True
Topic: Introduction
Difficulty: Easy
Page: 3

47. At its most basic level, a computer consists of only two parts: A processor and an I/O device.

Answer: False
Topic: Introduction
Difficulty: Easy
Page: 3

48. There are one billion microseconds in a second.

Answer: False
Topic: An Example System
Difficulty: Easy
Page: 5

49. We can be certain that a mebibyte always consists of 2^{20} bytes.

Answer: True
Topic: An Example System
Difficulty: Medium
Page: 6

50. Peripheral Component Interconnect (PCI) is the recommended replacement for SATA (serial ATA).

Answer: False
Topic: An Example System
Difficulty: Medium
Page: 12

51. Hot plugging means the same thing as Plug-and-Play.

Answer: False
Topic: An Example System
Difficulty: Medium
Page: 12

52. Color depth reflects the number of colors that can be displayed on an LCD screen at one time.

Answer: True
Topic: An Example System
Difficulty: Easy
Page: 14

53. Herman Hollerith invented punched card tabulating machines.

Answer: True
Topic: Historical Development
Difficulty: Easy
Page: 21

54. Ballistic tables were produced by the ENIAC during World War II.

Answer: False
Topic: Historical Development
Difficulty: Medium
Page: 25

55. A single transistor can replace several vacuum tubes.

Answer: False
Topic: Historical Development
Difficulty: Easy
Page: 28

56. The CDC 6600 supercomputer was among the first computers to employ transistors.

Answer: True
Topic: Historical Development
Difficulty: Easy
Page: 27

57. The continuation of Moore's Law is helped by Rock's Law.

Answer: False
Topic: Moore's Law
Difficulty: Easy
Page: 34

58. The control level is above the machine level in the computer level hierarchy.

Answer: False
Topic: The Computer Level Hierarchy
Difficulty: Medium
Page: 35

59. A control unit consists of a central processing unit (CPU) with an arithmetic logic unit (ALU) and registers.

Answer: False
Topic: The von Neumann Architecture
Difficulty: Easy
Page: 40

60. Cognitive computing can make inferences within a problem's context using hard facts and incomplete information.

Answer: True
Topic: Parallelism: Enabler Of Machine Intelligence
Difficulty: Easy
Page: 49

Exam Bank Chapter 4 – Null & Lobur 4th ed.

Multiple Choice

1. The _____ is a digital logic component that is often used in computer registers.
A) control unit
B) D flip-flop
C) multiplexer
D) inverter

Answer: B
Topic: CPU Basics
Difficulty: Easy
Page: 216

2. The _____ is responsible for fetching program instructions, decoding each one, and

performing the indicated sequence of operations.
A) program counter
B) pre-processor
C) co-processor
D) control unit

Answer: D
Topic: CPU Basics
Difficulty: Easy
Page: 215

3. A computer bus consists of data lines, _____, control lines, and power lines.
A) address lines
B) protocol lines
C) cycle lines
D) master/slave lines

Answer: A
Topic: Buses
Difficulty: Easy
Page: 219

4. The _____ connects the CPU to memory.
A) backplane bus
B) I/O bus
C) expansion bus
D) system bus

Answer: D
Topic: Buses
Difficulty: Easy
Page: 220

5. Clock skew is a problem for:
A) control buses
B) address buses
C) asynchronous buses
D) synchronous buses

Answer: D
Topic: Buses
Difficulty: Medium
Page: 220

6. _____ is the process whereby devices connected to a bus autonomously determine which of the devices shall have control over the bus:
A) distributed arbitration using self-selection
B) centralized parallel arbitration
C) daisy chain arbitration
D) distributed arbitration using collision detection
Answer: A
Topic: Buses
Difficulty: Medium
Page: 220

7. This bus arbitration method can cause throughput delays owing to bottlenecks in the selection process:
A) distributed arbitration using self-selection
B) centralized parallel arbitration
C) daisy chain arbitration
D) distributed arbitration using collision detection
Answer: B
Topic: Buses
Difficulty: Medium
Page: 220

8. The equation below relates seconds to instruction cycles. What goes in the ???? space?

$$\text{CPU time} = \frac{\text{seconds}}{\text{program}} = \frac{\text{instructions}}{\text{program}} \times \frac{\text{????}}{\text{instruction}} \times \frac{\text{seconds}}{\text{cycle}}$$

A) maximum bytes
B) average bytes
C) maximum cycles

D) average cycles

Answer: D
Topic: Clocks
Difficulty: Easy
Page: 222

9. This common method used to increase CPU throughput can result in destructive overheating of the CPU:
A) resynchronization
B) asynchronization
C) overclocking
D) skewing

Answer: C
Topic: Clocks
Difficulty: Easy
Page: 223

10. If, after fetching a value from memory, we discover that the system has returned only half of the bits that we expected; it is likely that we have a problem with:
A) the I/O bus
B) the system bus
C) byte alignment
D) the control unit
Answer: C
Topic: Memory Organization and Addressing
Difficulty: Hard
Page: 225

11. Suppose that a 32MB system memory is built from 32 1MB RAM chips. How many address lines are needed to select one of the memory chips?
A) 4
B) 5
C) 8
D) 32
Answer: B
Topic: Memory Organization and Addressing

Difficulty: Hard
Page: 225

12. Suppose that a 64MB system memory is built from 64 1MB RAM chips. How many address lines are needed to select one of the memory chips?
A) 6
B) 8
C) 32
D) 64
Answer: A
Topic: Memory Organization and Addressing
Difficulty: Hard
Page: 225

13. Suppose a system has a byte-addressable memory size of 256MB. How many bits are required for each address?
A) 8
B) 28
C) 32
D) 48
Answer: B
Topic: Memory Organization and Addressing
Difficulty: Medium
Page: 225

14. Suppose a system has a byte-addressable memory size of 4GB. How many bits are required for each address?
A) 16
B) 24
C) 32
D) 48
Answer: C
Topic: Memory Organization and Addressing
Difficulty: Medium
Page: 225

15. Suppose that a system uses 32-bit memory words and its memory is built from 16 1M × 8 RAM chips. How many address bits are required to uniquely identify each memory word?
A) 16
B) 22
C) 24
D) 32
Answer: B
Topic: Memory Organization and Addressing
Difficulty: Hard
Page: 226

16. Suppose that a system uses 16-bit memory words and its memory is built from 32 1M × 8 RAM chips. How many address bits are required to uniquely identify each memory word?
A) 16
B) 24
C) 32
D) 64
Answer: B
Topic: Memory Organization and Addressing
Difficulty: Hard
Page: 226

17. Suppose that a system uses 32-bit memory words and its memory is built from 16 1M × 16 RAM chips. How large, in words, is the memory on this system?
A) 8M
B) 16M
C) 32M
D) 64M
Answer: A
Topic: Memory Organization and Addressing
Difficulty: Medium
Page: 226

18. Suppose that a system uses 16-bit memory words and its memory built from 32 1M × 8 RAM chips. How large, in words, is the memory on this system?
A) 8M

B) 16M
C) 32M
D) 64M
Answer: B
Topic: Memory Organization and Addressing
Difficulty: Medium
Page: 226

19. Suppose we have a 1024-word memory that is 16-way low-order interleaved. What is the size of the memory address offset field?
A) 12 bits
B) 10 bits
C) 6 bits
D) 4 bits
Answer: C
Topic: Memory Organization and Addressing
Difficulty: Medium
Page: 226

20. Suppose we have a 4096-word memory that is 64-way high-order interleaved, what is the size of the memory address offset field?
A) 12 bits
B) 10 bits
C) 8 bits
D) 4 bits
Answer: D
Topic: Memory Organization and Addressing
Difficulty: Medium
Page: 226

21. The _____ of a machine specifies the instructions that the computer can perform and the format for each instruction.
A) control unit
B) CPU
C) instruction set architecture
D) fetch-decode-execute cycle

Answer: C

Topic: ISA
Difficulty: Easy
Page: 233

22. The _____ is a group of bits that tells the computer to perform a specific operation.
A) program counter
B) opcode
C) register
D) microoperation

Answer: B
Topic: ISA
Difficulty: Easy
Page: 233

23. The _____ register keeps track of the next instruction to be fetched.
A) program counter
B) accumulator
C) address register
D) memory buffer register

Answer: A
Topic: Registers and Buses
Difficulty: Easy
Page: 232

24. The register that holds the address of the data to be transferred is called:
A) memory address register
B) index register
C) memory buffer register
D) none of these

Answer: A
Topic: Registers and Buses
Difficulty: Easy
Page: 232

25. The register that holds the actual data to be read from or written to a given memory address is called:
A) memory address register
B) index register
C) memory buffer register
D) none of these

Answer: C
Topic: Registers and Buses
Difficulty: Easy
Page: 232

26. Which MARIE instruction is being carried out by the RTN that follows?

```
MAR ← X
MBR ← M[MAR]
AC ← MBR
```

A) **Store X**
B) **Add X**
C) **Load X**
D) **Jump X**

Answer: C
Topic: Register Transfer Notation
Difficulty: Easy
Page: 237

27. Which MARIE instruction is being carried out by the RTN statement that follows?

```
PC ← X
```

A) **Store X**
B) **JnS X**
C) **Load X**
D) **Jump X**

Answer: D
Topic: Register Transfer Notation
Difficulty: Easy
Page: 237

28. The RTN for the first step in the fetch-decode-execute cycle is:

A) **MAR ← PC**
B) **PC ← PC + 1**
C) **IR ← MAR**
D) **IR ← MBR**

Answer: A
Topic: The Fetch–Decode–Execute Cycle
Difficulty: Medium
Page: 239

29. Which MARIE instruction is being carried out by the RTN that follows?

```
MAR ← X
MBR ← M[MAR]
MAR ← MBR
MBR ← AC
M[MAR] ← MBR
```

A) **Store X**
B) **JnS X**
C) **Load X**
D) **StoreI X**

Answer: D
Topic: Register transfer notation
Difficulty: Medium
Page: 250

30. Assembly language:
A) is not translated into machine language
B) uses alphabetic (mnemonic) codes in place of binary strings
C) is easier to program in than high-level languages
D) all of the above

Answer: B
Topic: Assembly Language
Difficulty: Medium

Page: 246

31. Among other things, assembler directives can:

A) determine the next action after numeric overflow
B) distinguish a value as hexadecimal or decimal
C) invoke interrupt service routines
D) control conditional assembly using macro instructions

Answer: B
Topic: Assembly Language
Difficulty: Hard
Page: 247

32. During the first pass of an assembler:

A) instructions are only partially assembled
B) the symbol table is only partially completed
C) addresses from the symbol table are placed in object code
D) external code is merged with the object code

Answer: A
Topic: Assembly Language
Difficulty: Medium
Page: 247

33. During the second pass of an assembler:

A) instructions are only partially assembled
B) the symbol table is only partially completed
C) addresses from the symbol table are placed in object code
D) external code is merged with the object code

Answer: C
Topic: Assembly Language
Difficulty: Medium
Page: 247

34. Which of the following is placed into the symbol table during the first pass?

A) labels
B) comments
C) directives
D) mnemonics

Answer: A
Topic: Assembly Language
Difficulty: Medium
Page: 247

35. What is the maximum value of the cycle counter when the following sequence of microoperations is executed?

```
MAR ← X, MBR ← AC
M[MAR] ← MBR
```

A) 1
B) 2
C) 3
D) 4

Answer: A
Topic: Hardwired Control
Difficulty: Medium
Page: 260

36. Suppose a computer's control unit consists of a 4-bit counter and a 4 × 16 decoder. What is the maximum number of clock cycles that can be consumed by any instruction?
A) 4
B) 16
C) 32
D) 48

Answer: B
Topic: Machine Control
Difficulty: Medium
Page: 260

37. Suppose a computer's control unit consists of a 5-bit counter and a 5 × 32 decoder. What is the maximum number of clock cycles that can be consumed by any instruction?
A) 4
B) 16
C) 32
D) 48

Answer: C
Topic: Machine Control
Difficulty: Medium
Page: 260

38. If a system's instruction set consists of a 5-bit opcode, what is the maximum number of output signal lines required for the control unit?
A) 4
B) 16
C) 32
D) 48

Answer: C
Topic: Machine Control
Difficulty: Medium
Page: 260

39. If a system's instruction set consists of an 8-bit opcode, what is the maximum number of output signal lines required for the control unit?
A) 8
B) 64
C) 128
D) 256
Answer: D
Topic: Machine Control
Difficulty: Medium
Page: 260

40. If a system's entire set of microoperations consists of 41 statements, how many bits

must be used for its microop code?
A) 4
B) 5
C) 6
D) 41
Answer: C
Topic: Machine Control
Difficulty: Medium
Page: 260

41. If a system's entire set of microoperations consists of 92 statements, how many bits must be used for its microop code?
A) 7
B) 8
C) 64
D) 92
Answer: A
Topic: Machine Control
Difficulty: Medium
Page: 260

42. In order to pass parameters to subprograms a(n) _____ must be implemented to support the ISA.
A) bus
B) assembler
C) counter
D) stack
Answer: D
Topic: Real-World Examples of Computer Architectures
Difficulty: Medium
Page: 268

True or False

43. In high-order memory interleaving, the high-order bits of the memory address are used to select the memory bank.

Answer: True
Topic: Memory Organization and Addressing
Difficulty: Easy
Page: 226

44. A program counter points to the memory address of the instruction that the CPU is currently executing.

Answer: False
Topic: Registers and Buses
Difficulty: Medium
Page: 232

45. While and if statements are examples of conditional branching instructions.

Answer: True
Topic: ISA
Difficulty: Easy
Page: 233

46. Most systems automatically convert numeric ASCII characters, such as "1" "2" and "3," to their numeric equivalents.

Answer: False
Topic: ISA
Difficulty: Easy
Page: 233

47. An assembler "assembles" assembly language into register transfer language (RTL).

Answer: False
Topic: Assembly Language
Difficulty: Medium

Page: 246

48. Interrupt checking is typically carried out at various times during the execution of a machine instruction.

Answer: False
Topic: Interrupts
Difficulty: Medium
Page: 241

49. One good reason to use assembly language is to compensate for shortcomings in optimizing compilers for higher-level languages.
Interrupt checking is typically carried out at various times during the execution of a machine instruction.

Answer: True
Topic: Assembly Language
Difficulty: Easy
Page: 248

50. The purpose of both hardwired control units and microprogrammed control units is to raise a series of signals that carry out operations inside a computer system.

Answer: True
Topic: Machine Control
Difficulty: Easy
Page: 256

51. The control store for a hardwired control unit is implemented using ROM, EPROM, or PROM.

Answer: False
Topic: Machine Control
Difficulty: Medium
Page: 263

52. The MIPS family of processors employs a superscalar design and NetBurst microarchitecture for improved performance.

Answer: True
Topic: Real-World Examples of Computer Architectures
Difficulty: Easy
Page: 270

53. A thread shares code and data with the parent process but has its own resources, including a stack and instruction pointer.

Answer: True
Topic: Real-World Examples of Computer Architectures
Difficulty: Medium
Page: 271

54. In a pure load/store architecture, no instructions other than the load and store instructions are allowed to directly access memory.

Answer: True
Topic: Real-World Examples of Computer Architectures
Difficulty: Easy
Page: 275

Short Answer

55. Given the instruction set for MARIE:

Instruction Opcode	**Instruction**	**Instruction Opcode**	**Instruction**
0	JnS X	7	Halt
1	Load X	8	Skipcond (00 for AC<0, 01 for AC=0, 10 for AC>0)
2	Store X	9	Jump X
3	Add X	A	Clear

4	Subt X	B	AddI X
5	Input	C	JumpI X
6	Output		

Write the assembly language equivalent for the machine instruction: 0011 000000000101

Answer: Add 005
Topic: Assembly Language
Difficulty: Medium
Page: 236

56. Given the instruction set for MARIE:

Instruction Opcode	**Instruction**	**Instruction Opcode**	**Instruction**
0	JnS X	7	Halt
1	Load X	8	Skipcond (00 for AC<0, 01 for AC=0, 10 for AC>0)
2	Store X	9	Jump X
3	Add X	A	Clear
4	Subt X	B	AddI X
5	Input	C	JumpI X
6	Output		

Write the assembly language equivalent for the machine instruction: 1011 000000001111

Answer: AddI 00F
Topic: Assembly Language
Difficulty: Medium
Page: 236

57. Given the instruction set for MARIE:

Instruction Opcode	**Instruction**	**Instruction Opcode**	**Instruction**
0	JnS X	7	Halt
1	Load X	8	Skipcond (00 for AC<0, 01 for AC=0, 10 for AC>0)
2	Store X	9	Jump X
3	Add X	A	Clear
4	Subt X	B	AddI X
5	Input	C	JumpI X
6	Output		

Write the assembly language equivalent for the machine instruction: 1000 100000000000

Answer: Skipcond 800
Topic: Assembly Language
Difficulty: Hard
Page: 236

Exam Bank Chapter 5 – Null & Lobur 4th ed.

Multiple Choice

1. Instruction sets are differentiated by which feature?
A) operand storage
B) number of operands
C) operand location
D) operations
E) all of the above

Answer: E
Topic: Instruction Formats
Difficulty: easy
Page: 294

2. The term *endian* refers to a computer architecture's:
A) ability to complete arithmetic operations
B) ability to find the end of variable length instructions
C) byte order
D) address modes
E) none of the above

Answer: C
Topic: Endianness
Difficulty: Medium
Page: 295

3. There are three basic ISA architectures for internal storage in the CPU:
A) cache, RAM, and ROM
B) stack, accumulator, and general-purpose registers
C) cache, RAM, and registers
D) load-store, cache, and RAM

Answer: B
Topic: Instruction Formats
Difficulty: Medium
Page: 298

4. General-purpose architectures are divided into three groups:
A) memory-memory, register-memory, and load-store
B) stack addressing, accumulator addressing, and register addressing
C) Von Neumann, parallel, and quantum
D) Windows, Mac, and Linux

Answer: A
Topic: Instruction Formats
Difficulty: Medium
Page: 298

5. Fixed-length instructions:
A) waste space but are fast and perform better than variable length instructions
B) are more complex to decode than variable-length instructions but save space
C) save space and are faster and perform better than variable-length instructions
D) are less complex to decode than variable-length instructions and save space

Answer: A
Topic: Instruction Formats
Difficulty: Medium
Page: 299

6. Consider the infix expression: 16/(5+3). The equivalent postfix (reverse Polish notation) expression is:
A) 16/8
B) 16 / 5 + 3

C) 16 5 3 + /
D) 5 3 + / 16

Answer: C
Topic: Postfix Notation
Difficulty: Easy
Page: 301

7. Consider the postfix expression: A-B+C*(D*E-F)/(G+H*K). The equivalent postfix (reverse Polish notation) expression is:

A) AB-C+DE*F-GH+K**/
B) AB-CDE*F-*+GHK*+/
C) ABC+-E*F-*+GHK*+/
D) None of these

Answer: B
Topic: Postfix Notation
Difficulty: Hard
Page: 301

8. Consider the postfix (reverse Polish notation) 10 5 + 6 3 - /. The equivalent infix expression is:

A) (10+5)/(6-3)
B) (10+5)-(6/3)
C) 10/5+(6-3)
D) (10+5)-(6/3)

Answer: A
Topic: Postfix Notation
Difficulty: Medium
Page: 301

9. In reverse Polish notation, the expression A*B+C*D is written:
A) ABCD**+
B) AB*CD*+
C) AB*CD+*

D) A*B*CD+

Answer: B
Topic: Postfix Notation
Difficulty: Easy
Page: 301

10. A stack-organized computer uses _____ addressing.
A) indirect
B) zero
C) indexed
D) direct

Answer: B
Topic: Instruction Formats
Difficulty: Easy
Page: 304

11. To carry out a binary arithmetic operation, an accumulator architectures uses _____ operand(s).
A) zero
B) one
C) two
D) either one or two

Answer: B
Topic: Instruction Formats
Difficulty: Easy
Page: 304

12. If the opcodes field for an instruction has n bits, that means there are _____ potential distinct operations.
A) 2n
B) n/2
C) 2^n
D) n^2

Answer: C

Topic: Instruction Formats
Difficulty: Hard
Page: 305

13. A “jump” statement is an example of:
A) a data movement instruction
B) an arithmetic instruction
C) a Boolean logic instruction
D) a bit manipulation instruction
E) an input/output instruction
F) a transfer of control instruction

Answer: F
Topic: Instruction Types
Difficulty: Medium
Page: 311

14. A “subtract” statement is an example of:
A) a data movement instruction
B) an arithmetic instruction
C) a Boolean logic instruction
D) a bit manipulation instruction
E) an input/output instruction
F) a transfer of control instruction

Answer: B
Topic: Instruction Types
Difficulty: Easy
Page: 309

15. A “store” statement is an example of:
A) a data movement instruction
B) an arithmetic instruction
C) a Boolean logic instruction
D) a bit manipulation instruction
E) an input/output instruction
F) a transfer of control instruction

Answer: A
Topic: Instruction Types
Difficulty: Easy
Page: 311

16. Examples of hazards in pipelines include:
A) resource conflicts, data dependencies, and conditional branch statements
B) superscalar and VLIW
C) addressing modes and memory
D) ILP and VLIW

Answer: A
Topic: Pipelining
Difficulty: Medium
Page: 319

True or False.

17. Short instructions are typically better because they take up less room and can be fetched quickly.

Answer: True
Topic: Instruction Formats
Difficulty: Easy
Page: 294

18. Variable-length instructions are easier to decode than fixed-length instructions.

Answer: False
Topic: Instruction Formats
Difficulty: Easy
Page: 294

19. Memory organization has no effect on instruction format.

Answer: False
Topic: Instruction Formats
Difficulty: Hard
Page: 294

20. Fixed-length instructions always have the same number of operands.

Answer: False
Topic: Instruction Formats
Difficulty: Medium
Page: 294

21. A fixed-length instruction must have fixed-length opcodes.

Answer: False
Topic: Instruction Formats
Difficulty: Medium
Page: 305

22. The best architecture for evaluating postfix notation is the stack-based architecture.

Answer: True
Topic: Postfix Notation
Difficulty: Easy
Page: 301

23. Little endian computers store a two-byte integer with the least significant byte at the lower address.

Answer: True
Topic: Endianness
Difficulty: Medium
Page: 295

24. Big endian computers store a two-byte integer with the least significant byte at the lower address.

Answer: False
Topic: Instruction Formats
Difficulty: Medium
Page: 295

25. One disadvantage to big endian representation is that most computers require words to be written on word address boundaries.

Answer: True
Topic: Endianness
Difficulty: Hard
Page: 297

26. Stack architectures store all operands on the stack.

Answer: True
Topic: Instruction Formats
Difficulty: Easy
Page: 298

27. Accumulator architectures store one operand on the stack and the other in the accumulator.

Answer: False
Topic: Instruction Formats
Difficulty: Easy
Page: 298

28. Accumulator architectures use sets of general purpose registers to store operands.

Answer: False
Topic: Instruction Formats

Difficulty: Easy
Page: 298

29. General-purpose register architectures are the most widely accepted models for computers today.

Answer: True
Topic: Instruction Formats
Difficulty: Easy
Page: 298

30. The term “endian” refers to the byte ordering, or the way a computer stores the bytes of a multiple-byte data element.

Answer: True
Topic: Endianness
Difficulty: Easy
Page: 295

31. A Very Long Instruction Word (VLIW) is an architectural characteristic in which each instruction can specify multiple scalar operations.

Answer: True
Topic: Pipelining
Difficulty: Hard
Page: 231

Short Answer.

32. Assume a computer has 32-bit integers. Show how the value 0xCAFEBABE would be stored sequentially in memory, starting at address 0x100, on both a big endian machine and a little endian machine, assuming that each address holds one byte.

Address	Big Endian	Little Endian
0x100		
0x101		
0x102		
0x103		

Answer:

Address	Big Endian	Little Endian
0x100	CA	BE
0x101	FE	BA
0x102	BA	FE
0x103	BE	CA

Topic: Endianness
Difficulty: Hard
Page: 296

33. Assume a computer has 32-bit integers. Show how the value 0x0001122 would be stored sequentially in memory, starting at address 0x000, on both a big endian machine and a little endian machine, assuming that each address holds one byte.

Address	Big Endian	Little Endian
0x000		
0x001		
0x002		
0x003		

Answer:

Address	Big Endian	Little Endian
0x000	00	22
0x001	00	11
0x002	11	00
0x003	22	00

Topic: Endianness
Difficulty: Medium
Page: 296

34. Suppose we have the instruction LDA 800. Given memory as follows:

Memory

800	900
…	
900	1000
…	
1000	500
…	
1100	600
…	
1200	800

What would be loaded into the AC if the addressing mode for the operating is immediate?

Answer: 800
Topic: Addressing Modes
Difficulty: Easy
Page: 315

35. Suppose we have the instruction LDA 800. Given memory as follows:

Memory

800	900
…	
900	1000
…	
1000	500
…	
1100	600
…	
1200	800

What would be loaded into the AC if the addressing mode for the operating is direct?

Answer: 900
Topic: Addressing Modes
Difficulty: Easy
Page: 315

36. Suppose we have the instruction LDA 800. Given memory as follows:

Memory

800	900
…	
900	1000
…	
1000	500
…	
1100	600
…	
1200	800

What would be loaded into the AC if the addressing mode for the operating is indirect?

Answer: 1000
Topic: Addressing Modes
Difficulty: Easy
Page: 315

37. Given 8-bit instructions, is it possible to use expanding opcodes to allow the following to be encoded?
3 instructions with two 3-bit operands
3 instructions with one 4-bit operand
4 instructions with one 3-bit operand

Answer: Yes
Topic: Expanding Opcodes
Difficulty: Medium
Page: 308

38. A nonpipelined system takes 300ns to process a task. The same task can be processed in a 5-segment pipeline with a clock cycle of 60ns. Determine the speedup ratio of the pipeline for 100 tasks.

Answer: (300ns x 100)/((5+100-1)(60ns)) = 30000/6240 = 4.8
Topic: Pipelining
Difficulty: Medium

Page: 317

39. A nonpipelined system takes 300ns to process a task. The same task can be processed in a 5-segment pipeline with a clock cycle of 60ns. What is the maximum speedup that could be achieved with the pipeline unit over the nonpipelined unit?

Answer: 5
Topic: Pipelining
Difficulty: Medium
Page: 317

40. Suppose a computer has 16-bit instructions. The instruction set consists of 32 different operations. All instructions have an opcode and two address fields (allowing for two addresses). The first of these addresses must be a register, and the second must be memory. Expanding opcodes are not used. The machine has 16 registers. How many bits are needed for the opcode field?

Answer: 5
Topic: Instruction Formats
Difficulty: Easy
Page: 305

41. Suppose a computer has 16-bit instructions. The instruction set consists of 32 different operations. All instructions have an opcode and two address fields (allowing for two addresses). The first of these addresses must be a register, and the second must be memory. Expanding opcodes are not used. The machine has 16 registers. How many bits are needed for a register address?

Answer: 4
Topic: Instruction Formats
Difficulty: Easy
Page: 305

42. Suppose a computer has 16-bit instructions. The instruction set consists of 32 different operations. All instructions have an opcode and two address fields (allowing for two addresses). The first of these addresses must be a register, and the second must be

memory. Expanding opcodes are not used. The machine has 16 registers. What is the maximum allowable size for memory?

Answer: $2^7 = 128$
Topic: Instruction Formats
Difficulty: Hard
Page: 305

43. Suppose an instruction takes 4 cycles to execute in an unpipelined CPU: one cycle to fetch the instruction, one cycle to decode the instruction and fetch any operands, one cycle to perform the ALU operation, and one cycle to store the result. In a CPU with a 4 stage pipeline, that instruction still takes 4 cycles to execute, so how can we say the pipeline speeds up the execution of the program?
Answer: The pipeline allows us to overlap stages of instructions, for example, the fetch of one instruction with the decode of the previous one.
Topic: Pipelining
Difficulty: Medium
Page: 316

44. Suppose the memory of a computer is as follows:

Address 0x100	Address 0x101	Address 0x102	Address 0x103
12	34	56	78

What integer value is this on a big endian computer?

Answer: 12345678
Topic: Endianness
Difficulty: Easy
Page: 295

45. Suppose the memory of a computer is as follows:

Address 0x100	Address 0x101	Address 0x102	Address 0x103
12	34	56	78

What integer value is this on a little endian computer?

Answer: 78563412
Topic: Endianness
Difficulty: Easy

Page: 295

46. How does a computer architecture that uses zero-address instructions get data from memory?

Answer: It uses a stack.
Topic: Instruction Formats
Difficulty: Medium
Page: 299

47. How does register addressing differ from direct addressing?

Answer: In direct addressing, the address given is an address is memory. In register addressing, a register is used instead of memory.
Topic: Address Modes
Difficulty: Medium
Page: 313

48. What is the purpose of having various address modes?

Answer: Multiple addressing modes allow us to specify a much larger range of locations than if we were limited to using one or two modes.
Topic: Addressing Modes
Difficulty: Medium
Page: 316

49. What is a load-store architecture?

Answer: These architectures require data to be moved into registers before any operations can be performed on that data.
Topic: Instruction Formats
Difficultly: Medium
Page: 298

50. What is meant by instruction set orthogonality?

Answer: Each instruction should perform a unique function (without duplicating any other

instruction) and the instructions should be independent and consistent.
Topic: Instruction Types
Difficulty: Hard
Page: 311

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Multiple Choice

1. _____ memory allows data to be both read from and written to easily and rapidly.
A) EPROM
B) ROM
C) RAM
D) PROM

Answer: C
Topic: Memory Types
Difficulty: Easy
Page: 342

2. _____ memory is a small, high-speed, high-cost memory that servers as a buffer for frequently accessed data.
A) ROM
B) RAM
C) cache
D) SRAM

Answer: C
Topic: Memory Types
Difficulty: Easy
Page: 341

3. The basic difference between RAM and ROM memory is:
A) RAM is nonvolatile while ROM is volatile

B) RAM is read/write while ROM Is read only
C) ROM is used to store programs and data, while RAM is not
D) ROM is typically specified when you buy a computer; RAM is not

Answer: B
Topic: Memory Types
Difficulty: Medium
Page: 342

4. The approach of using a combination of memory types to provide the best performance at the best cost is called:
A) caching
B) hierarchical memory
C) solid state memory
D) off-line memory

Answer: B
Topic: Memory Hierarchy
Difficulty: Medium
Page: 343

5. Examples of secondary memory include:
A) ROM, PROM, and EROM
B) main memory and cache
C) magnetic disk drives and solid state memory
D) optical jukeboxes and tape libraries

Answer: C
Topic: Memory Types
Difficulty: Medium
Page: 343

6. When the requested data resides in a given level of memory, we call this a _____.
A) hit
B) penalty
C) miss
D) locality of reference

Answer: A
Topic: Memory Hierarchy
Difficulty: Easy
Page 345

7. “Locality of reference” refers to:
A) data always being in cache
B) programs always referencing data in RAM
C) clustering of memory references
D) the requirement that forces us to use a large amount of expensive memory

Answer: C
Topic: Memory
Difficulty: Medium
Page 346

8. Which of the following types of memory has the shortest (fastest) access time?
A) cache memory
B) main memory
C) secondary memory
D) registers

Answer: D
Topic: Memory Hierarchy
Difficulty: Easy
Page: 345

9. Which of the following types of memory has the longest (slowest) access time?
A) cache memory
B) main memory
C) secondary memory
D) registers

Answer: C
Topic: Memory Hierarchy
Difficulty: Easy
Page: 345

10. Which of the following types of memory needs to be refreshed periodically to maintain its data?
A) SRAM
B) DRAM
C) ROM
D) all of the above

Answer: B
Topic: Memory Types
Difficulty: Medium
Page: 342

11. If a cache access requires one clock cycle and dealing with cache misses requires an additional five clock cycles, which of the following cache hit rates results in an effective access time of 2 clock cycles?
A) 70%
B) 80%
C) 85%
D) 90%
E) 95%

Answer: B
Topic: Cache Memory
Difficulty: Medium
Page: 367

12. A major advantage of direct mapped cache is its simplicity and ease of implementation. The main disadvantage of direct mapped cache is:
A) it is more expensive than fully associative and set associative mapping
B) it has a greater access time than any other method
C) its performance is degraded if two or more blocks that map to the same location are used alternately
D) it does not allow the cache to store the tag that corresponds to the block currently residing in that cache location

Answer: C
Topic: Cache memory
Difficulty: Medium

Page: 358

13. The average time required to reach a memory storage location and retrieve its contents is called:
A) latency
B) response time
C) hit time
D) effective access time

Answer: D
Topic: Cache Memory
Difficulty: Medium
Page: 366

14. Memory that is accessed by searching for content is called:
A) read only memory
B) erasable memory
C) associative memory
D) virtual memory

Answer: C
Topic: Cache Memory
Difficulty: Medium
Page: 356

15. The main memory in a desktop personal computer is made of:
A) ROM
B) RAM
C) cache
D) none of the above

Answer: B
Topic: Memory
Difficulty: Easy
Page: 342

16. Cache memory is effective because:
A) it is very inexpensive
B) it is very large
C) it is very small
D) of the principle of locality

Answer: D
Topic: Memory
Difficulty: Medium
Page: 349

17. Cache memory is typically positioned between:
A) the CPU and RAM
B) the CPU and the hard drive
C) ROM and RAM
D) none of the above

Answer: A
Topic: Cache Memory
Difficulty: Medium
Page: 348

18. What characteristic of RAM makes it unsuitable for permanent storage?
A) not reliable
B) too slow
C) volatile
D) all of the above

Answer: C
Topic: Memory Types
Difficulty: Medium
Page: 342

19. Information can be retrieved fastest from:
A) hard disk
B) magnetic tape
C) optical disk
D) USB flash drive

Answer: A
Topic: Memory Types
Difficulty: Medium
Page: 345

20. Cache mapping is necessary because:
A) the address generated by the CPU must be converted to a cache location
B) cache is so small that its use requires a map
C) cache is larger than main memory and mapping allows us to store multiple copies of each piece of data from main memory
D) none of the above

Answer: A
Topic: Cache Memory
Difficulty: Medium
Page: 349

21. The tag field of a main memory address is used to determine:
A) if the cache entry is valid
B) if the cache entry is the desired block
C) if the memory address is valid
D) none of the above

Answer: B
Topic: Cache Memory
Difficulty: Medium
Page: 350

22. The offset field of a main memory address is used to determine:
A) if the cache entry is valid
B) if the cache entry is the desired block
C) the location of the desired data in the cache block
D) none of these

Answer: C
Topic: Cache Memory
Difficulty: Medium

Page: 350

23. Cache replacement policies are necessary:
A) to determine which cache mapping policy to use
B) to determine which block in cache should be the victim block
C) to decide where to put blocks when cache is empty
D) all of the above

Answer: B
Topic: Cache Memory
Difficulty: Medium
Page: 365

24. All of the following are cache replacement algorithms except:
A) LRU
B) FIFO
C) random
D) thrashing

Answer: D
Topic: Cache Memory
Difficulty: Medium
Page: 366

25. Assuming an 8-bit virtual address with pages of 32 bytes, the virtual address format is:
A) 5 bits for the page and 3 bits for the offset
B) 3 bits for the page and 5 bits for the offset
C) 8 bits for the page and 32 bits for the offset
D) 32 bits for the page and 8 bits for the offset

Answer: B
Topic: Virtual Memory
Difficulty: Medium
Page: 376

26. Memory segmentation can result in _____ fragmentation, while paging

can result in _____ fragmentation.
A) external / internal
B) internal /external
C) incoherent / coherent
D) coherent / incoherent
E) unified / dissipated

Answer: A
Topic: Virtual Memory
Difficulty: Medium
Page: 386

27. Cache memory improves performance by improving memory _____ while virtual memory improves performance by increasing memory _____.
A) execution time/access time
B) locality/access time
C) access time/address space
D) organization/paging

Answer: C
Topic: Memory
Difficulty: Hard
Page: 372

28. The purpose of a TLB is:
A) to cache page table entries
B) to cache frequently used data from memory
C) to hold the starting address of the page table
D) to hold the length of the page table

Answer: A
Topic: Virtual Memory
Difficulty: Medium
Page: 382

True or False

29. All cache mapping schemes require a main memory address to have an offset field.

Answer: True
Topic: Cache Memory
Difficulty: Medium
Page: 350

30. It is important to know if a computer is byte or word addressable because we need to know how many addresses are contained in main memory, cache, and in each block when doing cache mapping.

Answer: True
Topic: Cache Memory
Difficulty: Medium
Page: 350

31. Caching breaks down when programs exhibit good locality.

Answer: False
Topic: Cache Memory
Difficulty: Medium
Page: 367

32. The two types of cache write policies are write-through and write-back.

Answer: True
Topic: Cache Memory
Difficultly: Medium
Page: 368

33. A unified cache is a cache that holds both data and instructions.

Answer: True

Topic: Cache Memory
Difficulty: Medium
Page: 371

34. When a computer uses paging, there must be a page table for every process.

Answer: True
Topic: Virtual Memory
Difficulty: Easy
Page: 374

Short Answer

35. Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

Answer: 3
Topic: Cache Memory
Difficulty: Easy
Page: 352

36. Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the block field.

Answer: 5
Topic: Cache Memory
Difficulty: Easy
Page: 352

37. Suppose we have a byte-addressable computer using direct mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the

size of the tag field.

Answer: 8
Topic: Cache Memory
Difficulty: Medium
Page: 352

38. Suppose we have a byte-addressable computer using fully associative mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 16 bytes, determine the size of the offset field.

Answer: 4
Topic: Cache Memory
Difficulty: Easy
Page: 357

39. Suppose we have a byte-addressable computer using fully associative mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 16 bytes, determine the size of the tag field.

Answer: 12
Topic: Cache Memory
Difficulty: Medium
Page: 357

40. Suppose we have a byte-addressable computer using 2-way set associative mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the offset field.

Answer: 3
Topic: Cache Memory
Difficulty: Medium
Page: 359

41. Suppose we have a byte-addressable computer using 2-way set associative mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8

bytes, determine the size of the set field.

Answer: 4
Topic: Cache Memory
Difficulty: Medium
Page: 359

42. Suppose we have a byte-addressable computer using 2-way set associative mapping with 16-bit main memory addresses and 32 blocks of cache. If each block contains 8 bytes, determine the size of the tag field.

Answer: 9
Topic: Cache Memory
Difficulty: Medium
Page: 359

43. Suppose we have a byte-addressable computer with a cache that holds 8 blocks of 4 bytes each. Assuming that each memory address has 8 bits, to which cache block would the hexadecimal address 0x09 map if the computer uses direct mapping?

Answer: Block 2
Topic: Cache Memory
Difficulty: Medium
Page: 352

44. Suppose we have a byte-addressable computer with a cache that holds 8 blocks of 4 bytes each. Assuming that each memory address has 8 bits, to which cache set would the hexadecimal address 0x1F map if the computer uses direct mapping?

Answer: Block 7 (111)
Topic: Cache Memory
Difficulty: Medium
Page: 361

45. Suppose we have a byte-addressable computer with a cache that holds 8 blocks of 4 bytes each. Assuming that each memory address has 8 bits, to which cache set would

the hexadecimal address 0x1F map if the computer uses 2-way set associative mapping?

Answer: Set 3 (11)
Topic: Cache Memory
Difficulty: Medium
Page: 361

46. Suppose the cache access time is 10ns, main memory access time is 200ns, and the cache hit rate is 90%. Assuming parallel (overlapped) access, what is the average access time for the processor to access an item?

Answer: 29ns
Topic: Cache Memory
Difficulty: Medium
Page: 367

47. Consider a byte-addressable computer with 24-bit addresses, a cache capable of storing a total of 64K bytes of data, and blocks of 32 bytes. Show the format of a 24-bit memory address if the computer uses direct mapping.

Answer:

Tag	Block	Offset
8	11	5

Topic: Cache Memory
Difficulty: Medium
Page: 352

48. Consider a byte-addressable computer with 24-bit addresses, a cache capable of storing a total of 64K bytes of data, and blocks of 32 bytes. Show the format of a 24-bit memory address if the computer uses 4-way set associative mapping.

Answer:

Tag	Set	Offset
10	9	5

Topic: Cache Memory
Difficulty: Medium
Page: 358

49. Given a computer using a byte-addressable virtual memory system with a two-entry TLB, a 2-way set associative cache, and a page table for a process P. Assume cache blocks of size 8 bytes. Assume pages of size 16 bytes and a main memory of 4 frames. Assume the following TLB and page table for Process P:

TLB	
0	3
4	1

	Page Table	
	f	Valid
0	3	1
1	0	1
2	-	0
3	2	1
4	1	1
5	-	0
6	-	0
7	-	0

How many bits are in a virtual address for process P?

Answer: 7
Topic: Virtual Memory
Difficulty: Medium
Page: 376

50. Given a computer using a byte-addressable virtual memory system with a two-entry TLB, a 2-way set associative cache, and a page table for a process P. Assume cache blocks of size 8 bytes. Assume pages of size 16 bytes and a main memory of 4 frames. Assume the following TLB and page table for Process P:

TLB	
0	3
4	1

	Page Table	
	f	Valid
0	3	1

1	0	1
2	-	0
3	2	1
4	1	1
5	-	0
6	-	0
7	-	0

How many bits are in a physical address?

Answer: 6
Topic: Virtual Memory
Difficulty: Medium
Page:

51. Given a computer using a byte-addressable virtual memory system with a two-entry TLB, a 2-way set associative cache, and a page table for a process P. Assume cache blocks of size 8 bytes. Assume pages of size 16 bytes and a main memory of 4 frames. Assume the following TLB and page table for Process P:

TLB	
0	3
4	1

	Page Table	
	f	Valid
0	3	1
1	0	1
2	-	0
3	2	1
4	1	1
5	-	0
6	-	0
7	-	0

Show the address format for virtual address 0x12.

Answer:

Page (3 bits)	Offset (4 bits)
0001	0010

Topic: Virtual Memory

Difficulty: Medium

Page: 377

52. Given a computer using a byte-addressable virtual memory system with a two-entry TLB, a 2-way set associative cache, and a page table for a process P. Assume cache blocks of size 8 bytes. Assume pages of size 16 bytes and a main memory of 4 frames. Assume the following TLB and page table for Process P:

TLB	
0	3
4	1

	Page Table	
	f	Valid
0	3	1
1	0	1
2	-	0
3	2	1
4	1	1
5	-	0
6	-	0
7	-	0

List the steps necessary to convert the virtual address 0x06 to a physical address and give that address.

Answer: Divide the address into page/offset fields to get:

Page (3 bits)	Offset (4 bits)
000	0110

Then use the page 000 to check the TLB for an entry for page 0. It is found in the TLB, so substitute page 000 with frame 11 to get the physical address 110110, or 0x36.
Topic: Virtual Memory
Difficulty: Hard
Page: 384

True/False

1. A standard monitor is the only output device that presents results to the user.

<Answer: True>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 401

Multiple Choices Static

2. _____ follows closely behind the CPU and memory in determining the overall effectiveness of a computer system.

A. Drive I/O
B. Disk I/O
C. I/O
D. none of the above

<Answer: B>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 405

3. The signals exchanged between a sender and a receiver is called a _____

A. protocol
B. prototype
C. message
D. rule

<Answer: B>

Topic: Input/Output and Storage Systems

Difficulty: Easy

Page: 407

True/False

4. The simplest way for a CPU to communicate with an I/O device is through polled I/O

<Answer: True>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 407

Multiple Choices Static

5. The large computer systems use an intelligent type of DMA interface known as _____

A. I/O channel
B. memory-mapped I/O
C. interrupt-driven I/O
D. memory I/O

<Answer: A>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 413

6. CCW means

A. channel command words
B. channel connections words
C. channel command works
D. change command words

<Answer: A>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 413

True/False

7. Channel I/O is a type of non-isolated I/O because the systems are equipped with separate I/O buses.

<Answer: False>

Topic: Input/Output and Storage Systems

Difficulty: Easy

Page: 416

Multiple Choices Static

8. Buses having memory on its own do memory transfer _____

A. asynchronously
B. synchronously
C. parallelly
D. randomly

<Answer: B>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 418

True/False

9. Two types of transmission modes are serial and parallel transmission modes.

<Answer: True>

Topic: Input/Output and Storage Systems

Difficulty: Easy

Page: 420

10. Serial transfer methods can be used for time-sensitive isochronous data transfers.

<Answer: True>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 423

Multiple Choices Static

11. _____are divisions of concentric circles called tracks in disk drives.

A. Sectors
B. Segments
C. Paths
D. Symmetry

<Answer: A>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 425

True/False

12. Cylinders describe circular areas on each disk in Rigid Disk Drives.

<Answer: True>

Topic: Input/Output and Storage Systems

Difficulty: Easy

Page: 425

Multiple Choices Static

13. If a read/write head in Rigid Disk Drives were to touch the surface of the disk, the disk would become unusable. This condition is known as a _____

A. head crash
B. head corrupt
C. head clean
D. head burn

<Answer: A>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 426

14. COLD means

A. computer output laser disc
B. computer output laser direct
C. computer organization laser disc
D. compact output laser disc

<Answer: A>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 432

15. Lineal spaces between the pits in a CD-ROM are called _____

A. tracks
B. segments
C. lands
D. circles

<Answer: C>

Topic: Input/Output and Storage Systems

Difficulty: Difficult

Page: 432

True/False

16. Rewritable optical media replace the dye and reflective coating layers of a CD-R disk with a non-metallic alloy.

<Answer: False>

Topic: Input/Output and Storage Systems

Difficulty: Easy

Page: 438

17. The storage systems that are not protected by RAID are known as just a bunch of disks (JBOD).

<Answer: False>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 444

18. RAID Level 1, or RAID-1, is also known as disk mirroring.

<Answer: True>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 445

19. A hologram is a three-dimensional image rendered by the manipulation of laser beams.

<Answer: True>

Topic: Input/Output and Storage Systems

Difficulty: Medium

Page: 454

20. Memristor memories are a type of volatile RAM.

<Answer: False>

Topic: Input/Output and Storage Systems

Difficulty: Difficult

Page: 457

True/False

21. The I/O modules take care of data movement between main memory and a particular device interface.

<Answer: True>

Topic: Input/Output and Storage Systems
Difficulty: Easy
Page: 406

Multiple Choices Static

22. A simpler and more elegant approach is memory-mapped I/O because I/O devices and main memory share the _____.

A. same memory space
B. same address space
C. same register
D. same interface

<Answer: B>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 411

23. Electrical signal loss over time or distance during data transfer is called an _____.

A. attention
B. attribute
C. attenuation
D. attendention

<Answer: C>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 415

24. The extra line used for synchronization in parallel data transmission is called a _____.

A. throbe
B. strobe
C. channel
D. stroke

<Answer: B>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 420

True/False

25. Solid-state drives consist of a microcontroller and flash memory.

<Answer: True>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 429

Multiple Choices Static

26. _____ is a technique that distributes data and erase/write cycles evenly over the entire disk to extend the life of the disk.

A. Wear labeling
B. Wear leveling
C. Wear tearing
D. Wear sequencing

<Answer: B>

Topic: Input/Output and Storage Systems
Difficulty: Difficult
Page: 430

27. DVDs rotate at about _____ times the speed of CDs.

A. two
B. Three
C. four
D. five

<Answer: B>

Topic: Input/Output and Storage Systems
Difficulty: Easy
Page: 436

28. Ultra Density Optical disks can store up to _____ and _____ respectively.

A. 23GB and 60GB
B. 23GB and 64GB
C. 20GB and 60GB
D. 24GB and 60GB

<Answer: A>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 437

29. Systems that require high availability and must be able to tolerate more than one concurrent drive failure use_____.

A. RAID 1
B. RAID 2
C. RAID 3
D. RAID 6

<Answer: D>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 449

True/False

30. Large systems are also limited to using only one type of RAID.

<Answer: False>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 452

Multiple Choices Static

31. _____ devices offer another approach to transcend the limits of magnetic storage.

A. Micro-electronic-mechanical
B. Micro-electro-magnetic
C. Micro-electro-mechanical
D. Macro-electro-mechanical

<Answer: C>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 456

32. Holographic data storage stores enormous data density by using _____.

A. one-dimensional medium
B. two-dimensional medium
C. three-dimensional medium
D. n-dimensional medium

<Answer: C>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 455

33. MTTR means

A. Mean Time To Repeat
B. Mean Time To Repair
C. Mean Time To Report
D. Median Time To Repair

<Answer: B>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 449

True/False

34. The disadvantage of RAID-1 is that it is costly and requires large memory space.

<Answer: True>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 445

35. Like RAID-6, RAID DP can tolerate the simultaneous loss of two disk drives without loss of data.

<Answer: True>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 450

Multiple Choices Static

36. _____ law states the interrelationship of all components with the overall efficiency of a computer system with a simple formula.

A. Amdahl's
B. Ambhal's
C. Amdad's
D. Amda's

<Answer: A>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 402

37. Disk and tape are forms of _____ storage.

A. durable
B. sequential

C. random
D. direct

<Answer: A>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 407

True/False

38. I/O channels are driven by small CPUs called I/O processors (IOPs).

<Answer: True>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 413

Multiple Choices Static

39. Engineers describe bus operation through clearer and precise pictures known as _____.

A. timing diagrams
B. sequential diagrams
C. direct diagrams
D. circuit diagrams

<Answer: A>

Topic: Input/Output and Storage Systems
Difficulty: Easy
Page: 419

True/False

40. Disk drives sometimes “skip around” to allow time for the drive circuitry to process the contents of a sector prior to reading the next sector. This is called as interpathing.

<Answer: False>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 425

Multiple Choices Static

41. CD-ROMs are are made up of _____.

A. polyester
B. polycarbonate
C. polysynthetic
D. polycarbon

<Answer: B>

Topic: Input/Output and Storage Systems
Difficulty: Medium
Page: 432

42. _____ is the oldest and most cost-effective of all mass-storage devices .

A. Magnetic drive
B. Compact dick
C. Magnetic tape
D. Floppy disk

<Answer: C>

Topic: Input/Output and Storage Systems
Difficulty: Easy
Page: 439

43. In RAID-2, the error-correction information generated in additional drive is using _____.

A. Hamming code
B. Humming code
C. spanning code
D. hamming table

<Answer: A>

Topic: Input/Output and Storage Systems

Difficulty: Medium
Page: 445

44. Big data is measured in _____ bytes.

A. mega
B. kilo
C. tera
D. giga

<Answer: C>

Topic: Input/Output and Storage Systems
Difficulty: Easy
Page: 457

True/False

45. RAID-2 writes one bit per strip instead of writing data in blocks of arbitrary size.

<Answer: True>

Topic: Input/Output and Storage Systems
Difficulty: Difficult
Page: 445

True/False

1. RISC machines originally offered a smaller instruction set compared with CISC machines.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Easy
Page: 550

2. CISC architectures include a large number of instructions that directly access memory.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Medium

Page: 551

Multiple Choices Static

3. CISC machines rely on _____ to tackle instruction complexity.

A. macrocode
B. microcode
C. nanocode
D. bytecode

<Answer: B>

Topic: Alternative Architectures
Difficulty: Easy
Page: 552

True/False

4. Most of the CPU architectures today have a combination of RISC and CISC.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Medium
Page: 555

Multiple Choices Static

5. _____ considers two factors: the number of instructions and the number of data streams that flow into the processor.

A. Flynn's taxonomy
B. Faynn's taxonomy
C. Flyan's taxonomy
D. Flewnn's taxonomy

<Answer: A>

Topic: Alternative Architectures
Difficulty: Medium
Page: 557

6. There are two major parallel architectural paradigms, _____ and _____.

A. Single multiprocessors (SMPs), massively parallel processors (MPPs)
B. symmetric multiprocessors (SMPs), multiple parallel processors (MPPs)
C. systematic multiprocessors (SMPs), massively parallel processors (MPPs)
D. symmetric multiprocessors (SMPs), massively parallel processors (MPPs)

<Answer: D>

Topic: Alternative Architectures
Difficulty: Difficult
Page: 558

True/False

7. Program instructions act on the data, unlike data-driven, or dataflow, architectures.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Medium
Page: 560

Multiple Choices Static

8. The superscalar components analogous to our additional highway lanes are called _____units.

A. execution
B. production
C. transaction
D. compilation

<Answer: A>

Topic: Alternative Architectures
Difficulty: Medium
Page: 562

True/False

9. Interconnection networks can be either static or dynamic.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Easy

Page: 565

Multiple Choices Static

10. Multistage networks are often called _____ networks.

A. shuffle
B. ruffle
C. shunt
D. shuttle

<Answer: A>

Topic: Alternative Architectures
Difficulty: Medium
Page: 568

11. Shared memory MIMD machines can be divided into two categories: _____ and _____.

A. UMA, NUMA
B. VMA, NVMA
C. UUA, NUUA
D. UMA, DUMA

<Answer: A>

Topic: Alternative Architectures
Difficulty: Difficult
Page: 571

True/False

12. Pervasive computing are the systems that are totally embedded in the environment, simple to use, completely connected, typically mobile, and often invisible.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Medium
Page: 575

13. Cloud computing and the classical distributed computing are not the same in all of the concepts they use.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Medium
Page: 576

14. Neural network computers are composed of a large number of simple processing elements that individually handle one piece of a much larger problem.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Easy
Page: 580

Multiple Choices Static

15. _____ computers derive their name from drawing an analogy to how blood rhythmically flows through a biological heart.

A. Systonic array
B. Symbolic array
C. Systolic array
D. Systoly array

<Answer: C>

Topic: Alternative Architectures
Difficulty: Medium
Page: 582

True/False

16. DNA computing uses DNA as software and enzymes as hardware.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Easy
Page: 584

Multiple Choices Static

17. The realization of _____ computing has prompted many to consider what is known as the technological singularity.

A. quanum
B. quadratic

C. quandum
D. quantum

<Answer: D>

Topic: Alternative Architectures
Difficulty: Difficult
Page: 587

18. _____ are trained by use of either supervised or unsupervised learning algorithms.

A. Perceptron
B. Proton
C. Perton
D. Percepton

<Answer: A>

Topic: Alternative Architectures
Difficulty: Medium
Page: 581

19. The computation sequence of a dataflow computer can be understood by examining its _____ graph.

A. dataflow
B. flow
C. sequence flow
D. data draw

<Answer: A>

Topic: Alternative Architectures
Difficulty: Medium
Page: 577

20. Public-resource computing is also known as _____ computing.

A. global
B. local
C. static
D. dynamic

<Answer: A>

Topic: Alternative Architectures
Difficulty: Medium

Page: 574

True/False

21. The analogy of human languages can be compared with the qualities of RISC and CISC.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Medium
Page: 551

Multiple Choices Static

22. High-level languages depend on _____ for efficiency.

A. modularization
B. modularity
C. modernization
D. multiplexing

<Answer: A>

Topic: Alternative Architectures
Difficulty: Easy
Page: 554

23. SIMD means

A. single instruction stream, multiple display streams
B. single instrument stream, multiple data streams
C. single instruction stream, multiple data streams
D. single instruction stream, multiple device streams

<Answer: C>

Topic: Alternative Architectures
Difficulty: Difficult
Page: 557

24. A _____ is a collection of distributed workstations that works in parallel only while the nodes are not being used as regular workstations.

A. network of servers
B. network of nodes

C. collection of workstations
D. network of workstations

<Answer: D>

Topic: Alternative Architectures
Difficulty: Medium
Page: 559

True/False

25. VLIW processors rely entirely on the compiler rather than on the hardware.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Medium
Page: 563

Multiple Choices Static

26. Like _____, EPIC bundles its instructions for delivery to various execution units.

A. VLIW
B. VLIV
C. WLIW
D. VLLW

<Answer: A>

Topic: Alternative Architectures
Difficulty: Medium
Page: 563

True/False

27. Switching networks use switches to dynamically alter routing.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Easy
Page: 567

28. Distributed computing is another form of multiprocessing.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Medium
Page: 573

Multiple Choices Static

29. _____ extend the concept of distributed computing and help provide the necessary transparency for resource sharing

A. Remote procedure calls (RPCs)
B. Remote program calls (RPCs)
C. Remote procedure codes (RPCs)
D. Remote protocol calls (RPCs)

<Answer: A>

Topic: Alternative Architectures
Difficulty: Medium
Page: 575

30. The example of a neural net is the _____ a single trainable neuron.

A. perceptron
B. proton
C. perton
D. percepton

<Answer: A>

Topic: Alternative Architectures
Difficulty: Medium
Page: 580

True/False

31. Optical computing uses photons instead of electrons to perform logic in a computer.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Easy
Page: 584

Multiple Choices Static

32. The first company in the world to manufacture and sell what it identifies as a quantum computer was _____.

A. Wave Computers
B. B-Wave Computers
C. D-Wave Computers
D. E-Wave Computers

<Answer: C>

Topic: Alternative Architectures
Difficulty: Medium
Page: 585

True/False

33. Biological computing uses components from living organisms instead of inorganic silicon ones.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Difficult
Page: 587

34. One obstacle is the tendency for qubits to decay into a single incoherent state (called decoherence), which leads to inconsistency of data.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Difficult
Page: 587

Multiple Choices Static

35. _____ are typically used for repetitive tasks, for example, Fourier transformations, image processing, data compression, and shortest path problems.

A. Systonic array
B. Symbolic array
C. Systolic array
D. Systoly array

<Answer: C>

Topic: Alternative Architectures
Difficulty: Easy
Page: 583

Multiple Choices Static

36. Only explicit load and store instructions were permitted access to memory in _____ machines.

A. RISC
B. CISC
C. FISC
D. RSIC

<Answer: A>

Topic: Alternative Architectures
Difficulty: Medium
Page: 551

True/False

37. The RISC clock cycles are often longer than CISC clock.

<Answer: False>

Topic: Alternative Architectures
Difficulty: Medium
Page: 553

Multiple Choices Static

38. _____ has focused on efficiency in the mobile and embedded systems market.

A. ARM
B. RAM
C. AARM
D. RMA

<Answer: A>

Topic: Alternative Architectures
Difficulty: Easy
Page: 557

True/False

39. The problem with Flynn's taxonomy is with the MIMD category; it considers how the processors are connected and the memory is viewed.

<Answer: False>

Topic: Alternative Architectures
Difficulty: Medium
Page: 558

40. A pile of PCs (PoPC) is a cluster of dedicated heterogeneous hardware used to build a parallel system out of mass market commodity components, or COTs.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Medium
Page: 559

41. Super pipelining occurs when a pipeline has stages that require less than two o'clock cycle to execute.

<Answer: False>

Topic: Alternative Architectures
Difficulty: Difficult
Page: 562

Multiple Choices Static

42. _____networks are those in which all components are connected to all other components.

A. Completely connected
B. Ring
C. Bus
D. Mesh

<Answer: A>

Topic: Alternative Architectures
Difficulty: Medium

Page: 565

43. Specially designed hardware units, known as _____, monitor inconsistencies in data on the system.

A. snoopy vector controllers
B. snoopy common controllers
C. snoopy cache controllers
D. snoopy cache compilers

<Answer: C>

Topic: Alternative Architectures
Difficulty: Difficult
Page: 572

True/False

44. Data drives processing on dataflow systems, and dataflow multiprocessors do not suffer from the contention and cache coherency problems.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Easy
Page: 579

45. Quantum computers use quantum bits (qubits) that can be in multiple states simultaneously.

<Answer: True>

Topic: Alternative Architectures
Difficulty: Medium
Page: 584

Multiple Choices Static

1. Vector processors and parallel processors increase performance by reducing _____.

A. CPU time
B. Memory time
C. Output time
D. Compilation time

<Answer: A>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 634

True/False

2. Mathematical and statistical tools give us many ways to rate the overall performance of a system and its components.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 635

Multiple Choices Static

3. Measures of_____ indicate to us the expected behavior of the sampled system.

A. central tendency
B. Throughput
C. response time
D. Compilation time

<Answer: A>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 636

4. It would be easy for the computer buyer if there were some way to classify systems according to a _____.

A. Metric
B. Method
C. Ranking
D. Cadre

<Answer: A>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 643

True/False

5. A CPU running at double the clock speed of another is likely to give better CPU throughput.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 644

Multiple Choices Static

6. SPEC stands for_____.

A. System Performance Evaluation Corporation
B. Standard Performance Evaluation Computer
C. Standard Perdominant Evaluation Corporation
D. Standard Performance Evaluation Corporation

<Answer: D>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 648

7. The final collection of kernel programs is called a_____.

A. Benchmark suite.
B. Benchmark group
C. Benchmark route
D. Benchmark tree

<Answer A>

Topic: Performance Measurement and Analysis
Difficulty: medium
Page: 648

8. _____ benchmarks are helpful to computer buyers whose prime concern is CPU performance.

A. TP CPU
B. SPEC’s CPU

C. CPA CPU
D. PEC’s CPU

<Answer: B>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 651

9. The _____ benchmarking suite models the activities of a wholesale product distribution company.

A. TPC-C
B. TPC-D
C. TPC-E
D. TPC-F

<Answer: A>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 634

10. The TPC produced two benchmarks,_____ and _____, to describe the performance of decision support systems through OLTP.

A. TPC-H,TPC-E
B. TPC-H,TPC-R
C. TPC-U,TPC-R
D. TPC-G,TPC-R

<Answer: B>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 657

True/False

11. Branch prediction is the process of attempting to guess the next instruction in the instruction stream.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: difficult

Page: 661

12. In branching, static prediction and fixed prediction are the same.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 662

Multiple Choices Static

13. _____ is an important tool for improving program performance.

A. Loop fusion
B. Loop optimization
C. Loop breaking
D. Loop triping

<Answer: B>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 665

14. A CPU needs only a few _____ to execute an instruction when all operands are in its registers.

A. Nanoseconds
B. Microseconds
C. Seconds
D. Minutes

<Answer: A>

Topic: Performance Measurement and Analysis

Difficulty: easy

Page: 666

True/False

15. Disk scheduling can be a function of either the disk controller or the host operating system.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 668

16. The elevator algorithm works much similar to how skyscraper elevators service their passengers.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 669

17. Caches with battery backups are costly.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: easy

Page: 673

Multiple Choices Static

18. _____ is the process of removing the beginning or ending statements from a loop.

A. Loop peeling
B. Loop fusion
C. Loop optimization
D. Loop breaking

<Answer:A>

Topic: Performance Measurement and Analysis

Difficulty: difficult

Page:665

19. SSTF stands for _____.

A. Shortest seek time first

B. Shortest standard time first

C. Small seek time first

D. Shortest seek time found

<Answer:A>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 669

True/False

20. When throughput is more important than reliability, a system may employ the write-back cache policy.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: easy

Page: 673

Multiple Choices Static

21. A computer user is most concerned with_____.

A. response time

B. Compilation time

C. Seek time

D. Lead time

<Answer: A>

Topic: Performance Measurement and Analysis

Difficulty: medium

Page: 635

True/False

22. More time-consuming programs have greater influence on the harmonic mean.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: difficult

Page: 641

Multiple Choices Static

23. MIPS stands for _____.

A. minute of instructions per second
B. millions of instructions per sector
C. millions of instruments per second
D. millions of instructions per second

<Answer: D>

Topic: Performance Measurement and Analysis

Difficulty: easy

Page: 634

True/False

24. Clock speed, MIPS, and FLOPS are the metrics in comparing relative performance across a line of similar computers offered by the same vendor.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: medium

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Multiple Choices Static

25. The IBM Corporation invented a benchmark to help with the design of its mainframe systems it was called as _____.

A. TP1
B. TP2

C. TP3
D. TP4

<Answer: A>

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Difficulty: medium

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True/False

26. The TPC has recently improved (but not yet replaced) the TPC-C benchmark.

<Answer: True>

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Difficulty: difficult

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True/False

27. Simulation is very useful for estimating the performance of systems or system configurations that only exist.

<Answer False>

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Difficulty: medium

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Multiple Choices Static

28. Modern processors have increasingly longer _____.

A. pipelines.
B. Queues
C. Streams
D. process

<Answer: A>

Topic: Performance Measurement and Analysis

Difficulty: medium

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Multiple Choices Static

29. _____ is one method of dealing with the effects branching on pipelines.

A. Delayed branching
B. Queues branching
C. Streams branching
D. process branching

<Answer: A>

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Difficulty: medium

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Multiple Choices Static

30. _____ is one way to enhance the performance of your program.

A. Operation counting
B. Branch counting
C. Looping
D. snooping

<Answer: A>

Topic: Performance Measurement and Analysis

Difficulty: easy

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Multiple Choices Static

31. _____ combines loops that use the same data items.

A. Loop fusion
B. Loop optimization
C. Loop breaking
D. Loop triping

<Answer: A>

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Difficulty: medium

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True/False

32. Disk utilization, the measure of the percentage of time that the disk is busy servicing I/O requests.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: medium

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Multiple Choices Static

33. _____ is moving the disk arm from the innermost track to the outermost, or vice versa

A. full-stroke seek.
B. Fool stoke seek
C. Greek seek
D. Stroke seek

<Answer: A>

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Difficulty: medium

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True/False

34. Disks should not be defragmented, or reorganized, on a regular basis.

<Answer: False>

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Difficulty: medium

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True/False

35. Disk cache memory is usually associative memory type.

<Answer: True>

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Difficulty: medium

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Multiple Choices Static

36. _____ occurs when the cache is filled with data that needs no process leaving less space for useful data.

A. Cache processing
B. Cache pollution
C. Cache pollination
D. Cache polling

<Answer: B>

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Difficulty: medium

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True/False

37. Prefetching is conceptually similar to CPU-to-memory caching.

<Answer: True>

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Difficulty: medium

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38. CPU optimization is not the only way to increase system performance.

<Answer: True>

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Difficulty: medium

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Multiple Choices Static

39. The _____ allows us to form a mathematical expectation of throughput and to compare the relative throughput of systems or system components.

A. harmonic mean

B. Geometric mean

C. Arithmetic mean

D. Median mean

<Answer: A>

Topic: Performance Measurement and Analysis

Difficulty: medium

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True/False

40. A rhetorical logic, this is called the argumentum ad verecundiam.

<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: medium

Multiple Choices Static

41. Three of the best known synthetic benchmarks are the _____ and _____.

A. Wheatstone, Linpack, and Dhrystone metrics.

B. Whetstone, Linpack, and Dhrystone metrics.

C. Whetstone, Linpad, and Dhrystone metrics.

D. Whetstone, Linpack, and Drystone metrics.

<Answer: B>

Topic: Performance Measurement and Analysis

Difficulty: difficult

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True/False

42. TPC-A is now in the fifth version of its third major revision, TPC-C Version 5.
<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: medium

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Multiple Choices Static

43. The _____ benchmark simulates an online brokerage.
A. TPC-C
B. TPC-D
C. TPC-E
D. TPC-F

<Answer: C>

Topic: Performance Measurement and Analysis

Difficulty: medium

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True/False

44. One of the major challenges of system simulation lies in determining the characteristics of the workload.
<Answer: True>

Topic: Performance Measurement and Analysis

Difficulty: medium

Multiple Choices Static

45. _____ gather detailed behavior information using hardware or software probes into the activity of the component of interest.
A. System traces
B. System drives
C. System trap
D. System process

<Answer: A>

Topic: Performance Measurement and Analysis

Difficulty: easy

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