Logical Design

CS 221

Prof.Dr. Mohamed Osama Khozium

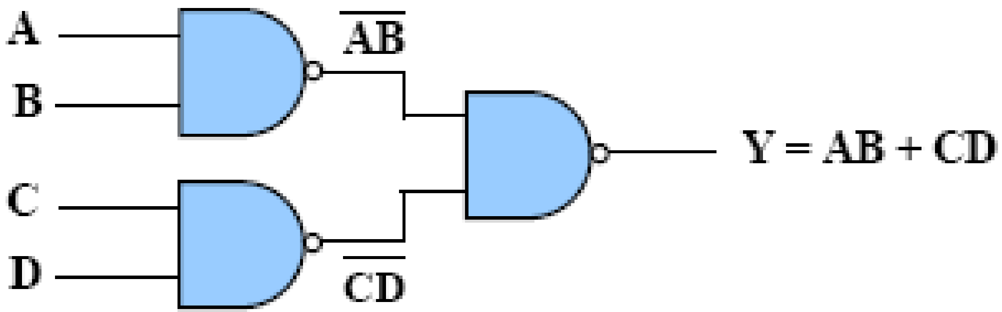
Combinational logic circuits

NOR & NAND
XOR & XNOR
Half & Full Adder
Decoder
Multiplexer

$$\overline{A \bullet B} = \overline{A} + \overline{B}$$

NAND Negative-OR

Example



$$Y = \overline{(\overline{AB})(\overline{CD})}$$

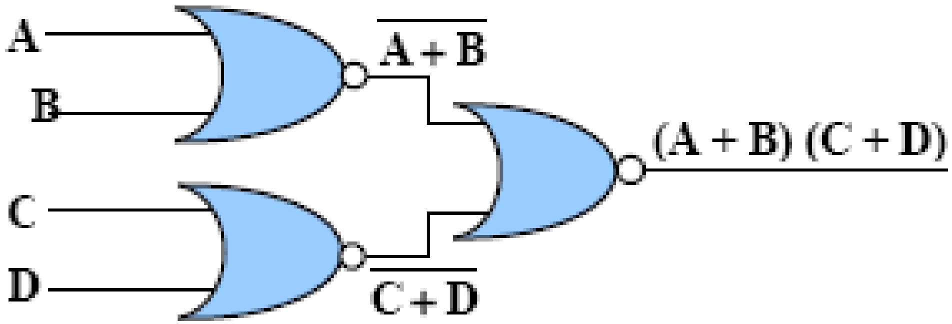
From Demorgan Theorem

$$Y = \overline{\overline{AB}} + \overline{\overline{CD}}$$

Then Y = AB + CD

$$\overline{A+B} = \overline{A}\bullet\overline{B}$$

NOR Negative-AND



$$Y = \overline{(\overline{A+B}) + (\overline{C+D})}$$

From Demorgan Theorem

$$Y = (\overline{\overline{A+B}})\bullet(\overline{\overline{C+D}})$$

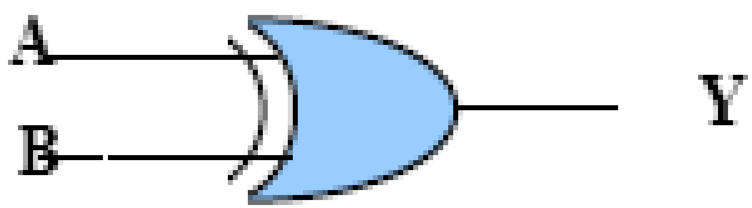
$$Y = (A+B)\bullet(C+D)$$

Exclusive-OR Gate XOR-gate

IN		OUT	
A	B	Y	
0	0	0	A'B'
0	1	1	A'B
1	0	1	AB'
1	1	0	AB

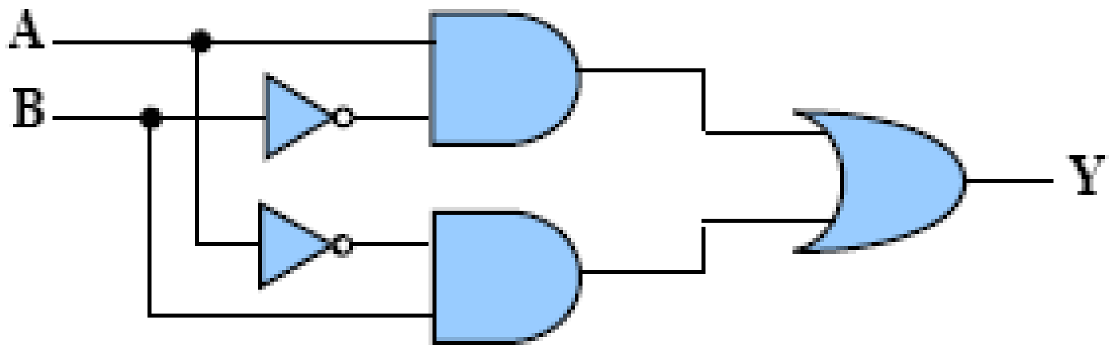
$$Y = \overline{A}B + A\overline{B}$$

$$Y = A \oplus B$$



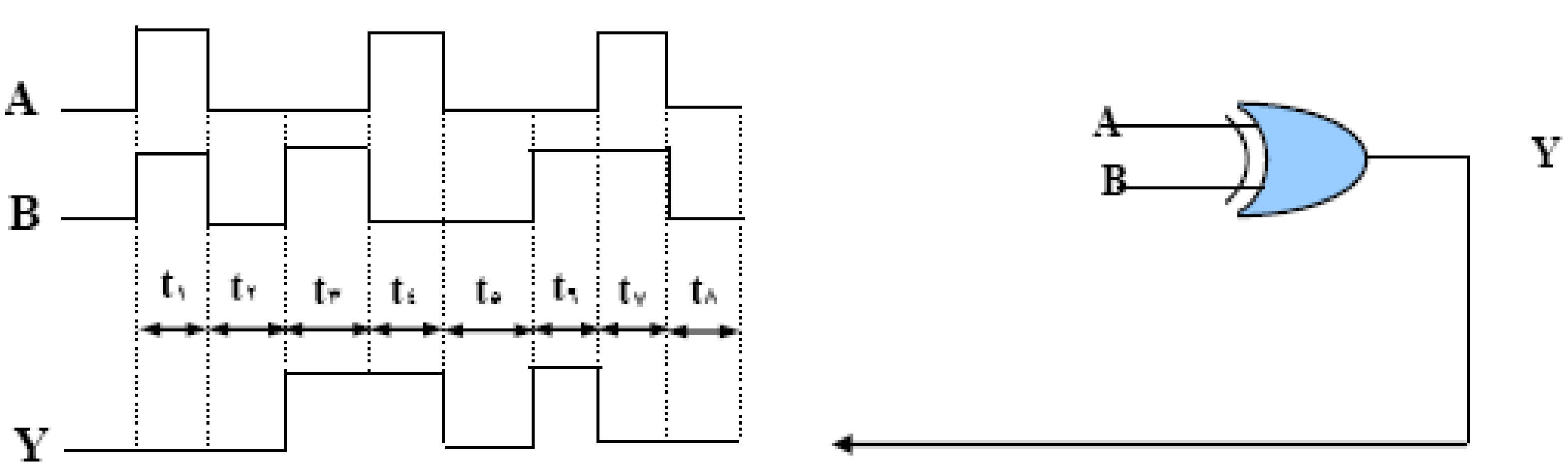
$$Y = \overline{A}B + A\overline{B}$$

$$Y = A \oplus B$$



XOR represented by AND & OR & NOT

Timing Diagram



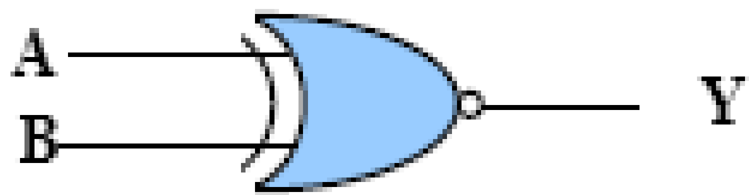
$$Y = A \oplus B$$

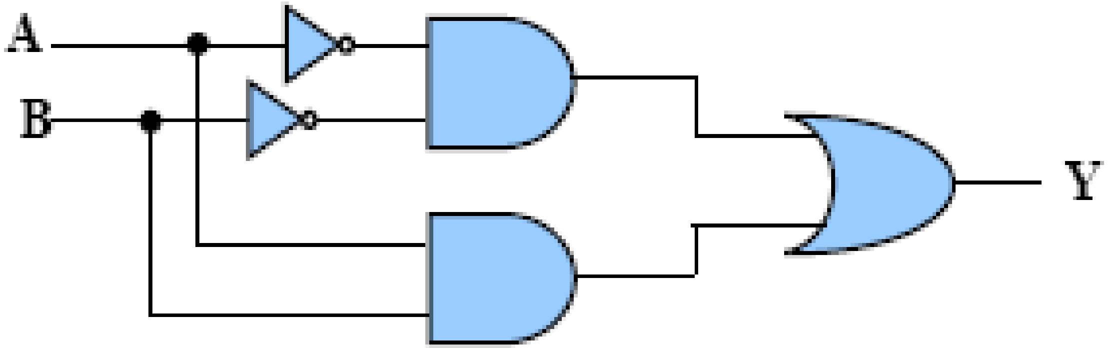
Exclusive-NOR Gate XNOR-gate

IN		OUT	
A	B	Y	
0	0	1	A'B'
0	1	0	A'B
1	0	0	AB'
1	1	1	AB

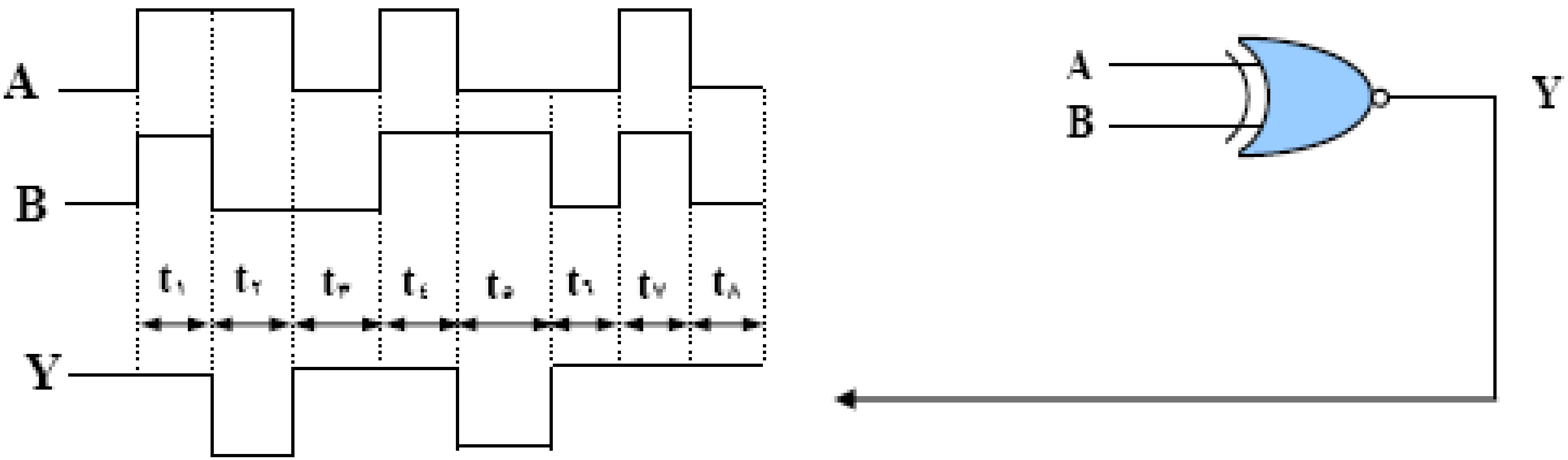
$$Y = AB + \overline{AB}$$

$$Y = A \odot B$$





XNOR represented by AND & OR & NOT


A
B
Y
t١
t٢
t٣
t٤
t٥
t٦
t٧
t٨
A
B
Y

Half Adder

Half Adder

Follow The Design Procedures

(1) Determine inputs : A & B
Determine outputs : S & C

(2) Derive the truth table :

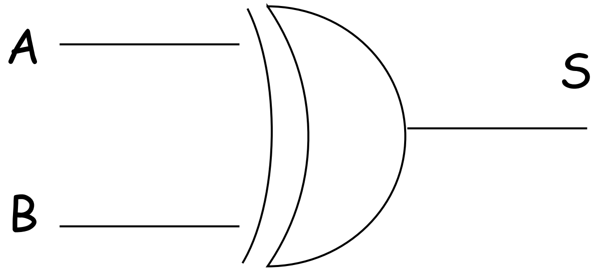
A	B		S	C
0	0		0	0
0	1		1	0
1	0		1	0
1	1		0	1

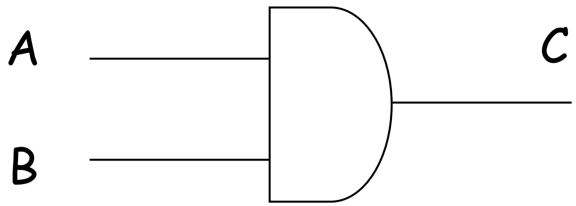
(3) Obtain the simplified Boolean functions :

$S = A'B + AB' = A \oplus B$

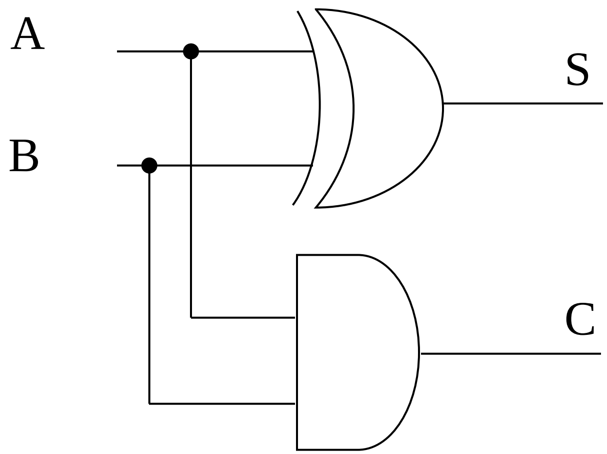
$C = AB$

(4) Draw the logic diagram :





(5) Verify the correctness of the design :



Full Adder

(1) Inputs : A, B Cin

Output : S, C

(2)

A	B	Cin		S	C
0	0	0		0	0
0	0	1		1	0
0	1	0		1	0
0	1	1		0	1
1	0	0		1	0
1	0	1		0	1
1	1	0		0	1
1	1	1		1	1

(3) $S = A' \, B' \, Cin + A' \, B \, Cin' + A \, B' \, Cin' + A \, B \, Cin$

$C = A' \, B \, Cin + A \, B' \, Cin + A \, B \, Cin' + A \, B \, Cin$

(3) $S = A'B'Cin + A'BCin' + AB'Cin' + ABCin$

$C = A'BCin + AB'Cin + ABCin' + ABCin$

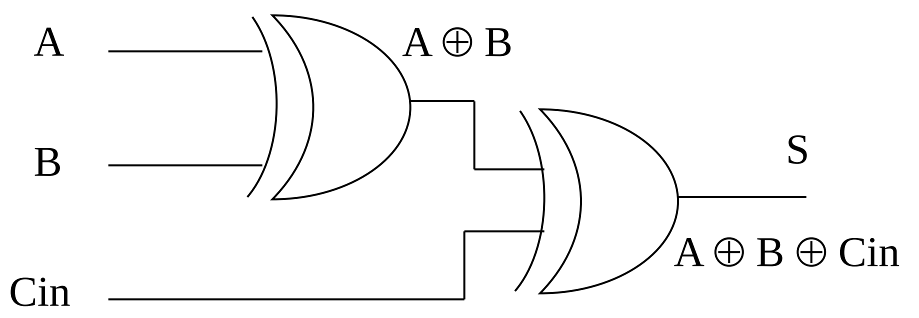
$S = (A'B + AB')Cin' + (A'B' + AB)Cin$

$= (A \oplus B)Cin' + (A \odot B)Cin$

$= (A \oplus B)Cin' + (\overline{A \oplus B})Cin$

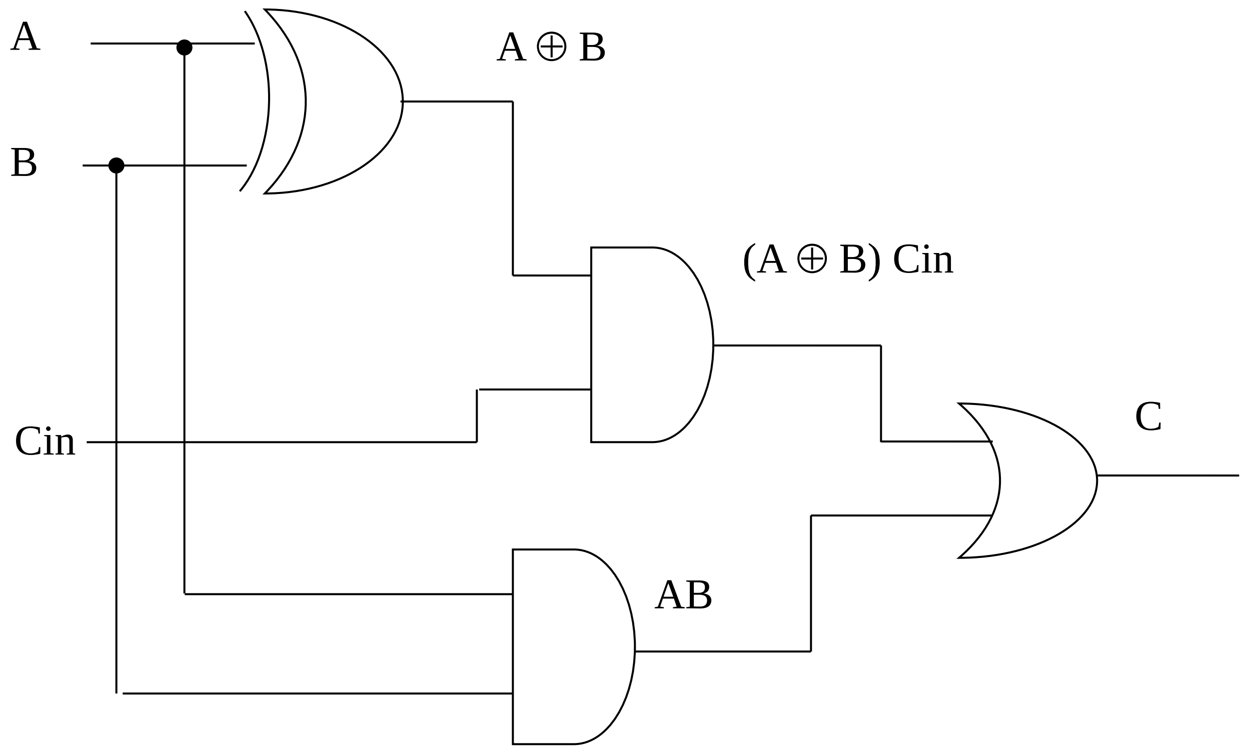
$= A \oplus B \oplus Cin$

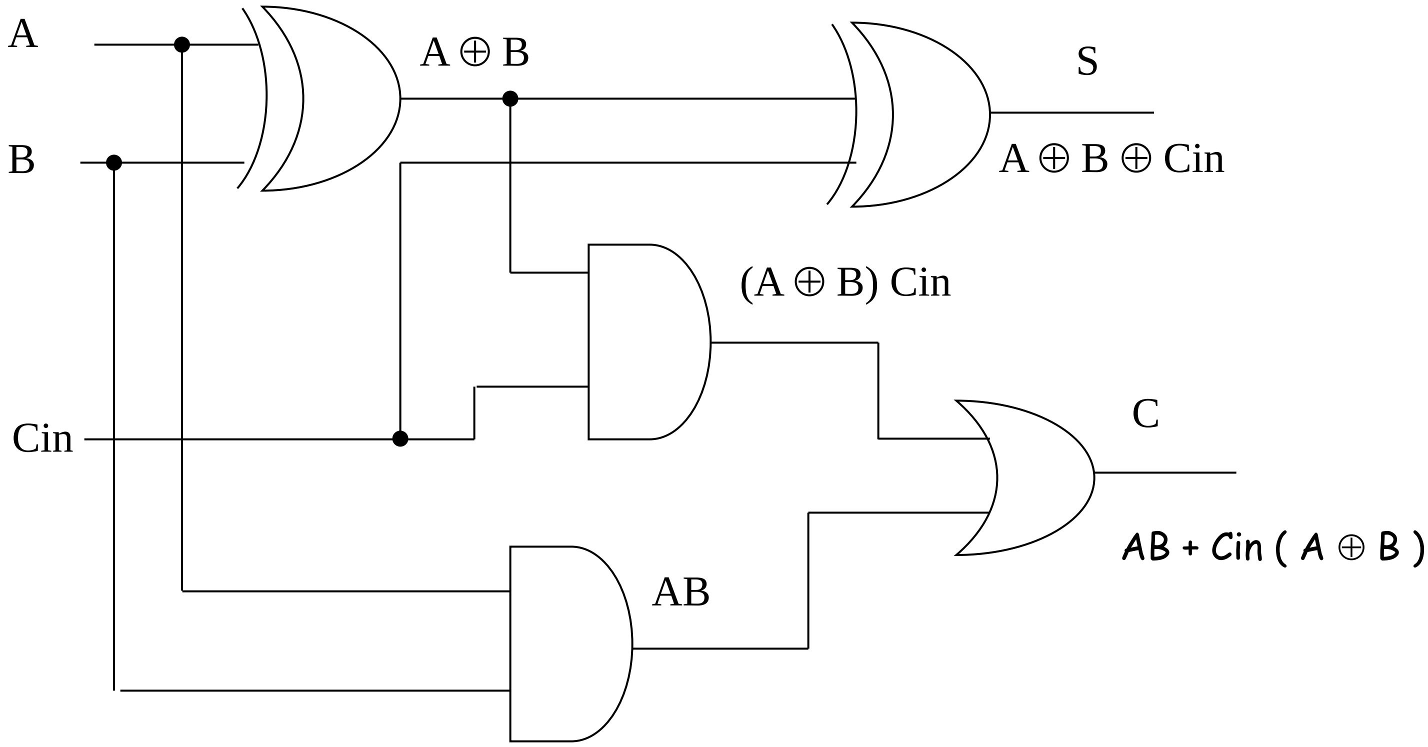
$$\boxed{\begin{array}{l} Cin = Y \;;\; A \oplus B = X \\ \therefore S = XY' + X'Y \Rightarrow S = X \oplus Y \end{array}}$$



$$C = AB\,(Cin + Cin') + Cin\,(A'B + AB')$$

$$= AB + Cin\,(A \oplus B)$$



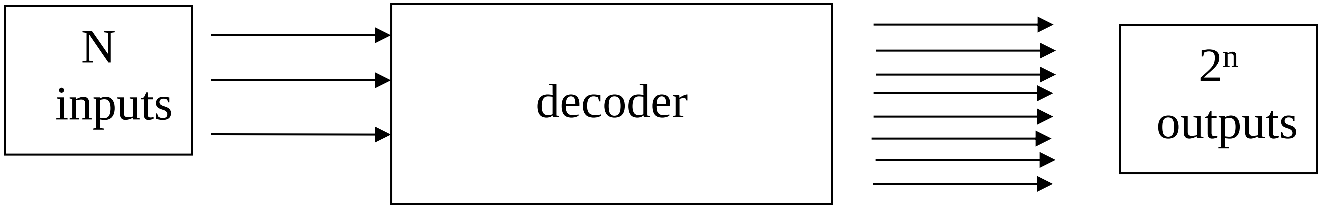


A
B
Cin
A ⊕ B
S
A ⊕ B ⊕ Cin
(A ⊕ B) Cin
C
AB + Cin (A ⊕ B)
AB

Decoders

Decoders are important type of combinational circuit.
Address decoders with n inputs can select any of 2^n locations.

They are useful in selecting a memory location according a binary value place don the address lines of a memory bas.



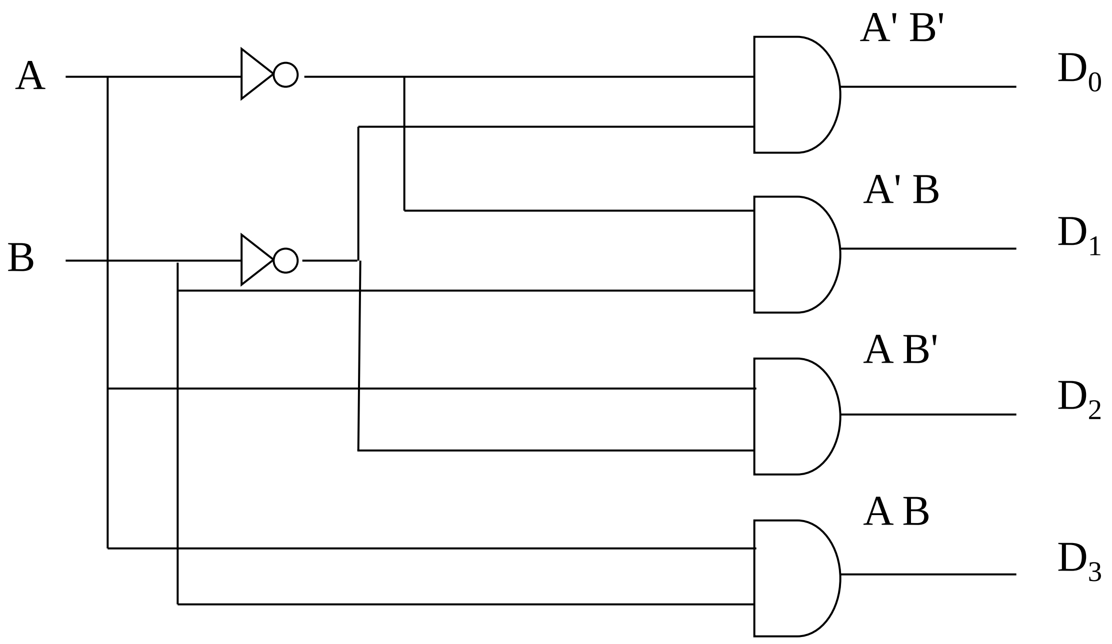
Black diagram for a decoder

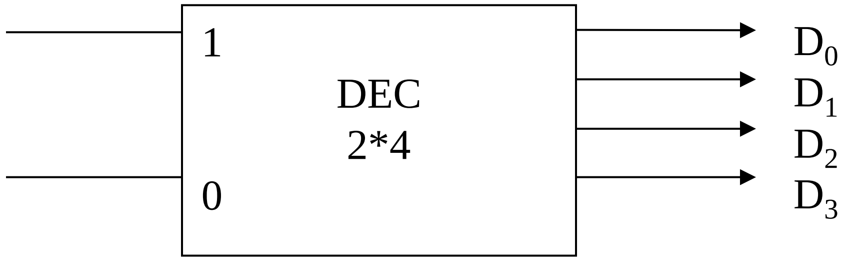
Decoder 2*4

	Inputs		Outputs			
	A	B	D3	D2	D1	D0
0	0	0	0	0	0	1
1	0	1	0	0	1	0
2	1	0	0	1	0	0
3	1	1	1	0	0	0

Inputs = 2

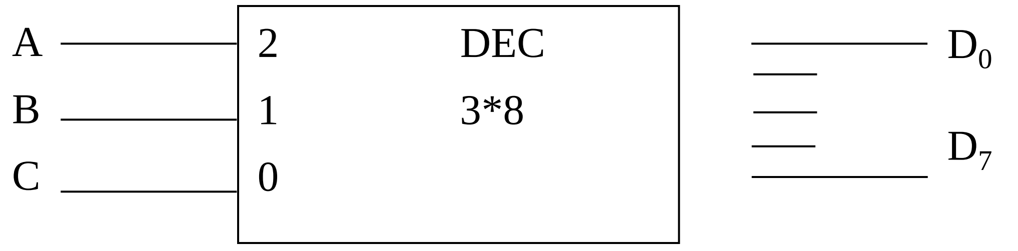
Outputs = 4



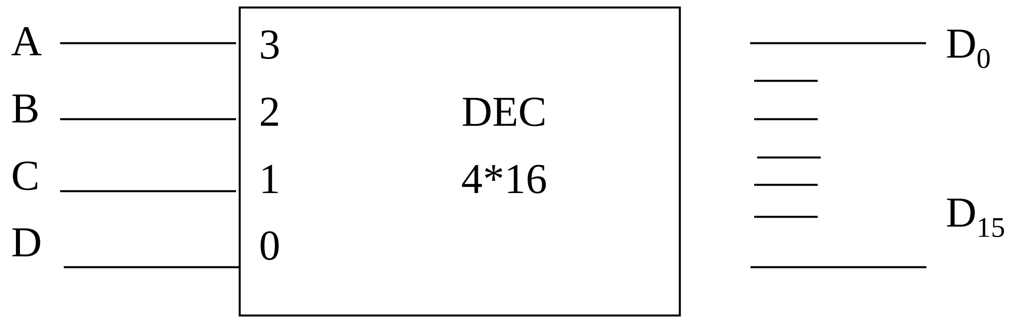


Decoder Block Diagram 2×4

Decoder 3*8



Decoder 4*16



Decoder with enable

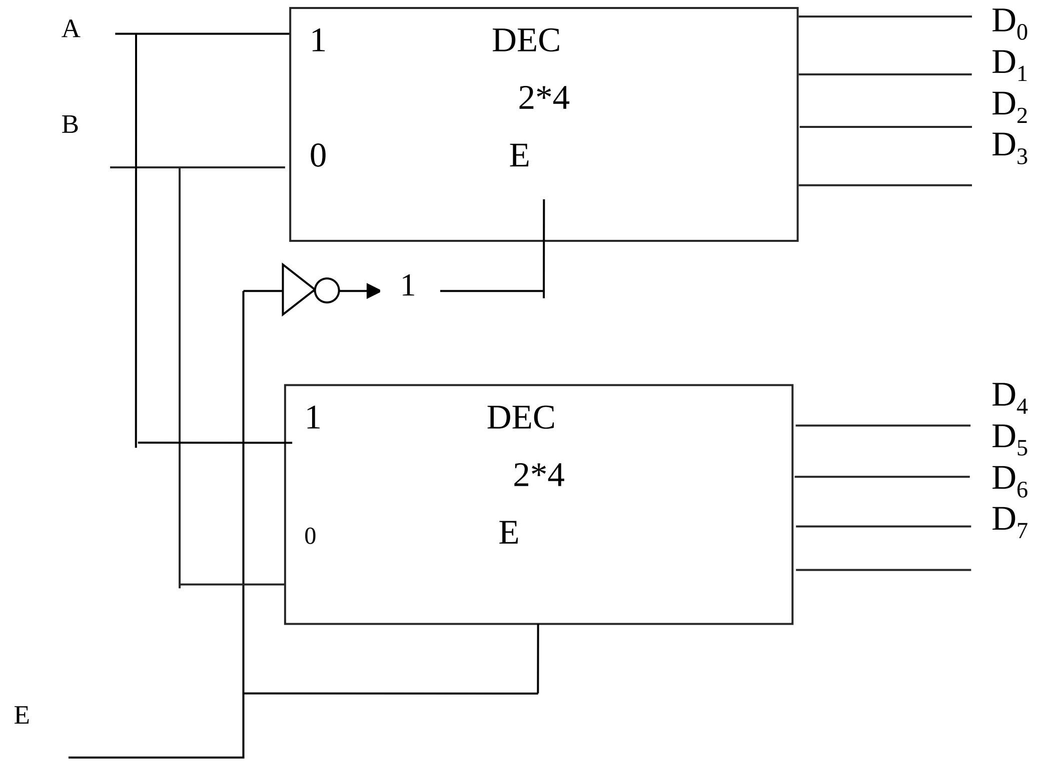
Decoder works when enable = 1

Decoder doesn't work when enable = 0

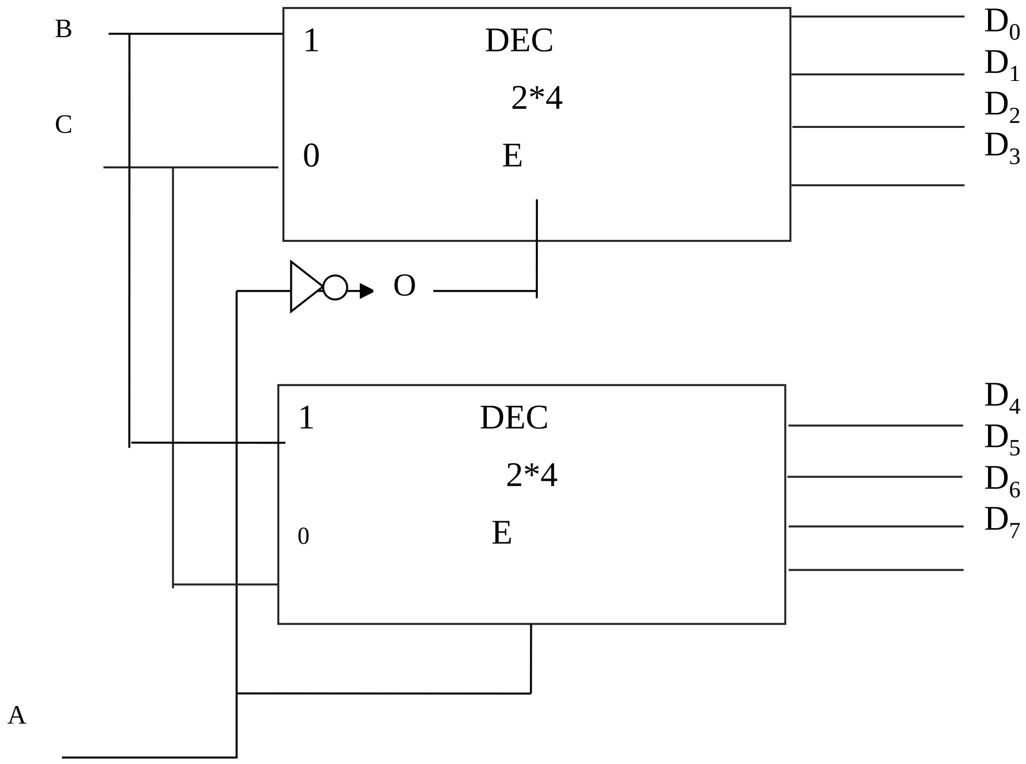
Inputs			Outputs			
E	A	B	D3	D2	D1	D0
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Inputs			Outputs			
E	A	B	D3	D2	D1	D0
0	×	×	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Designing 3*8 Decoder using 2*4 decoder and enable.



Designing 3*8 Decoder using 2*4 decoder and enable.



Multiplexer

A multiplexer has 2^n inputs, 1 outputs and n selections

N = 3

= المدخلات ...8 $\Rightarrow 2^n$

= المخرجات 1

= الاختيارات 3

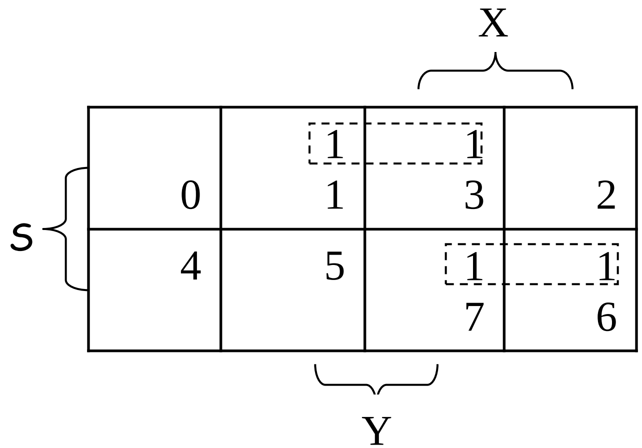
Multiplexer 2*1

2 inputs 1 outputs 1 selection

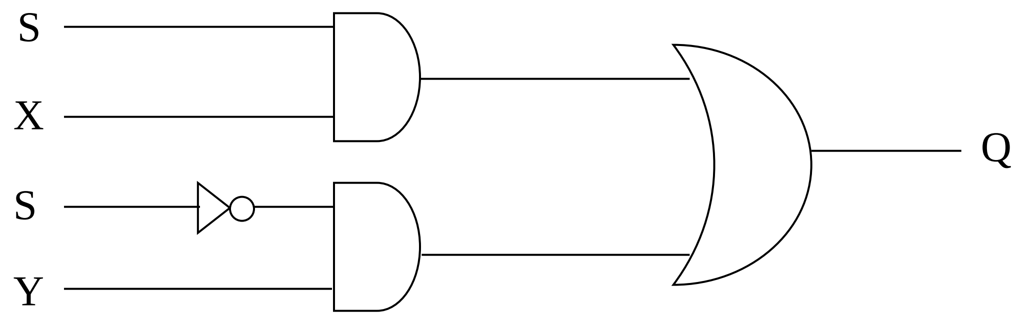
selection	Inputs		Outputs
S	X	Y	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

إذا كانت قيم S = 0 فإن قيم المزج Q هي قيم Y Q = Y

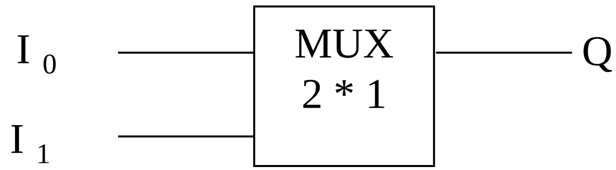
إذا كانت قيم S = 1 فإن قيم المزج Q هي قيم X Q = X



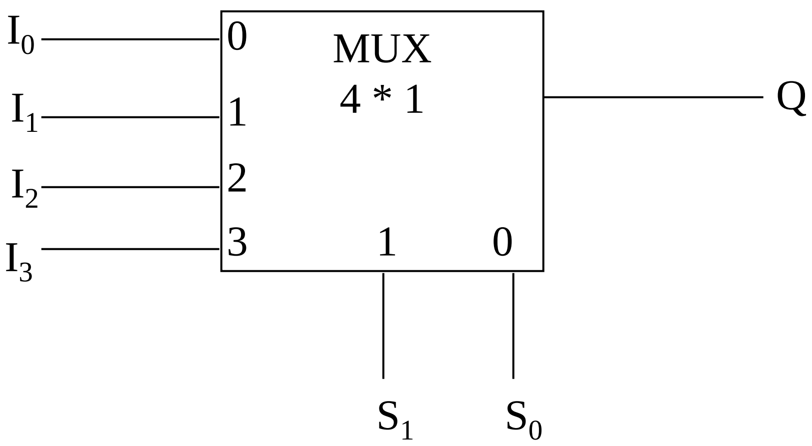
$$Q = Y\,S' + X\,S$$



Block D

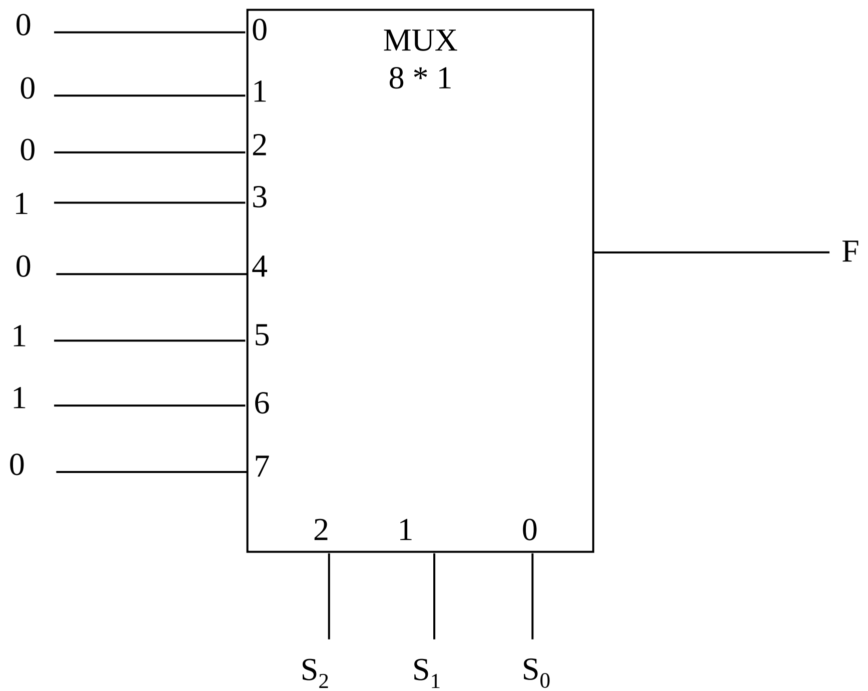


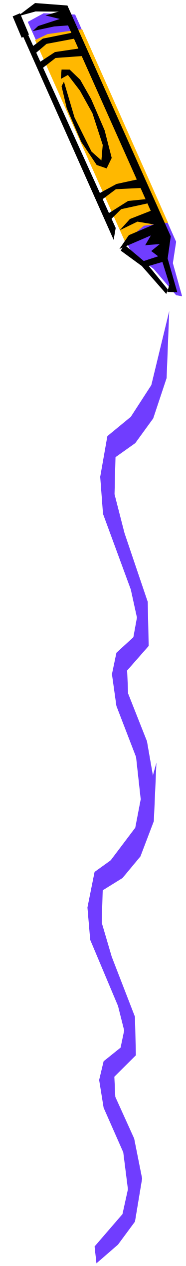
Multiplexer 4 * 1

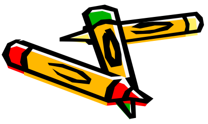


Example :

Implement the following function $F(X,Y,Z)= \sum (3,5,6)$ using an 8 * 1 Multiplexer







Thank you