



# Logical Design

CS 221

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# Sequential Circuits

Logic circuits is classified into two types :

## 1 – Combinational logic circuits

Outputs are entirely dependent on the current input

Basic units is the logic gates

يعتمد الخرج فى أى لحظة على المدخلات الموجودة فى تلك اللحظة  
وحدة البناء الأساسية البوابات المنطقية

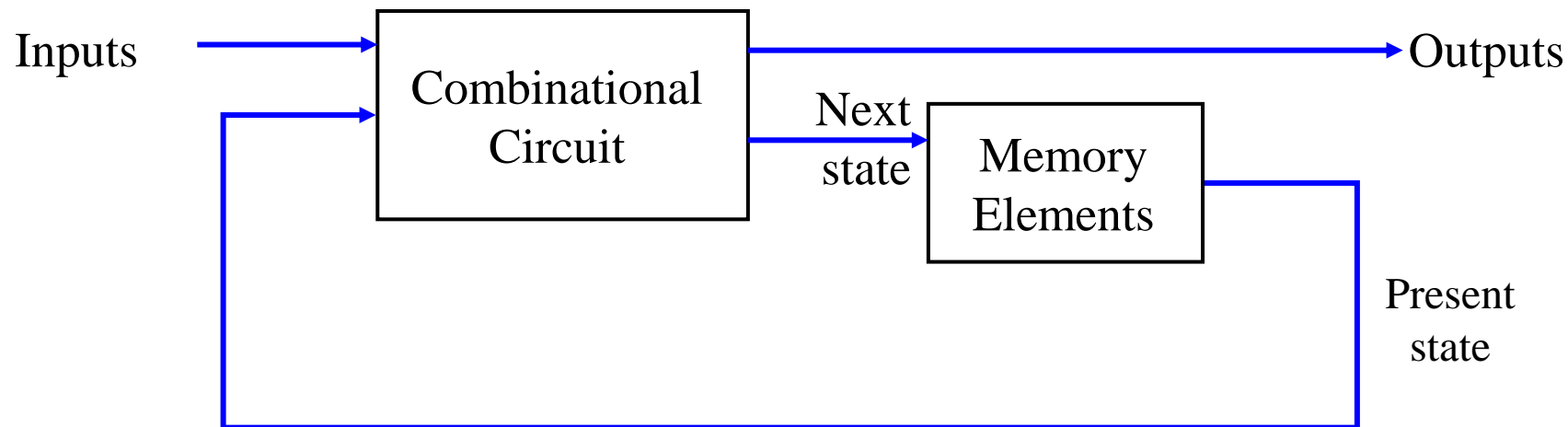


## 2 – Sequential Circuits

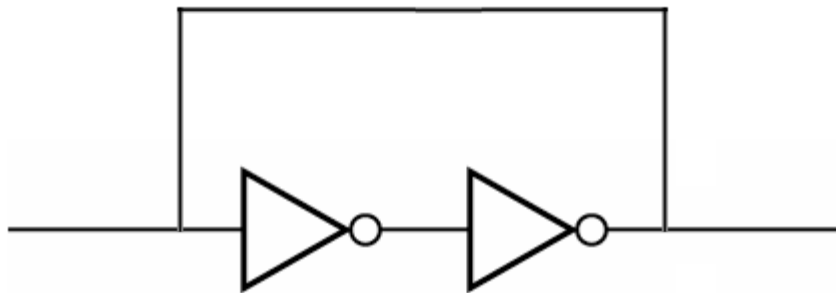
It consists of a combinational circuit to which storage elements are connected to form a feedback path.

The storage elements are devices capable of storing binary information. The basic units is flip flop circuit

يتميز هذا النوع من الدوائر بوجود ذاكرة (memory) ووحدة البناء الأساسية هي دوائر النطاظ.



**Block Diagram of Sequential Circuit**



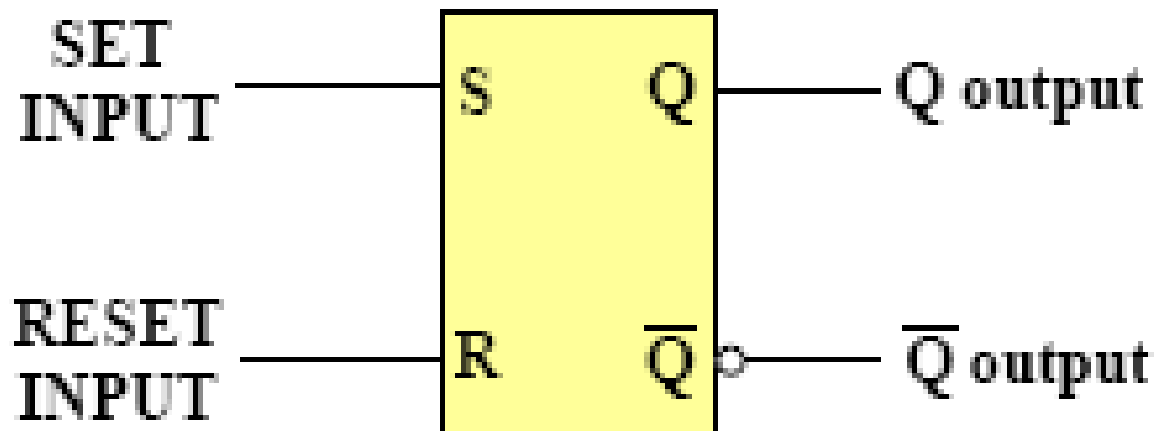
Simple example for memory unit



## Latches ( المساكات )

Memory element differs from the flip flop in the way used to change its stability condition

عنصر من عناصر التخزين ويختلف عن الانطاط في الطريقة المستخدمة للتغيير فقط.

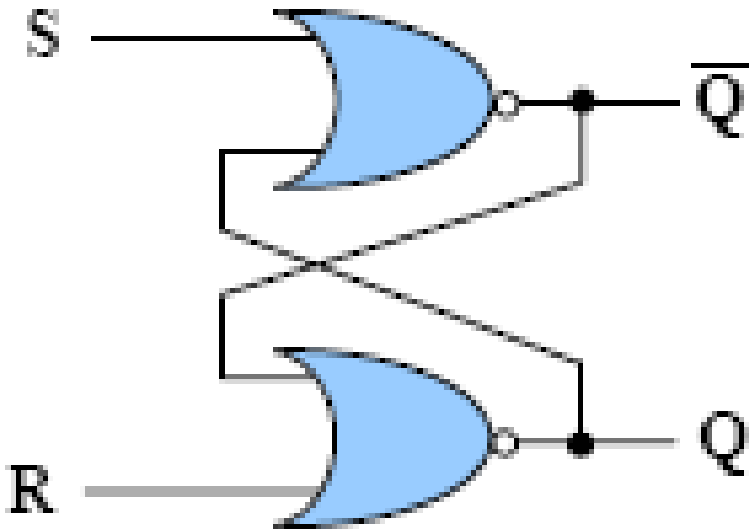


SR Latch Circuit



# SR Latch Circuit

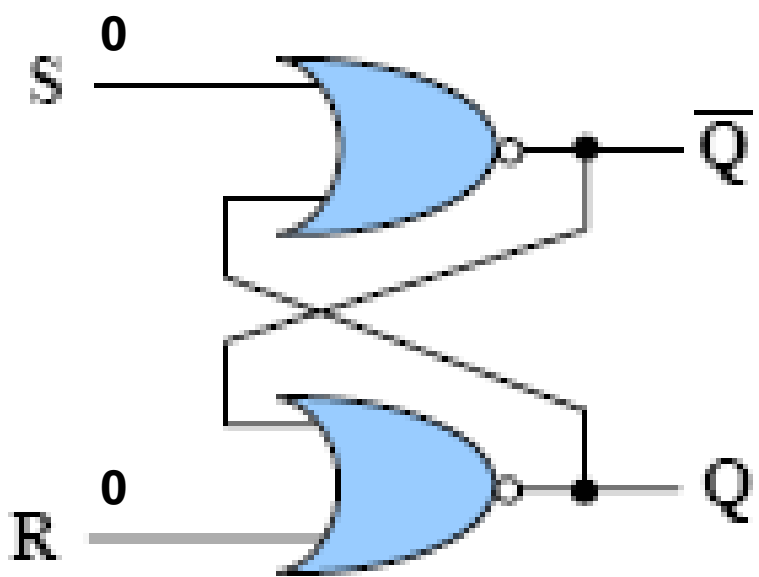
Could be built by NOR gates using feed back (Active High Inputs)





المدخلات		الخروج	وضع التشغيل (Mode of Operation)
S	R	Q	
•	•	Q.	وضع الإمساك (عدم التغيير) No Change
•	١	•	الوضع الغير فعال Latch RESETS
١	•	١	الوضع الفعال Latch SETS
١	١	?	وضع الخطر أو وضع غير مسموح به Invalid condition

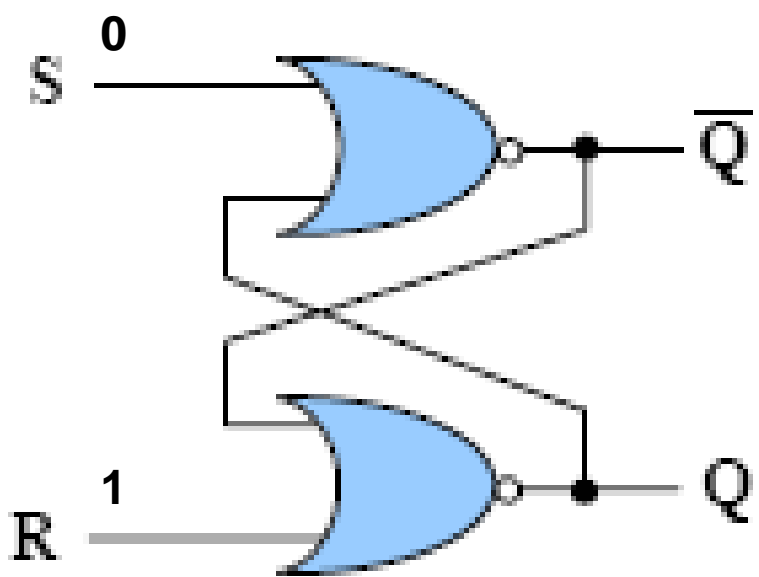




Start				Start			
0	0	0	0	1	1	1	
1	1	1	1	0	0	0	

When  $S = 0$  &  $R = 0$

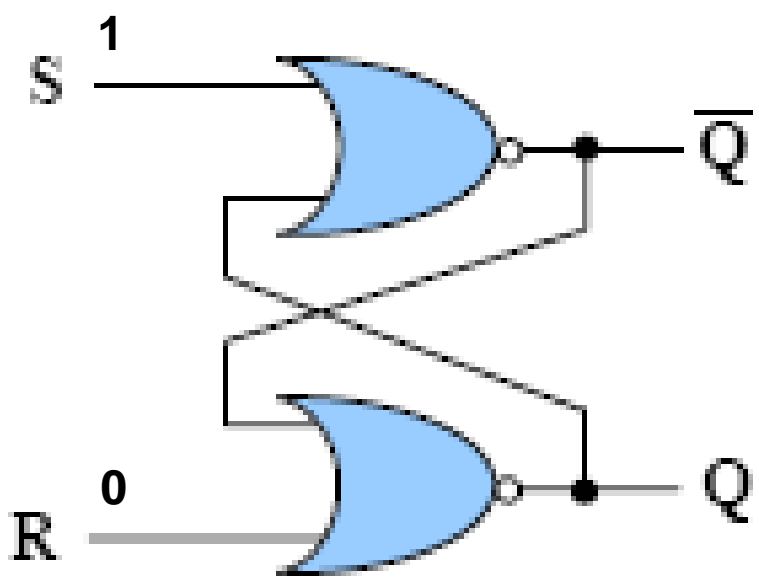
Condition = No change



Start				Start			
0	1	1		1	1	1	
1	0	0		0	0	0	

When  $S = 0$  &  $R = 1$

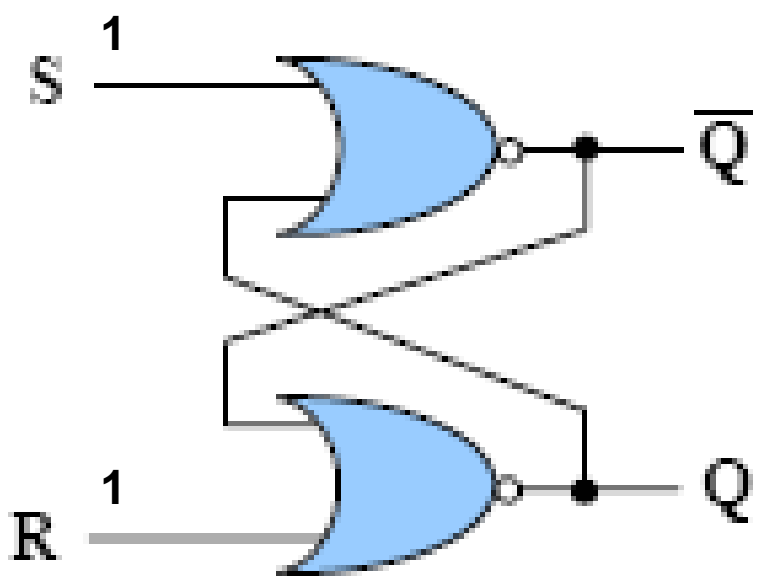
Condition = Reset (  $Q = 0$  &  $Q' = 1$  )



Start				Start			
0	0	0		1	1	0	
1	1	1		0	1	1	

When  $S = 1$  &  $R = 0$

Condition = Set (  $Q = 1$  &  $Q' = 0$  )



Start				Start			
0	0	0		1	0	0	
1	0	0		0	0	0	

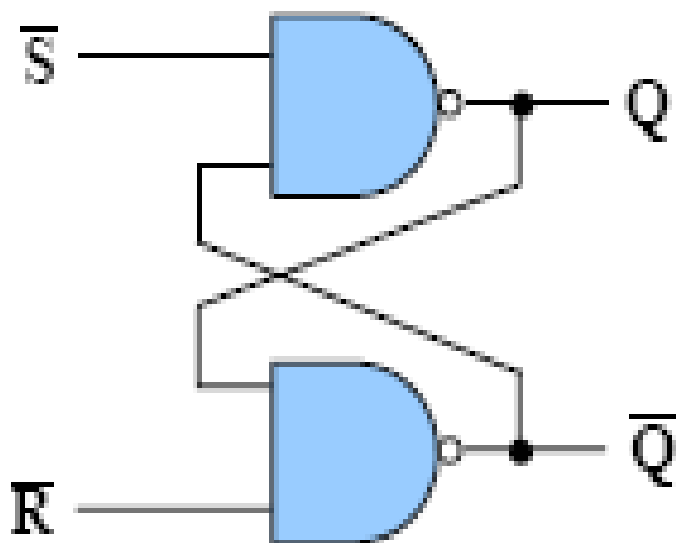
When  $S = 1$  &  $R = 1$

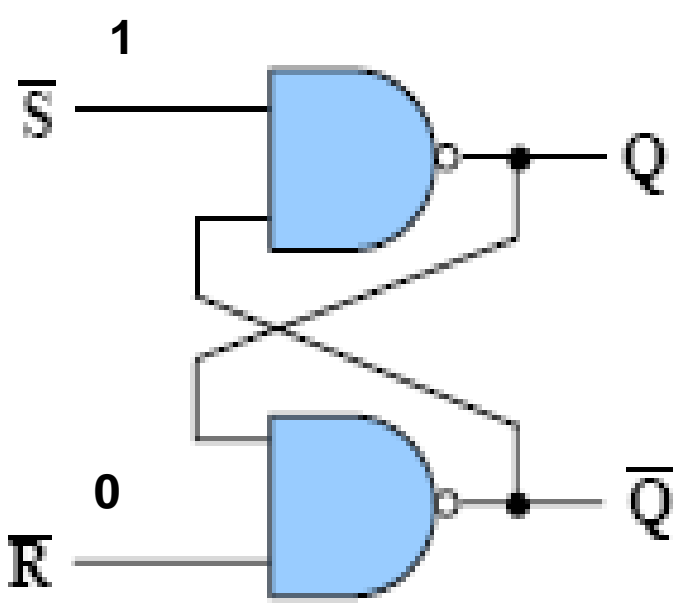
Condition = invalid condition



## Using Nand Gate for SR Latch ( Active low inputs)

لاحظ أن المستوى الفعال لدائرة ال ( NAND ) هو الصفر وبالتالي  
الخطر يكون عند  $S = 0$  &  $R = 0$

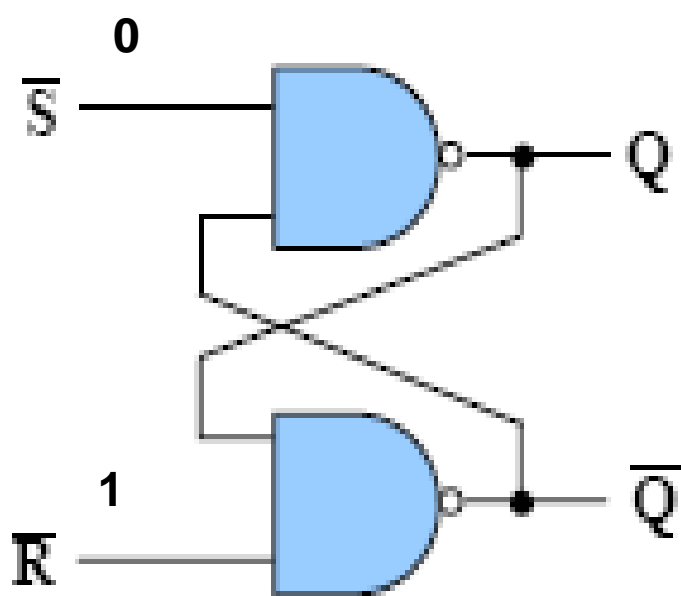




Start				Start			
0	0	0		1	0	0	
1	1	1		0	1	1	

When  $S = 1$  &  $R = 0$

Condition = Reset (  $Q = 0$  &  $Q' = 1$  )



Start				Start			
0	1	1		1	1	1	
1	0	0		0	0	0	

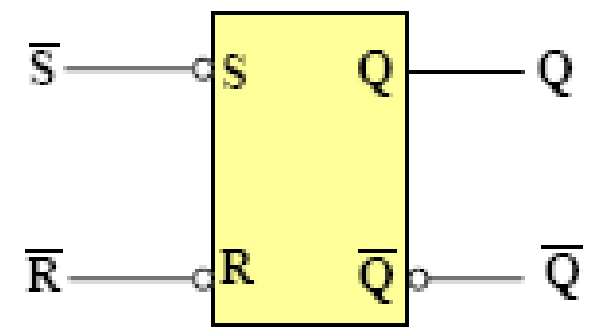
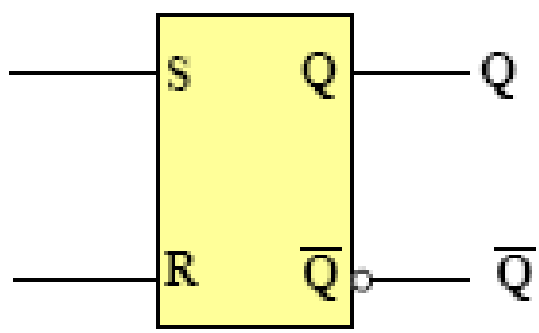
When  $S = 1$  &  $R = 0$

Condition = Reset (  $Q = 0$  &  $Q' = 1$  )



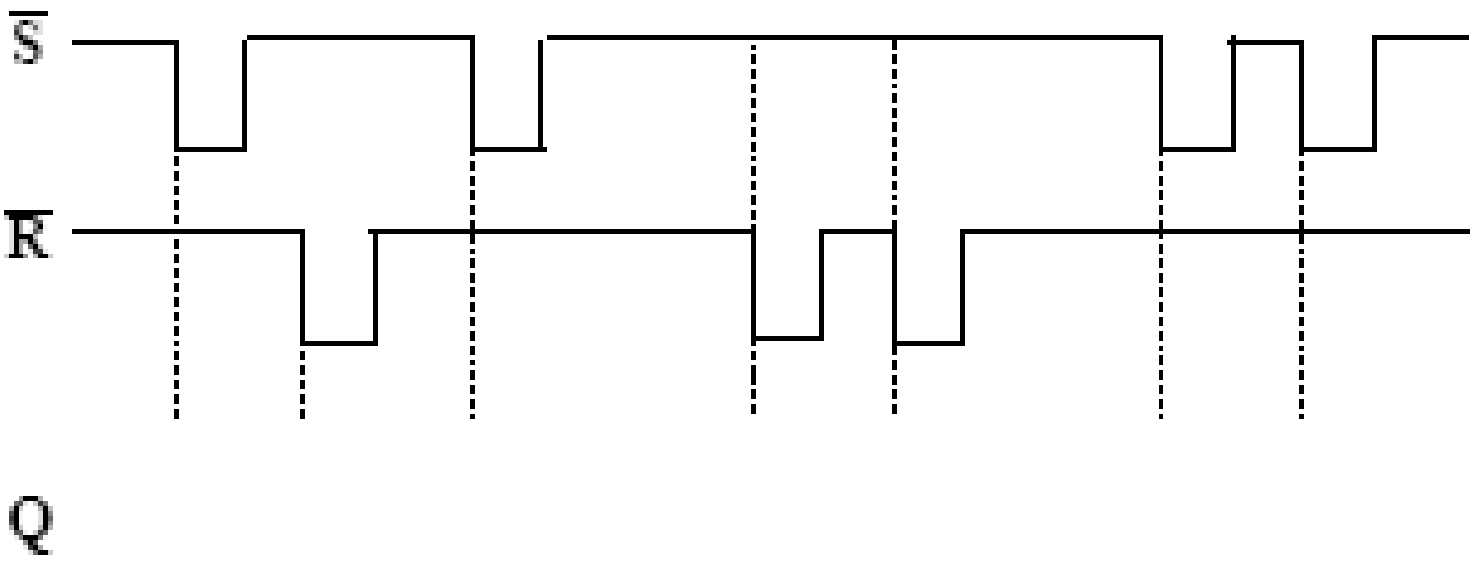
المدخلات		الخروج	وضع التشغيل (Mode of Operation)
$\bar{S}$	$\bar{R}$	Q	
0	0	?	وضع الخطر أو وضع غير مسموح به Invalid condition
0	1	1	الوضع الفعال Latch SETS
1	0	0	الوضع غير الفعال Latch RESETS
1	1	Q.	وضع الإمساك (عدم التغيير) No Change

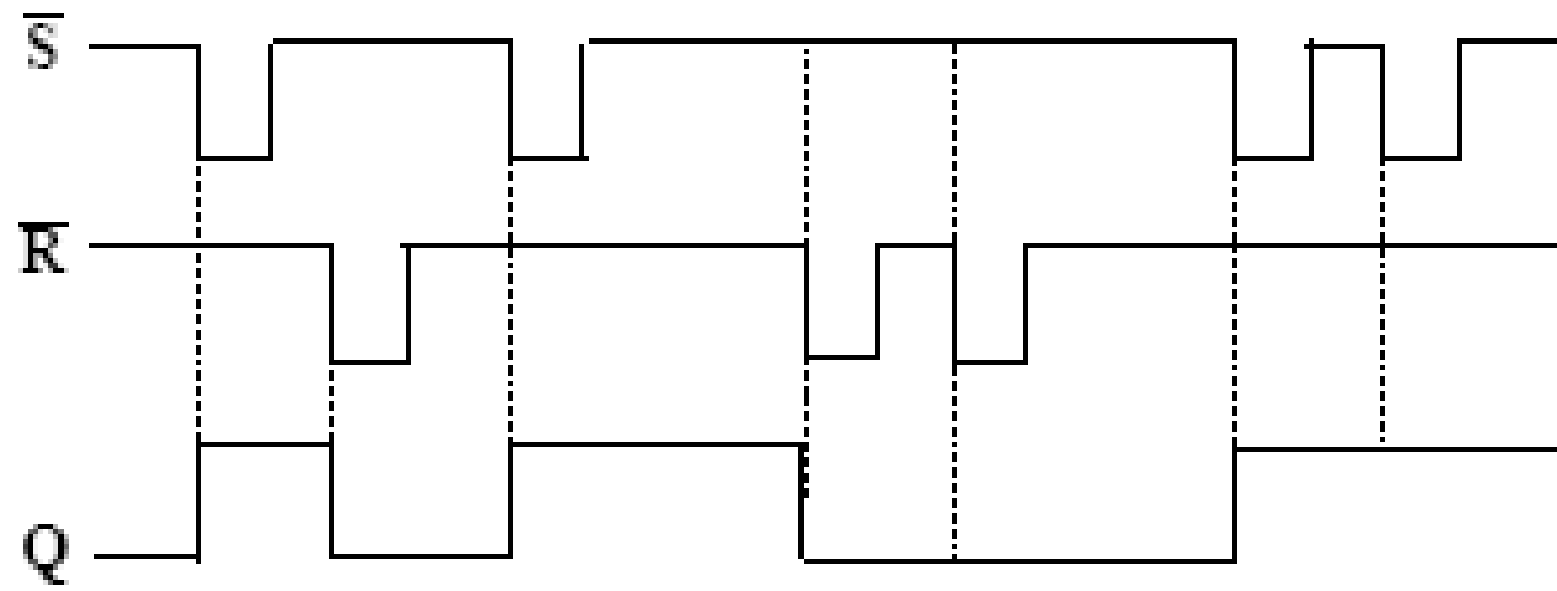


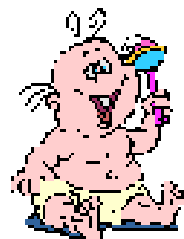




The following is a timing diagram for SR ( Active low inputs )  
Draw the timing diagram for Q ( Initial Q = 0 ) ... Note the  
timing clock.







H A K



T

N

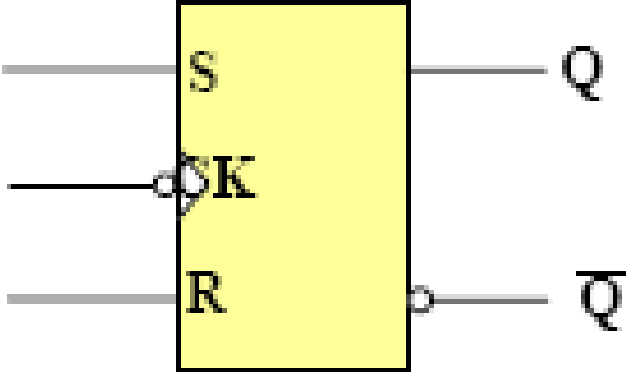
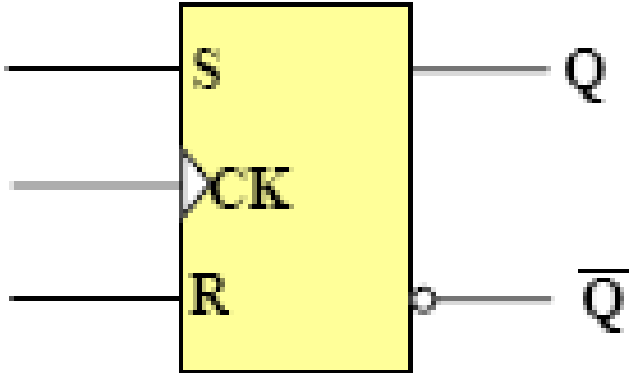
S





# S-R Flip Flop

Block diagram for clocked S-R Flip Flop





1. The Ministry of Education and Higher Education of the Republic of Turkey, in order to ensure the quality of education and to provide a fair and equitable education for all students, has decided to implement a new curriculum for the primary and secondary schools.

2. The new curriculum will be based on the principles of the National Education Law and the National Curriculum Framework. It will aim to develop the students' knowledge, skills, and values, and to prepare them for the challenges of the 21st century.

3. The new curriculum will be implemented in the following areas:

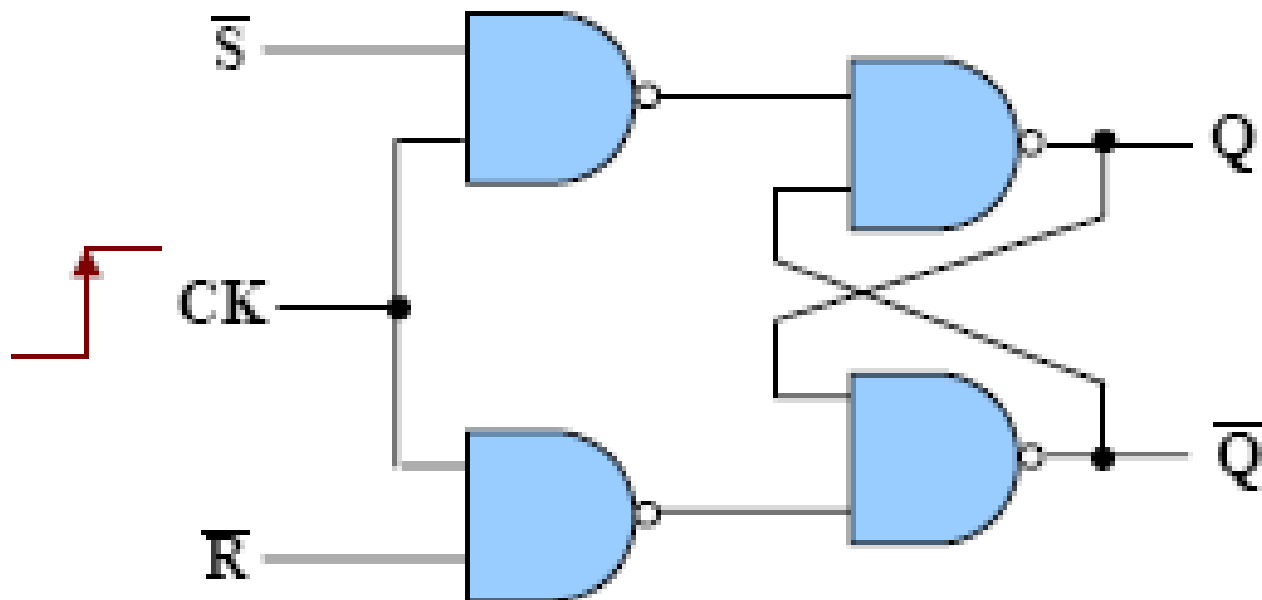
- a. Language and Literature
- b. Mathematics
- c. Science and Technology
- d. Social Studies
- e. Art and Music
- f. Physical Education and Sports

4. The Ministry of Education and Higher Education will provide the necessary resources and support to the schools and teachers to implement the new curriculum successfully.

5. The Ministry of Education and Higher Education will monitor the implementation of the new curriculum and will make necessary adjustments to ensure its effectiveness.



We add another ( Two Nand gates )



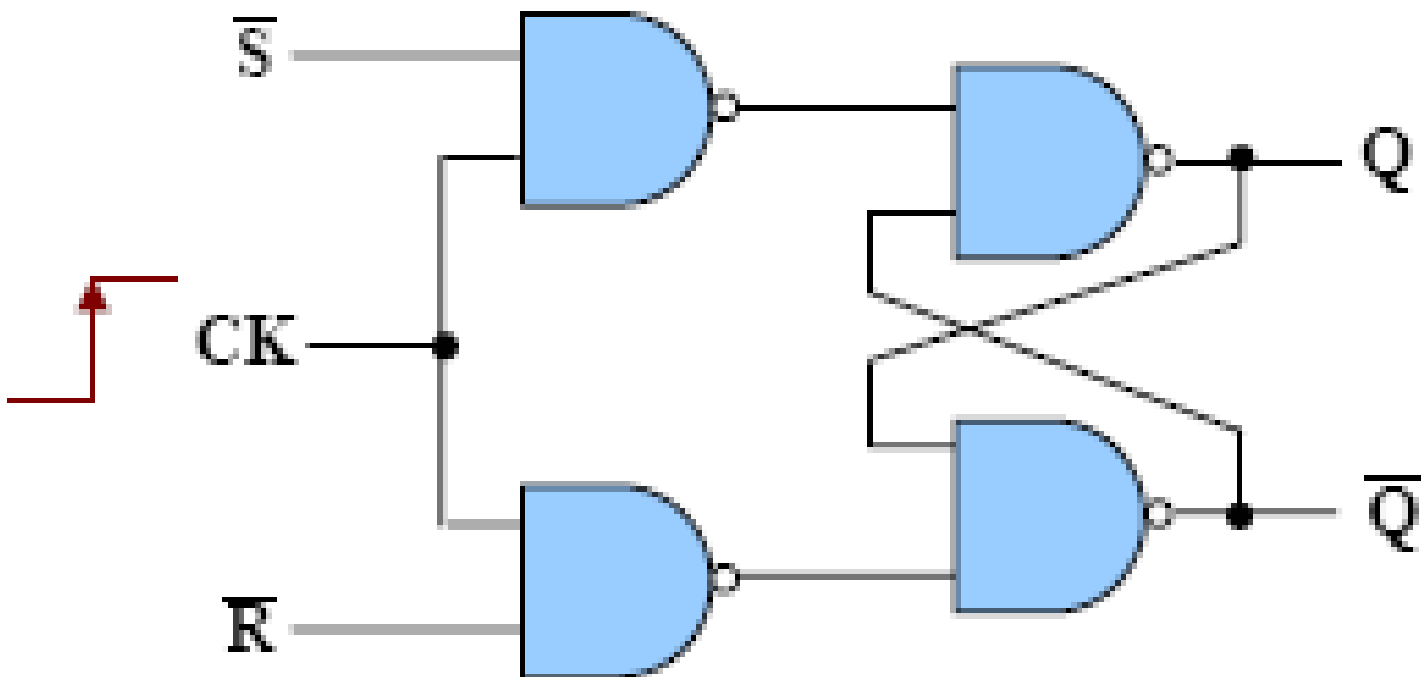
Logic diagram for SR Latch ( Flip flop ) with control input

( لو فاكتر ( Active low inputs ) مع ال Nand وهو عكس ال Or وبالتالي ال 0 & 0 المشكلة .....  
هنا مع وجود ال CK و ال Nand الأولى نرجع لل Active high وبالتالي تكون 1 & 1 هي المشكلة.



المدخلات			الخروج	وضع التشغيل (Mode of Operation)
S	R	CK	Q	
0	0	X	Q.	وضع الإمساك (عدم التغير) No Change
0	1	↑	0	الوضع غير الفعال Latch RESETS
1	0	↑	1	الوضع الفعال Latch SETS
1	1	↑	?	وضع الخطر أو وضع غير مسموح به Invalid condition



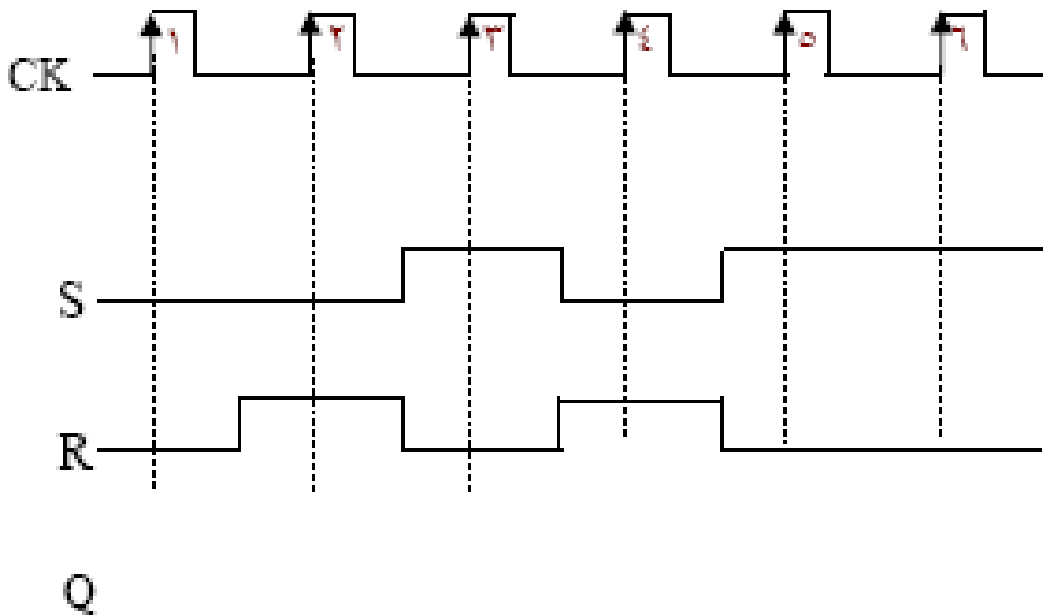


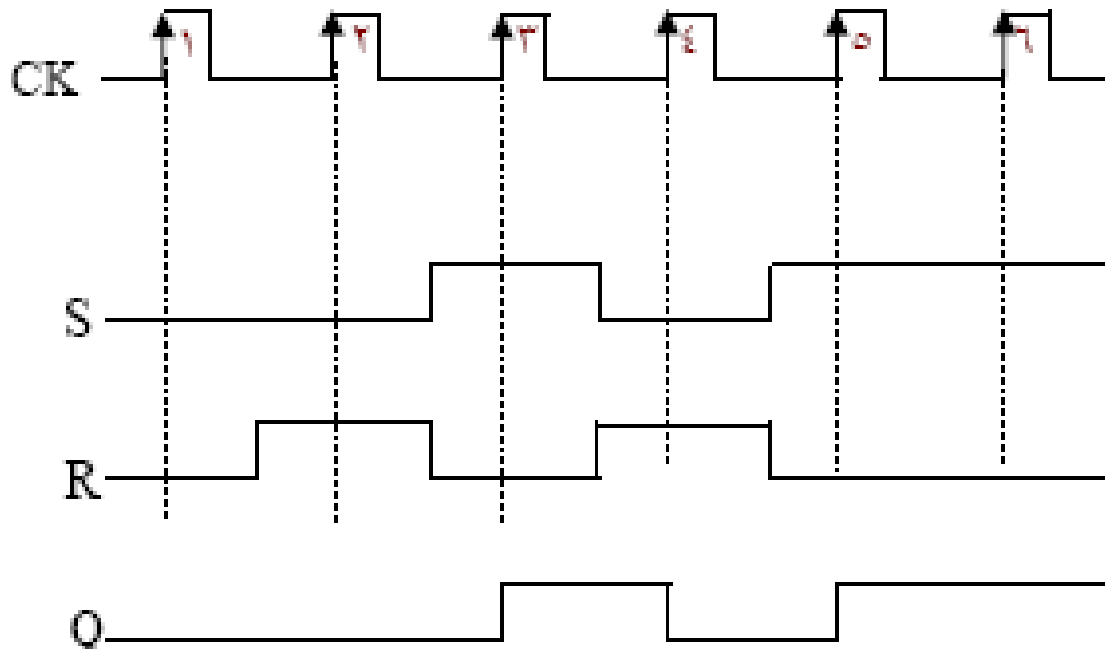


The following is timing diagram for S R flip flop with control input ( S , R , K ) ....

Draw the timing diagram for Q ( initial Q = 0 ) ...

Note the timing clock.



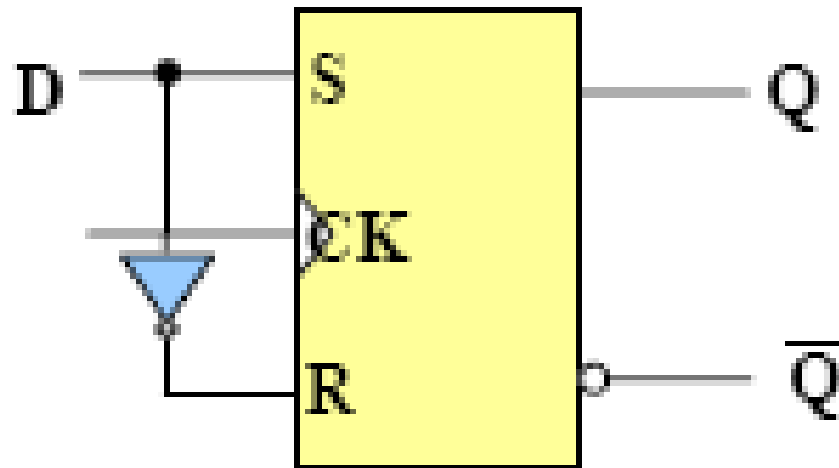


- 1 – First pulse  $S = 0$  &  $R = 0$  Then  $Q = 0$
- 2 – Second pulse  $S = 0$  &  $R = 1$  Then  $Q$  still 0
- 3 – Third pulse  $S = 1$  &  $R = 0$  then  $Q \rightarrow 1$
- 4 – Fourth pulse  $S = 0$  &  $R = 1$  then  $Q \rightarrow 0$
- 5 – fifth pulse  $S = 1$  &  $R = 0$  then  $Q \rightarrow 1$
- 6 – Sixth pulse  $S = 1$  &  $R = 0$  then  $Q$  still 1

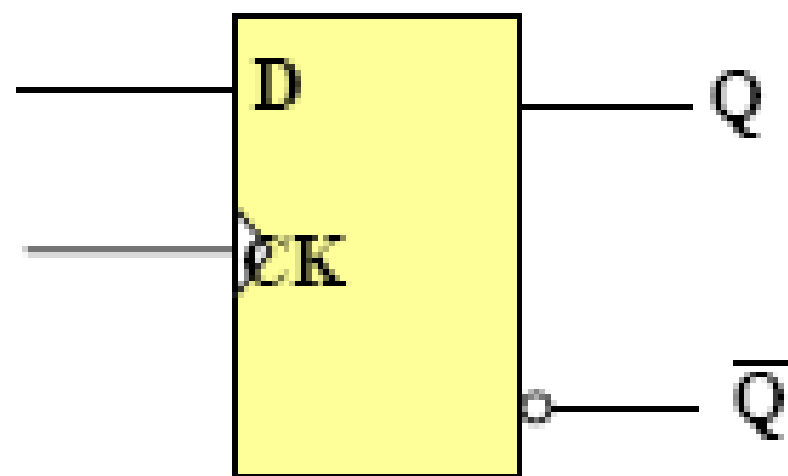


# D type flip flop

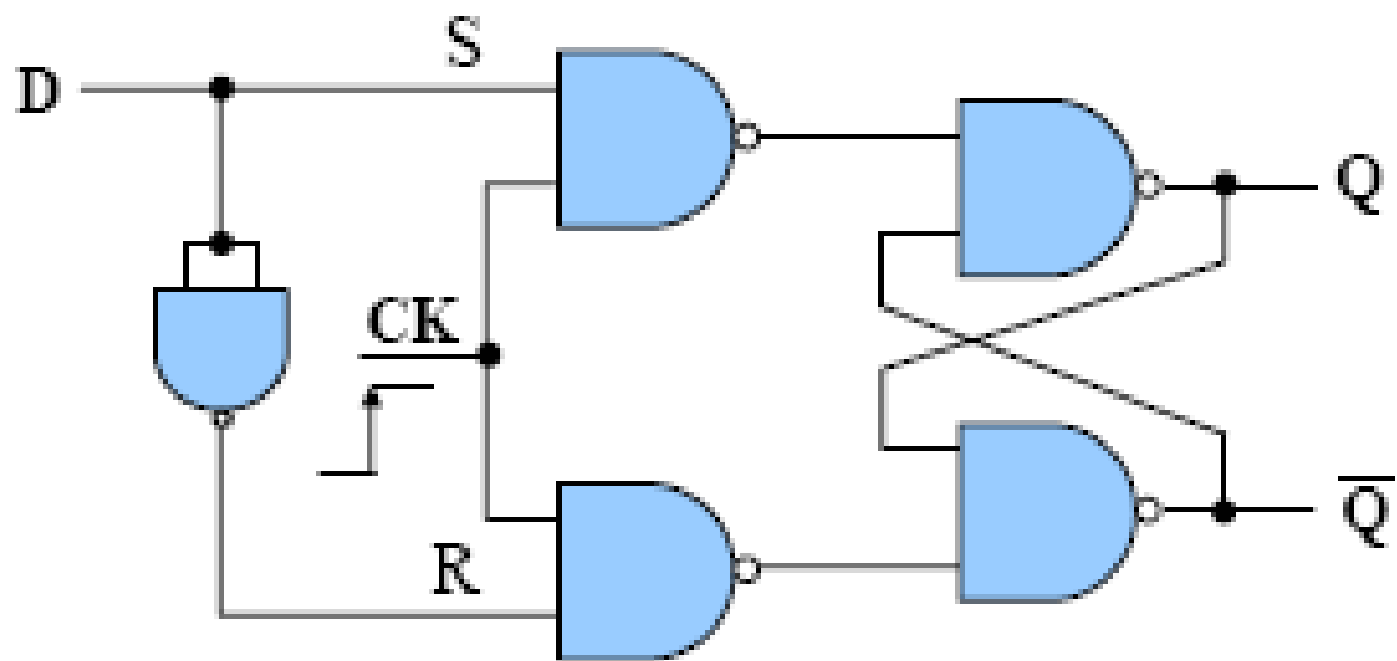
Memory unit for single bit ....Zero or One



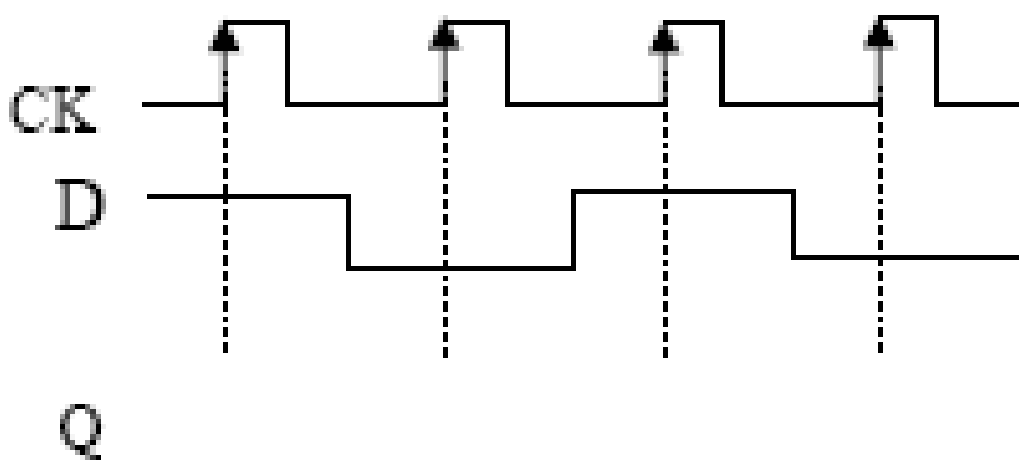




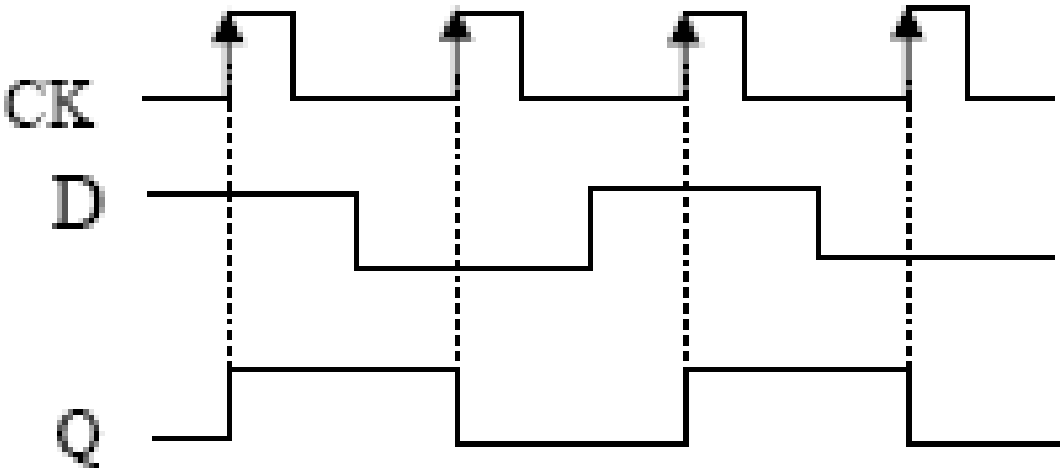
Block diagram for D flip Flop



Logic diagram for D flip Flop







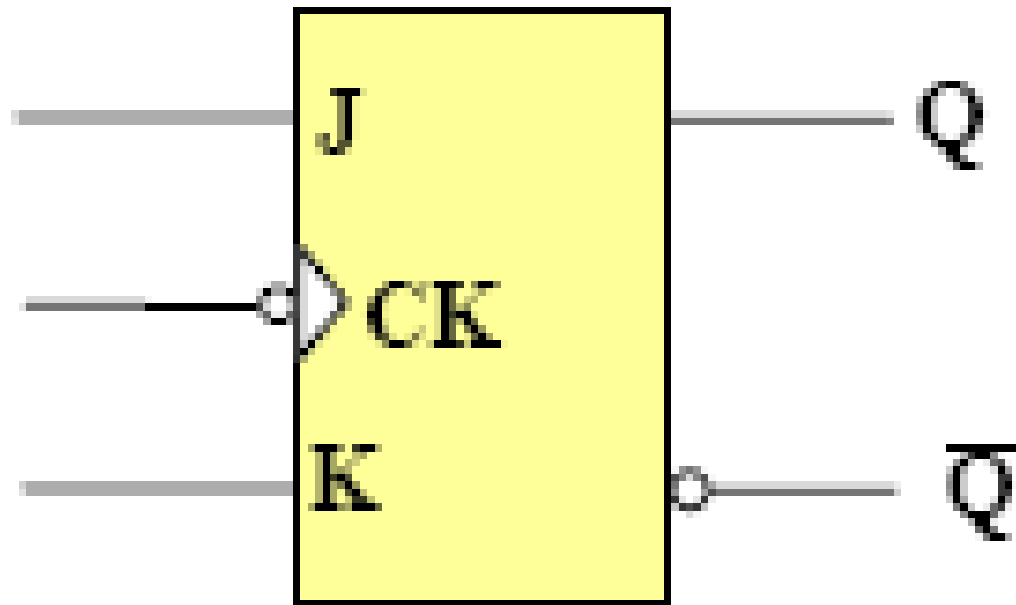


# J-K Flip flop

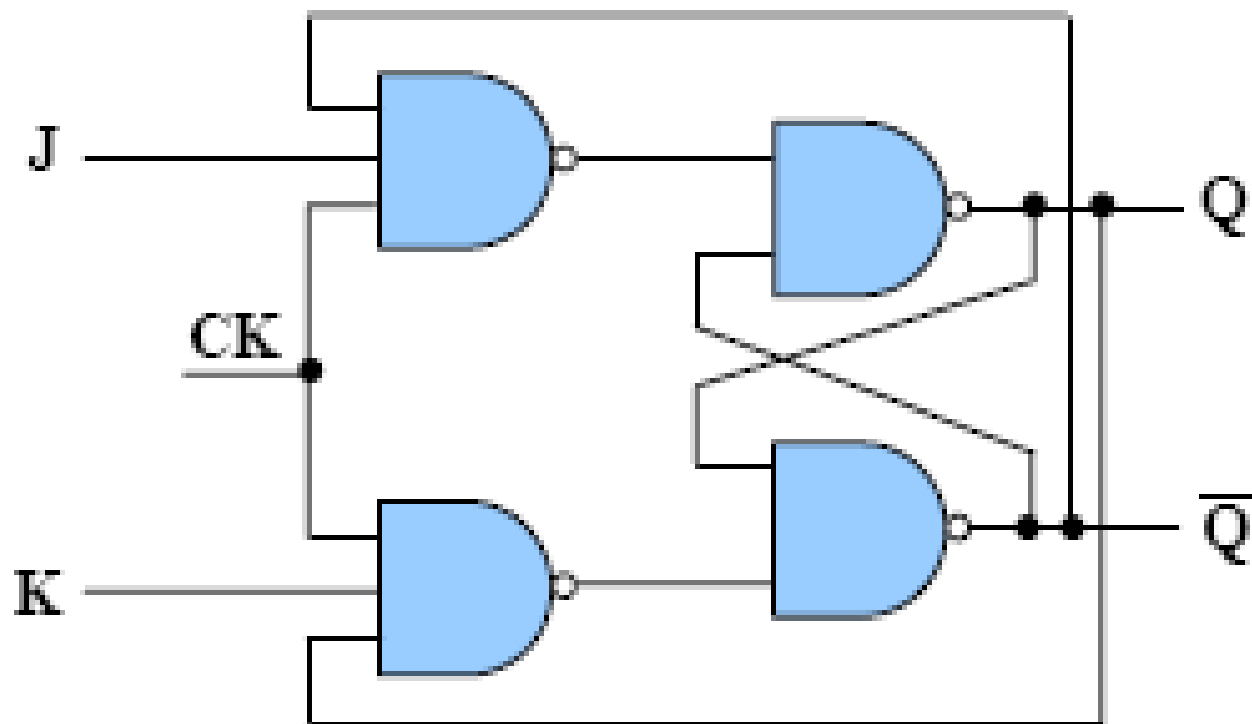
J & K are just letters

J-K flip flop is the same like SR except Q & Q' are used as inputs again ...

then there is no invalid condition.... when J & K = 1 it called toggle condition where Q becomes Q' and vice versa



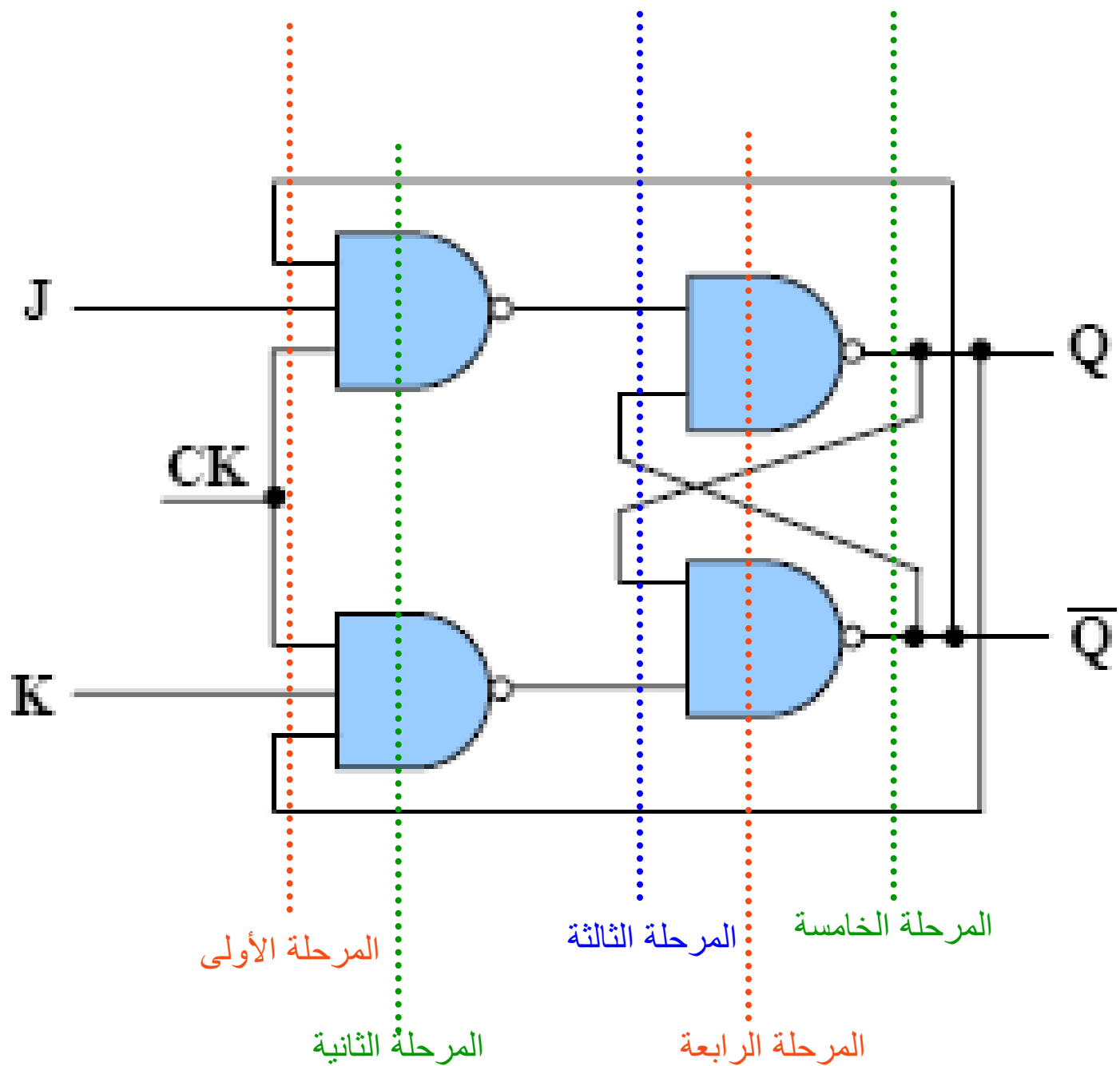
Block Diagram for J – K Flip Flop



Logic diagram for J – K Flip Flop

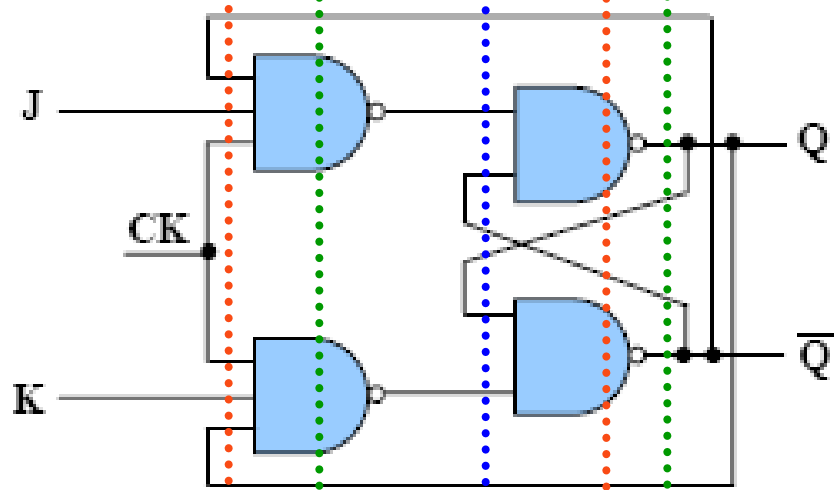


المدخلات			الخروج	وضع التشغيل (Mode of Operation)
J	K	CK	Q	
0	0	↓	$Q_0$	وضع الإمساك (عدم التغير) No Change
0	1	↓	0	الوضع غير الفعال (RESET)
1	0	↓	1	الوضع الفعال (SET)
1	1	↓	$\overline{Q}_0$	وضع التبدل Toggle





1



0

المرحلة الأولى  
المرحلة الثانية  
المرحلة الثالثة  
المرحلة الرابعة  
المرحلة الخامسة

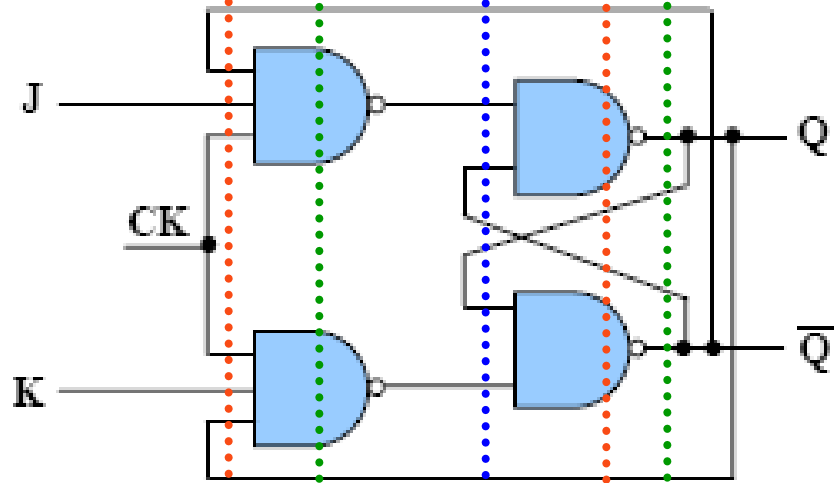
Start				Start			
0	1	1		1	1	1	
1	0	0		0	0	0	

When  $J = 1$  &  $K = 0$

Condition = Set (  $Q = 1$  &  $Q' = 0$  )



0



1

المرحلة الأولى  
المرحلة الثانية  
المرحلة الثالثة  
المرحلة الرابعة  
المرحلة الخامسة

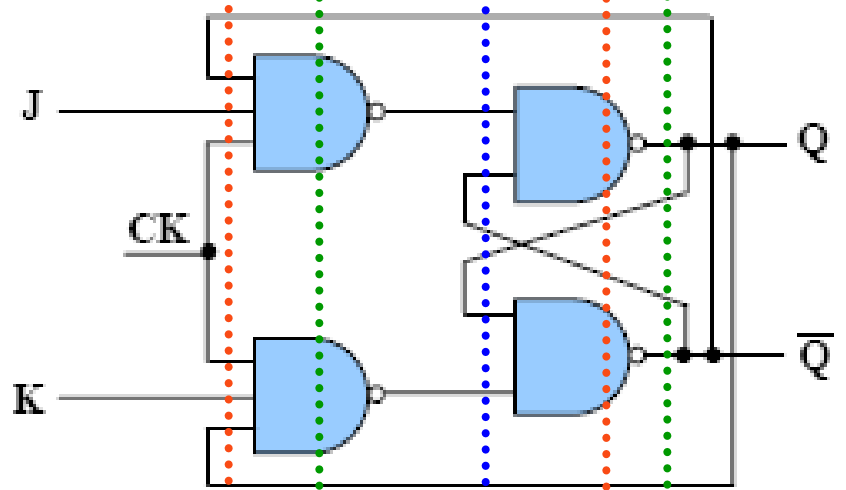
Start				Start			
0	0	0		1	0	0	
1	1	1		0	1	1	

When  $J = 0$  &  $K = 1$

Condition = Reset (  $Q = 0$  &  $Q' = 1$  )



0



0

المرحلة الأولى  
المرحلة الثانية  
المرحلة الثالثة  
المرحلة الرابعة  
المرحلة الخامسة

Start				Start			
0	0	0		1	1	1	
1	1	1		0	0	0	

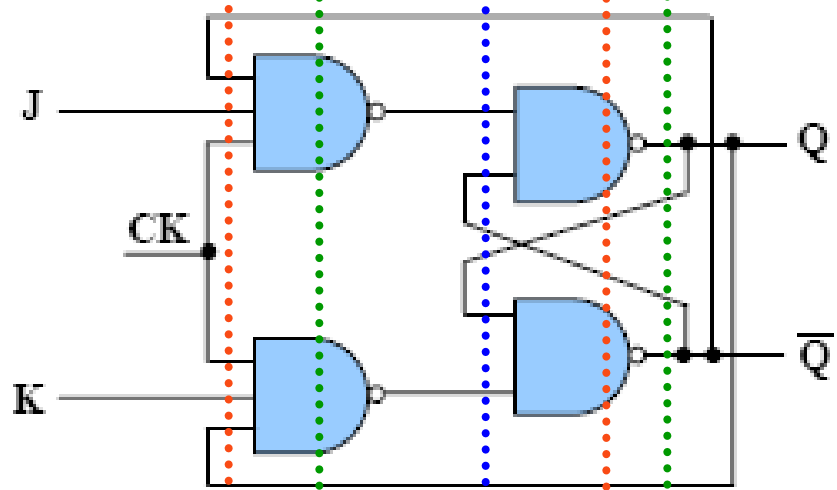
When  $J = 0$  &  $K = 0$

Condition = No change





1



1

المرحلة الأولى  
المرحلة الثانية  
المرحلة الثالثة  
المرحلة الرابعة  
المرحلة الخامسة

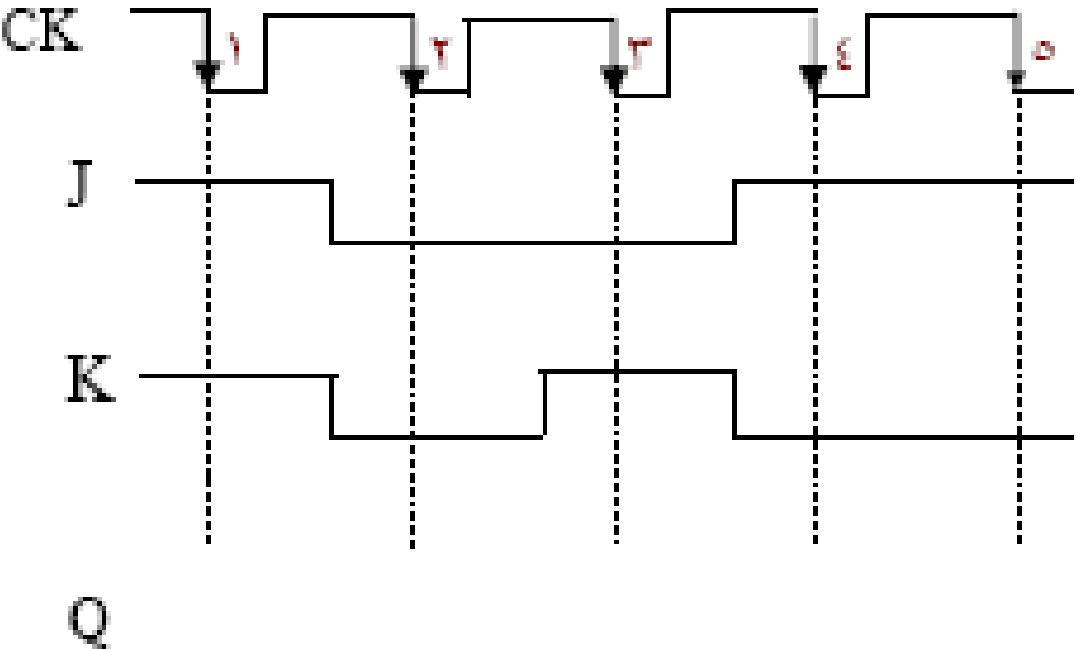
Start				Start			
0	1	1		1	0	0	
1	0	0		0	1	1	

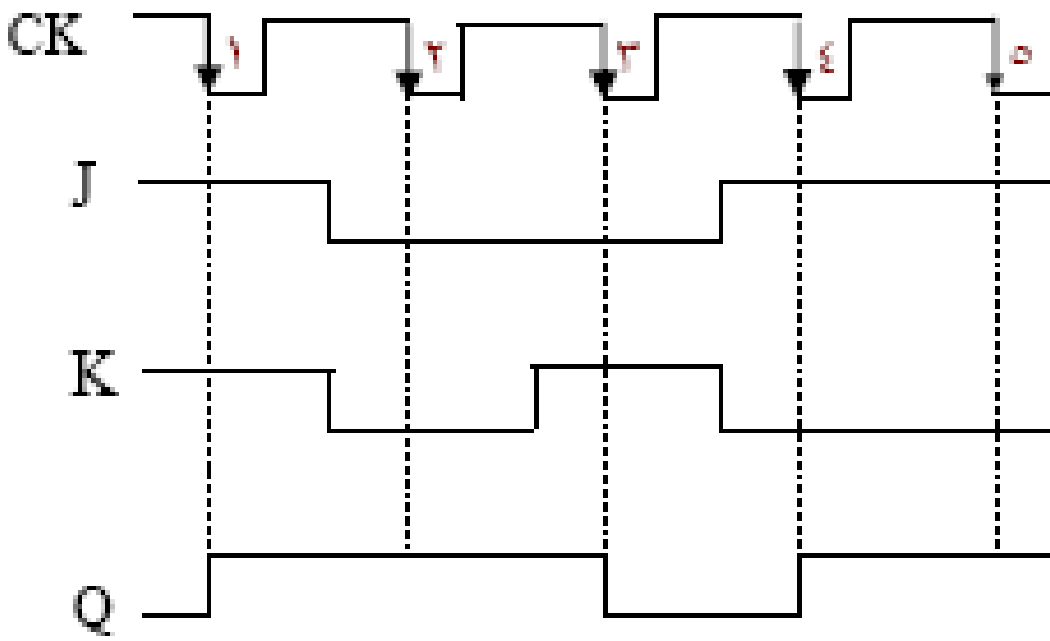
When  $J = 1$  &  $K = 1$

Condition = Toggle



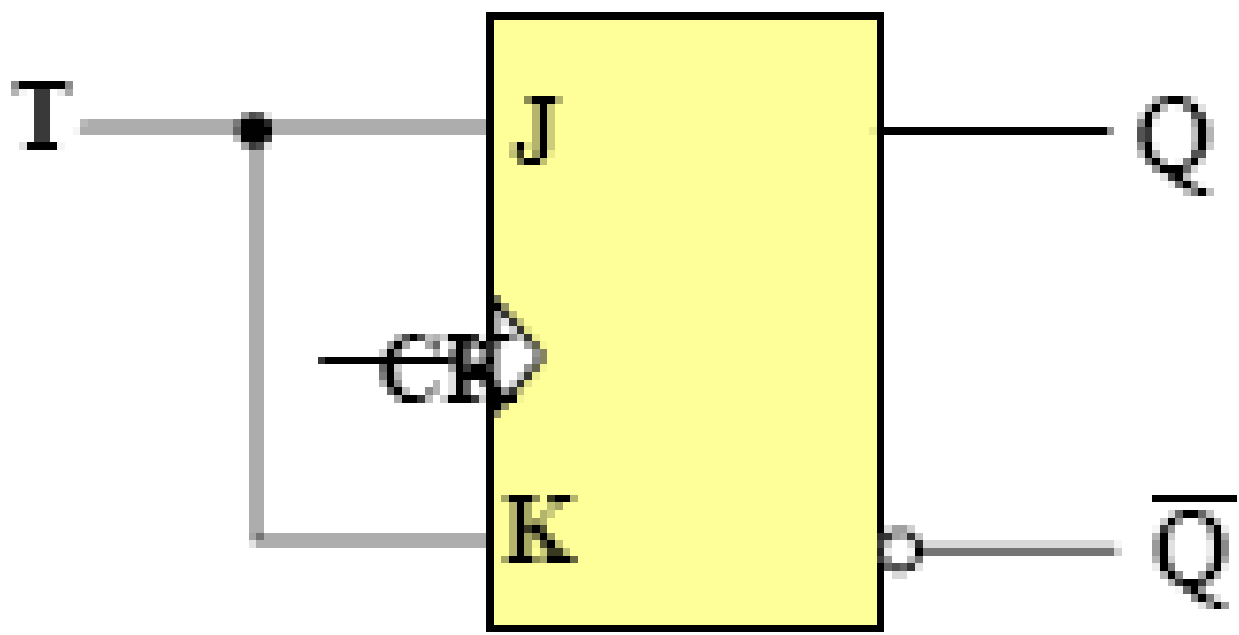
The following is timing diagram for J K flip flop .....Draw the pulse shape for the output Q ( initial Q = 0 ) clock pulse from ( 1 ) to ( 0 ) ↓







# T – Type flip flop

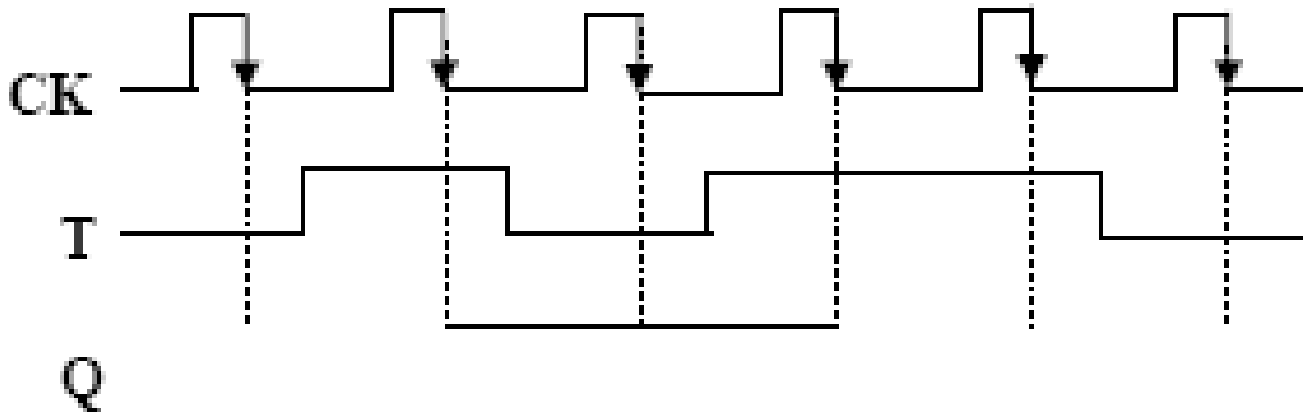


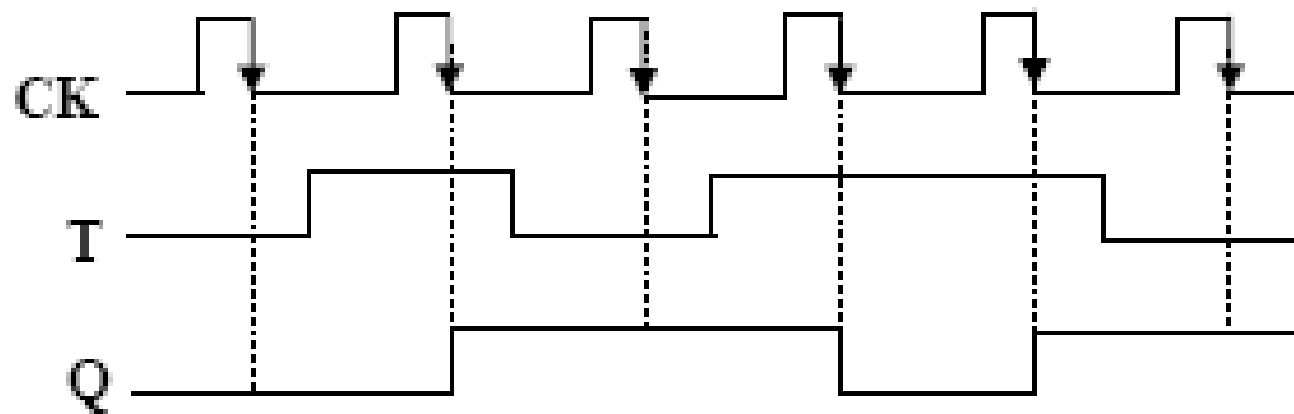
From J-K flip flop connect J with K

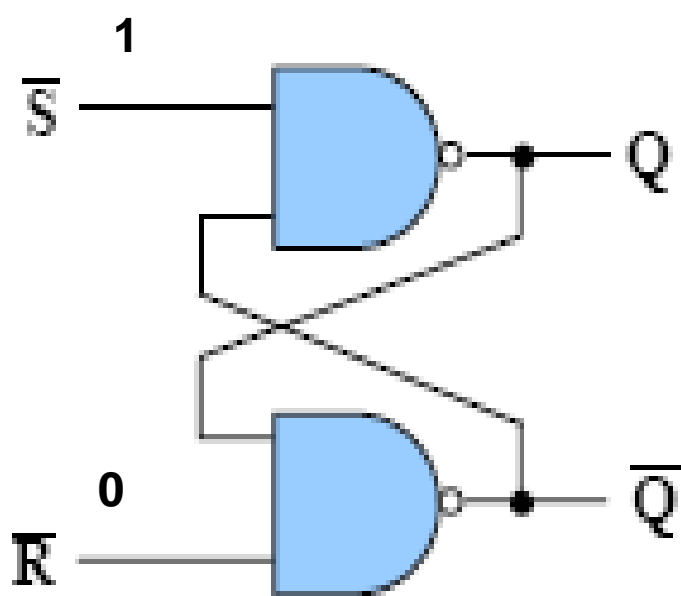


المدخلات		الخروج	وضع التشغيل (Mode of Operation)
T	CK	Q	
0	↓	$Q_0$	وضع الإمساك (عدم التغيير) No Change
1	↓	$\overline{Q}_0$	وضع التبديل Toggle

1 2 3 4 5 6 7 8 9 10 11 12







Start				Start			
0	0	0		1	0	0	
1	1	1		0	1	1	

When  $S = 1$  &  $R = 0$

Condition = Reset (  $Q = 0$  &  $Q' = 1$  )