Logical Design

CS 221

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Sequential Circuits

Logic circuits is classified into two types :

1 – Combinational logic circuits

Outputs are entirely dependent on the current input

Basic units is the logic gates

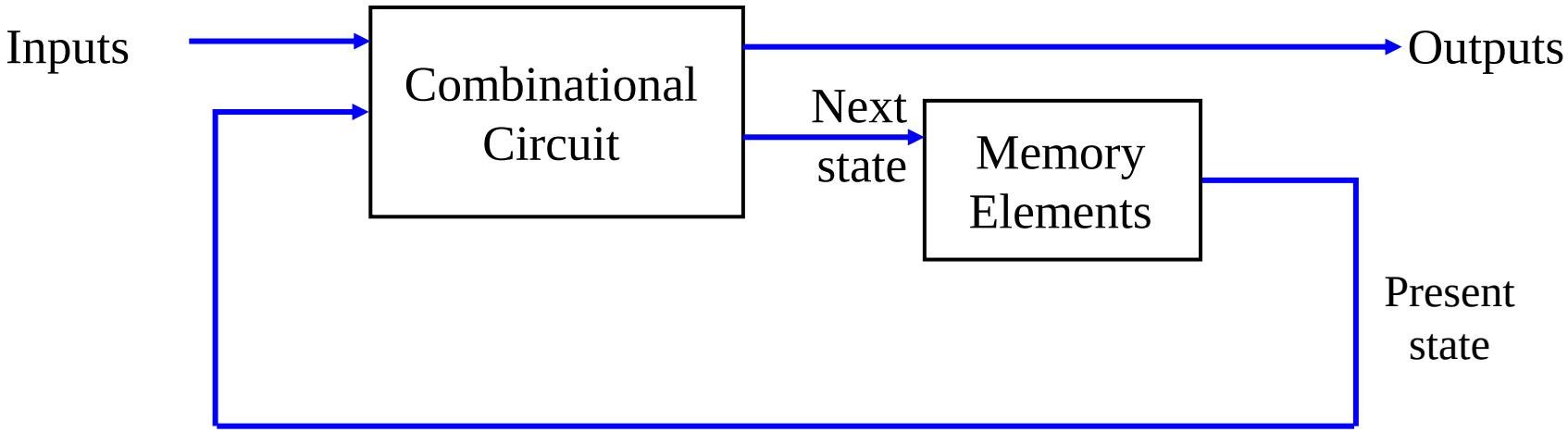
يعتمد الخرج فى أى لحظة على المدخلات الموجودة فى تلك اللحظة
وحدة البناء الأساسية البوابات المنطقية

2 – Sequential Circuits

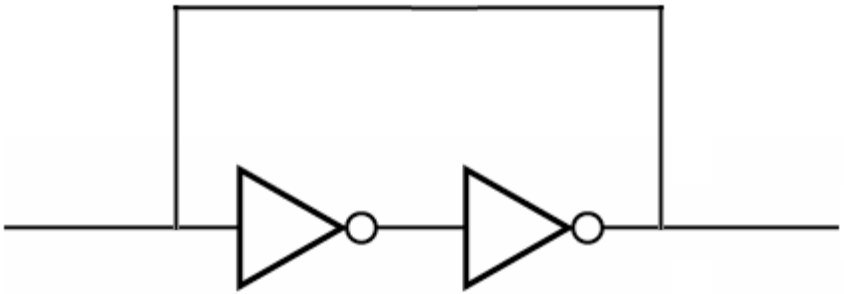
It consists of a combinational circuit to which storage elements are connected to form a feedback path.

The storage elements are devices capable of storing binary information. The basic units is flip flop circuit

يتميز هذا النوع من الدوائر بوجود ذاكرة (memory)
ووحدة البناء الأساسية هى دوائر النطاط.



Block Diagram of Sequential Circuit

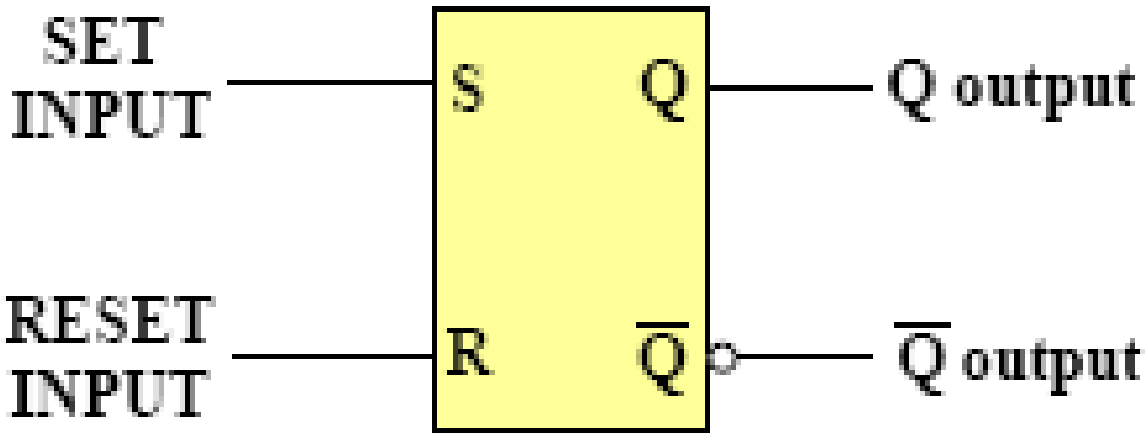


Simple example for memory unit

Latches (المساكات)

Memory element differs from the flip flop in the way used to change its stability condition

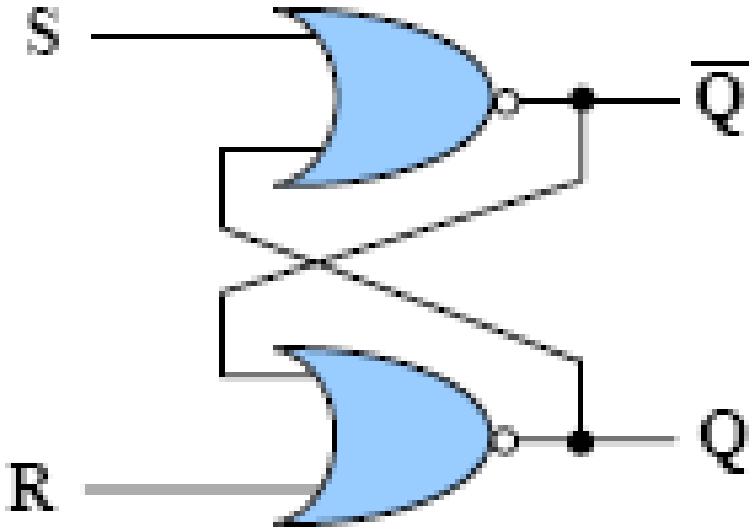
عنصر من عناصر التخزين ويختلف عن ا لنطاط فى الطريقة المستخدمة للتغيير فقط.



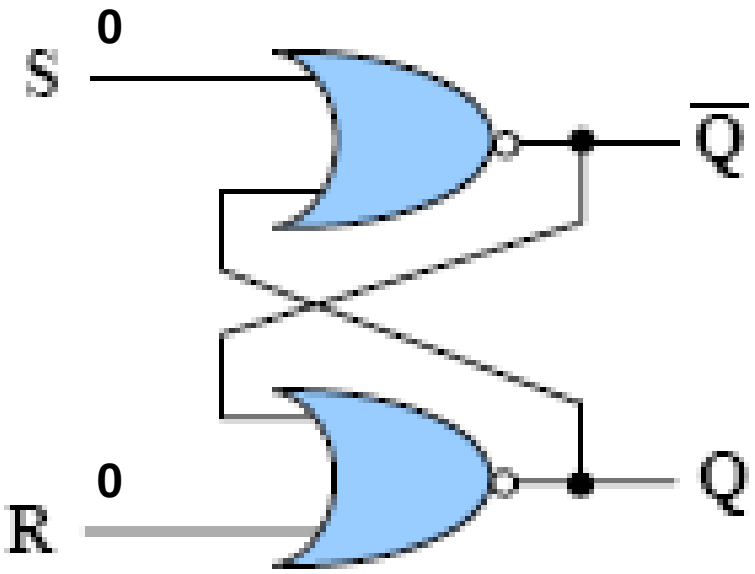
SR Latch Circuit

SR Latch Circuit

Could be built by NOR gates using feed back (Active High Inputs)

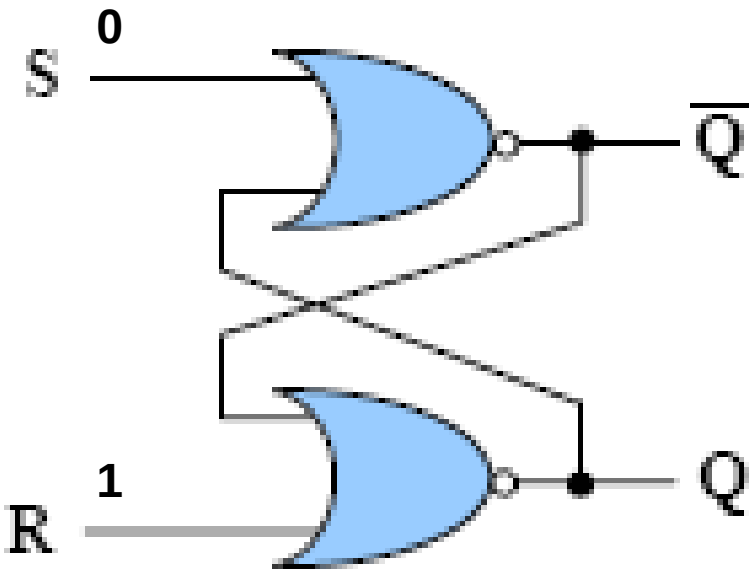


المدخلات		الخرج	وضع التشغيل
S	R	Q	(Mode of Operation)
٠	٠	Q.	وضع الإمساك (عدم التغير) No Change
٠	١	٠	الوضع الغير فعال Latch RESETS
١	٠	١	الوضع الفعال Latch SETS
١	١	?	وضع الخطر أو وضع غير مسموح به Invalid condition



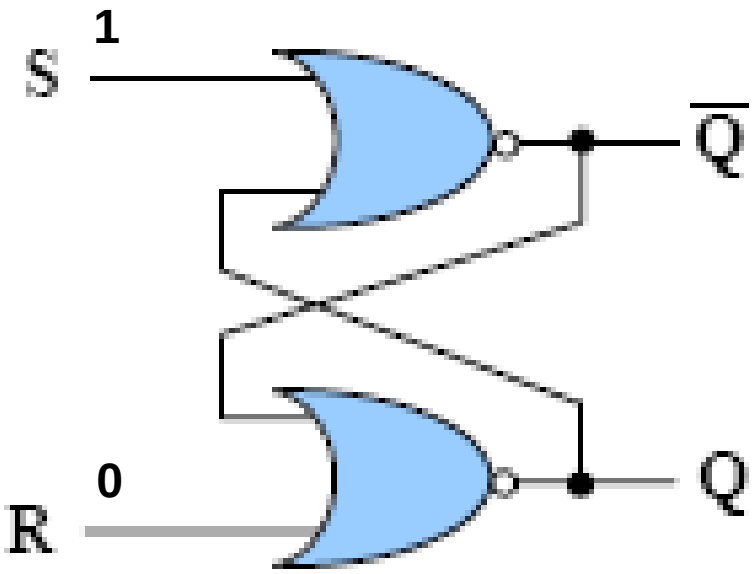
Start				Start		
0	0	0		1	1	1
1	1	1		0	0	0

When S = 0 & R = 0 Condition = No change



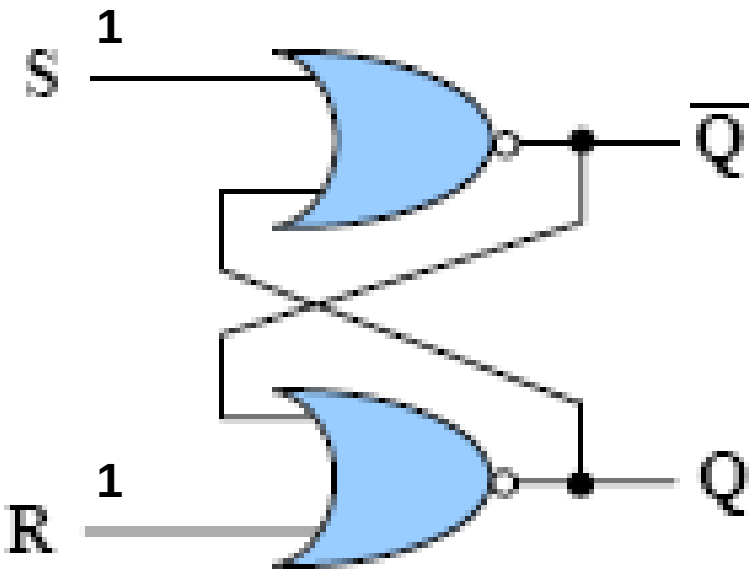
Start				Start		
0	1	1		1	1	1
1	0	0		0	0	0

When S = 0 & R = 1 Condition = Reset (Q = 0 & Q’ = 1)



Start				Start		
0	0	0		1	·	0
1	1	1		0	1	1

When S = 1 & R = 0 Condition = Set (Q = 1 & Q’ = 0)

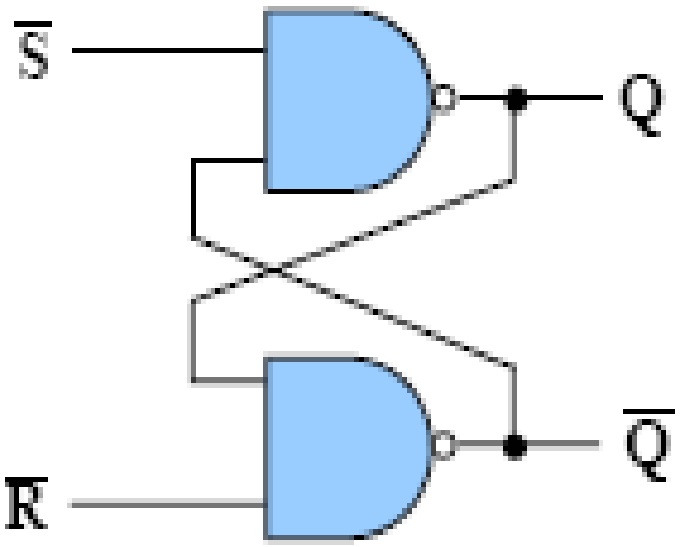


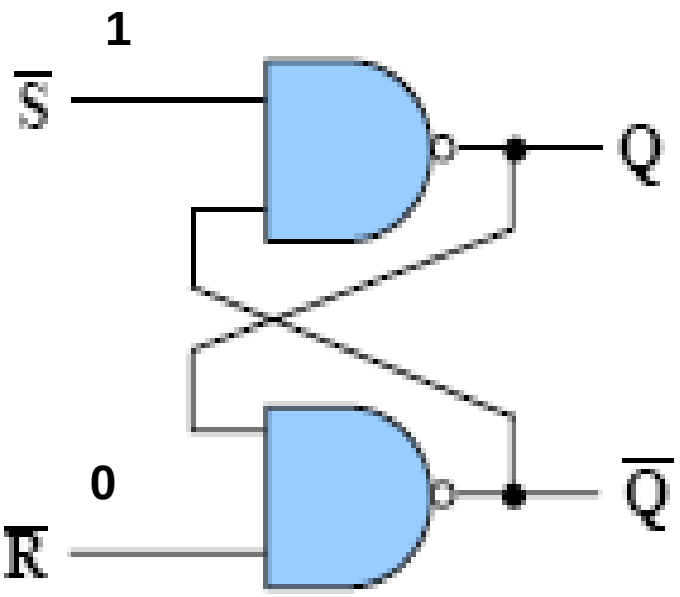
Start				Start		
0	0	0		1	0	0
1	0	0		0	0	0

When S = 1 & R = 1 Condition = invalid condition

Using Nand Gate for SR Latch (Active low inputs)

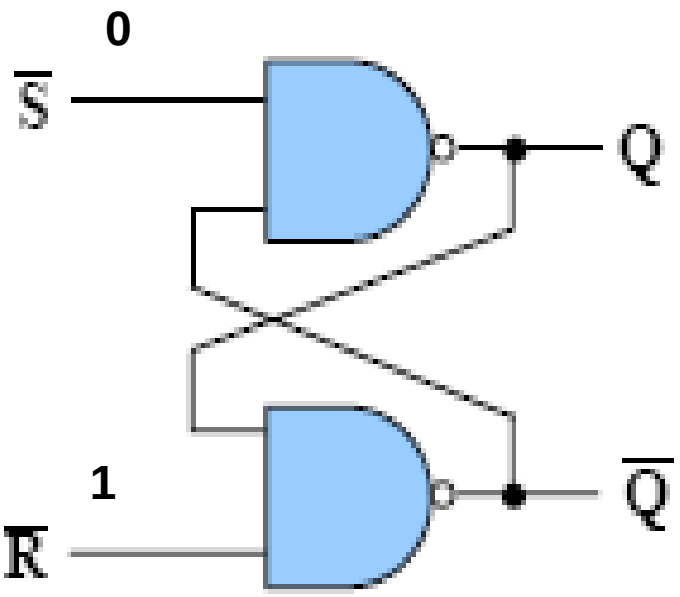
لاحظ أن المستوى الفعال لدائرة ال (NAND) هو الصفر وبالتالى
الخطر يكون عند S = 0 & R = 0





Start				Start		
0	0	0		1	0	0
1	1	1		0	1	1

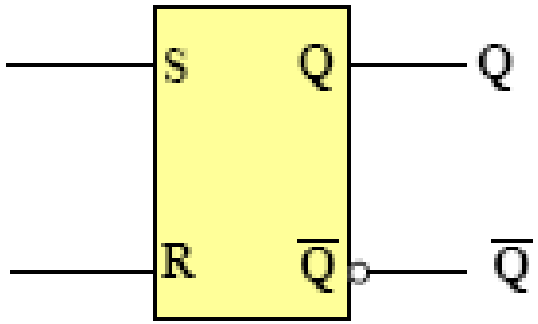
When S = 1 & R = 0 Condition = Reset (Q = 0 & Q' = 1)

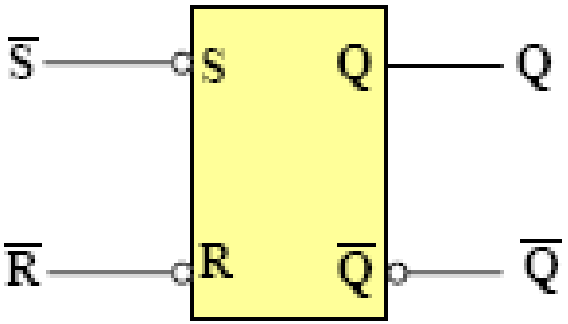


Start				Start		
0	1	1		1	١	1
1	0	0		0	0	0

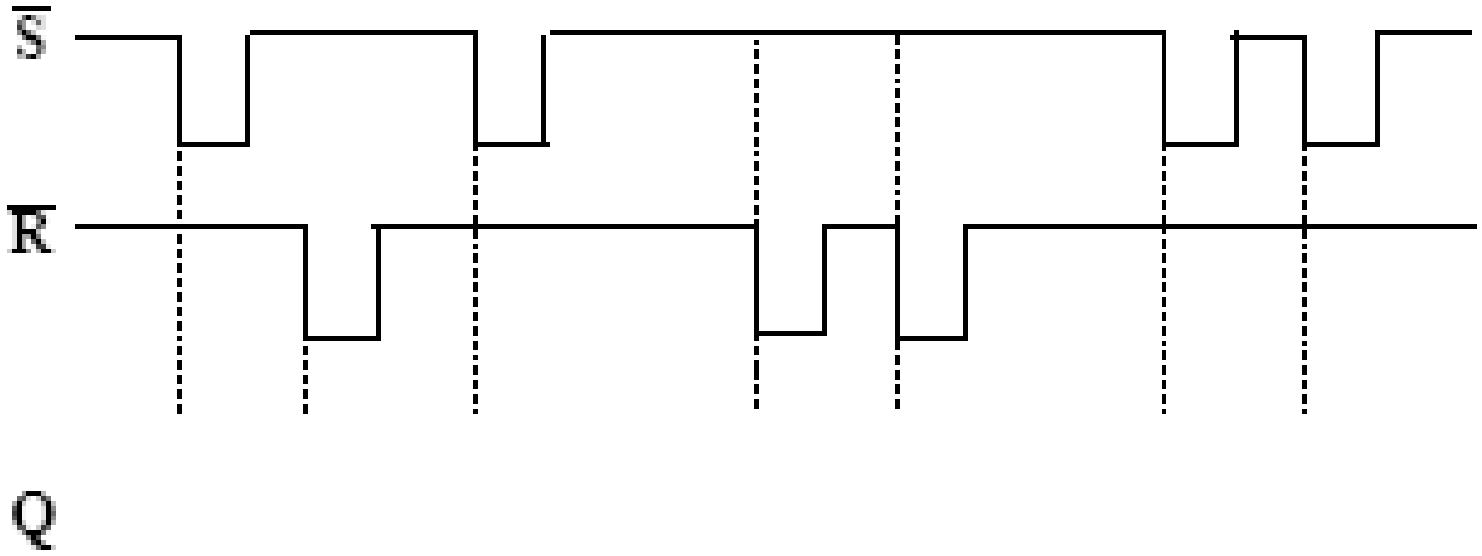
When S = 1 & R = 0 Condition = Reset (Q = 0 & Q' = 1)

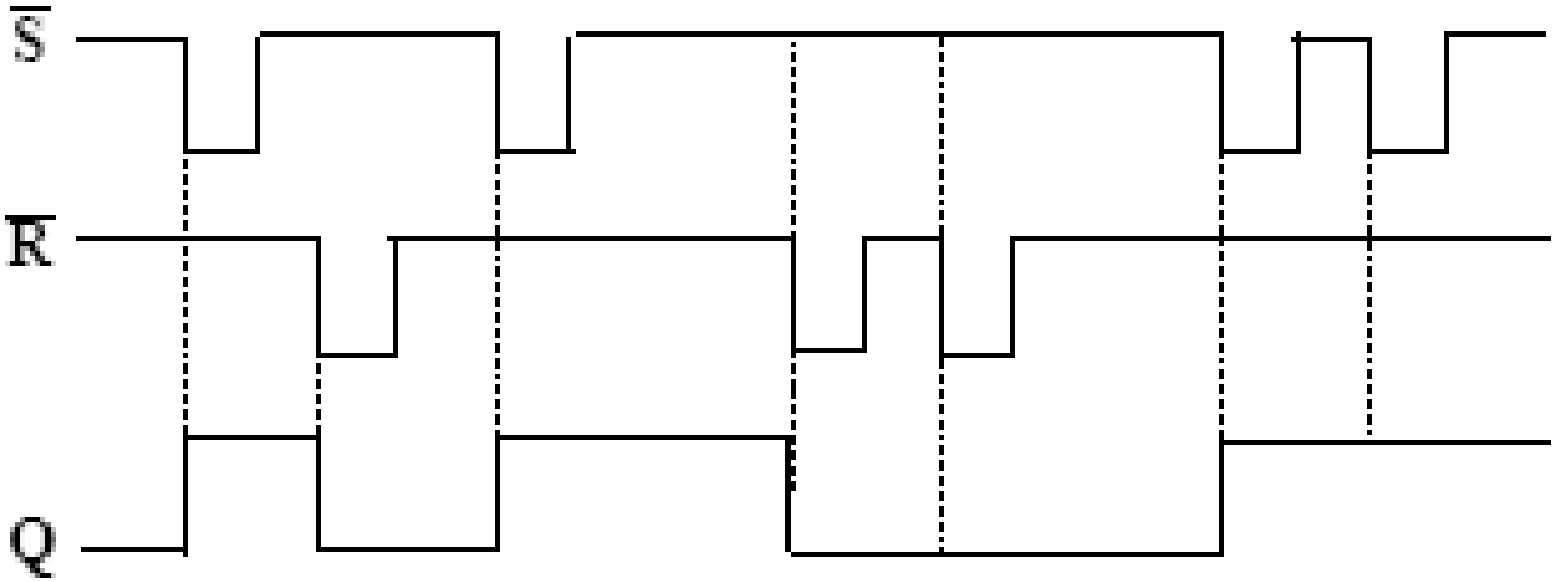
المدخلات		الخرج	وضع التشغيل
$\overline{S}$	R	Q	(Mode of Operation)
٠	٠	?	وضع الخطر أو وضع غير مسموح به Invalid condition
٠	١	١	الوضع الفعال Latch SETS
١	٠	٠	الوضع غير الفعال Latch RESETS
١	١	Q.	وضع الإمساك (عدم التغير) No Change


S
Q
Q
R
$\overline{Q}$
$\overline{Q}$


$\overline{S}$
S
Q
Q
$\overline{R}$
R
$\overline{Q}$
$\overline{Q}$

The following is a timing diagram for SR (Active low inputs) Draw the timing diagram for Q (Initial Q = 0) … Note the timing clock.



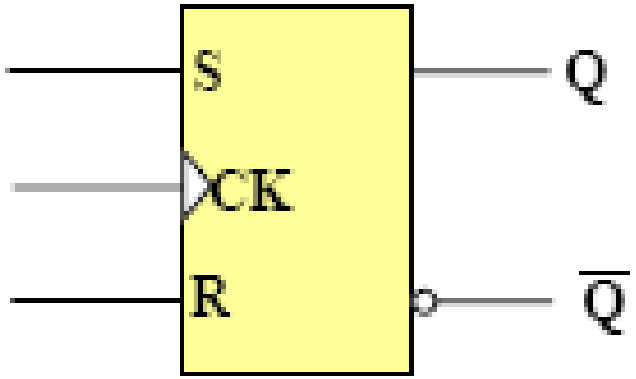

$\overline{S}$
$\overline{R}$
Q

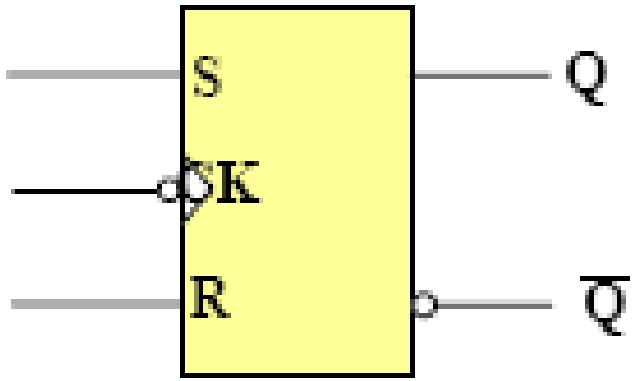
H A K

T N S

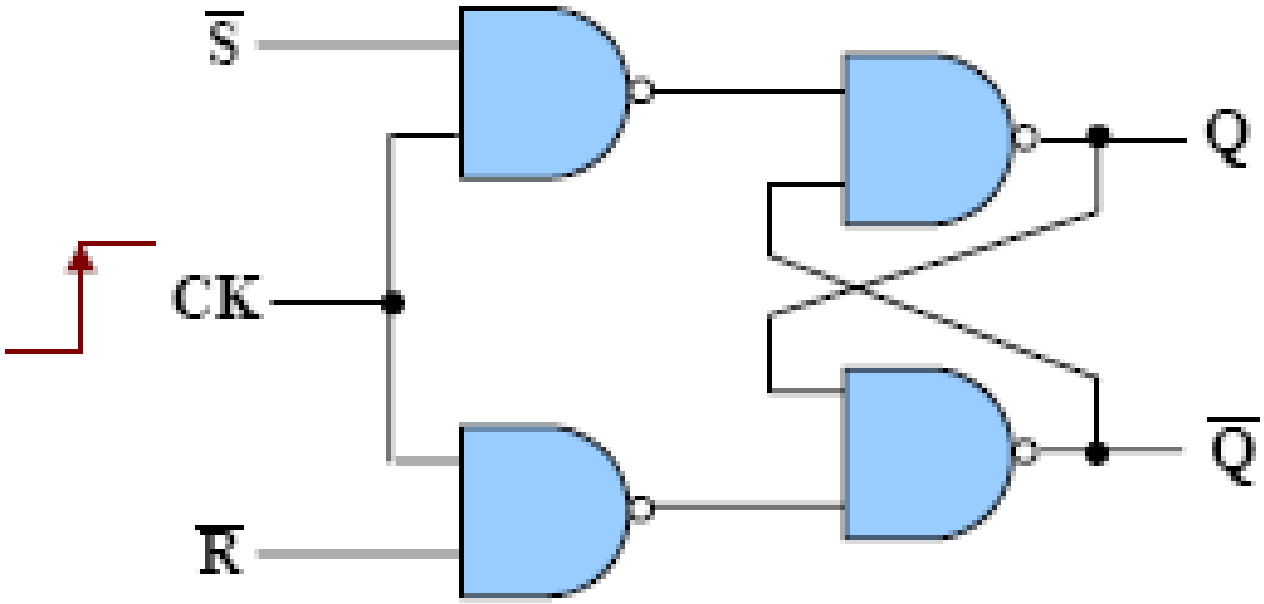
S-R Flip Flop

Block diagram for clocked S-R Flip Flop





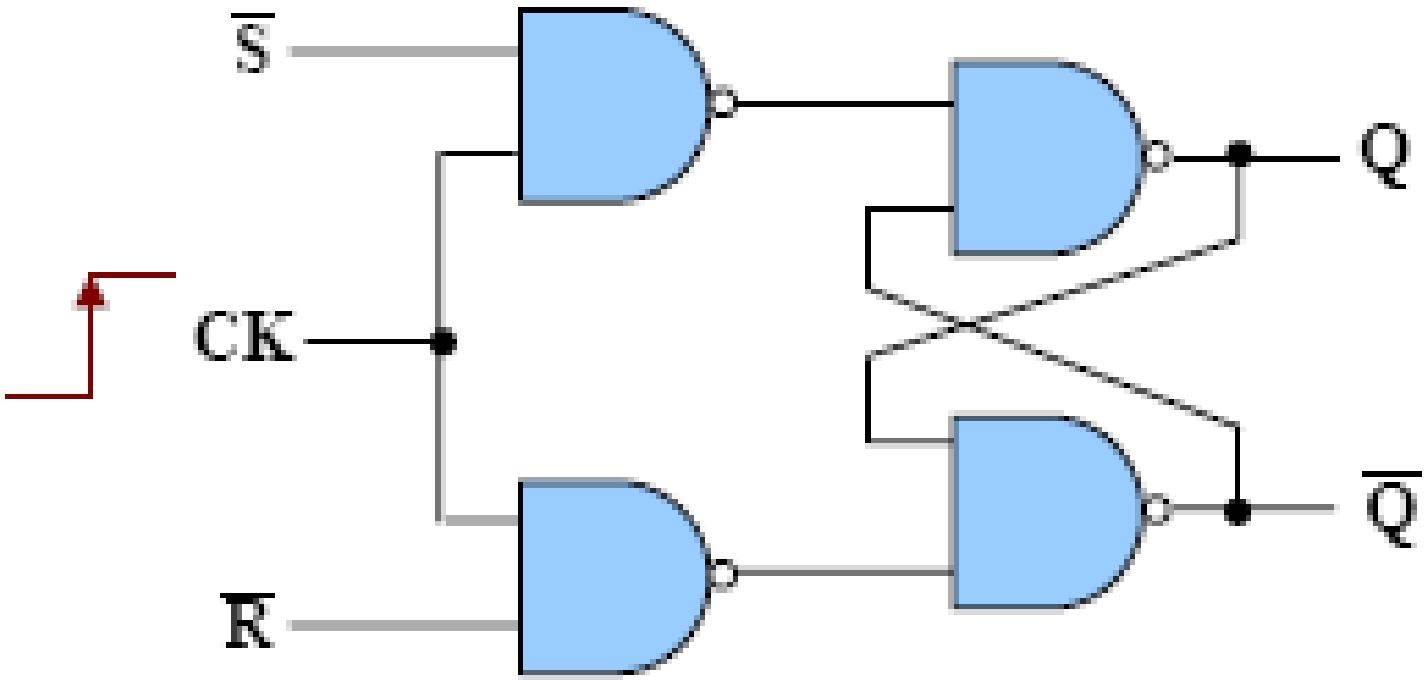
We add another (Two Nand gates)



Logic diagram for SR Latch (Flip flop) with control input

(لو فاكر (Active low inputs مع ال Nand وهو عكس ال Or وبالتالى ال 0 & 0 المشكلة .....
هنا مع وجود ال CK و ال Nand الأولى نرجع لل Active high وبالتالى تكون 1 & 1 هى المشكلة.

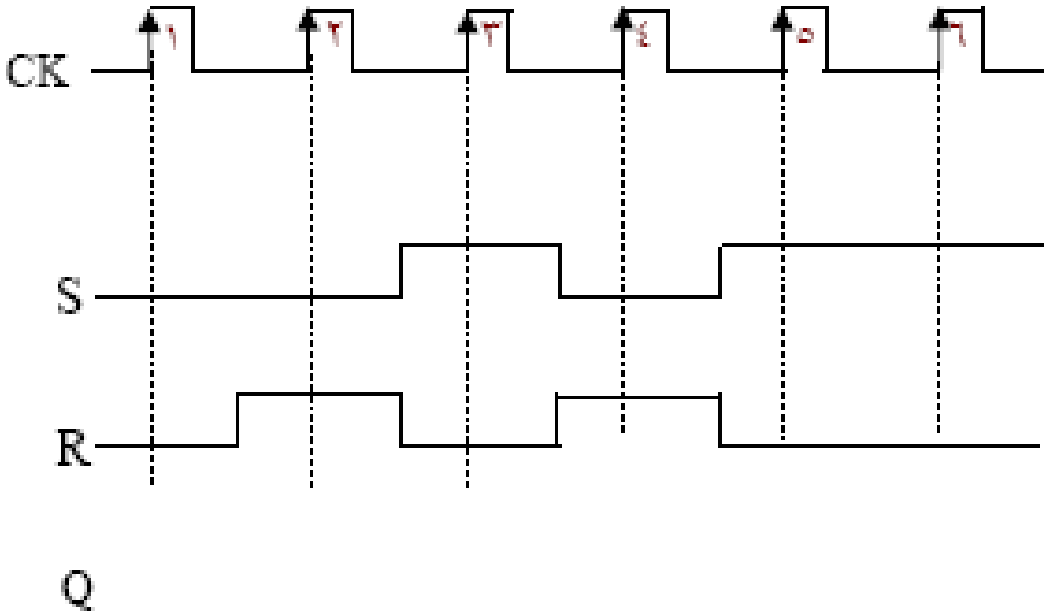
المدخلات			الخرج	وضع التشغيل
S	R	CK	Q	(Mode of Operation)
٠	٠	X	Q.	وضع الإمساك (عدم التغير) No Change
٠	١	↑	٠	الوضع غير الفعال Latch RESETS
١	٠	↑	١	الوضع الفعال Latch SETS
١	١	↑	?	وضع الخطر أو وضع غير مسموح به Invalid condition

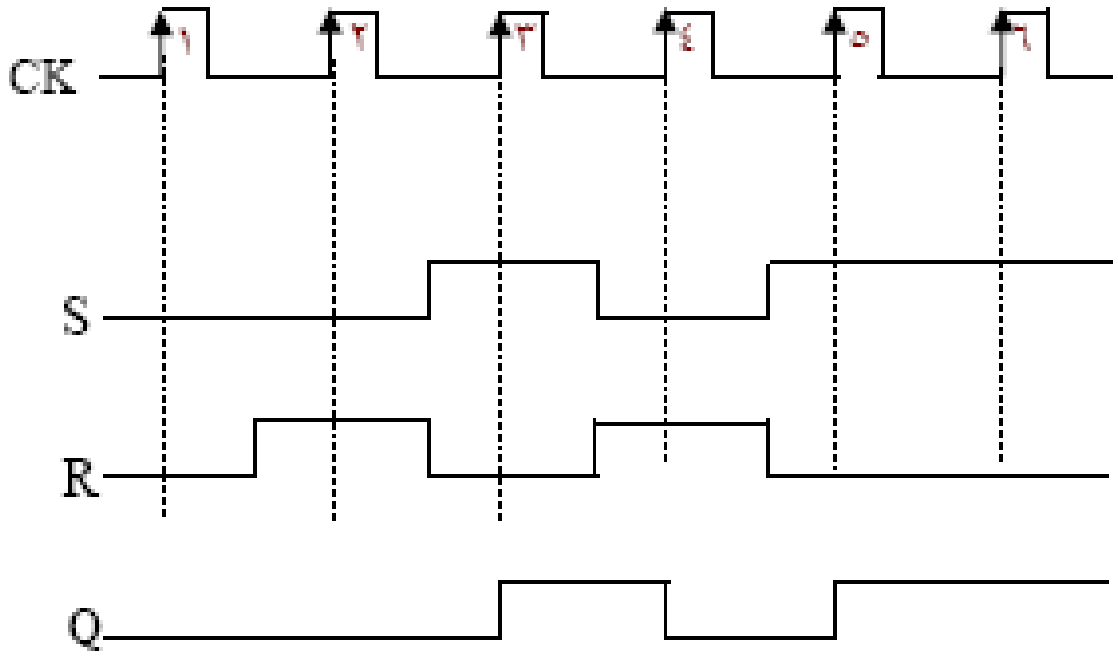

$\overline{S}$
CK
$\overline{R}$
Q
$\overline{Q}$

The following is timing diagram for S R flip flop with control input (S , R , K) ….

Draw the timing diagram for Q (initial Q = 0) …

Note the timing clock.





1 – First pulse S = 0 & R = 0 Then Q = 0

2 – Second pulse S = 0 & R = 1 Then Q still 0

3 – Third pulse S = 1 & R = 0 then Q → 1

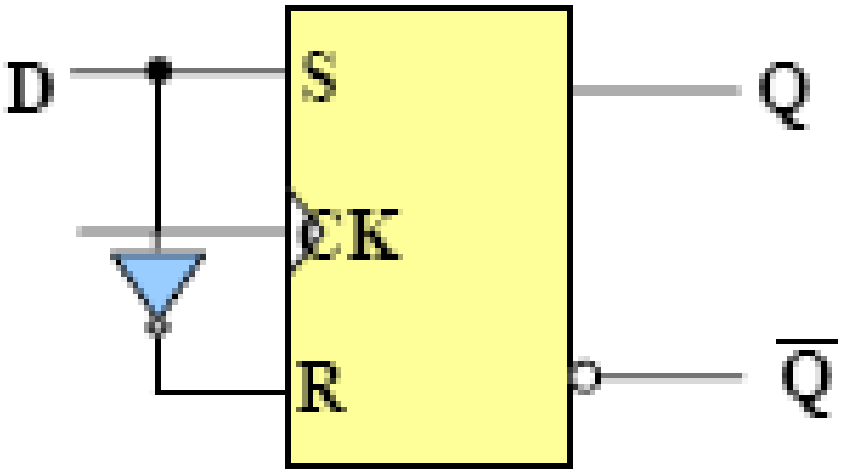
4 – Fourth pulse S = 0 & R = 1 then Q → 0

5 – fifth pulse S = 1 & R = 0 then Q → 1

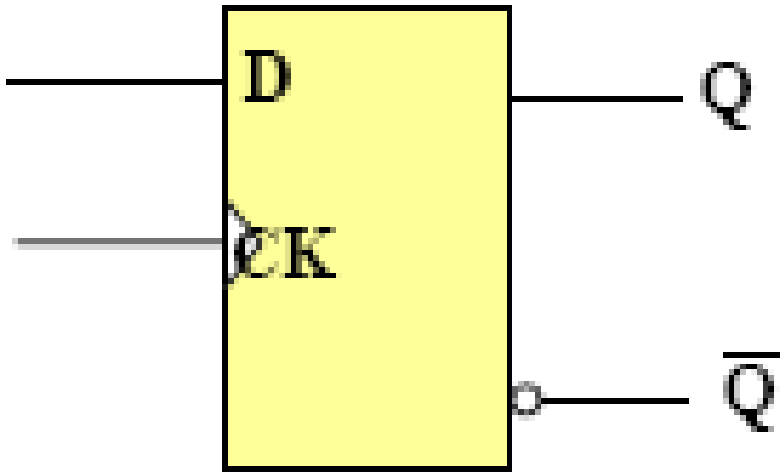
6 – Sixth pulse S = 1 & R = 0 then Q still 1

D type flip flop

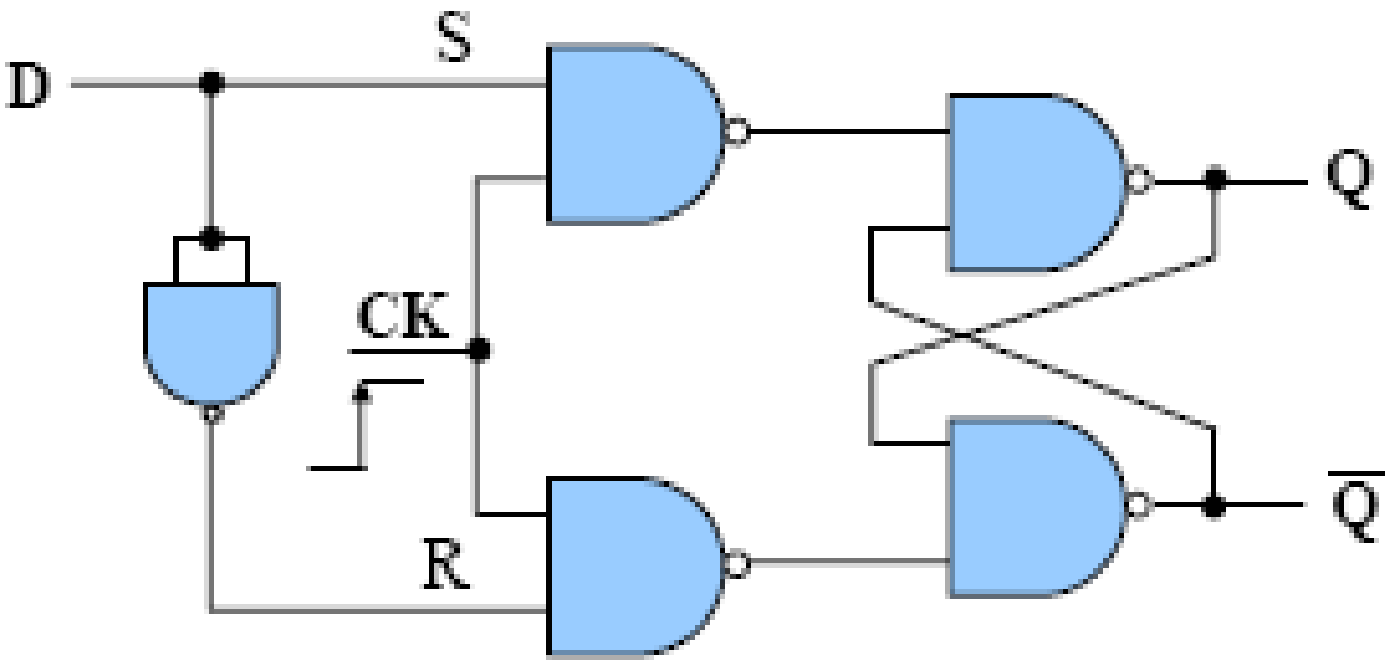
Memory unit for single bit ….Zero or One



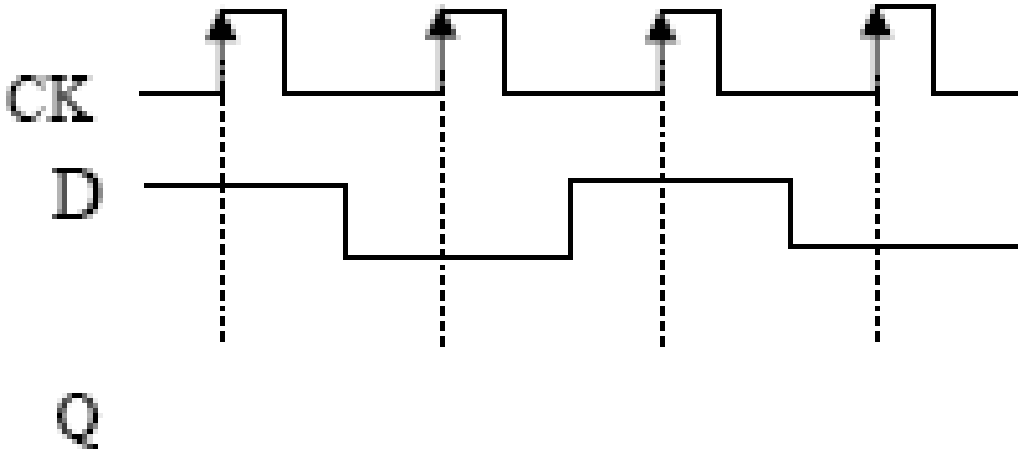
المدخلات		الخرج	وضع التشغيل
D	CK	Q	(Mode of Operation)
١	↑	١	الحالة الفعالة (SET) (stores a ١)
٠	↑	٠	الحالة الغير فعالة (RESET) (stores a ٠)

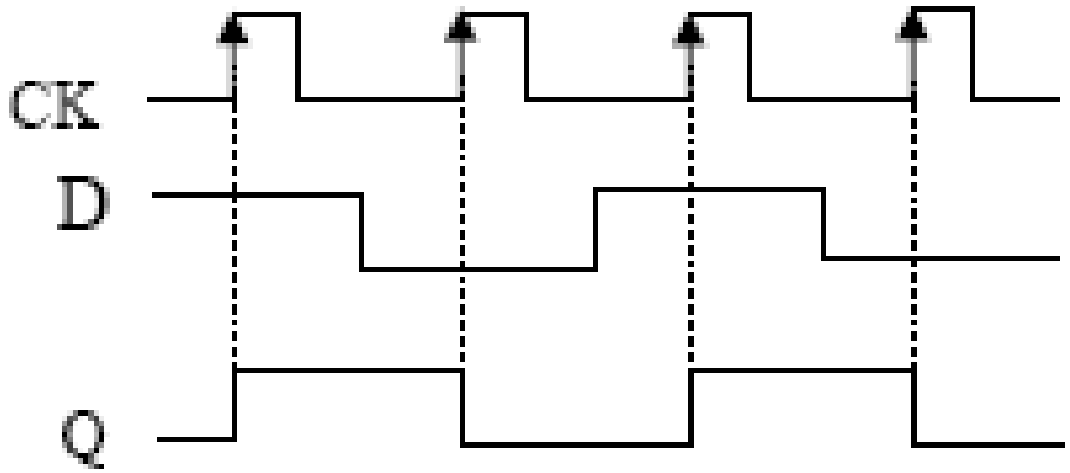


Block diagram for D flip Flop



Logic diagram for D flip Flop


CK
D
Q

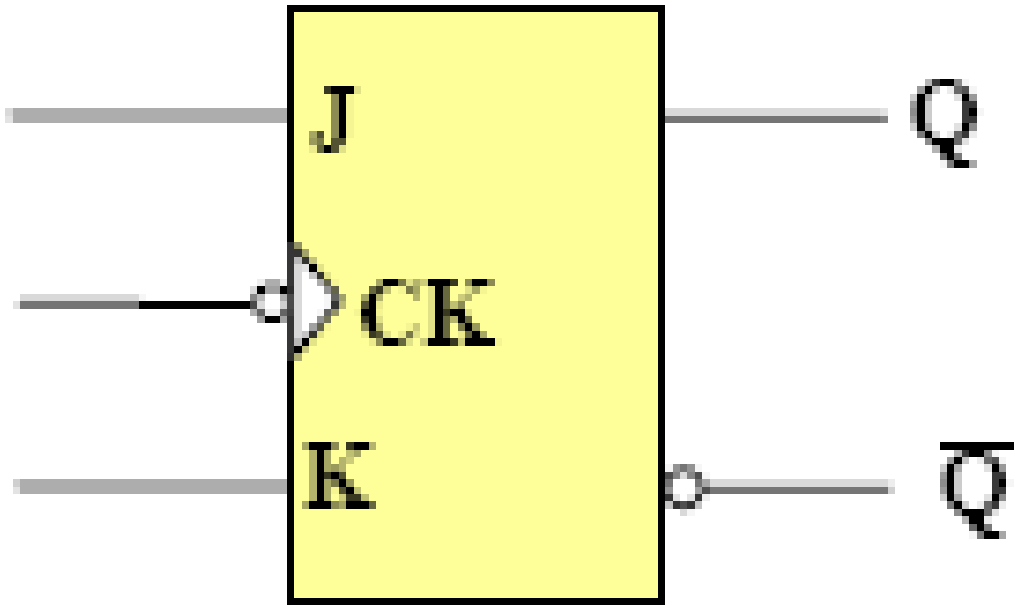

CK
D
Q

J-K Flip flop

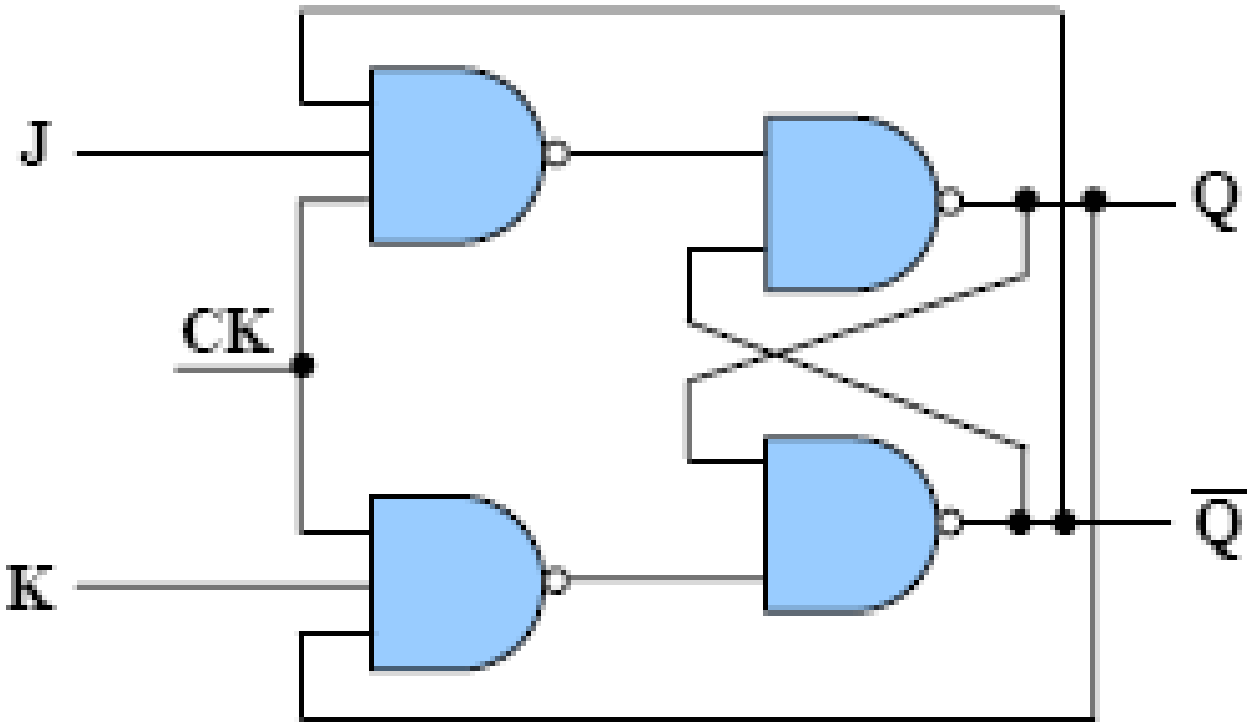
J & K are just letters

J-K flip flop is the same like SR except Q & Q' are used as inputs again …

then there is no invalid condition…. when J & K = 1 it called toggle condition where Q becomes Q' and vice versa

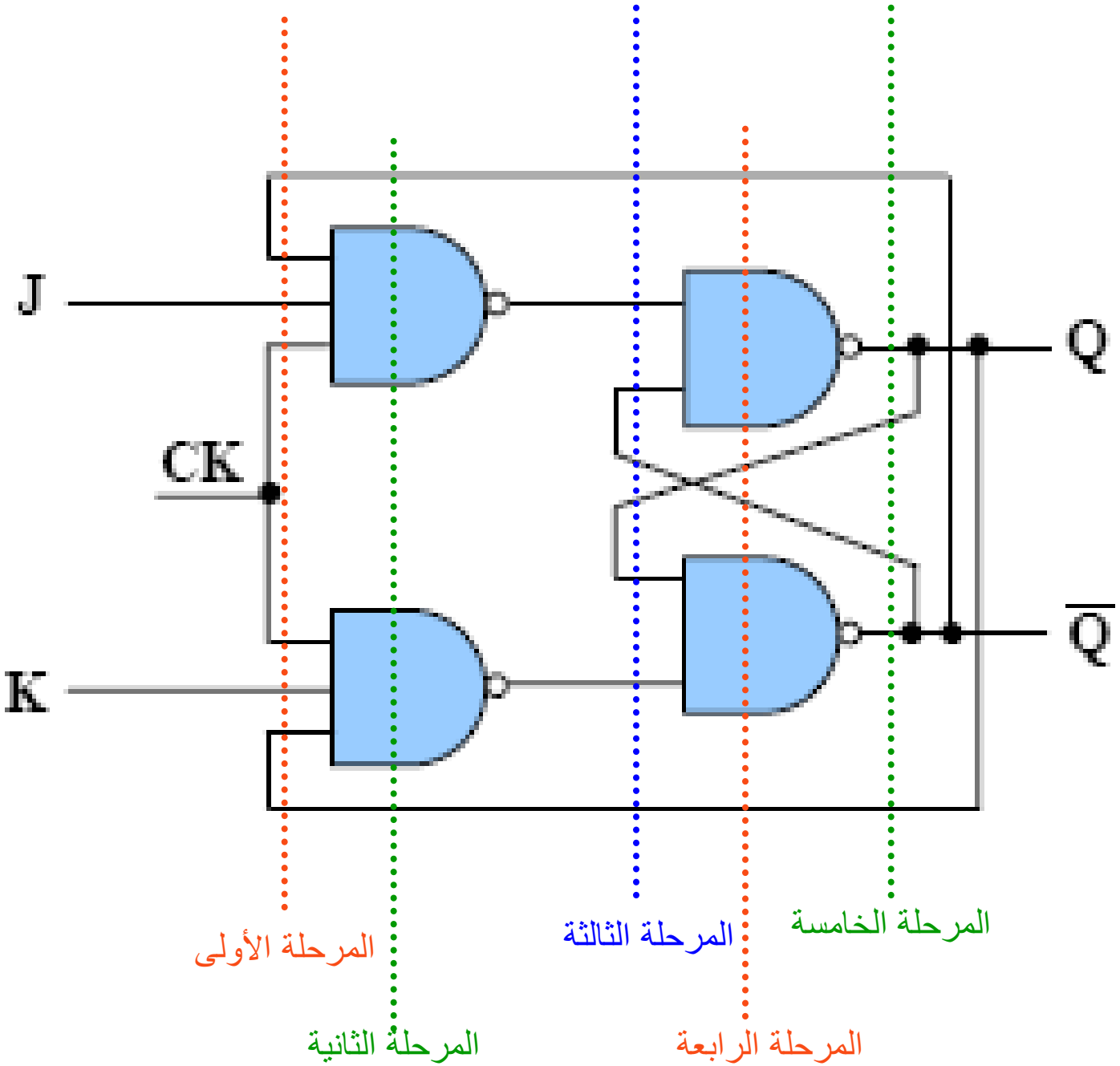


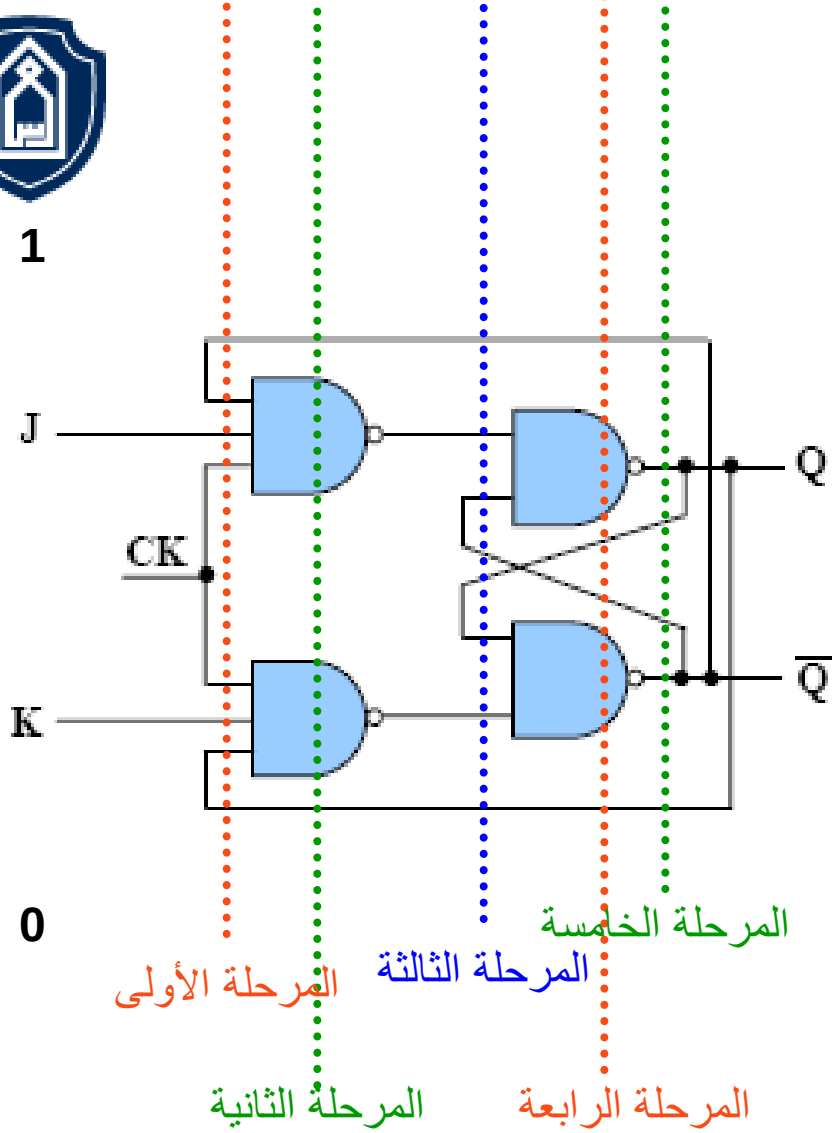
Block Diagram for J – K Flip Flop



Logic diagram for J – K Flip Flop

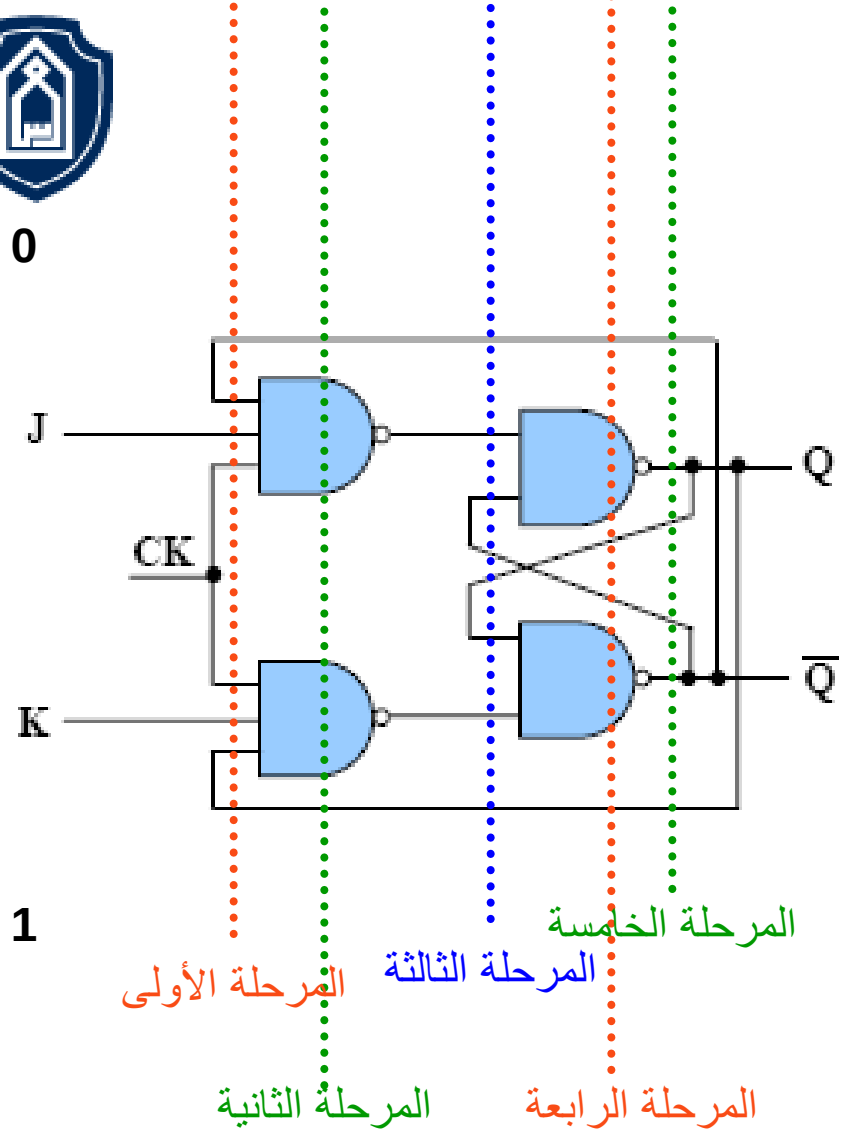
المدخلات			الخرج	وضع التشغيل
J	K	CK	Q	(Mode of Operation)
٠	٠	↓	Q_0	وضع الإمساك (عدم التغير) No Change
٠	١	↓	٠	الوضع غير الفعال (RESET)
١	٠	↓	١	الوضع الفعال (SET)
١	١	↓	$\overline{Q}_0$	وضع التبديل Toggle


J
CK
K
Q
$\overline{Q}$
المرحلة الأولى
المرحلة الثانية
المرحلة الثالثة
المرحلة الرابعة
المرحلة الخامسة



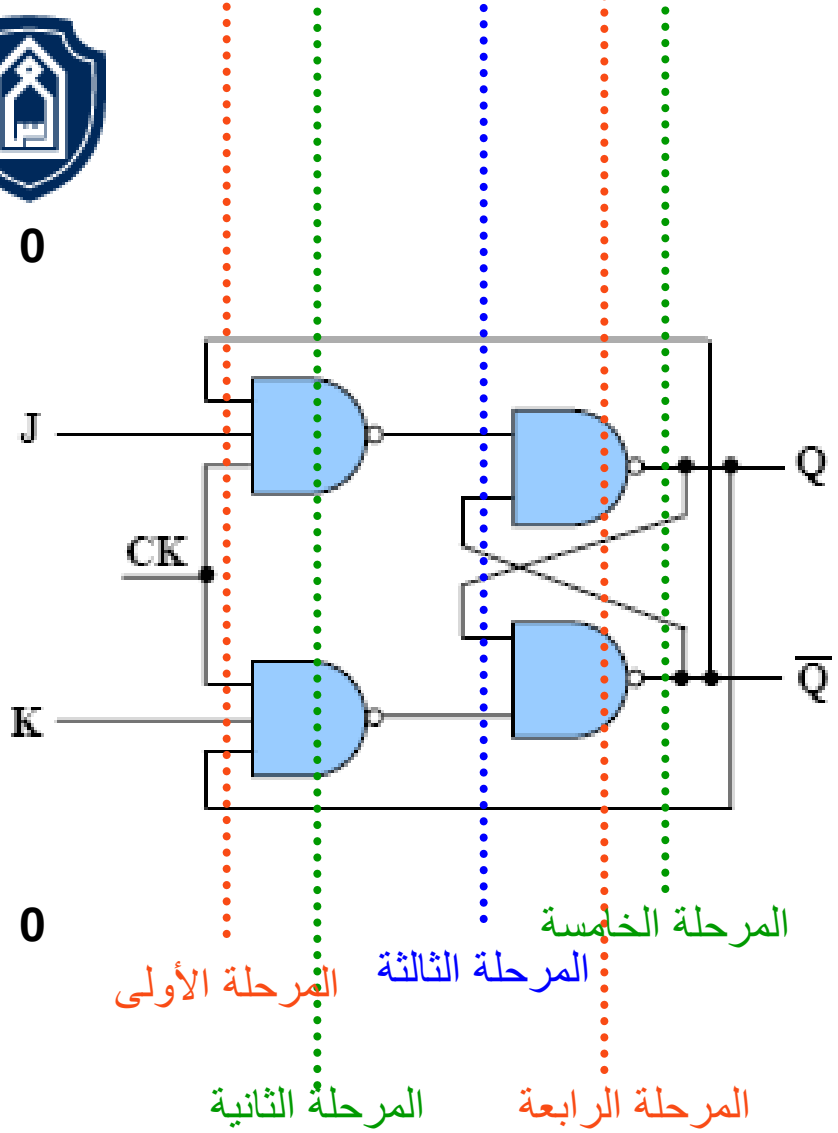
Start				Start		
0	1	1		1	1	1
1	0	0		0	0	0

When J = 1 & K = 0 Condition = Set (Q = 1 & Q' = 0)



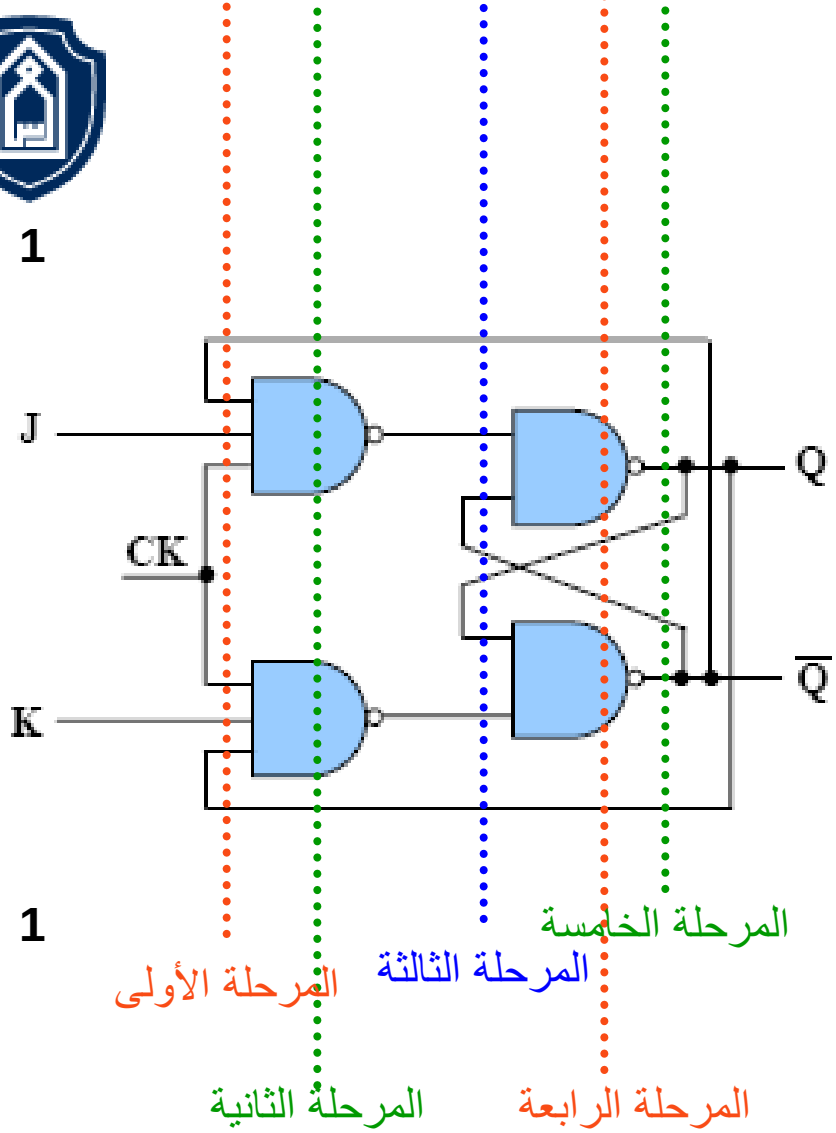
Start				Start		
0	0	0		1	0	0
1	1	1		0	1	1

When J = 0 & K = 1 Condition = Reset (Q = 0 & Q' = 1)



Start				Start		
0	0	0		1	1	1
1	1	1		0	0	0

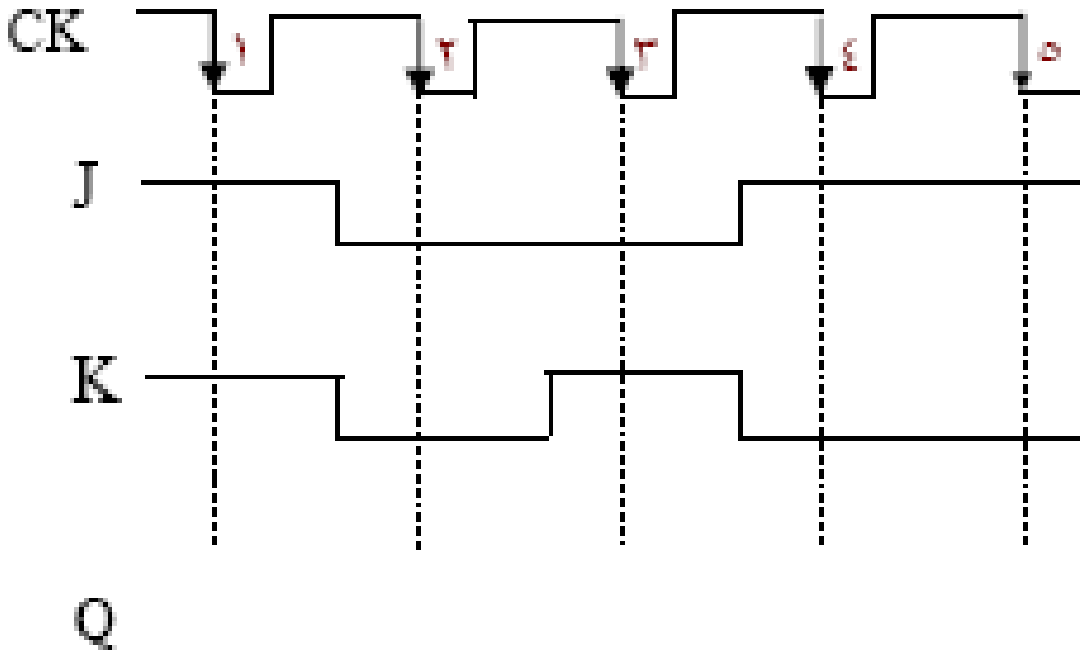
When J = 0 & K = 0 Condition = No change

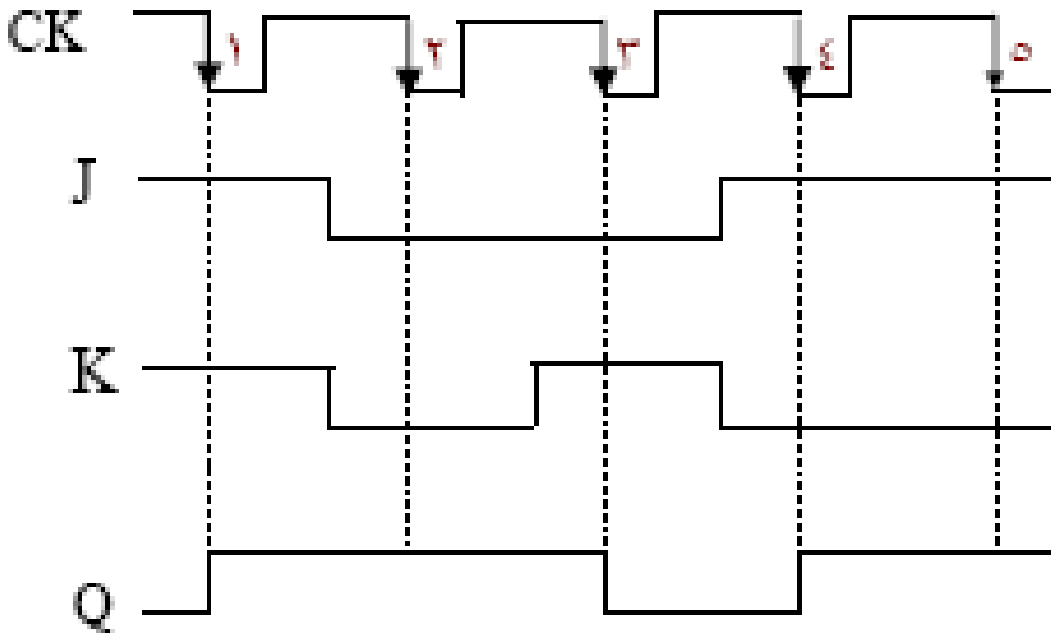


Start				Start		
0	1	1		1	0	0
1	0	0		0	1	1

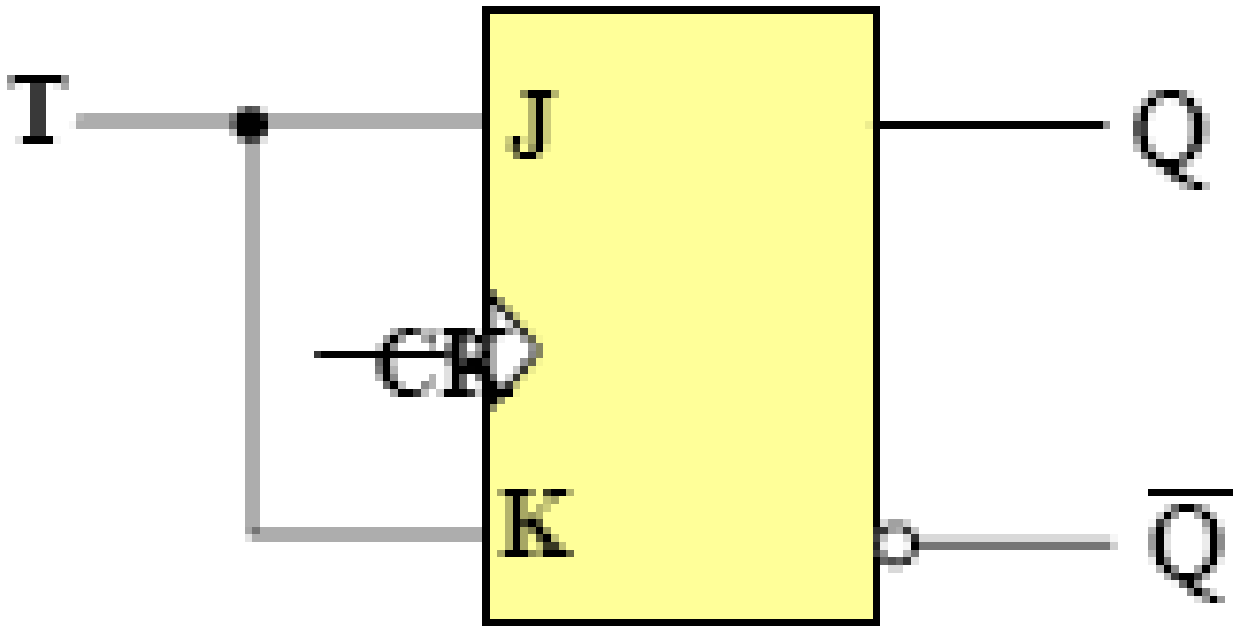
When J = 1 & K = 1 Condition = Toggle

The following is timing diagram for J K flip flop …….Draw the pulse shape for the output Q (initial Q = 0) clock pulse from (1) to (0) ↓



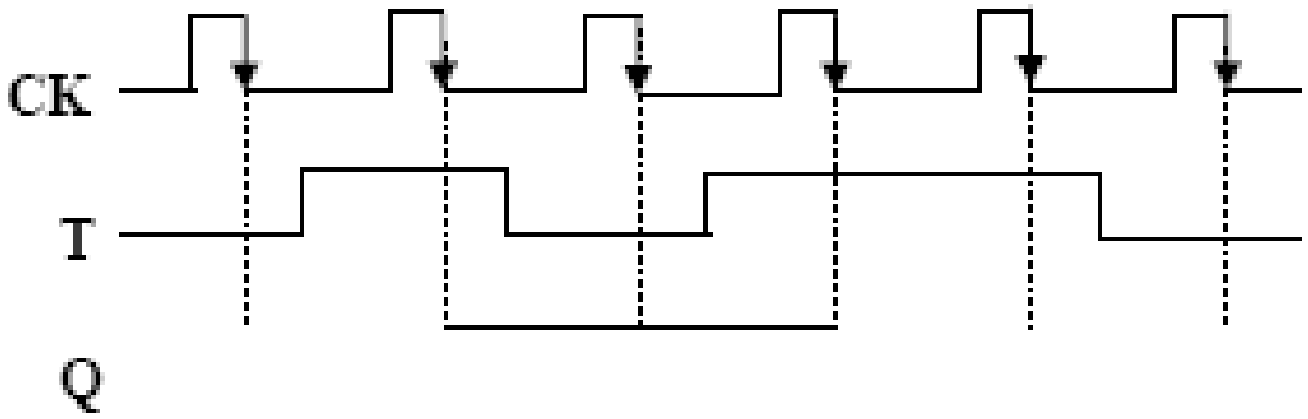

CK
J
K
Q
١
٢
٣
٤
٥

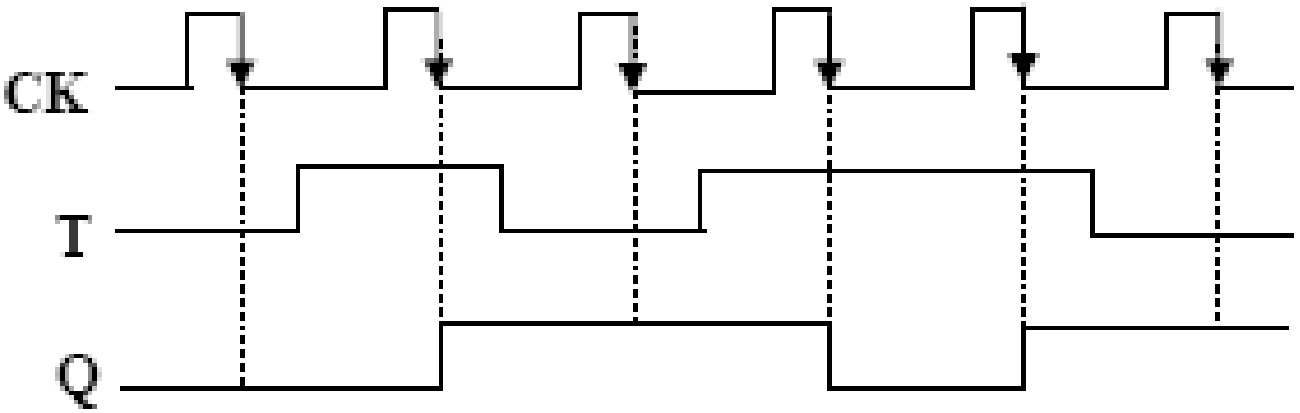
T – Type flip flop

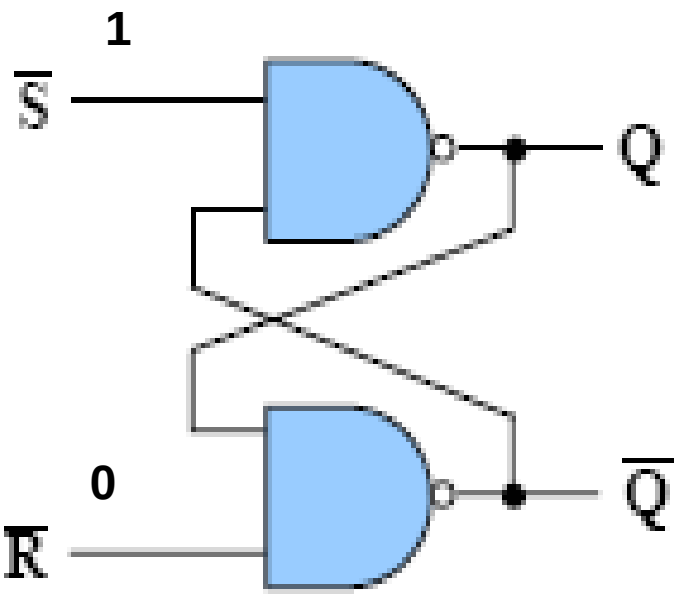


From J-K flip flop connect J with K

المدخلات		الخرج	وضع التشغيل
T	CK	Q	(Mode of Operation)
٠	↓	Q_0	وضع الإمساك (عدم التغير) No Change
١	↓	$\overline{Q_0}$	وضع التبديل Toggle


CK
T
Q


CK
T
Q



Start				Start		
0	0	0		1	0	0
1	1	1		0	1	1

When S = 1 & R = 0 Condition = Reset (Q = 0 & Q' = 1)