

CS/B.Tech/EE/Odd/Sem-5th/EE-504C/2015-16



**MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY,  
WEST BENGAL**

**EE-504C**

**MICROPROCESSORS AND MICROCONTROLLERS**

Time Allotted: 3 Hours

Full Marks: 70

*The questions are of equal value.  
The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.  
All symbols are of usual significance.*

**GROUP A  
(Multiple Choice Type Questions)**

1. Answer any ten questions. 10×1 = 10

- (i) The control signal used to distinguish between an I/O operation and memory operation is  
 (A) ALE (B) IO/M\*  
 (C) SID (D) SOD
- (ii) Whenever PUSH instruction is executed the stack pointer is  
 (A) Incremented by 1 (B) Incremented by 2  
 (C) Decrementd by 1 (D) Decrementd by 2
- (iii) The number of T-States required to execute an Opcode fetch operation is  
 (A) 1 (B) 2  
 (C) 3 (D) 4

Turn Over

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(iv) Which of the following is not a maskable interrupt?

- (A) TRAP (B) INTR  
 (C) RST 7.5 (D) RST 3

(v) LDA 2050<sub>H</sub> is a \_\_\_\_\_ byte(s) instruction

- (A) 1 (B) 2  
 (C) 3 (D) 4

(vi) The number of register pair of 8085 are \_\_\_\_\_

- (A) 1 (B) 2  
 (C) 3 (D) 4

(vii) The instruction XCHG exchanges the contents of

- (A) BC and HL pairs  
 (B) BC and DE pairs  
 (C) BC pair and Accumulator  
 (D) DE and HL pairs

(viii) The number of machine cycles for 'IN' instruction are

- (A) 1 (B) 2  
 (C) 3 (D) 4

(ix) The address bus of 8085 microprocessor is of \_\_\_\_\_ bits

- (A) 5 (B) 8  
 (C) 12 (D) 16

(x) 8254 is a \_\_\_\_\_

- (A) Interrupt controller (B) Programmable interval timer  
 (C) Counter (D) USART IC

(xi) DAD instruction is used to

- (A) Decimal Adjust Delay (B) Add register pair to H-L registers  
 (C) Don't care and Add (D) None of these

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(xii) The number of flag bits of 8085 microprocessor are \_\_\_\_\_

- (A) 2 (B) 3  
(C) 4 (D) 5

**GROUP B**  
(Short Answer Type Questions)

Answer any three questions.

3 × 5 = 15

2. With a neat timing diagram explain the purpose of the instruction 'STA' for 8085 microprocessor. 5
3. What do you mean by a 'Subroutine'? What is its necessity in case of 8085 microprocessor? 5
4. What are flag bits? Explain the bit configuration of 8085 flag register. 2+3
5. What is a DMA controller? With diagram explain the interfacing of 8237 DMA controller with 8085 microprocessor. 2+3
6. Elaborate the following instructions related to 8085 programming. 5  
(i) INTA' (ii) HOLD (iii) READY (iv) SID (v) SOD

**GROUP C**  
(Long Answer Type Questions)

Answer any three questions.

3 × 5 = 15

7. (a) Explain with diagram the hardware architecture of 8085 microprocessor. 5  
(b) What do you mean by memory mapped I/O? How are MEMW' and MEMR' signals generated? 3+2  
(c) Design an interfacing circuit using a 3-8 decoder to interface a 2732 (4096×8) EPROM chip. 5

*Handwritten note:* All questions

Turn Over

8. (a) What are Vectored and Non-Vectored Interrupts? 5  
(b) Write a program to generate a continuous square wave with the period of 500 μs. Assume the system clock period is 325 ns and use bit D<sub>0</sub> to output the square wave. 5  
(c) What are Restart instructions? How many types of Restart instructions are there in 8085 microprocessor? 3+2
9. (a) What are 'Tri-State Devices'? What is the function of a 'Tri-State Buffer'? 2+3  
(b) What is a 'Counter'? Explain in brief the 'loop-technique' to design a Counter. 2+3  
(c) Write a program to count continuously in hexadecimal from FF<sub>11</sub> to 00<sub>11</sub> in a system with a 0.5 μs clock period. Use register C to set up a one millisecond delay between each count and display the numbers at one of the output ports. 5
10. (a) What are the different addressing modes of 8086 microprocessor? 5  
(b) Explain the hardware architecture of 8051 microcontroller with diagram. 5  
(c) In how many modes can 8254 operate? Explain in brief. 5
11. Write short notes on any three of the following: 3×5  
(a) Stack Memory  
(b) Assemblers vs. Cross-Assemblers  
(c) BSR mode of 8255  
(d) Min-Max mode of 8086  
(e) 8259A Programmable interrupt controller.