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ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE - 2009 **DIGITAL ELECTRONICS & INTEGRATED CIRCUITS SEMESTER - 4**

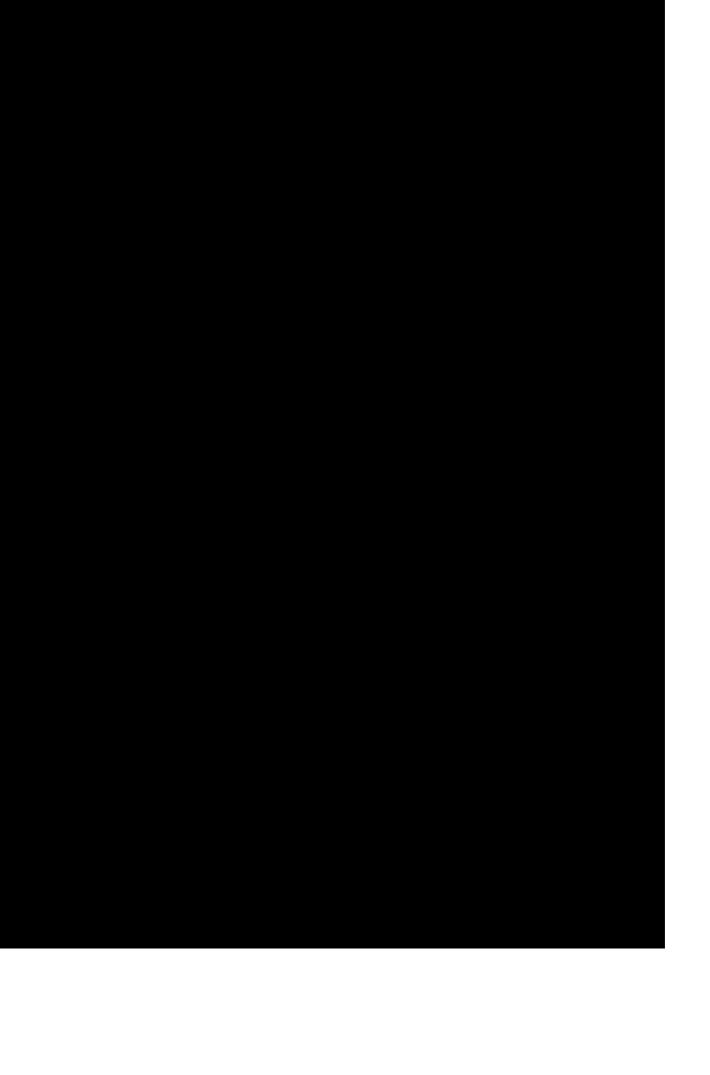
Time : 3 Hours]	[Full Marks : 70
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GROUP - A

		(M)	iltiple Choice	туре 9	uestions ;	
Cho	ose th	ne correct alterna	tives for any te	n of the	e following :	10 × 1 = 10
ŋ	The octal equivalent of the binary number 11010111 is					
	a)	656		b)	327	
	c)	653		d)	D7.	
11)	ne Boolean function					
٠.	. A+	$AB^{\dagger} + AB^{\dagger}C$ is	equal to			
	a)	zero		b) -	1	
	c)	4		d)	7 .	
H1)	Ind	entify the operati	ion of the follow	ving log	ic gate circuit.	
			<u></u>	1		
					<u>*</u> _	
			-(,J		
	a)	OR gate		b)	AND gate	
	c)	NOT gate		d)	none of these.	
	11)	i) The a) c) ii) The A+ a) c) iii) Ind	Choose the correct alternation of the octal equivalent all 656 cl 653 ii) The minimum number $A + AB' + AB'C$ is all zero cl 4 iii) Indentify the operation of the operation o	Choose the correct alternatives for any term of the octal equivalent of the binary in a) 656 c) 653 ii) The minimum number of NAND gate A + AB' + AB' C is equal to a) zero c) 4 iii) Indentify the operation of the following a control of the following at the control of the following a co	Choose the correct alternatives for any ten of the interval of the binary number a) 656 b) c) 653 d) ii) The minimum number of NAND gates required A + AB' + AB' C is equal to a) zero b) c) 4 d) iii) Indentify the operation of the following log allowed as a contract of the followi	a) 656 b) 327 c) 653 d) D7. ii) The minimum number of NAND gates required to implement the A + AB' + AB' C is equal to a) zero b) 1 c) 4 d) 7. iii) Indentify the operation of the following logic gate circuit.

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3. Minimize the following expression in SOP form using Quine McClusky method:

$$F(A, B, C, D) = \sum m(1, 2, 3, 8, 9, 10, 11, 14) + \sum d(7, 15).$$

- Explain the race around condition. Draw the Master/Slave JK flip-flop using all NAND gates.
- 5. Implement a full-adder circuit using 3 to 8 decoder with all active high outputs and other necessary logic gates.
- 6. Draw and explain the circuit of 8×1 MUX using two 4×1 MUX and one 2×1 MUX.

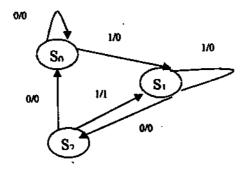
GROUP - C

(Long Answer Type Questions)

Answer any three of the following questions.

 $3\times15=45$

7. a) Design a clocked synchronous sequential network whose state diagram is given below:



- b) Design a combinational circuit, which converts excess 3 number to its
 corresponding BCD number.
- 3. a) Implement the following Boolean expressions using Decoder.

$$F_1(A, B, C, D) = \sum (1, 2, 5, 7, 8, 10, 12, 13).$$

b) Implement a full adder circuit using minimum number of NOR gates only. 5

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