Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech(ECE/NEW)/SEM-7/EC-702/2009-10

2009

EDA FOR VLSI DESIGN

Time Allotted : 3 Hours | Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) The example of physical defects is
   a) oxide defects
   b) resistive shorts and opens
   c) slower transition
   d) none of these.

ii) The example of electrical faults is
   a) slower transition
   b) logical stuch-at-0 or stuck-at-1
   c) bridging faults
   d) none of these.

iii) LUT is used in
   a) CPLD b) ASIC
   c) FPGA d) SPLD.

iv) What is the full form of VHDL ?

a) Very high speed digital logic
b) Verilog hardware description language
c) Very high digital logic
d) None of these.

v) In a PLA

a) only AND array is programmable
b) only OR array is programmable
c) both OR & AND array are programmable
d) macro cell is the building block.

vi) The graph that is used to represent an algorithm is known as

a) a signal flow graph b) a data flow graph
c) a control flow graph d) a binary decision graph.

vii) High level synthesis has design constraints like

a) Area b) Timing
c) Power d) All of these.

viii) VHDL is a

a) multi threaded program
b) a programming language like C
c) single user program
d) sequential program.

ix) The suitable interconnect among the following is

a) Aluminium b) Gold
c) Copper d) Silver.

x) Minimum transistor gates required to design XOR gate is

a) six b) eight
c) twelve d) ten.

xi) VLSI design flow is a
  a) cyclic process only
  b) parallel process
  c) sequential and cyclic process
  d) none of these.

xii) In VHDL, sequential statements are defined in the
  a) architecture b) process
  c) package d) none of these.

xiii) Which of the following logical operator does not follow associative properties ?
  a) OR b) XOR
  c) NAND d) AND.

xiv) In full custom ASIC design
  a) All the diffused layers are defined
  b) All the lithographic layers are defined
  c) All the metal layers are defined
  d) None of these.

xv) Which of the following is not a part of FPGA ?
  a) RTL b) I/O
  c) PI d) CLB.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. a) What is ASIC ? Give its classification. 2
   b) Why VLSI design flow is often called as cycle ? Explain. 3

3. What are the steps in VLSI design flow ? Explain.

4. a) What do you mean by testability of a circuit ?
   b) Describe the method of Built-In Self Test Technique. 1 + 4

5. What is PLA ? Derive a PLA programming table for the combinational circuit that squares a 3 bit number. 1 + 4

6. What is an FPGA ? How is it different from CPLD ? What are its advantages ? 1 + 2 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) What are the issues that a hardware description language must address ? Explain briefly. 5

   b) Describe the purpose of the following : 5

      i) the entity declaration

      ii) the architecture body.

   c) Write the VHDL code for HALF ADDER circuit. 5

8. a) Why FPGA is preferred over CPLD ? Explain the architecture of FPGA. 4

   b) Write the steps for programming a FPGA. 4

   c) How Look Up Table (LUT) is used to program an FPGA ? Explain with an example. 7

9. a) What are the characteristics of any material to be used as interconnect ? 5

   b) What are problems associated with aluminum interconnect ? 5

   c) "Placement is a fundamental problem in physical design'". Explain with an example and necessary diagrams. 5

10. a) How the logic capability of PLA measured ? 3

    b) What are the differences between PAL and PLA ? 2

    c) Implement the following functions using PLA : 5

       i) $f = AB' + A'B$

       ii) $f = A + (B + C').D$

    d) Explain the arhitecture of PLD. 5

11. Write short notes on any *three* of the following : 3×5

    a) Scan Based Techniques

    b) Built-In-Self Test (BIST) techniques

    c) XILINX FPGA architecture

    d) Analog design automation tools

    e) NORA logic.