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Roll	No. :	:				no cy's soundage 3nd Explorer	
Invi	gilato	or's Si	ignature :			••••	
C	S/B	.Tecl	h (CSE/IT/PW	E/EEE)/SI	EM-5/EI-5	02/2010-11	
			2	010-11			
M	IICF	OP	ROCESSOR	AND MIC	ROCONT	ROLLER	
Time Allotted: 3 Hours					Full Marks : 70		
		Th	e figures in the i	margin indice	ate full marl	cs.	
Ca	ındid	ates (are required to g as f	ive their ans ar as practic		r own words	
			G	ROUP – A			
			(Multiple Cho	oice Type G	uestions ()	
1.	. Choose the correct alternatives for any <i>ten</i> of the following :						
						10 × 1 = 10	
	i) What is the vector location of NMI?						
		a)	H00000	b)	00008H		

00010H 00014H. c) d) The ii) interrupt pin available in the 8085A microprocessor chip is a) **ALE** b) **HLDA**

INTER d) SOD. c)

For 8257 controller is the highest priority iii) channel by default.

CH-3 b) CH-0 a)

CH-1 d) any channel. c)

The clock frequency is 60 Hz. The clock interrupt iv) handler on a computer needs 2 msec per clock tick. What percentage of the CPU is devoted to the clock?

7.5 1.2b) a) c) 12 d) 18.5.

5001 [Turn over

v)	v) What is the BSR control word to set PC ₄ ?					
	a)	09	b)	07 To Annual Ly Exemple of Explanat		
	c)	04	d)	05.		
vi)	The total memory space available in 8086 is					
	a)	16 kB	b)	64 kB		
	c)	1 MB	d)	256 kB.		
vii)	An 8-bit A/D converter has a resolution of					
	a)	$1/2^4$	b)	$1/2^8$		
	c)	$1/2^2$	d)	$1/2^{16}$.		
viii)	Sele	ct the invalid instruction	n:			
	a)	MOV M, A	b)	ADI 67		
	c)	LDAX B	d)	STAX H.		
ix)	The maximum operating frequency of 8254 is					
	a)	2 MHz	b)	3 MHz		
	c)	6 MHz	d)	8 MHz.		
x)	The number of multiplexed bus in case of 8086 is					
	a)	16	b)	8		
	c)	20	d)	4.		
xi)	8086 exchanges data word with odd memory bank when					
	a)	BHE ⁻ = 0 and $A_0 = 0$	b)	BHE $^-$ = 0 and A_0 = 1		
	c)	BHE ⁻ = 1 and $A_0 = 0$	d)	BHE ⁻ = 1 and $A_0 = 1$.		
xii)	ntroduce/8088 μP.					
	a)	wait	b)	idle		
	c)	wait and remain idle	d)	all of these.		
5001		2				

CS/B.Tech (CSE/IT/PWE/EEE)/SEM-5/EI-502/2010-1

GROUP - B

(Short Answer Type Questions)

Answer any three of the following.

 $3 \times 5 = 15$

- 2. Write down the steps of execution of an instruction sequentially by 8085 microprocessor.
- 3. Write an A.L.P. in 8085 to find the total number of zeros and ones in a given string. Store the results in the memory location 9055 H onwards.
- 4. i) Explain why no. of output ports in I/O mapped I/O technique is restricted to 256 ports.
 - ii) Specify the 8085 signals that are used to enable an input and output port.
 - iii) If an output port can have the same 8 bit address, how does the 8085 differentiate between ports? 2 + 1 + 2
- 5. Draw the timing diagram of MOV A, M.
- 6. State the difference between architectures of 8086 and $8088 \, \mu P.$

GROUP - C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

- 7. a) What do you mean by DMA operation? Write down the steps of DMA operation. What is fixed priority mode and what is rotating priority mode? 2 + 3 + 3
 - b) If the clock frequency is 5 MHz, how much time is required to execute the instruction MVI B, 08 (7T state)? Draw the timing diagram. 3 + 4

5001 3 [Turn over

CS/B.Tech (CSE/IT/PWE/EEE)/SEM-5/EI-502/2010-1

- 8. a) What is two key lockout and N-key rollover mode of 8279 ? How an A/D converter can be interfaced with a 8085 microprocessor ? 3+5
 - b) Write an assembly language program for BCD to binary conversion.
 - c) What are the functions of RESET, HOLD, INTERRUPT and READY pins?
- 9. a) Describe the different addressing modes of 8086 microprocessor. 5
 - b) Draw the architecture of 8086. What are the functions performed by BIU and EU of 8086 microprocessor. 7
 - c) How is pipelining achieved in 8086 microprocessor? 3
- 10. a) What do you mean by interrupt driven system? Arrange the interrupt according to their priority. Define maskable and non-maskable interrupts. What is interrupt call location? 2 + 2 + 2 + 1
 - b) Why is decoder circuit needed? Using 74LS 138 draw and explain the interfacing of memory and IO devices.

1 + 7

- 11. Write short notes on any three of the following:
- 3×5
- a) Addressing modes of 8051 microcontroller
- b) 8259 Interrupt controller
- c) BSR mode of 8255
- d) MIN/MAX mode operation of 8086 microprocessor
- e) Hardware interrupt of 8085 CPU.

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