Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH (EIE)(N)/SEM-3/EC(EI)-301/2012-13

2012

DIGITAL ELECTRONIC CIRCUITS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) The octal equivalent of the binary number 11010111 is

   a) 656 b) 327

   c) 653 d) D7.

   ii) The minimum number of NAND gates required to implement the Boolean function $A + AB' + AB'C$ is equal to

   a) zero b) 1

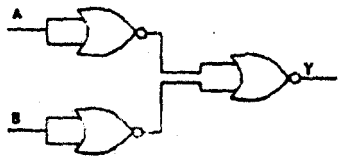
   c) 4 d) 7.

   iii) The fastest logic gate family is

   a) CMOS b) ECL

   c) TTL d) RTL.

iv) Identify the operation of the following logic gate circuit :



a) OR gate b) AND gate

c) NOT gate d) none of these.

v) Which one is used in EPROM eraser ?

a) Laser light b) UV ray

c) LED light d) Sunrays.

vi) Gray code of 1011 (binary) =

a) 0101 b) 1101

c) 1110 d) none of these.

vii) A ring counter consists of 5 flip-flops will have

a) 5 states b) 10 states

c) 32 states d) none of these.

viii) The flip-flop, which is free from race amount problem is

a) R-S flip-flop

b) Master-slave JK flip-flop

c) J-K flip-flop

d) none of these.

ix) The minterms for $A + BC$ are

a) $\sum m(2,3,4,5,7)$ b) $\sum m(3,4,5,6,7)$

c) $\sum m(1,3,4,5,6,7)$ d) none of these.

x) A 10 Mhz signal is applied to a MOD-5 counter followed by a MOD-8 counter then the O/P frequency will be

a) 10 kHz b) 2·5 kHz

c) 5 kHz d) 250 kHz.

xi) Calculator keyboard is an example of
a) decoder b) encoder
c) multiplexer d) demultiplexer.

xii) A single bit memory device is
a) ROM b) RAM
c) F-F d) PROM.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following $3 \times 5 = 15$

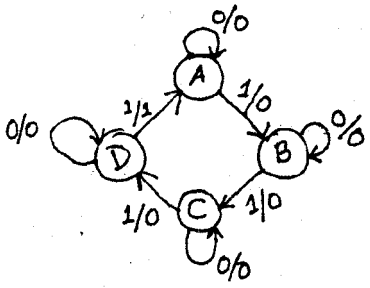
2. Perform the arithmetic operation : $(-22)_{\text{decimal}} + (13)_{\text{decimal}} + (-15)_{\text{decimal}}$ using 2's complement binary form.
3. Minimize the following expression is SOP form using Quine McClusky method :
$F(A,B,C,D) = \sum m(1,2,3,8,9,10,11,14) + \sum d(7,15)$
4. Explain the race around condition. Draw the Master/Slave JK flip-flop using all NAND gates. 2 + 3
5. Realize the 3-input majority function using NAND gates only.
6. Realize JK flip-flop using *T* flip-flop and other SSI gates.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Design a clocked synchronous sequential network whose state diagram is given below :



b) Design a mod-6 ripple counter using PRESET lines of JK flip-flops. 8 + 7

8. a) Implement the following Boolean expression using Decoder and extra gate :

$F(A,B,C,D) = \sum(1,2,5,7,8,10,12,13)$.

b) Implement a full adder circuit using minimum number of NOR gates only.

c) An 8 : 1 MUX has inputs *A, B, C* connected to select line S_2, S_1, S_0 respectively. The data inputs I_0 to I_7 are connected as $I_1 = I_2 = I_7 = 0$, $I_3 = I_5 = 1$, $I_0 = I_4 = D$, $I_6 = D'$. Determine the Boolean expression of the MUX output. 5 + 5 + 5

9. a) Construct a 4-bit register with parallel load and shift right controls.

b) Describe the basic principles of Successive Approximation Method for A/D converter. 10 + 5

10. a) Design MOD-8 synchronous DOWN-counter using the D-flip-flops and other required logic gates.

b) Calculate the propagation delay for a 4-bit synchronous UP-counter when JK flip-flops are connected in series connection and parallel connection. Given propagation delay $t_p(FF)$ equals to 30 nsec and the propagation delay of the gates used in the circuit are 20 nsec (assumed to be equal for all gates). 10 + 5

11. Write short notes on any *three* of the following : 3 × 5

a) Tri-state gates in TTL family

b) Data Lock-out in a counter

c) Magnitude comparator

d) Mealy machine and Moore machine

e) Parity generator.

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