Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH(ECE)/SEM-6 /EC-604/2012

2012

VLSI CIRCUITS AND SYSTEMS

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) The noise margin for high signal levels $\left(NM_H \right)$ is

   a) $V_{IL} - V_{OL}$ b) $V_{OH} - V_{IH}$

   c) $V_{OH} - V_{OL}$ d) none of these.

   ii) The switching threshold voltage of CMOS inverter is obtained when

   a) $V_{in} = V_{out}$ b) $V_{T,n} = -V_{T,p}$

   c) $V_{in} = 2V_{out}$ d) none of these.

   iii) In CMOS static logic design, total number of transistors required for the Boolean function $F = A + (B + CD)$ is

   a) 10 b) 8

   c) 5 d) none of these.

iv) The sum-of-product expression of a Boolean function can be realized by
   a) AOI gates b) OAI gates
   c) both (a) and (b) d) none of these.

v) Dynamic logic circuit is
   a) faster than static design
   b) slower than static design
   c) bigger than static design
   d) none of these.

vi) VHDL is used for
   a) Timing analysis b) layout diagram
   c) logic design d) RTL coding.

vii) Active resistor is used for
   a) less fabrication area
   b) load resistor
   c) constant current source
   d) all of these.

viii) For depletion type NMOS
   a) the threshold voltage is + v*e*
   b) the threshold voltage is – v*e*
   c) the threshold voltage is – v*e* and + v*e*
   d) all of these.

ix) BiCMOS means
   a) two BJT circuits
   b) two CMOS circuits
   c) both BJT and CMOS circuits
   d) none of these.

x) For a symmetrical CMOS inverter the relation between aspect ratio of NMOS and PMOS is
   a) $(W/L)p = (W/L)n$ b) $(W/L)p = 2 \cdot 5\ (W/L)n$
   c) $(W/L)n = 2 \cdot 5\ (W/L)p$ d) $(W/L)p = 5\ (W/L)n$.

xi) Pseudo *n*MOS logic provides which of the following advantages ?

a) Static power dissipation is less compared to CMOS logic

b) It is faster compared to other logics

c) It requires less no. of transistors compared to CMOS logic

d) It is more noise immune.

xii) Configurable logic blocks are used in

a) gate array design style

b) standard cell based design

c) field programmable gate array layout

d) full custom design.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. What is current source and current sink in VLSI circuit ? Design a current sink using $V_{DD} = -V_{SS} = 2 \cdot 5\text{V}$ to sink a current of $10\mu\text{A}$. Estimate the minimum voltage across the current source and the output resistance. Assume $K_P = 50\mu\text{A/V}^2$, $L = 5\mu\text{m}$, $V_{THN} = 0 \cdot 83\text{V}$, $\lambda = 0 \cdot 06$. 2 + 3

3. Draw and explain the operation of MOS Switched Capacitor Integrator and also find the expression for output voltage.

4. Compare between static logic and dynamic logic. Explain the operation of Domino-logic to design any CMOS circuit. 2 + 3

5. What is Transmission Gate (TG) ? Explain the operation of Edge Triggered *D* Flip-Flop using CMOS TG gates. Implement the expression using CMOS TG logic. $Z = XY' + X'Y$. (X' = complement of X) 1 + 2 + 2

6. Draw the circuit of a CMOS full adder circuit and explain its operation.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Explain the fabrication process steps for an NMOS transistor with necessary diagrams.
   b) Write down the difference between twin-tub process and *P*-well process.
   c) Draw the layout of the following :
   (i) $F = AB + CD$ (ii) $F = A + BC$ 7 + 3 + 5

8. a) Explain how CMOS can be used for inverter logic. Draw the voltage transfer characteristics of CMOS inverter and clearly define operating regions of NMOS and PMOS.
   b) Show that for a symmetric CMOS inverter the two noise margins are same and are equal to VIL. Also show that for ideal CMOS inverter $(W / L)p = 2 \cdot 5\ (W / L)n$.
   3 + 3 + 3 + 3 + 3

9. a) What is CMRR ?
   b) Explain with a circuit diagram, operation of a differential amplifier.
   c) Explain briefly different stages of an OP-AMP with the help of a block diagram. 2 + 7 + 6

10. a) What do you mean by current sink and current source ?
   b) Explain how combination of switches and capacitors can be used to emulate a resistor.
   c) What is phase locked loop ? Explain its operation. Mention two uses of phase locked loop.
   2 + 5 + 2 + 5 + 1

11. Write short notes on any *three* of the following : 3 × 5
   a) Constant voltage scaling
   b) CMOS NORA logic
   c) ASIC
   d) DCVSL and pseudo *n*-MOS inverter.