



Name :

Roll No. :

Invigilator's Signature :

CS/B.Tech(CSE-OLD)/SEM-4/CS-403/2012

2012

ADVANCE COMPUTER ARCHITECTURE

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following :

10 × 1 = 10

i) Higher order memory interleaving called

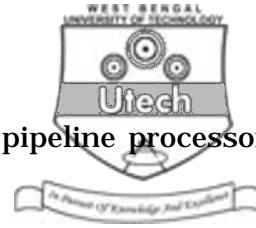
- a) S-access b) C-access
c) S-access & C-access d) none of these.

ii) For two successive instruction I & J WAW hazard occur, if

- a) $R(I) \cap D(J) \neq \Phi$ b) $D(I) \cap R(J) \neq \Phi$
c) $R(I) \cap R(J) \neq \Phi$ d) none of these.

4401 (O)

[Turn over



iii) The instruction execution flow in the pipeline processor is represented by

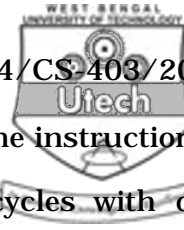
- a) Reservation table
- b) Data flow diagram
- c) Flow chart
- d) Space time diagram.

iv) Associative memory is

- a) very cheap memory
- b) pointer addressable memory
- c) content addressable memory
- d) slow memory.

v) The locality of reference property justifies the use of

- a) Secondary memory b) Main memory
- c) Cache memory d) Register.



- vi) A computer uses words of size 32-bit. The instruction
- a) must always be fetched in two cycles with one byte in each cycle
 - b) must always be fetched in one cycle with two bytes in each cycle
 - c) may or may not be of one byte length
 - d) none of these.
- vii) The handshaking technique
- a) is used in synchronous data transfer
 - b) is used in asynchronous data transfer and uses two control signals in opposite direction
 - c) works even if one communicating device gets faulty in the midway of data transfer
 - d) is not much flexible.
- viii) Bus arbitration means
- a) master – slave synchronous or asynchronous data transfer
 - b) a process by which a bus controller controls the bus most of the time
 - c) a process by which the current bus master accessed and then leaves the control of the bus and passes it to another bus requesting device
 - d) a process to give bus accesses among many devices by polling the requesting device.



ix) Overlapped register windows are used to speedup procedure call and return in

- a) RISC architecture b) CISC architecture
- c) both (a) and (b) d) none of these.

x) The number of cycle require to get the first output of n tasks in k stage pipeline

- a) k b) n
- c) $k + n - 1$ d) none of these.

GROUP - B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Describe the different type architecture-superscalar, superpipeline and superscalar superpipelined.
3. Define the term — "locality of reference", "Degree of memory interleaving".
4. Using a block diagram explain the operation of an SIMD array processor.
5. What is bus arbitration ? What are different methods of bus arbitration ? Explain them.
6. Compare between centralized and distributed share memory architecture. Which is the best architecture among them ?



GROUP - C

(Long Answer Type Questions)

Answer any *three* of the following.

$3 \times 15 = 45$

7. a) Write down the forbidden & permission latency and collision vector.
- b) Write an algorithm to draw the state diagram of a pipeline.

Consider the following reservation table :

	1	2	3	4	5
S1	X			X	
S2		X			X
S3			X		

- c) According to this reservation table write down forbidden latency and initial collision vector.

Draw the state diagram for scheduling the pipelining.

$3 + 5 + 7$

8. a) What is cache memory ? Define global miss & local miss with an suitable example.
- b) Describe different technique to reduce Miss Penalty.
- c) Describe different technique to reduce Miss Rate.

CS/B.Tech(CSE-OLD)/SEM-4/CS-403/2012



9. Write short notes on any *three* of the following : 3×5

- a) Power PC
- b) Memory to memory vector architecture
- c) Array processor
- d) Memory inclusion
- e) Memory interleaving.

10. a) What do you mean by multiprocessor system ? What are the similarities and dissimilarities between the multiprocessor system and multiple computer system ?

b) What are the different architectural models for multiprocessors ? Explain each of them with example.

c) Distinguish between loosely coupled and tightly coupled multiprocessor architectures. Which architecture is better and why ?

$5 + 5 + 5$



11. a) Write short note on : vectorizing compilers.
- b) What are strip mining and vector stride, in respect of vector processors ?
- c) Both vector processors and array processors are specialized to operate on vectors. What are the main differences between them ?

5 + 5 + 5

=====