VLSI CIRCUITS & SYSTEMS (SEMESTER - 6)

CS/B.Tech (ECE)/SEM-6/EC-604/09

1. ....
Signature of Invigilator

2. ....
Signature of the Officer-in-Charge

Reg. No. | | | | | | | | | | | | | | | |

Roll No. of the Candidate | | | | | | | | | | | | | | | |

CS/B.Tech (ECE)/SEM-6/EC-604/09

ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2009

VLSI CIRCUITS & SYSTEMS (SEMESTER - 6)

Time : 3 Hours] [Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. This Booklet is a Question-cum-Answer Booklet. The Booklet consists of **32 pages**. The questions of this concerned subject commence from Page No. 3.
2. a) In **Group – A**, Questions are of Multiple Choice type. You have to write the correct choice in the box provided **against each question**.
   b) For **Groups – B** & **C** you have to answer the questions in the space provided marked 'Answer Sheet'. Questions of **Group – B** are Short answer type. Questions of **Group – C** are Long answer type. Write on both sides of the paper.
3. **Fill in your Roll No. in the box** provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. **Use of Mobile Phone and Programmable Calculator is totally prohibited in the examination hall.**
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, **which will lead to disqualification**.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

FOR OFFICE USE / EVALUATION ONLY

Marks Obtained

	Group – A										Group – B			Group – C				
Question Number																	***Total Marks***	***Examiner's Signature***
Marks Obtained																		

....
Head-Examiner/Co-Ordinator/Scrutineer

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GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) What is another name of D. Gzaski chart ?

a) Y Chart b) Smith Chart

c) Z Chart d) Log Chart. ☐

ii) Channel-less Gate array is a sub-type of

a) FPGA b) PLD

c) ASIC d) None of these. ☐

iii) Minimum number of transistors required to implement $F = ABC + DE + F$ is

a) 5 b) 6

c) 7 d) none of these. ☐

iv) The output of physical design is

a) Circuit diagram b) Mask

c) Lay-out d) RTL. ☐

v) DRAM is widely used because

a) refreshing operation is not needed

b) of low cost and high density

c) of low power consumption

d) of high speed.

vi) Data refresh operation is needed in

a) DRAM b) Flash

c) SRAM d) FRAM.

vii) For a symmetrical CMOS inverter the relation between aspect ratio of NMOS and PMOS is

a) $(W/L)p = (W/L)n$ b) $(W/L)p = 2{\cdot}5\,(W/L)n$

c) $(W/L)n = 2{\cdot}5\,(W/L)p$ d) $(W/L)n = 5\,(W/L)p$.

viii) Frequency compensation of Op-Amp using MOS technology is done by

a) decreasing the number of stages

b) minimizing the number of poles in single path

c) achieving low voltage gain

d) all of these.

ix) A BJP is considered as Open Switch (or OFF) when

a) both junctions are forward biased

b) EBJ is forward and CBJ is reverse

c) both junctions are reverse biased

d) EBJ is reverse and CBJ is forward.

x) Hierarchical decomposition of a large system in VLSI design is called

a) modularity b) regularity

c) locality d) none of these.

xi) Which of the following is not a part of FPGA ?

a) CLB b) I/O Block

c) Vertical routing channel d) FSM.

xii) The quantisation noise of a DAC having *N* number of bits is

a) directly proportional to 2^N

b) directly proportional to 2^{N-1}

c) inversely proportional to 2^N

d) inversely proportional to 2^{N-1}.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 ∞ 5 = 15

2. What is MOSFET scaling ? What is the need of scaling ? Compare various types of scaling. 1 + 2 + 2

3. Explain the following phenomenon in an MOS structure : 3 + 2

a) Channel length modulation

b) Pinch-off.

4. a) What do you mean by VHDL ? Why is it required in VLSI circuit simulation ? 1 + 1

b) Derive saturation current in an *n*-MOS transistor. 3

5. a) What is current mirror ?

b) With circuit diagram explain the operation of an MOS current mirror. 1 + 4

6. Draw the layout and schematic diagram of a 2-input static CMOS NOR Gate and identify the corresponding components in the two drawings. 1 + 1 + 3

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 ∞ 15 = 45

7. a) What is *Y* cycle in VLSI ? Explain VLSI design cycle in detail. 2 + 6

b) What do you mean by standard cell design ? How does it differ from gate arrray design ? 2 + 3

c) What is top-down and bottom-up design in VLSI ? 2

8. a) Design a static CMOS circuit to implement the Boolean function :

$F = AB + AB^{/} C + A^{/} C^{/}$. 7

b) Draw the CMOS half adder circuit and explain its operation. 5

c) Explain why NMOS is preferred for pull-down network and PMOS is preferred for pull-up network. 3

9. a) Design the following circuit using PAL, PLA and ROM :

$Y1 = AB + A^{/} C + ABC^{/}$, $Y2 = AB^{/} C$, $Y3 = BC + ABC^{/}$ 6

b) Design a master-slave *D* flip-flop. Describe its operation. 3

c) Describe the read and write operation of a six transistor SRAM cell. 6

10. a) Explain lambda (λ) design rules in VLSI. 4

b) Compare the advantage of lambda design rule over micron rule. 3

c) What is CMOS twin tub process ? Explain. 3

d) Find out an expression for dynamic power dissipation in CMOS. 3

e) What are the properties of VLSI interconnects ? 2

11. a) Discuss the merits and demerits of Flash ADC. Find resolution for a DAC if the output voltage is desired to change in 1mV increments while using a reference voltage of 5V ? 2 + 3

b) How can a MOS device be used as a voltage reference ? 5

c) What do you mean by hierarchy, regularity, modularity & locality of any ASIC design. 5

END