ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2007

DIGITAL ELECTRONICS AND INTEGRATED CIRCUIT

SEMESTER – 4

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) Excess-3 coded representation of $(19)_{10}$ is

a) 10011 b) 00011001

c) 01001100 d) 11000100.

ii) The decimal equivalent of the binary number $(101111.1101)_2$ is

a) $(46.8125)_{10}$ b) $(47.8125)_{10}$

c) $(47.8155)_{10}$ d) $(47.8145)_{10}$.

iii) A 10 MHz signal is applied to a MOD 5 counter followed by a MOD 8 counter. The output frequency will be

a) 10 kHz b) 2·5 kHz

c) 5 kHz d) 25 kHz.

iv) A 4-stage ripple counter counts upto

a) 12 b) 15

c) 11 d) 4.

v) Which family has the better noise margin ?

a) ECL b) DTL

c) MOS d) TTL.

vi) On a Karnaugh map, grouping of OS produces

a) a PVS expression b) an SOP expression

c) a don't care condition d) none of these.

vii) The number of flip-flops required for a MOD-10 ring counter is

a) 10 b) 5

c) 4 d) 12.

viii) Circuit hazards are present in

a) combination circuits only

b) combination and sequential circuit only

c) sequential circuits only

d) none of these. ☐

ix) When two *n*-bit binary numbers are added, the sum will contain at the most

a) *n* bits b) $n + 1$ bits

c) $n + 2$ bits d) $n + n$ bits. ☐

x) In a binary *R-Z-R* ladder *DAC*, the input resistance of each input is

a) *R* b) $2R$

c) $3R$ d) $4R$. ☐

xi) The number of control lines for a 8 to 1 multiplexer is

a) 2 b) 3

c) 4 d) 5. ☐

xii) The simplification of the Boolean expression $\left(A + \overline{A} + B + C \right)$ is

a) 0 b) 1

c) *A* d) *BC*. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Explain race around condition of J-K flip-flop. Show how this condition can be avoided.

3. Simplify the Boolean function using *K*-map :

$$F(A, B, C, D) = \Sigma m(0, 1, 2, 8, 10, 11, 14, 15).$$

4. Design a full subtractor using (i) NAND gates, (ii) NOR gates.

5. Simplify algebraically, $Y = AB + A\overline{B}\left(\overline{\overline{A}\ \overline{C}} \right)$.

6. Define the following terms as applied to digital circuits :

a) Set-up time

b) Hold time

c) Maximum clock frequency

d) Fin in

e) Power dissipation.

GROUP – C

(Long Answer Type Questions)

Answer any *three* questions. $3 \times 15 = 45$

7. a) What is the difference between a latch and a edge triggered flip-flop ?

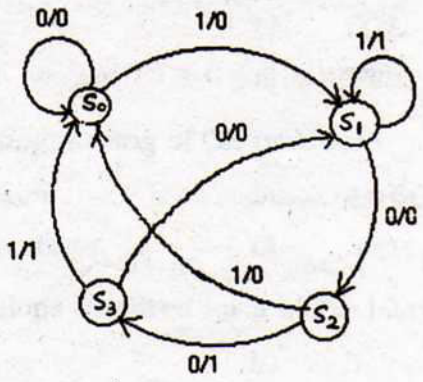
b) Design a clocked R-S fip-flop using NAND gates. Explain its principle of operation.

c) Design a MOD 10 synchronous binary UP conter using J-K flip-flop and necessary logic gates. 3 + 8 + 4

8. a) Describe the operation of successive approximation type ADC. How many clock pulses are required in worst case for each conversion cycle of an 8-bit SAR type ADC ?

b) Draw a neat diagram of a R-2R ladder type DAC.

c) Design a sequential circuit that implements the following state diagram. Use all *D*-type flip-flops for the design. 5 + 3 + 7



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