



ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER - 2007

DIGITAL ELECTRONICS & LOGIC DESIGN**SEMESTER - 3**

Time : 3 Hours]

[Full Marks : 70

GROUP - A**(Multiple Choice Type Questions)**

1. Choose the correct alternatives for any ten of the following :

10 × 1 = 10

i) Convert $(444.456)_{10}$ into its octal equivalent

a) 673.5136

b) 674.35136

c) 674.735

d) none of these.

ii) $(A + \bar{B} + \bar{A}B)C =$

a) 1

b) 0

c) C

d) \bar{C} .
iii) How many 1's are present in the binary representation of decimal number $(3 \times 512 + 7 \times 64 + 5 \times 8 + 3)$?

a) 8

b) 9

c) 10

d) 11.

iv) An example of reflected code is

a) BCD

b) ASCII

c) GRAY

d) Hamming.

- 4001

-

$$3 \times 5 = 15$$

<http://www.makaut.com>



3. Implement the following function using all 4 : 1 multiplexers

$$F = \sum m (0, 2, 3, 6, 8, 9, 12, 14)$$

4. Implement a full-adder circuit using a 3 to 8 decoder with all active-low outputs and one additional logic gate if required.

5. Define the following terms in relation with logic families :

5 × 1

- propagation delay
- fan-in
- fan-out
- power dissipation
- floating inputs.

6. Find out the 7's complement of $(- 756)_8$.

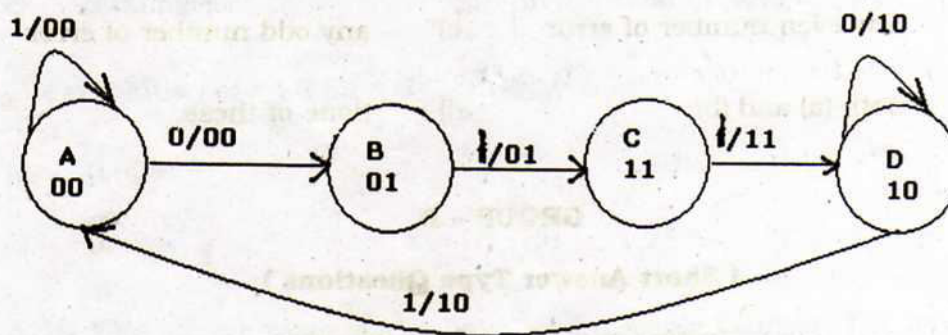
GROUP - C

(Long Answer Type Questions)

Answer any *three* questions.

3 × 15 = 45

- Design an asynchronous 4-bit up-down counter and it will count up when a signal line $M = 0$ and count down when a signal line $M = 1$.
- Design a circuit that will function as prescribed by the state diagram shown below. Use S-R flip-flops for implementation.



State Diagram

6 + 9



8. a) With the help of necessary circuit diagram explain the operation dual slope ADC.
- b) A 4-bit binary ladder D/A converter with $R = 10 \text{ K}\Omega$ uses a reference of 5 V. Find
- the ideal scale factor in V/step
 - the analog o/p corresponding to the binary i/p 0110
 - resolution in %
 - full scale o/p
 - the maximum deviation in volts from the best straight line in order to meet standard linearity. $5 + 5 \times 2 = 15$
9. a) Design a BCD to 7-segment common anode display code converter using PROM type PLD.
- b) Implement the following functions using a $3 \times 4 \times 2$ PLA :
- $$F_1(A, B, C) = \sum(3, 5, 6, 7)$$
- $$F_2(A, B, C) = \sum(0, 2, 4, 7). \quad 7 + 8$$
10. a) Simplify the following function by means of tabulation method :
- $$F = \sum m(0, 1, 4, 7, 9, 11, 13, 15) + \sum d(3, 5).$$
- b) Simplify the following function using K-map.
- $F = \prod m(0, 1, 3, 8, 10, 15) \cdot \prod d(11, 13, 14)$
 - $F = \sum m(0, 4, 7, 9, 13, 15) + \sum d(10, 14) \quad 5 + 5 + 5$
11. Write short notes on any three of the following : 3×5
- EPROM
 - PLD
 - A/D converter
 - Johnson counter.

END