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Paper Code : PCC-CS402 Computer Architecture

UPID : 004442

Time Allotted : 3 Hours *Full Marks :70*

The Figures in the margin indicate full marks.
Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer any ten of the following : [1 x 10 = 10]

(I) _____ is a processor architecture that executes multiple instructions in a single clock cycle by using multiple functional units.

(II) A _____ computer is a group of interconnected computers that work together to perform a task.

(III) _____ architecture is a type of parallel architecture that emphasizes data flow and emphasizes communication between nodes rather than a shared memory space.

(IV) _____ is a technique for increasing instruction-level parallelism by simultaneously executing multiple instructions.

(V) The primary goal of exception handling is to _____.

(VI) The _____ policy in virtual memory is used to decide which page to remove from memory when a new page needs to be loaded into the memory.

(VII) What is a superpipelined processor?

(VIII) What is synchronization in a centralized shared-memory architecture?

(IX) What is exception handling in computer architecture?

(X) What are memory replacement policies?

(XI) What is a memory replacement policy?

(XII) What is a VLIW processor?

Group-B (Short Answer Type Question)

Answer any three of the following : [5 x 3 = 15]

2. What is a cache memory, and how is it different from main memory? [5]
3. What are some of the design trade-offs involved in implementing a superscalar processor architecture? [5]
4. What are data hazards in computer architecture? How can they be resolved? [5]
5. What is a cache miss, and what are the causes of cache misses in a computer system? [5]
6. What is the role of the memory management unit (MMU) in virtual memory management? [5]

Group-C (Long Answer Type Question)

Answer any three of the following : [15 x 3 = 45]

7. Explain the concept of pipeline hazards in computer architecture. How can they be avoided or minimized? [15]
8. (a) Describe the concept of virtual memory? [8]
   (b) Explain how it is implemented in modern computer systems. [7]
9. Explain the concept of cache coherence miss penalty, and discuss the techniques used to reduce it. [15]
10. Compare and contrast superscalar and VLIW processor architectures in terms of their performance, complexity, and design challenges. [15]
11. A system has a 64-bit virtual address space and a 4 KB page size. The page table is stored in main memory, which has a memory access time of 100 ns. The TLB has a hit rate of 90%, and a TLB miss takes 500 ns to service. What is the effective memory access time? [15]

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