Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH/CSE/SEM-8/CS-801D/2013

2013
VLSI DESIGN

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct answers for the following : 10 × 1 = 10

i) NMOS Transistor in linear region can be modelled as

a) Resistance

b) Current Source

c) Open Circuit

d) None of these.

ii) With decrease of Vdd, the delay of an CMOS inverter

a) increases b) decreases

c) remains same d) none of these.

iii) Minimum number of transistors in CMOS logic Y = ABC + DE is

a) 12 b) 6

c) 14 d) 10.

iv) The output of Physical Design is

a) Logical Netlist b) Circuit Diagram

c) Layout d) RTL.

v) Stick Diagram represents

a) Logic b) Circuit

c) Layout d) Architecture.

vi) Value of "Lambda" in 0·5 um Technology is

a) 0·5 um b) 1 um

c) 0·25 um d) 2 um.

vii) BDD is used in

a) High Level Synthesis b) Logic Synthesis

c) Layout Floor Plan d) Routing.

viii) Most popular interconnect material is

a) Gold b) Silver

c) Aluminium d) Silicon dioxide.

ix) For a standard Cell Layout

a) height is fixed

b) width is fixed

c) both height and width are fixed

d) none of these.

x) Memory Design is normally done using

a) Full Custom

b) Semi-custom using standard cells

c) FPGA

d) None of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) Draw circuit diagram of a D-Latch using CMOS Transmission Gate (TG). 3

b) Draw circuit diagram of a Negative Edge Triggered D-Flip-flop using D-Latch. 2

3. a) Draw circuit diagram of 2-input XOR gate using CMOS Logic. 2

b) Draw circuit diagram of 2-input XOR gate using CMOS Transmission Gate (TG). 3

4. Draw layout of CMOS inverter using Standard Cell Layout Topology and show all the layers.

5. Write VHDL code of Behavioural Modelling of a D-Flip-flop.

6. Draw flow diagram of High Level Synthesis.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Draw flow diagram of Logic synthesis. 5

   b) Draw BDD Diagram for function

   $f = abc + ab^{l}c + a^{l}bc^{l} + a^{l}b^{l}c^{l}$ using

   ordering of $a \leq b \leq c$. 5

   c) Create ROBDD Diagram of same function and corresponding optimized Boolean expression. 5

8. a) What is the difference between "Micron based Design Rule" and "Lambda based Design Rule" ? 2

b) What are the differences between Full Custom Design and Standard-Cell based Semi custom Design ? 3

c) Explain Euler path solution of a CMOS gate which represents function $f = (\overline{A + B + CD})$. 5

d) Draw Stick Diagram of the same CMOS gate based on Euler path solution. 5

9. a) Draw Flow Diagram of Physical Layout Automation 3

b) For the following Channel Routing Problem, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG) : 6

Terminal connection is as follows :

11122563040 ..... Upper Boundary

25055330604 ..... Lower Boundary

0 means no connection.

Assume *HV* Layer (*V* = Metal 1, *H* = Metal 2)

c) Provide Optimum Channel Routing Solution for above case using Left Edge Algorithm. 6

10. a) For Floor planning problem, what are inputs, outputs and objective (cost) function ? 5

b) Write problem formulation of Global Routing using Steiner Tree. 5

c) Explain Maze Routing. 5

11. Write short notes on any *three* of the following : 3 × 5

a) Various Power Dissipations in CMOS digital gate

b) *n*-well CMOS Fabrication Process

c) VLSI interconnect

d) FPGA

e) Stuck at fault modelling for *si* testing.