ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER – 2008

EDA FOR VLSI DESIGN

SEMESTER - 7

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) Among the following which one has the greatest gate integration capacity ?

a) FPGA b) CPLD

c) PLD d) ASIC. ☐

ii) The fastest logic family is

a) TTL b) CMOS

c) ECL d) IIL. ☐

iii) The logic family which consumes least amount of power is

a) DTL b) RCTL

c) CMOS d) none of these. ☐

iv) FPGA is a

a) full-custom ASIC b) semi-custom ASIC

c) programmable ASIC d) none of these. ☐

v) Min-cut algorithm is a

a) placement algorithm b) routing algorithm

c) testing algorithm d) floor planning algorithm. ☐

vi) VLSI design flow is a

a) cyclic process only b) parallel process

c) sequential and cyclic process d) none of these. ☐

vii) VHDL is a

a) multi-threaded program b) a programming language like C
c) single user program d) sequential program. ☐

viii) The suitable interconnect among the following is

a) Aluminium b) Gold
c) Copper d) Silver. ☐

ix) Minimum TTL gates required to design XOR gate is

a) Six b) Eight
c) Twelve d) Ten. ☐

x) PLA and PAL are know as

a) CPLD b) FPLD
c) SPLD d) GPLD. ☐

xi) Bird's Beak phenomenon occurs in

a) Diffusion b) Ion implantation
c) Oxidation d) Lithography. ☐

xii) DRAM is widely used because

a) refreshing operation is not needed
b) of low cost and high density
c) of low power consumption
d) of high speed. ☐

xiii) Scaling is done for

a) improving the switching speed
b) decreasing the power dissipation
c) reducing chip size
d) all of these. ☐

xiv) LUT is used in

a) CPLD b) SPLD
c) ASIC d) FPGA. ☐

xv) The output of physical design is

a) Circuit b) Layout
c) Logical model d) RTL Schematic. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) What is Layout ? 1

   b) Draw the Layout of CMOS Inverter. 2

   c) What is FOX is IC fabrication ? 2

3. Implement a Full Adder in VHDL code using Mixed Style of Modelling. 5

4. a) What are μ-based and λ-based designs in VLSI fabrication ? In which case full capability of the Fab.Lab. can be utilised ? 2 +1

   b) For 0·5 μm process what is the value of λ ? According to the design rule, what will be the minimum widths of diffused region and metal interconnect lines ? 1 + 1

5. Draw the physical mask layout design for the following Boolean functions :

   a) $F = (BA + DC)$

   b) $F = (B + \bar{C}) A.$ 5

6. a) What is cell Library ? 2

   b) What is cell technology ? 1

   c) What is Full custom design ? 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Write down the difference between CPLD and FPGA. 5

   b) Write a program on 4-bit full adder using FA-1 bit. 10

8. a) Explain the difference between Entity and architecture in a VHDL design. 4

   b) What are the different styles of describing the Architecture in VHDL ? Explain each with an example. 3 × 3

   c) Is mixed style description allowed in VHDL ? 2

9. a) Give a logic circuit example in which "Stuck-at-1" fault and "Stuck-at-0" fault are indistinguishable. 5

   b) Write down VHDL code for 4 to 1 mux and obtain the code for 16 to 1 mux using this 4 to 1 mux module. 10

10. a) Explain the *n*-well CMOS fabrication process with necessary diagram. 10

    b) Draw the CMOS NAND gate and CMOS NOR gate using layout technique. 5

11. Write short notes on any *three* of the following : $3 \times 5 = 15$

    a) Floor Planning

    b) Application specific integrated circuits

    c) Test generation

    d) Analog design automation tools

    e) Optimazation of Combinational circuits.

END