Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH/ECE/SEM-7/EC-702/2012-13

2012

EDA FOR VLSI DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) The HDL used for industrial purpose is

   a) VHDL b) PSPICE

   c) VERILOG d) MATLAB.

   ii) Which of the following is not included in EDA design flow ?

   a) ASIC design flow

   b) Simulation

   c) Synthesis

   d) Testing and verification.

iii) CAD tools for VLSI design are required to

a) reduce the time to market

b) increase the yield of chip

c) both (a) and (b)

d) none of these.

iv) Mead and Conway proposed the

a) Stick diagram

b) Lambda Layout diagram

c) Micron Layout diagram

d) none of these.

v) LUT is used in

a) CPLD b) ASIC

c) FPGA d) SPLD.

vi) Scan-design technique is used to achieve

a) controllability b) observability

c) both (a) and (b) d) none of these.

vii) Synthesis translates from

a) physical description to behavioural description

b) physical description to structural description

c) behavioural description to structural description

d) behavioural description to physical description.

viii) Which are the simple PLDS ?

a) CPLD b) FPGA

c) CBIC d) PLA.

ix) BDD is useful for

a) high level synthesis

b) low level synthesis

c) testing

d) timing analysis.

x) Kernighan-Lin algorithm is used for

a) partitioning b) placement

c) floor planning d) routing.

xi) Min-cut algorithm is a

a) placement algorithm

b) routing algorithm

c) testing algorithm

d) floor planning algorithm.

xii) The width of PMOS is three times larger than that of NMOS because

a) channel length of NMOS is three times larger than that of PMOS

b) mobility of NMOS is three times greater than that of PMOS

c) oxide capacitance of PMOS is three times smaller than that of NMOS

d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following $3 \times 5 = 15$

2. What do you mean by fault and error ? Write down the differences between verification and testing. 2 + 3

3. What is ASIC ? Describe the design flow of an ASIC design. 1 + 4

4. a) Name the various languages to describe hardware.

   b) Write a VHDL code for JK flip-flop. 2 + 3

5. Describe Binary Decision diagram.

6. a) What are μ-based design and λ-based design in VLSI system ?

   b) Draw the stick diagram for 2-input NAND gate.

   2½ + 2½

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Draw the block diagram for CPLD and explain the functions of each block.

   b) What is logic synthesis ? What are the optimization techniques involved with this ? 10 + (2½ + 2½)

8. a) How Look Up Table (LUT) is used to program an FPGA ? Explain with an example.

   b) Explain the architecture of FPGA. Write the steps for programming an FPGA.

c) What is the difference between PAL and PLA ?

d) Implement the following function using PLA :

$F = A'B + AB' + ABC'$ 5 + (3 + 2) + 2 + 3

9. a) Explain the *n*-well CMOS fabrication process with necessary diagram.

b) Draw the CMOS NAND gate and CMOS NOR gate using layout technique. 9 + 6

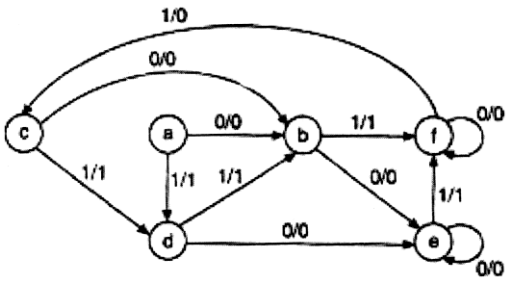
10. a) What are Controllability and Observability ? Discuss on Path-sensitization method of testing with example.

b) Explain D-Algorithm with proper example. (2 + 6) + 7

11. a) Describe the Sliceable, Non-Sliceable and Hierarchical Floor Planning using their corresponding trees with a suitable example.

b) Describe the Special Routing, Global Routing and Detail Routing.

c) Optimize the system described by the State Diagram given below :



5 + 5 + 5

12. Write short notes on any *three* of the following : 3×5

a) Reduced Ordered Binary Decision Diagrams (ROBDD)

b) ATPG

c) BIST

d) Data path and control synthesis

e) CAD tools.

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