Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH(ECE-NEW)/SEM-4/EC-402/2012

2012

DIGITAL ELECTRONICS AND INTEGRATED CIRCUITS

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) If $\sqrt{61} = 7$, the base of the number system is

a) 4 b) 8

c) 9 d) 6 .

ii) Which family has the better noise margin ?

a) ECL b) DTL

c) MOS d) TTL.

iii) The number of flip-flops required for a MOD-10 ring counter is

a) 4 b) 10

c) 5 d) none of these.

iv) A serial adder requires

a) one half adder b) two full adders

c) one full adder d) one multiplexer .

v) The simplification of the Boolean expression $(A + B + C + \overline{C})$ is

a) $A + B$ b) 0

c) AB d) 1

vi) 2's complement of 1's complement of the number 10110101 is

a) 01001010 b) 01001011

c) 10110101 d) 10111010.

vii) Gray code of binary 1101 is

a) 1001 b) 1101

c) 1011 d) 1111.

viii) 8421 is a

a) Non-weighted b) Weighted

c) Complementary code d) all of these .

ix) Which flip-flop acts as a buffer ?

a) D flip-flop b) T flip-flop

c) J-K flip-flop d) S-R flip-flop.

x) The characteristic equation of T flip-flop is

a) $Q_{n+1} = \overline{T}Q_n + T\overline{Q}_n$ b) $Q_{n+1} = TQ_n + \overline{T}\overline{Q}_n$

c) $Q_{n+1} = T\overline{Q}_n$ d) $Q_{n+1} = \overline{T}Q_n$.

xi) $F = (\overline{A}\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + A\overline{B}\,C + AB\overline{C} + ABC)$. Express it as POS .

a) $F = \prod (1, 2, 3)$ b) $F = \prod (1, 2, 3, 4, 5)$

c) $F = \prod (0, 5, 6)$ d) $F = \prod (0, 6, 7)$

xii) Latch is a memory cell of

a) 1 bit b) 2 bit

c) 3 bit d) none of these .

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Design 16 × 8 memory RAM chip using two 16 × 4 memory RAM chips.

3. Design a 5 × 32 decoder using 3 × 8 decoder and 2 × 4 decoder.

4. Perform the conversion from D flip-flop to S-R flip-flop.

5. Design a full subtractor using fewer

   (i) NAND gates

   (ii) NOR gates.

6. Explain race around condition of J-K flip-flop. Show how this condition can be avoided.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. Write the definitions of BCD code and Self complementing code with example. What is Gray code ? What is ASCII code ?

   Design a Gray code to binary converter using suitable logic gates.

   Convert the Gray Code 11011 to equivalent binary code.

   4 + 1 + 1 + 8 + 1

8. What is flip-flop ? What is the difference between combinational and sequential circuits ? What do you mean by the asynchronous inputs of a flip-flop ? What is edge trigger flip-flop and why is it required ? Convert S-R flip-flop to J-K R flip-flop. 2 + 2 + 2 + 3 + 6

9. What is ripple counter ? Design a presettable 4-Bit up asynchronous counter using J-K F-F. A binary ripple counter is required to count up to $(16383)_{10}$. How many F-Fs are required ? If the clock frequency is 8·192 MHz, what is the frequency at the output of the MSB ? 2 + 7 + 6

10. Construct a 5 × 32 decoder with four 3 × 8 Decoder and a 2 × 4 decoder. Show block diagram only. Describe the basic principle of successive approximation method for A/D converter.

    Implement the following Boolean equations using PLA device :

    a) $F1 = \sum m(0,5,9,15)$

    b) $F2 = \sum m(1,3,7,11,13)$

11. Write short notes on any *three* of the following : 3 × 5

    a) EPROM

    b) BCD to Excess-3 converter

    c) R-2R Ladder type DAC

    d) Even Parity Generator and Checker

    e) Universal gates

    f) Ring Counter.