MICROELECTRONICS TECHNOLOGY & CIRCUITS (SEMESTER - 6)

CS/B.TECH (ECE-O)/SEM-6/EC-604/09

1. ..... *Signature of Invigilator*

2. ..... *Signature of the Officer-in-Charge*

Reg. No. | | | | | | | | | | | | | | |

Roll No. of the Candidate | | | | | | | | | | | | | | |

CS/B.TECH (ECE-O)/SEM-6/EC-604/09

ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2009

MICROELECTRONICS TECHNOLOGY & CIRCUITS (SEMESTER - 6)

Time : 3 Hours] [Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. This Booklet is a Question-cum-Answer Booklet. The Booklet consists of **32 pages**. The questions of this concerned subject commence from Page No. 3.
2. a) In **Group – A**, Questions are of Multiple Choice type. You have to write the correct choice in the box provided **against each question**.
   b) For **Groups – B** & **C** you have to answer the questions in the space provided marked 'Answer Sheet'. Questions of **Group – B** are Short answer type. Questions of **Group – C** are Long answer type. Write on both sides of the paper.
3. **Fill in your Roll No. in the box** provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. **Use of Mobile Phone and Programmable Calculator is totally prohibited in the examination hall.**
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, **which will lead to disqualification**.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

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FOR OFFICE USE / EVALUATION ONLY

Marks Obtained

	Group – A										Group – B			Group – C			***Total Marks***	***Examiner's Signature***
Question Number																		
Marks Obtained																		

.....

Head-Examiner/Co-Ordinator/Scrutineer

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ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2009

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GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

i) ..... provides electrical isolation of multilevel metalization systems.

a) SiO_2 b) HCl

c) $SiCl_4$ d) none of these.

ii) In silicon bipolar technology, early voltage can be increased by

a) increasing the base width and / or doping concentration

b) decreasing the base width and / or doping concentration

c) increasing the collector width and / or doping concentration

d) decreasing the emitter width and / or doping concentration.

iii) The process of entering data into ROM is called

a) writing b) burning

c) decoding d) registering.

iv) Average power dissipation per unit TTL NAND gate is

a) 15 mW b) 5 mW

c) 10 mW d) 1 W.

v) The fan-out of a standard TTL driver when connected to a load having 6 input is

a) 60 b) 6

c) 10 d) 12. ☐

vi) Typically 1 'mil' thickness means

a) 25·4 nm b) 25·4 mm

c) 25·4 μm d) 2·54 mm. ☐

vii) Which of the following has minimum propagation delay ?

a) ECL b) TTL

c) RTL d) DTL. ☐

viii) Which of the following is / are advantage of CMOS ?

a) Wide range of supply voltage

b) Greater noise margin

c) Large packing density

d) All of these. ☐

ix) Basic CCD is a

a) majority carrier device b) minority carrier device

c) can't be determined d) none of these. ☐

x) Optical lithography exposure tool is specified by

a) resolution, recycling, registration

b) throughput, tensile strength, resolution

c) throughput, resolution, registration

d) registration, clarity, explicability. ☐

xi) An ideal Op-Amp will have CMRR value

a) 0 b) ∞

c) 1 d) – 1. ☐

xii) Thin film circuits are preferable than the thick film circuits because

a) features sizes are comparable to MOS and bipolar process

b) temperature characteristics are quite good

c) hot spot effect is not there

d) all of these. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following questions. 3 × 5 = 15

2. a) What are the limitations of Op-Amp as comparator ? 3

b) What are the remedies for avoiding channelling in ion implantation ? 2

3. a) State the Moore's law. $1\frac{1}{2}$

b) What do we mean by a 'Class 100' clean room ? $1\frac{1}{2}$

c) What are the merits and demerits of Ion-Implantation ? 2

4. Draw the schematic diagram of the oxidant flow during oxidation. What do you mean by plasma oxidation ? 3 + 2

5. a) Write Fick's 2nd law of diffusion for a 3-*d* isotropic medium. Explain its significance in Si integrated circuit processing. 3

b) Draw the *C-V* curve of a MOS system for low and high frequencies. 2

6. Compare wet etching and dry etching. What do you mean by anisotropic etching ? What is loading effect ? 2 + 2 + 1

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following questions. 3 × 15 = 45

7. a) What properties of SiO_2 make it so important for IC fabrication technology ?

   b) What do you mean by isotropic and anisotropic etching ?

   c) What is the function of lithography in fabrication of VLSI chips ?

   d) Describe chemical vapour deposition (CVD) process used in VLSI.

   3 + 4 + 3 + 5

8. a) Explain how CMOS can be used for inverter logic. Draw the transfer characteristics.

   b) What is understood by speed power product ? Discuss how this factor decides the choice of appropriate logic family.

   c) Discuss the parasites associated with basic CMOS inverter and their role in logic transitions. 5 + (2 + 3) + 5

9. a) What are the different transistor models ?

   b) Draw an equivalent circuit of an *n-p-n* transistor by using the Ebers-Moll model.

   c) Derive the *I-V* relationship from this model.

   d) Draw and explain the collector characteristics from this model for normal biasing. 3 + 3 + 7 + 2

10. a) Draw the circuit diagram for BICMOS inverters and explain its principle of operation.

    b) How are BJT's connected in BICMOS and what is the amount of current gain ? Show the layout diagram of the BICMOS. 7 + 3 + 5

11. Write short notes on any *three* of the following : 3 × 5

a) Charge coupled device

b) Gummel-Poon model of BJT

c) Digital to analog converter

d) Open collector TTL gates

e) Ion implantation.

END