

Name :

Roll No. :

Invigilator's Signature :

CS/B.Tech/(ECE-NEW)/SEM-4/EC-402/2013

2013

**DIGITAL ELECTRONICS & INTEGRATED
CIRCUITS**

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

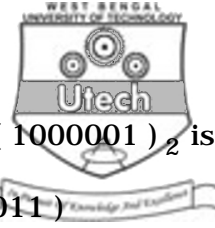
GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

$$10 \times 1 = 10$$

- i) A 10 MHz signal is applied to a Mod-5 counter followed by a Mod-8 counter. The output frequency will be
 - a) 10 kHz
 - b) 2.5 kHz
 - c) 5 kHz
 - d) 25 kHz.
- ii) Which family has better speed ?
 - a) ECL
 - b) DTL
 - c) TTL
 - d) MOS.
- iii) Digital multiplexer is basically a combinational logic circuit to perform the operation
 - a) AND-AND
 - b) OR-OR
 - c) AND-OR
 - d) OR-AND.



- iv) Gray code equivalent of binary number $(1000001)_2$ is
- a) (1100001) b) (1100011)
c) (1000011) d) (110101) .
- v) The decimal equivalent of 10111.0110 is
- a) 22.3 b) 23.375
c) 25.5 d) 26.55 .
- vi) Which flipflop may act as buffer ?
- a) SR b) JK
c) D d) T.
- vii) 2's complement of $(24)_{10}$ is
- a) 00011000 b) 11100111
c) 11101000 d) 11110011 .
- viii) Full form of FPGA is
- a) Full Programmable Gated Array
b) Field Programmable Gated Array
c) Full Peripheral Gated Array
d) Field Peripheral Gated Array.
- ix) A bubbled AND gate is equivalent to
- a) OR gate b) NAND gate
c) NOR gate d) X-OR gate.
- x) A carry look ahead adder is frequent, because it is
- a) faster b) more accurate
c) uses fewer gate d) costs less.

- xii) A decoder with enables input can be used as
- | | |
|---------------|------------------|
| a) encoder | b) demultiplexer |
| c) comparator | d) decoder. |



8. a) Design the following function using suitable MUX :
$$F(A, B, C, D) = \sum_m (1, 3, 4, 11, 12, 13, 14, 15).$$
 5
- b) Design a 16 : 1 MUX using 4 : 1 MUX. 5
- c) Design a full subtractor using decoder and necessary gates. 5
9. a) Describe DRAM and SRAM. Distinguish between them. 4 + 4 + 2
- b) Mention differences of ROM, RAM, EPROM, EEROM. 5
10. a) Design a combinational circuit for excess 3 code to BCD conversion using minimum number of logic gates. 9
- b) Describe dual slope A/D converter. 6
11. Write short notes on any *three* of the following : 3 × 5
- a) Priority encoder
 - b) Up-down counter
 - c) PLA
 - d) TTL
 - e) BCD to 7 segment decoder driver.
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