2013

COMPUTER ARCHITECTURE

Time Allotted : 3 Hours | Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A

(Multiple Choice Type Questions)

1 Choose the correct alternatives for the following : $10 \times 1 = 10$

i) Booth's Algorithm for computer arithmetic is used for

a) multiplication of numbers in sign magnitude form

b) multiplication of numbers in 2's complement form

c) division of numbers in sign magnitude form

d) division of numbers in 2's complement form.

ii) The technique of placing software in a ROM semiconductor chip is called

a) PROM

b) EPROM

c) EEPROM

d) FIRMWARE.

iii) Micro instructions are kept in

a) main memory

b) control store

c) cache memory

d) none of these.

iv) Associative memory is

a) content addressable memory

b) pointer addressable memory

c) slow memory

d) none of these.

v) The principle of locality justifies the use of

a) DMA

b) Hard disk

c) Polling

d) Cache memory.

vi) The full form of DMA is

a) Direct Memory Access

b) Dual Memory Access

c) Direct Machine Access

d) none of these.

vii) Physical memory broken into groups of equal size is called

a) page b) bloci

c) frame d) index.

viii) Instruction cycle is

a) decode-fetch-execute

b) fetch-execute-decode

c) fetch-decode-execute

d) execute-decode-fetch.

ix) The logic circuitry in ALU is

a) entirely combinational

b) entirely sequential

c) both combinational and sequential

d) none of these.

x) Maximum n bit 2's complement number is

a) 2^n

b) $2^n - 1$

c) $2^n + 1$

d) $2^{n-1} - 1$.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. a) Write three points to differentiate memory mapped I/O and I/O mapped I/O.

b) What are the advantages of Interrupt I/O over Programmed I/O ? 3 + 2

3. a) Represent (-15.50) in 64 bit IEEE floating point representation.

b) What are 'write through' and 'write back' policies in cache memory ? 2 + 3

4. a) Write the differences between serial adder and parallel adder.

b) Write the different addressing modes. 2 + 3

5. a) Compare RISC and CISC.

b) Discuss the role of operating system. 3 + 2

6. a) How many hardware models are present in VHDL ?

b) What do you mean by Top down disign and Bottom up design style ? 2 + 3

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) What are the bottlenecks of Von-Neumann architecture ?

b) Explain with an example how logical address is converted into physical address and also explain how page replacements take place.

c) Evaluate the following arithmetic statement using Three, Two, One and Zero address instructions:

$X = (A + B) - (C \times D)$. 3 + 6 + 6

8. a) Explain Booth's algorithm. Apply Booth's algorithm to multiply the two numbers $(-12)_{10}$ and $(-10)_{10}$.

   b) Discuss the different hazards in pipelining. 10 + 5

9. a) Draw the internal cell diagram of SRAM cell.

   b) What is cache memory ? What do you mean by hit ratio 75% ?

   c) According to the following information, determine the size of subfields (bits) in the address for Associative. Direct and Set associative mapping schemes :

   256 MB main memory and 1 MB cache memory

   Block size = 128 bytes : and there are 8 sets in a block.

   d) Draw and explain memory hierarchy pyramid.

   3 + 3 + 6 + 3

10. a) Show the bus connection with a CPU to connect four RAM chips of size 256 × 8 bits each and a ROM chip of 512 × 8 bit size. Assume that CPU has 8-bit data bus and 16 bit address bus. Clearly specify generation of chip select signals.

    b) Why do peripherals need interface circuits with them ?

    c) Explain with diagram the daisy chaining priority interrupt technique.

    d) Draw a block diagram to illustrate the basic organization of computer system and explain functions of each unit. 5 + 2 + 3 + 5

11. Write short notes on *any three* of the following : 3 × 5

    a) DMA

    b) Associative memory

    c) Harvard architecture

    d) Instruction pipeline

    e) Flynn's classification.