(c) Suppose the time delays of five stages of a linear synchronous pipeline t_1, t_2, t_3, t_4, t_5 are 70, 80, 60, 70, 85 ns respectively. The interface latch has an delay of 5 ns then calculate 4

(i) The minimum value of clock duration and maximum clock frequency.

(ii) Maximum speedup of this pipeline over its equivalent non-pipeline counterpart.

9. (a) What is the role of cache memory in computer architecture? 3

(b) What do you mean by 'locality of reference' in cache memory? 3

(c) Write the working principle of set associative mapping. 6

(d) Distinguish between L1 and L2 level cache memory. 3

10.(a) Why DMA based I/O is better than I/O techniques? 4

(b) Differentiate between isolated I/O and and memory mapped I/O. 3

(c) Explain DMA based data transfer operation between memory and other peripheral. 4

(d) What is the difference between vectored and non vectored interrupt? 4

11. Write short notes on any *three* of the following: 3×5

(a) Demand paging

(b) IEEE standard for floating point numbers.

(c) Pipeline Hazards

(d) Optimal page replacement algorithm

(e) Mainframe computer

(f) Structural modeling in VHDL

EC-504A

COMPUTER ARCHITECTURE

Time Allotted: 3 Hours Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. 10×1 = 10

(i) How many memory locations can be accessed with 6 bit address bus?

(A) 32 (B) 128
(C) 16 (D) 64

(ii) In a microprocessor the address of next executable instruction is stored in

(A) stack pointer (B) address latch
(C) program counter (D) GPP

(iii) Control unit operation is performed by

(A) hardware control only (B) microprogram control only
(C) (A) and (B) (D) none of these

(iv) A microprogram written as string of 0's and 1's is a

(A) symbolic microinstruction (B) binary microinstruction
(C) binary micro-program (D) none of these

(v) CPU does not perform the operation

(A) data transfer (B) logic operation
(C) arithmetic operation (D) all of these

(vi) The advantage of RISC processor over CISC processor is that

(A) the hardware architecture is simpler
(B) an instruction can be executed in one cycle
(C) less number of registers accommodate in chip
(D) parallel execution capabilities

(vii) Dynamic RAMs are best suited to

(A) slow system (B) large system
(C) one bit system (D) none of these

(viii) To provide increased memory capacity for operating system, the

(A) virtual memory is created
(B) cache memory is increased
(C) memory for OS is reserved
(D) additional memory is installed

(ix) The inter instruction dependencies in program cause

(A) data hazard (B) structural hazard
(C) control hazard (D) both (A) and (B)

(x) A page fault

(A) occurs when a program accesses to a page memory
(B) it is an error in a specified page
(C) is an access to a page not currently in memory
(D) none of these

(xi) Principal of locality justifies the use of

(A) interrupts (B) polling
(C) DMA (D) cache memory

(xii) 'Delayed branching' is related to

(A) pipeline hazard (B) pipeline remedy
(C) both (A) and (B) (D) none of these

GROUP B
(Short Answer Type Questions)

$3 \times 5 = 15$

Answer any *three* questions.

2. Write key feature of Von-Neumann architecture of a computer and mention the bottlenecks. How does Harvard architecture differ from Von-Neumann architecture?

3. Why memory hierarchy is needed? What is locality of reference? What is memory mapping?

4. Discuss the differences between (i) Centralized bus and Distributed bus (ii) Synchronous bus and Asynchronous bus.

5. Draw the control circuit for the following RTL
   T1 : A < -B
   T2 : A < -C

6. State and explain the different types of instruction formats.

GROUP C
(Long Answer Type Questions)

$3 \times 15 = 45$

Answer any *three* questions.

7. (a) Describe the function of major components of a digital computer. 7
   (b) Discuss the role of an operating system in computer system. 4
   (c) Explain the advantages and disadvantage of a parallel adder over a serial adder. 2
   (d) Distinguish between carry look ahead adder and a ripple carry adder. 2

8. (a) Discuss the working principle of a synchronous linear pipeline. 5
   (b) Define (i) speed up (ii) efficiency (iii) throughput. 6

[Turn over]