2013
MICROPROCESSOR & MICROCONTROLLER

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) The address line required for 16 k byte memory chip are

      a) 13 b) 14

      c) 15 d) 16.

   ii) The interrupt line having highest priority is

      a) RST 7·5 b) READY

      c) TRAP d) INTR.

   iii) How many interrupts are controlled by 8259 A ?

      a) 8 b) 6

      c) 9 d) 5.

iv) PSW in 8085 microprocessor is a

a) 8-bit register b) 16-bit register

c) 4-bit register d) 32-bit register.

v) Intel 8086 processor is

a) 16-bit b) 32-bit

c) 64-bit d) none of these.

vi) 8085 microprocessor operates at a frequency of

a) 6 MHz b) 3·2 MHz

c) 5 MHz d) 3 MHz.

vii) READY is used for

a) input b) output

c) both (a) & (b) d) none of these.

viii) The memory map of a 4 kB memory chip begins at location 3000 H. The last location of memory address and number of pages in the chip are

a) 3FFFH, 16 b) 4000H, 16

c) 3F00H, 8 d) 300FH, 4.

ix) Number of segment registers in 8086 microprocessor are

a) 8 b) 4

c) 16 d) 32.

x) On-chip ROM size of 8051 microcontroller is

a) 1 kB b) 16 kB

c) 4 kB d) 8 kB.

xi) In 8255 programmable peripheral interface, bidirectional mode of operation is supported in

a) Mode 1 b) Mode 0

c) Mode 0 and Mode 1 d) Mode 2.

xii) In 8051 microcontroller external ROM is selected using

a) $\overline{EA}$ b) $\overline{PSEN}$

c) RESET d) ALE.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) Interface two 2 K × 8 RAM with 8085 microprocessor by using IC 74138 decoder such that starting address assigned to them are 8000 H and 9000 H respectively.

b) What are maskable interrupts ? Give an example. 3 + 2

3. a) What do the following instructions do ?

i) XRA A

ii) LHLD 8000 H

iii) RRC.

b) Discuss the 'fetch' and 'execute' operations of 8086 microprocessor.

4. Write an assembly language program to add two 16-bit numbers using 8051 controller.

5. Write an assembly language program to load a block of data from memory location 80XX H to memory location 80XY H. Clearly mention the assumptions.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

6. a) Briefly discuss the different transfer modes of 8237 DMA controller.

b) **Draw a timing diagram for Op-Code 'fetch' machine cycles of 8085 microprocessor.**

c) How much time is required to execute the following instruction ?

MVI B, 07 (07 *T*-states).

d) What are the different modes of operations of 8255 PPI ? 5 + 3 + 3 + 4

7. a) How does 8086 microprocessor support memory segmentation ?

b) How is pipelining implemented in 8086 ?

c) What is the relationship between logical address and physical address in 8086 ?

d) How can even and odd addresses be achieved for memory organization in 8086 ?

e) Discuss the flag register of 8086. 5 × 3

8 a) Write an assembly language program using 8085 assembly language to arrange a string of length 10 bytes in ascending order.

b) Explain bidirectional data transfer using 8255 PPI. 8 + 7

9. a) What will be the contents of the accumulator and flag after the following instructions from a program that are executed sequentially ?

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MVI A, 01
MVI B, 02
ADD B
XRA A
HLT
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b) Draw the block diagram of 8254 timer and briefly discuss its operation and organization.

c) Describe the priority scheme and EOI scheme of 8259 A. (2 + 2) + 6 + 5

10 Write short notes on any *three* of the following . 3 × 5

a) Function of 8251 USART

b) Serial mode of operation using 8085 microprocessor

c) Subroutine organization (including calls) in 8086 microprocessor

d) BIU and EU of 8086 microprocessor

e) DMA.