Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech (CSE-OLD)/SEM-4/CS-403/2013

2013

ADVANCED COMPUTER ARCHITECTURE

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : 10 × 1 = 10

   i) Total number of registers in SPARC processor is

      a) 24 b) 64

      c) 128 d) 136.

   ii) In SPARC processor at any instant, a program can address

      a) 8 registers

      b) 24 registers

      c) 32 registers

      d) 64 registers.

iii) The CPU of RISC processor is controlled by

a) Control Memory

b) RAM

c) Hardware without control memory

d) None of these.

iv) If memory access takes 20 ns with cache and 110 ns without it, then the hit ratio is

a) 93% b) 90%

c) 87% d) 88%.

v) How many stages does MMX pipeline have ?

a) 2 b) 4

c) 6 d) 12.

vi) Which one of the following networks provides the highest bandwidth and interconnection capability ?

a) Crossbar network b) Multistage network

c) Bus system network d) None of these.

vii) Total number of degrees of a completely connected network (total number of nodes N) is

a) 1 b) N – 2

c) N – 1 d) N.

viii) Intel Pentium-4 is a ..... type of processor.

a) 8 bit

b) 16 bit

c) 32 bit

d) 64 bit.

ix) Choose the correct statement :

a) MAL is lower bounded by the maximum number of check marks in a row of the reservation table

b) MAL is upper bounded by the maximum number of check marks in a row of the reservation table

c) MAL is lower bounded by the maximum number of check marks in a column of the reservation table

d) None of these.

x) If a program of 15000 instructions is being executed by a linear 5 stage pipelined processor with a clock rate of 25 MH, then the speed-up of this pipeline when compared to an equivalent non-pipelined processor is

a) 2·33

b) 4·99

c) 3

d) 5·4.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. What are meant by horizontal and vertical vector processing ? Find out speed-up of horizontal processing over uniprocessing ?

3. Discuss Flynn's Taxonomy of computer architecture.

4. Explain the following terms :

   i) Write-through *vs* Write-back caches

   ii) Factors affecting cache hit ratio. 3 + 2

5. Consider the following interleaved memory designs for a main memory system with 16 memory modules. Each module is assumed to have a capacity of 1 MByte. The machine is byte-addressable. Design 16 way interleaving with one memory bank.

6. What is the usefulness of MIMD architecture ? What is the difference between UMA and NUMA ?

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Consider the following pipeline reservation table :

	1	2	3	4
S1	X			X
S2		X		
S3			X	

i) Find out the forbidden latencies and the initial collision vector. 2

ii) Draw the state transition diagram. 3

iii) List all the simple cycles and the greedy cycles. 3

iv) Determine the MAL. 2

b) How do you calculate the optimal performance/cost ratio (PCR) for a pipelined architecture ? How to achieve the maximum throughput of a pipelined architecture ? 5

8. a) Compare the relative merits of the 3 cache memory organizations.

   i) Direct-mapping cache

   ii) Fully-associative cache

   iii) Set-associative cache.

   b) Answer the following questions with reasoning :

   i) In terms of hardware complexity and implementation cost, the three cache organizations with justification.

   ii) With respect to flexibility in implementing block replacement algorithms, rank the three cache organizations and justify the ranking order.

   iii) Explain the effects of block size, set number, associativity and cache size on the performance of a set associative cache organization. 3 + 7 + 5

9. a) Write down the difference between Control Flow Architecture and Data Flow Architecture.

   b) What are the advantages of Message Passing Architecture ?

   c) Describe 8 × 8 Omega network with the following permutation :

   $\prod$ = (0, 7, 6, 4, 2) (1, 3) (5) 5 + 3 + 7

10. a) Compare between SIMD architecture and vector processor. 2

    b) Define an expression to calculate CPI (clock cycles per instruction) and CPU time. 2

    c) Following performance measures were recorded while running a machine.

Instruction Category	Percentage of occurrence	Number of cycles/instruction
ALU	35	1
LOAD & STORE	30	2
BRANCH	15	3
OTHERS	20	5

   Calculate the CPI and MIPS for this machine assuming the clock rate to be 200 MHz. 6

    d) Describe the shared memory model of SIMD architecture. 5