



Name :

Roll No. :

Invigilator's Signature :

CS/B.Tech (EE)(N)/EEE (N)/ICE (N)/SEM-3/EC(EE)-302/2012-13

2012

DIGITAL ELECTRONICS CIRCUITS

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

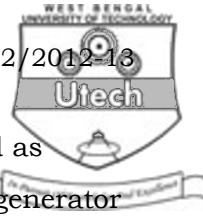
GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

$$10 \times 1 = 10$$

- i) The fastest ADC is
 - a) dual slope type
 - b) successive approximation type
 - c) counter type
 - d) none of these.
- ii) The fastest logic family is
 - a) TTL
 - b) CMOS
 - c) RTL
 - d) ECL.
- iii) A flip-flop has
 - a) one stable state
 - b) two stable states
 - c) no stable states
 - d) none of these.



- iv) A decoder with enable input can be used as
 - a) encoder
 - b) parity generator
 - c) multiplexer
 - d) demultiplexer.
- v) The operation which is commutative but not associative is
 - a) AND
 - b) XOR
 - c) NAND
 - d) NOT.
- vi) The minimum number of NAND gates required to design one full adder circuit is
 - a) 5
 - b) 9
 - c) 6
 - d) 10.
- vii) Which of the following codes is self complementing ?
 - a) Gray code
 - b) BCD code
 - c) Hamming code
 - d) Excess-3 code.
- viii) A decade counter counts up to
 - a) 9
 - b) 10
 - c) 11
 - d) 12.
- ix) $(A + B + C + D)'$ equals
 - a) $A'B'CD$
 - b) $A'B'C'D'$
 - c) $AB'C'D$
 - d) $AB'CD$.
- x) The universal register
 - a) accepts serial input
 - b) accepts parallel input
 - c) gives serial and parallel outputs
 - d) all of these.



- xi) The SOP form of logic expression is most suitable for designing logic circuits using only
- a) XOR gates b) NOR gates
- c) NAND gates d) OR gates.
- xii) The parity of the binary number 100110011 is
- a) even b) odd
- c) 2 d) 1.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Implement the following expression using NOR gate only :

$$F(A,B,C) = \sum m(0,1,4,6)$$
3. Design a carry look ahead adder.
4. Using 2's complement method subtract 101101_2 from 1011101_2 .
5. Convert an SR F/F to a T F/F.
6. Explain the operation of a master-slave J-K F/F.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Draw the circuit diagram of a 2 input TTL NAND gate and explain how it works.
- b) Describe the R-2R ladder type D/A converter.
- c) What do you mean by resolution ? $7 + 7 + 1$



8. a) What is the difference between the synchronous counter and asynchronous counter ?
 b) Design a mod 6 ripple counter.
 c) Design a mod 3 synchronous counter. 3 + 6 + 6
9. a) Write down the excitation table of JK and D flip-flop and derive the excitation equation for these two flip-flops.
 b) What is MUX ? What are its applications ?
 c) Design a full subtractor using 4 to 1 MUX. 6 + 3 + 6
10. a) Describe the operation of successive approximation type ADC.
 b) How many clock pulses are required in worst case for each conversion cycle of an 8-bit SAR type ADC ? Define quantizing error for an ADC.
 c) Design a JK flip-flop using D flip-flop 6 + 2 + 2 + 5
11. a) Design BCD to excess-3 decoder using suitable logic gates.
 b) Implement the following functions using 3 X 4 X 2 PLA :
 $F_1(A, B, C) = \sum m(3, 5, 6, 7)$ and
 $F_2(A, B, C) = \sum m(0, 2, 4, 7)$
 c) Explain the working principle of Universal shift register with suitable logic diagram. 5 + 5 + 5