CS/B.Tech(CSE/IT)/SEM-3/EC-312/07/(08)

3



ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER - 2007 DIGITAL ELECTRONICS & LOGIC DESIGN

SEMESTER - 3

Time: 3 Hours]		A. Carrier		[Full Marks: 70
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GROUP - A

		(Multiple Choice	Туре	Questions)	
l. Ch	oose t	he correct alternatives for any to	en of th	ne following:	$10\times1=10$
ij	Cor	nvert (444.456) ₁₀ into its octal	equiva	lent	
	a)	673.5136	b)	674.35136	
	c)	674.735	d)	none of these.	
ii)	(A	$A + \bar{B} + \bar{A}B$ $C =$			
	a)		b)	0	
	c)		d)	č.	
iii)	Hov	w many l's are present in the	e bina	ry representation of	decimal number
	(3)	\times 512 + 7 \times 64 + 5 \times 8 + 3)?			
	a)	8	b)	9	
	c)	10	d)	11.	
iv)	An e	xample of reflected code is			
	a)	BCD	b)	ASCII	
•	c)	GRAY	d)	Hamming.	

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v)	The	value of 2^{5} in octal sys	item is		•
	a)	40	b)	20	
	c)	400	d)	none of these.	
vi)	The	minimum number of N	AND gates req	uired to design one XOR g	ate is
	a)	4	b)	5	
	•				
	c)	6	d)	3.	
•					
	The o		tativa hest s	not appopiative is	
vii)	1116	operation which is com	mutative but I	iot associative is	
	a)	AND	b)	XOR	
	c)	NAND	d)	NOT.	
viii)	A d	ecoder with enable i/p o	an used as		
٠.	a)	Encoder	b)	Parity generator	
	· ·	Micouci		Turity gorrorum.	·
	c)	Multiplexer	d)	DeMultiplexer.	
				•	
ix)	Ine	resolution of an 8 bit A	/D converter	1S	
	a)	0.62%	b)	0.38%	• 1
	c)	0.39%	d)	1.25%.	
	A 1	O MUz paraza more ala	oko hove o E	bit ripple counter. The fre	nuency of
x)			cas have a 3	on uppe counter, the ne	quoney or
e e	3rd	flip-flop's output is			
	a)	2 MHz	b)	1.25 MHz	
	c)	50 kHz	d)	25 kHz.	. 1

d)

50 kHz

c)

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		/111/86:M-3/64:314/U//(UO	
 D. I CC			,

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xi)	If (2	$212)_x = (23)_{10}$, where x is ba	use (+ v	e integer), then the value of	x is
	a)	2	b)	3	
	c)	5	d)	4.	
xii)	Calc	culator keyboard is an example	of		
	a)	decoder	b)	multiplexer	
	c)	encoder	d)	de Multiplexer.	
xiii)	The	carry output of a full adder is	three ir	nput	
	a)	majority logic	b)	minority logic	
•	c)	XOR logic	d)	NAND logic.	
xiv)	Flip	o-flop that makes output equals	s to inpu	it after clock is	
	a)	J-K flip-flop	b)	D flip-flop	
	c)	T flip-flop	d)	None of these.	
xv)	One	e-bit even parity error detection	n code f	ails to detect	
	a)	any even number of error	b)	any odd number of error	
	c)	both (a) and (b)	d)	none of these.	
	•		UP – B		
		(Short Answer	Type Q	uestions)	
		Answer any three	ee of the	e following.	$3 \times 5 = 15$
Sim	plify t	the Boolean function using K-m	nap		

 $F(W, X, Y, Z) = \sum m(0, 4, 5, 6, 8, 9) + \sum d(10, 11, 12, 13, 14, 15).$

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2.

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6



3. Implement the following function using all 4: 1 multiplexers

$$F = \sum m(0, 2, 3, 6, 8, 9, 12, 14)$$

- Implement a full-adder circuit using a 3 to 8 decoder with all active-low outputs and one additional logic gate if required.
- Define the following terms in relation with logic families :

5 x

- a) propagation delay
- b) fan-in
- c) fan-out
- d) power dissipation
- e) floating inputs.
- Find out the 7's complement of (-756)₈.

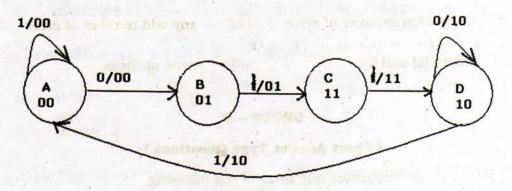
GROUP - C

(Long Answer Type Questions)

Answer any three questions.

 $3 \times 15 = 45$

- 7. a) Design an asynchronous 4-bit up-down counter and it will count up when a signal line M = 0 and count down when a signal line M = 1.
 - b) Design a circuit that will function as prescribed by the state diagram shown below. Use S-R flip-flops for implementation.



State Diagram

6 + 9

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- 8. a) With the help of necessary circuit diagram explain the operation dual slop ADC.
 - b) A 4-bit binary ladder D/A converter with $R = 10 \text{ K}\Omega$ uses a reference of 5 V. Find
 - i) the ideal scale factor in V/step
 - ii) the analog o/p corresponding to the binary i/p 0110
 - iii) resolution in %
 - tv) full scale o/p
 - v) the maximum deviation in volts from the best straight line in order to meet standard linearity. $5 + 5 \times 2 = 15$
- 9. a) Design a BCD to 7-segment common anode display code converter using PROM type PLD.
 - b) Implement the following functions using a $3 \times 4 \times 2$ PLA:

$$F_1(A, B, C) = \sum (3, 5, 6, 7)$$

$$F_2(A, B, C) = \sum (0, 2, 4, 7).$$

7 + 8

10. a) Simply the following function by means of tabulation method:

$$F = \sum m(0, 1, 4, 7, 9, 11, 13, 15) + \sum d(3, 5).$$

- b) Simplify the following function using K-map.
 - i) $F = \prod m(0, 1, 3, 8, 10, 15) . \prod d(11, 13, 14)$
 - ii) $F = \sum m(0, 4, 7, 9, 13, 15) + \sum d(10, 14)$

5 + 5 + 5

11. Write short notes on any three of the following:

 3×5

- a) EPROM
- b) PLD
- c) A/D converter
- d) Johnson counter.

END