	Utech
Name:	
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Invigilator's Signature :	

CS/B.Tech(CSE/IT)/SEM-3/EC-312/2009-10 2009

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A

			artour			
(Multiple Choice Type Questions)						
1.	Choose the correct alternatives for any ten of the following					
					$10 \times 1 = 10$	
	i)	i) An example of weighted code is				
		a)	Excess-3	b)	ASCII	
		c)	Hamming code	d)	8421.	
	ii) The minimum number of NAND gates required to desi				gates required to design	
one Full Adder circuit is						
		a)	5	b)	9	
		c)	6	d)	10.	
	iii) A decoder with enable input can be used as				n be used as	
		a)	Encoder	b)	Parity Generator	

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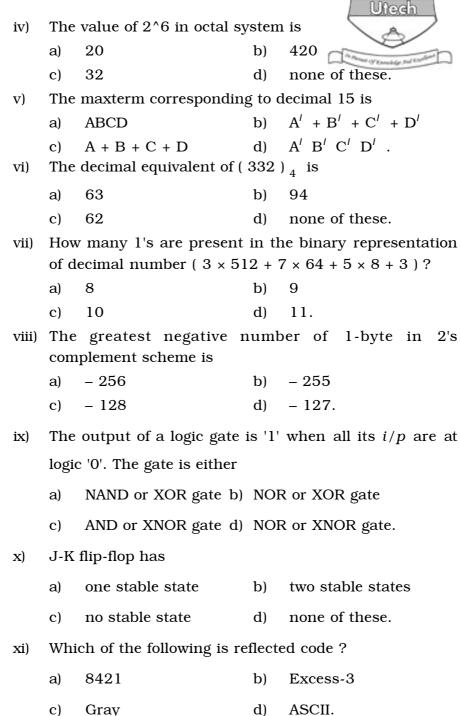
c)

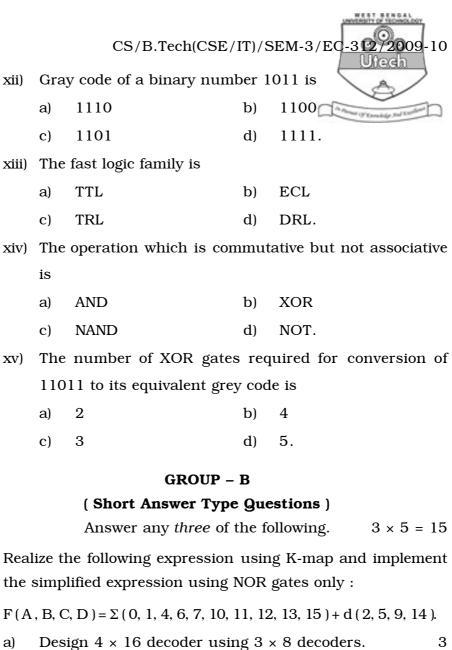
NAND

d)

Demultiplexer.

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 $F(A, B, C, D) = \Sigma(0, 1, 4, 6, 7, 10, 11, 12, 13, 15) + d(2, 5, 9, 14).$

3. Design 4×16 decoder using 3×8 decoders.

b) Implement 2-input XOR function using minimum number of 2-input NAND gates.

Design full subtractor using 4:1 multiplexers. 4.

a)

c)

a)

c)

is

a)

c)

a)

c)

2.

2

3

- 5. Perform the conversion from S-R to J-K flip-flop.
- Realise a full-subtractor using all NAND gates. 6.

GROUP - C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

- 7. a) Describe the operation of successive approximation type ADC. How many clock pulses are required in worst case for each conversion cycle of an 8-bit SAR type ADC? Define quantizing error for an ADC.
 - b) Draw a neat diagram for an R-2R ladder type DAC & explain its operation. 7 + 8
- 8. a) Design a MOD-10 synchronous binary UP-counter using JK flip-flop & other necessary logic gates.
 - b) Calculate the propagation delay for a 4-bit synchronous binary UP-counter when JK flip-flops are connected in series connection & parallel connection.
 Given Propagation delay Tp (F/F) in 30 nsec & propagation delay of the gates used in the circuit is 20 nsec (assumed to be equal for all gates).
- 9. a) Draw the circuit for a 4-bit Johnson counter sing D flip-flop & explain its operation. Draw its timing diagram. How does its timing diagram differ from that of Ring counter?
 - b) Perform the conversion from D f/f to JK f/f. 8 + 7
- 10. a) Distinguish between ROM, PLA & PLD's as elements realizing Boolean function.
 - b) Design a combinational circuit using an 8×4 ROM that accepts a 3-bit number & generates an output binary number equal to the square of input no.
 - c) Draw a logic diagram of master-slave JK f/f. Why is it called so? 7 + 5 + 3
- 11. Write short notes on any *three* of the following: 3×5
 - a) EEPROM
 - b) D/A converter
 - c) Triggering of flip-flops
 - d) Comparator
 - e) Data lock-out in a counter.

44001 4