ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2009

DIGITAL ELECTRONICS & INTEGRATED CIRCUITS

SEMESTER - 4

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

i) The octal equivalent of the binary number 11010111 is

a) 656 b) 327

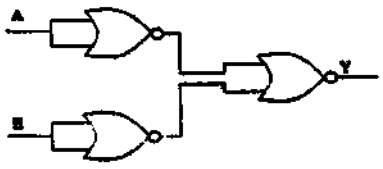
c) 653 d) D7.

ii) The minimum number of NAND gates required to implement the Boolean function $A + AB' + AB'C$ is equal to

a) zero b) 1

c) 4 d) 7.

iii) Indentify the operation of the following logic gate circuit.



a) OR gate b) AND gate

c) NOT gate d) none of these.

3. Minimize the following expression in SOP form using Quine McClusky method :

$F(A, B, C, D) = \Sigma m(1, 2, 3, 8, 9, 10, 11, 14) + \Sigma d(7, 15)$.

4. Explain the race around condition. Draw the Master/Slave JK flip-flop using all NAND gates. 2 + 3

5. Implement a full-adder circuit using 3 to 8 decoder with all active high outputs and other necessary logic gates.

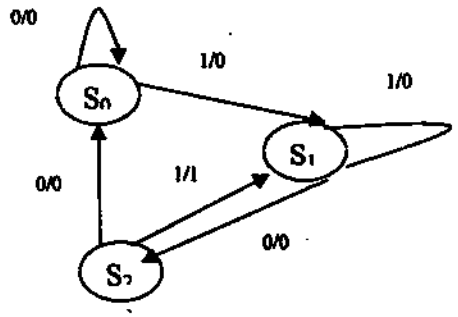
6. Draw and explain the circuit of 8 × 1 MUX using two 4 × 1 MUX and one 2 × 1 MUX.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following questions. 3 × 15 = 45

7. a) Design a clocked synchronous sequential network whose state diagram is given below : 8



b) Design a combinational circuit, which converts excess – 3 number to its corresponding BCD number. 7

8. a) Implement the following Boolean expressions using Decoder.

$F_1(A, B, C, D) = \Sigma(1, 2, 5, 7, 8, 10, 12, 13)$. 5

b) Implement a full adder circuit using minimum number of NOR gates only. 5