Name : ……………………………………………………………

Roll No. : …………………………………………………………

Invigilator's Signature : ……………………………………………

CS/B.TECH(CSE)(N)/SEM-5/CS-502/2012-13

2012

MICROPROCESSOR & MICROCONTROLLER

Time Allotted : 3 Hours   *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words

as far as practicable.

GROUP – A

(Multiple Choic   Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

$$10 \times 1 = 10$$

    i)   The … ….. ……. ensures that only one IC is active at a time to avoid a bus conflict caused by two ICs writing different data to the same bus.

        a)   Control bus   b)   Control instructions

        c)   Address decoder   d)   CPU.

    ii)   What is the vector call location of NMI ?

        a)   002CH   b)   0028H

        c)   0010H   d)   0024H.

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    iii)   The total memory space available in 8086 is

        a)   16 kb   b)   64 kb

        c)   1 Mb   d)   256 kb.

    iv) T-States in 'CALL' instruction of 8085 CPU are

        a)   13   b)   18

        c)   10   d)   7.

    v)   8259A interrupt controller controls how many interrupts ?

        a)   8   b)   5

        c)   6   d)   9.

    vi)   If ready pin grounded, it will introduce .... status into the bus Cycle of 8086/8088 microprocessor.

        a)   w it   b)   idle

        c)   wait & remains idle   d)   all of these.

    vii)   The instruction : XCHG exchanged the contents of

        a)   Acc & H

        b)   DE-pair & HL pair

        c)   BC-pair & HL pair

        d)   HL-pair & memory location.

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viii) If DMA request is sent to the microprocessor with a high signal to the HOLD pin, the microprocessor acknowledge the request

    a)   after completing the present cycle

    b)   immediately after receiving the signal

    c)   after completing the program

    d)   none of these.

ix) The number of programmable 8- it register of 8085 microprocessor is

    a)   5   b)   6

    c)   8   d)   7.

x) For 8257 controller .... is the highest priority channel by default.

    a)   CH 0   b)   CH-1

    c)   CH-3   d)   any channel.

xi) In 'JZ NEXT' instruction of 8051 microprocessor, which register's content is checked to see if it is zero ?

    a)   A   b)   R2

    c)   R1   d)   B.

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   xii) When a subroutine is called the address of the instruction next to CALL is saved

   a) stack pointer register

   b) program counter

   c) stack

   d) combination of flag and BC register.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following $3 \times 5 = 15$

2. If the system clock is 1·5 MHz, find the time to execute the given instruction code :

MVI A, (5A) H

MVI B, (A7) H

ADD B

INR A

XRA A

HLT

3. a) L st the operating mode of the 8255A PPI.

   b) How is pipelining achieved in 8086 microprocessor ?

                                                          2 + 3

4. a) What is tri-state ? Why it is important ?

   b) Can an import and an output port have same address ? Justify.   2 + 3

5. Briefly describe timing diagram of Memory write cycle.

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GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following.   3 × 15 = 45

6. a) What are BSR & IO mode in 8255A ?

   b) Write a program to initialize 8255 in the configuration given below :

   port A : O/P with handshake

   port B : I/P with handshake

   port C_L : O/P

   port C_U : I/P, assume address of the ctrl word register of 8255 as 23H.

   c) What is scan ounter in 8279A ?

7. a) Write down the different interrupts of 8051MC.

   b) Draw the block diagram of 8051 and explain it.

   c) Copy the byte in TCON to register R2 using at least three different methods.   5 + 7 + 3

8. a) Explain different flags of 8086.

   b) Write a program for 8086 to add the bytes of data stored from 00D00H to 00D0FH and to store the result in location 00B00H.

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c) What is addressing mode ? Explain with examples of different addressing modes of 8086. 3 + 7 + 5

9.

m/m loc^n in hex	mnemonics
8000	LXI SP, 20FFH
8003	LXI H. 1234H
8006	MVI A, 05H
8008	CALL2010H
800B	MOV B, A
800C	HLT
2010	PUSH B
2011	PUSH PSW
2012	MVI B, 12H
2014	ADD B
2011	RET

a) Write down the content of PC before CALL instruction.

b) Write down the content of stack & SP after execution of CALL.

c) What happen when RET instruction is executed ?

d) What happen when PUSH instruction is executing ?

e) What is the value of PC after execution of CALL instruction ?

f) Calculate the total execution time of above program if clk frequency is 2 MHz ? 2 + 2 + 2 + 2 + 2 + 5

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10. Write short notes on any *three* of the following : 3×5

    a)   DMA

    b)   RIM & SIM

    c)   MODE 2 of 8255 A

    d)   Addressing mode of 8051 MC

    e)   1 sec DELAY subroutine.

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