Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH(ECE)/SEM-5/EC-503/2011-12

2011

COMPUTER ARCHITECTURE AND ORGANIZATION

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : 10 × 1 = 10

i) The capacity of a memory unit is defined by the number of words multiplied by the number of bits / word. How many separate addresses and data lines are needed for a memory 4 K × 16 ?

a) 10 addresses, 16 data lines

b) 11 addresses, 8 data lines

c) 12 addresses, 16 data lines

d) 12 addresses, 12 data lines.

ii) In which type of operation zero address field instruction is used ?

a) Single CPU organization

b) General Register organization

c) Stack organization

d) None of these.

iii) The minimum number of operands with any instruction is

a) 1 b) 0

c) 2 d) 3.

iv) Which logic gate has the highest speed ?

a) DTL b) RTL

c) ECL d) TTL.

v) Micro-instructions are kept in

a) main memory b) control memory

c) cache memory d) none of these.

vi) The basic principle of von Neumann computer is

a) storing program and data in separate memory

b) using pipeline concept

c) storing both program and data in the same memory

d) using large number of registers.

vii) Program counter is

a) storing program and data in separate memory

b) using pipeline concept

c) storing both program and data in the same memory

d) none of these.

viii) The instruction execution flow in the pipeline processor is represented by

a) Reservation table b) Data flow diagram

c) Flow chart d) Space time diagram.

ix) Memory mapped I/O scheme is used for the allocation of address to memories and I/O devices is used for

a) small system

b) large system

c) both small and large systems

d) very large system.

x) Number of transistors in a CMOS static RAM cell is

a) 1 b) 4

c) 6 d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Evaluate the following arithmetic expression in zero address, one address and two address machines.

$Y = (A - B) / (C + D * E)$.

3. Briefly explain the functionality of associative memory.

4. What is an interrupt ? What is the difference between vectored and non-vectored interrupts ?

5. Discuss about the different hazards in pipelining.

6. Explain the purpose of different types of registers used in a computer.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. With the help of a block diagram, describe the components of a Microprogrammed Control Unit. Differentiate between hardwired and microprogram approaches to control design. Discuss the advantages and disadvantages of horizontal and vertical microinstructions. What is a microprogram sequencer/control and why is it required ? 4 + 4 + 4 + 3

8. a) What is virtual address ? In virtual memory how address mapping is done using pages ? Explain with example.

   b) An instruction is stored at location 302 with its address field at location 303. The address field has a value 405. A processor register R1 contains the number 206 at the beginning. Evaluate the effective address if the addressing mode is
      i) direct
      ii) relative
      iii) register indirect
      iv) index with R1 as the index register. 2 + 7 + 6

9. a) What is meant by DMA ? Why is it useful ? Briefly explain with suitable diagram, the DMA operation in association with CPU.

   b) Draw the schematic diagram for daisy chain polling arrangement in case of vectored interrupt for three devices. 2 + 2 + 4 + 7

10. a) Design the ALU of a digital computer.

    b) What do you mean by instruction cycle, machine cycle and T-states ? 10 + 5

11. Write short notes on any *three* of the following : 3 × 5
    a) CD ROM drive.
    b) Difference between computer architecture and organization.
    c) Harvard and Neumann architecture.
    d) Carry look-ahead adder.
    e) Content addressable memory.