Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech (CSE)/SEM-8/CS-801D/2011

2011

VLSI DESIGN

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) The composition of the aluminium-copper-silicon alloy used to reduce the electromigration effects is

a) 89% Al, 5% Cu and 6% Si

b) 95% Al, 4% Cu and 1% Si

c) 70% Al, 10% Cu and 20% Si

d) 89% Al, 10% Cu and 5% Si.

ii) NMOS enhancement mode transistors are faster than PMOS transistors, because

a) the electron mobility is higher than the hole mobility

b) the hole mobility is higher than the electron mobility

c) concentration of electron is greater than holes

d) none of these.

iii) Gate current of a MOSFET is smaller than that of a JFET, because

a) the insulating oxide layer offers a very high input resistance

b) the insulating oxide layer offers a very low input resistance

c) the insulating oxide layer offers a very high output resistance

d) none of these.

iv) For a symmetric CMOS inverter, $Z_{pd} : Z_{pu}$ =

a) 1·5 : 1 b) 2·5 : 1

c) 2·1 : 1 d) 2 : 1.

v) The full form of the abbreviation of FPGA is

a) Field Programmable Gate Array

b) Function Programmable Gate Array

c) Field Programmable Graphics Array

d) Field Programmable Graphics Adaptor.

vi) Ingots of single crystal silicon are produced from molten polycrystalline silicon by

a) Czochralski method b) CVD method

c) CCD method d) None of these.

vii) One property of fuse-based FPGA is

a) one-time programmable

b) two-time programmable

c) three-time programmable

d) none of these.

viii) For pseudo nMOS logic ratio of Z (pull-up) and Z (pull-down) is

a) 4 : 1 b) 3 : 1

c) 2 : 1 d) 1 : 1.

ix) Maximum fan-outs of CMOS inverter circuit are

a) 4 b) 10

c) 14 d) 20

x) For a given process if all dimensions are in terms of λ rule, then minimum dimension is of

a) 2 λ b) 4 λ

c) 6 λ d) 8 λ.

xi) Which design rule is scalable in the context of VLSI design ?

a) λ rule b) μ rule

c) σ rule d) none of these.

xii) For nMOS transistor the source and drain should be

a) *n* type b) *p* type

c) *m* type d) none of these.

xiii) Which of the following devices is expected to have the highest input impedance ?

a) BJT

b) JFET

c) MOSFET.

xiv) The source self-bias technique cannot be used for

a) JFETs

b) enhancement MOSFETs

c) depletion MOSFETs.

xv) A depletion MOSFET differs from a JFET because it has no

a) gate

b) channel

c) $p - n$ junction.

GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Give the CMOS implementation of an XOR gate.

3. Compare between CMOS technology and BiCMOS technology.

4. Explain how two cross-coupled inverters function like a flip-flop.

5. What is scaling in VLSI ? What are the two scaling models used in VLSI ? What is ion implantation ?

6. Describe the procedures for "placement" and "Routing" in VLSI physical design.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Show that the resistance of an enhancement mode *N*-MOSFET for low drain-source voltage is

$$R = \frac{LD}{\mu \xi W\left(V_{GS} - V_{TH} - V_{DS}/2\right)}$$

where the symbols have their usual meanings.

b) How is the drain current related to the gate-source voltage in the saturation region ? 10 + 5

8. a) Derive an expression for the inverter logic threshold voltage V_{INV} for an *N*-MOS inverter and hence show that for V_{INV} to lie midway between the drain supply voltage and ground, $Z_{pu} : Z_{pd} = 4 : 1$.

b) An *N*-MOS transistor with $k = \mu \xi / D = 25 \times 10^{-6}\ \text{A/V}^2$ and $V_{TH} = 1{\cdot}5\ \text{V}$ is operated at $V_{GS} = 5\ \text{V}$, $I_D = 50\mu\ \text{A}$ and $V_{GS} = 0{\cdot}25\ \text{V}$. Find the value of W/L and the power dissipated by the transistor. If $V_{DD} = 5\ \text{V}$, calculate the load resistance R to be connected in series with the drain. 9 + 6

9. a) Explain the operation of a basic NMOS inverter.

   b) Why is a depletion mode MOSFET used in the place of resistor as a pull-up in the inverter circuit ?

10. a) What do you mean by the transfer characteristic of an inverter ?

    b) Explain the characteristic.

    c) Explain the following terms :

       i) Inverter logic threshold voltage

       ii) Gain

       iii) Aspect ratio.

    d) How do the logic threshold voltage and the gain of an inverter behave as increase ? 2 + 4 + 2 + 2 + 2 + 3

11. a) What is the function of a Programmable Logic Array (PLA) ?

    b) Mention its advantages and disadvantages.

    c) Draw the circuit diagram of a PLA and explain its operation.

    d) How are the AND/OR combinational logic requirements realized in the MOS fabrication of the PLA ?

2 + 3 + 6 + 4