Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech/ECE(N)/SEM-5/EC-504A/2012-13

2012

COMPUTER ARCHITECTURE

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

i) The programs which are as permanent as hardware and stored in ROM is known as

a) Hardware b) Software

c) Firmware d) ROM ware.

ii) Primary memory stores

a) Data alone b) Program alone

c) Results alone d) all of these.

iii) The idea of cache memory is based on

a) the heuristic 90-10 rule

b) the property of locality of reference

c) the fact that only a small portion of a program is referenced relatively frequently

d) all of these.

iv) The capacity of a memory unit is defined by the no. of words multiplied by the no. of bits/word. How many separate address and data lines are needed for a memory of 4K × 16 ?

a) 10 address, 16 data lines

b) 11 address, 8 data lines

c) 12 address, 12 data lines

d) 12 address, 16 data lines.

v) Which of the following techniques is hardware based, is used in high performance computer systems to provide certain types of parallelism in instruction processing ?

a) Pipelining b) Networking

c) Multiprocessing d) Multitasking.

vi) The "Instruction Register" in a CPU, holds the instruction which

a) was executed previously

b) is being executed currently

c) to be executed next

d) contain no instruction information at all.

vii) How many memory locations can be accessed with a 6-bit address bus ?

a) 32 b) 128

c) 64 d) 16.

viii) The basic principle of the Von-Neumann computers

a) storing program and data in separate memory

b) using pipeline concept

c) storing both program and data in the same memory

d) using a large no. of registers.

ix) In a microprocessor the address of the next instruction to be executed in stored in

a) stack pointer

b) address latch

c) program counter

d) generated purpose register.

x) Cache memory

a) increase performance

b) reduces performance

c) machine cycle increases

d) none of these.

xi) Instruction cycle is

a) Fetch-decode-execution

b) Decode-fetch-execution

c) Fetch-execution-decode

d) none of these.

xii) Associative memory is a

a) very cheap memory

b) pointer addressable memory

c) content addressable memory

d) slow memory.

xiii) The performance of a pipelined processor suffers if

a) the pipeline stages home different delays

b) consecutive instruction are dependent on each other

c) the pipeline stages share hardware resources

d) all of these.

xiv) Control unit operation is performed by

a) Hardware control only

b) Micro-program control only

c) Hardware or micro-program control

d) none of these.

xv) A 'hit' occurs

a) when word is found in virtual memory

b) when word is found in cache memory

c) when word is not found in virtual memory

d) when word is not found in cache memory.

xvi) Which one of the following is the advantages of virtual memory ?

a) Faster access to memory on an average

b) Process can be given protected address space

c) program larger than the physical memory size can be run

d) none of these.

GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) Write key features of von Neumann architecture of a computer and mention the bottlenecks.

b) How does Harvard architecture differ from von Neumann architecture ? 2 + 1 + 2

3. With diagram, distinguish between DRAM and SRAM.

4. Write three points to differentiate I/O mapped IO and Memory Mapped IO.

5. Write a VHDL programme of 4 bit adder using structural modeling style.

6. Discuss about the different hazards in pipelining.

7. What is virtual memory ? Why is it called virtual ? Write the advantage of virtual memory. 2 + 1 + 2

GROUP – C
(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

8. a) What is Cache memory ? Why is it needed ? Explain the write-through and write-back mechanism. Why is set-associative mapping and technique more advantageous than direct or associative mapping technique ? A computer has 512 kB cache memory and 2 MB main memory. If the block size is 64 bytes, then find out the subfields for

   i) direct mapped cache

   ii) associative

   iii) 8-way set associative cache.

   b) Why memory hierarchy is needed ? 11 + 4

9. a) Describe the function of major components of a digital computer with neat sketch.

   b) Explain the role of an operating system in a computer system.

   c) Explain the relative advantages and disadvantages of parallel adder over serial adder.

   d) What is the difference between carry look ahead adder and carry ripple adder ? 7 + 4 + 2 + 2

10. What do you mean by HDL ? How many hardware models are present in VHDL ? Briefly discuss with proper example of various hardware modeling in VHDL. What do you mean by Top down design and Bottom up design style ?

    1 + 1 + 8 + 5

11. Write short notes on any *three* of the following : 3 × 5

    a) Flynn's classification

    b) DMA processing

    c) Bus organization using tri-state buffer

    d) Magnetic recording

    e) Serial adder

    f) Harvard architecture.