			•••••	
invigilato	r's Signature :			
	CS/B.1		SEM-4/EC-402	2/2010
		2010	ornoruma a	
	DIGITAL ELEC	CTRONIC		
Time Allo	otted: 3 Hours		Full Ma	r ks : 70
	The figures in the	marqin indica	te full marks.	
Candid	ates are required to g			words
Cultula		ar as practica		
	G (Multiple Cho	ROUP - A	restions)	***
	(Multiple Cli	uce type &	ucseions ,	
		-14	for any ten	of the
	oose the correct	aiternatives		$\times 1 = 10$
foll	owing:			
i)	A message bit is generator. So the p			
	a) 0 /	b)	1	
	c) 0 & 1	d)	none of these.	
ii)	What is the decir	nal equivalen	t code for the	following
	canonical?			
	$P(X, Y, Z) = (X + Y + (X^{l} + Y^{l} + Z^{l}))$	Z^{I}) (X + Y ^I + Z	$(X + Y + Z)(X^T)$	$+Y+Z^{I}$
•	a) $m_1 + m_2 + \pi$	$n_3 + m_4$ b)	$m_1 + m_2 + m_4$	+ m ₅
	c) $m_1 + m_3 + m_3$	$n_4 + m_5$ d)	none of these.	
4053		*	[7	Turn over
	Annual Control of the	the second second	***	

iii) If $(128)_{10} = (1003)_b$, the possible base b is

a) 3

b) 4

c) 5

d) 6.

iv) The logical expression $y = \sum m$ (0, 3, 6, 7, 10, 12, 15) is equivalent to

a) $y = \prod M(0, 3, 6, 7, 10, 12, 15)$

b) $\prod M(1, 2, 4, 5, 8, 9, 11, 13, 14)$

c) $\Sigma m(1, 2, 4, 5, 8, 9, 11, 13, 14)$

d) $y = \sum m (0, 3, 6, 7, 10, 12, 15).$

v) The Sop form of logical expression is most suitable for designing logic circuits using only

a) XOR gates

b) AND gates

c) NAND gates

d) NOR gates.

vi) Which of the following flip-flops is used as latch?

a) JK flip-flop

b) D flip-flop

c) RS flip-flop

d) T flip-flop.

vii) The fraction 0.68_{10} is equal to

a) 0.010101_2

b) 0.101_2

c) 0.10101_2

d) 0.10111_2 .

viii) The resolution of a 12-bit D/A converter using a binary ladder with + 10V as the full scale output will be

- a) 2.44 mV
- b) 3.50 mV
- c) 4.32 mV
- d) 5·12 mV.

ix) The initial state of MOD 16 down counter is 0110. The state after 37 clock pulse will be

a) 0000

b) 0110

c) 0101

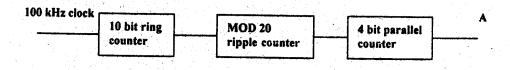
d) 0001.

x) In a D type latch Enable i/p is HIGH, D = 1. The o/p will be

a) 0

- **b**) 1
- c) don't care
- d) blocked.

xi) The frequency of the pulse at point A is



a) 10 kHz

b) 31.25 Hz

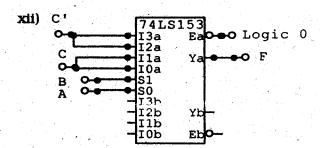
c) 50 Hz

d) 5 kHz.

4053

3

[Turn over



The value of F is

- a) A XOR B
- b) A XNOR C
- c) A XOR C
- d) B XNOR C.
- xiii) Largest negative number that can be represented by 8bit word length in 2's complement system is

xiv) The logic family that gives fastest switching is

a) CMOS

- b) ECL
- c) Schottky TTL
- d) DTL.

GROUP – B (Short Answer Type Questions)

Answer any three of the following.

 $3 \times 5 = 15$

- 2. Draw a BCD adder circuit to add two BCD numbers maximum up to 9. The output of this adder should also be in BCD.
- 3. Design a full subtractor circuit using multiplexer.
- 4. Construct a 2-bit comparator using only decoder.
- 5. a) Define the following terms related with digital IC:
 - i) Noise margin
 - ii) Propagation delay
 - iii) Fan-in & Fan-out.
 - b) Write down the characteristic equation of JK & D Flip-flops.
- 6. What is the main difference between a latch and a flip-flop?

4053

5

[Turn over

GROUP - C

(Long Answer Type Questions)

Answer any three of the following.

 $3\times15=45$

- 7. a) Write down the differences between combinational logic circuit & sequential logic circuit.
 - b) Design a MOD 14 asynchronous UP/DOWN counter with JK flip-flop. 3 + 12
- 8. a) With the help of necessary circuit diagram explain the operation Ramp type ADC.
 - b) A 6-bit R-2R ladder type DAC has reference voltage of 6.5 V.

Find:

- i) resolution in % & volt
- ii) the full scale voltage
- iii) the o/p for the i/p 011100.

10 + 2 + 1 + 2

- 9. a) Discuss the totem pole output configuration of TTL logic family.
 - b) Design a combinational circuit that accepts a BCD as i/p and generates XS3 as an o/p using ROM.
 - c) Design & explain the operation of a 4-bit universal register. 5+5+5

- 10. a) Write down the excitation table of JK and D flip-flops and derive the excitation equation for these two flipflops.
 - b) Design a full subtractor using full adder module and NOT gates.
 - c) Design a full subtractor using 4 to 1 MUX. 6+3+6
- 11. Write short notes on any three of the following: 3×5
 - a) Priority encoder
 - b) Even parity generator and checker
 - c) PLD
 - d) Johnson counter
 - e) Parallel in serial out (PISO) shift register.