ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER – 2008

DIGITAL INTEGRATED CIRCUITS

SEMESTER – 3

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) Gray code of 1011 (binary) =

a) 0101 b) 1101

c) 1110 d) None of these. ☐

ii) An example of reflected code is

a) BCD b) ASCII

c) GRAY d) Hamming code. ☐

iii) The minimum number of NAND gates required to design one X-OR gate is

a) 3 b) 4

c) 5 d) 6. ☐

iv) If $(212)_x = (23)_{10}$, where x is base (+ve integer), then the value of x is

a) 2 b) 3

c) 4 d) 5. ☐

v) Full form of FPGA is

a) Full Programmable Gated Array

b) Field Programmable Gated Array

c) Full Peripheral Gated Array

d) Field Peripheral Gated Array. ☐

vi) The resolution of 8-bit A/d converter is

a) 0.62% b) 0.38%

c) 0.39% d) 1.25%.

vii) One bit even parity detector code fails to detect

a) any even number of error b) any odd number of error

c) both (a) & (b) d) none of these.

viii) What is the word size of 16 × 8 ROM ?

a) 16 b) 8

c) 128 d) None of these.

ix) $(A + B' + A'B)\,C =$

a) 1 b) 0

c) C d) C'.

x) F/F that makes output equals to input after clock is

a) J-K F/F b) D F/F

c) T F/F d) none of these.

xi) 8421 is a

a) weighted code b) non-weighted code

c) complementary code d) none of these.

xii) The characteristic equation of T flip-flop is given by

a) $Q^+ = \bar{T}Q + T\bar{Q}$ b) $Q^+ = \bar{T}\bar{Q} + TQ$

c) $Q^+ = T\bar{Q}$ d) none of these.

xiii) For a n-bit parallel-in-parallel-out shift register we need

a) 1 b) n

c) $2n + 1$ d) $n + 1$

clock pulse/pulses. ☐

xiv) The number of flip-flops required to design a MOD – 18 counter is

a) 3 b) 4

c) 5 d) 6. ☐

xv) A ring counter consisting of 5 flip-flops will have

a) 5 states b) 10 states

c) 32 states d) $(2^5 - 1)$ states. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Given the Boolean function $F = xy + \overline{xy} + \bar{y}z$:

a) Implement it with only OR and NOT gates.

b) Implement it with only AND and NOT gates. $2 \times 2\frac{1}{2}$

3. a) If the solution of the equation $x^2 + 11x + 22 = 0$ are $x = 3, 6$, then determine base of x.

b) What do you mean by arithmetic overflow ? $4 + 1$

4. Design a 2-input NAND gate using CMOS transistors. 5

5. Implement the following function using a Multiplexer :

$F(a, b, c) = \sum m(1, 3, 5, 6)$. 5

6. Use a K-MAP to simplify the following Boolean expression

$F(a, b, c, d) = \sum m(0, 2, 6, 8, 12, 13, 15) + d(3, 9, 10)$

d = don't care (*i.e.* either 1, 0). 5

GROUP – C

(Long Answer Type Questions)

Answer any *three* questions. $3 \times 15 = 45$

7. a) What do you mean by prime-implicant and essential prime-implicant ? $1\frac{1}{2} + 1\frac{1}{2}$

   b) The four-variable function f is given in terms of minterm as

   $f(A, B, C, D) = \sum m(2, 3, 8, 10, 11, 12, 14, 15)$.

   Using Quine McCluskey method, minimize the function in the SOP form. Also give the realization using only two-input NAND gate. 10 + 2

8. A new clocked X-Y flip-flop is defined with two inputs, X and Y in addition to the clock input. The flip-flop function as flows :

   If $XY = 00$ the FF changes state with each clock pulse

   If $XY = 01$ the FF states Q become 1 with the next clock pulse

   If $XY = 10$ the FF states Q become 0 with the next clock pulse

   If $XY = 11$ no changes of state occur with the clock pulse

   a) Write the truth table for the XY flip-flop. 3

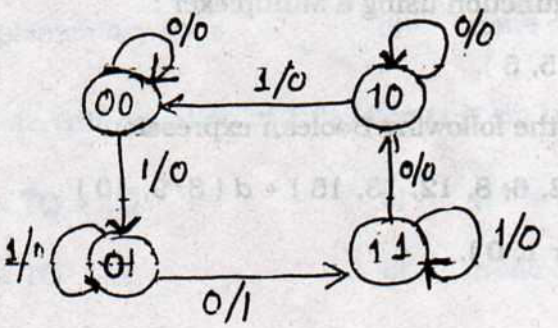
   b) Write the excitation table for the XY flip-flop. 3

   c) It is desired to convert a J-K flip-flop into the X-Y flip-flop by adding some extra gates, if necessary. Draw a circuit to show how you will implement the XY flip-flop using a J-K flip-flop. 9

9. a) What are the differences between a latch and a flip-flop ? 2

   b) What is Johnson counter ? State the advantages and disadvantages of Johnson counter. 1 + 2

   c) Design a sequential circuit that implement the following state diagram. Use all D flip-flops for the design. 10



10. a) Design a compactor circuit to output logic-1 when a 4-bit binary number X satisfies the condition $4 \leq X \leq 12$. 8

b) Design a binary multiplier circuit to multiply two 2-bit numbers. Use a suitable decoder and logic gates. Assume that all the outputs of the decoder are active low. 7

11. a) Implement a 16-to-1 MUX using two 8-to-1 MUXs. 6

b) Design a Gray code to binary converter using suitable logic gates. 7

c) How can a decoder be used as a DEMUX ? 2

12. Write short notes on any *three* of the following : 3 × 5

a) PLD

b) Even Parity checker and generator

c) EEROM

d) Successive Approximation register

e) Hamming code.

END