MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : ES-201

BASIC ELECTRICAL & ELECTRONIC ENGINEERING - II

Time Allotted : 3 Hours   Full Marks : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own
*words as far as practicable.*

PART - I (Electrical)

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *five* of the following : $5 \times 1 = 5$

   i) Iron losses in a *dc* machine are independent of variation in

      a) frequency   b) load

      c) voltage   d) flux density.

   ii) A series motor will run at very high speed when

      a) the load is increased

      b) the field is opened

      c) the armature is opened

      d) the load is removed.

   iii) A transformer core is laminated to

      a) reduce hysteresis loss

      b) reduce eddy current loss

      c) reduce copper losses

      d) reduce all losses mentioned above.

   iv) The effective capacitance between terminals A & B is given by
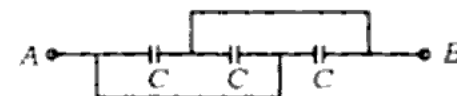
      a) $2C$ b) $3C$

      c) C d) $C/3$.

   v) In a 3-phase balanced system, the line voltage makes an angle with phase voltage. The value of the angle is

      a) $30°$ b) $60°$

      c) $90°$ d) $120°$.

   vi) If the induction motor is supplied with voltage having frequency f and s is the slip of the motor, then the frequency of rotor current is given by

      a) sf b) f

      c) $sf + f$ d) $sf - f$.
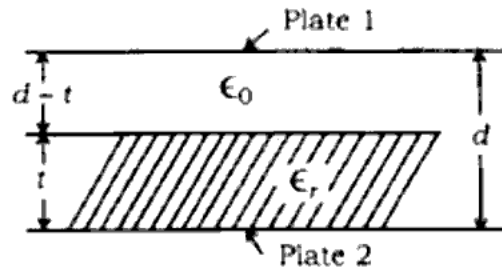
GROUP – B

(Short Answer Type Questions)

Answer any *two* of the following. $2 \times 5 = 10$

2. Show that if a dielectric of thickness t and with the same area as the plates of parallel plate capacitor is

introduced, the capacitor would then have, the

capacitance $C = \dfrac{\epsilon_0 A}{d - t\dfrac{t}{\epsilon_r}}$.

Plate 1

ϵ_0

$d - t$

ϵ_r

d

t

Plate 2

3. A star connected three-phase load draws a current of 15A at a lagging power factor of 0·9 from a balanced 440 V, 50 Hz supply. Find the circuit elements in each phase of the elements connected in series.

4. What do you mean by the term 'back emf' ? Derive the expression of torque of a separately excited dc motor.

$$1 + 4$$

5. Explain the working of a transformer on load.

GROUP - C
(Long Answer Type Questions)

Answer any *two* of the following. $2 \times 10 = 20$

6. a) Explain why the open circuit test on a transformer is conducted at a rated voltage.

b) The following test data were obtained on a 20 kVA, 50 Hz, 1 ph, 2000/200 V transformer.
No. load test : 200 V, 1 A, 120 W
Short circuit test : 60 A, 10 A, 300 W.
Find —

i) efficiency of the transformer at $\frac{1}{2}$ of the full load and 0·8 p.f. lagging.

ii) maximum efficiency and the load at which it occurs. $2 + 8$

7. a) What is commutation in a dc machine ?

b) A 4-pole 240 V dc shunt motor has armature and shunt field resistances of 0·24 Ω and 240 Ω respectively. It takes 20 A from a 240 V dc supply while running at a speed of 1000 rpm. Find — (i) field current, (ii) armature current, (iii) back *emf* (iv) torque developed in Nm. $2 + 8$

8. a) Derive the exact equivalent circuit of a 3-phase induction motor on per phase basis.

b) Discuss voltage control method of speed control of induction motor. $5 + 5$

9. Write short notes on any *two* of the following : 2×5

a) Speed control of *dc* motor by armature voltage control

b) General single line diagram of an electrical power system from power generation to distribution

c) Torque-speed characteristics of a 3-phase induction motor

d) 3-point starter.

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PART - II (Electronics)
GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *five* of the following : $5 \times 1 = 5$

   i) JFET is a
      a) voltage controlled voltage source
      b) voltage controlled current source
      c) current controlled voltage source
      d) current controlled current source.

   ii) When the gate source voltage of N-channel JFET is more negative, the drain current
      a) increases
      b) decreases
      c) remains constant
      d) may increase or decrease.

   iii) $|AB| = 1$
      a) sustained oscillations
      b) exponentially decay
      c) exponentially increased
      d) none of these.

   iv) Which of the following statements is/are correct in regard to excess 3 codes ?
      a) It is a BCD code
      b) It is an unweighted code
      c) It is a self-complementing code
      d) All of these.

   v) In inverting amplifier circuit if input feedback resistances are 1 kΩ and 2 kΩ respectively, i/p voltage is 3 V and power supply voltage is ± 6V, then the o/p voltage of an Op-Amp is
      a) – 6V   b) + 6V
      c) – 9V   d) ± 9V.

   vi) The minimum number of 2-input NAND gates required to implement the XOR operation of 2 variables is
      a) 5   b) 4
      c) 6   d) 2.

GROUP – B
(Short Answer Type Questions)

Answer any *two* of the following. $2 \times 5 = 10$

2. Why do *p*-channel enhancement mode MOSFETs require threshold voltage ? Explain with suitable diagram.

3. What is oscillator ? Which type of feedback is used to design an oscillator ? Draw the block diagram of an oscillator and explain its principle of operation. $1 + 1 + 3$

4. Identify the circuit and calculate the output voltage when $V_1 = 350$ mV and $V_2 = 200$ mV. $1 + 4$
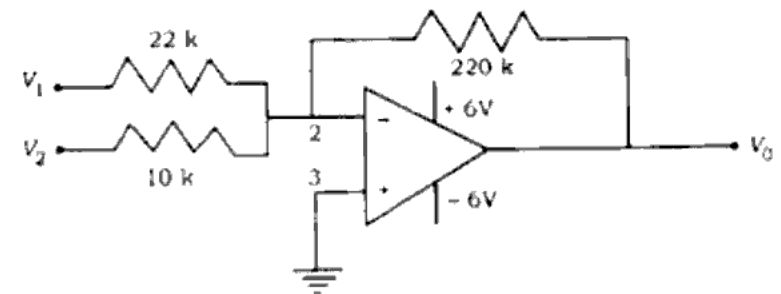
5. a) Perform the following number conversions :
      i) $(456)_{16} = (?)_8$
      ii) $(1010101)_2 = (?)_{16}$

   b) Realize the Boolean expression using minimun number of NAND gates :
      $$Y = (A + \overline{B})(\overline{A} + B)$$ $3 +$

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GROUP – C
(Long Answer Type Questions)

Answer any *two* of the following. $2 \times 10 = 20$

6. a) Explain the basic operation of n-channel JFET with suitable diagram.

    b) What are the differences between MOSFET and JFET ?

    c) An n-channel JFET has $I_{DSS} = 12$ mA and pinch-off voltage is -4V, find the I_D for $V_{GS} = -2$V. If the g_{mo} of a JFET with same L_{DSS} at $V_{GS} = 0$ is 4 milli-mho, find pinch-off voltage. $4 + 2 + 4$

7. a) What is negative feedback ? Draw the block diagram of different types of feedback topologies.

    b) An amplifier has a voltage gain of -100. The feedback ratio is -0.04. Find (i) voltage gain with feedback, (ii) amount of voltage gain, (iii) the output voltage of the feedback amplifier for an input voltage of 40 mV. $2 + 4 + 4$

8. a) Write down De Morgan theorem.

    b) Perform the following number conversion :

    i) $(11001 \cdot 101)_2 = (?)_8$

    ii) $(284 \cdot 56)_{10} = (?)_2$

    c) Realize the Boolean expression using basic gates.
    $Y = B(\overline{A}C + A\overline{C}) + A\overline{B}C$ $2 + 4 + 4$

9. Write short notes on any *two* of the following : 2×5

    a) Summing Amplifier

    b) CMOS

    c) Different parameters of JFET

    d) Race around condition in JK latch.