MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

CS-502

MICROPROCESSORS AND MICROCONTROLLERS

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.
All symbols are of usual significance.

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. 10×1 = 10

(i) The instruction MOV A,B belongs to

(A) immediate addressing (B) directing addressing
(C) implied addressing (D) register addressing

(ii) In 8085, TRAP is

(A) always maskable
(B) can't interrupt a service sub-routine
(C) use for temporary power failure
(D) lowest priority interrupt

(iii) How many hardware interrupt requests a single interrupt controller IC8259A can process?

(A) 8 (B) 15
(C) 16 (D) 64

(iv) When the instruction LHLD executed, the number of T-states required are

(A) 10 (B) 14
(C) 13 (D) 15

(v) In DMA operation data transfer takes place between

(A) memory and CPU (B) CPU and I/O
(C) I/O and memory (D) Different CPUs

(vi) For 8255 PPI, the bi-directional mode of operation is supported in

(A) mode-1 (B) mode-2
(C) mode-0 (D) none of these

(vii) The interrupt masks in 8085 can set or reset by the instruction

(A) EI (B) DI
(C) RIM (D) SIM

(viii) The vector address corresponding to software interrupt command RST7 in 8085 microprocessor is

(A) 0017 H (B) 0027 H
(C) 0038 H (D) 0700 H

(ix) How many flag registers are in 8086?

(A) 9 (B) 8
(C) 6 (D) 5

(x) The instruction XCHG exchange the content of

(A) Accumulator and H (B) BC pair and HL pair
(C) DE pair and HL pair (D) HL pair and memory

(xi) RAL/RAR is useful for

(A) DMA controlling (B) Serial data transfer
(C) Decimal adjust operation (D) None of these

(xii) The number of register pairs of 8085 microprocessor are

(A) 3 (B) 4
(C) 2 (D) 5

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. Draw the timing diagram of LXI H, 2051 instruction.

3. What is the function of DAD instruction in 8085 processor? Write the output if input is F0:

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LXI H, 2050
MOV A, M
CMA
ADI 01
STA 2060
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4. Write the control word format of 8255 PPI in I/O mode.

5. What is the difference between SIM and RIM instruction?

6. Explain the memory segmentation scheme with reference to 8086 microprocessor.

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) Distinguish between Software and Hardware interrupt in 8085. 5+5+5
   (b) What is memory interfacing? Write the difference between memory mapped I/O and peripheral mapped I/O?
   (c) Write an ALP to find out the largest number from a given array of 10 numbers.

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8. (a) What do you mean by subroutine? Briefly discuss the sequence of events that takes place while executing CALL instruction. 5+5+5
   (b) What is meant by pipeline in 8086? Show the neat sketch for this process.
   (c) Write an ALP to convert Binary to ASCII number.

9. (a) Describe the operation of transmitter and receiver section of 8251. 5+5+5
   (b) Briefly describe the DMA operation. Which IC is used for this purpose?
   (c) What are the differences between a micro-processor and a micro-controller? Discuss the memory organization of 8051 microcontroller.

10. (a) What do you mean by BSR control word in 8255? Describe the different modes of operation of 8255 PPI. 5+5+5
    (b) What is the function of program counter and stack pointer in 8085 Processor? Write the function of HOLD and HLDA in 8085 Processor.
    (c) Explain the need to demultiplex $AD_7 - AD_0$ of 8085 Processor. Draw the timing diagram of memory fetch operation.

11. Write short notes on any *three* of the following: 3×5
    (a) Synchronous and Asynchronous communication.
    (b) DMA controller
    (c) 8259 interrupt controller
    (d) Status and control signals of INTEL 8085
    (e) RIM and SIM