Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH (IT/EEE)/SEM-4/CS-404/2010

2010

COMPUTER ORGANIZATION AND ARCHITECTURE

Time Allotted : 3 Hours | **Full Marks : 70**

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) Periodic Refreshing is needed in

   a) ROM b) EPROM

   c) SRAM d) DRAM.

   ii) The 2's complement representation of (– 24) in a 16-bit micro-computer is

   a) 0000 0000 0001 1000

   b) 1111 1111 1110 0111

   c) 1111 1111 1110 1000

   d) 0001 0001 1111 0011.

iii) Which of the following addressing modes is used in 'Push B' ?

a) Immediate b) Register

c) Direct d) Register Direct.

iv) Which of the following I/O mechanisms requires the least hardware support ?

a) Polled b) Interrupt driven

c) DMA d) Memory-mapped.

v) The basic principle of Von Neumann computer is

a) storing program and data in separate memory

b) using pipeline concept

c) storing program and data in the same memory

d) using a large number of register.

vi) The performance of pipelined processor suffers if

a) the pipeline stages have different delays

b) consecutive instructions are depends on each other

c) the pipeline stages share H/W resource

d) all of these.

vii) Associative memory is a

a) very cheap memory

b) pointer addressable memory

c) content addressable memory

d) slow memory.

viii) How many RAM chips of size (256 K × 1 bit) are required to build 1 M byte memory ?

a) 24 b) 10

c) 32 d) 8.

ix) A ripple carry adder requires time in the order of

a) linear time (O (N))

b) constant

c) (O (log (N)))

d) (O (N log (N))).

x) How many address bits are required for a 1024 × 8 memory ?

a) 5 b) 10

c) 1024 d) None of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Using 8-bit 2's complement integers, perform the following computations :

   i) $26 - (-4)$

   ii) $1 - 7$.

3. Explain the following with respect to pipelined architecture :

   Speed-up, throughput, efficiency.

4. Explain the working (with a suitable example) of a carry look ahead adder.

5. Explain how a RAM of capacity 2 k bytes can be mapped into address space (1000) H to (17 FF) H of CPU having a 16-bit address lines. Show how the address lines are decoded to generate the chip select condition for the RAM.

6. What is Cache memory ? What are the different mechanisms of writing into it ? Briefly describe.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) What do you mean by Instruction Cycle, Machine Cycle and T-States ?

   b) Compare RISC with CISC.

   c) What do you mean by Von Neumann bottleneck ? Specify possible strategies for handling it. 6 + 5 + 4

8. a) With the help of a block diagram, describe the components of a Micro-programmed Control Unit. Discuss the advantages and disadvantages of horizontal and vertical micro-instructions. What is a micro-program sequencer/control ?

   b) What is bus arbitration ? Explain clearly.

   (4 + 4 + 2) + 5

9. a) A CPU has 32-bit memory address and a 256 kB cache memory. The cache is organized as a 4-way set associative cache with cache block size of 16 bytes.

   i) What is the number of sets in the cache ?

ii) What is the size (in bits) of the tag field per cache block ?

iii) What is the number and size of comparators required for tag matching ?

iv) How many address bits are required to find the byte offset within a cache block ?

b) What are the widths of data bus and address bus for (4096 × 8) memory ? What do you mean by program status word ? Define content addressable memory. What is control word ? (4 × 2) + (2 + 2 + 2 + 1)

10. a) Draw and explain the flowchart for division of two binary numbers using Non-Restoring algorithm. Use the example of 8 to be divided by 3.

b) Explain the difference between instruction pipeline and arithmetic pipeline.

c) Why is Carry Look-Ahead Adder (CLA) called a fast parallel adder ? What will be the delay if you construct a 16-bit CLA using 4-bit CLA blocks ?

8 + 4 + (2 + 1)

11. a) What is SRAM ?

b) What is DMA ?

c) What is the bandwidth of a memory system that transfers 128-bit data per reference having a speed of 20 nano sec per operation ?

d) How do the following influence the performance of a Virtual Memory System ?

i) Size of page

ii) Replacement policies of pages.

e) What is a floating point number ? Write down the steps to subtract 110·101101 from 10110·1110.

2 + 3 + 3 + 4 + 3