Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech (EIE)/SEM-3/EC-302(EI)/2010-11

2010-11

DIGITAL INTEGRATED CIRCUITS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) ASCII code is

      a) 4 bit code

      b) 6 bit code

      c) 7 bit code

      d) 8 bit code.

   ii) The minimum of bits in the BCD representation of the decimal number 25 is

      a) 5 b) 4

      c) 3 d) 6.

iii) Excess-3 code representation of decimal 59 is

a) 01100010 b) 00111110

c) 10001100 d) none of these.

iv) Hexadecimal equivalent of $(26.25)_{10}$ is

a) A6.4 b) 1A.4

c) FA.4 d) none of these.

v) The number of 1's in the binary representation of the decimal number 11 is

a) 5 b) 4

c) 3 d) none of these.

vi) With the same number of flip-flops where the Johnson counter has N states and the ring counter has M states are

a) $N > M$ b) $N = M$

c) $N < M$ d) none of these.

vii) The minimum number of NOR gates required to design one XOR gate is

a) 5 b) 4

c) 7 d) none of these.

viii) A decoder with enable input can be used as

a) encoder b) parity generator

c) multiplexer d) demultiplexer.

ix) The logic family that gives fastest switching is

a) CMOS

b) ECL

c) Schottky TTL

d) Low power Schottky TTL.

x) A 64:1 MUX consists of

a) 54 no. of 2:1 MUX

b) 63 no. of 2:1 MUX

c) 45 no. of 2:1 MUX

d) 36 no. of 2:1 MUX.

xi) How many RAM chips of size (256k*1bit) are required to build 1M byte memory ?

a) 24 b) 10

c) 32 d) 8.

xii) Which one is the fastest logic in logic families ?

a) RTL b) TTL

c) ECL d) none of these.

xiii) Binary division 10010.1011 ÷ 11.01 yields

a) 110.11 b) 100.11

c) 101.10 d) 101.11

xiv) The value of 2^5 in octal system is

a) 40 b) 20

c) 400 d) 200.

xv) Excess-3 code is also known as

a) weighted code

b) self complementing code

c) algebraic code

d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) Design half-adder circuit using NAND gate only.

b) Design full adder circuit using half-adder and OR gate only.

3. Draw the output waveform of J-K flip-flop for input sequence J = 1011010 and K = 0110110, if

a) the flip-flop is positive edge-triggered

b) the flip-flop is negative edge-triggered.

4. Explain BCD addition with proper diagram and proper example.

5. a) Design 8:1 MUX using 4:1 MUX and 2:1 MUX.

   b) What is priority encoder ?

6. Prove that :

   a) $A+\overline{A}B+\overline{A}\,\overline{B}\,\overline{C}\,D+\overline{A}\,\overline{B}\,\overline{C}\,D=A+B+C+D$

   b) $AB+\overline{AC}+A\overline{B}C(AB+C)=1$

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Simplify the following Boolean function using Quine - McCluskey method :

   $Y(A, B, C, D) = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15) + d(4, 8, 11)$

   b) Draw the logic circuit of S-R flip-flop using *D* flip-flop.

   c) What are the advantages of *D* flip-flop over S-R flip-flop ? $8 + 5 + 2$

8. a) Using the K-map method, simplify the following Boolean function and obtain

   i) SOP &

   ii) POS expressions for

   $Y = \Sigma m\ (0, 2, 3, 6, 7) + \Sigma d\ (8, 10, 11, 15)$

   b) Design a Mod-5 synchronous counter using J-K flip-flop.

   c) What do you mean by Race-around condition ? 6 + 7 + 2

9. a) Implement a full-subtractor circuit using PLA having three inputs and two outputs.

   b) Design 8:1 Multiplexer using NAND gates only.

   c) Implement the following function using 3-to-8 line decoder :

   $Y(A, B, C) = \Sigma m\ (4, 5, 6, 7)$ 6 + 6 + 3

10. a) Design a Gray code to binary converter using suitable logic gates.

    b) Explain addition and subtraction for 1's complement using 4-bit parallel adder.

c) What are the differences between a latch and a flip-flop ?

d) What are the differences between Edge-triggered and level-triggered flip-flop ? 7 + 4 + 2 + 2

11. Answer any *three* of the following : 3 × 5

a) Even parity checker and generator

b) Successive approximation register type ADC

c) PAL

d) BCD to Excess-3 converter

e) R-2R ladder type D/A converter

f) Universal gate.