Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH/ECE(O)/SEM-5/EC-503/2012-13

2012

COMPUTER ARCHITECTURE AND ORGANIZATION

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) The logic circuit in ALU is
      a) entirely combinational
      b) entirely sequential
      c) combinational cum sequential
      d) none of these.

   ii) Physical memory broken down into groups of equal size is called
      a) page b) tag
      c) block d) index.

   iii) Principle of the locality justifies the use of
      a) interrupts b) DMA
      c) polling d) cache memory.

iv) A 'hit' occurs

a) when a word is found in virtual memory

b) when a word is found in cache memory

c) when a word is not found in virtual memory

d) when a word is not found in cache memory.

v) A digital computer has a common bus system for 16 registers of 32-bits each. How many MUX are needed and what will be the size of each MUX ?

a) 32, 16 b) 16, 32

c) 8, 16 d) 16, 8.

vi) Number of transistor in a CMOS static RAM cell is

a) 1 b) 4

c) 6 d) none of these.

vii) CPU consists of

a) main memory and ALU

b) main memory, ALU and control unit

c) cache memory ALU and control unit

d) ALU, control unit and registers.

viii) Which operating system supports multiple CPUs through shared main memory ?

a) Multi programming OS

b) Real-time OS

c) Distributed OS

d) Multiprocessing OS.

ix) Micro operation in computers is an operation

a) In ALU

b) on stored data in register

c) in control unit

d) performed by the operating system.

x) asynchronous data transfer

a) can be initiated by source or destination device

b) is initiated by source device

c) is initiated by destination device

d) is controlled by clock and can be initiated by source or destination device.

xi) How many memory locations can be addressed by a 32-bit computer ?

a) 64 kB b) 32 kB

c) 4 GB d) 4 MB.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Draw the control cir uit for the following RTL :

$T_1 : A \leftarrow B$

$T_2 : A \leftarrow C$

3. With a diagram distinguish between DRAM and SRAM.

4. What s locality of reference ? What is memory mapping ? Why is it needed ? 2 + 1 + 2

5. a) Briefly explain IEEE 754 standard format for floating point representation in single precision.

b) Write $+ 7_{10}$ in IEEE 754 floating point representation in double precision. 3 + 2

6. What are the different types of interrupts ? Give an example. What is programmed I/O technique ?

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Using Booth's algorithm multiply (– 9) and (– 3). 10
   b) Show how the non-restoring method is deduced from restoring division method. 3
   c) Write down the steps of the algorithm of addition or subtraction of two floating point numbers. 2
8. a) Discuss the principle of carry look ahead adder and design a 4-bit CLA adder and estimate speed enhancement with respect to ripple carry add r. 5 + 4
   b) Briefly state the relative advantages and di advantages of parallel adder over serial adder. 3
   c) $X = (A + B) \times C$
   Write down the Zero addr ss and one address instruction for the expression. 3
9. Write short notes on any *three* f the following : 3 × 5
   a) Magnetic recording
   b) Adder-subtractor circuit
   c) Bus organization using tri-state buffer
   d) DMA
   e) Addressing moods.
10. a) What do you mean by logical address space and physical address space ?
   b) Explain wi h an example how logical address is converted into physical address ? Explain how page replacements take place.
   c) Write the advantages of virtual memory system.
   d) i) How many address lines are present in a 256 K × 8 RAM ?
      ii) How many such RAMs will be required to construct 1M × 32 memory bank ?
      iii) How many such RAMs will be required to construct 512 K × 32 memory bank ?
      2 + 4 + 3 + (3 × 2)