Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH(CSE-OLD)/SEM-3/CS-303/2011-12

2011
COMPUTER ORGANIZATION

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : 10 × 1 = 10

   i) The principle of locality justifies the use of

   a) Interrupt b) Polling

   c) DMA d) Cache memory

   ii) Instruction cycle is

   a) fetch-decode-execution

   b) fetch-execution-decode

   c) decode-fetch-execution

   d) none of these.

   iii) Subtractor can be implemented using

   a) adder b) complementer

   c) both (a) and (b) d) none of these.

   iv) How many RAM chips of size (256 KX 1 bit) are required to built 1M Memory ?

   a) 24 b) 10

   c) 32 d) 8.

v) Maximum n bit 2's complement number is

a) 2^n b) $2^n - 1$

c) $2^{n-1} - 1$ d) cannot be said.

vi) Micro instruction are kept in

a) Main memory b) Control memory

c) Cache memory d) None of these.

vii) Physical memory broken down into groups of equal size is called

a) Page b) Tag

c) Block d) Index.

viii) Overflow occurs when

a) data is out of range b) data is within range

c) both (a) and (b) d) none of these.

ix) The minimum number of operands with any instruction is

a) 1 b) 0

c) 2 d) 3.

x) The basic principle of the von Neumann computer is

a) storing program and data in separate memory

b) using pipeline concept

c) storing both program and data in the same memory

d) using a large number of register.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) What is tri-state buffer ? Construct a single line common bus system using tri-state buffer.

   b) What are guard bits ? (1 + 2) + 2

3. Describe stack based CPU.

4. a) Write $+7_{10}$ in IEEE 32 bit format.

   b) Convert IEEE 32-bit format 40400000_{16} in decimal value.

   c) What is the role of an Operating System ? 2 + 2 + 1

5. Evaluate the following arithmetic expression into three-address, two-address, one-address, zero-address instruction format :

   X = (A + B) * C

6. a) Explain the difference between full associative and direct mapped cache Mapping approaches.

   b) What are "Write through" and write back " policies in cache ? 3 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. What is virtual memory ? Why is it called virtual ? What are the different address spaces ? Explain with example how logical address is converted into physical address and also explain how page replacements take place. Explain the instruction cycle with a neat diagram. Explain the disadvantages of stored program computer. 2 + 2 + 4 + 5 + 2

8. Show the memory map with a CPU having 8 bit data bus and 16 bit address bus requiring four RAM chips of size 256 × 8 bit each and a ROM chip of 512 × 8 bit size. Explain the memory map. Among dynamic MOS cell and static MOS cell which one is used for the construction of cache memory and which one for main memory ? What is destructive readout and non-destructive readout memory ? 7 + 4 + 4

9. Explain with a neat diagram circuit diagram of static MOS cell and dynamic MOS cell. Describe memory reading and writing process. What is daisy chaining ? Discuss the data transfer using the DMA, 2 + 7 + 2 + 4

10. Discuss various addressing modes with examples. Write a program that can evaluate the expression $X = A - B + C - D$ in a single accumulator processor. Assume that the processor has load, store, sub and add instructions. What is the difference between zero address and one address instructions. Write a short note on overflow detection with examples. What are status flags ?

5 + 3 + 2 + 5

11. Write short notes on any *three* of the following : 3 × 5

    a) Carry look ahead adder

    b) Design of a 4-bit adder-sub tractor circuit

    c) Tri-state buffer

    d) Booth's algorithm for multiplication

    e) Cache memory.