ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER - 2006

DIGITAL ELECTRONICS AND LOGIC DESIGN

SEMESTER - 3

Time : 3 Hours] [Full Marks : 70

Group - A

(Multiple Choice Questions)

1. Choose the correct alternatives for any *ten* of the following questions : 10 × 1 = 10

a) A full adder circuit can be designed using

i) a half adder & an OR gate

ii) a half adder & an AND gate

iii) two half adders & an OR gate

iv) none of these. ☐

b) The fastest logic family is

i) TTL ii) CMOS

iii) RTL iv) ECL. ☐

c) For a parallel in parallel out shift register we need

i) 1 ii) n

iii) 2n + 1 iv) n + 1

clock pulse/pulses. ☐

d) The number of Flip-Flops required to design a MOD-18 counter is

i) 3 ii) 4

iii) 5 iv) 6. ☐

e) The maximum positive number that can be represented in 1's complement representation is

i) $2^{n-1} - 1$ ii) $1 - 2^{n-1}$

iii) $-(2^{n-1} - 1)$ iv) 2^{n-1}. ☐

f) Flip-Flop has

i) one stable state ii) two stable states

iii) no stable state iv) none of these.

g) The fastest ADC is

i) dual slope ii) successive approximation

iii) parallel comparator iv) none of these.

h) The minimum number of NAND gates required to implement an EX-OR gate is

i) 2 ii) 3

iii) 4 iv) 5.

i) According to Boolean algebra which of the following relations is not valid ?

i) $X (Y, Z) = (XY) Z$ ii) $X (Y + Z) = XY + XZ$

iii) $X + XZ = X$ iv) $X (X + Y) = 1$.

j) The figure of merit of a logic family is given by

i) gain bandwidth product

ii) propagation delay time × power dissipation

iii) fan-out × propagation delay time

iv) noise margin × power dissipation.

k) PROMs are used primarily for

i) data storage

ii) temporary program and data storage

iii) they are inexpensive

iv) permanent program & data storage.

l) The decimal 37 is represented in BCD by

i) 100101 ii) 00111011

iii) 00100101 iv) none of these.

Group - B

(Short Answer Questions)

Answer any *three* questions. $3 \times 5 = 15$

2. Perform the arithmetic operation $(-25)_{10} + (-15)_{10}$ in sign 2's complement method, Assume 1-bit sign and 6-bit information.

3. Minimize the following expression using K-map and realize the simplified expression using NAND gates only.

   $G(A, B, C, D) = \Sigma (1, 2, 3, 5, 6, 11, 12) + D(7, 8, 10, 14)$

4. Implement a full adder circuit using decoder.

5. Implement a clocked JK flip-flop using NAND gates only.

6. Implement the following function using 8 : 1 MUX :

   $F(A, B, C, D) = \Sigma (0, 2, 4, 8, 9, (10, 11, 12, 13, 14, 15)$

Group - C

(Long Answer Questions)

Note : Answer any *three* of the following questions. $3 \times 15 = 45$

7. a) Distinguish between ROM, PLA and PLD's as elements realising Boolean functions. 6

   b) Design a combinational circuit using an 8×4 ROM that accepts a 3-bit number and generates an output binary number equal to the square of the input number. 6

   c) Draw logic diagram of Master/Slave JK flip-flop. Why is it called so ? 3

8. a) Write down the excitation table of JK and D flip-flops. Derive the excitation equations for these two flip-flops. 3 + 3

   b) Design a 4-bit Up/Down asynchronous counter using all JK flip-flops and other necessary logic gates. Use one direction control input M. If M = 0, the counter will count up and for M = 1 the counter will count down. 9

9. a) Describe the operation of successive approximation type A to D converter. How many clock pulses are required in worst case for conversion for an 8-bit SAR ? Define quantizing error for an ADC. 6 + 1 + 1

b) Draw a neat diagram for a R-2R ladder type DAC. What is linearity error and offset error in a DAC ? 5 + 1 + 1

10. a) Draw the circuit for a four-bit Johnson counter using D flip-flops and explain its operation. Draw the timing diagram for this 4-bit Johnson counter. How does this timing diagram differ from that of a Ring counter ? 8 + 2 + 2

b) Perform the conversion from D flip-flop to JK flip-flop. 3

11. Write short notes on any *three* from the following : 3 × 5 = 15

a) Content Addressed Memory

b) Tri-state gates in TTL family

c) BCD-to-7 segment decoder/driver

d) Data lock-out in a counter.