CS/B.Tech(CSE/TT)(N)/SEM-3/CS-301/2011-12 2011

ANALOG & DIGITAL ELECTRONICS

Time Allotted: 3 Hours

Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A (Multiple Choice Type Questions)

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1.	Choose the correct alternatives for any ten of the following:							
					$10 \times 1 = 10$			
	i)	Maximum efficiency of transformer coupled class A						
		power amplifier is						
		a)	78.5%	b)	50%			
		c)	25%	d)	100%.			
	ii)	A 2	-transistor class E	3 power	amplifier is commonly			
		called						
		a)	push-pull	b)	dual			
		c)	differential	d)	none of these.			
	iii)	Clas	ss C amplifiers are ι	used as				
		a)	AF amplifiers	b)	detectors			
		c)	RF amplifiers	d)	none of these.			
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	iv)	A bistable multivibrator circuit has						
		a)	two unstable states	b)	two stable states			
		c)	quasi-stable states	d)	none of these.			
	v)	A Wien-bridge oscillator has a frequency						
		a)	$1/2\pi\sqrt{RC}$	b)	1/√RC			
		c)	1/2π RC	d)	none of these.			
	vi)	Which of the following oscillators is used at audifrequency?						
		a)	Crystal Oscillators					
		b)	Wien-bridge Oscillator					
		c)	RC Phase-shift Oscillator					
		d)	Colpitt's Oscillator.					
	vii)	The minimum no. of NAND gates required to design one						
	full adder circuit is							
		a)	6	b)	5			
		c)	10	d)	9.			
	viii)	The race-around condition does not occur in flip-flop						
		a)	J-K	b)	Master Slave			
		c)	T	d)	None of these.			
ix) The decimal equivalent of (1111100100) 2 is								

568

b)

d)

x) The J-K flip-flop has

998

996

a)

c)

a) no stable state

b) two stable states

None of these.

c) one stable state

d) none of these.

xi)	The	decimal	equivalent	of ((A0F9.0EB)) ₁₆ is
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- a) 44297.0967
- b) 67902.8796
- 41209.0572 c)
- d) none of these.
- xii) How many full adders are required to construct m bit parallel adder?
 - m/2a)

b) m-1

c) m d) m + 1.

GROUP - B

(Short Answer Type Questions)

Answer any three of the following.

 $3 \times 5 = 15$

- 2. Simplify the following Boolean function into
 - Sum of product form i)
 - Product of sum form: ii)

$$F(A, B, C, D) = \Sigma(0, 1, 2, 5, 8, 9, 10).$$
 $2\frac{1}{2} + 2\frac{1}{2}$

$$2\frac{1}{2} + 2\frac{1}{2}$$

Implement the following using 3.

8: 1 MUX,
$$F(A, B, C, D) = \Sigma(0, 2, 4, 6)$$
.

- Explain the operation of successive approximation ADC with 4. diagram.
- 5. Draw and explain the operation of astable multivibrator using 555 Timer.
- Define upper threshold, lower threshold, hysteresis voltage 6. and centre voltage related to a Schmitt trigger circuit.

GROUP - C

(Long Answer Type Questions)

Answer any three of the following. $3 \times 15 = 45$ 7. Design an asynchronous 3-bit up-down counter using a) J-K flip-flop which counts up when external signal M =1 and counts down when M = 0.

With a neat circuit diagram, explain the operation of a b) 4-bit Johnson counter implemented using D flip-flop.

7 + 8

Design full subtractor uisng 4:1 multiplexers. 8. a)

Describe the operation of a bidirectional universal shift b) ١ register

(with parallel load) with a neat diagram. 6 + 9

- Draw the circuit diagram of a transformer coupled 9. a) Class A power amplifiers and explain its operation.
 - b) Calculate the total efficiency of this amplifier.
 - c) What is cross-over distortion found in Class B power amplifiers? How it can be eliminated? 5 + 4 + 6
- 10. a) What are the conditions necessary for the generation of oscillation?
 - b) Explain the operation of a Wien Bridge oscillator using Opamp with a circuit diagram.
 - Derive an expression for its frequency of oscillation. c)

4 + 6 + 5

11. Write short notes on any three of the following: 3×5

- a) Ring Counter
- Odd Parity Generator and Checker b)
- c) BCD adder
- d) R-2R ladder DAC.
- e) CMOS Logic family
- Data lock-out in a counter. f)