Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH(CSE)/SEM-4/CS-403/2011

2011

ADVANCED COMPUTER ARCHITECTURE

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alte nat ves for any *ten* of the following :

10 × 1 = 10

i) Consider th high speed 40 ns memory cache with a successful hit ratio of 80 ns. The regular memory has an access time of 100 ns. What is the effective access time for CPU to access memory ?

a) 52 ns b) 60 ns

c) 70 ns d) 80 ns.

ii) Assume a system where main memory is of size 16 K × 12 and cache memory is of size 1K × 12. For a direct mapping ststem which statement is correct ?

a) Tag field is 9 bits and index field is 6 bits

b) Tag field is 4 bits and index field is 10 bits

c) Tag field is 7 bits and index field is 8 bits

d) None of these.

iii) The advantage of RISC over CISC is that

a) RISC can achieve pipeline segments, requiring just one clock cycle

b) CISC uses many segments in its pipeline with the longest segment requi ing two or more clock cycle

c) Both (a) & (b)

d) None of these.

iv) The expressio for Amadahl's law is

a) $S(n) = 1/f$ where $n \rightarrow \infty$

b) $S(n = f$ where $n \rightarrow \infty$

c $S(n) = 1/T$ where $n \rightarrow \infty$

d) None of these.

v) The vector stride value is required to

a) deal with the length of vectors

b) find the parallelism in vectors

c) access the elements in multi-dimensional vectors

d) execute vector instruction.

vi) Which MIMD systems are best according to scalability with respect to the number of processors ?

a) Distributed memory computers

b) ccNUMA systems

c) nccNUMA systems

d) Symmetric multiprocessors.

vii) In general an *n* input Omega network requires ..... stages of 2*2* switches.

a) 2 b) 4

c) 8 d) 16.

viii) Dynamic pipeline allows

a) Multiples function to evaluate

b) Only streamline connection

c) To perform fixed function

d) None of these.

ix) The performance of a pipeline processor suffers if

a) the pipeline stages suffers different delay

b) consecutive instructions are dependent on each other

c) the pipelining stages share same resources

d) All of these.

x) Superscalar processors have CPI of

a) Less than 1 b) Greater than 1

c) More than 2 d) Greater than 3.

xi) The main memory of a computer has 2 cm blocks while the cache has 2 c blocks. If the cache uses the set associative mapping scheme with 2 blocks per set; then block k of the main memory maps to the set

a) (k mod m) of the cache

b) (k mod c) f the cache

c) (k mod $2c$) of the cache

d) (k mod 2 cm) of the cache.

xii) Overlapped register windows are used to speed up procedure call and return in

a) RISC architecture b) CISC architecture

c) Both (a) and (b) d) None of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Discuss different types of vector instruction.

3. What are the differences between loosely coupled and tightly coupled architecture ? What do you mean by non-uniform memory access, uniform memory access and memory bandwidth ? 2 + 3

4. A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts :

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmatic	50000	2
Data Transfer	70000	3
Floating p int ar thmetic	25000	1
Branch	4000	2

Calculate the effective CPI, MIPS rate and execution time fopr this program. 2 + 2 + 1

5. Compare superscalar, super-pipeline & VLIW technique.

6. What is the cache coherence problem ? Suggest one method to solve this problem. 2 + 3

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. What is pipeline ?

Consider the following reservation table :

	1	2	3	4
S1	X			X
S2		X		
S3			X	

Write down the forbidden latencies and initial collision vector. Draw the state diagram for scheduling the pipeline. Find out the sample cycle, greedy cycle and MAL. If the pipeline clock rate is 25 MHz, what is the throughput of the pipeline ? What are the bounds on MAL ?

2 + 2 + 3 + 3 + 2 + 3

8. a) What do you mean by MMX ? Differentiate a data flow computer from a control flow computer.

b) List some potential problems with data flow computer implementation.

c) With simple diagram explain data flow architecture.

d) Draw data flow graphs to represent the following computations :

i) $P = X + Y$

ii) $Q = P \div Y$

iii) $R = X * P$

iv) $S = R - Q$

v) $T = R * P$

vi) $U = S \div T$

2 + 2 + 3 + 5 + 3

9. What is the main difference and similarities between multi-computer and Multiprocessor ? Give the architecture for a typical MIMD processor ? Explain the shared memory modes of MIMD. 5 + 5 + 5

10. What are the common data routing functions among the Processing Elements and how are they implemented ? Explain the main factors that can influence the Performance of interconnection networks. What are the different types of Multi-stage interconnection networks ? 4 + 2 + 6 + 3

11. Write short notes on any *three* of the following :

    i) Flynn's classification

    ii) Vector registers archit ctures

    iii) Write through and write back caches

    iv) Branch handling in instruction pipeline

    v) Pipeline ha ards.