Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech/(ECE-NEW)/SEM-4/EC-402/2013

2013

DIGITAL ELECTRONICS & INTEGRATED CIRCUITS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP A

(Multiple Choice Type Questions)

1. Choose the correct altern tives for any *ten* of the following : $10 \times 1 = 10$

   i) A 10 MHz signal is applied to a Mod-5 counter followed by a Mod 8 counter. The output frequency will be

   a) 10 kH b) 2·5 kHz

   c) 5 kHz d) 25 kHz.

   ii) Which family has better speed ?

   a) ECL b) DTL

   c) TTL d) MOS.

   iii) Digital multiplexer is basically a combinational logic circuit to perform the operation

   a) AND-AND b) OR-OR

   c) AND-OR d) OR-AND.

iv) Gray code equivalent of binary number $(1000001)_2$ is

a) (1100001) b) (1100011)

c) (1000011) d) (110101).

v) The decimal equivalent of 10111·0110 is

a) 22·3 b) 23·375

c) 25·5 d) 26·55.

vi) Which flipflop may act as buffer ?

a) SR b) JK

c) D d) T.

vii) 2's complement of $(24)_{10}$ is

a) 00011000 b) 11100111

c) 11101000 d) 11110011.

viii) Full form of FPGA is

a) Full Programm ble Gated Array

b) Field Programmable Gated Array

c) Full Peripheral Gated Array

d Field Peripheral Gated Array.

ix) A bubbled AND gate is equivalent to

a) OR gate b) NAND gate

c) NOR gate d) X-OR gate.

x) A carry look ahead adder is frequent, because it is

a) faster b) more accurate

c) uses fewer gate d) costs less.

xi) Given that $\left(\sqrt{61} \right)_b = (7)_{10}$, the value of b is

a) 6 b) 8

c) 4 d) 5.

xii) A decoder with enables input can be used as

a) encoder b) demultiplexer

c) comparator d) decoder.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following $3 \times 5 = 15$

2. Simplify using *k*-map in SOP form :

$f (A, B, C, D) = \sum_m (1, 2, 4, 5, 9, 10) + \sum_d (6, 7, 8, 13)$.

3. Describe successive approximation type A/D converter.

4. a) Describe the design of 4 bit ring counter and Johnson counter. 4

b) Mention the differences in terms of Mod-value. 1

5. Design a full adder using 3 to 8 decoder with all active low outputs and additional logic gates, if required.

6. Design a full adder with two half adders.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Give the design of synchronous decade counter using D flipflop. 5

b) Give design of asynchronous decade counter. 5

c) Explain with circuit one shift left-shift right shift register. 5

8. a) Design the following function using suitable MUX :
$F(A, B, C, D) = \sum_{m} (1, 3, 4, 11, 12, 13, 14, 15)$. 5

b) Design a 16 : 1 MUX using 4 : 1 MUX. 5

c) Design a full subtractor using decoder and necessary gates. 5

9. a) Describe DRAM and SRAM. Distinguish between them.

4 + 4 + 2

b) Mention differences of ROM, RAM, EPROM, EEROM. 5

10. a) Design a combinational circuit for excess 3 code to BCD conversion using minimum number of logic gates.

9

b) Describe dual slope A/D converter. 6

11. Write short notes n any *three* of the following : 3 × 5

a) Priority encoder

b) Up-down counter

c) PLA

d) TTL

e) BCD to 7 segment decoder driver.