Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech (ECE-NEW)/SEM-6/EC-604/2011

2011

VLSI CIRCUITS AND SYSTEM

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) What is the intermediate step between circuit design and fabrication in VLSI ?

      a) logic design

      b) physical design

      c) functional representation

      d) system specification.

   ii) Channel less gate array is a sub type of

      a) standard gate ASIC b) configurable ASIC

      c) full custom ASIC d) gate array ASIC.

iii) Always interconnection will be done between neighbouring modules means

a) locality b) regularity

c) modularity d) synthesis.

iv) Why band bending in MOSFET structure occurs ?

a) difference of work function

b) natural phenomena

c) due to application of electric field

d) none of these.

v) An ideal constant current source gives a current of 200 mA, for a load resistance of 500 Ω when it is short circuited, the current is

a) 40 mA b) 50 mA

c) 100 mA d) 200 mA.

vi) A MOS diode cannot be used as a component of

a) current mirror b) rectifier circuit

c) level translator d) current sink.

vii) In a CMOS Inverter circuit which of the following will act as driver ?

a) depletion type PMOS

b) depletion type NMOS

c) enhancement type PMOS

d) enhancement type NMOS.

viii) To implement the Boolean function $F = \overline{(A + B).(C + D)}$ using Pseudo NMOS logic design number of transistor required is

a) 3 b) 4

c) 5 d) 6.

ix) The model parameter LAMDA (λ) in a MOS structure stands for

a) flicker noise coefficient

b) transit time

c) channel length modulation

d) transconductance.

x) Frequency compensation for an OP-AMP can be achieved by

a) increase gain

b) adding zero

c) minimize overall phase shift

d) none of these.

xi) The expression for body - effect coefficient in MOSFET is

a) (2qNA εsi) 1/2 / Cox.

b) (2qNA εsi) / Cox.

c) (4qNA εsi) 1/2 / Cox.

d) (4qNA εsi) / Cox.

xii) The expression of low noise margin (NML) in MOSFET is

a) $V_{IL} - V_{OL}$ b) $V_{OL} - V_{IL}$

c) $V_{OH} - V_{IH}$ d) $V_{IH} - V_{OH}$.

xiii) For 0·25 μm process what is the value of λ ?

a) 0·5 μm b) 0·125 μm

c) 0·75 μm d) 1 μm.

xiv) Soft node leakage problems of CMOS NORA structure can be reduced using

a) TSPC logic

b) Zipper CMOS logic

c) NM logic

d) Cascaded domino logic.

xv) Which domain is not included in three domains of *Y* chart ?

a) system specification b) structural

c) geometrical layout d) beavioural.

xvi) Latch up occurs for CMOS as

a) CMOS invariably picks up stray signal

b) unavoidable existence of npn, pnp transistors embedded in CMOS

c) absence of parasitic effect

d) CMOS has low power dissipation.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) Draw the flow chart of VLSI design flow and explain.

   b) What are the different design rules ? Discuss each in brief. 3 + 2

3. Explain how a combination of switches and capacitors can be used to emulate a resistor.

4. What are the advantages of dynamic CMOS logic having precharge and evaluate phase ?

5. a) What do you mean by CMOS transmission Gate (TG) ?

   b) Design the following circuits using transmission gates

      i) Half adder

      ii) *D* flip-flop. 2 + 3

6. Why is reference voltage required in IC ? What are the criteria for a good reference voltage source in a VLSI circuit ? 2 + 3

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) What do you mean by rise time (t_r), fall time (t_f) and delay time (t_d) ?

   b) Prove that W_p (channel width of P-MOS) = 2·5 W_n (Channel width of N-MOS).

   c) Explain Dynamic CMOS Logic and Domino CMOS Logic with suitable diagram. (1 + 1 + 1) + 4 + (4 + 4)

8. a) Write the basis steps of fabrication.

   b) Describe the *n*-well fabrication process with a suitable diagram.

   c) Draw the schematic diagram of $Y = (A + B) \cdot (C + D)$

   4 + 8 + 3

9. a) What is static and dynamic power dissipation in a MOS circuit ?

   b) What is routing capacitance in a MOS ? Deduce switching characteristics rise time, fall time and delay time of an inverter circuit. (4 + 4) + (3 + 4)

10. a) Explain the basic building block of FPGA with diagram.

    b) What is PLA ?

    c) Implement $f_1(a, b, c) = \Sigma m(3, 5, 6, 7)$ and $f_2(a, b, c) = \Sigma m(0, 2, 4)$ using PLA.

    d) Explain the design flow of an ASIC. 6 + 1 + 3 + 5

11. Write short notes on any *two* of the following :

    a) FPGA

    b) Design rule checker (DRC)

    c) Phase locked loop

    d) Comparator

    e) ASIC