Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech(EE/OLD)/SEM-6/EI(EE)-611/2013

2013

MICROPROCESSOR AND MICROCONTROLLERS

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following questions : 10 × 1 = 10

   i) Which of the following buses would not be commonly found in a microprocessor system ?

      a) Address Bus b) Interrupt Bus

      c) Data Bus d) Control Bus.

   ii) Which of the following control signals would be provided to a static RAM component ?

      a) Refresh

      b) DMA request

      c) Write enable

      d) Interrupt request.

iii) A microprocessor is said to be 8-bit, 16-bit or 32-bit processor depending on its

a) Register b) Data Bus

c) Address Bus d) ALU.

iv) The control signal, 'ALE' is sent by 8085 in order to

a) inform I/O device that the address is being sent over the AD line

b) achieve separation of address from data

c) inform memory device that the address is being sent over the A/D line

d) inform I/O and memory that the data is being sent over the AD line.

v) The instruction MOV A, B belong to

a) immediate addressing

b) direct addressing

c) implied addressing

d) register addressing.

vi) What is the direction of address bus ?

a) Unidirectional into MP

b) Unidirectional out of MP

c) Bidirectional

d) Mixed direction when lines into MP and some other out of MP.

vii) Tri-state buffers are often used to make sure the unselected devices have their data outputs placed in the

a) High-impedance state b) Logic 1 state

c) Logic 0 state d) Input state.

viii) How many output devices can be identified by the MPU of 8085 using I/O mapped I/O ?

a) 256 b) 255

c) 1024 d) 128.

ix) In 8085 TRAP is

a) lowest priority interrupt

b) always maskable

c) highest priority interrupt

d) level triggered interrupt.

x) How many outputs are there in the output of a 10 bit DAC ?

a) 1000 b) 1023

c) 1024 d) 1224.

xi) Restart address of TRAP is

a) 0024H b) 0034H

c) 003CH d) 0038H.

xii) The address to which a software or hardware restart branches is known as

a) vectored location b) SID

c) SOD d) TRAP.

xiii) How much memory can a standard 8086 processor address in real mode ?

a) 64 kB b) 1MB

c) 16 MB d) 4 GB.

xiv) What does MMX stand for ?

a) Memory management extensions

b) Multi-media extensions

c) Machine management extension

d) Mobile machine extension.

xv) Assume Intel 8086 is in real mode. The offset is 24H. The segment register contains 0B500H. What is the physical address ?

a) 0B524H b) 0B5024H

c) 24B5H d) 240B5H.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. What are the various registers of 8085 microprocessor ? Discuss their function.

3. a) Why are program counter and stack pointer 16-bit registers? What are their uses ?

   b) Why crystal is a preferred clock source ? Can an RC circuit be used as clock source for 8085 ?

4. a) Show the register contents as each of the following instructions is being executed

   MVI C, FFH

   LXI H, 8070 H

   XI D. 8070 H

   MOV M, C

   LDAX D

   HLT 2

b) Draw the timing diagram of 'MOV A, M' instruction. 3

5. a) Why absolute decoding is preferred over partial decoding to interface memory chip ? 2

b) Compare Memory mapped I/O and I/O mapped I/O. 3

6. Write an assembly language program for 8085 microprocessor to XOR to 8-bit data without using XRA instruction.

7. What are the Hardware and Software interrupts in 8085 microprocessor ? Distinguish them.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

8. a) What is monitor program of a microcomputer ? 2

b) Specify the function of the address bus and data bus of 8085 microprocessor. Discuss the direction of the information flow on the buses with bus architecture diagram. 7

c) What is the need to demultiplex the bus AD0-AD7 in 8085 μP ? Show the demultiplexing scheme. 6

9. a) For a 8085μP, the system clock frequency is 3 MHz. Write a nested delay loop to implement a time delay of 2 msec. 5

   b) An array of 10 numbers (all 8bits) is stored in consecutive memory locations starting from 4000H. Write a program in 8085 assembly language to find out the smallest of those 10 numbers. Save the smallest number in location 5000H. 6

   c) What is the function of sub-routine ? How is a sub-routine handled in a microprocessor ? 2 + 2

10. a) If the memory chip size is 1024 X 4 bits, how many chips required to make up 2K bytes of memory ? 2

    b) Design a circuit to interface one 6116 (2K X8) CMOS R/W chip with 8085 microprocessor using 74LS138 (a 3-to-8 line decoder with $\overline{E}_1$, $\overline{E}_2$ and E_3 enabling lines). Follow absolute decoding scheme. 7

    c) Write an 8085 Assembly Language Program to generate N elements of a Fibonacci series. Store your result at X000H onward. 6

11. a) What are the various interrupt lines of 8085 μP ? On what priority are they served ? Explain the operation of "Vectored Interrupt" with suitable diagram showing vector locations. 2 + 1 + 5

b) What are the contents of stack pointer register and program counter after the execution of the CALL instruction ? 2

c) Interface an 8-bit ADC with 8085 μP using status check scheme. 5

12. a) Assume that the 8085 is completing an RST7·5 interrupt request. Write an assembly language program to check if RST6·5 is pending. If it is pending enable RST6·5 without affecting any other interrupts otherwise return to the main program. Assume that RST6·5 is stored in location 7000 H. 5

b) Describe the operations of transmitter and receiver sections of 8251 USART. 5

c) What is DMA ? With suitable block diagram explain how the data is transferred using DMA controller. 1 + 4

13. a) What do you mean by Mode 0, Mode 1 and Mode 2 operations of 8255 PPI ? 4

b) Discuss the control word format in BSR mode of 8255 PPI 3

c) In mode 1 operation of 8255 PPI, what are the control signals when ports *A* and *B* act as output ports ? 4

d) List the major components of the 8259A interrupt controller and explain their functions. 4