Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH(ECE-N)/SEM-3/EC-302/2012-13

2012

SOLID STATE DEVICES

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

10 × 1 = 10

i) A *p*-type semiconductor contains holes and

a) Positive ions b) Negative ions

c) Pentavalent atoms d) Donor atoms.

ii) Diffussion of free electrons across the junction of an unbiased diode produces

a) Forward bias b) Reverse bias

c) Breakdown d) the Depletion Layer.

iii) When a pentavalent impurity is added a semiconductor becomes

a) positively charged b) negatively charged

c) neutral d) none of these.

iv) PIN diode has

a) *p* and *n* layers separated by I layer

b) *p*+ and *n*+ layers separated by I layer

c) *p* – and *n* – ayers separated by I layer

d) either (b) or (c).

v) Under high electric fields, in a semiconductor with increasing electric field

a) the mobility of charge carriers decreases

b) the mobility of charge carriers increases

c) velocity of carriers saturate

d) both (a) and (c).

vi) Compared to Field effect phototransistors, a bipolar phototransistors are

a) more sensitive and faster

b) more sensitive and slower

c) less sensitive and slower

d) less sensitive and faster.

vii) The probability of recombination of EHP in semiconductor is proportional to

a) density of electrons

b) density of holes and electrons

c) density of holes

d) none of these.

viii) Diffussion constant of holes and electrons are in ratio 4 : 1. Then the mobility of holes and electrons will be in the ratio

a) 4 : 1 b) 16 : 1

c) 1 : 4 d) 1 : 16.

ix) Consider the following statements :

The threshold voltage of a MOSFET can be increased by

1. Using thinner Gate oxide
2. Reducing the Substrate concentration
3. Increasing the Substrate concentration

of these

a) (3) alone is correct

b) (1) and (2) are correct

c) (1) and (3) are correct

d) (2) alone is correct.

x) Consider the following w.r.t. tunnel diode :

1. It is a 2 terminal device with no isolation between input and output
2. Same current can be achieved at 3 different voltage levels.

of these

a) (1) only

b) (2) only

c) (1) and (2)

d) none of these.

xi) If for CE model

h_{ie} = 1 k.ohm, h_{fe} = 50 then for

common collector model h_{ie} , h_{fe} will be

a) 1 k.ohm, 50 b) 1 k.ohm, –51

c) 1/51 k.ohm, 50 d) 1/51 k.ohm, –51.

xii) In a voltage regulator circuit, the maximum value of load current can be

a) 2.5 mA b) 0.9 mA

c) 1.6 mA d) 3.4 mA.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Draw & explain E-K diagram for a direct & indirect band gap semiconductor with suitable example.

3. What is mobility & conductivity ? Define effective mass. Derive relation ship between energy & momentum. 1 + 1 + 3

4. State the difference between a *p-n* junction diode & Schottky diode. Describe punch through effect in BJT. 2 + 3

5. Explain negative differential resistance that occurs in an IMPATT diode.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

6. Draw the V-I characteristic of JEET & explain it.

   Draw FET small signal model. A JFET has V_p = – 4·5V, Idss = 10m Amp & Ids = 2·5 mA. Determine the transconductance. 7 + 8

7. Explain band bending & channel inversion in case of NMOS. What is channel length modulation ? 10 + 5

8. Briefly explain the operation of a photodiode. Explain how an LED works as a source of light. Find the expression of drift current in a *p-n* junction diode. 5 + 5 + 5

9. Explain how a Zener diode works as a voltage regulator. Derive the expression for the depletion width along a *p-n* junction. 5 + 10

10. Write down the names of different steps in IC fabrication. Explain photolithography. 5 + 10

11. a) Explain how the junction theory helps to understand the gate control over the channel current.

b) Justify the reason of high doping of the gate compared to the channel doping. 8 + 7