ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER - 2008

COMPUTER ORGANIZATION

SEMESTER - 3

Time : 3 Hours] [Full Marks : 70

GROUP - A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

i) When signed numbers are used in binary arithmetic then which one of the following notations would have unique representation for zero ?

a) Sign magnitude b) 1's Complement

c) 2's Complement d) None of these. ☐

ii) The logic circuitry in ALU is

a) entirely combinational

b) entirely sequential

c) combinational cum sequential

d) none of these. ☐

iii) In a micro-processor, the address of the next instruction to be executed, is stored in

a) Stack pointer

b) Address latch

c) Program counter

d) General purpose register. ☐

iv) The technique of placing software in a ROM semiconductor chip is called

a) PROM b) EPROM

c) FIRMWARE d) Micro-Processor. ☐

v) Cache Memory

b) increases performance b) increases machine cycle

c) reduces performance d) none of these. ☐

vi) Associative memory is a

a) very cheap memory b) pointer addressable memory

c) content addressable memory d) slow memory. ☐

vii) A single bus structure is primarily found in

a) main frames b) super computers

c) high performance machines d) mini and micro-computers. ☐

viii) Memory mapped I/O scheme is used for the allocation of address to memories and I/O devices is used for

a) small system b) large system

c) both large and small systems d) very large system. ☐

ix) The convertion of $(FAFAFA)_{16}$ into octal form is

a) 76767676 b) 76575372

c) 76737672 d) 76727672. ☐

x) Which of the following addressing modes is used in the instruction PUSH B ?

a) Immediate b) Register

c) Direct d) Register Indirect. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Show the circuit diagram for implementing the following register transfer operation. If $(ab^- = 1)$ then R1 ← R2 else R1 ← R3, where a and b are control variables.

3. What do you mean by instruction cycle, machine cycles and T states ?

4. What is virtual memory ? Why is it called virtual ? Write the advantage of virtual memory. 2 + 1 + 2

5. What are the advantages of microprogramming control over hardwared control ? What is the role of operating system ? 3 + 2

6. What are the different types of interrupt ? Give examples. What is programmed I/O technique ? 3 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following questions. 3 × 15 = 45

7. a) What are Von Neumann concept and its bottleneck ?

   b) Represent the decimal value - 7·5 in IEEE - 754 single precision floating-point format.

   c) Compare parallel adder with serial adder.

   d) What is the necessity of guard bits ?

   e) Explain and draw the 4-bit binary decrementer circuit. 4 + 3 + 4 + 1 + 3

8. a) Draw the internal cell diagram of PROM and explain its functionality.

   b) What is cache memory ? How does it increase the performance of a computer ? What is hit ratio ?

   c) A three level memory system having cache access time of 5 nsec and disk access time of 40 nsec, has a cache hit ratio of 0·96 and main memory hit ratio of 0·9. What should be the main memory access time to achieve an overall access time of 16 nsec ?

   d) Define : (i) rotational latency, (ii) seek time. 4 + 4 + 5 + 2

9. a) What is instruction cycle ? Draw the time diagram for memory write operation.

   b) Explain the basic DMA operations for transfer of data between memory and Peripherals.

   c) Evaluate the arithmetic statement $X = (A * B) / (C + D)$ in one, two and three address machines. 1 + 4 + 5 + 5

10. a) Given the following, determine the size of the sub-fields in the address for direct mapping, associative mapping and set-associative mapping cache schemes :

Main memory size	512 MB
Cache memory size	1 MB
Address space of processor	512 MB
Block size	128 B

8 blocks in cache set.

b) Differentiate between memory mapped I/O and I/O mapped I/O. 10 + 5

11. Write short notes on any *three* of the following : 3 × 5

a) Magnetic recording

b) Cache replacement policies

c) Non-restoring division method

d) Addressing modes

e) Booth's algorithm.

END