Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech(CSE/IT)/SEM-3/EC-312/2009-10

2009

# DIGITAL ELECTRONICS & LOGIC DESIGN

*Time Allotted* : 3 Hours *Full Marks* : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

## GROUP – A

## ( Multiple Choice Type Questions )

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) An example of weighted code is

a) Excess-3 b) ASCII

c) Hamming code d) 8421.

ii) The minimum number of NAND gates required to design one Full Adder circuit is

a) 5 b) 9

c) 6 d) 10.

iii) A decoder with enable input can be used as

a) Encoder b) Parity Generator

c) NAND d) Demultiplexer.

 

iv) The value of 2^6 in octal system is

a) 20 b) 420

c) 32 d) none of these.

v) The maxterm corresponding to decimal 15 is

a) ABCD b) $A' + B' + C' + D'$

c) A + B + C + D d) $A' B' C' D'$ .

vi) The decimal equivalent of $( 332 )_4$ is

a) 63 b) 94

c) 62 d) none of these.

vii) How many 1's are present in the binary representation of decimal number $( 3 \times 512 + 7 \times 64 + 5 \times 8 + 3 )$ ?

a) 8 b) 9

c) 10 d) 11.

viii) The greatest negative number of 1-byte in 2's complement scheme is

a) – 256 b) – 255

c) – 128 d) – 127.

ix) The output of a logic gate is '1' when all its *i/p* are at logic '0'. The gate is either

a) NAND or XOR gate b) NOR or XOR gate

c) AND or XNOR gate d) NOR or XNOR gate.

x) J-K flip-flop has

a) one stable state b) two stable states

c) no stable state d) none of these.

xi) Which of the following is reflected code ?

a) 8421 b) Excess-3

c) Gray d) ASCII.

xii) Gray code of a binary number 1011 is

a) 1110 b) 1100

c) 1101 d) 1111.

xiii) The fast logic family is

a) TTL b) ECL

c) TRL d) DRL.

xiv) The operation which is commutative but not associative is

a) AND b) XOR

c) NAND d) NOT.

xv) The number of XOR gates required for conversion of 11011 to its equivalent grey code is

a) 2 b) 4

c) 3 d) 5.

## GROUP – B

### ( Short Answer Type Questions )

Answer any *three* of the following. $3 \times 5 = 15$

2. Realize the following expression using K-map and implement the simplified expression using NOR gates only :

$F(A, B, C, D) = \Sigma(0, 1, 4, 6, 7, 10, 11, 12, 13, 15) + d(2, 5, 9, 14)$.

3. a) Design 4 × 16 decoder using 3 × 8 decoders. 3

b) Implement 2-input XOR function using minimum number of 2-input NAND gates. 2

4. Design full subtractor using 4 : 1 multiplexers.

5. Perform the conversion from S-R to J-K flip-flop.

6. Realise a full-subtractor using all NAND gates.

## GROUP - C

### ( Long Answer Type Questions )

Answer any *three* of the following. 3 × 15 = 45

7. a) Describe the operation of successive approximation type ADC. How many clock pulses are required in worst case for each conversion cycle of an 8-bit SAR type ADC ? Define quantizing error for an ADC.
   b) Draw a neat diagram for an R-2R ladder type DAC & explain its operation. 7 + 8
8. a) Design a MOD-10 synchronous binary UP-counter using JK flip-flop & other necessary logic gates.
   b) Calculate the propagation delay for a 4-bit synchronous binary UP-counter when JK flip-flops are connected in series connection & parallel connection.
   Given Propagation delay Tp ( F/F ) in 30 nsec & propagation delay of the gates used in the circuit is 20 nsec ( assumed to be equal for all gates ). 8 + 7
9. a) Draw the circuit for a 4-bit Johnson counter sing D flip-flop & explain its operation. Draw its timing diagram. How does its timing diagram differ from that of Ring counter ?
   b) Perform the conversion from D f/f to JK f/f. 8 + 7
10. a) Distinguish between ROM, PLA & PLD's as elements realizing Boolean function.
   b) Design a combinational circuit using an 8 × 4 ROM that accepts a 3-bit number & generates an output binary number equal to the square of input no.
   c) Draw a logic diagram of master-slave JK f/f. Why is it called so ? 7 + 5 + 3
11. Write short notes on any *three* of the following : 3 × 5
   a) EEPROM
   b) D/A converter
   c) Triggering of flip-flops
   d) Comparator
   e) Data lock-out in a counter.