Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH(ECE)/SEP.SUPPLE/SEM-7/EC-702/2012

2012

EDA FOR VLSI DESIGN

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

   i) FPGA based design is suitable for
      a) Prototype development
      b) Large scale product development
      c) Low power application
      d) High speed application.

   ii) A feed-through cell is an empty cell (with no logic) that is used for
      a) Vertical interconnection
      b) Horizontal interconnection
      c) Both (a) and (b)
      d) Feeding power to a cell.

   iii) A hard macro refers to a
      a) Flexible block
      b) Fixed block
      c) Flexible block with fixed aspect ratio
      d) Fixed block with fixed aspect ratio.

iv) In VHDL, the '&' operator indicates

a) Logical AND operation

b) Concatenation operation

c) Both (a) and (b)

d) None of these.

v) In VHDL, which architectural style represents the lowest level of abstraction ?

a) Behavioural Modelling

b) Structural Modelling

c) Dataflow Modelling

d) Mixed Modelling.

vi) A Boolean space consists of

a) ON-set b) OFF-set

c) DC-set d) All of these.

vii) Which of the following blocks is not present in a logic synthesizer ?

a) RTL Behavioural Model

b) Cell library

c) Configurable Logic Block

d) Design Constraints.

viii) The critical path for a design refers to

a) The path having maximum delay

b) The path with minimum delay

c) The path having optimum delay

d) The path with no delay.

ix) Left Edge algorithm is used for

a) Floor planning b) Placement

c) Routing d) Partitioning.

x) BDD is useful for

a) High level Synthesis b) Logic level Synthesis

c) Testing d) Timing Analysis.

xi) Which of the following languages is not appropriate for specifying an electronic system ?

a) Verilog b) VHDL

c) UDL d) C++

xii) More than one active contacts are drawn to

a) increase the switching time

b) decrease the propagation delay

c) reducing the contact resistance

d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Design a 3-input, 2-output PLA using pseudo-NMOS NOR logic to implement a Full adder. 5

3. Briefly explain Floor planning and Placement in VLSI design flow.

4. a) What do you mean by channel in Physical Design ?

b) Discuss between Global and Detailed Routing. 2 + 3

5. Explain the following terms with proper example :

(i) Stuck-at fault

(ii) Bridging fault

(iii) Stuck open fault. 5

6. What do you mean by testability of a circuit ? Describe the method of BIST technique. 1 + 4

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) What are the different types of architecture in VHDL ? Explain each with relevant examples.

   b) Using 4 : 1 multiplexers design a 16 : 1 multiplexer (using structural modelling). Write the VHDL codes for both 4 : 1 MUX and 16 : 1 MUX. 8 + 7

8. a) Draw and explain the Xilinx architecture of FPGA.

   b) What is PSM ? Briefly explain it.

   c) What are the various technologies used for programming FPGAs ?

   d) Draw and explain the FPGA design flowchart.

   4 + 3 + 4 + 4

9. Describe Y-Chart Model. Differentiate between Structural and Behaviroual domain. Define PLA and PAL architectures.

   5 + 5 + 5

10. Define synthesis. What are the processing steps used in High Level Synthesis ? Differentiate between data flow and control-flow graphs with example.

11. Define logic synthesis. What is a Binary Decision Tree ? What is multilevel synthesis ? What are the advantages of multilevel synthesis over two-level synthesis ? 2 + 4 + 3 + 6

12. Write short notes on any *three* of the following : 3 × 5

    a) Automatic test pattern generation

    b) FPGA Architecture

    c) PLD

    d) CAD tools

    e) Reduced Ordered Binary Decision Diagram.