

Name :

Roll No. :

Invigilator's Signature :

CS/B.Tech (EIE)/SEM-3/EC-302(EI)/2010-11

2010-11

DIGITAL INTEGRATED CIRCUITS

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP - A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any ten of the following : $10 \times 1 = 10$

i) ASCII code is

- a) 4 bit code
- b) 6 bit code
- c) 7 bit code
- d) 8 bit code.

ii) The minimum of bits in the BCD representation of the decimal number 25 is

- | | |
|------|-------|
| a) 5 | b) 4 |
| c) 3 | d) 6. |

CS/B.Tech (EIE)/SEM-3/EC-302(EI)/2010-11

- iii) Excess-3 code representation of decimal 59 is
- a) 01100010 b) 00111110
c) 10001100 d) none of these.
- iv) Hexadecimal equivalent of $(26.25)_{10}$ is
- a) A6.4 b) 1A.4
c) FA.4 d) none of these.
- v) The number of 1's in the binary representation of the decimal number 11 is
- a) 5 b) 4
c) 3 d) none of these.
- vi) With the same number of flip-flops where the Johnson counter has N states and the ring counter has M states are
- a) $N > M$ b) $N = M$
c) $N < M$ d) none of these.
- vii) The minimum number of NOR gates required to design one XOR gate is
- a) 5 b) 4
c) 7 d) none of these.
- viii) A decoder with enable input can be used as
- a) encoder b) parity generator
c) multiplexer d) demultiplexer.

CS/B.Tech (EIE)/SEM-3/EC-302(EI)/2010-11

- ix) The logic family that gives fastest switching is
- CMOS
 - ECL
 - Schottky TTL
 - Low power Schottky TTL.
- x) A 64:1 MUX consists of
- 54 no. of 2:1 MUX
 - 63 no. of 2:1 MUX
 - 45 no. of 2:1 MUX
 - 36 no. of 2:1 MUX.
- xi) How many RAM chips of size (256k*1bit) are required to build 1M byte memory ?
- 24
 - 10
 - 32
 - 8.
- xii) Which one is the fastest logic in logic families ?
- RTL
 - TTL
 - ECL
 - none of these.
- xiii) Binary division $10010.1011 \div 11.01$ yields
- 110.11
 - ~~100~~.11
 - 101.10
 - 101.11

CS/B.Tech (EIE)/SEM-3/EC-302(EI)/2010-11

4. Explain BCD addition with proper diagram and proper example.
5. a) Design 8:1 MUX using 4:1 MUX and 2:1 MUX.
- b) What is priority encoder ?
6. Prove that :
- a) $A + \overline{A}B + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}\overline{C}D = A + B + C + D$
- b) $AB + \overline{A}C + \overline{A}BC(AB + C) = 1$

GROUP - C**(Long Answer Type Questions)**Answer any *three* of the following. $3 \times 15 = 45$

7. a) Simplify the following Boolean function using Quine - McCluskey method :
- $Y(A, B, C, D) = \sum m(1, 2, 3, 5, 9, 12, 14, 15) + d(4, 8, 11)$
- b) Draw the logic circuit of S-R flip-flop using D flip-flop.
- c) What are the advantages of D flip-flop over S-R flip-flop ?

 $8 + 5 + 2$

CS/B.Tech (EIE)/SEM-3/EC-302(EI)/2010-11

8. a) Using the K-map method, simplify the following Boolean function and obtain

i) SOP &

ii) POS expressions for

$$Y = \sum m (0, 2, 3, 6, 7) + \sum d (8, 10, 11, 15)$$

- b) Design a Mod-5 synchronous counter using J-K flip-flop.

- c) What do you mean by Race-around condition ? $6 + 7 + 2$

9. a) Implement a full-subtractor circuit using PLA having three inputs and two outputs.

- b) Design 8:1 Multiplexer using NAND gates only.

- c) Implement the following function using 3-to-8 line decoder :

$$Y (A, B, C) = \sum m (4, 5, 6, 7) \quad 6 + 6 + 3$$

10. a) Design a Gray code to binary converter using suitable logic gates.

- b) Explain addition and subtraction for 1's complement using 4-bit parallel adder.

CS/B.Tech (EIE)/SEM-3/EC-302(EI)/2010-11

- c) What are the differences between a latch and a flip-flop ?
- d) What are the differences between Edge-triggered and level-triggered flip-flop ?

7 + 4 + 2 + 2

11. Answer any *three* of the following :

3 × 5

- a) Even parity checker and generator
- b) Successive approximation register type ADC
- c) PAL
- d) BCD to Excess-3 converter
- e) R-2R ladder type D/A converter
- f) Universal gate.

=====