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CS/B.Tech (EIE)/SEM-4/CS-404 (EI)/2010

2010

COMPUTER ORGANISATION AND ARCHITECTURE

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) How many bits are needed to represent a digit in Hexadecimal notation ?

   a) 8 b) 16

   c) 4 d) 2.

   ii) How many RAM chips (each 128*4) are required to provide a memory capacity of 2048 bytes ?

   a) 32 b) 16

   c) 8 d) 64.

   iii) Principle of locality is justified in the use of

   a) Daisy chaining b) DMA

   c) Interrupts d) Cache memory.

   iv) Range of values on a databus of an 8-bit microprocessor using 2's complement representation will be

   a) – 128 to + 128 b) – 128 to + 127

   c) – 127 to + 128 d) – 127 to + 127.

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v) Bidirectional buses use

a) two back to back connected buffers

b) two tristate buffers in cascade

c) tri-state buffers

d) two tri-state buffers back to back connected in parallel

vi) How many memory locations can be accessed by a 232-bit computer ?

a) 64 kB b) 32 kB

c) 4 GB d) None of these.

vii) Highest speed Logic gate among the following is

a) TTL b) DTL

c) RTL d) ECL.

viii) A 'hit' is considered when

a) word is found in cache

b) word is not found in cache

c) word is found in virtual memory

d) word is not found in virtual memory.

ix) Which one of the following is volatile in nature ?

a) ROM b) DVD-ROM

c) CD-ROM d) RAM.

x) Using binary arithmetic, the unique representation of zero is

a) Sign magnitude b) 2's complement

c) 1's complement d) none of these.

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GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Explain an interrupt cycle with a flowchart.

3. What is the difference between hardwired control and microprogrammed control ?

4. What is a multiprocessor ? Write briefly about Harvard architecture. 1 + 4

5. With the help of a diagram explain clearly the structure and working of a typical arithmetic pipeline to perform : $X * Y + Z$.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

6. a) Show the bus connection with a CPU to connect four RAM chips of size 256 × 8 bits each and a ROM chip of 512 × 8 bit size. Assume the CPU has 8-bit data bus & 16-bit address bus. Clearly specify generation of chip select signals.

   b) What is an instruction cycle ? Describe the steps of instruction cycle with suitable diagram.

   c) What are the advantages of interrupt-initiated I/O over programmed I/O. 6 + 6 + 3

7. a) What are the different types of DMA controllers and how do they function ?

   b) Briefly describe pipeline hazards.

   c) What is the difference between a carry-look ahead adder and a ripple carry adder ?

   d) What are the bottlenecks of von Neumaun concept ?

   5 + 5 + 3 + 2

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8. a) A hierarchical cache-main memory sub-system has the following specifications cache access time :

50 ns, main memory access time 500 ns, 80% of memory request for read, hit ratio 0·9 for read access and write-through scheme is used.

i) Calculate the average access time of the memory system considering only memory read cycle.

ii) Calculate the average access time of the memory system both for read & write.

b) Explain clearly the procedure of virtual address translation into real address in a paged virtual memory system.

c) What is the difference between associative and set-associative mappings ? 6 + 6 + 3

9. a) Using Booth's algorithm multiply (–3) and f (–5) upto five digits. Show every step.

b) Evaluate the following statement using zero address and two-address machines : $Z = (M + N)*(P + Q)$.

c) Explain Flynn's classification with respect to computer architecture. 6 + 5 + 4

10. a) Design and describe the function of a control unit with block diagram for a typical computer having 16-bit instruction register.

b) Describe briefly the different addressing modes. 9 + 6

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