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Invigilator's Signature :	

### CS/B.TECH(CSE)/SEM-8/CS-801D/2012

## 2012

## **VLSI DESIGN**

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Group-A is compulsory and answer any *six* questions from rest of the Groups B, C and D taking two from each Group.

# GROUP - A ( Multiple Choice Type Questions )

- 1. Choose the correct alternatives for the following:  $10 \times 1 = 10$ 
  - i) NMOS enhancement mode transistors are faster than PMOS transistors, because
    - a) the electron mobility is higher than the hole mobility
    - b) the hole mobility is higher than the electron mobility
    - c) concentration of electrons is greater than holes
    - d) concentration of holes is greater than electrons.
  - ii) Which of the following devices is expected to have the highest input impedance?
    - a) BJT

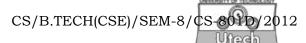
- b) JFET
- c) MOSFET
- d) CMOS.

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The size of an IC is generally measured by

	a)	physical size			Tan-	Camplely 2nd Ex	- Tolan
	b)	No. of two-input	NAND ga	tes	7	Considge 2nd Ex	
	c)	No. of transistors	used				
	d)	No. of pins.					
iv)	The	full form of abbre	viation Bl	ILBO re	gister is	3	
ŕ	a)						
	b)	b) built in linear back operation register					
	c)	c) built in logic block observer register					
	d)	d) none of these.					
v)	To	implement a fou	ır-input	NAND	gate u	ısing	MOS
	trai	nsistors, number o	f transist	or requ	ired is		
	a)	2	b)	4			
	c)	6	d)	8.			
vi)	P M	IOS transistor offer	rs .				
	a)	strong '0'	b)	stron	ıg '1'		
	c)	weak Group-B'1	•	weak	: '0'.		
vii)	ASI	Cs are more flexible	le than Fl	PGAs			
	a)	true					
	b)	false					
	c)	none of these.					
viii)							
		ed to reduce the ele	_		ect is		
	a)	89% Al, 5% Cu a					
	b)	95% Al, 4% Cu a					
	c)	70% Al, 10% Cu			_		
ix)		ximum fan out of C			rcuit ar	e	
	a)	4	b)	10			
,	c)	14	d)	20.			, .
x)		pseudo nMOS lo	gic ratio	of $Z$ (1	oull up	and	(pul
		vn) is	1-1	2 . 1			
	a)	4:1	b)	3:1			
	c)	2:1	d)	1:1	•		
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2.	a)	How nMOS transistor can be used as a switch and a
		pass transistor ? What is the difference between
		<i>n</i> -channel and <i>p</i> -channel pass transistors? $4 + 4$
	b)	Draw circuit diagram of a tri-state buffer. 2
3.	a)	What is transmission gate? What is its advantage?
		6
	b)	Design EX-OR circuit using transmission gate and inverter.
4)	a)	Draw an X-OR and EXNOR circuit using CMOS
		transistors. 4
	b)	Design a AND/NAND, OR/NOR and XOR gate using
		complementary pass transistor logic. 6
5.	a)	Design a MOD8 counter and draw block diagram. 4
	b)	Draw the circuit of a 2:1 multiplexer using tri-state
		buffer. 3
	c)	What are the disadvantages of multiplexer design using
		nMOS two-variable functional block?
		GROUP – C
6.	a)	What are the different stages of physical design cycle? 3
	b)	Explain the function of each stage. 5
	c)	What are the objectives of placement?
7.	a)	Write a verilog code for full adder using half adder and
		<i>J-K</i> flip-flop.
	b)	Define pure and impure functions with example. 4
8.	a)	What is ASIC? What are the limitations of ASIC? How
		are these limitations eliminated in FPGA? $2 + 1 + 2$
	b)	What are the basic building blocks of a typical FPGA?
		With an example, explain how LUTs (Look Up Table) are
		used as configurable Logic block in FPGAs? 2 + 3

CS/B.TECH(CSE)/SEM-8/CS-801D/2012 9. What is the difference between Stick Diagram a) Layout Diagram? b) What is lamda rule? Explain. 2 Draw the Stick Diagram of a two-input NOR gate. 3 c) 3 Draw the Layout Diagram of a NOT gate. d) GROUP - D 10. Explain the formation of the MOS capacitance in a two terminal MOS structure. Derive an expression for the effective MOS capacitance and explain with suitable diagram.

How does the MOS capacitance vary with Gate voltage? Will there be any difference in the pattern if the measurement is done using low frequency and high frequency signals?

- Justify your statement. 11. With the help of band-diagram, explain the formation of accumulation, depletion and inversion regions in an n-MOS. Explain weak, moderate and strong inversions. What is Flat Band voltage? At what voltages will the weak, moderate and strong inversions occur? Why does the surface voltage saturate at strong inversion? 4 + 2 + 1 + 2 + 1
- 12. Draw the small-scale equivalent circuit of a MOSFET at low frequency and derive expressions for each of the circuit components. How will this be modified for high frequency case? What will be the parasitic capacitances? Also identify 2 + 3 + 2 + 2 + 1the noise sources.
- 13. a) Write down the Voltage and Charge Balance equations for a two-terminal real MOS. If the Gate voltage changes by  $\Delta V$ , how will these two equations be affected? Why? 2 + 2 + 1
  - Explain Latch-up in a CMOS. How can it be prevented? b)

3 + 2

3 + 2 + 2 + 1 + 2

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