MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : PC-EE302/PC-EEE302   Analog Electronics

UPID : 003520

Time Allotted : 3 Hours

Full Marks :70

The Figures in the margin indicate full marks.
Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

[1 x 10 = 10]

1. Answer any ten of the following :

(I) What is the conduction angle of a class C power amplifier?

(II) What is the value of CMRR of an Ideal OP-Amp?

(III) What is the relation between I_{CEO} and I_{CBO} in a BJT?

(IV) Where the bias point should be located on the dc load line of a series fed class-A power amplifier?

(V) How many stable state are possible in a monostable multivibrator?

(VI) According to Barkhausen criteria, what must be the closed loop gain of a feedback circuit in order to create a sustained oscillation?

(VII) Use of negative feedback reduces the noise level in a amplifier system. True or False

(VIII) The Q point (I_{CQ}, V_{CEQ}) is at the middle of the ac load line in a class-A transformer coupled power amplifier. Then what is the maximum possible peak to peak variation in the collector-emitter voltage.

(IX) A full wave bridge rectifier with a 20 V (p-p) sinusoidal input has a load resistance of 1 KΩ. Determine the average dc output voltage. Assume ideal diode.

(X) What are the operating regions of a BJT characteristics used when the BJT is intended to act as a switch?

(XI) For a transistor α = 0.988, I_B = 10 μA. Determine I_E.

(XII) One differential amplifier has a differential gain 20000. Find out the common mode gain if CMRR = 80 dB.

Group-B (Short Answer Type Question)
Answer any three of the following

[5 x 3 = 15]

2. Describe piece wise linear diode model. Show the break down region in the I-V characteristics of an actual diode. [5]

3. Design a differentiator circuit using Op-Amp and other necessary circuit element so that it will have a time constant of 10^{-2} s and an input capacitance of 0.01 μF. Determine the voltage gain magnitude and phase of the designed circuit at 10 rad/s. [5]

4. Draw a high frequency model of a BJT. Define and give an expression of the parameters used in the model. [5]

5. Draw and explain the functioning of a current to voltage converter using OP-Amp. https://www.makaut.com [5]

6. Draw a differential amplifier using two *npn* transistor and a constant current source and other necessary circuit elements. Explain how it rejects the common mode input voltage. [5]

Group-C (Long Answer Type Question)
Answer any three of the following

[15 x 3 = 45]

7. (a) What is the difference between series voltage regulator and shunt voltage regulator? Describe the working principle of a shunt voltage regulator with a neat diagram. [12]

   (b) Define the line and load regulation of a voltage regulator. [3]

8. (a) What is the difference between power amplifier and voltage amplifier. [3]

   (b) Draw a circuit diagram of transformer coupled class-A power amplifier. Describe its operating principle. [8]

   (c) Derive an expression for a power conversion efficiency of a power amplifier. Calculate the possible maximum efficiency of a transformer coupled class-A power amplifier. [4]

9. (a) What are the main factors which affects the stability of a Q point in BJT transistor. Define three stability factor associated with a BJT. [3]

   (b) Draw a neat circuit diagram of a collector feedback biasing circuit using an NPN transistor in CE mode without emitter resistance. Find out its Q point (V_{CE}, I_C). [6]

   (c) Calculate its stability factor $S(I_{CO})$. [6]

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10. (a) Draw an instrumentation amplifier using OP-Amp. Explain its functioning [7]

(b) Design and analyses an integrator using an OP-Amp. Describe how it behaves as an integrator circuit. Draw the corresponding output if a triangular waveform is applied. [8]

11. (a) Determine R_{in}, R_o and A_v of the following circuit by applying hybrid-Π model of the transistor. [7]
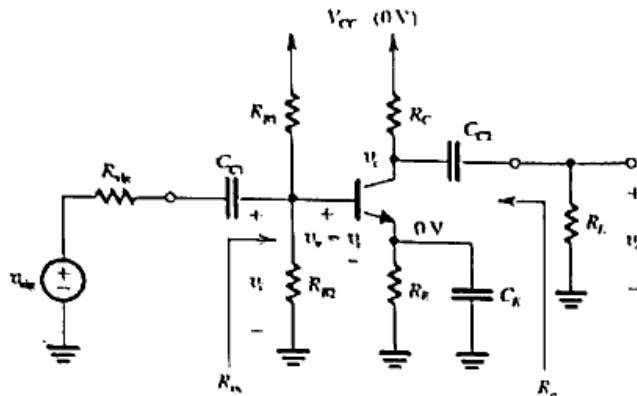
(b) A CE amplifier uses a BJT with $\beta = 100$ is biased at a collector current of 1 mA and has a collector resistance $R_C = 5$ kΩ. Find g_m, r_n, r_o. Assume $V_A = 100$V. [4]

(c) Draw an emitter stabilized bias configuration circuit using pnp transistor in CE mode and other necessary circuit elements. Derive an expression for I_C. [4]