WEST BENGAL UNIVERSITY OF TECHNOLOGY

EC-402

DIGITAL ELECTRONICS AND INTEGRATED CIRCUITS

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. 10×1 = 10

(i) The 2's complement representation of $(-19)_{10}$ is

(A) 101100 (B) 101110
(C) 101101 (D) none of these

(ii) An example of reflected code is

(A) BCD (B) GRAY
(C) ASCII (D) Hamming code

(iii) A 4-bit ripple counter counts up to

(A) 12 (B) 15
(C) 11 (D) 4

(iv) The Gray code of $(1011)_2$ is

(A) 0101 (B) 1101
(C) 1110 (D) none of these

(v) If $(212)x = (23)_{10}$ then what is the value of x is

(A) 2 (B) 3
(C) 4 (D) 5

(vi) The fastest logic gate family is

(A) CMOS (B) ECL
(C) TTL (D) RTL

(vii) The minimum number of NAND gates required to implement the Boolean function $(A+A\bar{B}+A\bar{B}C)$ is

(A) 1 (B) 4
(C) 7 (D) ZERO

(viii) The number of D flip-flop required to design MOD-10 ring counter is

(A) 5 (B) 10
(C) 9 (D) 8

(ix) The fastest ADC is

(A) Dual slope type (B) SAR type
(C) Counter type (D) None of these

(x) The memory which is ultraviolet erasable and electrically programmable is

(A) RAM (B) EEROM
(C) PROM (D) EPROM

(xi) Master-slave configuration is in flip-flops to

(A) increase its clocking rate (B) reduce power dissipation
(C) eliminate race-around condition (D) improve its reliability

(xii) The output frequency of decade counter clocked from a 50 kHz signal is

(A) 50 kHz (B) 500 kHz
(C) 5 kHz (D) 25 kHz

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. Design a full subtractor circuit using 4:1 Multiplexer. 5

3. (a) Differentiate combinational logic circuit and sequential logic circuit. 2+3
   (b) Minimize the following function using K-Map-
   $F(A,B,C,D) = \sum_m(1,3,4,5,9,10,11) + \sum_d(6,8)$ and implement the circuit using basic gates.

4. Draw the circuit of priority encoder. Explain how the problems of a plain encoder are removed in a priority encoder. 2+3

5. (a) Define the following terms related with Digital IC- 3+2
   (i) Propagation Delay
   (ii) Noise Margin
   (iii) Fan In and Fan Out
   (b) Design 2-input NOR gate using MOS.

6. (a) Implement full adder circuit using ROM. 3+2
   (b) Design Binary to Gray code converter using logic gates.

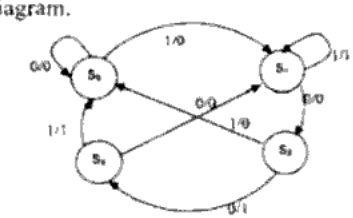
GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) Design a circuit using suitable MUX to implement the following function: 5+5+5
   $F(A,B,C,D)=\sum_m(1,3,4,11,12,13,14,15)$
   (b) Design a full subtractor circuit using MUX.
   (c) Perform the conversion from D flip-flop to S-R flip-flop.

8. (a) Design a synchronous decade counter using D flip-flop.
   (b) Design an asynchronous 3 bit up-down counter using JK flip flop which counts up, when external signal M = 1 and counts down when M = 0.

9. (a) Using D flip-flop design a sequential circuit that implements the following state diagram. 7+8



   (b) Realize a 4-bit Johnson counter using JK flip-flops.

10. (a) Design a combinational circuit for Excess-3 code to BCD conversion using minimum number of logic gates. 9+6
   (b) Describe dual slope A/D converter.

11. (a) Mention differences of ROM, RAM, EPROM and EEPROM. 5+5+5
   (b) Discuss the totem pole output configuration of TTL logic family.
   (c) Design a basic 2 input TTL NAND gate and explain its performance.

12. Write short notes on any *three* of the following: 3×5
   (a) Bi-directional shift register
   (b) Priority encoder
   (c) R-2R Ladder type DAC
   (d) Carry look ahead adder
   (e) BCD to 7 segment decoder driver.