ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2007

ADVANCED COMPUTER ARCHITECTURE

SEMESTER – 4

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

i) The number of cycles required to complete n tasks in a k stage pipeline is

a) $k + n - 1$ b) $nk + 1$

c) k d) none of these.

ii) A computer with cache access time of 100ns, a main memory access time of 1000 ns, and a hit ratio of 0·9 produces an average access time of

a) 250 ns b) 200 ns

c) 190 ns d) none of these.

iii) Which of the following types of instructions are useful in handling sparse vectors or sparse matrices often encountered in practical vector processing applications ?

a) Vector-Scalar instruction b) Masking instruction

c) Vector-memory instructions d) None of these.

iv) A 4-ary 3-cube hypercube architecture has

a) 3 dimensions wih 4 nodes along each dimension

b) 4 dimensions with 3 nodes along each dimension

c) both (a) and (b)

d) none of these.

v) Which of these are examples of 2-dimensional topologies in static networks ?

a) Mesh b) 3 CCC networks

c) Linear array d) None of these.

vi) Consider the high speed 40 ns memory cache with a successful hit ratio of 80%. The regular memory has an access time of 100 ns. What is the effective access time for CPU to access memory ?

a) 52 ns b) 60 ns

c) 70 ns d) 80 ns. ☐

vii) Assuming a Main memory of size 32 K × 12, Cache memory of size 512 × 12 and block size of 1 word, the addressing relationships using direct mapping would be

a) tag field-6 bits, index field-9 bits

b) tag field-9 bits, index field-6 bits

c) tag field-7 bits, index field-8 bits

d) none of these. ☐

viii) Overlapped register windows are used to speed-up procedure call and return in

a) RISC architectures b) CISC architectures

c) both (a) and (b) d) none of these. ☐

ix) The seek time of a disk is 30 ms. It rotates at the rate of 30 rotations / second. The capacity of each track is 300 words. The access time is approximately

a) 62 ms b) 60 ms

c) 47 ms d) none of these. ☐

x) For two instructions I and J WAR hazard occur, if

a) $R(I) \cap D(J) \neq \phi$ b) $R(I) \cap R(J) \neq \phi$

c) $D(I) \cap R(J) \neq \phi$ d) none of these. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Compare superscalar, superpipeline and superscalar superpipelined architecture.

3. Describe Flynn's classification for parallel computer.

4. What are the different factors that can affect the performance of a pipelined system ? Differentiate between WAR and RAW with a suitable example. 2 + 3

5. Consider the performance of a main memory organization, when a cache miss has occurred as

i) 4 clock cycles to send the address

ii) 24 clock cycles for the access time per word

iii) 4 clock cycles to send a word of data.

Estimate :

a) The miss penalty for a cache block of 4 words.

b) The miss penalty for a 4 way interleaved main memory with a cache block of 4 words. $2\frac{1}{2} + 2\frac{1}{2}$

6. How do you speed up memory access in case of vector processing ? With architecture and timing diagram explain S-access memory organization. 1 + 4

GROUP – C

(Long Answer Type Questions)

Answer any *three* questions. $3 \times 15 = 45$

7. What is a pipeline ?

Consider the following reservation table :

	1	2	3	4
S1	X			X
S2		X		
S3			X	

Write down the forbidden latencies and initial collision vector. Draw the state diagram for scheduling the pipeline. Find out the sample and greedy cycle and MAL. If the pipeline clock rate is 25 MHz, then what is the throughput of the pipeline ? What are the bounds on MAL ? 2 + 2 + 3 + 3 + 2 + 3

8. a) Differentiate between multiprocessors and multicomputers based on their structures, resource sharing and inter processor communication.

   b) With the help of neat sketches, explain the 10 subsystems in case of lightly coupled multiprocessor system.

9. a) Compare dynamic connection networks such as multistage interconnection networks and crossbar switch networks in terms of the following characteristics :

   Bandwidth and Hardware complexity such as switching, arbitration, wires etc.

   b) Compare between centralized and distributed shared memory architecture. Which is the best architecture among them and why ?

10. a) How does the Cache memory effect the throughput of a computer system ? 3

    b) Distinguish between Write back and Write through Cache. 4

    c) What effect does memory bandwidth have on the effective memory access time ? 4

    d) What is Cache coherence ? How can this problem be overcome ? 4

11. Write short notes on any *three* of the following : 3×5

    a) Array processor

    b) Power PC

    c) MMX Technology

    d) Scalar and Vector processors.