



Name :

Roll No. :

Invigilator's Signature :

CS/B.Tech (EE-OLD)/SEM-4/EC(EE)-402/2013

2013

DIGITAL ELECTRONICS & INTEGRATED CIRCUITS

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) $11001 - 10001 = ?$

- | | |
|---------|----------|
| a) 1001 | b) 1000 |
| c) 1010 | d) 1011. |

ii) What is the octal equivalent of $1001101 \cdot 1011_2$?

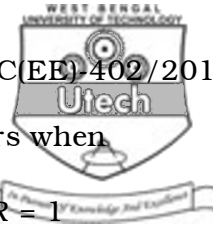
- | | |
|-------------------|---------------------|
| a) $114 \cdot 54$ | b) $115 \cdot 54$ |
| c) $115 \cdot 45$ | d) $115 \cdot 56$. |

- iii) The maximum number of 3-input gates in a 16 pin IC will be

- | | |
|------|-------|
| a) 2 | b) 3 |
| c) 4 | d) 5. |



- iv) The Boolean expression $\overline{A}\overline{B}\overline{C}\overline{D}$ is
- a) a sum term
 - b) a product term
 - c) a literal term
 - d) always 1.
- v) A feature that distinguishes the J-K flip-flop from the S-R flip-flop is the
- a) toggle condition
 - b) preset input
 - c) type of clock
 - d) clear input.
- vi) The number of flip-flops required for a MOD-10 ring counter is
- a) 10
 - b) 5
 - c) 4
 - d) 12.
- vii) A modulus 10 Johnson counter requires
- a) ten flip-flops
 - b) four flip-flops
 - c) five flip-flops
 - d) twelve flip-flops.



viii) The invalid state of an S-R flip-flop occurs when

- a) $S = 1, R = 0$ b) $S = 0, R = 1$
- c) $S = 1, R = 1$ d) $S = 0, R = 0$.

ix) A 4-bit parallel adder can add

- a) two 4-bit binary numbers
- b) two 2-bit binary numbers
- c) four bits at a time
- d) four bits in sequence.

x) The minimum number of NAND gates required to implement the Boolean function $A + AB' + AB'C$ is equal to

- a) zero b) 1
- c) 4 d) 7.

xi) The fastest logic gate family is

- a) CMOS b) ECL
- c) TTL d) RTL.

xii) The memory, which is ultraviolet erasable and electrically programmable is

- a) RAM b) EEROM
- c) EPROM d) PROM.

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Y2 + ZY

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- Y2 + ZY**

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In Pursuit of Knowledge and Excellence

Y2 + ZY



4. Design and implement a full adder circuit using decoder.
5. a) Construct the following :
 - i) EX-OR using NAND
 - ii) EX-NOR using NOR.
- b) Why are NAND gate and NOR gates called universal gates ? 2 + 2 + 1
6. Simplify algebraically, $Y = AB + A\bar{B}(\bar{A}\bar{C})$.
7. What are the specifications for D/A converters ?

GROUP – C

(Long Answer Type Questions)

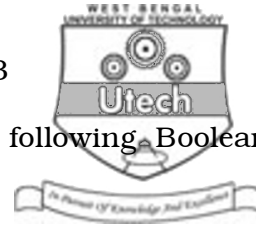
Answer any *three* of the following. 3 × 15 = 45

8. a) Expand the expression to a standard SOP form :

$$\bar{A}\bar{B} + A\bar{B}\bar{C}D + CD + B\bar{C}D + ABCD.$$
- b) Simplify the Boolean expression using Karnaugh map technique :

$$F(A, B, C, D) = \sum m(0, 1, 3, 7, 11, 15) + \sum d(2, 5, 8, 12).$$

Also implement the circuit using suitable logic gates.
- c) Using 2's complement method subtract 101101_2 from 1011101_2 . 4 + 7 + 4



9. a) Using a 8X1 MUX, implement the following Boolean expression :

$$F(A, B, C, D) = \sum m(0, 2, 4, 7, 12, 15)$$

- b) Design a full adder using shift register and full adder circuit. 5 + 10

10. a) Design a Master-Slave JK flip-flop using NAND gates only and explain its operation.

- b) What is the advantage of Programmable Logic Device (PLD) ? 12 + 3

11. What is a Register ? What is Universal Shift Register ?
Implement a 4-bit universal register using multiplexer and D-flip-flops. 1 + 2 + 12

12. a) Design a 3-bit synchronous up-counter using J-K flip-flops.

- b) Design a 3-bit Binary up/down counter with a direction control M. Use J-K flip-flops in your design. 7 + 8



13. a) Describe the working principle of R-2R ladder D/A converter.
- b) What is sample and hold circuit ? Why do we need to use this circuit ? 10 + 5
14. Write short notes on any *three* of the following : 3 × 5
- a) Odd parity checker
 - b) Data lock-out in a counter
 - c) Dual slope ADC
 - d) 7 segment display device
 - e) Carry look ahead adder
 - f) SOP and POS canonical forms of binary function.
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