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Paper Code : EC-504A

COMPUTER ARCHITECTURE

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) The inter-instruction dependencies in program cause

      a) data hazards b) structural hazards

      c) control hazards d) both (a) and (b).

   ii) The advantage of RISC over CISC processor is that

      a) hardware architecture is simpler

      b) an instruction can be executed in one cycle

      c) less number of registers accommodate in chip

      d) parallel execution capabilities.

   iii) The mode field determines

      a) the type of addressing

      b) the type of operand

      c) the type of instruction format

      d) the type of arithmetic or logic operation.

   iv) Associative memory is a

      a) pointer addressable memory

      b) content addressable memory

      c) slow memory

      d) none of these.

   v) One *n*-bit processor has

      a) data bus of size *n*-bit

      b) address bus of size *n*-bit

      c) system bus of size *n*-bit

      d) none of these.

   vi) In case of superscalar processor

      a) CPI is less than 1

      b) CPI is greater than 1

      c) CPI is equal to 1

      d) CPI cannot be measured (indeterminate).

vii) In case of little-endian memory

a) lower-order byte is stored to higher-order address

b) reverse of (a)

c) same as big-endian

d) none of these.

viii) In a microprocessor the address of the next instruction to be executed in stored in

a) Stack pointer

b) Address latch

c) Program counter

d) General purpose register.

ix) Cache memory

a) increases performance

b) reduces performance

c) machine cycle increases

d) none of these.

x) A page fault

a) occurs when a program accesses a main memory

b) is an error in a specific page

c) is an access to a page currently not residing in main memory

d) is a reference to a page currently residing in main memory.

xi) A 'hit' occurs

a) when word is found in virtual memory

b) when word is found in cache memory

c) when word is not found in virtual memory

d) when word is not found in cache memory.

xii) Delayed branching is related to

a) pipeline hazard b) pipeline remedy

c) both (a) and (b) d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Evaluate the following arithmetic statement using three, two, one, zero address instructions and RISC instructions :

$X = (A + B) * (C + D)$

3. a) What is virtual memory and why is it called virtual ?

b) What do you mean by logical address space and physical address space ? 3 + 2

4. Explain von Neumann architecture with clear diagram.

5. Write a VHDL program of 4-bit adder using structural modelling.

6. Write down different characteristics of RISC and CISC architecture.

GROUP – C
(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) What is meant by 'Pipeline architecture' ?

   b) What are pipeline hazards ?

   c) A non-pipeline system takes 40 ns to process a task. The same task can be processed in a four segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 50 tasks. What is the maximum speed up that can be achieved in this case ?

   d) What do you mean by speed-up, efficiency and throughput of a pipelined processor ? 3 + 6 + 3 + 3

8. a) Multiply (+ 13) and (– 6) following Booth's algorithm.

   b) Explain how computation time (for addition) is reduced in carry look-ahead adder.

   c) Write down the names of the generic addressing modes to address an operand.

   d) Compare RISC with CISC. 5 + 4 + 3 + 3

9. a) Explain the working principle of direct mapping of cache memory.

   b) According to the following information, determine the size of the subfields (in bits) in the address for direct mapping, associative mapping and set associative mapping cache schemes :

      i) Main memory size is 256 MB, Cache memory size is 1 MB

      ii) The address space of the processor is 256 MB

      iii) The block size is 128 bytes

      iv) No. of blocks in a cache set is 8. 5 + 10

10. a) Why DMA based I/O is better than I/O techniques ?

    b) Differentiate between isolated I/O and memory mapped I/O.

    c) Explain DMA based data transfer operation between memory and other peripheral.

    d) What is the difference between vectored and non-vectored interrupt ? 3 + 3 + 3 + 4 + 2

11. Write short notes on any *three* of the following : 3 × 5

a) Flynn's Classification

b) Harvard Architecture

c) Bus organization using tri-state buffer

d) Paging

e) Associative memory.