

Name :

Roll No. :

Invigilator's Signature :

CS/B.Tech/SEM-2/EC-201/2010

2010

BASIC ELECTRONICS ENGINEERING

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

10 × 1 = 10

- i) If the temperature of an *n*-type semi-conductor is increased then it becomes
 - a) more *n*-type
 - b) *p*-type
 - c) intrinsic
 - d) none of these.
- ii) Compared to avalanche diode, Zener diode has
 - a) less doping concentration
 - b) less barrier field intensity
 - c) higher barrier field intensity
 - d) higher depletion width.



- iii) Forbidden energy gap of silicon at 0 K is
- a) 0.78 eV b) 1.2 eV
- c) 1.5 eV d) 0.3 eV.
- iv) The major part of current flowing in an intrinsic semiconductor is due to the drift of
- a) conduction band electrons
- b) conduction band holes
- c) valence band electrons
- d) valence band holes.
- v) The capacitance of a varactor diode can be changed by varying its
- a) doping level b) temperature
- c) forward bias d) reverse bias.
- vi) If a resistor has the colour code yellow-violet-gold, the value of the resistor is
- a) 47 Ω b) 0.47 Ω
- c) 470 Ω d) 4.7 Ω .
- vii) SCR may be turned off by
- a) interrupting its anode current
- b) reversing polarity of anode-cathode voltage
- c) both (a) & (b)
- d) none of these.



- viii) Voltage series negative feedback
- a) increases input & output impedances
 - b) increases input impedance & decreases output impedance
 - c) decreases input & output impedances
 - d) increases output impedance & decreases input impedance.
- ix) In reverse biased condition junction capacitance of step graded PN-junction diode varies proportionally
- a) $V^{-1/2}$
 - b) $V^{-1/3}$
 - c) $V^{-1/4}$
 - d) none of these.
- x) Without a DC source a clipper acts like a
- a) rectifier
 - b) clamper
 - c) chopper
 - d) demodulator.
- xi) Integrated circuit acts as a/an
- a) LPF
 - b) HPF
 - c) BPF
 - d) none of these.
- xii) Output impedance of an ideal op-amp is
- a) 0
 - b) 75 ohm
 - c) 100 k ohm
 - d) none of these.
- xiii) The value of CMRR for an ideal op-amp is
- a) 0
 - b) 1
 - c) infinite
 - d) none of these.



- xiv) The maximum efficiency of a full-wave rectifier can be
- a) 37.2% b) 40.6%
- c) 53.9% d) 81.2%.
- xv) If the line frequency is 60 Hz, the output frequency of a bridge rectifier is
- a) 30 Hz b) 60 Hz
- c) 120 Hz d) 240 Hz.

GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Explain how Zener diode can be used as a reference voltage source.
3. Compare between an FET and a BJT.
4. Explain the working of an integrator circuit using ideal op-amp.
5. For what purpose is a triggering circuit provided in a CRO ?
Explain how a CRO is used to measure the frequency of an alternating current flowing in a circuit.
6. An amplifier has a voltage gain of 200. The gain is reduced to 50 when negative feedback is applied. Determine feedback factor β and express the amount of feedback in dB.



GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following.

3 × 15 = 45

7. a) What are the advantages of negative feedback ? 3
- b) Explain with proper diagram the configuration of current series and current shunt feedback circuit. 8
- c) Distinguish among Class A, Class B and Push-pull amplifiers. 4
8. a) Write the working principle of JFET with diagram. 6
- b) Define Transconductance, AC drain resistance, Amplification factor of JFET. 3
- c) Draw the common source JFET amplifier circuit and find out the expression for voltage gain, input impedance and output impedance. 4
- d) Write three differences between JFET and MOSFET. 2
9. a) Explain the Ebers-Moll Model. 5
- b) What are the factors that affect the bias stability of a transistor ? 3



c) What is early effect ?

2

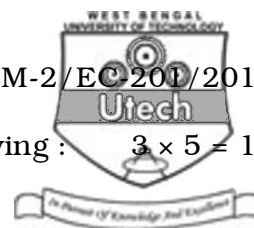
d) Draw the circuit diagram for self bias configuration considering an $n-p-n$ transistor in the CE configuration.

Derive the expressions for its stability factors. 3 + 2

10. a) The metal lead of the p -side of a $p-n$ diode is soldered to the metal lead of the p -side of another $p-n$ diode. Will the structure form an $n-p-n$ transistor ? Why ? 3

b) Draw the common emitter circuit of a transistor. Sketch its output characteristics. Indicate the active, cut-off and saturation regions. 7

c) For a silicon BJT as shown in the following figure, find R_B to establish $V_{CE} = 2 \text{ V}$. Assume $V_{BE} = 0.7 \text{ V}$. 5



11. Write short notes on any *three* of the following : $3 \times 5 = 15$

- a) Early effect
- b) Clipper circuit
- c) UJT
- d) Enhancement and depletion type CMOS
- e) Hybrid parameters for a transistor.

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