b) Write down the excitation table and convert SR to JK flip-flop.

c) Describe the operation of a bidirectional universal shift register (with parallel load) with a neat diagram. 5 + 5 + 5

8. a) Explain the operation of a Wien-bridge oscillator.

b) Derive an expression for its frequency of oscillation.

c) Write the condition of oscillation & application of oscillators. 5 + 6 + 2 + 2

9. a) Design a divide by 5 asynchronous down counters.

b) Explain the operation of a ring counter with proper circuit diagram and waveform. 7 + 8

10. a) Design a full-adder using a decoder.

b) Design a logical circuit that will detect illegal BCD code.

c) Implement half-subtractor using MUX. 6 + 6 + 3

11. a) Minimize the following expression using Karnaugh Map.

i) $F(A, B, C, D) = \prod M(0, 1, 3, 8, 10, 15) + \prod d(11, 13, 14)$

ii) $F(A, B, C, D) = \Sigma m(0, 1, 2, 5, 8, 14) + \Sigma d(4, 10, 13)$

b) Draw the circuit for a 4-bit Johnson counter using *D* flip-flop & explain its operation. Draw its timing diagram. How does its timing diagram differ from that of Ring counter ? 6 + 9

2013
ANALOG & DIGITAL ELECTRONICS

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

***Candidates** are required to give their answers in their own words as far as practicable.*

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

i) An amplifier that operates in the linear region at all times is

a) Class *A* b) Class *B*

c) Class *AB* d) Class *C*.

ii) The maximum theoretical efficiency of Class *A* power amplifier is

a) 50% b) 25%

c) 75% d) 98%.

iii) Cross-over distortion is a problem for

a) Class *A* amplifiers b) Class *B* amplifiers

c) Class *C* amplifiers d) Class *AB* amplifiers.

iv) The operation which is commutative but *not* associative is

a) AND b) XOR

c) NAND d) NOT.

v) The flip-flop required to design a MOD-18 counter is

a) 3 b) 5

c) 4 d) 6.

vi) Hexadecimal equivalent of the binary no. 10111010001111 is

a) 2E8F b) 1E7A

c) 2F3B d) 1E9D.

vii) Minimum number of NAND gates required to implement the XOR gate of two variables is

a) 5 b) 7

c) 4 d) 3.

viii) Fastest logic gate family is

a) CMOS b) TTL

c) ECL d) RTL.

ix) A carry look ahead adder is frequently used for addition, because it

a) is faster b) is more accurate

c) uses fewer gates d) costs less.

x) Two 4-bit 2's complements of binary numbers 1011 and 0110 are added. Then the result will be

a) 1111 b) 0010

c) 1101 d) 0001.

xi) The number of min. terms of 4 variables is

a) 16 b) 8

c) 4 d) 2.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

a) Distinguish between latch and flip-flop.

b) Distinguish between ripple counter and synchronous counter. 2 + 3

c) Draw a BCD adder circuit to add two BCD numbers maximum up to 9. The output of this adders should be in BCD.

d) Subtract 111001_2 from $(101011)_2$ using 2's complement method. 3 + 2

e) Implement the following function using 4 : 1 multiplexer : $F(A, B, C) = \sum m(1, 3, 5, 6)$.

f) Write the application of multiplexer. 4 + 1

g) Draw the basic logic circuit arrangement of a 3 bit ripple counter using flip-flop and briefly describe the operational principle.

h) Implement the function $F(A, B, C) = \sum_m (1, 3, 5, 6)$ using decoder. What is the difference between combination circuit & sequential circuit ? 3 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

a) Draw and explain the master-slave J-K flip-flop using NAND gate.