MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

EC-504A

COMPUTER ARCHITECTURE

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.
All symbols are of usual significance.

GROUP A
(Multiple Choice Type Questions)

1. Answer *all* questions. $10 \times 1 = 10$

(i) Priority interrupt may be accomplished by
(A) daisy chain
(B) polling
(C) parallel method of priority interrupt
(D) all of these

(ii) CPU gets the address of next instruction to be processed from
(A) Instruction register (B) Memory address register
(C) Program counter (D) Index register

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(iii) The logic circuit in ALU is
(A) content addressable memory (B) entirely combinational
(C) slow memory (D) both (A) and (B)

(iv) The principle of locality justifies the use of
(A) polling (B) DMA
(C) interrupts (D) cache memory

(v) Instruction cycle is
(A) fetch-decode-execution (B) fetch-execution-decode
(C) decode-fetch-execution (D) none of these

(vi) Cache memory is used to enhance the speed of
(A) processor (B) hard disk
(C) RAM (D) all of these

(vii) Bi-directional buses are
(A) tri-state buffers
(B) two tri-state buffers in cascade
(C) two back to back connected tri-state buffers in parallel
(D) two back to back connected buffers

(viii) In fourth generation computers the technology used is
(A) SSI (B) LSI
(C) VLSI (D) LSI and VLSI

(ix) The last statement of any symbolic microprogram must contain
(A) OVER (B) NEXT
(C) FETCH (D) none of these

(x) Cache memory
(A) increases machine cycle (B) increases performance
(C) both (A) and (B) (D) none of these

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GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. Discuss Harvard architecture. 5

3. What is virtual memory? Write the advantages of virtual memory. 2+3

4. What is interrupt? Differentiate between vectored and non vectored interrupts. 2+3

5. What is vector processing? With an example explain the difference between scalar and vector operation. 2+3

6. What do you mean by cache hit and cache misses? What is 'TLB'? 3+2

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) Describe the function of major components of a digital computer. 7+4+2+2

   (b) Discuss the role of an operating system in a computer system.

   (c) Explain the advantages and disadvantages of a parallel adder over a serial adder.

   (d) Distinguish between carry look ahead adder and a ripple carry adder.

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8. (a) State in brief different techniques to improve cache memory performance. 9+(3+3)

   (b) A hierarchical cache-main memory subsystem has the following specification:
   (i) Cache memory access time: 83 ns
   (ii) Main memory access time : 147 ns
   (iii) Hit ratio of cache memory :0.85,
   Calculate (i) Average access time of the memory system,
   (ii) Efficiency of the memory system.

9. (a) Discuss the working principle of a synchronous linear pipeline. 5+6+4

   (b) Define (i) speed up (ii) efficiency (iii) throughput.

   (c) Suppose the time delays of six stages of a linear synchronous pipeline; t_1, t_2, t_3, t_4, t_5, t_6 are 70, 80, 60, 70, 85, 83 ns respectively. The interface latch has a delay of 3 ns. Calculate
   (i) The minimum value of clock duration and maximum clock frequency.
   (ii) Maximum speed up of this pipeline over its equivalent non-pipeline counterpart.

10.(a) What is the role of cache memory in computer architecture? 3+3+6+3

   (b) What do you mean by 'locality of reference' in cache memory?

   (c) Write the working principle of set associative mapping.

   (d) Distinguish between L1 and L2 level cache memory.

11.(a) Why DMA based I/O is better than I/O techniques? 4+3+4+4

   (b) Differentiate between isolated I/O and memory mapped I/O.

   (c) Explain DMA based data transfer operation between memory and other peripheral.

   (d) What is the difference between vectored and non vectored interrupt?

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