2014

Advance Computer Architecture

Time Alloted : 3 Hours *Full Marks : 70*

The figure in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP - A
(Multiple Choice Type Questions)

1. Choose the most appropriate alternative for the following : 10x1=10

i) The degree of parallelism of the superscalar processor is constrained by the
   a) Resource conflicts b) Data dependency
   c) Both (a) and (b) d) None of these

ii) CPI of RISC processor is
   a) =1 b) >1
   c) <1 d) >10

iii) The most general and latest performance metric is
   a) Clock speed b) MIPS
   c) No of instruction d) No of register

iv) Hardwired control unit is used in processor

a) CISC b) RISC

c) Both (a) and (b) d) None

v) In SPARC processor, at any instant, a program can address

a) 8 registers b) 24 registers

c) 32 registers d) 64 registers.

vi) For two instructions I and J, RAW hazard occurs if

a) $R(I) \cap D(J) \neq \varnothing$ b) $R(I) \cap R(J) \neq \varnothing$

c) $D(I) \cap R(J) \neq \varnothing$ d) None

vii) The seek time of a disk is 30 ms. It rotates at a rate of 30 rotations/second. The capacity of each track is 300 words. The access time is approximately

a) 62 ms b) 60ms

c) 42 ms d) None

viii) Which of the followings are examples of 2-dimentional topologies in static networks?

a) Linear array b) Mesh

c) 3 CCC networks d) None

ix) Code reordering technique is a solution to

a) Control hazard b) Data hazard

c) Both (a) and (b) d) None

x) NUMA model is an example of

a) SIMD processor b) MIMD processor

c) MISD processor d) None

GROUP B

(Short Answer Type)

Answer any *three* of the following 3x5=15

2. What do you mean by load-store architecture? How the load-store architecture helps RISC processors to increase the throughput?

2+3

3. Consider the execution of an object code with 200,000 instructions on a 40-MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment:

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

a) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.

b) Calculate the corresponding MIPS rate based on the CPI obtained in part (s).

3+2

4. Describe different type of data routing function for inter processing element (PE) routing network.

5

5. Explain the inclusion property and memory coherence require-

ments in a multi level memory hierarchy. Distinguish between write through and write back policies in maintaining the coherence in adjacent levels.

5

6. Develop two algorithms for fast multiplication of two n x n matrices with a system of p processors, where $1 < p < n^3 / \log n$. Choose an appropriate PRAM model to prove that matrix multiplication can be done in $T = O(n^3 / p)$ time.

a) Prove that $T = O(n^2)$ if $p = n$.

b) Show the parallel algorithm with $T = O(n)$ if $p = n^2$

3+2

GROUP - C

(Long Answer Type)

Answer any three of the following.

3x15=45

7. a) Characterize the architectural operations of SIMD and MIMD computers.

b) Distinguish between multiprocessor and multicomputers based on their structure, resource sharing and interprocessor communications.

c) Explain the differences among UMA, NUMA and COMA computers.

d) The following code segment, consisting of six instructions, needs to be executed 64 times for the evaluation of vector arithmetic expression : $D(I) = A(I) + B(I) \times C(I)$ for $0 \le I \le 63$.

Load R1, B(I)	//R1 ← Memory (X + I)
Load R2, C(I)	//R2 ← Memory (Y + I)
Multiply R1, R2	//R1 ← (R1) x (R2)
Load R3, A(I)	//R3 ← Memory (Z + I)
Add R3,R1	//R3 ← (R3) + (R1)
Store D(I), R3	//Memory (P + I) ← (R3)

Where R1, R2 and R3 are CPU registers, (R) is the content of R1, X, Y, Z and P are the starting memory addresses of arrays B(I), C(I), A(I) and D(I), respectively. Assume 4 clock cycles for each Load or Store, 2 cycles for the Add and 8 cycles for the Multiply on either a uniprocessor or a single PE in an SIMD machine.

i) Calculate the total number of CPU cycles needed to execute the above code segment repeatedly 64 times on an SISD uniprocessor computer sequentially, ignoring all other time delays.

ii) Consider the use of an SIMD computer with 64 PEs to execute the above vector operations in six synchronized vector instructions over 64-component vector data and both driven by the same-speed clock. Calculate the total execution time on the SIMD machine, ignoring instruction broadcast and other delays.

iii) What is the speedup gain of the SIMD computer over the SISD computer?

3+4+3+5

7. a) What are the conditions of parallelism ?

b) Define Bernstein's conditions for parallelism.

c) Perform a data dependence analysis on each of the following Fortran program fragments. Show the dependence graphs (data dependence and resource dependence) among the statements with justification.

i)

S1: A = B + D

S2: C = A x 3

S3: A = A + C

S4: E = A / 2

ii)

S1: X = SIN(Y)

S2: Z = X + W

S3: Y = -2.5 x W

S4: X = COS(Z)

3+4+4+4

9. a) Discuss the concept of data flow architecture using an example.

b)What is the basic purpose of data flow architecture? Compare it with control flow architecture.

c)Write down the difficulties for implementation of data flow architecture.

d) Describe different type of grain and their relation for implementing parallelism.

(5+3+2+5)

10. a) What is memory hierarchy? Briefly describe different memories used.

b) How does cache memory increase the throughput of a computer in the light of locality of reference property.

c) Compare the relative merit and demerit of direct-mapping and fully associative cache memory organization.

(2+6)+3+4

11. a) You are asked to perform to capacity planning for a two level memory system. The first level M1 is a cache with capacity 64KBytes. Second level M2 is a main memory with a 4MByte capacity. Let c1 and c2 be the cost per byte and t1 and t2 the access time for M1 and M2 respectively . Assume c1 =20c2 and t2=10t1. The cache hit ratio is 0.7.

i) What is the average access time in terms of t1=20 ns.

ii) Express the average Byte cost of the entire memory hierarchy if c2=$0.2/Kbyte.

b) Distinguish between write -back and write -through policies in maintaining the coherence in adjacent levels.

c) Explain different type of locality associated with program/ data access in memory hierarchy.

((3+3)+4+5)