CS/B.Tech (ECE-NEW) (Supple)/SEM-7/EC-702(N)/09
EDA FOR VLSI DESIGN (SEMESTER - 7)

1. ..... *Signature of Invigilator*

2. ..... *Signature of the Officer-in-Charge*

Reg. No. | | | | | | | | | | | | | | |

Roll No. of the Candidate | | | | | | | | | | | | | | |

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CS/B.Tech (ECE-NEW) (Supple)/SEM-7/EC-702(N)/09
ENGINEERING & MANAGEMENT EXAMINATIONS, JULY – 2009
EDA FOR VLSI DESIGN (SEMESTER - 7)

Time : 3 Hours] [Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. This Booklet is a Question-cum-Answer Booklet. The Booklet consists of **32 pages**. The questions of this concerned subject commence from Page No. 3.
2. a) In **Group – A**, Questions are of Multiple Choice type. You have to write the correct choice in the box provided **against each question**.
   b) For **Groups – B** & **C** you have to answer the questions in the space provided marked 'Answer Sheet'. Questions of **Group – B** are Short answer type. Questions of **Group – C** are Long answer type. Write on both sides of the paper.
3. **Fill in your Roll No. in the box** provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. **Use of Mobile Phone and Programmable Calculator is totally prohibited in the examination hall.**
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, **which will lead to disqualification**.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

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Marks Obtained

	Group – A										Group – B				Group – C				
Question Number																	***Total Marks***	***Examiner's Signature***
Marks Obtained																		

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Head-Examiner/Co-Ordinator/Scrutineer

S–53034 (29/07) (N)

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EDA FOR VLSI DESIGN

SEMESTER - 7

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) 'EDA' stands for

a) Electronic Device Automation

b) Electrical Design Automation

c) Electronic Design Automation

d) Electrical Device Automation.

ii) Which of the following is not a part of FPGA cell ?

a) Logic Module b) IOB

c) Interconnect d) Product Term Array.

iii) Compared to conventional ICs FPGAs are

a) slower b) faster

c) less efficient in area d) none of these.

iv) "ISR" stands for

a) In Service Resource

b) Input System Reprogram

c) Input System Reprogrammability

d) In System Reprogrammability.

v) PLA has

a) 1 programmable plane

b) 2 programmable planes

c) 1 fixed and 1 programmable planes

d) 2 fixed planes.

vi) VHDL stands for

a) Verilog Hardware Description Language

b) Very High Speed Integrated Circuit Hardware Description Language

c) Valid Hardware Description Language

d) Very High Speed Integrated Circuit Hardware Display Language.

vii) The steps of implementation of FPGA must be carried out in the order

a) Synthesize – Place & Route – Map – Timing Simulate – Program

b) Synthesize – Map – Place & Route – Timing Simulate – Program

c) Program – Synthesize – Place & Route – Timing Simulate – Map

d) Program – Map – Place & Route – Timing Simulate – Synthesize.

viii) How many types of FPGAs is/are available ?

a) One type b) Two types

c) Three types d) Four types. ☐

ix) In VHDL, collection of commonly used data types and subprograms is called

a) Driver b) Attribute

c) Generic d) Package. ☐

x) Which of the following processes generates RTL model in VHDL programming ?

a) Simulation b) Compilation

c) Synthesis d) Boundary Scan. ☐

xi) Spartan-3E is a

a) High volume, Low power CPLD

b) World's lowest cost FPGA

c) GAL

d) Altera MAX-7000 series CPLD. ☐

xii) Physical Design Automation consists of

a) Placement, Floor Planning, Routing

b) Fault modelling, Simulation, Test generation

c) Datapath and Control synthesis

d) Logic Level Synthesis. ☐

xiii) PAL has

a) Fixed OR gate plane

b) Fixed AND gate plane

c) Both planes that are fixed

d) Both planes that are programmable. ☐

xiv) CMOS diffusion layers have

a) Moderate IR drop but low C

b) Low IR drop but high C

c) High IR drop

d) Low C. ☐

xv) Regularity of a VLSI circuit is defined as

a) total no. of transistor on the chip/no. of transistor circuits that must be designed in detail

b) no. of transistor circuits that must be designed in detail/total no. of transistor on the chip

c) total no. of transistor on the chip/total chip area

d) none of these. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 ∞ 5 = 15

2. What are the differences between FPGA and CPLD in terms of architecture and feature ?

3. What are slice, CLB, LUT ? Is it possible to configure CLB as RAM ?

4. Define 'package' and 'architecture' in VHDL. Write a VHDL code for tri-state buffer.

2 + 3

5. Explain the BIST techniques.

6. What are the several factors to improve propagation delay of standard cell ?

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 ∞ 15 = 45

7. a) What do you mean by test and testability of VLSI systems ?

   b) Define controllability and observability of VLSI circuits.

   c) Explain the D-algorithm for combinational logic.

   d) What do you mean by sensitized path based testing ? 4 + 4 + 4 + 3

8. a) Define physical design.

   b) Mention the need of physical design in VLSI.

   c) Explain the various steps of physical design.

   d) What is standard cell design ? How does it differ from gate-array design ?

2 + 2 + 6 + 2 + 3

9. a) What is FPGA ?

b) Compare Antifuse FPGA and SRAM based FPGA.

c) With diagram, explain the architecture of SRAM based FPGA.

d) What is JTAG ?

e) Write down the differences between CPLD and FPGA. 2 + 3 + 5 + 2 + 3

10. a) Write a VHDL code for LONG_WAY_SHIFTER given in the following figure.

Dia.

b) Write a VHDL code for 4:1 MUX using PROCESS.

c) What are the differences between 'If statement' and 'case statement' in VHDL ?

8 + 4 + 3

11. Write short notes on any *three* of the following : 3 ∞ 5

a) Floor planning

b) Application specific integrated circuits

c) Test generation

d) Analog Design automation tools

e) Optimization of Combinational circuits.

END