	Utech
Name:	
Roll No. :	To Planning Of Strengthing Staff Excellent
Invigilator's Signature :	

2012 EMBEDDED SYSTEM

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A (Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following:

 $10 \times 1 = 10$

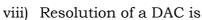
- i) In embedded system design actuator acts as a
 - a) Input device
- b) Output device
- c) Memory device
- d) Both (a) and (b).
- ii) USB stands for
 - a) Universal Serial Bus
 - b) Uniform Serial Bus
 - c) Universal Service Bus
 - d) None of these.

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- iii) VLIW processor means
 - a) Very Large Instruction Word
 - b) Very Low Integrated Word
 - c) Very Load Instruction Word
 - d) None of these.
- iv) Sigma-delta converter is a
 - a) A to D converter
 - b) D to A converter
 - c) both (a) and (b)
 - d) none of these.
- v) Which one is not embedded in a single chip in an embedded system?
 - a) Memory
- b) Processor
- c) A to D converter
- d) None of these.
- vi) Fastest type of ADC is
 - a) Flash type
 - b) Dual-slope
 - c) Successive-approximation
 - d) None of these.
- vii) Strain gauge has a property called
 - a) Piezo-resistive
- b) Piezo-electric
- c) Photo-electric
- d) None of these.









c) 2^n

- d) none of these.
- ix) Among the following which one has the greatest gate integration capacity?
 - a) FPGA

b) CPLD

c) ASIC

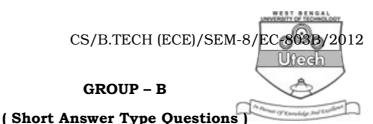
- d) PLD.
- x) Configurable logic blocks are used in
 - a) Gate array design
 - b) Full custom design
 - c) FPGA design
 - d) Standard cell based design.
- xi) A microphone has a diaphragm behaving like a
 - a) capacitive device
- b) resistive device
- c) inductive device
- d) active device.
- xii) The *Z*-transform of $\delta(t kT)$ for k = 0 to ∞ is
 - a) $\sum_{k=0}^{\infty} z^{-k}$
- b) $\sum_{k=0}^{\infty} z^k$
- c) $\sum_{k=0}^{\infty} (1-z)^{-k}$
- d) $\sum_{k=0}^{\infty} (1-z^{-k})$.



xiii) In Harvard architecture

- a) separate address and data buses are used to access program and data memory
- b) same address and data buses are used to access program and data memory
- c) separate address bus but same data buses are used to access program and data memory
- d) same address bus but separate data buses are used to access program and data memory.
- xiv) Sequential execution of program statements pre-stored in memory is the fundamental principle of
 - a) von Neumann computing
 - b) dataflow computing
 - c) pipelining
 - d) embedded processors.
- xv) Maximum efficiency of pipelined computing can be obtained when the pipe is
 - a) full
 - b) empty
 - c) partially full
 - d) full in an interleaved manner.

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(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

- 2. a) Define system on chip (SOC) with example.
 - b) Distinguish between hard and soft real time systems.

2 + 3

- 3. a) How watchdog timer is different from normal timer?
 - b) What is its importance in embedded system? 3 + 2
- 4. State various features in RTOS. 5
- 5. Explain the FPGA architecture with proper diagram. 5
- 6. How does DSP differ from general purpose processor (GPP)?

 Why is SIMD architecture common among DSPs? 3 +2

GROUP - C

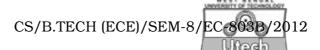
(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

- 7. a) What do you mean by hardware-software co-design? Explain it with a suitable block diagram.
 - b) Describe the different components of an embedded system.
 - c) Describe the design methodology of an embedded system.
 - d) Describe the different types of microphones are used in an embedded system. 3 + 3 + 3 + 6



- 8. a) Compare CISC and RISC.
 - b) What do you mean by pipeline processing?
 - c) Discuss various registers and 3-stage pipelining concept used in ARM 7 embedded processor. 4 + 2 + 9
- 9. a) Design a PAL to realize $Y_1 = AB'C + A'B \text{ and }$ $Y_2 = A'BC + AB'$
 - b) Draw the architecture of a basic module in Macrocell's p-ASIC FPGA architecture
 - c) How will you realize a half adder on the above architecture?
 - d) State one approach of mapping the synthesized logic in a computer on to FPGA. 5 + 3 + 4 + 3
- 10. a) A successive approximation type analog -to- Digital Convertor (ADC) has a clock frequency of 100 kHz. If the word length of the ADC is 8-bits, considering one additional clock cycle for latching the digital output to a register, what is the time required to convert one analog value of the sampled signal?
 - Explain the logic used to synthesize the binary patterns over the clock cycles in Successive Approximation type ADC.
 - c) A 4-bit Digital-to-Analog Converter (ADC) has a binary input pattern = 1 1 0 1. If the maximum (full scale) voltage is 5 V, what is the analog equivalent of the binary input?
 - d) Which is the fastest ADC and why? 4 + 5 + 4 + 2



11. Write short notes on any three of the following:

- $3 \times 5 = 15$
- a) Cache memory and Cache controller.
- b) Sigma-Delta type ADC.
- c) Pressure and Temperature sensors.
- d) JTAG.
- e) UART.
- f) Design of 4bit ALU and a 4 bit counter using any embedded software language.

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