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cuss how 8253 is used to generate square wave?	2
lain the major components and priority modes of 8259	2+2
te the BSR control word for setting PC2 in 8255	1
t are the main functions performed by BIU and EU unit of 8086 microprocessor?	5
is pipelining achieved in 8086 microprocessor?	4
ribe different addressing modes of 8086 microprocessor.	4
t is the difference between 8086 and 8088 microprocessor?	2
the timing diagram of OUT 08 Instruction stored from memory location 8000H.	4
do you mean by mode 0, mode 1 and mode 2 operation in 8255?	5
are the functions of major components in 8259 interrupt controller?	4
is polling in 8259?	2
in interrupts in 8051 microcontroller.	3
is meant by subroutine? Briefly discuss the sequence of events that take place executing CALL instruction.	2+2
n the burst mode transfer and cycle stealing in context of DMA data transfer e.	2+2
of eight readings is stored in memory location starting at XX50H. Write a n to check whether 40H exists in the set or not. If present, then stop checking re the corresponding memory location in XXA0H and XXA1H. Otherwise FH at ZZA0H.	4
l): 42, 38, 32, 48, F2, 40, 82, 8A.	
hort notes on any *three* of the following.	3×5
ing modes of 8051 microcontroller.	
d RLC instructions in 8085 µp.	
ture of Intel 8255A.	
x mode operations of 8086 µp.	
rocontroller.	

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EC-502

MICROPROCESSOR AND MICROCONTROLLER

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. 10×1 = 10

(i) MOV A, M is executed by
(A) 1 machine cycle (B) 2 machine cycle
(C) 3 machine cycle (D) 4 machine cycle

(ii) 8253 has
(A) 6 modes of operation (B) 5 modes of operation
(C) 4 modes of operation (D) 3 modes of operation

(iii) When PUSH instruction is executed, the stack pointer register is
(A) decremented by two (B) incremented by two
(C) decremented by one (D) incremented by one

(iv) The program counter (PC) in a microprocessor
(A) keeps the address of the next instruction to be fetched
(B) counts the number of instructions being executed on the microprocessor
(C) count the number of program being executed on the microprocessor
(D) counts the number of interrupts handled by the microprocessor

(v) The USART perform
(A) A serial-to-parallel conversion (B) parallel-to-serial converter
(C) control and monitoring function (D) all of these

(vi) Which of the following signals indicates an 8-bit data transfer from odd address bank?
(A) A_0 = 0 and BHE = 0 (B) A_0 = 1 and BHE = 1
(C) A_0 = 0 and BHE = 1 (D) A_0 = 1 and BHE = 0

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· 8051 microcontroller has

4 K-Bytes of on-chip ROM (B) 8 K-Bytes of on-chip ROM
16 K-Bytes of on-chip ROM (D) 32 K-Bytes of on-chip ROM

· Bit Set Reset mode in 8255 is used with one of the following

port A (B) port B (C) port C (D) none of these

it are the conditions that BIU can suspend fetching instruction?

current instruction requires access to memory or I/O port
a transfer control (jump or call) instruction occurs
transfer queue is full
none of these

ch one of the following is the software interrupt of 8085 microprocessor?

RST 7.5 (B) EI (C) RST 1 (D) Trap

DMA request is sent to the microprocessor with a high signal to the HOLD pin, microprocessor acknowledges the request

fter completing the present cycle
nmediately after receiving the signal
fter completing the program
one of these

ack and stack pointer

oth reside in memory
th reside in CPU
rmer reside in memory and the later in CPU
rmer reside in CPU and the latter in memory

ddressing mode of the instruction LDAX B is

ect (B) register indirect
plicit (D) immediate

struction PCHL

res the content of HL pair to a specified memory location
ies the content of HL pair to the program counter
es the content of HL pair to accumulator
hanges the content of HL pair with the program counter

(xx) The instruction register holds

(A) flag condition (B) op-code
(C) instruction address (D) hex code

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. What is the difference between Latch and a Buffer? Explain why a Latch is used for an output port, but a tri-state buffer can be used for an input port. 5

3. How does the ALE signal demultiplex the AD0–7 bus? Explain with diagram. 5

4. (a) Define addressing mode in 8085 microprocessor. 2+3
   (b) How many addressing modes are available in 8085 microprocessor? Explain with two examples each.

5. (a) What is pipelined architecture? How is it implemented in 8086 microprocessor? 1+2+2
   (b) How many address lines are used for I/O mapped I/O technique in the context of interfacing with 8086?

6. (a) Explain the function of the following pins of 8085. 2+3
   READY, INTR
   (b) Discuss the functions of the following instructions of 8085:
   ADC H, LHLD 9000H

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) What are vectored and non-vectored interrupts? 2
   (b) Explain the instruction RIM and SIM. Write a program to calculate the no of even and odd number from a set of eight 8 bit data stored from memory location 8030H and the result will be stored in 8050H and 8060H. 2+2+2