MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

CS-303

COMPUTER ORGANIZATION

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable. All symbols are of usual significance.

GROUP A
(Multiple Choice Type Questions)

1. Answer *all* questions. $10 \times 1 = 10$

(i) The maximum number of additions and subtractions are required for which of the following multiplier numbers in Booth's algorithm?

(A) 01001111 (B) 01111000
(C) 00001111 (D) 01010101

(ii) In the processor, the address of the next instruction to be executed is stored in

(A) stack pointer register (B) index register
(C) base register (D) program counter register

(iii) By logical left-shifting the content of a register once, its content is

(A) doubled
(B) halved
(C) both (A) and (B)
(D) no such decision can be made

(iv) If k be the number of registers and n be the size of each register, then in order to construct n-line common bus system using tri-state buffers, the total number of tri-state buffers and the size of decoder would be

(A) $n*k$ and 2-to-4 (B) $n*k$ and $\log_2 k$-to-k
(C) k and $\log_2 n$-to-n (D) $n*k$ and $\log_2 n$-to-n

(v) The principle of locality justifies the use of

(A) interrupt (B) polling
(C) DMA (D) cache memory

(vi) Instruction cycle is

(A) fetch-decode-execution (B) fetch-execution-decode
(C) decode-fetch-execution (D) none of these

(vii) Subtractor can be implemented using

(A) adder (B) complementer
(C) both (A) and (B) (D) none of these

(viii) How many RAM chips of size (256 K × 1 bit) are required to build 1M Memory?

(A) 24 (B) 10 (C) 32 (D) 8

(ix) Maximum n bit 2's complement number is

(A) 2^n (B) $2^n - 1$
(C) $2^{n-1} - 1$ (D) cannot be said

(x) Micro instructions are kept in

(A) main memory (B) control memory
(C) cache memory (D) none of these

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. (a) What is tri-state buffer? Construct a single line common bus system using tri-state buffer. 1+2
   (b) What are guard bits? 2

3. Describe stack based CPU. 5

4. (a) Write $+7_{10}$ in IEEE 32 bit format. 2
   (b) Convert IEEE 32-bit format 40400000_{16} in decimal value. 3

5. Evaluate the following arithmetic expression into three-address, two-address, one-address, zero-address instruction format. 5

$$X = (A + B) * C$$

6. (a) Explain the difference between full associative and direct mapped cache memory mapping approaches. 3
   (b) What are "write back" and "write through" policies in cache? 2

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) Suppose register A holds the 8-bit number 11011101. Determine the sequence of binary values in A after an arithmetic shift-right, followed by a circular shift-right and followed by a logical shift-left. 3
   (b) Describe Booth's multiplication method and use this to multiply decimal numbers -23 and 9. 8
   (c) Suppose we are given RAM chips each of size 256 × 4. Design a 2K × 8 RAM system using this chip as the building block. Draw a net logic diagram of your implementation. 4

8. (a) For Booth's algorithm, when do worst case occur? Explain with example.
   (b) What are the advantages of Interrupt I/O over I/O?
   (c) Discuss the concept of associative memory with example.

9. (a) Write a program to evaluate the arithmetic statement $Y = (A - B + C)/(G + H)$.
   (i) Using an accumulator type computer with one address instruction.
   (ii) Using a stack organized computer with zero address instructions.
   (b) What is von Neumann bottleneck? How can this
   (c) A digital computer has a memory unit of 64K words. The cache uses a cache memory of 1K words with a block size of 4 words. How many bits are there in the tag, index, block and words fields of the address format? Also calculate address format for associative mapping and 4-way set associative mapping.

10. (a) Differentiate between hardwired control and microprogrammed control. Draw the block diagram of a hardwired control organization with two decoders, a sequence counter and a number of control logic gates.
   (b) A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.
   (i) How many selection inputs are there in each multiplexer?
   (ii) How many multiplexers are there in the bus?
   (c) Explain the basic DMA operations for transfer of data between memory and peripherals.

11. (a) Explain different hazards in pipelining.
   (b) What are vector interrupts? How are they used in implementing hardware interrupts?
   (c) What is speedup, throughput and efficiency of a pipelined architecture?