WEST BENGAL UNIVERSITY OF TECHNOLOGY

CS-403

COMPUTER ARCHITECTURE

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP A
(Multiple Choice Type Questions)

1. Answer *all* questions. 10×1 = 10

(i) The compiler optimization technique is used to reduce
(A) cache miss penalty (B) cache miss rate
(C) cache hit time (D) none of these

(ii) The CPI value for RISC processors is
(A) 1 (B) 2 (C) 3 (D) more

(iii) The vector stride value is required
(A) to deal with the length of vectors
(B) to find the parallelism in vectors
(C) to access the elements in multi-dimensional vectors
(D) none of these

(iv) The task of a vectorizing compiler is
(A) to find the length of vectors
(B) to convert sequential scalar instructions into vector instructions
(C) to process multi-dimensional vectors
(D) to execute vector instructions

(v) Utilization pattern of successive stages of a synchronous pipeline can be specified by
(A) truth table (B) excitation table
(C) reservation table (D) periodic table

(vi) The UMA multiprocessor system is best suited
(A) when the degree of interaction among different modules in program is large
(B) when the degree of interaction among different modules in program is less
(C) when there is no interaction among different modules in program
(D) when different programs are to be executed concurrently

(vii) The cache coherence is a potential problem especially
(A) in asynchronous parallel algorithm execution in multiprocessor
(B) in synchronous parallel algorithm execution in multiprocessor
(C) in asynchronous parallel algorithm execution in data flow m/c
(D) in synchronous parallel algorithm execution in data flow m/c

(viii) A direct mapped cache memory with n blocks is nothing but which of the following set associative cache memory organization?
(A) 0-way set associative (B) 1-way set associative
(C) 2-way set associative (D) n-way set associative

(ix) Array processors perform computations to exploit
(A) temporal parallelism (B) spatial parallelism
(C) sequential behavior of programs (D) modularity of programs

(x) The time to access shared memory is same in which of the following shared-memory multiprocessor model?
(A) NUMA (B) UMA
(C) COMA (D) ccNUMA

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. What are the different parameters used to measure the CPU performance? Briefly discuss each. 2+3

3. "Instruction execution throughput increases in proportion with the number of pipeline stages". Is it true? Justify your statement. 5

4. Use Bernstein's conditions for determining the maximum parallelism in the following sequence of instructions: 5

$A = B \times C$
$B = D + E$
$C = A + B$
$E = F - D$

5. Discuss data hazards briefly. 5

6. Briefly describe cache coherence problem with an example. Suggest one software protocol for this. 3+2

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) What is SPEC rating? Explain. 3

(b) A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts: 1+2+2

Instruction type	Instruction count	Clock cycle count
Integer arithmetic	50000	1
Data transfer	35000	2
Floating point arithmetic	20000	2
Branch	6000	3

Calculate the effective CPI, MIPS rate and execution time for this program

(c) Why do we need parallel processing? What are different levels of parallel processing? Explain. 2+5

8. (a) What is meant by pipeline hazard? Briefly discuss different pipeline hazards. 1+6

(b) What do you mean by job collision in pipeline processor? Show how collisions occur in the following static pipeline. 1+2

	0	1	2	3	4
S_0	X				X
S_1		X		X	
S_2			X		

(c) Consider the execution of a program of 20,000 instructions by a linear pipeline processor with a clock rate 40 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out-of-order executions are ignored. Calculate the speed-up of the pipeline over its equivalent non-pipeline processor, the efficiency and throughput.

9. (a) Why do we need masking mechanism in SIMD array processors? 1+
In an SIMD array processor of 8 PEs, the sum $S(k)$ of the first k components in a vector A is desired for each k from 0 to 7. Let $A = (A_0, A_1, \ldots\ldots, A_7)$. We need to compute the following 8 summations:

$$S(k) = \sum_{i=0}^{k} A_i \text{ ; for } k = 0,1,\ldots\ldots,7.$$

Discuss how data-routing and masking are performed in the processor.

(b) How do vector processors improve the speed of instruction execution over scalar processors? Illustrate with an example.

(c) What is vectorizing compiler? Why do we need it in a vector processor?

10.(a) What is the basic objective of data flow architecture? Compare it with control flow architecture 1+

(b) What is meant by the cache miss penalty? Briefly discuss "early restart" technique to reduce miss penalty. 1+

(c) Let us consider a memory system consisting of main memory and cache memory. In case of a cache miss, assume the performance of the basic memory organization as: 3+

- 4 clock cycles to send the address.
- 24 clock cycles for the access time per word.
- 4 clock cycles to send a word of data.

(i) What will be the miss penalty, given a cache block of four words?
(ii) What will be the memory bandwidth?

11.(a) Compare and contrast RISC and CISC computers. Give one example for each. 5

(b) What is multi-processor system? Classify it with examples. 1+3

(c) Design $2^2 \times 3^2$ Delta network. 6