.



ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE - 2007 DIGITAL ELECTRONIC CIRCUITS

SEMESTER - 4

ìm	e:3	Hours				[Full Marks : 70			
				GROUP - A					
•									
•	Cho	ose ti	he correct alternatives of	the following		$10\times1=10$			
	i)	Wh	ich of the following is sel						
		a)	Gray	b)	Excess-3				
		c)	BCD	d)	Parity code				
		e)	Hamming code.						
	ii)	Wh	ich one is known as refle	cted code ?					
		a)	Gray	b)	Excess-3				
		c)	BCD	ď)	Hamming code				
		e)	Parity code.						
***	iii)	(15) $_{10}$ – (27) $_{10}$ is equal to (using 2's complementing method):							
		a)	01100	b)	10100				
	4	c)	00100	d)	11100				
	× .	e)	01010.						
	iv)	v) 2's complement of which 5-bit binary number is the same number?							
	. • . · . · . · . · . · . · . · . · . ·	a)		b)	00001				
		c)	01000	d)	01111	• 0			
		e)	10000.						
			•						



CS/B.TECH(ECE-NEW)/SEM-4/EC-402/07



v)	If $\sqrt{(34)}$ is	equal to 5 in a partic	cular number	system, then	base of that	number
	system is		•		•	

5

6 b)

c) 7 d) 8

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- How many Flip-flops are required to design MOD-1024 counter?
 - a) 1024

b) 102

c) 10 d) 1

e) None of these.

- Resolution of n-bit DAC is given by
 - $1/(2^{n}-1)$ a)

b}

 $1/(2^{n}+1)$

- d)
- viii) To design an MOD-N Johnson Counter the number of FFs required are
 - a)

b) (N-1)

c) 7

- d) N/2.
- Race around condition occurs in a JK flip-flop when ix)
 - a) J=K=0

J = K = 1b)

c) J = 0, K = 1

- J = 1, K = 0.d)
- A memory has 16 bit address bus. The number of location in the memory are
 - a) 16

b) 32

1024 c)

d) 65536.

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GROUP - B

(Short Answer Type Questions)

Answer any three of the following.

 $3 \times 5 = 15$

- Check whether the Even parity Hamming code for 4-bit data. (1001011) 2 is correct or not. If not, correct the code.
- 3. Minimize the expression using K-Map technique;

$$Y(A, B, C, D) = ABCD + \overline{B}CD + \overline{A} \cdot \overline{B} + A + BD.$$

4. Implement the function using only one 8×1 MUX and (connect only B,C,D with select lines to select the data inputs)

$$F(A, B, C, D) = \Sigma m.(0, 1, 2, 5, 9, 11, 13, 15).$$

- Draw neat diagram of 4-bit Bi-directional shift register using mode control (M). When
 M is logic zero then left shift and right shift for M is logic one.
- 6. Design Adder/Subtractor composite unit using 4-bit binary full adder and necessary logic gates.

GROUP - C

(Long Answer Type Questions)

Answer any three questions of the following.

 $3 \times 15 = 45$

7. a) Minimize the following expression using K-map and realise the simplified function using NOR gates only

$$F(A, B, C, D) = \pi M(1, 2, 3, 8, 9, 10, 11, 14) d(7, 15)$$
 3+3

b) Find the complement of (735) 8

2

- c) Draw the logic circuit diagram for a 2-to-4 decoder with one active low enable line. Assume also that all the outputs of the decoders are active low.
- d) How do you cascade two 2-to-4 decoders to make one 3-to-8 decoder? Draw the necessary circuit.

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- WBU ON Utech
- 8. a) What is ROM and RAM? What is the basic difference between EPROM and EEROM?
 - b) A ROM is used to implement of the Boolean function:

$$F_1(A, B, C, D) = ABCD + \bar{A} \bar{B} \bar{C} \bar{D}$$

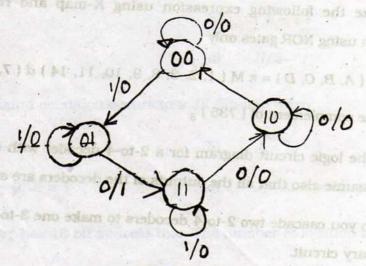
 $F_2(A, B, C, D) = (A + B) (\bar{A} + \bar{B} + \bar{C})$
 $F_3(A, B, C, D) = \sum 13, 15)$

- 1) What is the minimum size of ROM required?
- ii) Determine the data in each location of the ROM.

5 + 5

- 9. a) Draw the state table of a JK flip-flop and write down its characteristic equation.
 - b) Draw the circuit of Master / Slave JK flip-flop and explain the operation of the circuit.
 - c) What do you mean by 0's catching and 1's catching phenomena in the master / slave JK flip-flop?

 5 + 6 + 4
- 10. a) Describe the operation of a Flash Type A/D converter with proper circuit.
 - b) What are the advantages and disadvantages of the Flash Type A/D converter ? 3
 - c) Discuss the following TTL parameters briefly:
 - Floating input
 - ii) Fan-out
 - iii) Switching speed.
- 11. a) Draw the timing diagram of a MOD-10 counter where the MOD-10 counter is designed by cascading MOD-2 followed by MOD-5 counter units.
- b) Design a sequential circuit that implements the following state diagram. Use all D-type FF for the design. 7 + 8



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