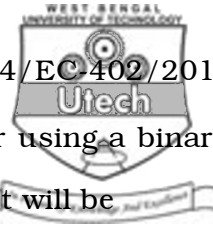


- 2



viii) The resolution of a 12-bit D/A converter using a binary ladder with + 10V as the full scale output will be

- a) 2.44 mV b) 3.50 mV
- c) 4.32 mV d) 5.12 mV.

ix) The initial state of MOD 16 down counter is 0110. The state after 37 clock pulse will be

- a) 0000 b) 0110
- c) 0101 d) 0001.

x) In a D type latch Enable i/p is HIGH, $D = 1$. The o/p will be

- a) 0 b) 1
- c) don't care d) blocked.

xi) The frequency of the pulse at point A is

- a) 10 kHz b) 31.25 Hz
- c) 50 Hz d) 5 kHz.

xii)



The value of F is

- a) $A \text{ XOR } B$
- b) $A \text{ XNOR } C$
- c) $A \text{ XOR } C$
- d) $B \text{ XNOR } C.$

xiii) Largest negative number that can be represented by 8-bit word length in 2's complement system is

- a) -255
- b) -128
- c) -127
- d) $-256.$

xiv) The logic family that gives fastest switching is

- a) CMOS
- b) ECL
- c) Schottky TTL
- d) DTL.



GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following.

3 × 5 = 15

2. Draw a BCD adder circuit to add two BCD numbers maximum up to 9. The output of this adder should also be in BCD.
3. Design a full subtractor circuit using multiplexer.
4. Construct a 2-bit comparator using only decoder.
5. a) Define the following terms related with digital IC :
 - i) Noise margin
 - ii) Propagation delay
 - iii) Fan-in & Fan-out.
- b) Write down the characteristic equation of JK & D Flip-flops.
6. What is the main difference between a latch and a flip-flop ?



GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following.

3 × 15 = 45

7. a) Write down the differences between combinational logic circuit & sequential logic circuit.
- b) Design a MOD 14 asynchronous UP/DOWN counter with JK flip-flop. 3 + 12
8. a) With the help of necessary circuit diagram explain the operation Ramp type ADC.
- b) A 6-bit R-2R ladder type DAC has reference voltage of 6.5 V.

Find :

- i) resolution in % & volt
- ii) the full scale voltage
- iii) the o/p for the i/p 011100. 10 + 2 + 1 + 2
9. a) Discuss the totem pole output configuration of TTL logic family.
- b) Design a combinational circuit that accepts a BCD as i/p and generates XS3 as an o/p using ROM.
- c) Design & explain the operation of a 4-bit universal register. 5 + 5 + 5



10. a) Write down the excitation table of JK and D flip-flops and derive the excitation equation for these two flip-flops.
- b) Design a full subtractor using full adder module and NOT gates.
- c) Design a full subtractor using 4 to 1 MUX. $6 + 3 + 6$
11. Write short notes on any *three* of the following : 3×5
- a) Priority encoder
- b) Even parity generator and checker
- c) PLD
- d) Johnson counter
- e) Parallel in serial out (PISO) shift register.
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