Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH(CSE)/SEP.SUPPLE/SEM-8/CS-801D/2012

2012
VLSI DESIGN

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) The model parameter LAMDA (λ) in a MOS structure stands for
      a) Flicker noise coefficient
      b) Transit time
      c) Channel length modulation
      d) Transconductance.

   ii) Soft node leakage problems of CMOS NORA structure can be reduced using
      a) TSPICE logic
      b) Zipper CMOS logic
      c) NM logic
      d) Cascaded domino logic.

   iii) Active resistor is used for
      a) less fabrication area
      b) load resistor
      c) constant current source
      d) all of these.

iv) For depletion type NMOS
   a) the threshold voltage is +ve
   b) the threshold voltage is –ve
   c) the threshold voltage is +ve and – ve
   d) all of these.

v) The noise margin for high signal level (NM_H) is
   a) $V_{IL} - V_{OL}$ b) $V_{OH} - V_{IH}$
   c) $V_{OH} - V_{OL}$ d) None of these.

vi) The example of electrical faults is
   a) Slower transition
   b) Logical Stuck-at-0 or Stuck-at-1
   c) Bridging faults.
   d) none of these

vii) The graph that is used to represent an algorithms id known as
   a) a signal flow graph
   b) a data – flow graph
   c) a control flow graph
   d) a binary decision graph.

viii) Minimum transistor gates required to design CMOS XOR gate is
   a) 6 b) 8
   c) 12 d) 10.

ix) Among the following which one has the greatest gate integration capacity ?
   a) FPGA b) CPLD
   c) PLD d) ASIC.

x) The fastest logic family is
   a) TTL b) CMOS
   c) ECL d) IIL.

xi) FPGA is a
  a) Full Custom ASIC
  b) Semi-Custom ASIC
  c) Programmable ASIC
  d) none of these.

xii) The output of physical design is
  a) Circuit b) Layout
  c) Logical Model d) RTL Schematic.

xiii) The suitable interconnect among the following is
  a) aluminium b) Gold
  c) Copper d) Silver.

xiv) PLA and PAL are known as
  a) CPLD b) EPLD
  c) SPLD d) GPLD.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. What is an FPGA ? How is it different from CPLD ? What are the advantages of FPGA ? 1 + 2 + 2

3. Implement the following functions using PLA : $2\frac{1}{2} \times 2$
  a) $F = AB' + A'B$
  b) $F = A + (B' + C)$.

4. a) What are the different design rules ? Discuss each in brief.
  b) Give the layout of CMOS Inverter. 2 + 3

5. What is Stuck-at-fault model ? How this model is classified ? Give example of each model. 1 + 1 + 3

6. Design the following function by CMOS logic : $2 \times 2\frac{1}{2}$
  a) $F = AB + (D + C) E$
  b) $F = A + B (C + D)$.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Explain how a MOSFET can be used as switch. 3
   b) Descrbie the architecture of Xilinx FPGA. 5
   c) Give VHDL code for Full Adder circuit. 3
   d) Describe circuit operation of CMOS NAND gate. 4
8. a) Explain the fabrication procedure of n-well MOSFET with suitable diagrams. 10
   b) What is Twin-Tub process ? 5
9. a) What are the differences between enhancement and depletion type MOSFET ? 2
   b) Obtain the VTC curve for a CMOS Inverter and clearly define operating regain of NMOS and PMOS. 5 + 3
   c) Prove that for an ideal CMOS Inverter $(W/L)p = 2{\cdot}5\ (W/L)n$. 5
10. a) Define floor planning. Briefly describe Slicing and Non-Slicing floor plan with example. 2 + 5
    b) Explain Build–in–self test. 3
    c) Define scan–based test. Explain Boundary-Scan test. 2 + 3
11. Write short notes on any *three* of the following : 3 × 5
    a) FPGA
    b) Power consumption in CMOs technology
    c) Silicon wafer preparation
    d) Design rule checker (DRC).