Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B. Tech (CSE)/SEM-3/CS-303/2009-10

2009
COMPUTER ORGANIZATION

Time Allotted : 3 Hours | Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives of the following : $10 \times 1 = 10$

   i) When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero ?

   a) Magnitude b) 1's complement

   c) 2's complement d) None of these.

   ii) Maximum n bit 2's complement number is

   a) 2^n b) $2^n - 1$

   c) $2^{n-1} - 1$ d) cannot be said.

iii) For BIOS (Basic Input/Output System) and IOCS (Input/Output Control System), which one of the following is *true* ?

a) BIOS and IOCS are same

b) BIOS controls all devices and IOCS controls only certain devices

c) BIOS is not a part of Operating System and IOCS is a part of Operating System

d) BIOS is stored in ROM and IOCS is stored in RAM.

iv) Which logic gate has the highest speed ?

a) ECL b) TTL

c) RTL d) DTL.

v) Booth's algorithm for computer arithmetic is used for

a) multiplication of numbers in sign magnitude form

b) multiplication of numbers in 2's complement form

c) division of numbers in sign magnitude form

d) division of numbers in 2's complement form.

vi) How many RAM chips of size (256 K × 1 bit) are required to build 1 M byte memory ?

a) 32 b) 10

c) 8 d) 24.

vii) The conversion (FAFAFB) 16 into octal form is

a) 76767676 b) 76575372

c) 76737672 d) none of these.

viii) A decimal no. has 30 digits. Approximately, how many would the binary representation have ?

a) 30 b) 32

c) 60 d) 90.

ix) The logic circuit in ALU is

a) entirely combinational

b) entirely sequential

c) combinational cum sequential

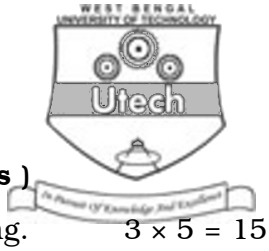
d) none of these.

x) State *True* or *False* :

Adding $0110\ 1101_2$ to $1010\ 0010_2$ in 8-bit 2's complement binary will cause an overflow

a) True

b) False.



GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) Briefly explain IEEE 754 standard format for floating point representation in single precision.

   b) Write $+7_{10}$ in IEEE 754 floating point representation in double precision. 3 + 2

3. What is interrupt ? What are the differences between vectored and non-vectored interrupts ? 1 + 4

4. a) Where does DMA mode of data transfer find its use ?

   b) What are the different types of DMA controllers and how do they differ in their functioning ? 2 + 3

5. Explain the difference between full associative and direct mapped cache mapping approaches.

6. Compare and contrast RISC and CISC architecture.

GROUP – C
(Long Answer Type Questions)
Answer any *three* of the following. 3 × 15 = 45

7. a) Give the Booth's algorithm for multiplication of signed 2's complement numbers in flowchart and explain.

   b) Multiply – 5 and – 3 using Booth's algorithm.

   c) What is von Neumann architecture ? What is von Neumann bottleneck ?

   d) What is the necessity of Guard bits ? 5 + 4 + 4 + 2

8. a) Define "latency time" of a memory.

   b) Can a ROM be also a RAM ? Justify your answer.

   c) Explain the memory hierarchy pyramid, also explain the relationship of cost, speed and capacity.

   d) A hierarchical cache-main memory subsystem has the following specification :

      i) Cache access item of 160 ns

      ii) Main memory access time 960 n

      iii) Hit ratio of cache memory is 0·9

      Calculate the following :

      a) Average access time of the memory system

      b) Efficiency of the memory system.

      1 + 3 + 5 + 3 + 3

9. a) What is locality of reference ? Explain the concept of cache memory with it.

   b) Briefly explain write-through and write-back policies.

   c) State $L1$ and $L2$ cache policies with suitable figure.

   d) Discuss the role of OS.

   e) How many 256 × 4 RAM chips are needed to provide a memory capacity of 2048 bytes ? Show also the corresponding interconnection diagram. 2 + 2 + 2 + 2 + 7

10. a) A 32-bit floating-point binary number has a bit plus a sign for the exponent. The mantissa is assumed to be a normalized fraction. Negative numbers in the mantissa and exponent are in signed-magnitude representation. What are the longest and smallest positive qualities that can be resented excluding zero ? Explain with example.

    b) Explain with diagrams, Serial & Parallel Adders.

    c) ADD $A + B$, where $A = 63{\cdot}11236589 \times 10^{15}$ & $B = 0{\cdot}002365991 \times 10^{-29}$. (4 + 4 + 4) + 3

11. Write short notes on any *three* of the following : 3 × 5

a) Pipeline hazards

b) Adder-subtractor circuit

c) Data flow architecture

d) Bus organization using tri-state buffer

e) Virtual address to real address mapping.