



Name :

Roll No. :

Invigilator's Signature :

CS/B.Tech (ECE)/SEM-5/EI(EC)-502/2010-11

2010-11

MICROPROCESSOR & MICROCONTROLLER

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) The control signal used to distinguish between an I/O operation and memory operation is

- | | |
|--------|---------|
| a) ALE | b) IO/M |
| c) SID | d) SOD. |

ii) The control signal, HOLD is sent by 8085 in order to

- a) inform I/O device that the address is being sent over the AD line
- b) achieve separation of address from data
- c) synchronize with low speed peripheral
- d) to activate DMA.



- vii) If a DMA request is sent to the microprocessor with a Hi signal to the HOLD pin, the microprocessor acknowledge the request
- a) after completing the present cycle
 - b) immediately after receiving the signal
 - c) after completing the program
 - d) none of these.
- viii) STA 9000H is a
- a) data transfer instruction
 - b) logical instruction
 - c) I/O and machine control instruction
 - d) none of these.
- ix) The segment and offset address of the instruction to be executed by 8086 microprocessor are pointed by
- a) CS and SI
 - b) DS and IP
 - c) CS and SP
 - d) CS and IP
- x) The instruction register holds
- a) flag conditions
 - b) instructions address
 - c) opcodes
 - d) none of these.

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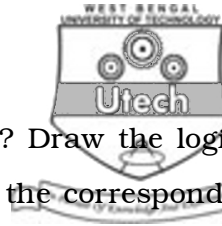
5. a) Define addressing mode in 8085 microprocessor.
- b) How many addressing modes are available in 8085 microprocessor ? Explain with two examples each. 1 + 4
6. a) What is pipelined architecture ? How is it implemented in 8086 microprocessor ?
- b) How many address lines are used for I/O mapped I/O technique in the context of interfacing with 8086 ? 1 + 2 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Draw the timing waveform of Mode 1 input control signals of 8255.
- b) Write an Assembly Language Programming in 8085 to interface a 8255 chip with Port B address DDh to scan Port A and send the data to Port B. Draw the logical circuit diagram. 6 + 4 + 5
8. a) What is software interrupt in 8085 microprocessor ?
- b) Explain the instruction SIM & RIM in 8085 microprocessor.



- c) What is RST instruction of 8085 μ P ? Draw the logical circuit for RST 6 interrupt and write the corresponding Assembly Language Programming. $2 + 5 + 1 + 3 + 4$
9. a) Explain the function of different types of control and status signals of 8085 μ P.
- b) Explain the need to demultiplex the bus $AD_7 - AD_0$ of 8085 μ P. What is the need of ALE signal in this purpose ?
- c) What is fold back memory ? Give an example.
- d) if the 8085 μ P clock frequency is 2 MHz then calculate the time required to execute the instruction STA 2000h. $4 + 3 + 4 + 4$
10. a) What is interrupt vector table ? Explain its structure. Explain the interrupt response sequence of 8086.
- b) What is the interrupt vector address of the following interrupt in the 8086 IVT ?
- i) INT0
- ii) NMI
- iii) INT 21H.
- c) How will you interface a stepper motor with 8086 ? Draw the interfacing circuit and flow-chart. $(1 + 2 + 3) + 3 + 6$



11. Write short notes on any *three* of the following : 3 × 5

- a) Addressing modes of 8051 microcontroller
- b) 8259 Interrupt controller
- c) Min/Max mode operations of 8086 microprocessor
- d) Architecture of 8051 microcontroller
- e) DMA data transfer scheme.

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