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Paper Code : EC(EE)-302

DIGITAL ELECTRONIC CIRCUIT

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) Gray code of 1011 (binary) = [| C |]
   a) 0101 b) 1101
   c) 1110 d) none of these.

ii) An example of reflected code is
   a) BCD b) ASCII
   c) GRAY d) Hamming code.

iii) The minimum number of NAND gates required to design one X-OR gate is
   a) 3 b) 4
   c) 5 d) 6.

iv) If $(212)_x = (23)_{10}$, where x is base (+ ve integer) then the value of x is
   a) 2 b) 3
   c) 4 d) 5.

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v) Full form of FPGA is
   a) Full Programmable Gated Array
   b) Field Programmable Gated Array
   c) Full Peripheral Gated Array
   d) Field Peripheral Gated Array.

vi) The resolution of 8-bit A/d converter is
   a) 0·62 % b) 0·38 %
   c) 0·39 % d) 1·25 %.

vii) One bit even parity detector code fails to detect
   a) any even number of error
   b) any odd number of error
   c) both (a) and (b)
   d) none of these.

viii) What is the word size of 16×8 ROM ?
   a) 16 b) 8
   c) 128 d) none of these.

ix) $(A + B' + A'B)\, C =$
   a) 1 b) 0
   c) C d) C'

x) F/F that makes output equals to input after clock is
   a) J-K F/F b) D F/F
   c) T F/F d) none of these.

xi) 8421 is a
   a) weighted code b) non-weighted code
   c) complementary code d) none of these.

xii) The characteristic equation of T flip-flop is given by
   a) $Q^+ = \bar{T}Q + T\bar{Q}$ b) $Q^+ = \bar{T}\,\bar{Q} + TQ$
   c) $Q^+ = T\bar{Q}$ d) none of these.

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GROUP – B
(Short Answer Type Questions)

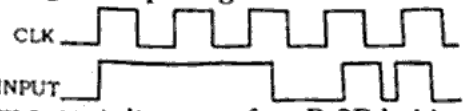
Answer any *three* of the following. 3 × 5 = 15

2. Using the K-map method, simplify the following Boolean function and obtain minimal POS expression :
$Y = \sum_m (0,2,6,7) + \sum_d (3,8,10,11,15)$
3. Implement a full adder circuit by using two 2 : 1 multiplexers.
4. Design a full adder using minimum number of NAND gates.
5. Realize a *D* flip-flop by using a *T* flip-flop and other required logic gates.
6. Construct a full substructure by using two half substructures and an OR gate.

GROUP – C
(Long Answer Type Questions)

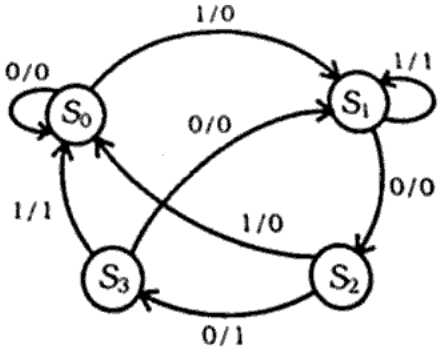
Answer any *three* of the following. 3 × 15 = 45

7. a) Draw the timing diagram of a *D* flip-flop & *D*-latch for the given input signals. 7 + 8



b) Draw a neat diagram of an R-2R ladder type DAC.

8. a) Design a sequential circuit that implements the following state diagram. Using all *D*-type flip-flops for the design.



b) Draw and explain the *BCD* adder using 7483. 10 + 5

9. a) Explain the operation of PROM, and EPROM.

b) Design a 5 Mod synchronous binary counter using *J-K* flip-flop and necessary logic gates. 6 + 9

10. a) What are the differences between the Decoder and Demultiplexer ?

b) Form a multiplexer tree to give 8 : 1 MUX from two 4 : 1 MUX and 2 : 1 MUX.

c) Implement a full-adder circuit using 3 to 8 decoders with all active high outputs and other necessary logic gates. 2 + 6 + 7

11. Write short notes on any *three* of the following : 3 × 5

a) Shift registers

b) Johnson counter

c) Successive Approximation Type A/D Converter

d) Noise margin

e) Master-slave *JK* flip-flop.