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Paper Code : EC-702

PUID : 07076 (To be mentioned in the main answer script)

MICROELECTRONICS & VLSI DESIGN

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) Frequency compensation for an op-amp can be achieved by

   a) increasing gain

   b) minimizing overall phase shift

   c) adding a zero

   d) none of these.

ii) Slant in (I_D-V_{Ds}) occurs due to

a) body effect

b) velocity saturation

c) channel length modulation

d) mobility degradation.

iii) Which is not a part of FPGA ?

a) Configurable logic block

b) IOB

c) Microprocessor

d) Routing Channels.

iv) Which are the simple PLDs ?

a) CPLD

b) FPGA

c) CBIC

d) PLA.

v) How many CMOS transistors are needed to implement XOR gates ?

a) 7

b) 10

c) 8

d) 9.

vi) What is full form of VHDL ?

a) Very high speed integrated circuit Hardware description language (HDL)

b) Vast HDL

c) Very simple HDL

d) Very high HDL.

vii) What is ASIC ?

a) Application simplified IC

b) Applied IC

c) Application specific IC

d) Authentic IC.

viii) VLSI design flow is a

a) cyclic process only

b) parallel process

c) sequential & cyclic process

d) none of these.

ix) VHDL is a

a) multithreaded program

b) language like C

c) single user program

d) multiuser program.

x) The output of physical design is

a) circuit b) layout

c) logical model d) RTL schematic.

xi) Typical manufacturing defects in IC fabrication are

a) layer to layer shorts

b) discontinuous wires

c) missing or damaged vias

d) any one of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Draw layout of MOSFET.
3. Design NOR with CMOS logic.
4. Dfinc op-amp ? Explain the characteristics of op-amp.
5. Implement thc following Boolean functions with TG logic :
   a) Y = ab' + bc + c'a
   b) F = ab' + a'bc
6. Proof that $(W/L)_P = 2.5\ (W/L)_N$.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. What are the different types of ASIC ? Explain briefly all of them. 6 + 9
8. Explain the VTC curve of CMOS logic. Calculate the Vth of CMOS inverter. 7 + 8
9. What do you mean by twin tub ? Explain the p-well CMOS fabrication process with necessary diagram. 4 + 11
10. Define Y chart. Explain it. What do you mean by regularity, locality, modularity. 3 + 3 + 3 + 3 + 3
11. Write short notes on any *three* of the following : 3 × 5
    a) CMRR
    b) Domino logic
    c) 6 transistor XOR design.
    d) Edge triggered D flipflop.