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Name : .....

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Invigilator's Signature : .....

CS/B.Tech/ECE/SEM-8/EC-803B/2013

2013

EMBEDDED SYSTEM

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

$10 \times 1 = 10$

i) I^2C bus stands for

a) Intra IC connect bus

b) Interface IC connect bus

c) Inter IC connect bus

d) none of these.

ii) DRAM is widely used because of

a) refreshing operation is not needed

b) low cost and high density

c) low power consumption

d) high speed.

iii) Who determines which task / process is to be executed at a given point of time ?

a) Process manager

b) Context Manager

c) Scheduler

d) (b) or (c).

iv) Architecture used in DSP processor is

a) Von Newman

b) Harvard architecture

c) SIMD

d) All of these.

v) Which is special variation is used to take note of certain actions to prevent any task or process from processing ?

a) Semaphore

b) Mutex

c) Buffer

d) Counting Semaphore.

vi) The main function of RTOS is

a) Real time task scheduling and interrupt latency control

b) Process Management

c) Device Management

d) Memory Management.

vii) Memory access in RISC architecture is limited to instructions

a) CALL and RET

b) PUSH and POP

c) STA and LDA

d) MOV and JMP.

viii) Which chip has a large number of arrays with each element having fusible links ?

a) GPP

b) ASSP

c) FPGA

d) Register.

ix) Pipelining strategy is called implement

a) instruction execution

b) instruction prefetch

c) instruction decoding

d) instruction manipulation.

x) Compared to FPGA, gate array design style has

a) Less chip utilization factor

b) More chip speed

c) More flexibility

d) none of these.

xi) MAC unit is present in which type of processor ?

a) ARM processor

b) DSP processor

c) ASIP processor

d) None of these.

xii) SOC means

a) a single chip that would realize the entire system

b) a system is distributed in different chips

c) a partially filled system within a chip

d) various program modules included within a chip.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Define an Embedded system. Write down the classification of embedded system. 1 + 4

3. What do you mean by fixed point & floating point arithmetic in connection with embedded system computation ? Discuss with example.

4. Explain about JTAG.

5. Design a 4 bit ALU and a 4 bit counter using any embedded software language.

6. Compare clock driven and event driven schedulers.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Compare SRAM and DRAM.

   b) What is the difference between standard write & late write is SRAM ?

   c) What is meant by Dynamic power loss of SRAM ?

   d) Name and explain different reading mechanisms of SRAM from the memory with timing diagram.

   3 + 2 + 2 + 8

8. What do you mean by pipelining ? How is this concept implemented in ARM core processor ? Describe different modes of ARM core. 3 + 4 + 8

9. a) What is DMAC ? Describe DMAC with the suitable block diagram.

   b) What do you mean by Black Box and White Box testing ? Explain it. 7 + 8

10. a) What is the difference between general purpose OS and RTOS ? Differentiate real-time tasks on the basis of time criticality.

    b) What do you mean by task scheduling ? Explain dynamic priority scheduling algorithm to schedule real time task with a suitable example.

    c) Mention advantages and disadvantages of fixed priority scheduling algorithm used to schedule real time task and also write down the necessary and sufficient conditions which have to be satisfied by the real time task. 6 + 4 + 5

11. Write short notes on any *three* of the following : 3 × 5

a) Adaptive Echo Cancellation

b) ARM Cache Organization

c) Sequential *vs* parallel Pipelining

d) Embedded Processor

e) Programmable devices.