

Name :

Roll No. :

Invigilator's Signature :

CS / B.TECH (ECE) / SEM-4 / EC-402 / 2011

2011

DIGITAL ELECTRONIC CIRCUITS

Time Allotted : 3 Hours

Ful Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

$$10 \times 1 = 10$$

- i) The Excess-3 representation of decimal 59 is

- a) 01100010 b) 00111110
c) 10001100 d) none of these.

- ii) The number of full address required to construct an
 m -bit parallel adder is

- a) $m/2$ b) $m - 2$
c) m d) $m + 1$.

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- iii) The 2's complement representation of $(-19)_{10}$ is
- a) 101100 b) 101110
- c) 101101 d) none of these.
- iv) The maxterm corresponding to decimal 9 is
- a) $A B' C' D$ b) $A + B' + C' + D$
- c) $A' + B + C + D'$ d) $A' B C D'$.
- v) The number of comparators required in a 8-bit flash type A/D converter is
- a) 256 b) 255
- c) 64 d) 8.
- vi) A 3-bit synchronous counter uses flip-flops with propagation delay of 20 ns each. The maximum possible time required for change of state will be
- a) 60 ns b) 40 ns
- c) 20 ns d) none of these.

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- xi) A two-input EX-OR gate can be used as an inverter when one of its inputs is kept at logic
- a) 0 b) 1
- c) either 0 or 1 d) none of these.
- xii) If the resolution of a D/A converter is approximately 0.4% of its full scale range, it is
- a) an 8-bit converter b) a 10 bit converter
- c) a 12-bit converter d) a 16-bit converter.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

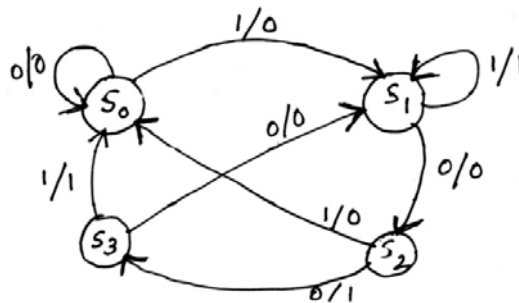
2. Design a Full Adder circuit using a decoder and other necessary logic gates. Assume that the decoder has all active low outputs. 5
3. Design a S-R flip-flop with the help of J-K flip-flop. 5
4. Implement a 16:1 MUX by using 4 : 1 MUX only. 5

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5. a) Distinguish between synchronous and Asynchronous counters. 2
- b) Calculate the frequency of 4-bit ripple counter, if the period of waveform at the last flip-flop is 64 microsecond. 3
6. Design a Binary to Gray code converter using PROM. 5

GROUP – C**(Long Answer Type Questions)**Answer any *three* of the following. $3 \times 15 = 45$

7. a) Design a sequential circuit that implements the following state diagram. (Use D flip-flop) 10



- b) Implement the following Boolean function using 8 : 1 MUX :

$$F(A, B, C, D) = \sum m(0, 7, 8, 9, 10, 11, 15).$$
 5

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8. a) Design a MOD-6 synchronous up-counter using J-K flip-flops. 7

- b) Implement the following function using $3 \times 4 \times 2$ PLA :

$$F_1(A, B, C) = \sum m(3, 5, 6, 7) \quad F_2(A, B, C) = \sum (0, 2, 4, 7). \quad 8$$

9. a) Simplify the following function in SOP form using Quine MC- Cluskey method :

$$F(A, B, C, D) = \sum m(0, 1, 4, 7, 9, 11, 13, 15) + \sum d(3, 5). \quad 9$$

- b) Describe the operation of a two-input NAND gate constructed with CMOS. 6

10. a) Design a combinational circuit for Excess-3 code to BCD conversion using minimum number of logic gates.

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- b) Describe the principle of operation of successive Approximation type A/D converter. 6

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11. Write short notes on any *three* of the following : 3×5

- a) 4-bit magnitude comparator
- b) Bi-directional shift register
- c) PAL
- d) Master-slave J-K flip-flop
- e) EEPROM.

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