Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS / B.TECH (EE-NEW) / SEM-4 / EC (EE)-402/ 2011

2011

DIGITAL ELECTRONICS AND INTEGRATED CIRCUITS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

$10 \times 1 = 10$

i) The carry look ahead adder is frequently used for addition because, it

a) is faster b) has more accuracy

c) uses fewer gates d) costs less.

ii) Which gates are used as an array of a programmes in ROM ?

a) AND gates b) OR gates

c) Both (a) and (b) d) None of these.

iii) $A + A'B + A'B'C + A'B'C'D + ... =$

a) $A + B + C + ...$ b) $A' + B' + C' + ...$

c) 1 d) 0.

iv) The decimal number –15 is represented in 8-bit signed 2's complement notation as

a) 11010001 b) 11100111

c) 11110001 d) 10001111.

v) Which of the following IC logic families has extremely low power dissipation ?

a) TTL

b) Schottky TTL

c) Low power Schottky TTL

d) CMOS.

vi) Two D flip-flops are connected as a synchronous counter that goes through the following Q_BQ_A sequence 00, 11, 01, 10, 00, ... The connections to the inputs D_A and D_B are

a) $D_A = Q_B, D_B = Q_A$

b) $D_A = Q_A', D_B = Q_B'$

c) $D_A = Q_AQ_B' + Q_A'Q_B,\ D_B = Q_A$

d) $D_A = Q_AQ_B + Q_A'Q_B',\ D_B = Q_B'$.

vii) The output of a logic gate is 1 when all its input are at logic zero. The gate is either

a) a NAND or an EX-OR b) an OR or an EX-OR

c) an AND or an EX-OR d) a NOR or an EX-NOR.

viii) A minterm is

a) the minimum term in a Boolean function

b) a prime implicant

c) always smaller than a maxterm

d) a square on a Karnaugh map.

ix) $[(xy' + xyz)' + x(y + xy')]' =$

a) 1 b) 0

c) x d) x'.

x) Party checker is used to detect

a) 1-bit error b) 2-bit error

c) 3-bit error d) 4-bit error.

xi) Which one is the fastest logic in logic families ?

a) RTL b) TTL

c) ECL d) none of these.

xii) If $(212)_x = (23)_{10}$ where x is base (+ ve integer) then the value of x is

a) 2 b) 3

c) 4 d) 5.

xiii) A flip-flop is called a latch when it is

a) edge trigger b) level trigger

c) both (a) and (b) d) without any trigger.

xiv) To add two *m*-bit numbers, the number of required half added is

a) $2m - 1$ b) $2m$

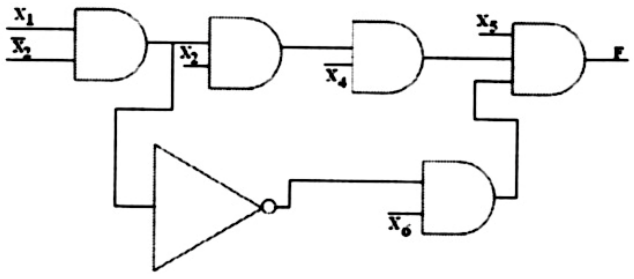
c) 2^m d) $2m + 1$.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Convert the following circuit into a multi-level circuit using all NAND gates. Assume that the three & complement of all variables are available to the circuit.



3. Design a full-subtractor using only NOR gates.

4. Explain the circuit operation of a Master-Slave JK flip-flop using all NAND gates. Write down the corresponding truth table. 3 + 2

5. Design a 4 to 16 decoder by using two 3 to 8 decoders. Write down the corresponding truth table. 4 + 1

6. Prove that the NAND gate is called a universal gate. Implement an EX-OR (2-input) logic using NAND gates. 4 + 1

7. Design a circuit using logic gates which will generate the odd parity of 3-bit binary number. What is the function of a parity checker ? 3 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

8. a) What do you mean by Prime implicant ? Simplify the following Boolean expression using K-map :

$$F(A, B, C, D) = \sum m(0, 2, 3, 6, 8, 11, 12, 14) + d(1, 4, 9, 10)$$

b) Design a full adder using two half adders and necessary gate.

c) Draw a network using only NAND gate to generate the function $Y = (\overline{A} + BC)$. (2 + 5) + 4 + 4

9. a) What are the advantages and disadvantages of totem pole ?

   b) What are the output voltages caused by logic 1 in each bit position in an 8-bit ladder if the input level for 0 level is 0 volt and for level 1 is 10 volt ?

   c) Compare the maximum conversion period of an 8-bit Digital ramp ADC and 8-bit successive approximation ADC, if both utilize 1 MHz clock frequency.

   d) With proper circuit diagram, explain the operation of NMOS NAND gate. 3 + 3 + 4 + 5

10. a) Perform the conversion of D flip-flop to JK flip-flop.

   b) What is presettable counter ? Design a MOD-5 counter that counts its natural count sequence from 000 to 100.

   c) Distinguish between a ripple counter and a synchronous counter. 5 + 8 + 2

11. a) What are the differences between the Decoder and Demultiplexer ?

   b) Form a multiplexer tree to give 4 × 1 MUX from two 2 × I MUX.

c) Show how a 16 input MUX is used to generate the function $F = (A, B, C, D) = \overline{A}\,\overline{B}\,\overline{C}D + BCD + A\,\overline{B}\,\overline{C} + AB\overline{C}D$.

5 + 5 + 5

12. a) What are RAM and ROM ? What is the basic difference between EPROM and EEROM ?

b) What is the major difference between the two classes of finite state machines and proper state diagram ?

c) What is Schmitt Trigger ? (2 + 3) + (4 + 4) + 2

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