(e) A computer has 1 KB 4-way set associative cache and 1 MB main memory. If the block size is 64 B, then in which cache set are the words $(ABCDE)_{16}$ and $(EDCBA)_{16}$ mapped?

[3+3+3+2+4]

11. Write short notes on any three of the following:

[5x3]

i) Amdahl's law and its significance.

ii) Cache coherence problem and its solutions.

iii) Pipeline hazards.

iv) Memory interleaving.

v) Array processor & Vector processor.

2014

Computer Architecture

Time Alloted : 3 Hours *Full Marks : 70*

The figure in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP - A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any ten of the following:

10x1=10

i) A pipeline stage

a) is sequential circuit

b) is combinational circuit

c) consists of both sequential and combinational circuits

d) none of these.

ii) Dynamic pipeline allows

a) Multiples function to evaluate

b) To perform fixed function

c) Only streamline connection

d) none of these.

iii) What will be the speed up for a 4 segment linear pipeline when the number of instruction n=64?

a) 4.5

b) 3.82

c) 8.16

d) 2.95

iv) For 2 Instructions I and J, WAR hazard occurs if

a) $R(I) \bigcap D(J) \neq \varphi$

b) $R(I) \bigcap R(J) \neq \varphi$

c) $D(I) \bigcap R(J) \neq \varphi$

d) none of these.

v) The division of stages of a pipeline into sub-stages is the basis for -

a) pipelining

b) super-pipelining

c) superscalar

d) VLIW processor

vi) The prefetching is a solution for

a) Data hazard

b) Structural hazard

c) Control hazard

d) none of these.

vii) Stride in Vector processor is used to

a) differentiate different data types

b) registers

c) differentiate different data

d) none of these.

viii) A computer with cache access time of 100ns,a main memory access time of 1000 ns, and a hit ratio of 0.9 produces an average access time of

a) 250 ns

b) 200 ns

c) 190 ns

d) none of these .

ix) Array processor are put under which of these categories?

a) SISD

b) SIMD

c) MISD

d) MIMD

x) Effectivetive access time (T_{eff}) of memory is given by

a) $T_{eff} = 1/\sum_{i=1}^{n} f_i t_i$

b) $T_{eff} = \sum_{i=1}^{n} f_i t_i$

c) $T_{eff} = \sum_{i=1}^{n} f_i / t_i$

d) none of these.

xi) Basic difference between Vector processor and Array processor is

a) pipelining

b) interconnection network

c) register

d) none of these

GROUP - B
(Short Answer Type Questions)

Answer any *three* of the following. 3x5=15

2. Compare CISC and RISC computer architectures. What are multiprocessor, multi-computer and multi-core systems? [2+3]

3. What is the drawback of direct mapped cache? How is it resolved in set associative cache? [2+3]

4. Compare superscalar, super-pipeline and VLIW technique. [5]

5. Discuss different types of vector instructions. [5]

6. What is branch hazard? Briefly discuss two methods to handle branch hazard. [1 +4]

GROUP - C
(Long Answer Type Questions)

Answer any *three* of the following. 3x15=45

7. (a) What is arithmetic and instruction pipeline?

(b) Consider the following reservation table

	1	2	3	4
S1	X		X	
S2		X		
S3			X	
S4		X		X

List the set of forbidden latencies and collision vector. Draw the state transition diagram. List all simple cycles from state diagram. Identify the greedy cycles among simple cycles. Find out minimum average latency (MAL). Find out maximum throughput of this pipeline if the clock rate is 25 MHz.

c) What are bounds on MAL?

[2+(2+3+2+2+1+1)+2]

8. (a) What is data flow computer? Differentiate a data flow computer from a control flow computer.

(b) What are the problems with data flow computer implementation?

(c) With simple diagram explain data flow architecture.

(a) Draw data flow graphs to represent the following computations:

P = A + B

Q = P / B

R = A * P

S = R - Q

T = R * P

U = S / T

[(2+2)+3+4+4]

a) What is the instruction level parallelism?

b) What do you mean by multiple issue processors?

c) Briefly describe the VLIW processor architecture. What are the limitations of VLIW?

d) What is the difference and similarities between multi-computer and multiprocessor?

[2+2+5+2+4]

a) Briefly discuss MIMD architecture.

b) What is the significance of interconnection network in multiprocessor architecture?

c) What are the different types of multi-stage interconnection networks?

d) What are the differences between loosely coupled and tightly coupled architecture?