



Name :

Roll No. :

Invigilator's Signature :

CS/B. TECH (ECE-NEW)/SEM-7/EC-702/2010-11

2010-11

EDA FOR VLSI DESIGN

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct answer for any *ten* of the following :

$10 \times 1 = 10$

- i) Synthesis translates from
 - a) Physical description to behavioral description
 - b) Structural to physical description
 - c) Behavioral description to structural description
 - d) Structural description to behavioral description



- ii) Channelless Gate array is a sub-type of
 - a) FPGA
 - b) PLD.
 - c) ASIC
 - d) Microprocessor.
- iii) BDD is useful for
 - a) High level synthesis
 - b) Logic level synthesis
 - c) Testing
 - d) Timing analysis.
- iv) FPGA is a
 - a) full-custom ASIC
 - b) semi-custom ASIC
 - c) programmable ASIC
 - d) structured ASIC.
- v) VHDL codes are inherently
 - a) Sequential
 - b) Concurrent.
 - c) Both (a) and (b)
 - d) Cyclic.
- vi) Which one is not a task of High Level Synthesis ?
 - a) Partitioning
 - b) Scheduling
 - c) Allocation
 - d) Binding.



vii) Which graph representation is not used in Floor planning ?

- a) Polar graph
- b) Adjacency
- c) Channel position graph
- d) Block placement graph

viii) Scan design technique is used for testing which provides

- a) Controllability
- b) Observe ability
- c) Scanning
- d) Both (a) & (b).

ix) In VHDL, Generic command is

- a) Local declaration
- b) Global declaration
- c) Both locally and globally
- d) None of these.



- x) Which technology is not used in FPGA ?
- a) Static RAM technology
 - b) Dynamic RAM technology
 - c) Anti-fuse technology
 - d) EEROM technology.
- xi) High level synthesis has design constraints like
- a) area
 - b) timing
 - c) power
 - d) all of these.
- xii) CLBs are used in
- a) gate array design style
 - b) standard cell based design
 - c) Field programmable gate array layout
 - d) full custom design.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following.

$$3 \times 5 = 15$$

2. What do you mean by High Level Synthesis ? What are the general steps in high level synthesis ?

$$2 + 3$$



3. Give a brief description of Binary Decision Diagram in the context of logic level synthesis ? 5
4. Explain with example the differences in between signal and variable in VHDL. 5
5. Find the minimal complete set of tests for stuck-at faults in the circuit as shown in the Fig. 5

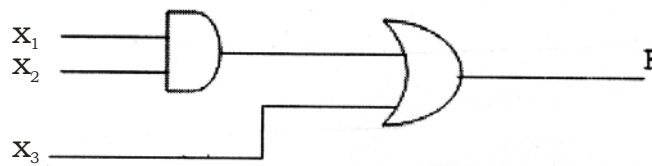


Fig.

6. Distinguish between Dynamic and Static timing analysis. 5

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following.

$$3 \times 15 = 45$$

7. a) Describe the *p*-well fabrication process with necessary diagram.
- b) What is the minimum width of polysilicon ?



- c) What are μ -based design and λ -based design in VLSI system ?
- d) Draw the 3-input CMOS NAND gate using layout technique. $8 + 1 + 3 + 3$
8. a) Why has verification an important role in High Level Synthesis ?
- b) Define "stuck-at-0", "stuck-at-one" and bridging faults with example.
- c) Define observability and controllability. $5 + 7 + 3$
9. a) Implement a 4 : 1 multiplexer in VHDL code using mixed style of modelling.
- b) Define the term Synthesis and discuss the different level of Synthesis.
- c) What is data path ? $5 + (3 + 5) + 2$
10. a) What is ASIC ?
- b) Discuss ASIC design options.
- c) What are the advantages and disadvantages of FPGA compared to ASIC ?
- d) Give a brief description of design issues and tools.
- e) What is the full form of CDFG ? $2 + 4 + 3 + 5 + 1$



11. Write short notes on any *three* of the following : 3×5

- a) Reduced Ordered Binary Decision Diagrams.
 - b) Routing
 - c) Classification of an ASIC
 - d) Formal Verification
 - e) VLSI design flow.
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