**ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE - 2009**

# DIGITAL ELECTRONIC CIRCUITS

## SEMESTER - 4

Time : 3 Hours ] [ Full Marks : 70

### GROUP - A

### ( Multiple Choice Type Questions )

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) Gray code of 1011 ( binary ) =

a) 0101 b) 1101

c) 1110 d) none of these. ☐

ii) An example of reflected code is

a) BCD b) ASCII

c) GRAY d) Hamming code. ☐

iii) If $(212)_x = (23)_{10}$ where $x$ is base ( + *ve* integer ) then the value of $x$ is

a) 2 b) 3

c) 4 d) 5. ☐

iv) Excess-3 code 3d representation of $(19)_{10}$ is

a) 10011 b) 00011001

c) 01001100 d) 11000100. ☐

v) The decimal equivalent of the binary number $(101111.1101)_2$ is

a) $(46{\cdot}8125)_{10}$ b) $(47{\cdot}8125)_{10}$

c) $(47{\cdot}8155)_{10}$ d) $(47{\cdot}8145)_{10}$. ☐

vi) A 10 MHz signal is applied to a MOD 5 counter followed by a MOD 8 counter. The output frequency will be

a) 10 kHz b) 2·5 kHz

c) 5 kHz d) 25 kHz. ☐

vii) A 4-stage ripple counter counts up to

a) 12 b) 15

c) 11 d) 4. ☐

viii) Which family has the better noise margin ?

a) ECL b) MOS

c) DTL d) TTL. ☐

ix) A 4-variable logic expression can be realized by using only one

a) 4-input NOR gate b) 4 : 1 demultiplexer

c) 16 : 1 multiplexer d) none of these. ☐

x) D flip-flop can be used as a

a) divider circuit b) delay switch

c) differentiator d) none of these. ☐

xi) Master-slave configuration is used in flip-flops to

a) increase its clocking rate

b) reduce power dissipation

c) eliminate race around condition

d) improve its reliability. ☐

xii) The output frequency of a decade counter clocked from a 50 kHz signal is

a) 50 kHz b) 500 kHz

c) 5 kHz d) 25 kHz. ☐

xiii) The number of D flip-flops required to design a mod-10 Ring counter is

a) 5 b) 10

c) 9 d) 8. ☐

xiv) The power consumption of the dynamic RAM is

a) equal to that of static RAM b) more than that of static RAM

c) less than that of static RAM d) almost zero. ☐

xv) The hexadecimal equivalent number of $( 7324{\cdot}456 )_8$ is

a) ED 4·87 b) ED 4·47

c) ED 4·57 d) ED 4·97. ☐

## GROUP – B

### ( Short Answer Type Questions )

Answer any *three* of the following questions. $3 \times 5 = 15$

2. Design a logic diagram, using logic gates, for addition / subtraction circuit, using a control variable $P$ such that this operates as full adder when $P = 0$, and full subtractor for $P = 1$.

3. Design a J-K F/F using a D F/F, a 2 : 1 MUX and one inverter.

4. Design a 2-input NAND gate using MOS inverter.

5. Implement the following function using 4 : 1 MUX only :

$$F = \Sigma m ( 0, 2, 3, 6, 8, 9, 12, 14 )$$

6. Implement the full-adder circuit using a 3 to 8 decoder with all active low output and additional logic gates, if required.

## GROUP – C

### ( Long Answer Type Questions )

Answer any *three* of the following questions. 3 × 15 = 45

7. a) Draw and explain the circuit of BCD adder using commercially available adder IC 748·3 and other necessary logic gates. 7

b) Simplify the following using Quine McClusky method :

$F(W, X, Y, Z) = \Sigma(0, 1, 2, 5, 8, 14) + \Sigma d(4, 10, 13)$. 8

8. a) What is CLA adder ? Define the terms 'carry propagate' and 'carry generate'. The propagation delay of EX-OR gate is 20ns and that of OR and AND gate is 10ns. Find the propagation delay of a CLA adder. 2 + 3 + 2

b) "Excess-3 code is self-complementing." Explain the statement and write its application. 4

c) Implement the following function using a 3 × 4 × 2 PLA :

$F_1(A, B, C) = \Sigma(3, 5, 6, 7)$

$F_2(A, B, C) = \Sigma(0, 2, 4, 7)$. 4

9. a) With the help of necessary circuit diagram, explain the operation of dual slope ADC. 9

b) A 4-bit binary ladder D/A converter with R = 10 kΩ uses a reference of 5 V. Find the following :

i) Ideal scale factor in V/step

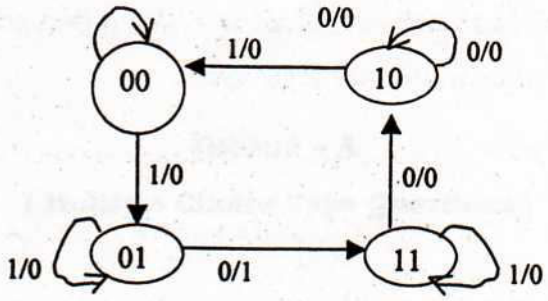
ii) Analog output corresponding to the binary input 0110

iii) Resolution in %

iv) Full scale output

v) Maximum deviation in volts from the best straight line in order to meet standard linearity. 6

10. a) Design a sequential circuit that implement the following state diagram. Use all D-type F/F for the design. 9




b) Draw and explain the 4 bit bi-directional Shift Register using mode control ( *M* ), when *M* is logic zero then left shift an right shift for *M* is logic one. 6

11. Write short notes on any *three* of the following : 3 × 5

a) D.C. noise margin and A.C. noise margin

b) Hold time and set-up time related to FF

c) Parity generator and checker

d) Tri-state gates in TTL family

e) EPROM.

END