Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech/(ECE-New)/SEM-7/EC-702/2013-14

2013

MICROELECTRONICS & VLSI DESIGN

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

Choose the correct alternatives for any *ten* of the following :

$10 \times 1 = 10$

i) Noise margin for low voltage is defined as

a) $NM_L = V_{IL} - V_{OL}$ b) $NM_L = V_{IL} - V_{IH}$

c) $NM_L = V_{OH} - V_{OL}$ d) $NM_L = V_{IH} - V_{IL}$.

ii) In the VTC curve of an inverter, critical voltages are obtained where the shape of the curve (dV_{out}/dV_{in}) is

a) 1 b) –1

c) 0 d) none of these.

iii) Slant in $(I_D - V_{DS})$ occurs due to

a) body effect

b) velocity saturation

c) channel length modulation

d) mobility degradation.

iv) The unit of $\mu_n C_{OX}$ is

a) A/V^2 b) V^{-1}

c) ohm d) $(\text{ohm})^{-1}$.

v) The model parameter LAMDA in MOS structure stands for

a) flicker noise

b) transit time

c) channel length modulation

d) transconductance.

vi) For an *n*-channel MOSFET $I_{D(SAT)}$ = 0·2 mA, V_{DS} = 5V and V_{th} = 0·6 V, the Gate voltage is

a) 4·8 V b) 5·6 V

c) 4·4 V d) 5 V.

vii) The equivalent (W/L) of two *n*MOS transistors with (W_1/L) and (W_2/L) connected in parallel is

a) $(W_1/L)+(W_2/L)$ b) $(W_1/L)\times(W_2/L)$

c) $(W_1/L)/(W_2/L)$ d) none of these.

viii) How many transistors are required to design function $F=(A.B+C.D)$?

a) 4 b) 6

c) 8 d) 10.

ix) The main advantage of precharge-evaluate dynamic logic is

a) lesser number of transistor required

b) high speed

c) low power consumption

d) all of these.

x) Which design is more efficient ?

a) Pull-up & pull-down design

b) TG design

c) Pre-charge & Evaluate logic.

xi) Dynamic logic requires periodic clock signals in order to

a) improve performance

b) synchronization

c) increasing

d) charge refreshing.

xii) The threshold voltage of an enhancement transistor is

a) greater than 0 V b) less than 0 V

c) equal to 0 V d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Describe photolithography process.

3. What is the problem of realizing a large value resistor by a MOSFET structure ? How can a switched capacitor be used to overcome this problem ? 2 + 3

4. What are the advantages of TG logic design style ? Explain with neat sketch the construction and operation of an XOR gate using TG design style. 1 + 4

5. How can resistance of a current source/sink be improved ?

6. Explain the operation of clocked CMOS S-R latch circuit.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Classify the different types of ASIC design.

b) Design the following circuit using PAL, PLA and PROM :

$Y1 = AB + A'C + ABC', Y2 = AB'C, Y3 = BC + ABC'$.

c) What do you mean by 'Lambda Rule' & 'Micron Rule' ? Draw the Layout & Schematic diagram of a static CMOS NAND/NOR gate & identify the corresponding components in the two drawing. 3 + 6 + 6

8. a) Design AND/NAND, XOR/XNOR gates using Pass Transistor Logic.

b) Describe the Logic '0' and logic '1' transfer mechanism of a Pass Transistor.

c) Design a CMOS Master Slave D flip-flop and describe its operation. 4 + 6 + 5

9. a) Describe the Fick's law for Diffusion process. What do you mean by Isotropic & Anisotropic Etching processes ?

b) Describe the Photolithographic process for MOSFET fabrication.

c) Describe the CMOS fabrication process with proper diagram. 5 + 4 + 6

10. a) What do you mean by Series-Parallel switched capacitor circuit ? Describe briefly.

b) Describe the different types of Switched Capacitor Integrator Circuit. Describe the drawbacks of discrete-time integrator. How do you solve this drawback ?

c) Design the 1st and 2nd order switched capacitor low-pass filters. 4 + 5 + 6

11. Write short notes on any *three* of the following : 3 × 5

a) Domino logic

b) Design of $M \times N$ bit SRAM

c) Switch capacitor

d) CPLD

e) CMOS NORA logic.

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