ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER – 2007

DIGITAL INTEGRATED CIRCUITS

SEMESTER – 3

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) The maxterms corresponding to decimal 15 is

a) $ABCD$ b) $\bar{A} + \bar{B} + \bar{C} + \bar{D}$

c) $A + B + C + D$ d) $\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D}$. ☐

ii) The decimal equivalent of $(332)_4$ is

a) 63 b) 94

c) 62 d) None of these. ☐

iii) Gray code of a binary number 1011 is

a) 1110 b) 1100

c) 1101 d) None of these. ☐

iv) The fast logic family is

a) TTL b) ECL

c) CMOS d) DTL. ☐

v) The decimal $(48)_{10}$ is represented in BCD by

a) 11011100 b) 01001000

c) 11100010 d) 00111010. ☐

vi) PROMs are used primarily for

a) data storage

b) temporary program and data storage

c) they are inexpensive

d) permanent program and data storage. ☐

vii) $3 \times 512 + 7 \times 64 + 5 \times 8 + 3$ then value in binary form contains ..... number of 1's.

a) 7 b) 6

c) 9 d) 8. ☐

viii) The minimum number of NAND gates required to implement AθB (XOR) is

a) 3 b) 4

c) 5 d) 6. ☐

ix) Which of the following are correct ?

1. A flip-flop is used to store 1-bit of information
2. Race around condition occurs in JK flip-flop when both the inputs are 1
3. Master-slave flip-flop is used to store 2 bits of information
4. A transparent latch consists of a D-flip-flop.

a) 1, 2, 3 b) 1, 3, 4

c) 1, 2, 4 d) 2, 3, 4. ☐

x) Minimum number of 2-input NAND gates that will be required to implement the function :

$Y = AB + CD + EF$ is

a) 4 b) 5

c) 6 d) 7. ☐

xi) The octal form of $(FAFAFA)_{16}$ is

a) 76767676 b) 76575372

c) 76737672 d) 76727672. ☐

xii) The output of a sequential circuit depends on

a) Present input b) Past input

c) Both present and past d) Past output. ☐

xiii) A code used for labelling the cell of K-map is

a) Natural BCD b) Gray Code

c) Hexadecimal Code d) Octal Code. ☐

xiv) A ring counter consisting of 5 flip-flop will have

a) 5 states b) 10 states

c) 32 states d) Infinite states. ☐

xv) The total conversion time need for Successive Approximation type *N*-bit ADC is

a) ($N \times 1$) clock time period b) ($2^N \times 1$) clock time period

c) ($2^N - 1$) clock time period d) None of these. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following questions. $3 \times 5 = 15$

2. Define the following terms : 5×1

a) Noise Margin

b) Fan-in

c) Fan-out

d) Power dissipation

e) Unit TTL load.

3. Design a 5 to 32 Decoder using one 2 to 4 and four 3 to 8 Decoder IC. 5

4. Use K-Map to simplify the following Boolean expression :

$F(W, X, Y, Z) = \sum m(0, 2, 6, 8, 12, 13, 14) + \sum d(3, 9, 10)$. 5

5. Design a 2-input NAND gate using CMOS inverter. 5

6. Which minterm is present in the function —

$F = (A + B)(AB + C)(B + AC)$? 5

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following questions. 3 × 15 = 45

7. a) Implement a 16 to 1 multiplexer using two 8 to 1 multiplexer ICs (IC 74151)

   b) Design a Gray code to Binary converter.

   c) Explain differences between a DEMUX and MUX. 6 + 7 + 2

8. a) Discuss the difference between synchronous and asynchronous sequential circuits.

   b) Discuss the difference between combinational and sequential circuit.

   c) Write down the characteristic equation of J-K flip-flop. 5 + 3 + 7

9. a) What is meant by duality of Boolean algebra ? Simplify the following Boolean function using K-map and realize the simplified function using NOR gates only :

   $$F(A, B, C, D) = \prod_M (1, 2, 3, 8, 10, 11, 14) + \Sigma_d (7, 15).$$

   b) Construct a 5 × 32 decoder with four 3 × 8 decoder and a 2 × 4 decoder. Show block diagram only. 10 + 5

10. What do you mean by irregular sequence counter ? Design the counter with the following sequence $3 \rightarrow 2 \rightarrow 7 \rightarrow 5 \rightarrow 6$. Show detail state diagram, state table and design procedure. Draw the logic diagram. Use J-K all flip-flops and other necessary logic gates. 5 + 10

11. Write short notes on any *three* : 3 × 5

    a) Johnson Counter

    b) Propagation Delay

    c) Parallel-In-Serial-Out (PISO)

    d) Even Parity Generator & Checker

    e) Tri-State gates in TTL family.

END