CS/B.Tech (ECE-OLD) (Supple)/SEM-7/EC-702(O)/09
VLSI DESIGN (SEMESTER - 7)

1. .....
Signature of Invigilator

2. .....
Signature of the Officer-in-Charge

Reg. No.

Roll No. of the Candidate

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CS/B.Tech (ECE-OLD) (Supple)/SEM-7/EC-702(O)/09
ENGINEERING & MANAGEMENT EXAMINATIONS, JULY – 2009
VLSI DESIGN (SEMESTER - 7)

Time : 3 Hours] [Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. This Booklet is a Question-cum-Answer Booklet. The Booklet consists of **32 pages**. The questions of this concerned subject commence from Page No. 3.
2. a) In **Group – A**, Questions are of Multiple Choice type. You have to write the correct choice in the box provided **against each question**.
   b) For **Groups – B** & **C** you have to answer the questions in the space provided marked 'Answer Sheet'. Questions of **Group – B** are Short answer type. Questions of **Group – C** are Long answer type. Write on both sides of the paper.
3. **Fill in your Roll No. in the box** provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. **Use of Mobile Phone and Programmable Calculator is totally prohibited in the examination hall.**
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, **which will lead to disqualification**.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

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Marks Obtained

	Group – A										Group – B			Group – C				
Question Number																	***Total Marks***	***Examiner's Signature***
Marks Obtained																		

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Head-Examiner/Co-Ordinator/Scrutineer

S–53033 (29/07) (O)

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VLSI DESIGN

SEMESTER - 7

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) Frequency compensation of Op-Amp using MOS technology is done by

a) decreasing the number of stages

b) minimising the number of poles in signal path

c) achieving low voltage gain

d) all of these.

ii) To implement the Boolean function $F = \overline{A\,(B + CD)}$ using static CMOS technology, number of MOSs required is

a) 4 b) 8

c) 6 d) 12.

iii) Resistive load in the *n*-MOS inverter is not used because

a) frequency of operation will be reduced too much

b) area required by the resistive load in the layout is very large

c) power dissipation of the inverter will be very large

d) the circuit will not be an inverter at all.

iv) In a TG one pMOS is connected in parallel with an nMOS because

a) current capability is increased by the parallel combination of transistor

b) the operating voltage is increased

c) it passes both a.c. and d.c. voltages

d) full voltage same as input appears at the output. ☐

v) Edge-triggered D-flip-flop circuit is configured

a) by detecting the edge of the clock by using RC differentiator circuit

b) by using the comparator

c) by using master/slave configuration

d) by using an integrator circuit. ☐

vi) The model parameter LAMBDA (λ) in a MOS structure stands for

a) Flicker noise coefficient b) Transit time

c) Channel length modulation d) Transconductance. ☐

vii) Which is not a part of Complementary Pass Transistor Logic (CPL) ?

a) Complementary output b) Complementary input

c) CMOS TG d) CMOS inverter. ☐

viii) The time for a logic circuit to make two successive transitions is called

a) clock frequency b) cycle time

c) propagation delay d) hold time. ☐

ix) A logic gate has V_{OH} = 5V, V_{OL} = 0.3V, V_{IH} = 2.2V and V_{IL} = 0.7V. The noise margin is

a) 0.6 V and 2.4 V b) 0.6 V and 0.6 V

c) 0.9 V and 0.9 V d) 1 V and 0 V. ☐

x) Which of the following is not a step of VHDL programming ?

a) Entity declaration b) Architecture body

c) Configuration declaration d) Package architecture. ☐

xi) Noise margin (NM) for low voltages is defined as

a) $NM_L = V_{IL} - V_{OL}$ b) $NM_L = V_{IL} - V_{IH}$

c) $NM_L = V_{OH} - V_{OL}$ d) $NM_L = V_{IH} - V_{IL}$. ☐

xii) Because of trapping & release of electrons in the Si/SiO_2 interface, association noise is known as

a) White noise b) Thermal noise

c) Flicker noise d) none of these. ☐

xiii) Stick diagram carries out the information about the

a) actual geometry relations of the individual circuit components

b) relative placement of the transistors and their interconnections

c) layout area of the devices

d) none of these. ☐

xiv) Pseudo NMOS logic provides which of the following advantages ?

a) Static power dissipation is less compared to CMOS logic

b) It is much faster compared to other logics

c) It requires less no. of transistors compared to CMOS logic

d) It is more noise immune.

xv) Scaling is done for

a) improving the switching speed

b) decreasing the power dissipation

c) reducing the chip size

d) all of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 ∞ 5 = 15

2. What are the effects that cause a practical current mirror to behave differently from an ideal one ? Discuss any one of them. 2 + 3

3. Calculate the Gate Capacitance of MOSFET after scaling in constant electric field model and constant voltage model. What is the advantage of constant electric field model after scaling ? 4 + 1

4. What do you mean by Channel Length Modulation for a MOS ? How is drain current related with Channel Length Modulation Coefficient ? 3 + 2

5. Prove that for a bilinear-switched capacitor realization of resistor, the equivalent resistance is $T/(4C)$ where T is the clock period and C is the capacitance of the circuit. 5

6. Implement the Boolean function $F = \overline{ABC + DE}$, using dynamic CMOS logic. 5

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Explain the operation of a 6-Transistor SRAM with neat sketch. 10

   b) Implement the following functions using CMOS TG : 5

   $Y = A\bar{B} + \bar{A}\,B$.

8. a) What are current source and current sink ? 3

   b) What is current mirror ? Explain the operation of MOS current mirror. 8

   c) What is Wilson current mirror ? Mention its' merits. 4

9. a) What is VHDL ? 2

   b) Explain the following terms related to VHDL : 4×2

      i) Entity

      ii) Signal

      iii) BUS

      iv) Generic.

   c) Write a VHDL code for a Full Adder cricuit. 5

10. a) Describe in detail Lambda – based design rule for lay out design. 10

b) What is stick diagram ? Mention it's use. 5

11. Write short notes on any *three* of the following : 3 ∞ 5

a) Constant Voltage Scaling

b) CMOS NORA Logic

c) Drain induced barrier lowering (DIBL)

d) Pass-Transistor

e) Clock Skew phenomenon in sequential circuits.

END