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**MAULANA ABUL KALAM AZAD UNIVERSITY OF  
TECHNOLOGY, WEST BENGAL**

**Paper Code : EC-702**

**MICROELECTRONICS & VLSI DESIGNS**

*Time Allotted : 3 Hours*    makautonline.com    *Full Marks : 70*

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own  
words as far as practicable.*

**GROUP - A**    makautonline.com

**( Multiple Choice Type Questions )**

1. Choose the correct alternatives for any ten of the following :  $10 \times 1 = 10$
- i) Among the following which one has the greatest gate integration capacity ?
- a) ☒ FPGA                      b) ☐ CPLD
- c) ☐ PLD                        d) ☐ ASIC.
- ii) FPGA is a    makautonline.com
- a) ☐ full-custom ASIC
- b) ☐ semi-custom ASIC
- c) ☒ programmable ASIC
- d) ☐ none of these.

iii) VHDL is a    makautonline.com

- a) ☒ multithreaded program
- b) ☐ a programming language like C
- c) ☐ single user program
- d) ☐ sequential program.

iv) The body effect occur due to potential difference between    makautonline.com

- a) ☒ source and body    b) ☐ body and drain
- c) ☐ gate and body        d) ☐ none of these.

v) In channel length modulation, the drain current

- a) ☐ increase                      b) ☐ decrease
- c) ☐ constant                      d) ☐ zero.

vi) PMOS are wider than NMOS transistor    makautonline.com

- a) ☒ mobility of holes is less than electrons
- b) ☐ mobility of holes is greater than electrons
- c) ☐ PMOS length is shorter than NMOS length
- d) ☐ does not depend on mobility.

vii) One of the disadvantage of pass transistor logic

- a) less number of transistor
- b) poor noise margin
- c) only NMOS are use
- d) none of these.

viii) Pinch of region of MOS transistor the current become

- a) saturated
- b) non-saturated
- c) decrease
- d) increase exponentially.

ix) Maximum transistor gate required to design XOR gate in CMOS structure

- a) 6
- b) 8
- c) 12
- d) 10.

x) Low power logic family is

- a) TTL
- b) CMOS
- c) ECL
- d) none of these.

xi) Memory configuration of CPLD is

- a) volatile
- b) non-volatile
- c) both volatile and non-volatile
- d) does not have memory.

xii) Scaling is done for

- a) improving switching capacity
- b) decreasing the power dissipation
- c) reduce chip size
- d) all of these.

### GROUP - B

#### ( Short Answer Type Questions )

Answer any *three* of the following.  $3 \times 5 = 15$

Describe the N-well CMOS fabrication process.

Draw and explain the operation of MOS Switched Capacitor Integrator.

4. What is MOSFET scaling ? What is the need of scaling ?

Compare various types of scaling.

1 + 2 + 2

5. What do you mean by 'Lambda rule' and 'Micro rule'?

Draw the stick diagram and schematic diagram of Static

CMOS NAND gate. **makautonline.com** 2 + 3

6. Explain with a circuit diagram, operation of a differential amplifier.

### GROUP - C

#### ( Long Answer Type Questions )

Answer any *three* of the following.  $3 \times 15 = 45$

7. a) Design a CMOS Master Slave D flip-flop and describe its operation.

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b) What is TG? Design the 4 : 1 MUX using TG.

c) What are the different types of lithography process? Describe photolithography with diagram.

5 + 5 + 5

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8. a) Why is reference voltage required in IC? What are the criteria for a good reference voltage source in VLSI circuit?

b) Explain the operation of a band gap voltage reference source in a VLSI circuit. **makautonline.com**

c) Explain briefly different stages of an operational amplifier with the help of a block diagram. 2 + 9 + 4

9. a) Explain why NMOS is preferred for pull-down network and PMOS is preferred for pull-up network. **makautonline.com**

b) Explain different power dissipation in CMOS.

c) Describe fick's law for diffusion process. What do you mean by Isotropic and Anisotropic Etching process? **makautonline.com**

d) What are the differences in between diffusion and ion implantation?  $3 + 3 + (3 + 3) + 3$

10. a) Design AND/NAND, XOR/XNOR gates using complementary pass transistor logic.

b) Describe the logic '0' and logic '1' transfer mechanism of Pass-Transistor.

c) Explain dynamic CMOS logic and Domino CMOS logic with suitable diagram. 5 + 5 + 5

~~X~~11. Write short notes on any *three* of the following :  $3 \times 5$

a) Constant voltage scaling

✓ b) ASIC

c) Comparator

✓ d) Programming methods of FPGA

e) Short channel effects.

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