2014

Digital Electronic & Integrated Circuits

Time Alloted : 3 Hours *Full Marks : 70*

The figure in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP - A

(Multiple Choice Type Questions)

1. **Choose the correct alternatives for any ten of the following** **10x1=10**

   i) Gray code of $(110101)_2$ is

   a) 101111 b) 100110 c) 111010 d) 101011

   ii) If $(211)_x = (152)_8$, then the value of base x is

   a) 6 b) 5 c) 7 d) 9

   iii) Minimum number of 2-input NOR gates are required to design a 2-input NAND gate is

   a) 1 b) 2 c) 3 d) 4

   iv) Which of the following expressions is in the sum-of-products (SOP) form?

   a) (A+B) (C+D) b) (A) B (CD)
   c) AB (CD) d) AB + CD

   v) In fig.- 1 the input condition, needed to produce X = 1, is

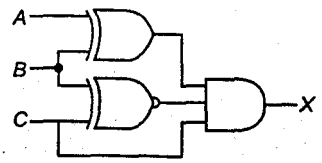

Fig.-1

a) A = 1, B = 1, C = 0 b) A = 1, B = 1, C = 1
c) A = 0, B = 1, C = 1 d) A = 1, B = 0, C = 0

vi) The minimization of logic expression is done in order to

a) reduces pace b) reduce cost
c) reduce number of gates d) all

vii) The number of 2 line to 4 line decoders are used to design a 4 line to 16 line decoder is

a) 2 b) 4 c) 5 d) 6

viii) The final carry output equation of carry-look-ahead addition is

a) $C_{n+1}=P_nC_n+G_n$ b) $C_{n+1}=P_n+C_nG_n$
c) $C_n=P_n+C_nG_n$ d) $C_n=P_nC_n+G_n$

ix) Multichannel signals can be transmitted through a single channel by using

a) demultiplexer b) encoder
c) decoder d) multiplexer

x) The initial output of S-R Flipflop Q is 0. It changes to 1, when a clock pulse is applied.
The input S and R will be-

a) S=1, R=1 b) S=0,R=0 c) S=0.R=1 d) S=1,R=0

xi) A Mod -2 counter, followed by a Mod -5 counter is

a) Decade counter b) Mod-9 counter
c) Mod-11 counter d) Mod-7 counter

xii) The Moore machine is defined by the following equations:

a) Next state = F (Present state, Inputs) and Outputs = G (Present State)
b) Next state=F(Inputs) and Outputs=G(Present State)

c) Next state=F(Present state) and Outputs=G(Present State)
d) Next state=F(Present state) and Outputs=G(Inputs)

GROUP - B

(Short Answer Type Questions)

Answer any *three* of the following 3x5=15

2. Convert J-K f/f to S-R f/f. (5)
3. Design a 16:1 multiplexer using 4:1 multiplexers only. (5)
4. Write down the excitation table of SR and T flip-flop and derive the characteristic equation for these two flip-flops. (2 + 3)
5. Design a bi-directional shift registers and explains its operation. (5)
6. Implement the BCD to Excess-3 code conversion using ROM. (5)
7. Design a full subtractor using two half-subtractors and OR gate. (5)

GROUP - C

(Long Answer Type Questions)

Answer any *three* of the following. 3x5=15

8. a) What is the main difference between a latch and a flip-flop?
   b) What is the race around condition? How can we overcome the race around condition?
   c) Design Mod-6 Synchronous counter using JK flip-flops and other gates.

   3 + (2 + 3) + 7

9. a) Consider a chemical mixing tank for which there are 3 variables of interest: liquid level, pressure and temperature.The alarm will be triggered under the following conditions:
      i) Low level with high pressure
      ii) High level with low pressure

iii) High level with low temperature and high pressure. Design the system, implement using only NOR gates.

b) Simplify using k-map in SOP form:
$F=\sum m(1,3,4,5,9,11,14,15)+\sum d(2,6,7,8)$

(10+5)

10. For Synchronous counter with sequence 2→6→5 →3→1→ 0→2
    i) Give present state/next state table.
    ii) Write state transition table using D flip-flops.
    iii) Simplify and realize the circuit. Draw the state diagram.
    iv) Justify whether the design counter will go in lockout condition or not.
    v) What should be the corrective design process to avoid the lockout condition?

(2+3+6+2+2)

11. What is the difference between synchronous counter and asynchronous counter? Realize a 4-bit Ring counter using JK flip flops. Develop the state table. Can this circuit be used to realize a frequency divider?

(5+8+2)

12. a) Define the resolution of a DAC. A 6-bit DAC has a step size of 50 mV. Determine the full scale output voltage and resolution.

    b) Describe the working principle of 4-bit R-2R ladder circuit.

    c) For a R-2R ladder 4-bit DAC converter with R=10KΩ and V_R=10V, find out the feedback resistance R_f of the OP-AMP for
    i) First LSB input at the output will be 0.1 V.
    ii) Analog output of 6 V for a binary input of 1000.
    iii) Full scale output voltage of 12 V.
    iv) The actual maximum output Voltage of 10 V.

(2+3)+5+5

13. Write short notes on any three of the following: (3x5=15)
    a) Venn diagram
    b) A 3-bit magnitude comparator
    c) Glitch and Spike
    d) Successive approximation ADC
    e) Draw the NAND, NOR, NOT gates using CMOS

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