Design Time Reduction of Analog Circuits using Machine Learning Techniques

Name: Gourav Tilwankar

Roll Number: 203070051
Email Id: gouravtil@ee.iitb.ac.in
Location: IIT Bombay

EE798: M.Tech. Thesis Project Phase 2

Supervisor: Prof. Rajesh H. Zele

Department of Electrical Engineering, IIT Bombay

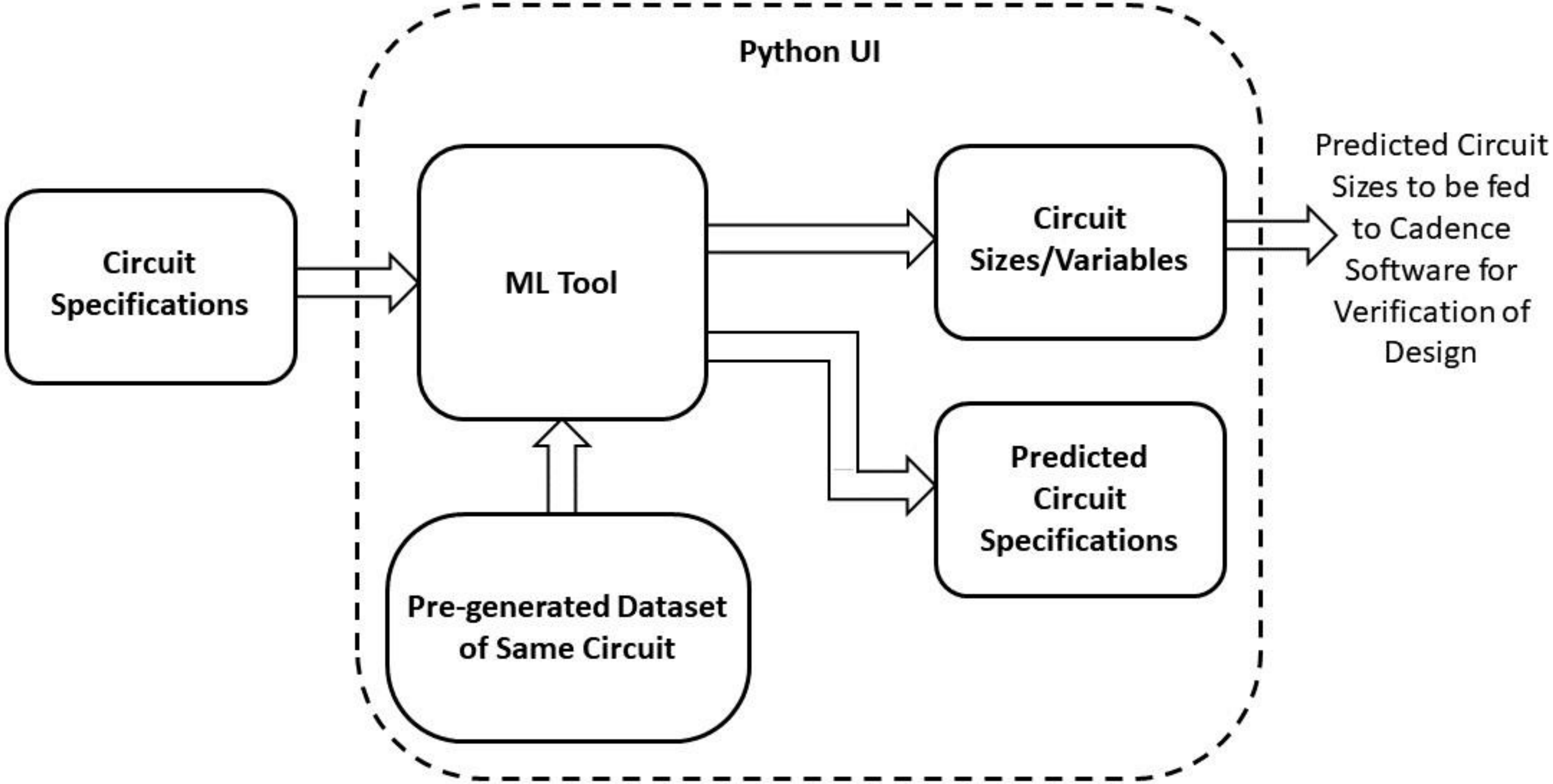
Project Objective

- Creation of a Machine Learning based tool that uses input-output relationships of a fully developed/designed circuit and gives the values of circuit parameters according to user specification.

- The circuit parameters used to feed into netlist – gives the verified output specifications

- No need of developing same circuit repeatedly for different specifications.

Block diagram of Project Objective



Outline

- Circuit Selection and Designing
- Different Testbenches in Cadence for Output Variables
- Converting Circuit parameters into Input Variables
- Dataset Generation
- Machine Learning Tool
- Testing of created tool
- Results

Circuit Selection and Designing

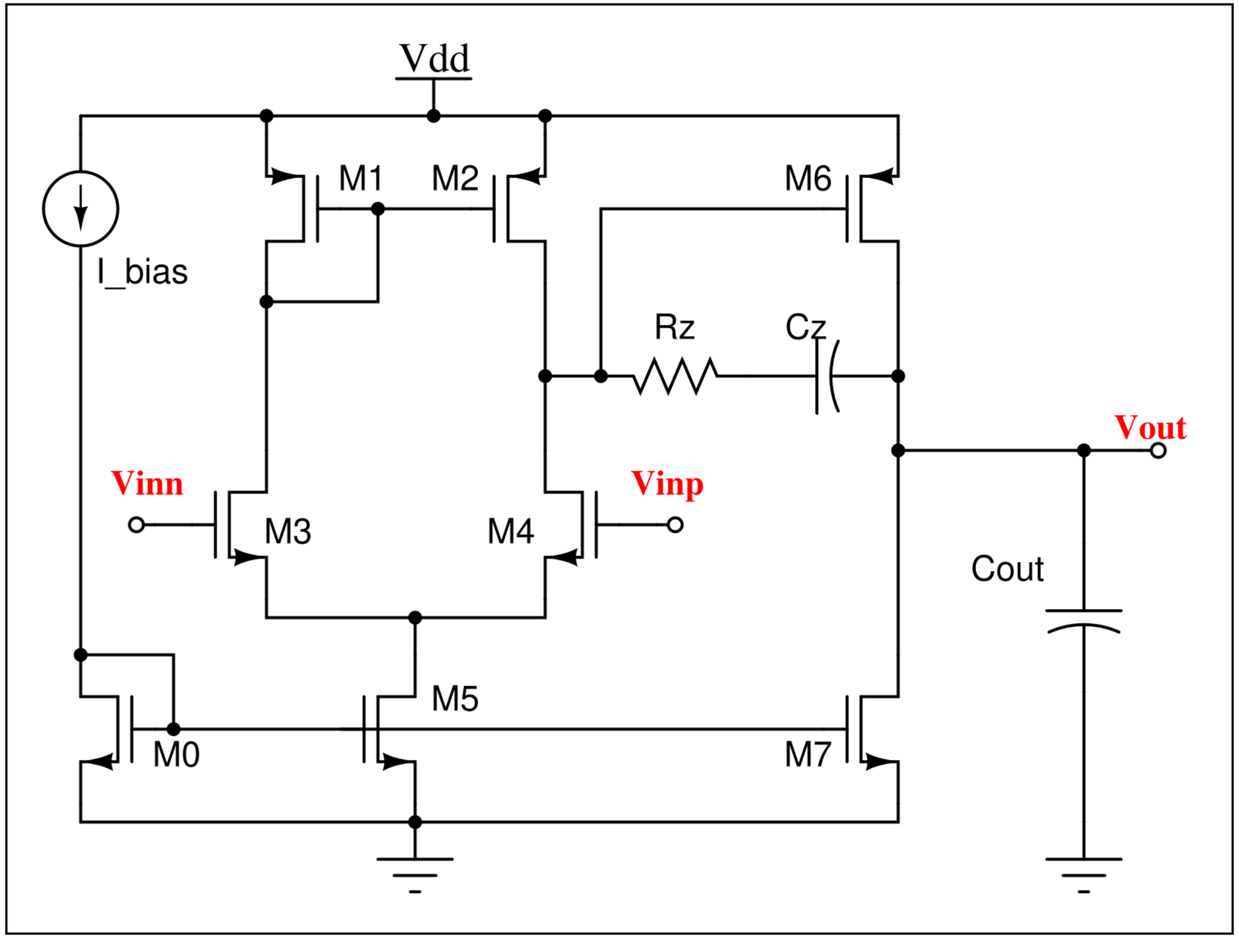


Fig: Two-stage Operational Amplifier with Miller Compensation [5]

NageshwarRao, Dr. D., K. Suresh Kumar, Y. Rajasree Rao and Grande Naga Jyothi. "Implementation and Simulation of Cmos Two Stage Operational Amplifier." (2013).

Circuit Selection and Designing

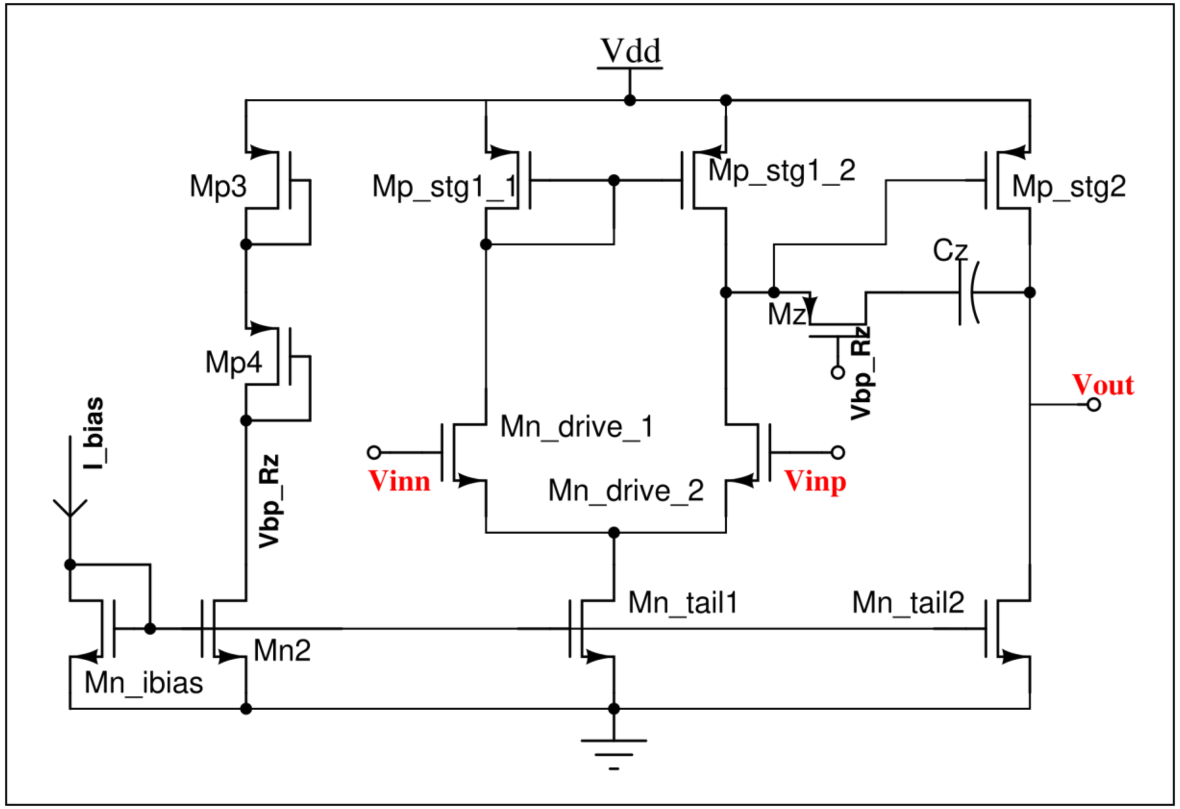


Fig: Modified Two-stage Operational Amplifier with Miller Compensation and Tracking Bias [2],[3]

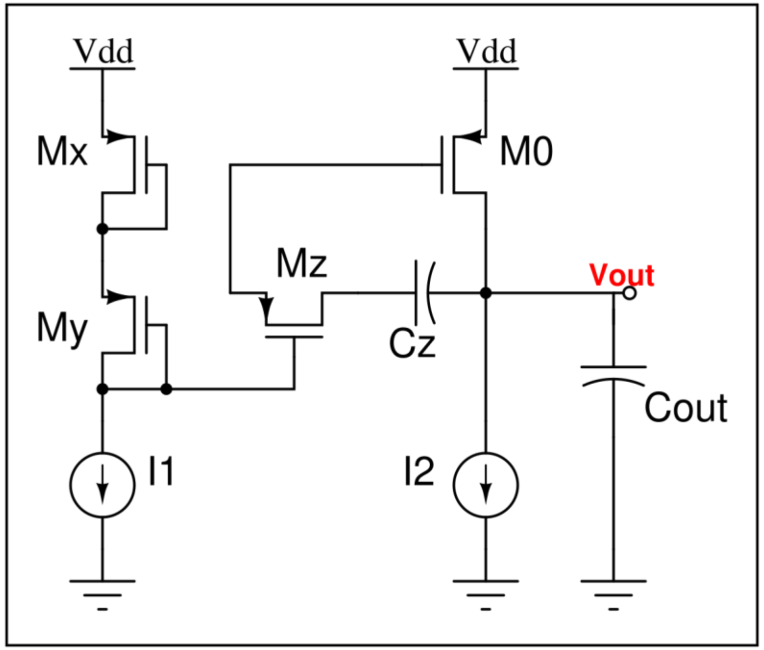


Fig: Tracking Bias Methodology [2],[3]

H. C. Yang and D. J. Allstot, "Modified modeling of Miller compensation for two-stage operational amplifiers," 1991., IEEE International Sympoisum on Circuits and Systems, 1991, pp. 2557-2560 vol.5, doi: 10.1109/ISCAS.1991.176049.

Y. -W. Kuo, P. K. Ramakrishna, A. V. Kayyil and D. J. Allstot, "Low-Voltage Tracking RC Frequency Compensation in Two-Stage Operational Amplifiers," 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS), 2019, pp. 782-785, doi: 10.1109/MWSCAS.2019.8885045.

Different Testbenches in Cadence for Output Variables

Different testbenches for obtaining output from circuit:

1. Stability Analysis
2. Slew Rate Analysis
3. Noise Analysis
4. CMRR Analysis
5. PSRR Analysis

Different Output Variables taken from Design:

1. DC Gain
2. DC Power
3. Slew Rate Value
4. Unity Gain Bandwidth
5. Phase Margin
6. 3dB Bandwidth
7. Noise at DC
8. Noise at 1 MHz
9. Noise at 10 MHz

Converting Circuit parameters into Input Variables

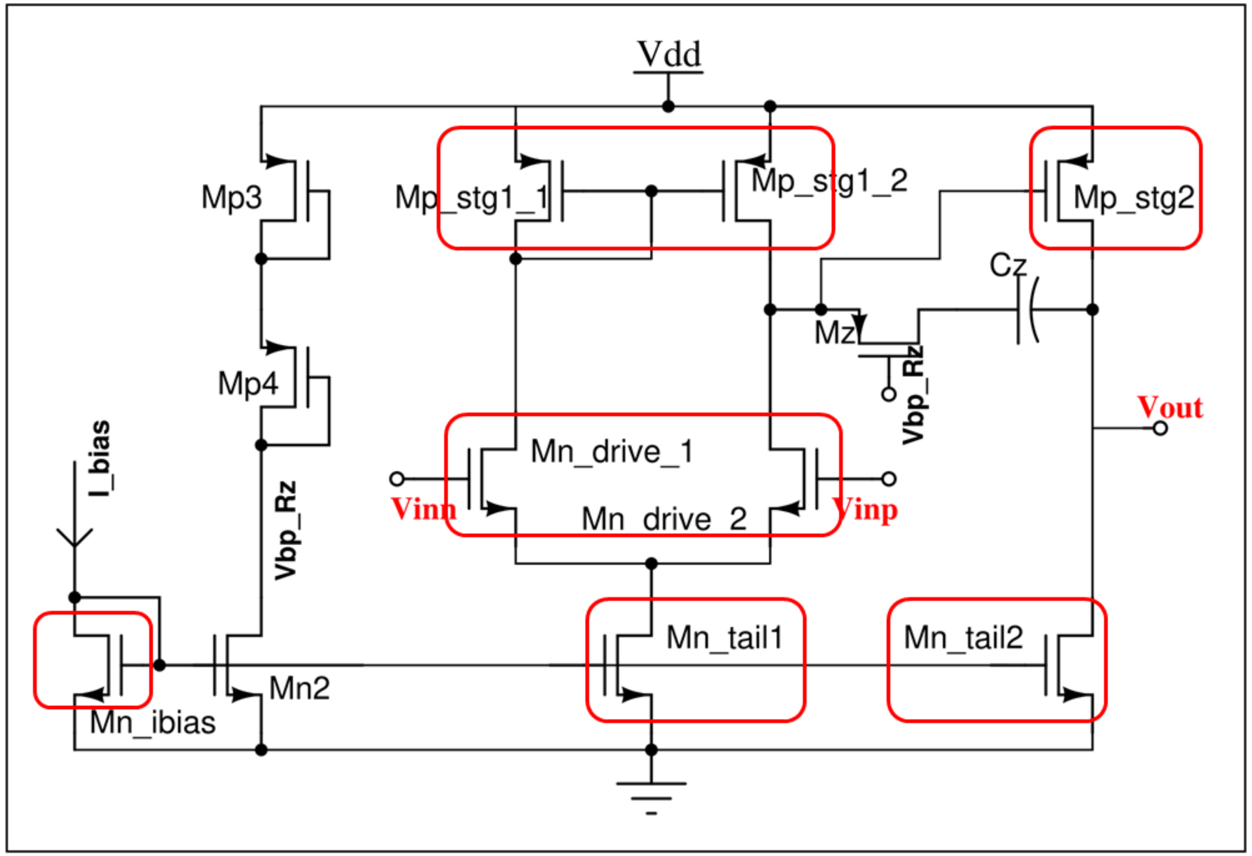


Fig: Iteration 1 for converting Sizes into Variables

Table: Variable Names in Circuit after Iteration 1

Lengths	Widths	Multipliers
L_Mn_drive	W_Mn_drive	mul_Mn_drive
L_Mn_tail1	W_Mn_tail1	mul_Mn_tail1
L_Mp_stg1	W_Mn_tail2	mul_Mn_tail2
	W_Mn_ibias	mul_Mn_ibias
	W_Mp_stg1	mul_Mp_stg1
	W_Mp_stg2	mul_Mp_stg2

Converting Circuit parameters into Input Variables

$$\frac{\mathbf{W}}{\mathbf{L}} = \left(\frac{\mathbf{nf} * \mathbf{Fw}}{\mathbf{L}}\right) * \mathbf{mul\_tran}$$

Table: Variable Names in Circuit after Iteration 2

Name of Transistor	Number of Fingers	Finger Width	Length of Transistor	Multiplier of Transistor
Mn_ibias	**nf_ibias**	0.5 µm	**L_Mn_tail1**	2
Mn_tail1	**nf_Mn_tail1**	0.5 µm	L_Mn_tail1	2
Mn_tail2	**nf_Mn_tail2**	0.5 µm	L_Mn_tail1	2
Mn_drive_1	**nf_Mn_drive**	0.5 µm	**L_Mn_drive**	2
Mn_drive_2	nf_Mn_drive	0.5 µm	L_Mn_drive	2
Mp_stg1_1	**nf_Mp_stg1**	0.5 µm	**L_Mp_stg1**	2
Mp_stg1_2	nf_Mp_stg1	0.5 µm	L_Mp_stg1	2
Mp_stg2	**nf_Mp_stg2**	0.5 µm	**L_Mn_stg2**	4
Mp_Rz	**nf_Rz**	0.5 µm	L_Mn_stg2	2
Mp3	**nf_Mp3**	0.5 µm	L_Mn_stg2	2
Mp4	**nf_Mp4**	0.5 µm	L_Mn_stg2	2
Mn2	nf_ibias	0.5 µm	L_Mn_tail1	2

Converting Circuit parameters into Input Variables

Lengths

- L_Mn_tail1
- L_Mn_drive
- L_Mp_stg1
- L_Mn_stg2

Number of Fingers

- nf_ibias
- nf_Mn_tail1
- nf_Mn_tail2
- nf_Mn_drive
- nf_Mp_stg1
- nf_Mp_stg2
- nf_Rz
- nf_Mp3
- nf_Mp4

→

Lengths

- L_Mn_tail1
- L_Mn_drive
- L_Mp_stg1

Number of Fingers

- nf_Mn_drive
- nf_Mn_tail1
- nf_ibias (not varied)
- nf_Mn_tail2
- nf_Mp_stg2

Other Variables

- mul_cap
- Ibias = 10 μA
- C_Load(not varied)=0.5 pF
- Vdd = 1.2 V

Dataset Generation

To generate Dataset for ML Tool, which variables need to be varied and in what range need to be known.

Hence, multiple attempts were made for the same.

Variable Name	Values
nf_ibias	2, 4, 8
nf_Mn_drive	13, 26, 53
nf_Mn_tail1	22, 44, 88
nf_Mn_tail2	115, 230, 460
nf_Mp_stg2	216, 432, 864

Table: Dataset 1

Variable Name	Values
nf_ibias	2, 4, 8
nf_Mn_drive	13, 26, 53
nf_Mn_tail1	22, 44, 88
nf_Mn_tail2	115, 230, 460
nf_Mp_stg2	216, 432, 864
mul_cap	6 : 2 : 14
ibias	5 μA : 3 μA : 20 μA

Table: Dataset 4

Final Dataset

- Length Variables not yet varied
- On changing on length variables, the aspect ratio changes for each transistor
- To keep aspect ratio same, number of fingers of transistors as a function of length of transistor

To study the effect of changing only length variables, 3 datasets generated keeping other variables same

Variable Name	Range/Values
L_Mn_drive	200 nm : 25 nm : 500 nm
L_Mn_tail1	1 µm : 100 nm : 3 µm
L_Mp_stg1	200 nm : 50 nm : 450 nm

Datasets	Dataset 5	Dataset 6	Dataset 7
nf_ibias	1	1	1
nf_Mn_tail1	10	8	12
nf_Mn_drive	26	22	32
nf_Mn_tail2	60	50	72
nf_Mp_stg2	216	180	280
mul_cap	10	10	10
ibias (µA)	10	10	10

Table: Variable Length with multiple set of constant values for other variables

Final Dataset (contd.)

Then all the Length variables are kept constant, while changing the rest of the variables.

Table: Dataset 8

Variable Name	Values
nf_Mn_drive	2 : 7 : 72
nf_Mn_tail1	2 : 6 : 32
nf_Mn_tail2	20 : 40 : 260
nf_Mp_stg2	100 : 100 : 1000
mul_cap	6 : 2 : 14

Table: Number of Combinations in each Dataset

Dataset	No. of Combinations
Dataset 5	13 * 21 * 6 = **1638**
Dataset 6	13 * 21 * 6 = **1638**
Dataset 7	13 * 21 * 6 = **1638**
Dataset 8	11 * 6 * 7 * 10 * 5 = **23100**

Final Dataset (contd.)

Although, we now have a valid dataset, but it contains combinations of failed simulations also.

Table: Valid Combinations in Final Dataset

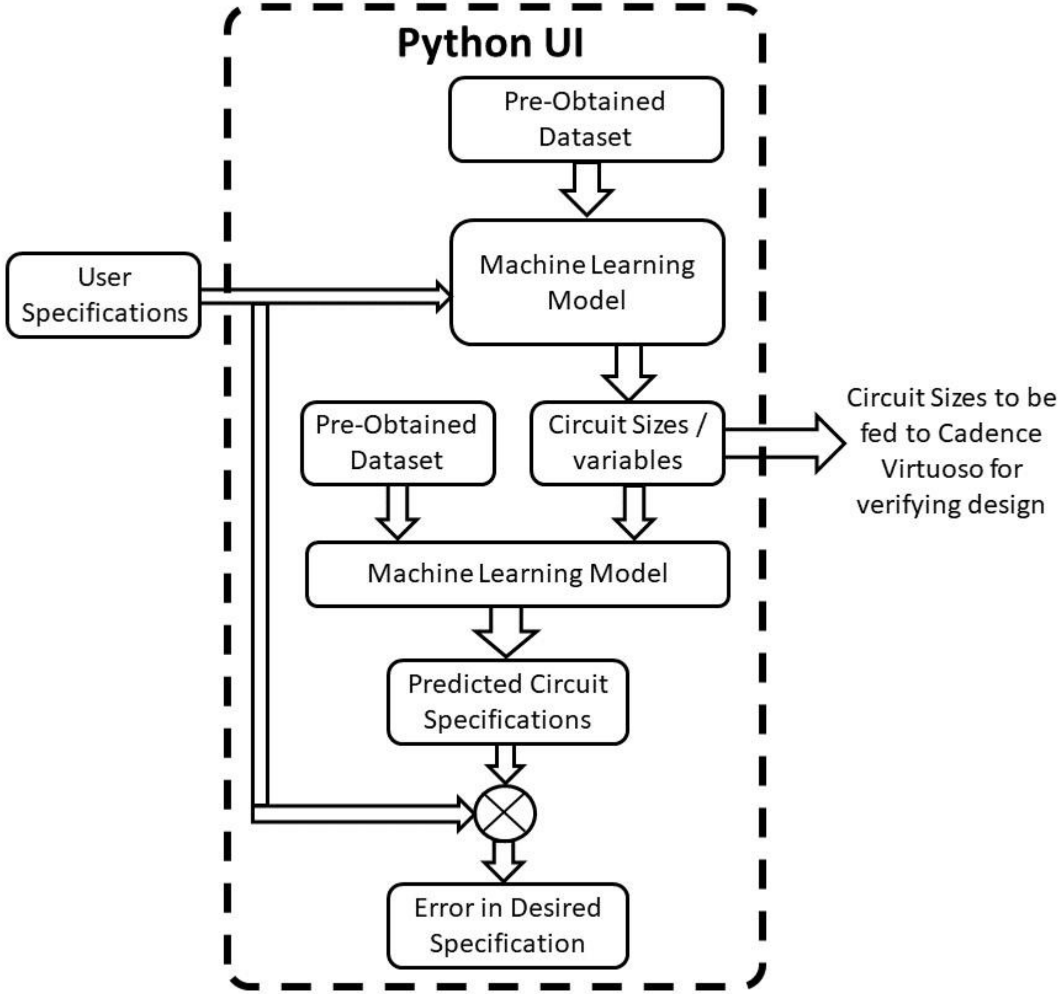
Datasets	Pass	Near/Fail	Total
Dataset 5	1610	28	1638
Dataset 6	1360	268	1638
Dataset 7	1541	97	1638
Dataset 8	9466	13634	23100
Total	**13977**	14037	28014

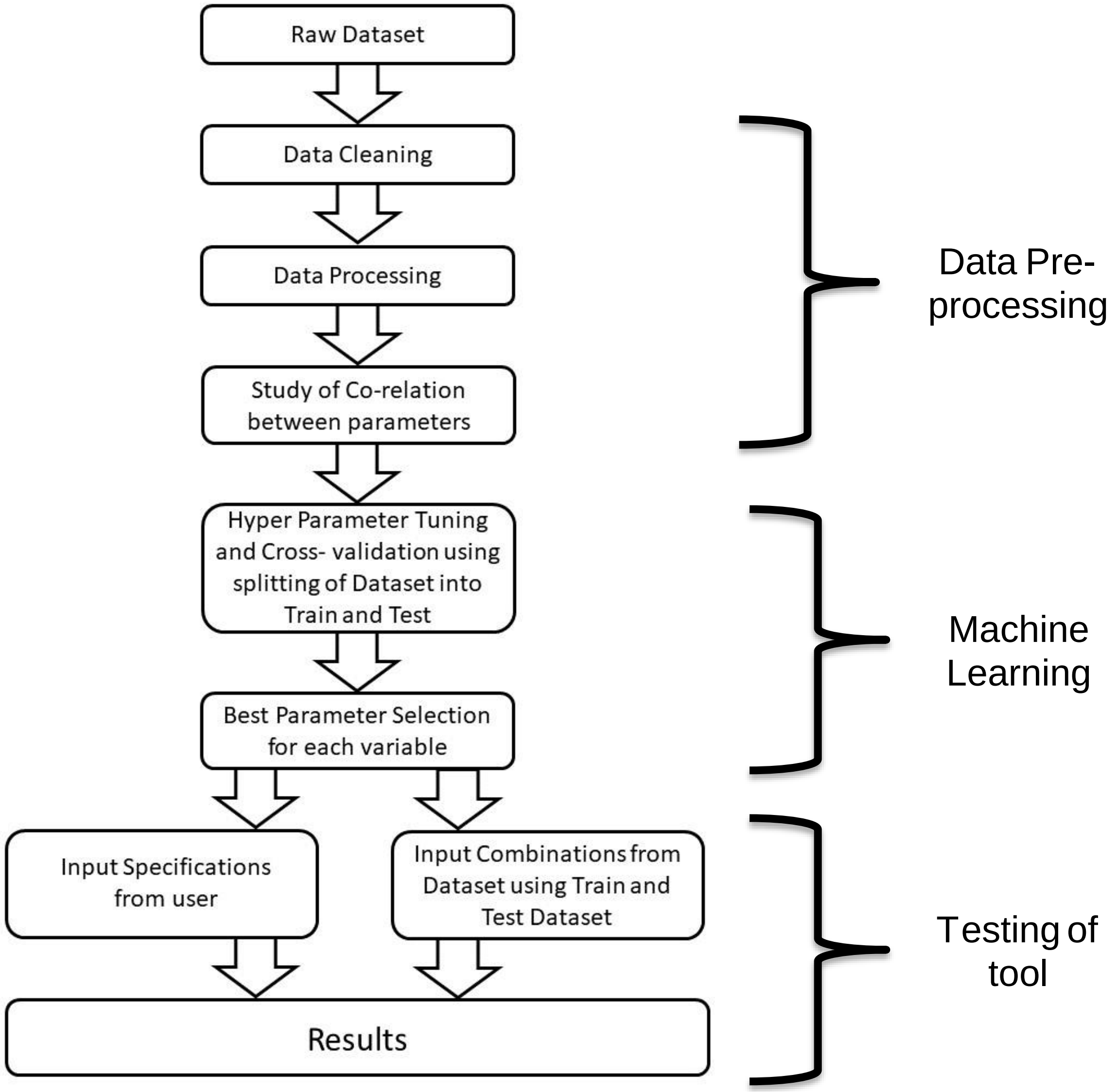
The criteria for a simulation to be considered as "Pass":

- **Phase Margin > 45º**
- **Region of all transistors = "Saturation"**
- **Region of Mp_Rz = "Linear", since transistor acting as resistor**

"Pass" Combinations only are considered in Machine Learning Tool

Flowchart of Machine Learning Tool





Machine Learning Technique used

The ML technique used here is **Support Vector Regression (SVR)**

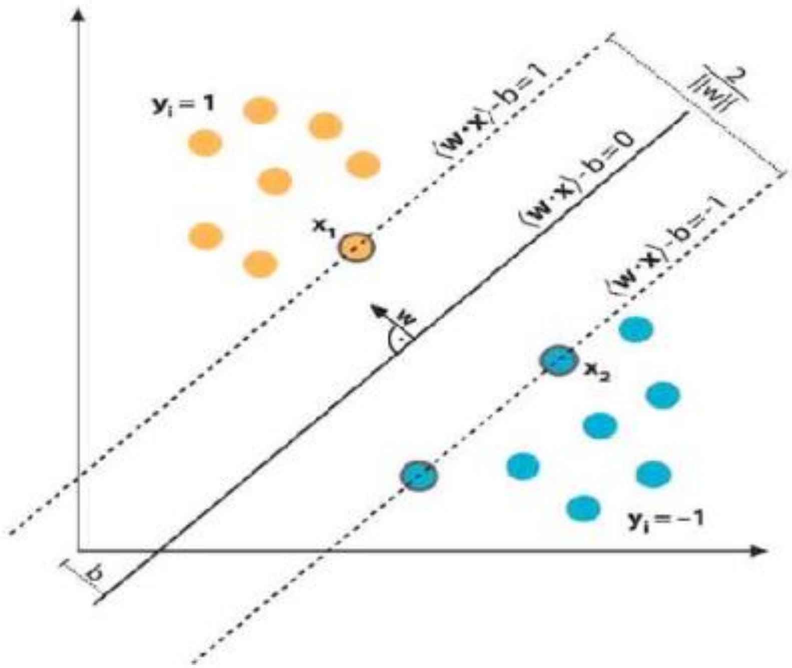


Fig: Support Vector Regression Hyper Plane

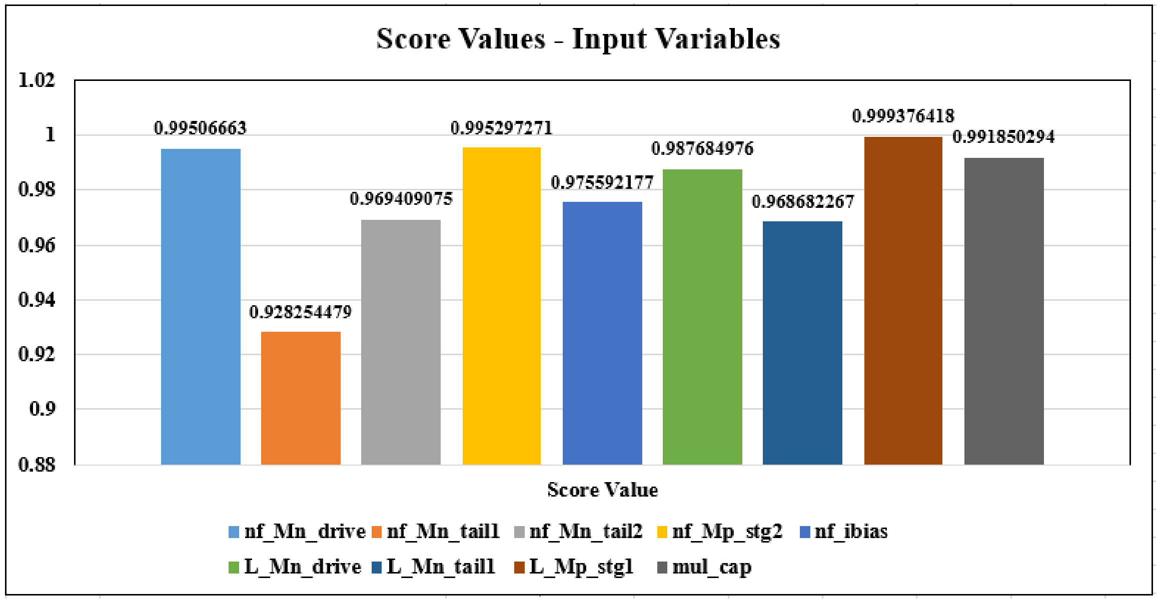
Hyperparameters used:

- **Kernel**
- Kernel Co-efficient, **gamma**
- tolerance for stopping criterion**, tol**
- Regularization Parameter, **C**
- **epsilon**

Hyper-parameter Name	Set of Values selected
kernel	linear, rbf, poly, sigmoid
gamma	1, 0.1, 0.01, 0.001
tol	0.1, 0.01, 0.001
C	0.1, 1, 10, 50
epsilon	1, 0.1, 0.01, 0.001

Hyper-Parameter Tuning

After selecting best parameters from Hyper-parameter Tuning, the score for each variable is given below:



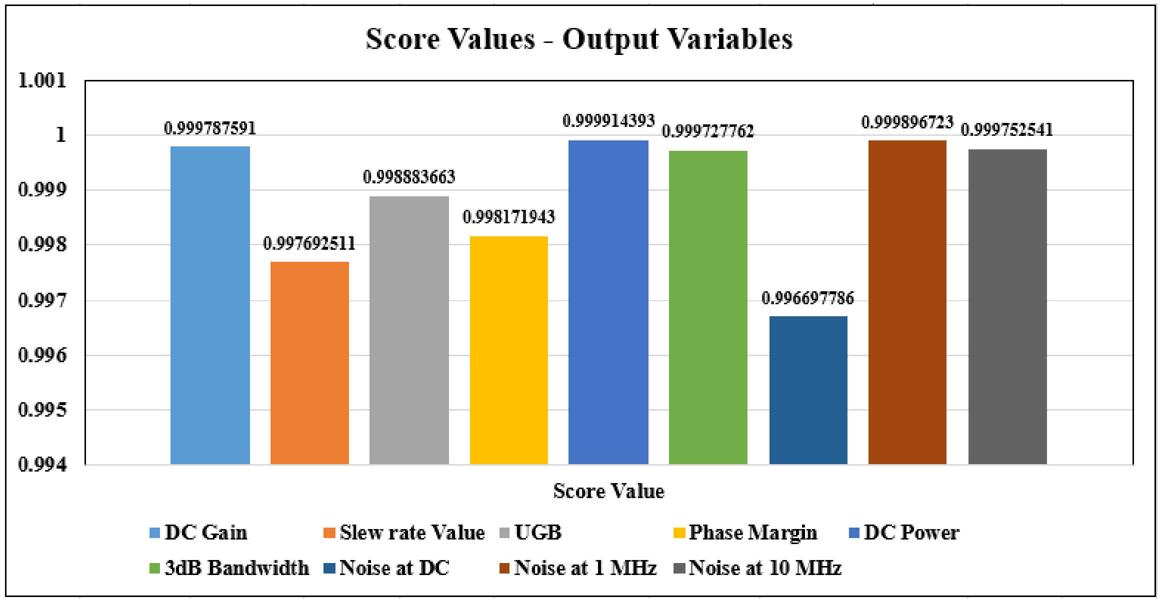


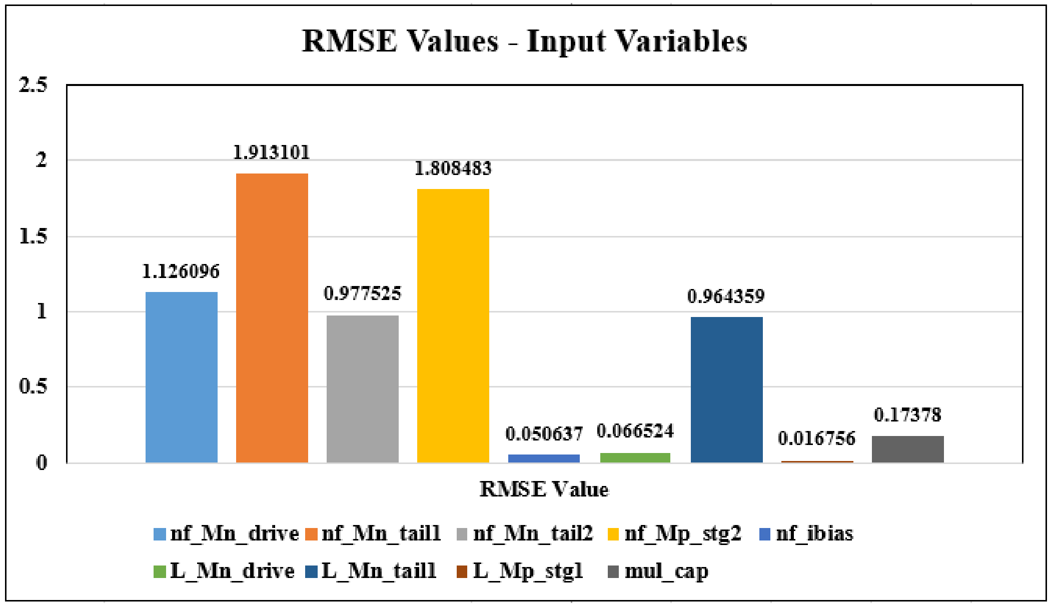
Fig: Score Values for Input and Output Variables after Hyper-parameter Tuning

- Score Value = 1 denotes perfect predictions
- Score Value = 0 denotes random predictions

Testing of created tool

The input can be taken from:

- Dataset (Train and Test Dataset)
- User (Using UI window)



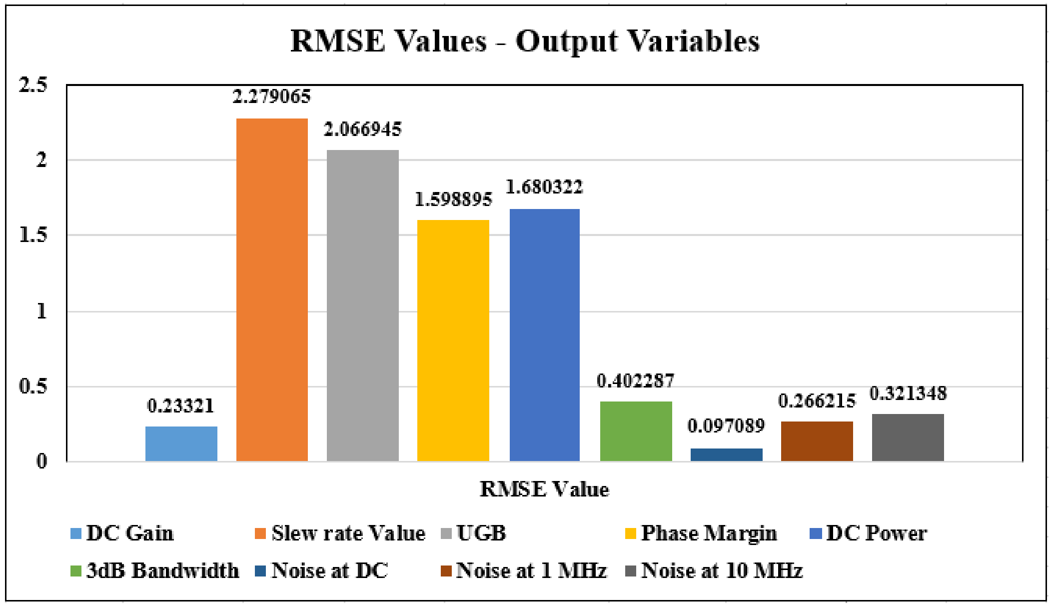
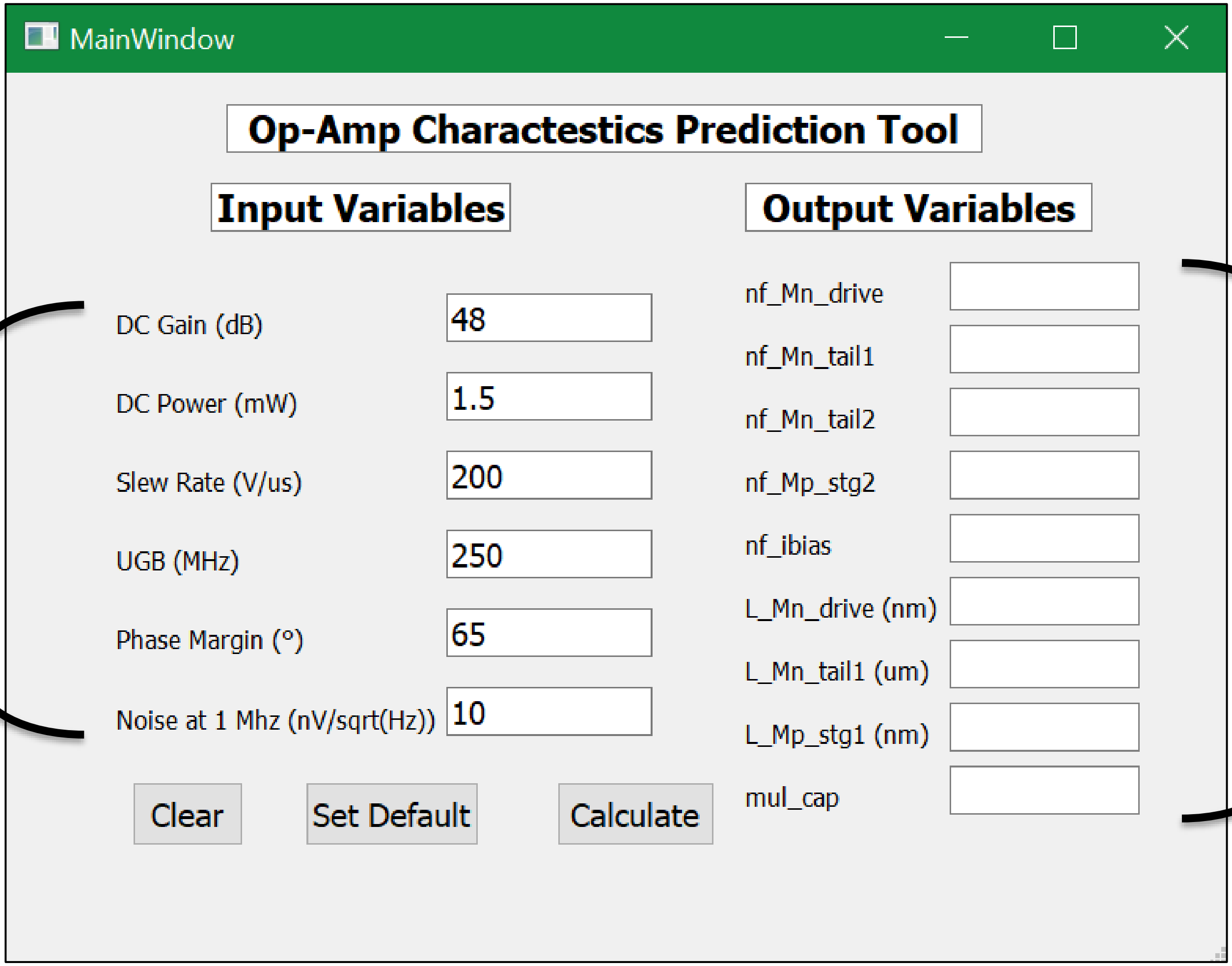


Fig: RMSE Values for Input and Output Variables using Test Dataset

Testing Machine Learning Tool (UI Window)

Input Specifications for 2-stage Operational Amplifier Circuit



Output Circuit Parameters for 2-stage Operational Amplifier Circuit

Fig: UI Window of created ML tool

Results

Table: Set 1 of Desired Value, Actual Value and Predicted Value of Specifications

Specifications	Desired Value	Actual Value (Cadence Output)	Predicted Value (ML tool Output)
DC Gain (dB)	48	50.63	50.19
DC Power (mW)	1.5	0.859	0.868
Slew Rate (V/µs)	200	141.2	133.66
UGB (MHz)	250	162	160.93
Phase Margin (º)	65	62.03	62.2
3dB Bandwidth (MHz)	4.55	2.7	3.03
Noise at DC (µV/$\sqrt{Hz}$)	33.32	24.13	29.83
Noise at DC (nV/$\sqrt{Hz}$)	10	9.232	10.23
Noise at DC (nV/$\sqrt{Hz}$)	7.261	8.19	8.79

Results

Table: Set 2 of Desired Value, Actual Value and Predicted Value of Specifications

Specifications	Desired Value	Actual Value (Cadence Output)	Predicted Value (ML tool Output)
DC Gain (dB)	45	48.53	48.02
DC Power (mW)	1	0.503	0.432
Slew Rate (V/µs)	300	214	228
UGB (MHz)	270	167.9	155.11
Phase Margin (º)	60	52.7	53
3dB Bandwidth (MHz)	4.91	3.04	3.39
Noise at DC (µV/$\sqrt{Hz}$)	40	21.95	24.55
Noise at DC (nV/$\sqrt{Hz}$)	12	9.178	10.64
Noise at DC (nV/$\sqrt{Hz}$)	8.72	7.568	8.43

Results

Table: Set 3 of Desired Value, Actual Value and Predicted Value of Specifications

Specifications	Desired Value	Actual Value (Cadence Output)	Predicted Value (ML tool Output)
DC Gain (dB)	50	48.78	48.79
DC Power (mW)	1.5	1.624	1.575
Slew Rate (V/µs)	400	271.9	250
UGB (MHz)	500	314.2	318
Phase Margin (º)	65	73.17	78.78
3dB Bandwidth (MHz)	9.10	5.37	5.58
Noise at DC (µV/$\sqrt{Hz}$)	33.32	45.67	45.57
Noise at DC (nV/$\sqrt{Hz}$)	10	10.11	10.4
Noise at DC (nV/$\sqrt{Hz}$)	7.261	7.49	7.78

Conclusion

- A Tool has been created which combines the knowledge of Analog Circuits and Machine Learning to predict the circuit parameters of **2-stage Single Ended Operational Amplifier** with Miller Compensation and Tracking Bias.
- We created **Multiple Circuit netlist** for **different specifications** as desired by user.
- The design of circuit with parameters from ML model can be verified upto schematic level.
- The steps followed for creating the tool in this project can be replicated for most analog circuits.
- Once, the user gets the circuit netlist that behaves near to that as required by user/designer, the designer can apply their expertise to make the circuit functionality even perfect.
- This **reduces the design time** of **analog circuits** to be **developed from scratch**.

References

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2. H. C. Yang and D. J. Allstot, "Modified modeling of Miller compensation for two-stage operational amplifiers," 1991., IEEE International Sympoisum on Circuits and Systems, 1991, pp. 2557-2560 vol.5, doi: 10.1109/ISCAS.1991.176049.
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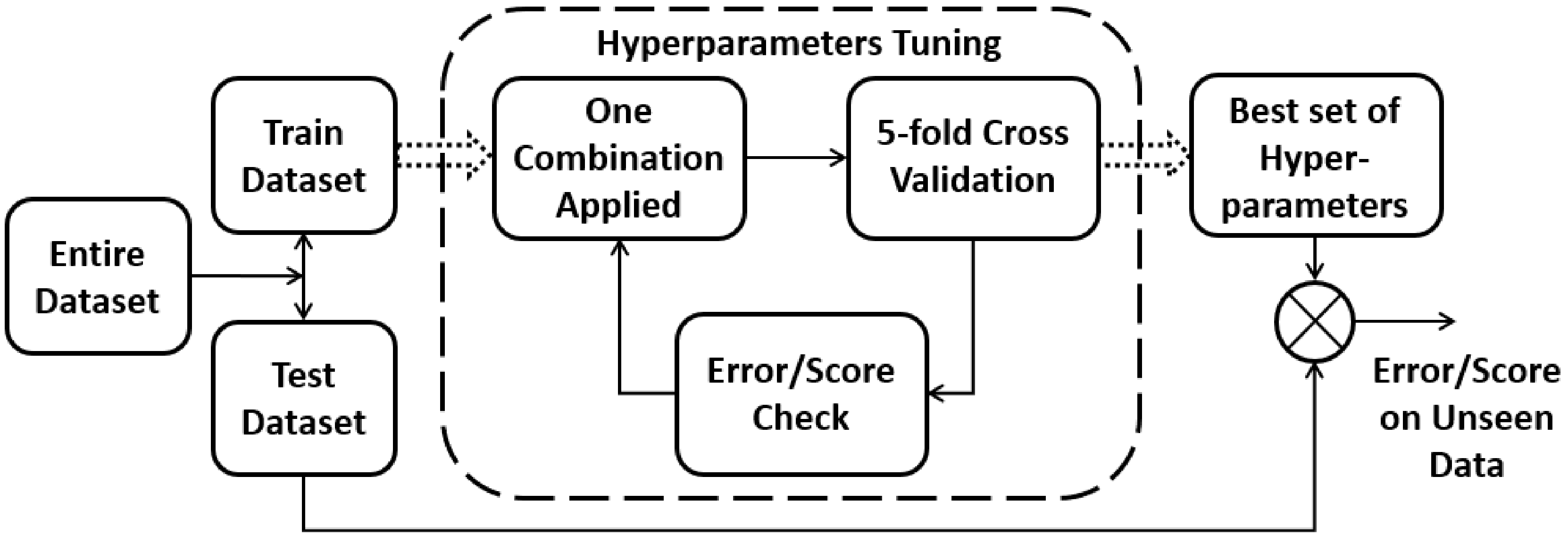
Thank You

Hyper Parameter Tuning and Cross Validation



Results

	Set 1			Set 2			Set 3		
Specifications	**Desired Value**	**Actual Value (Cadence Output)**	**Predicted Value (ML tool Output)**	**Desired Value**	**Actual Value (Cadence Output)**	**Predicted Value (ML tool Output)**	**Desired Value**	**Actual Value (Cadence Output)**	**Predicted Value (ML tool Output)**
DC Gain (dB)	48	50.63	50.19	45	48.53	48.02	50	48.78	48.79
DC Power (mW)	1.5	0.859	0.868	1	0.503	0.432	1.5	1.624	1.575
Slew Rate (V/µs)	200	141.2	133.66	300	214	228	400	271.9	250
UGB (MHz)	250	162	160.93	270	167.9	155.11	500	314.2	318
Phase Margin (º)	65	62.03	62.2	60	52.7	53	65	73.17	78.78
3dB Bandwidth (MHz)	4.55	2.7	3.03	4.91	3.04	3.39	9.10	5.37	5.58
Noise at DC (µV/$\sqrt{Hz}$)	33.32	24.13	29.83	40	21.95	24.55	33.32	45.67	45.57
Noise at DC (nV/$\sqrt{Hz}$)	10	9.232	10.23	12	9.178	10.64	10	10.11	10.4
Noise at DC (nV/$\sqrt{Hz}$)	7.261	8.19	8.79	8.72	7.568	8.43	7.261	7.49	7.78