**Designing Two stage Opamp using 90nm and 180nm technology**

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**Abstract -** In this paper, a two-stage ultra-low-power operational amplifier is designed, and a comparative analysis of the proposed subthreshold complementary amplifier is presented between 180nm and 90nm, CMOS technology. The proposed operational amplifier is compared across several different parameters to determine the optimal design. It achieves a maximum gain of around 65dB with a supply voltage of 0.039 V. The main purpose is to The proposed operational amplifier has been designed using a SPICE-based circuit simulator.

***Key Words*:** CMOS two stage Opamp , gain , bandwidth , low power

**1.INTRODUCTION**

The operational amplifier (Op-amp) is a fundamental and an integrated building block in analog circuit design. Op-amp in general is a 3-terminal device with an inverting input (denoted by “-” sign), a non inverting input(denoted by “+”sign) and an output terminal. The basic principle used in an Op-amp is to have high forward dc gain to implement the negative feedback so that when negative feedback is applied ,the closed loop transfer function of op-amp is independent of its gain. As the transistor channel length and supply voltages are shrinking, the CMOS is becoming a great success among all because it can be easily scaled down to dimensions like micrometer and nanometer. Due to scaling down of channel length more number of transistors can be integrated on a single chip which leads to the need of high operating frequency which can be implemented with the help of CMOS op-amp. Op-amps are linear devices having applications in various scientific devices and is extensively used to perform mathematical operations like addition, subtraction, integration and so on. .Op-amps with two or more stages are widely used to achieve higher gain. One of the most popular Op-amps is a two stage Op-amp which is the aim of this work. This paper represents the work done in a proper sequence. Part I describes the introduction. Part II describes the two stage CMOS op-amp with its working. It also calculates instance, threshold voltages of PMOS and NMOS, slew rate, etc. Part III discusses the AC simulation part where Further in part IV, The D Finally part V concludes the work do

## 2. Two Stage Opamp

A two stage CMOS Op-amp consists of three stages. The first stage is a differential amplifier followed by a gain stage which can be a common source stage and finally followed by an output buffer. The output buffer is used only if the Opamp is to drive large capacitive or/and resistive loads. Op-amps can have different topologies, a two stage CMOS op-amp is one such topology. The two stage CMOS Opamp topology is used where high input impedance and low output impedance is required[3]. Figure 1 below shows the basic configuration of a two stage CMOS Op-amp. Here transistors M1,M2,M3,M4 form the first stage which is the differential gain stage and transistors M6 and M7 form the second stage which is the gain stage. In the first stage, transistor M5 provides the biasing to entire circuit, transistors M1 and M2 form the differential input pair actively loaded by a current mirror pair formed by transistors M3 and M4. In the second stage, transistor M6 is a common source amplifier actively loaded by transistor M7.

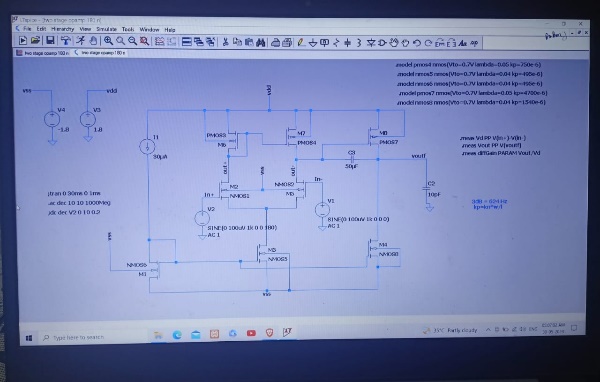
**Specifications of the staged two stage OPAMP**

|  |  |
| --- | --- |
| **Specification Name** | **Values** |
| Supply VDD | **+-**0.039V |
| Phase Margin | **>=**60 degree |
| Slew Rate | 20V/u sec |
| ICMR (+) | 1.6V |
| ICMR (-) | 0.8 V |
| Power Dissipation | **<=**300 watt |
| Gain bandwidth | 30 MHZ |

**3. CONCLUSIONS**

**STIMULATION RESULTS**

1. **Schematic of the Opamp**

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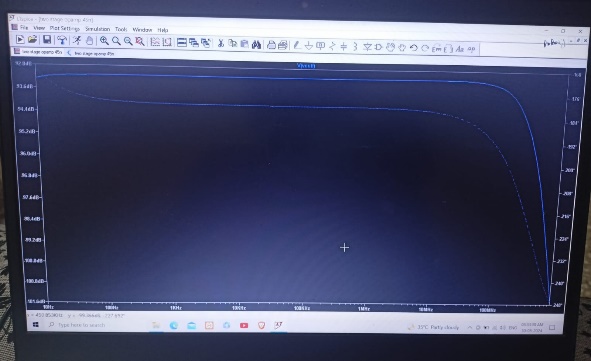
**Schematic Representation of two stage Opamp**

1. **Aspect Ratios Taken for Transistors**

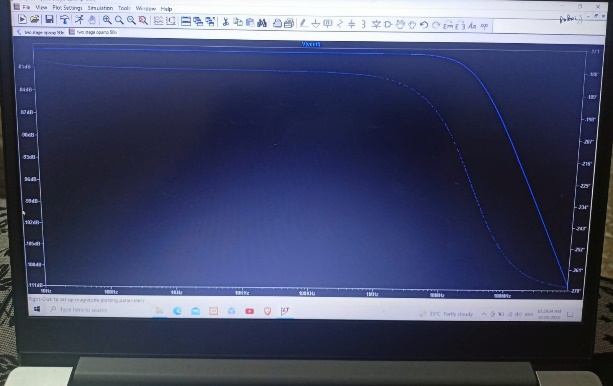
|  |  |
| --- | --- |
| **W/L Ratio** | **Values** |
| W1, W2 | 6 |
| W3, W4 | 14 |
| W5 | 12 |
| W6 | 174 |
| W7 | 75 |

1. **AC ANALYSIS**

**(a)** 180NM Technology

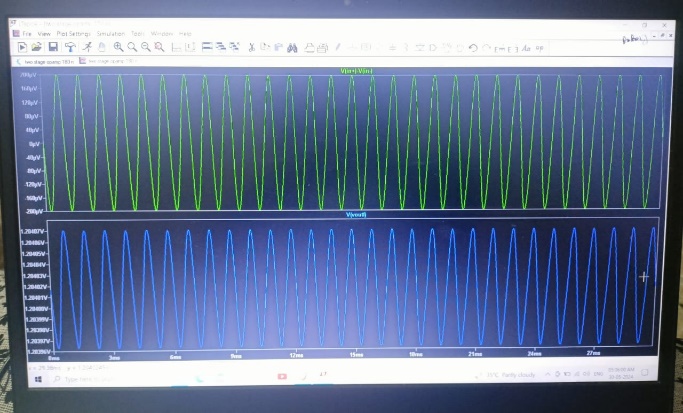


(b) 90 NM TECHNOLOGY 94

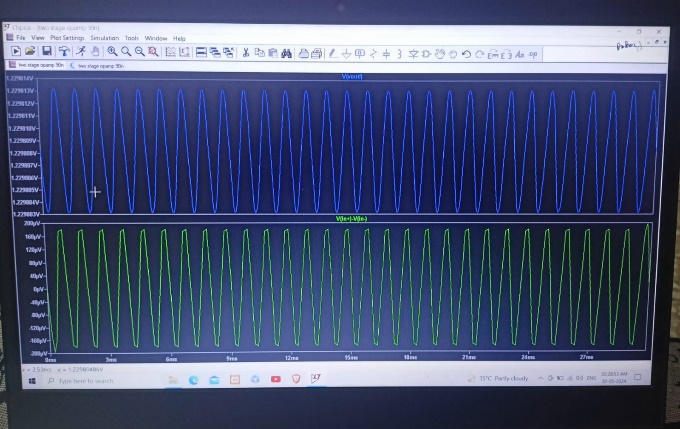


|  |  |  |
| --- | --- | --- |
| **Parameters** | **180nm** | **90nm** |
| **Gain** | 21.25 dB | 22.8 dB |
| **dB** | 5.05 MHZ | 1.51 MHZ |
| **Phase Margin** | 94.02 | 127.6 |

1. **DC ANALYSIS**
2. 180 NM technology

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(b)90 NM Technology

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|  |  |  |
| --- | --- | --- |
| **Parameters** | **180nm** | **90 nm** |
| **Gain** | 20.95dB | 26.2 dB |
| **dB** | 9.78 MHZ | 5.05 MHZ |
| **Phase Margin** | 93.69 | 82.89 |

1. **Conclusion**

Full design and analysis of a two stage CMOS op-amp has been presented in this paper. The result shows that the amplifier design has successfully satisfied all the design specification given in advanced.

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