CSE BUBBLE PROCESSOR

DOCUMENTATION

PDS1:

We have 32 registers, with different registers for different purposes. Here is how we will use them.

Symbolic Name	Number	Usage
zero	0	Constant zero
at	1	Reserved for the assembler
s0-s7	2-9	Saved registers 0…7
t0-t9	10-19	Temporary registers 0…9
v0-v1	20-21	Result registers
a0-a3	22-25	Argument registers 1…4
k0-k1	26-27	Kernel registers 0…1
sp	28	Stack Pointer
ra	29	Return Address
fp	30	Frame pointer
gp	31	Global Data Pointer

PDS2:

The size of instruction and words are 32 bits. We can create a total of 2^9 addresses, out of which first 2^8 addresses will be for instruction memory and the next 2^8 addresses will be for data memory. So our VEDA memory will be a 512×32 size memory.

PDS3:

Here we have our instruction layout for R, I and J type and their encoding methodology. Each instruction is 32 bits.

R TYPE :

32 bit instruction

	6 bit	5 bit	5 bit	5 bit	5 bit	6 bit
INS	**OP CODE**	**RS**	**RT**	**RD**	**SHAMT**	**FUNCT**
add r0,r1,r2	1	r1	r2	r0	0	32
sub r0,r1,r2	1	r1	r2	r0	0	33
addu r0,r1,r2	1	r1	r2	r0	0	34
subu r0,r1,r2	1	r1	r2	r0	0	35
and r0,r1,r2	1	r1	r2	r0	0	36
or r0,r1,r2	1	r1	r2	r0	0	37
slt r0,r1,r2	1	r1	r2	r0	0	38
sll r0,r1,int	1	0	r0	r1	int	40
srl r0,r1,int	1	0	r0	r1	int	41

J TYPE:

32 bit instruction

6 bit 26 bit

Instruction	**OP CODE**	**ADDRESS**
j int	2	int
jr ra	3	ra
jal int	4	int

I TYPE:

32 bit instruction

6 bit 5 bit 5 bit 16 bit

INS	**OP CODE**	**RS**	**RT**	**Immediate**
addi r0,r1,int	11	r0	r1	int
addiu r0,r1,int	12	r0	r1	int
andi r0,r1,int	13	r0	r1	int
ori r0,r1,int	14	r0	r1	int
slti r0,r1,int	15	r0	r1	int
lw r0,r1,int	17	r0	r1	int
sw r0,r1,int	18	r0	r1	int
beq r0,r1,int	19	r0	r1	int
bne r0,r1,int	20	r0	r1	int

bgt r0,r1,int	21	r0	r1	int
bgte r0,r1,int	22	r0	r1	int
ble r0,r1,int	23	r0	r1	int
bleq r0,r1,int	24	r0	r1	int