

ASSIGNMENT

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IITH - Future Wireless Communications (FWC)

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1 Question

1. The circuit shown in the figure below uses ideal positive edge-triggered synchronous J-K flip flops with outputs X and Y. If the initial state of the output is $X=0$ and $Y=0$ just before the arrival of the first clock pulse, the state of the output just before the arrival of the second clock pulse is

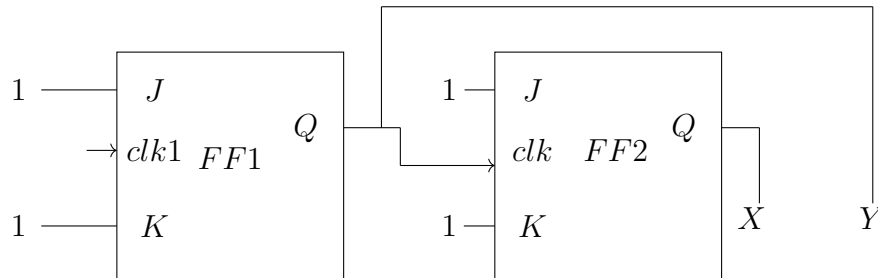


Figure 1

1. $X = 0, Y = 0$
2. $X = 0, Y = 1$
3. $X = 1, Y = 0$
4. $X = 1, Y = 1$

2 Components

| Component | values | Quantity |
|-------------|---------|----------|
| Arduino | UNO | 1 |
| Jumperwires | M-M | 12 |
| Breadboard | | 1 |
| LED | | 2 |
| Resistor | 220ohms | 2 |
| IC | 7476 | 2 |

Figure.a

3 TruthTable

| CLK | J | K | Q | Q' | State |
|-----|---|---|----|----|---------------|
| 1 | 0 | 0 | Q | Q' | No Change |
| 1 | 0 | 1 | 0 | 1 | Resets Q to 0 |
| 1 | 1 | 0 | 1 | 0 | Sets Q to 1 |
| 1 | 1 | 1 | Q' | Q | Toggle |

Truth tabel of JK filp flop

4 Stages

4.1 Stage

1

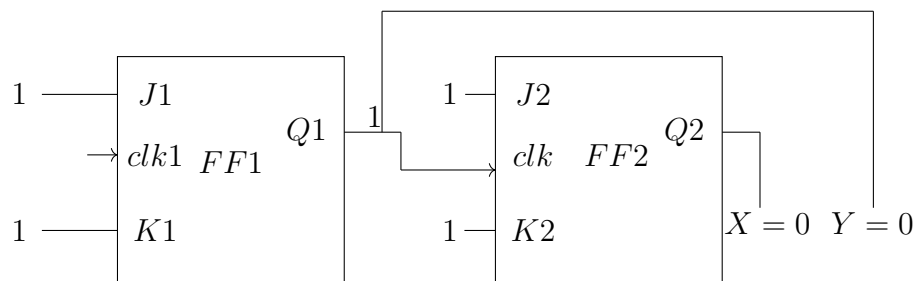


Figure 2

Initially, let $X=0$ and $Y=0$. According to the truth table, when $J=1$ and $K=1$, the circuit enters the toggle condition. Given that the previous value of $Q1$ was 0, toggling it changes $Q1$ to 1, as illustrated in Figure 2.

4.2 stage

2

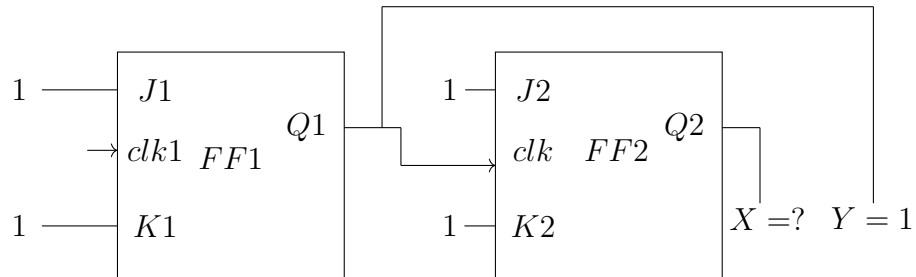


Figure 3

After toggling, the value of Q1 is set to be the same as the output value of Y, which is found to be 1. Therefore, both Q1 and Y are equal to 1 after the toggle operation. This behavior occurs due to the specific input conditions ($j=1$ and $k=1$) applied to the circuit, as shown in Figure 3

4.3 stage

3

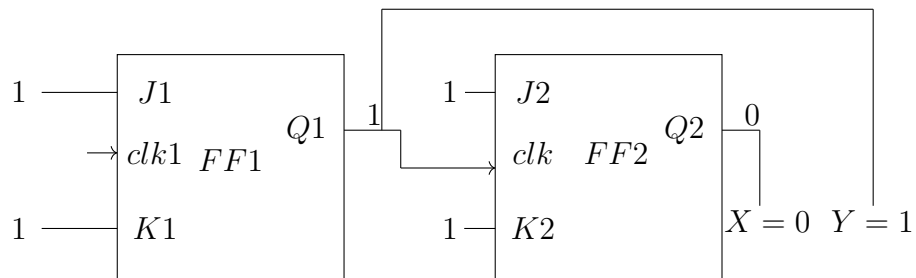


Figure 4

After Q1 and Y are set to 1, the value of X remains 0. At this point, Q1 is connected as the clock input to Flip Flop 2, causing the second Flip Flop to also enter the toggling condition.

4.4 stage

4

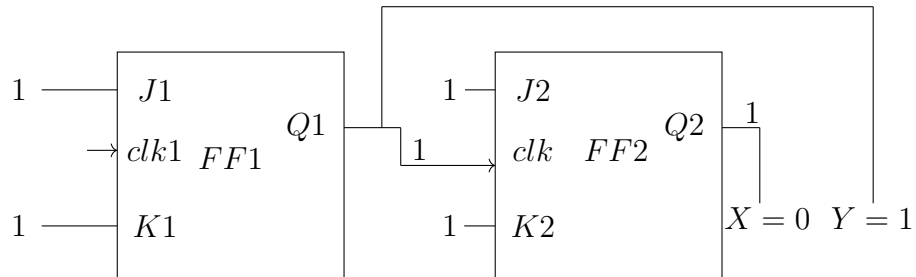


Figure 5

Once Q2 is set to 1, it assumes the same value as X, leading X to automatically become 1 as a result.

4.5 stage

5

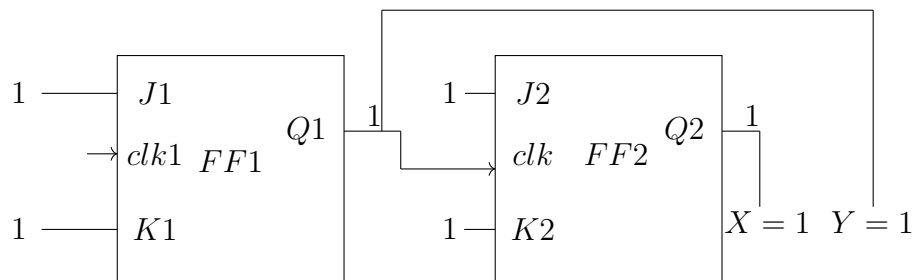
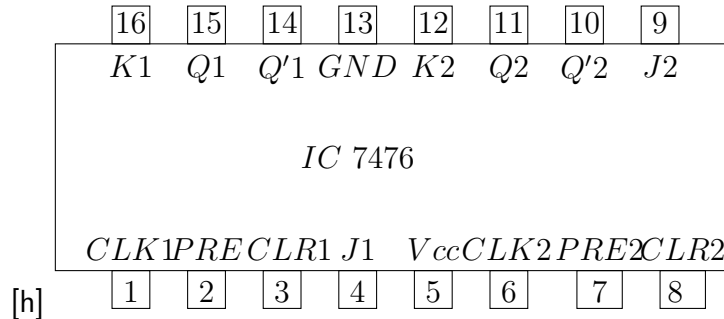


Figure 6

Thus, the output of the second clock pulse is X=1 and Y=1. This outcome arises as a consequence of the toggling process and the synchronization between the flip flops, which ultimately sets both X and Y to a value of 1. Based on the results obtained, it is evident that option (4) is correct. The analysis of the circuit's behavior demonstrates that the values of X and Y are indeed set to 1 after the second clock pulse, which aligns with option (4).

5 Hardware

The 7476 is a master—slave J-K and the 74LS76 is a negative edge-triggered J-K flip-flop. Both chips have the same pin configuration. Below is the pin diagram of IC7476.



6 Implementation

The connections between Arduino UNO and three IC 7476 is given in below Table

| | INPUT | | OUTPUT | CLOCK 1 | clock 2 | Vcc | GND |
|---------|--------|----|--------|---------|---------|-----|-----|
| ARDUINO | D2 | D3 | | 13 | | 5V | Gnd |
| 7476 | 16,2,3 | | 15 | 1 | 15 | 5 | 13 |
| 7476 | | 16 | 15 | | 1 | 5 | 13 |

Table 1: connections

7 Procedure

- 1.Connect the circuit as per the above table.
- 2.connect the output pins to the LED's
- 3.Connect inputs to Vcc for logic 1,ground for logic 0
- 4.Execute the circuit using the below code.

<https://github.com/Goutham-patel/FWC/blob/main/ide/codes/src/ln201912.cpp>