Low Complexity SDR Transceiver Design using Simulink, Matlab and Xilinx

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***Abstract*—The revolution of modern radio communication application such as radar, electronic warfare and signal intelligence using SDR technology has open an interest among researchers to adopt the technology in wireless communication system. This paper is focused on mechanisms and methodology to implement a low complexity SDR transceiver using Simulink, Matlab and Xilinx for FPGA environment. In this design, a spectrum frequency between 5 MHz to 20 MHz is sampled using QPSK modulation technique to achieve encoding and decoding of IF signal. The mechanisms and methodology of proposed transceiver design would help in SDR designing by providing a fast way altering a system with low complexity. It also opens the possibility of integrating cognitive radio aspect into wireless networks such as 3G and 4G in the future.**

***Keywords*—Software Defined Radio (SDR), Field Programmable Gate Array (FPGA), Intermediate Frequency (IF), Quadrature Phase-Shift Keying (QPSK).**

I. INTRODUCTION

Wireless communications have developed rapidly due to multiple purpose and demand of cellular network application. The cellular communication growth proved that wireless communication is viable for voice and data services. Traditional wireless devices are designed to deliver a single communication service using a particular standard. With the steady increase of new wireless services and standards, single purpose devices with dedicated hardware resources can no longer meet the user need [1]. It is also expensive to upgrade and maintain a wireless system each time a new standard comes into existence.

The ideal concept of a software defined radio (SDR) system is a radio communication system that can tune to any frequency band and receive any modulation across a large frequency spectrum using a programmable hardware controlled by software [1][3]. In this paper, a low complexity SDR implementation is proposed using Simulink, Matlab and Xilinx environment based on FPGA. Simulink and Matlab is used to produce random spectrum signal while, Xilinx is used as a platform-based as an approach to FPGA design. This paper is organized as follows. A Sections II introduces the SDR design. While Section III introduces the SDR proposed design. Section IV explains the methodology of the transceiver. Section V explains the experimental result and discussion. Section VI explains the conclusion of the result.

II. IDEAL SDR DESIGN

Software defined radio (SDR) is designed to support communication network in battle situation and security purposes for military. SDR capability to serve a variety of changing radio protocol and flexibility in the real time has made SDR as a cutting edge to modern radio technology implementation [3]. Recently, SDR is used to substitute the conventional radio for commercial and emerging purposes. An ideal SDR consists of a superheterodyne radio frequency (RF) front end to convert RF signal to analog IF signal which is commonly used in conventional radio. The IF section is made up of analog to digital converter (ADC) and digital to analog converter (DAC) which is used to convert digitized IF signal from analog form, as shown in Figure 1. The signal is transferred through channelization and sample rate conversion as an ADC interface to the processing hardware at the receiver part [4]. The real time SDR can be implemented by using base band processing with variety of digital hardware such as field programmable gate array (FPGA), digital signal processing (DSP), application specific integrated circuit (ASICs) and general purpose processors (GPP).

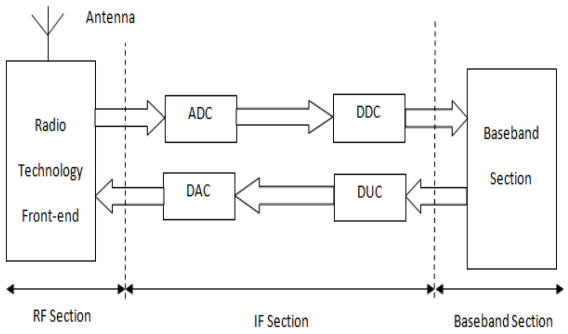

Figure 1: Function Block Diagram of Wireless Communication System

This digital hardware is chosen due to its flexibility, high processing speed and low power consumption. However, there is a tradeoff between maximum flexibility with high power consumption of DSP to minimum flexibility and low power consumption of ASICs. FPGA offered a good hardware optimization with reliable design, lower cost and low power consumption as compared to DSP and ASICs. FPGA flexibility and reconfigurable features made it ideal for prototyping and testing for SDR design [5].

III. THE PROPOSED SDR DESIGN

The proposed design block diagram is illustrated as in Figure 2. The proposed SDR design is implemented according to ideal SDR design. The proposed SDR design is realized using Simulink, Matlab and Xilinx design environment. The design is modeled in Simulink environment with Xilinx System Generator [5]. The DSP building blocks are provided in Xilinx DSP Blockset in the Simulink Library Browser as shown in Figure 3. The combinations of this device component made the designing process easy and more flexible as its function concurrently. The proposed SDR design simulations parameters are as shown in Table 1.

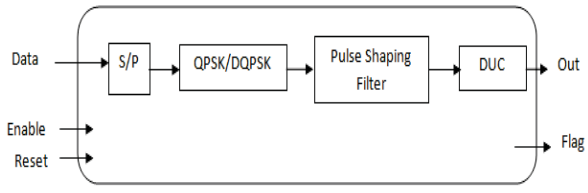

Figure 2: Proposed Transmitter Block Diagram

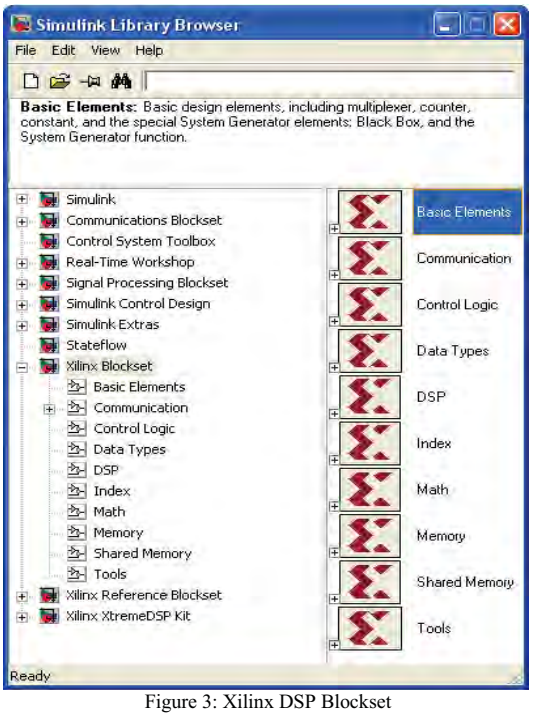

Figure 3: Xilinx DSP Blockset

TABLE 1.
SIMULATION PARAMETERS FOR SDR PROPOSED DESIGN

Type of transmission	Single rate transmission
Modulation type	QPSK
Random Spectrum Frequency	5 MHz
Receiver Sampling Rate	20 MHZ

IV. METHODOLOGY

Simulation and testing process were done using System Generator tool. The proposed design is modeled in Simulink environment using Simulink Blockset, Xilinx Blockset and Matlab Mcode coding [6]. It is divided into two sections; the transmitter and receiver. The System Generator random binary signal is setup at 10 MHz with 100ns. The designed transmitter received 8 bits word format. The received bits are broken down into 4 bits word format which act as an input to the transceiver. The process is done using a linear feedback shift register (LFSR). It generates continuously random binary step from random signal generator before it is fed into serial to parallel blockset. Serial to parallel blockset is used to represent the signal in parallel form and fed it into QPSK modulator [7][8] as in Figure 4. The QPSK modulation technique needs two bits to perform one symbol.

The encoding process required data of i and j to be scaled down by 1/sqrt(2) since there is a possibility that the coordinate of 00 changes to 11 that could caused i and j polarity to change at the same time. Besides that, the power required during transmission need to be normalized to 1 Watt. The QPSK modulator encoding process of real (phase) and imaginary (quadrature) data is tabulated as in Table 2. The proposed QPSK modulator is modeled according to Table 2 using as in Figure 5.

TABLE 2.
QPSK MODULATOR DESIGN

Data	Quadrant	Real and Imaginary
00	1st quadrant	i + j
01	2nd quadrant	-i + j
11	3rd quadrant	i - j
10	4th quadrant	- i - j

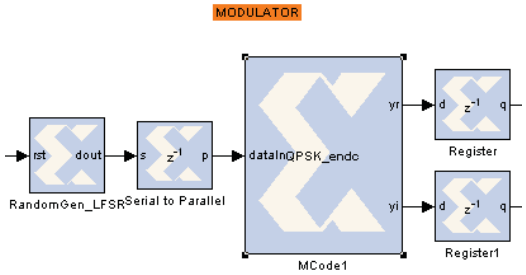

Figure 5: QPSK Modulator

The original spectrum is upsampled by 2 to maintain the spectrum frequency at 5 MHz to 20 MHz. The pulse shaping is implemented with raised root cosine (RRC) filter (FIR) using filter design and analysis (FDA) tool in Figure 6. The raised root cosine filter limits the spectral occupancy efficiency and removes adjacent channel interference. It also allowed an approximation of minimum Nyquist bandwidth with excellent band suppression [8][9]. The FDA Tool gave an advantage to estimate the cut off frequency and roll off values to achieve desirable response [10]. RRC filter is designed to attenuate the second sample with cutoff frequency, ω_c = 0.25 to obtain harmonic at 30 dB or more.

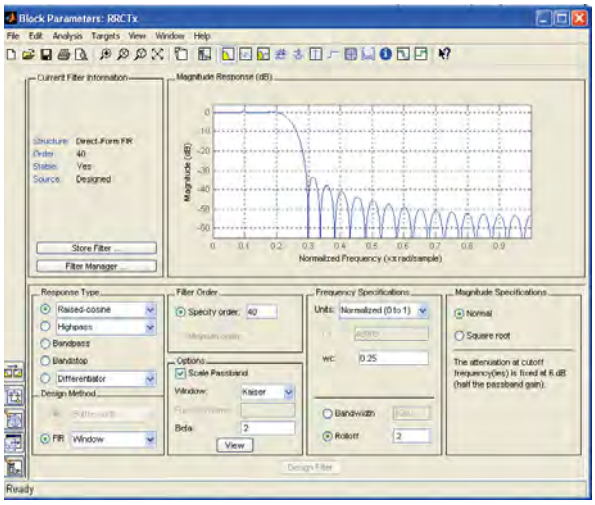

Figure 6: FDA Tool for RRC Design

Digital Up Conversion (DUC) and Digital Down Conversion (DDC) of the transceiver is used as a mixer to shift the sinusoidal and cosine signal of I and Q into 90°. The mixer must have a different polarity for the cosine oscillation on either up conversion or down conversion [11]. The DUC properties are important to obtain desired RF frequency at the transmitter. A similar polarity on the cosine oscillation of sinusoidal signal at DUC will result receiver signal to be sign inverted [12].

The produced IF from the transmitter is feed back into receiver system as an input to DDC subsystem [13] in Figure 7. The DDS is set to match the sampling rate of transmitter baseband and maintained an output oscillation at 5 MHz with 20 MHz sampling rate. The received signal is down sampled using the same RRC filter to obtain attenuation at between 50-60 dB.

VI. Result And Discussion

Figure 8 shows modulated I and Q mapping using QPSK modulation. From the observation, it shows that QPSK rate is two times slower than the binary. This is because in QPSK modulation technique, it needs two bits to transmit one symbol.

Then, these signals are filtered after being upsampled at transmitter baseband stage. The observation in Figure 9 shows, the original 5 MHz baseband spectrum maintained in 20 MHz spectrum domain.

In Figure 10, the different between IF and harmonic spectrum produced in DUC is about 30-40 dB. The attenuation range is still acceptable since the transmitter is designed for single rate transmission. Transmitter spectrum is produced after the signal is fed into the mixer. This process maintained the IF signal at 5 MHz and 15 MHz as in Figure 11 to achieve 20 MHz of receiver sampling rate. The 5 MHz IF signal replica is at 15 MHz and the harmonic is continued from 0, 10 untill 20 MHz in the spectrum. Figure 12 shows the IF signal produced by the designed transmitter.

The received spectrum in Figure 13 shows the cutoff frequency is maintained at 0.25 MHz and down sampling signal in Figure 14. From the observation, the attenuation range for the transceiver occurred between 50-60 dB. Figure 15 shows modulated IF signal mapped using QPSK modulator transmitter at the receiver. The transceiver design down sampled signal is valid after 56 samples at 10 MHz. These are included the 28 samples transmitted and 28 samples received.

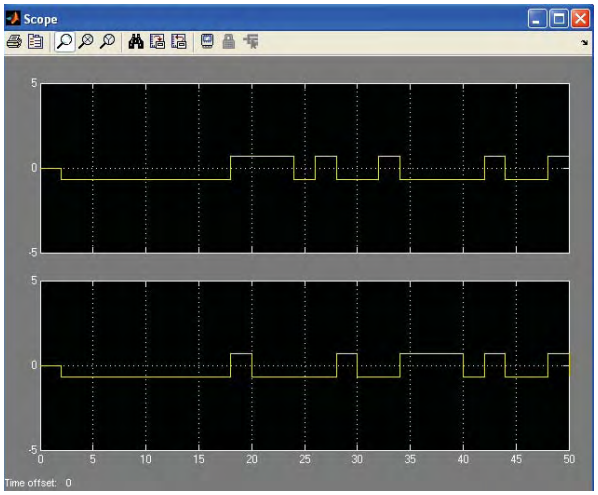

Figure 8: Modulated I and Q mapping

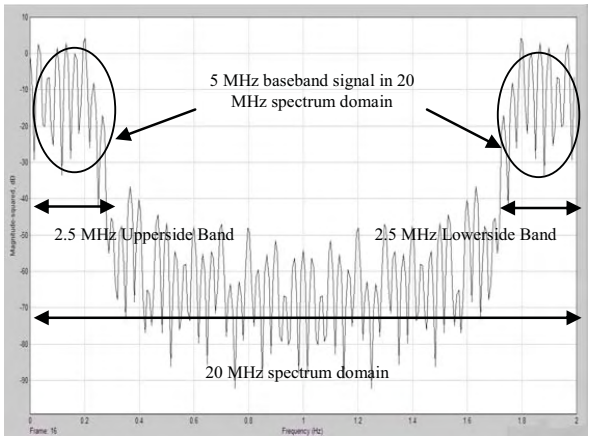

Figure 9: Transmitter Baseband Spectrum after Filtered

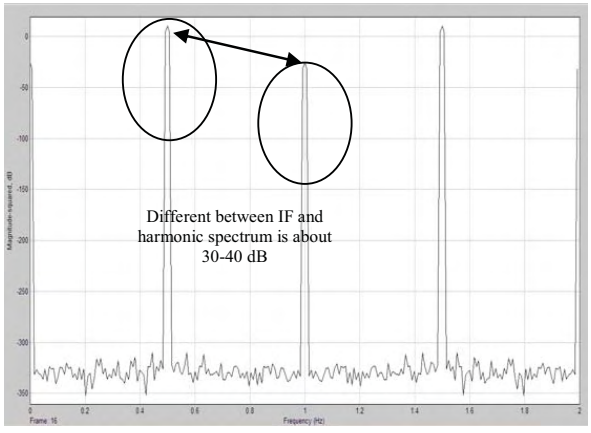

Figure 10: DUC Spectrum

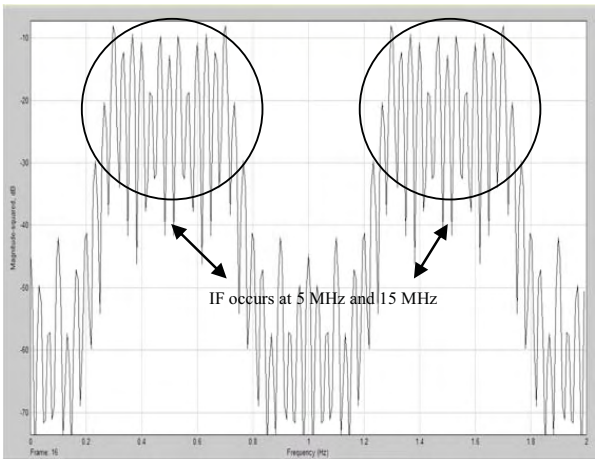

Figure 11: Transmitter Spectrum

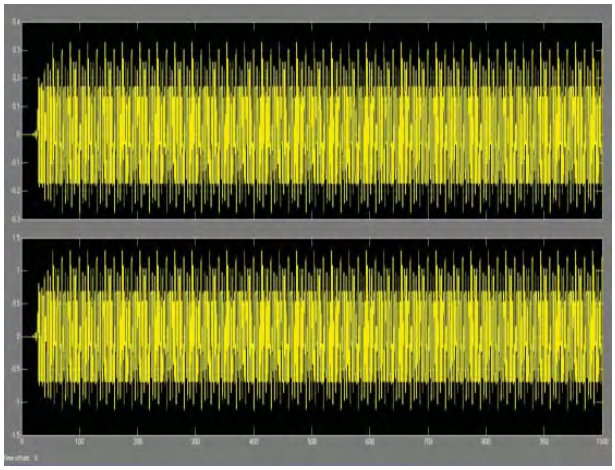

Figure 12: IF Signal at Transmitter

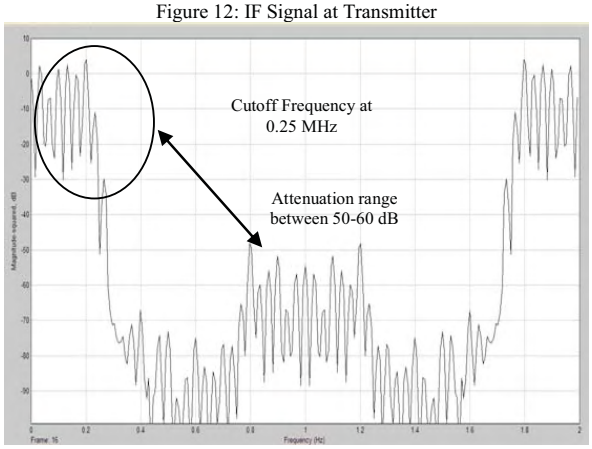

Figure 13: Receiver Spectrum

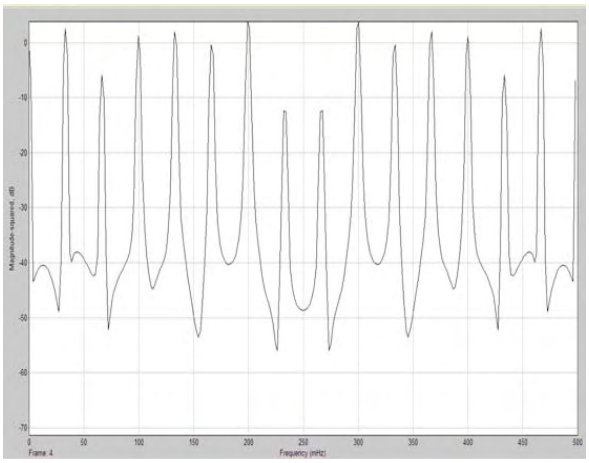

Figure 14: Down sampling spectrum

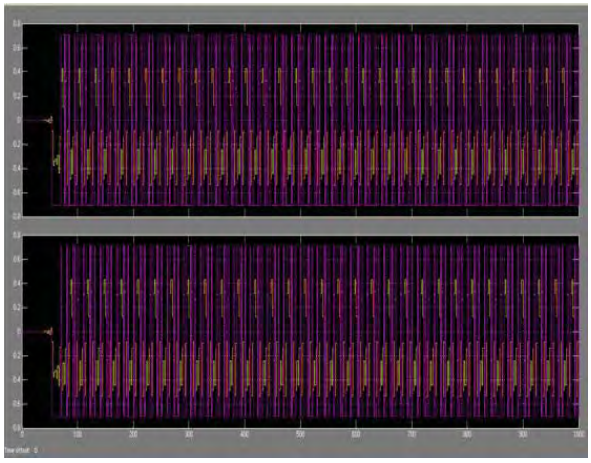

Figure 15: Receiver Output Signal

VII. CONCLUSION

In this paper a low complexity SDR design is present. The proposed design achieved the objective and proved it can easily implement using Simulink and Xilinx DSP Blockset. This design approach gave an advantage to designer either to use Matlab, Verilog or HDL. It also allows designer to identify problems and providing a fast way of altering a system. Hence, it opens the possibility of integrating cognitive radio into wireless network. The proposed design is recommended to be implemented using FPGA for further processing.

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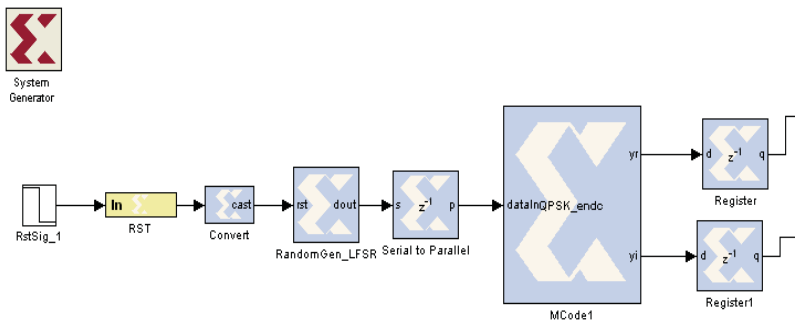

Figure 4: Proposed Transmitter Design

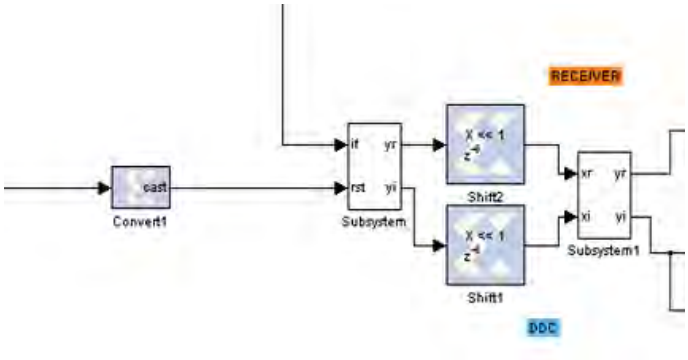

Figure 7: Proposed Receiver Design