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Design and Implementation of a novel QPSK demodulator for FPGA based system design

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***Abstract* − Quadrature Phase Shift Keying (QPSK) is used in various applications such as GSM, LTE, WLAN, mobile WiMAX, CDMA, Cable TV and satellite communication. Design and implementation of QPSK modulator and demodulator for FPGA based systems is proposed in this work. A novel comparator based method is employed for QPSK demodulation and the hardware implementation of the modules on a Zynq 7000 FPGA based ZED board is carried out using the concepts of model based design.**

Keywords – FPGA; QPSK; Comparators; Model based programming; Modulation; Demodulation.

I. INTRODUCTION

Quadrature Phase Shift Keying (QPSK) is a digital modulation technique, wherein two binary bits are modulated at once, selecting one of four possible carrier phase shifts (0º, 90º, 180º or 270º). QPSK possesses very good noise immunity, low error probability and bandwidth required is half of that required for BPSK with same bit error rate, thus yielding higher information transmission rate for QPSK. QPSK scheme is employed for various applications such as GSM, LTE, WLAN, mobile WiMAX, IEEE 802.11b Wi-Fi phone, CDMA, Cable TV, satellite communication and many more.

Design of building blocks for QPSK modulator using PIC microcontrollers is proposed in [1], QPSK modulator using TMS320C6711 digital signal processor in [2], QPSK modulator and demodulator using CEVA-XC321 digital signal processor is proposed in [3] and using TMS320C6713 digital signal processor in [4]. FPGAs provide powerful computational architectural features such as DSP blocks, Block RAMs, programmable logic elements, embedded multipliers etc., with higher level of flexibility, which has made FPGAs evolve as an increasingly common platform for various applications. Lot of research is in progress towards FPGA implementation of QPSK modulator/demodulator such as design of QPSK modulator using VHDL, using reconfigurable architecture, design of QPSK modem using Verilog, using System Generator and using Modelsim with Costas loop being the most commonly used demodulation scheme.

In this paper, design and implementation of QPSK modulator and demodulator for FPGAs is proposed, using model based programming. A simple and novel QPSK demodulation scheme using comparators is proposed in this work. Section II explains the proposed QPSK demodulation scheme and its hardware implementation using model based programming is explained in Section III. The experimental results are discussed in Section IV, followed by conclusion and references.

II. PROPOSED QPSK DEMODULATION SCHEME

The block diagram of QPSK modulator is shown in Fig. 1. Consider an input message sequence m(t) as shown in Fig. 2. QPSK modulation scheme first splits the input message sequence into in−phase and quadrature−phase components, $m_I(t)$ and $m_Q(t)$ respectively as shown in Fig. 2. $m_I(t)$ and $m_Q(t)$ signals are multiplied with $\sin(\omega_c t)$ and $\cos(\omega_c t)$ signals respectively and their sum yields QPSK modulated signal as shown in Fig. 2. The final QPSK modulated signal is given as

$$S(t) = y_{QPSK}(t) = S_I(t) + S_Q(t) \quad (1)$$

where $S_I(t) = \begin{cases} A\sin\omega_c t & if\ m_I(t) = 1 \\ -A\sin\omega_c t & if\ m_I(t) = 0 \end{cases}$ and

$$S_Q(t) = \begin{cases} A\cos\omega_c t & if\ m_Q(t) = 1 \\ -A\cos\omega_c t & if\ m_Q(t) = 0 \end{cases}$$

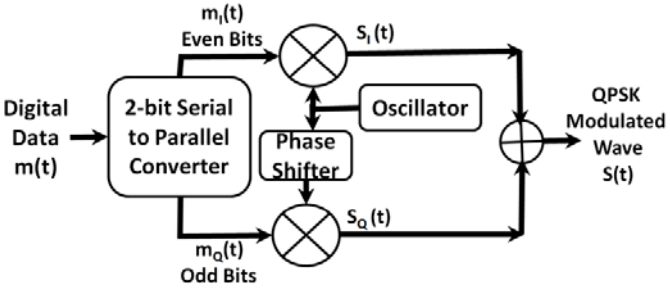

Fig. 1. Block diagram of QPSK Modulator

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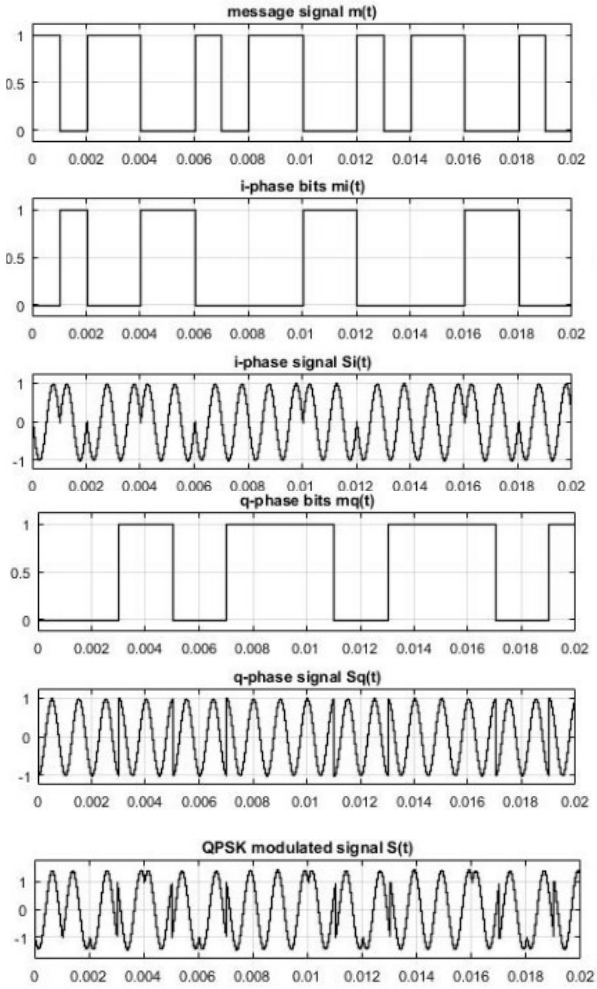

Fig. 2. QPSK Modulation Scheme

The block diagram of proposed QPSK demodulation scheme using comparators is shown in Fig. 3. The QPSK modulated signal along with its delayed or time shifted input is fed to an adder, as shown in Fig. 4. The QPSK signal should be delayed by δ, such that $\omega_c\delta = \pi$ for best results. The output signal from adder is fed to four comparators in parallel to detect the only positive component, only negative component, positive to negative component and negative to positive component, as shown in Fig. 5. These comparator outputs are used to find the in−phase and quadrature−phase components i.e., $m_I(t)$ and $m_Q(t)$ respectively, as shown in Fig. 5. A parallel to serial converter is used to obtain the original sequence m(t) from $m_I(t)$ and $m_Q(t)$ obtained from previous block, as shown in Fig. 6. It may be observed from Fig. 6 that the output sequence is obtained from 8ms onwards and the m(t) matches with the input in Fig. 2.

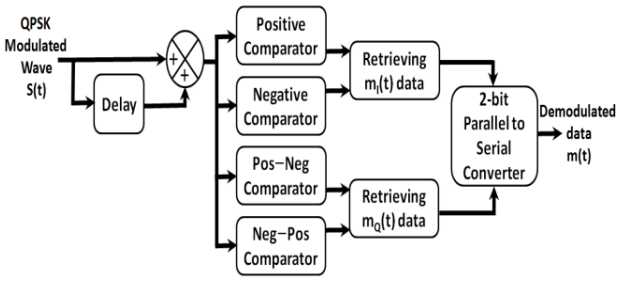

Fig. 3. Block diagram of proposed QPSK Demodulator

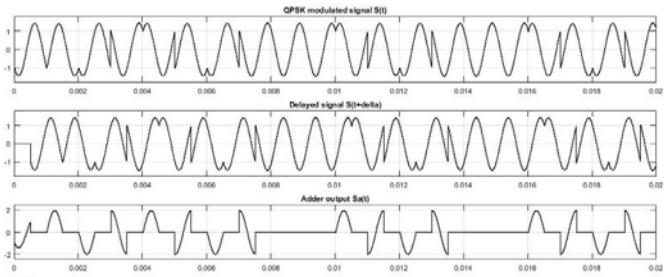

Fig. 4. Adder output of proposed QPSK Demodulator

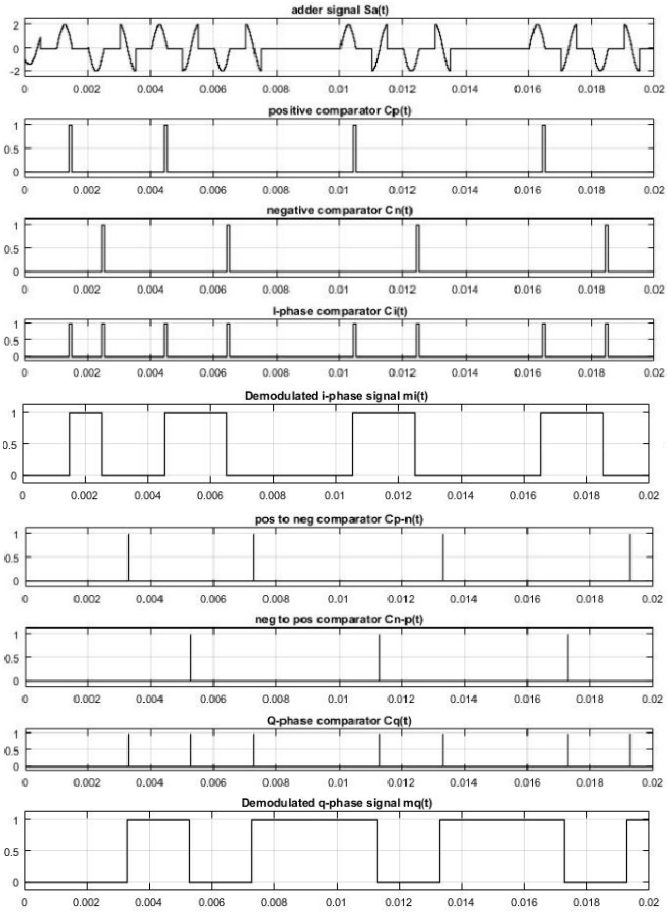

Fig. 5. I-phase and Q-phase comparator output of proposed QPSK demodulator

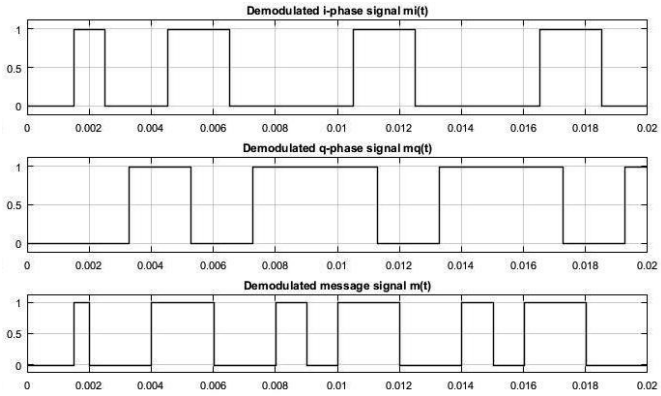

Fig. 6. Retrieval of original sequence m(t) from proposed QPSK Demodulator

III. Hardware Implementation of QPSK Modulator and Demodulator

The model designed for FPGA implementation of QPSK modulator, based on the block diagram shown in Fig. 1, is shown in Fig. 7. Model based programming using Xilinx System Genertator and DSP blocksets is employed for the proposed work. The $S_I(t)$ and $S_Q(t)$ signals obtained from these modules are added to generate QPSK modulated signals.

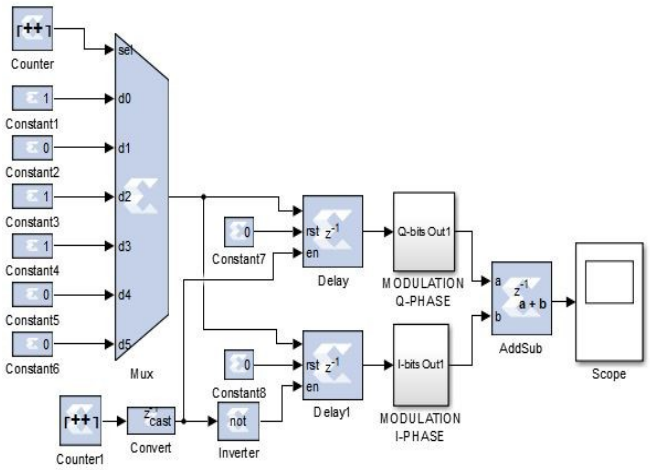

Fig. 7. Model based design of QPSK modulator

The QPSK modulated signals generated from the QPSK modulator designed is fed to the QPSK demodulator to evaluate the performance of the proposed demodulation scheme. The model based design for FPGA implementation of proposed QPSK demodulator, based on the block diagram explained in Section II is shown in Fig. 8. Most of the modules including comparators, $m_I(t)$, $m_Q(t)$ and m(t) signal generation in the design are customized using Mcode blocks.

IV. Experimental Results

The hardware setup employed to assess the performance evaluation of proposed QPSK demodulation scheme is shown in Fig. 9. QPSK modulated signals are connected to a Digital-to-Analog Converter (DAC) module and then monitored on an oscilloscope. Digital outputs are monitored directly from the general purpose input-output (GPIO) pins of FPGA board. All the intermediate signals of the QPSK modulator and proposed demodulator are also captured on the oscilloscope from the hardware. It may be noted that the simulation results of proposed work is reported in Fig. 2 – Fig. 6. The waveform captured from hardware implementation of QPSK modulator is shown in Fig. 10, wherein m(t), $m_I(t)$, $m_Q(t)$ and QPSK modulated waves are observed. The waveforms captured from hardware implementation of proposed QPSK demodulator along with intermediate signals are shown in Fig. 11−Fig. 15. It may be observed that the hardware results matched with the simulation results.

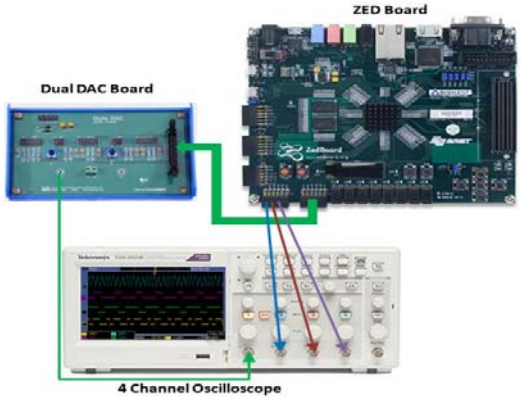

Fig. 9. Hardware setup employed to test the proposed hardware implementation

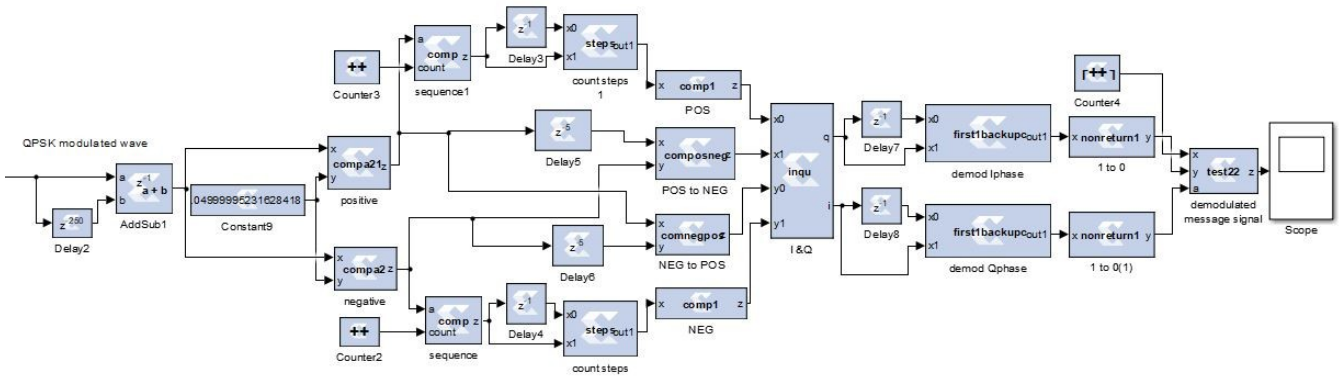

Fig. 8. Model based design of proposed QPSK demodulator

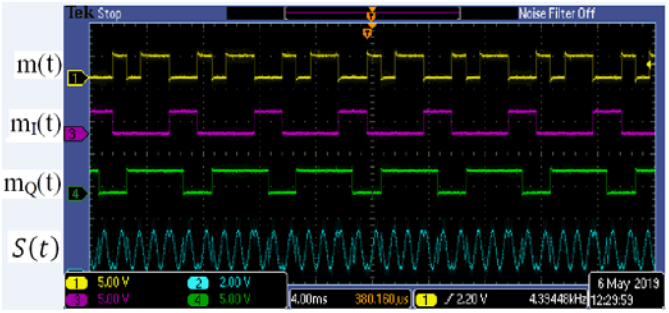

Fig. 10. Waveforms captured on oscilloscope for QPSK modulator

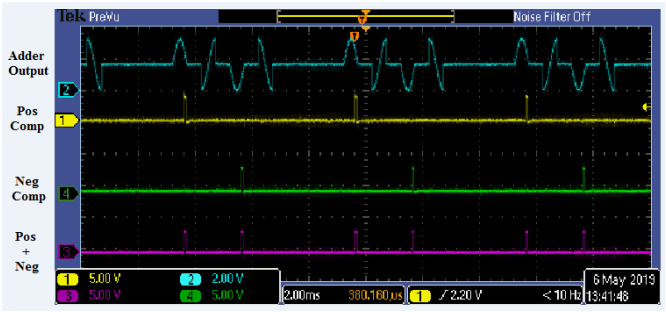

Fig. 11. I-phase Comparator outputs of proposed QPSK demodulator

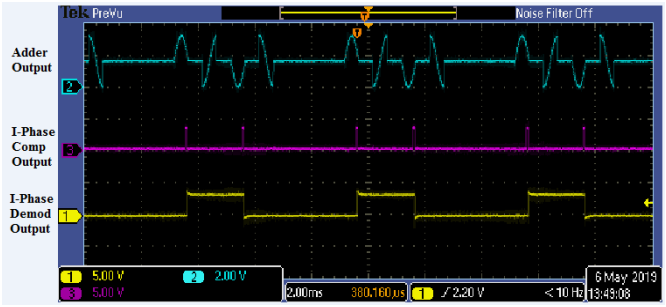

Fig. 12. I-phase demodulation output of proposed QPSK demodulator

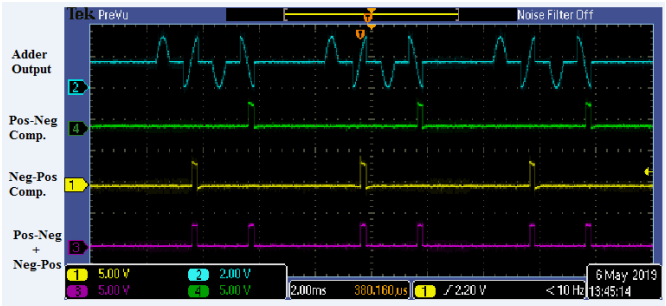

Fig. 13. Q-phase Comparator outputs of proposed QPSK demodulator

Details about the hardware resources utilized by the proposed model based design of QPSK modulator and novel QPSK demodulator on a Zynq 7000 FPGA are reported in Table I.

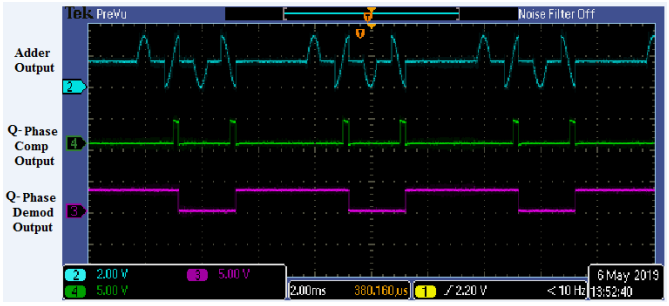

Fig. 14. Q-phase demodulation output of proposed QPSK demodulator

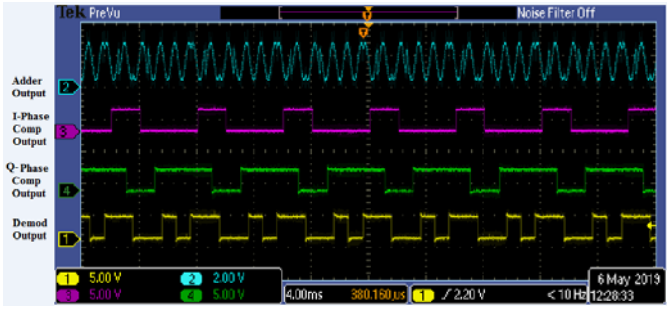

Fig. 15. Waveforms captured on oscilloscope for QPSK demodulator

TABLE I. HARDWARE RESOURCES UTILIZED BY PROPOSED DESIGN

Resource Type	Available	Resources Utilized	
		QPSK Modulator	QPSK Demodulator
LUT	53200	359	237
LUTRAM	17400	0	138
FF	106400	259	231
BRAM	140	60	0
DSP	220	1	0
IO	200	10	18
BUFG	32	1	1

V. CONCLUSION

In this paper, a novel QPSK demodulation scheme using comparators is proposed and is also implemented on a Zynq7000 FPGA based ZED board to assess its performance on hardware. The performance of the proposed QPSK demodulator is in par with the simulation results obtained and performed satisfactorily on hardware too.

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