A Quick Algorithm Implementation Method for ARM-FPGA Integrated SDR Platform

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***Abstract*—A new design method for radio communication algorithm verification is presented in this paper. When developing communication algorithm on Field-Programmable Gate Array (FPGA) based Software Defined Radio (SDR) system, traditional steps include the algorithm simulation, FPGA synthesis and implementations, hardware validation and iterative adjustment. In general, the algorithm simulation step is entirely isolated with hardware environment. More pressures are added on hardware debug process and this will lead to a longer production period. New generation of FPGA products consists of both ARM hard cores and FPGA arrays. Due to its existence of ARM core, data acquiring system is easy to be built. When developing algorithm and optimizing parameters, data could be obtained directly from hardware and be simulated on computer in real time. The algorithm could be directly verified on hardware environment without building FPGA model. Therefore, algorithm developing process could be accelerated.**

Keywords—FPGA, ARM, embedded system, Software Defined Radio, Quadrature Phase Shift Keying

I. INTRODUCTION

With the development of integration technology, increasing number of FPGA products comprise General Purpose Processors (GPP) blocks [1]. Embedded system based on traditional GPP chips could be easily migrated to these new products. Recently, research of the novel combinational system has gradually become a research hotspot [2]. On the other hand, some uncertain issues of front-end radio frequency blocks, such as the in-band spurious, and local oscillator (LO) jitter will cause unavoidable iterative adjustment and increase FPGA validation period [3]. Clock harmonics and signal intermodulation problems is predicted to be worse in the age of 5G [4]. Harsher hardware environment and shorter products development period pose a greater challenge to SDR system development.

New structure of ARM-FPGA combinational system provide potential solutions to this problem. Previous studies proved that arithmetic level simulations is quicker and more efficient comparing with direct lower level implementations [5, 6]. However, soft processors [6] or AISC [5] are either low speed or not suitable for a compact package. In this paper, ARM based hardware/software co-simulation method is used. Data streaming model is presented to be valid to conduct software algorithm validation in hardware when developing communication algorithm and optimizing parameters. In such design flow, data is acquired from hardware in real time, and algorithm processing output could be obtained immediately in computer environment. Parameters changes could be directly applied to be verified on hardware environment without conducting FPGA related operations. A Quadrature Phase Shift Keying (QPSK) development example is presented in this paper.

This paper is arranged as follows. Section II describes the application steps of my methods. Section III concerns an example of QPSK modulator and demodulator development on XILINX ZC702 platform and an AD9361 based radio frequency (RF) front-end board. The conclusion is made in section IV.

II. METHOD DESCRIPTION

As depicted in Fig.1, at the beginning of SDR algorithm development, conventional arithmetic level of algorithm development is conducted in entire software environment. FPGA developments follows software simulations. Hardware verifications would not begin, until all these procedures finished. When iterative adjustment need to be done, FPGA synthesis and implementation are unavoidable to be repeated. So the motivation of the new method is to verify algorithm on hardware platform earlier. In addition to the motivation, due to the application of ARM core, data streaming software is easy to be built. Some provider even provide low level data streaming drivers. In this paper, the Analog Devices, Inc. (ADI) libiio driver library is used.

The new method is to insert one step to bridge the gap between software simulations and hardware implementation. As depicted in Fig.1.b, at first, a communication algorithm model on pure software environment on computer is built. And then, data streaming SIMULINK model can be used to verify algorithm on hardware platform. After that, FPGA models are built when algorithm parameters optimization is finished. Finally, FPGA design validation could be conducted.

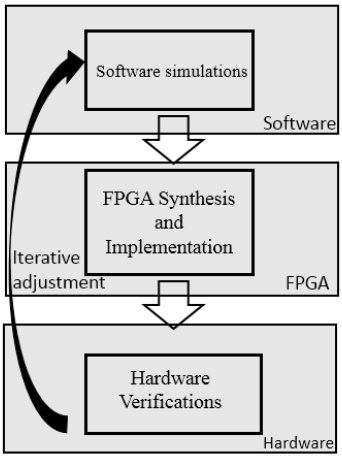

Fig.1.a Conventional SDR communication algorithm design flow

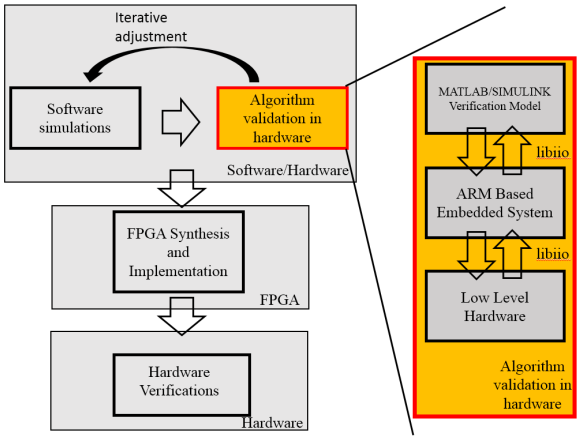

Fig.1.b The new SDR communication algorithm design flow.

III. VERIFICATION MODEL EXAMPLE

As an example, a QPSK modulator and demodulator design model is built. It has been successfully verified on previously mentioned SDR system.

A. Hardware platform

The SDR system consists of a XILINX ZC702 evaluation kit[7] and one AD9361[8] based transceiver board. XILINX ZYNQ-7000 series all programmable Soc is utilized on the XILINX ZC702 board. ZYNQ-7000 Soc features the integration of dual-core ARM Cortex-A9 MPCore based processing system (PS) and programmable logic (PL). Embedded system could be built upon PS part, and the communication algorithms could be built upon PL part. AD9361 is a high performance Agile Transceiver Soc. A RF board working at 4.8GHz~5GHz was designed using on it. These two boards are connected via one pair of FPGA Mezzanine Card (FMC) slots. Passive crystal oscillator is used on this board to produce local oscillator (LO) which may introduce large frequency drift. Therefore, carrier offset compensation algorithm should be carefully considered. The overall system structure is depicted as Fig.2. shows.

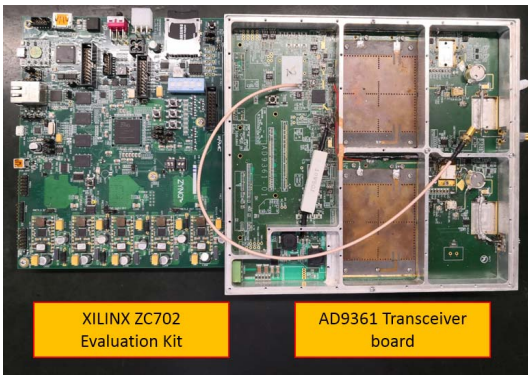

Fig.2. The SDR platform consists of one XILINX ZC702 evaluation board and one AD9361 transceiver board.

B. Algorithm parameter optimization

The proposed QPSK modulator includes baseband modulation, pulse shaping and digital up conversion blocks. Demodulation algorithm should be able to be used to address some practical issues in wireless communications, for instance, carrier frequency and phase offset compensation and timing synchronization. Phase-locked loop (PLL) structure could be used to implement carrier frequency offset compensation[9]. Two parameters, including equalized noise bandwidth B_n and damping factor ζ, should be optimized to obtain better compensation results. B_n influences acquisition time as indicated by Eq.1, where Δf is frequency offset, and T_{FL} is frequency lock time. Meanwhile tracking lock error could be denoted as Eq.2, where N_0 denoted as white Gaussian noise power density with input power of P_{in}. ζ influences PLL stability.

$$T_{FL} \approx 4\frac{(\Delta f)^2}{B_n^3} \quad (1)$$

$$\sigma_{\theta_e}^2 = \frac{N_0 B_n}{P_{in}} \quad (2)$$

Observing above equations, when using bigger B_n shorter acquisition time but also larger phase lock error would be introduced, while smaller B_n bring the opposite problems. Hence, trade should be made to obtain quicker acquisition and lower lock error depending on carrier oscillator offset and drift characters. Absolute frequency offset is easy to model, but LO jitter varies with time. So hardware validation is needed to ensure algorithm effectiveness.

Algorithm is first modeled in MATLAB environment. In this step, data is modulated and demodulated in baseband. After this step, software and hardware cross validation could be conducted. In this paper, baseband modulator and demodulator unit are divided to provide transceiver output and input.

Message data is modulated on computer and connected to XILINX ZC702 platform with MATLAB system object and low-level data link drivers. It should be noted that low level drivers have been provided by ADI. So MATLAB model need to be constructed. Receiving baseband data also could be obtained by another system object model. Carrier frequency jitter info could be modeled by these receiving data. As presented in Fig.3, in MATLAB environment, parameters could be optimized to obtain better demodulation performance.

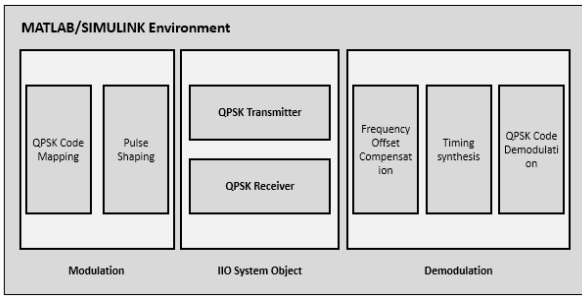

Fig.3. MATLAB/SIMULINK Verification Model.

C. FPGA implementation and hardware validation

After demodulation parameters optimizing steps, modulation and demodulation algorithm could be implemented with High-Level Synthesis (HLS) design. IP-core could be displayed in Fig.4 The width of data interface is 16. One internal message source is built inside of this IP-core and txSrcSelect port could be used to select internal data source or outside data source.

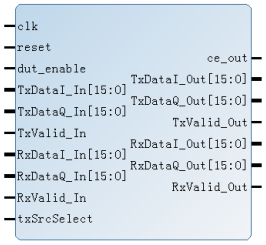

Fig.4. QPSK modulation and demodulation IP-core

ADI provides HDL reference design for the application of AD9361 chips. Hence, this QPSK IP-core need to be integrated to overall HDL design. This IP-core is constrained to run on 10 MHz clock.

Since the algorithm has been verified on hardware, FPGA synthesis and implementation passed without any repeat. Meanwhile, hardware validation results were also ensured.

D. Results

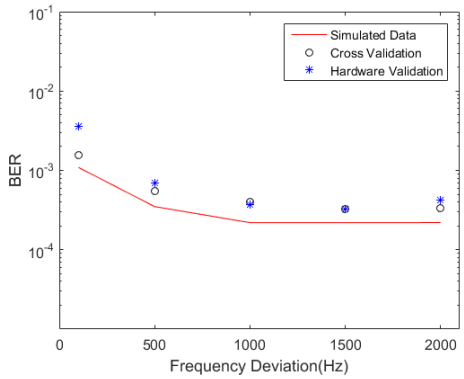

Fig.5. Validation Results

The verification results are presented in Fig. 5. Due to the existence of LO jitter, software simulation results exhibited difference with hardware validation. However, cross validation results were exactly identical with hardware verification results. Meanwhile, on the presented SDR platform, BER is below 10^{-3} which means LO jitter and frequency drift issues are solved to some degree. In this development period, no FPGA synthesis and implementations iterative adjustment is needed to optimize algorithm parameters.

IV. Conclusion

In this paper, an algorithm validation method is proposed to accelerate FPGA based wireless communication algorithm development. A QPSK implementation example is provided to illustrate the new design work follow. This proposed method could be applied to new generation of ARM-FPGA integrated product usage.

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